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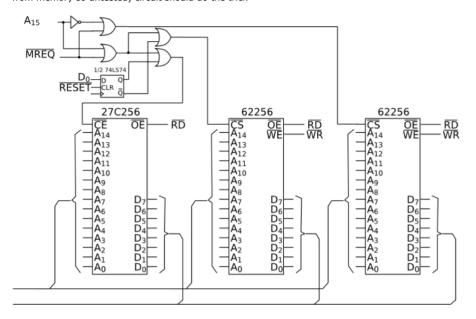
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Welcome, Guest. Please login or register. This topic **∨** | Search Did you miss your activation email? Forever V Login Login with username, password and session length Search About us Links Description Register A Home EEVblog Electronics Community Forum » Electronics » Beginners » Z80 single board memory bank switching Used N9917A FieldFox Handheld Microwave Analyzer, 18 GHz SHOP NOW >> Limited offer 55% off, options addable, calibrated 5 PCBs for \$2, any color L JLCPCB Production of PCB, SMT, Stencil is back to normal « previous next » Pages: Prev 1 2 [3] All Go Down SEARCH Author Topic: Z80 single board memory bank switching (Read 33646 times) 0 Members and 4 Guests are viewing this topic. Re: Z80 single board memory bank grumpydoc switching Super Contributor « Reply #50 on: November 24, 2013, 09:07:27 am » The 74LS138 does not have tri-state outputs, inactive outputs are just at logic 1 so you don't need to worry about pull-up resistors. Posts: 2705 Logged Country: Re: Z80 single board memory bank netdudeuk switching Frequent Contributor « Reply #51 on: November 24, 2013, 09:49:51 am » Posts: 409 Country: Great thanks. « Last Edit: November 24, 2013, 09:58:36 am by netdudeuk » ^{្ត្រា} Logged Re: Simple Z80 memory □ netdudeuk interfacing pt 3 Frequent Contributor « Reply #52 on: July 09, 2017, 10:57:36 am » Posts: 409 Quote from: grumpydoc on July 27, 2013, 04:27:49 pm Country:

OK, so the previous two examples are fine for micro-controller projects but the OP was interested in CP/M. For that you need RAM at low addresses because the TPA (i.e where programs are loaded) starts at 0x0100. Also you really need 64k of RAM if at all possible.

This all provides a bit of a problem, how do we have ROM at address 0 for the initial cold reset and RAM at address 0 when running CP/M? I should point out BTW that for the moment I'm thinking of CP/M 2.2 and below - CP/M 3.0 supported bank switching but it wasn't around the last time I built a machine to run CP/M so I need to go and have a look at how it works.

We need to introduce some ability to switch one bank between ROM & RAM - the following (totally from memory so untested) circuit should do the trick



We now have two 32kx8 SRAM chips plus some additional gating with half a 74LS74 and a couple more OR gates. On reset the flip flop is cleared so the output will be low, this allows the chip select signal to pass to the EPROM. If a "1" is written to the flip-flop then the chip select will pass to the SRAM.

So, after a reset code in the ROM will run - as part of its initialisation it needs to copy some code up into addresses above 0x8000 and then jump to that code - the flip flop can then be switched to allow the whole 64k to be RAM.

I haven't shown how the clock input to the flip-flop is generated, so that can be considered an exercise for the reader $\begin{tabular}{l} \begin{tabular}{l} \begin$

Hope these posts have been helpful.

Hi

Regarding the reset for the flip flop. Assuming that this is also connected to the processor reset pin, will the flip flop outputs always have settled before the processor is ready to read from memory for the first time?

I guess the related question is can you also be sure that the flip flop will always have changed state fast enough for the first memory access after the bank switch request?

I'm using a Z84C0010PEG clocked at 4MHz.

Thanks

Logged L



Super Contributor



Country:

Re: Simple Z80 memory interfacing pt 3

« Reply #53 on: July 11, 2017, 09:44:45 pm »

Quote from: netdudeuk on July 09, 2017, 10:57:36 am

Regarding the reset for the flip flop. Assuming that this is also connected to the processor reset pin, will the flip flop outputs always have settled before the processor is ready to read from memory for the first time?

I guess the related question is can you also be sure that the flip flop will always have changed state fast enough for the first memory access after the bank switch request?

I'm using a Z84C0010PEG clocked at 4MHz.

Thanks

There is plenty of time because reset going low will drive Q high (and \overline{Q} low). For a "normal" reset one holds \overline{RESET} low for at least 3 t-states which, at 750ns with a 4MHZ clock is rather longer than the propagation delay in a 74LS74. Even if one uses the "warm" reset feature (holding \overline{RESET} low just at the rising edge of T1 in an M1 cycle there are three clock cycles before the next read.

Logged

□ netdudeuk

Frequent Contributor



Posts: 409 Country:



Re: Z80 single board memory bank switching

« Reply #54 on: July 12, 2017, 06:22:43 am »

Thanks

Logged L

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