李金澄

University of Electronic Science & Technology of China (UESTC), Chengdu, P. R. China
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教育经历

电子科技大学格拉斯哥学院(中外合办项目) 2022-Present

电子信息工程专业, GPA: 3.81/4.0

排名: Top 18%

英语四级：647， 英语六级：590

IELTS: Total 7 (Listening 8.5, Reading 7, Speaking 6, Writing 6)

学术项目

基于 RISC-V 指令集 RV32I 的 CPU 设计 | UESTC | 课设/比赛作品（集创赛在打） 2024.2–2024.6

- 基于 RV32I 的指令集设计了一个单发射顺序执行 5 级流水的 CPU
- 实现了前递，分支预测， 流水线暂停
- 为后期乱序执行设计引入了简单的 ReorderBuffer
- 使用 Verilog 语言完成作品设计，包括简单的功能验证，以及在 Vivado 平台的综合与实现
- 全英文撰写设计报告，在课设期间每周与负责老师用全英文汇报交流。

SoC 上的 AI 加速器 ASIC 设计 |全国大学生嵌入式芯片与系统设计竞赛——芯片设计赛道 2024.8–2024.12

- 针对一个卷积神经网络 CNN 设计了一个 AI 加速芯片，采用脉动阵列架构。这个 CNN 网络在识别交通标志识别方向能取得 80%的准确度。加速模块通过 NICE 总线连接到蜂鸟 E203 的处理器上，拼成一块 SoC。
- 协助了部分的 RTL 设计与验证。
- 负责后端设计，包括在新思科技的 EDA 上完成综合与物理设计。成功将设计跑到 100MHz 的主频，并完成了 cts 与 placement.在 SMIC 的 40nm 工艺库条件下，面积达到 2.21 cm^2 ，功耗达到 31.3mW
- 作品成功进入决赛，并获得国家级二等奖

CMOS 二级运放设计 | UESTC | 课设 2024.11–Present

- 在 180nm 工艺节点下设计了一款二级运算放大器，并集成到带隙基准电路中。
- 使用了 Cadence EDA 和 Virtuoso ，完成设计与后端版图制作，并进行了仿真。
- 等待 fab 厂流片，回片后会在 PCB 上做测试。

获奖与荣誉

格拉斯哥学院,电子科技大学 UESTC 2022.8–Present

- 学院学业奖学金(三等) (2022.8~2023.8)
- 学院学业奖学金(二等) (2023.8~2024.8)
- 校级优秀学生奖学金 (二等) (2022.8~2023.8)
- 校级优秀学生奖学金 (一等) (2023.8~2024.8)

全国大学生嵌入式芯片与系统设计竞赛——芯片设计赛道 2024.8–2024.12

- 国家级二等奖

RESEARCH INTEREST

- 数字集成电路设计(ASIC)
- 计算机体系架构

技能

EDA: 熟练使用 Xilinx Vivado, Synopsys DC, Cadence Virtuoso.

Programming: 熟练编写 Verilog, C.

Li Jincheng

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EDUCATION

Glasgow College, University of Glasgow 2022-Present

Joint Program with University of Electronic Science & Technology of China (UESTC)

B.E. in Electronic Information Engineering, GPA: 3.81/4.0

Rank: Top 18%

CET4:647, CET6:590

IELTS: Total 7 (Listening 8.5, Reading 7, Speaking 6, Writing 6)

ACADEMIC PROJECTS

32-bit RISC-V CPU Design | UESTC | Course Project 2024.2–2024.6

- Designed a single issue 5-stage pipeline CPU based on RISC-V ISA, including Data forwarding, early-branch resolution
- Implemented stall/flush logic and precise exception logic，branch prediction unit
- Introduced simple reorder buffer for future updating of out-of-order execution design
- Completed the design using Verilog, including simple verification, synthesis on Vivado ISE and FPGA implementation
- Composed a detailed report of the design and reported to course coordinator weekly fully in English

AI Accelerator on SoC ASIC Design | National College Student Chip Design Contest 2024.8–2024.12

- Designed an AI accelerator for convolutional neural network computations, which reaches an accuracy of over 80% on traffic sign recognition. The chip is connected to Hbird E203 SoC through a BUS defined by contest committee
- Assisted in RTL design and verification of the chip, introducing a systolic array architecture
- Led backend design, including synthesis and physical design using Synopsys EDA. Successfully constrained the design to run at 100 MHz and had clock tree and placement. The chip is realized with an area of 2.21 cm^2 and 31.3mW power consumption under 40nm fabrication process (25° C, 1.1V)
- Made it to the final contest and received second prize at national level

Second-Order Operational Amplifier CMOS IC Design | UESTC | Course Project 2024.11–Present

- Designed a CMOS operational amplifier and integrated it into a bandgap circuit, using an 180nm fabrication process.
- Used Cadence Virtuoso for backend layout and performed functional simulations.
- Waiting for fab to tape out and will be doing PCB testing once receiving the chip.

HONORS & AWARDS

Glassgow College, UESTC 2022.8–Present

- College Academic Scholarship (Third Prize) (2022.8~2023.8)
- College Academic Scholarship (Second Prize) (2023.8~2024.8)
- Excellence Scholarship for Outstanding Students (Second Prize) (2022.8~2023.8)
- Excellence Scholarship for Outstanding Students (First Prize) (2023.8~2024.8)

National College Student Embedded System Design Contest- Chip Design, SoCChina 2024.8–2024.12

- National level second prize

RESEARCH INTEREST

- Digital Integrated Circuits Design (ASIC)
- Computer Architecture

SKILLS

EDA Software: Experienced in Xilinx Vivado, Synopsys DC, Cadence Virtuoso.

Programming: Familiar with Verilog, Python, C.

成绩证明

Certificate of Student's Rank and Grade

兹证明：

姓名：李金澄，学号：2022190503031，身份证号：[redacted]为电子科技大学格拉斯哥学院2022级电子信息工程专业本科生，该专业学生人数为246人，该生前5学期成绩为85.96，成绩排名为第46名（18.70%）。

Li Jincheng, Student ID of UESTC: 2022190503031, ID No. [redacted] ranks 46th (18.70%) among in his major Electronics and Electrical Engineering with 246 students. The grade for the last 5 semesters is 85.96.

电子科技大学格拉斯哥学院

学生事务中心

Student Affair Center of Glasgow College, UESTC

2025年03月26日

March, 26th, 2025