

USB2.0 HUB Controller IC

USB 2.0 HIGH SPEED 4-PORT HUB CONTROLLER

SL2.1A

Data Sheet

Data Sheet

CoreChips ShenZhen CO.,Ltd

Table of Contents

Chapter 1 Pin Assignment..... 3

1.1 SL2.1A Pinout 3 1.2 SL2.1A Pin
Definition..... 4

Chapter 2 Function Description..... 5

2.1 Overview 5 2.2 Charging
Support 5

Chapter 3 Electrical Characteristics..... 5

3.1 Extreme working conditions 5 3.2
Scope of work 6 3.3 DC
Characteristics 6 3.4
HS/FS/LS electrical characteristics 6 3.5 ESD
Characteristics 6

Appendix 1 Packaging..... 7

table directory

Table 1: Maximum Ratings..... 5

Table 2: Scope of work..... 6

Table 3: DC Characteristics..... 7

Illustrations

Figure 1: SL2.1A Pinout..... 3

Figure 2: Appendix Package Diagram.....7

Chapter 1 Pin Assignment

SL2.1A Pinout

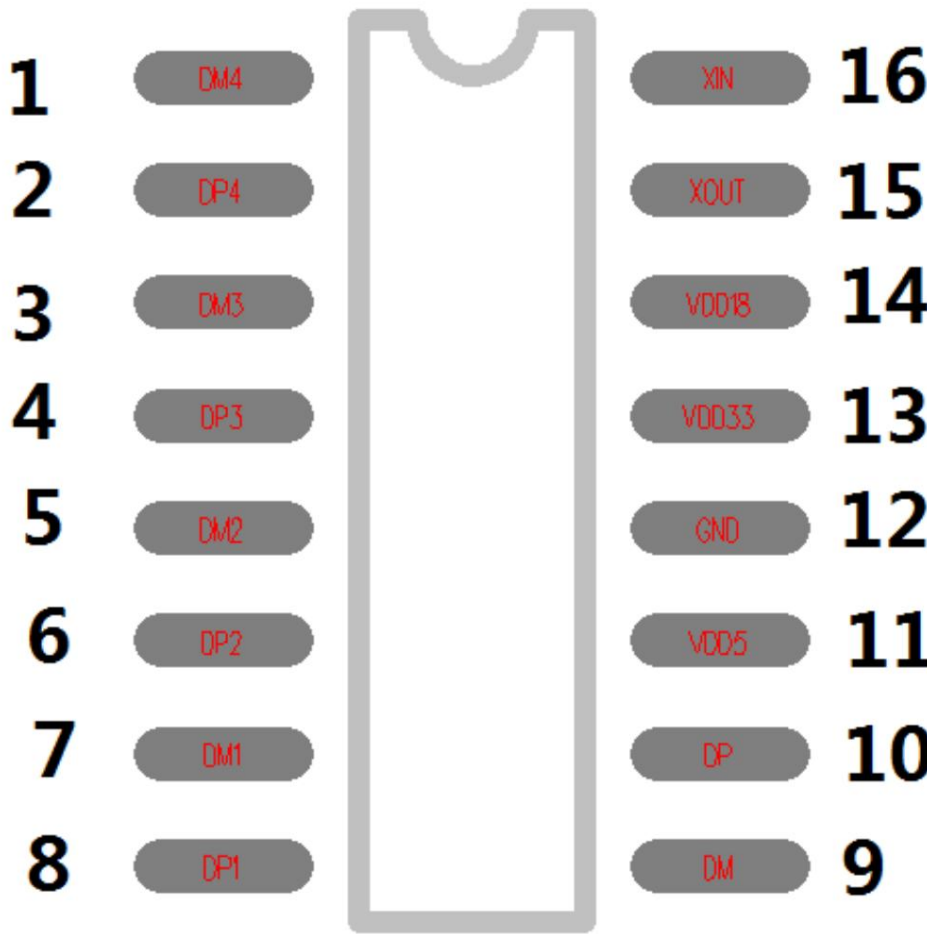


Figure 1: SL2.1A pinout

CoreChips ShenZhen CO.,Ltd

SL2.1A Pin Definition

Pin Name	16 Pin#	Die IO	type	definition
DM4	1		B	USB DM signal of downstream port 4
DP4	2		B	USB DP signal of downstream port 4
DM3	3		B	USB DM signal of downstream port 3
DP3	4		B	USB DP signal of downstream port 3
DM2	5		B	USB DM signal of downstream port 2
DP2	6		B	USB DP signal of downstream port 2
DM1	7		B	USB DM signal of downstream port 1
DP1	8		B	USB DP signal of downstream port 1
DM	9		B	USB DM signal of uplink port
DP	10		B	USB DP signal of the upstream port
VDD5	11		P	5v input
GND	12		P	Chip Ground
VDD33	13		P	Internal 3.3v
VDD18	14		P	Internal 1.8v
XOUT	15		O	Crystal Oscillator PAD
ASK FOR	16		I	

Note: O, output; I input; B bidirectional; P power/ground;

CoreChips ShenZhen CO.,Ltd

Chapter 2 Functional Description

2.1 Overview

SL2.1A is a highly integrated, high-performance, low-power USB2.0 hub controller chip;

Using STT technology, single power supply mode, the chip power supply voltage is 5v, the internal integrated 5V to 3.3V converter only needs

Add filter capacitors to the external power supply; the chip has its own reset circuit, and the low-power technology makes it even more outstanding.

The chip can use either an external crystal or a built-in crystal. If using the built-in crystal, it is required

Connect the XI input of the chip to ground. it is recommended that you use an external crystal oscillator, which is more stable*. *

Perfectly supports **USB2.0 high speed (480MHz)**, **USB2.0** full speed (12MHz), and low speed mode (1.5MHz)

Integrated 12M crystal oscillator

Integrated 12MHz-to-480MHz PPL (Phase Lock Loop)

Using Single Transaction Translator (STT) technology, it is the most cost-effective and efficient solution in the TT series

Supports automatic enumeration switching from self-powered to bus-powered

2.2 Charging support

SL2.1A supports the standard BC1.2 charging protocol.

Chapter 3 Electrical Characteristics

3.1 Extreme working conditions

Table 1: Maximum ratings

symbol	parameter	Minimum	Maximum	Unit
VDDM	Power Supply	-0.5	+5.5	IN
COME	Input Voltage for digital I/O	-0.5	+5.5	IN
VINUSB	Input Voltage for USB signal (DP, DM) pins	-0.5	+3.6	IN
TS	Storage Temperature under bias	-60	+100	°C
FOSC	Frequency	12 MHz ± 0.05%		

CoreChips ShenZhen CO.,Ltd

3.2 Scope of work

Table 2: Scope of work

symbol	parameter	Min	Typical	Max	Unit
VDD	Power Supply	4.0		5.0	5.25 IN
FIND	Input Voltage for digital I/O pins	-0.5		3.3	5.5 IN
VINUSB	Input Voltage for USB signal (DP, DM) pins	0.5		3.3	5.25 V
TA	Ambient Temperature	0			70 °C

3.3 DC characteristics

Table 3: DC characteristics

symbol	parameter	Min.	Typ.	Max.	Unit
IDD	Supply Current	50			120 mA
JESUS	Suspend Current				2.5 mA

3.4 HS/FS/LS electrical characteristics

See USB2.0 standard.

3.5 ESD characteristics

The ESD capability of this chip port is ±4KV (HBM).

Appendix package

SL2.1A SOP16

标注	尺寸	最小 (mm)	最大 (mm)	标注	尺寸	最小 (mm)	最大 (mm)
A		9.80	10.00	C3 ₂		0.05	0.15
A1		0.356	0.456	C4		0.203	0.233
A2		1.27TYP		D		1.05TYP	
A3		0.302TYP		D1		0.40	0.70
B		3.85	3.95	D2		0.15	0.25
B1		5.84	6.24	R1		0.20TYP	
B2		5.00TYP		R2		0.20TYP	
C		1.40	1.60	θ 1		8° ~ 12° TYP4	
C1		0.61	0.71	θ 2		8° ~ 12° TYP4	
C2		0.54	0.64	θ 3		0° ~ 8°	
C3 ₁		0.05	0.25	θ 4		4° ~ 12°	

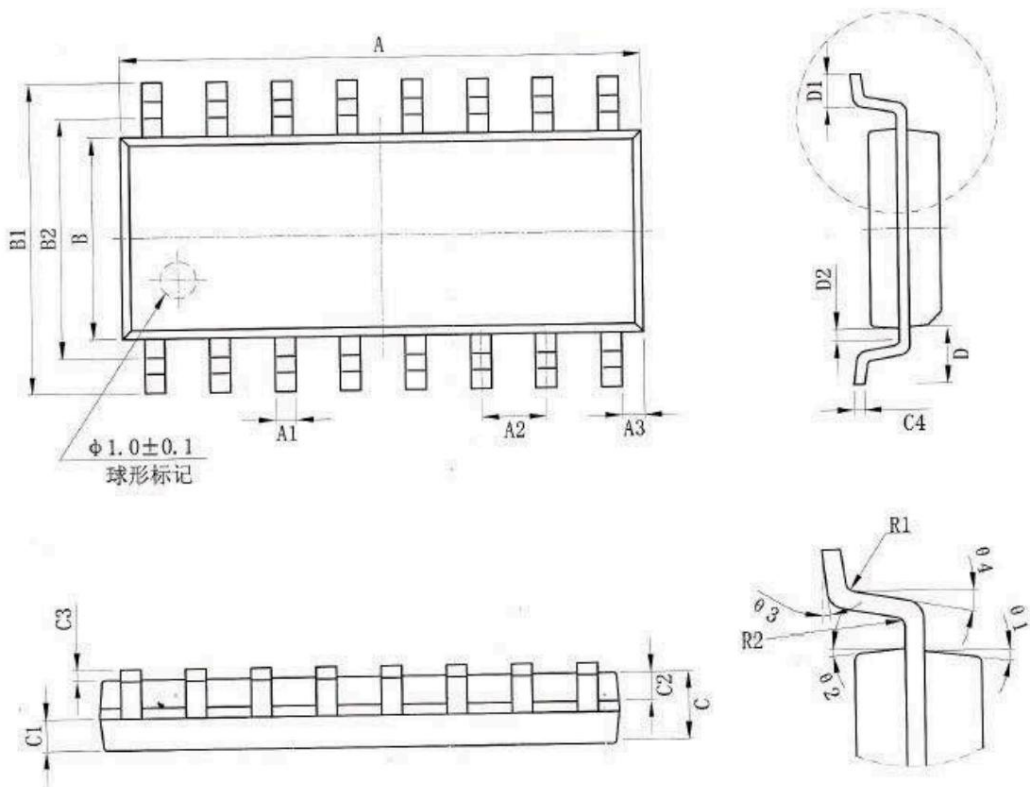


Figure 2: Package size diagram

