VIA Labs, Inc.

Data Sheet

VL811+ (B2)
USB 3.0 Hub Controller

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Revision 1.03

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Revision History

Rev	Date	Initial	Note
0.95	9/20/2012	TS	Added Q4S Package Option
0.96	10/31/2012	TS	Added Ordering Information
1.00	1/30/2013	TS	Added B2 Silicon Revision. Updated USB-IF Certification Information, Updated Core Voltage at 1.2V, Updated Pinout for Q4S Package
1.01	3/11/2013	TS	Updated Pin Descriptions for VL811-Q4S
1.03	10/04/2013	TS	Removed 100K Ohm Requirement for Green/Amber LEDs Clarified Open Drain for OC pins Clarified Test Mode Pin Added Description of Hub FW Update Fail-Safe Mechanism Added Option for Gold Bonding Wire Updated IC Reflow Profile Chart

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VL811+ System Overview

VIA Lab's VL811+ is an advanced USB 3.0 Hub controller featuring low power consumption and comprehensive USB Charging support without the need for external charger ICs. The VL811+ employs an advanced CMOS process and supports USB power management, allowing for improved power-efficient operation. The custom in-house USB PHY gives VL811+ excellent signal integrity characteristics and improved backwards compatibility. VL811+ also features a flexible firmware architecture, providing a framework for custom functions as well as advanced feature support, in addition to in-field updates.

VL811+ based hub devices work under Windows, Mac OS X, and various Linux kernels without additional drivers. Since USB 3.0 hubs do not require additional drivers, VL811+ is also compatible with non-x86 devices and platforms that support USB hub functions such as smart phones, tablets, and set-top boxes. It is well suited for all USB hub applications such as stand alone USB hubs, Notebook/Ultrabook docking stations/port-replicators, desktop PC front panel, motherboard on-board hub, and USB hub compound devices.

With well-planned pinout and a high level of integration, VL811+ based devices enjoy easy layout and simplified BOM. Full sideband signal pins are available for showing power enable, over current, GPIO, and LED status control. The SPI interface supports external EEPROM/Flash ROM which can be updated over USB. VL811+ is available in a 4-port configuration utilizing the QFN 88L package (10x10x0.85 mm) which is pin-compatible with VL810/VL811, and is also available in a 2-port configuration utilizing the QFN 48L (6x6x0.85 mm) package.

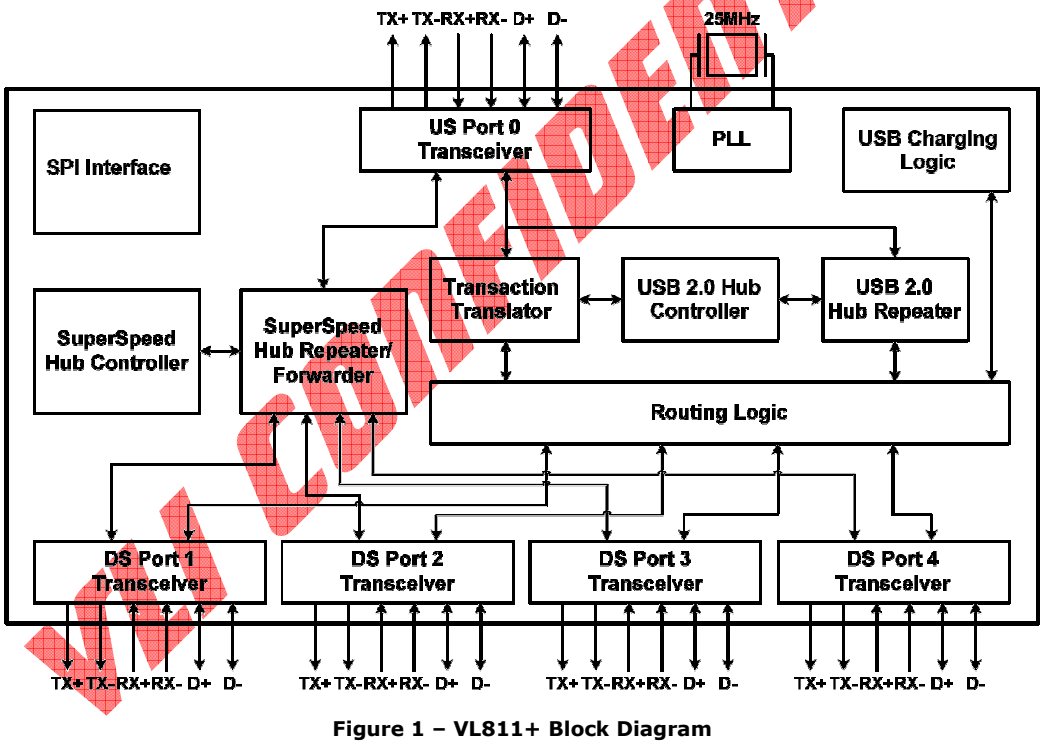


Figure 1 – VL811+ Block Diagram

Rapid Charging over USB in Detail

3 Concepts of Rapid Charging over USB:

- **Rapid Charging over USB enables charging of devices at rates in excess of baseline USB standards.** The current limit of USB 2.0 is 500mA for configured devices, and the current limit of USB 3.0 is 900mA for configured devices. Depending on the device, Rapid Charging implementations typically feature current limits between 1000mA to 2000mA.
- **It is the Host/Hub's responsibility to advertise Rapid Charging capabilities, and it is the Device's responsibility to recognize and determine the Rapid Charging capabilities of the Host/Hub port it is connected to.** Since Rapid Charging over USB allows charging at rates in excess of USB spec, this detection mechanism is necessary to ensure safe and reliable operation, and can prevent situations where a device requests more current than what a host/hub port can supply. Also, this implies that Rapid Charging will only occur when both Host/Hub and Device supports it.
- **The rate at which a device charges is dependant upon the device.** This means that the device must determine the host/hub port's capabilities to determine which charging mode to use. Also, the rate at which a device charges can vary depending on the status of the device. For example, some devices only charge at their maximum rate when the battery is nearly depleted. When the battery is nearly full, they may switch to a trickle-charge mode. The Host/Hub rapid-charging port has no control over this behavior.

Supported USB Charging Modes

SDP – Standard Downstream Port

This is a typical USB 2.0 or USB 3.0 port and does not explicitly support Rapid USB Charging. SDP is constrained to the current limits as defined in the USB 2.0 or USB 3.0 spec which are 500mA and 900mA respectively. While the actual current limit is enforced by the polyfuse or power-switch providing current-limiting functionality for the downstream port, most USB devices will not draw more than 500mA or 900mA under USB 2.0 or USB 3.0 modes.

CDP – Charging Downstream Port

CDP is defined in the USB Battery Charging Specification 1.2 and enables devices that are able to correctly recognize CDP to simultaneously function as a USB device while drawing up to 1.5A for Rapid Charging when connected to the downstream port of a USB Host or Hub that advertises CDP capability.

DCP – Dedicated Charging Port

DCP is defined in the USB Battery Charging Specification 1.2 and has been in use on an unofficial basis prior to the official USB Battery Charging Specification. DCP is a dedicated charging mode, so when a device is charging under DCP, regular USB operations such as data transfer to the device are not supported.

Special Modes

Various vendors such as Apple, RIM, Motorola, etc may employ different detection mechanisms compared to other USB devices and thus, may enter Rapid Charging under the previously mentioned charging modes. VL811+ supports an auto detection mechanism that provides charging for the majority of devices.

Product Features / QFN-88

VL811+
Super-Speed USB Hub Controller

USB 3.0 Compliant
- Compliant to Universal Serial Bus 3.0 Specification Rev 1.0, including Hub errata
- Compliant to Universal Serial Bus Specification Revision 2.0
- Supports simultaneous Super-speed(SS), high-speed (HS), full-speed (FS) traffic, and low-speed (LS) traffic
- Four down-stream ports, one up-stream port
- In-house USB PHY employs advanced CMOS process for low power consumption
- Supports USB Low-Power States such as Ux states and Selective Suspend

Full Sideband Signal Support
- Supports either individual mode or gang mode operation for power enable and over current detection on down-stream ports
- Supports Dual LED status indicators with automatic or manual control via GPIO per down-stream port (Typically Green & Amber)
- 2x GPIO, reserved for special functions

Comprehensive USB Battery Charging Support
- Supports USB Battery Charging Specification v1.2 (SDP, CDP, DCP)
- Adds Support for Vendor Specific Charging Modes eg. Apple, RIM, etc.
- Supports YD/T 1591-2009
- Supports "Sleep Charging" (DCP + Apple Mode)
- Support charging across all down-stream ports, depending on configuration

Physical
- QFN 88L green package (10x10x0.85 mm)
- Pin-to-Pin compatible with VL810, VL811

Certification
- Earned USB 2.0 USB-IF certification
- Earned USB 3.0 USB-IF certification TID# 330000022
- Passed Windows HCK Logo for Windows 8, RT

Applications
- Standalone USB hub
- Desktop/Notebook motherboard on-board hub
- Desktop front panel hub
- Notebook/Ultrabook Docking Station / Port Replicator
- USB hub compound device with keyboard, mouse, display, etc.

Platform and Operating System Support
- General support across all major OS and platforms that offer USB such as PC, MAC, Linux, etc.
- FW Update over USB
- USB hub function is dependent upon the USB Host Controller
- No proprietary driver needed, even for Battery Charging Function

Misc
- Optimized for Low Power consumption
- 3.3 V and 1.2 V power supply
- PLL embedded with external 25MHz crystal
- Support external SPI flash for firmware upgrade

Pinout

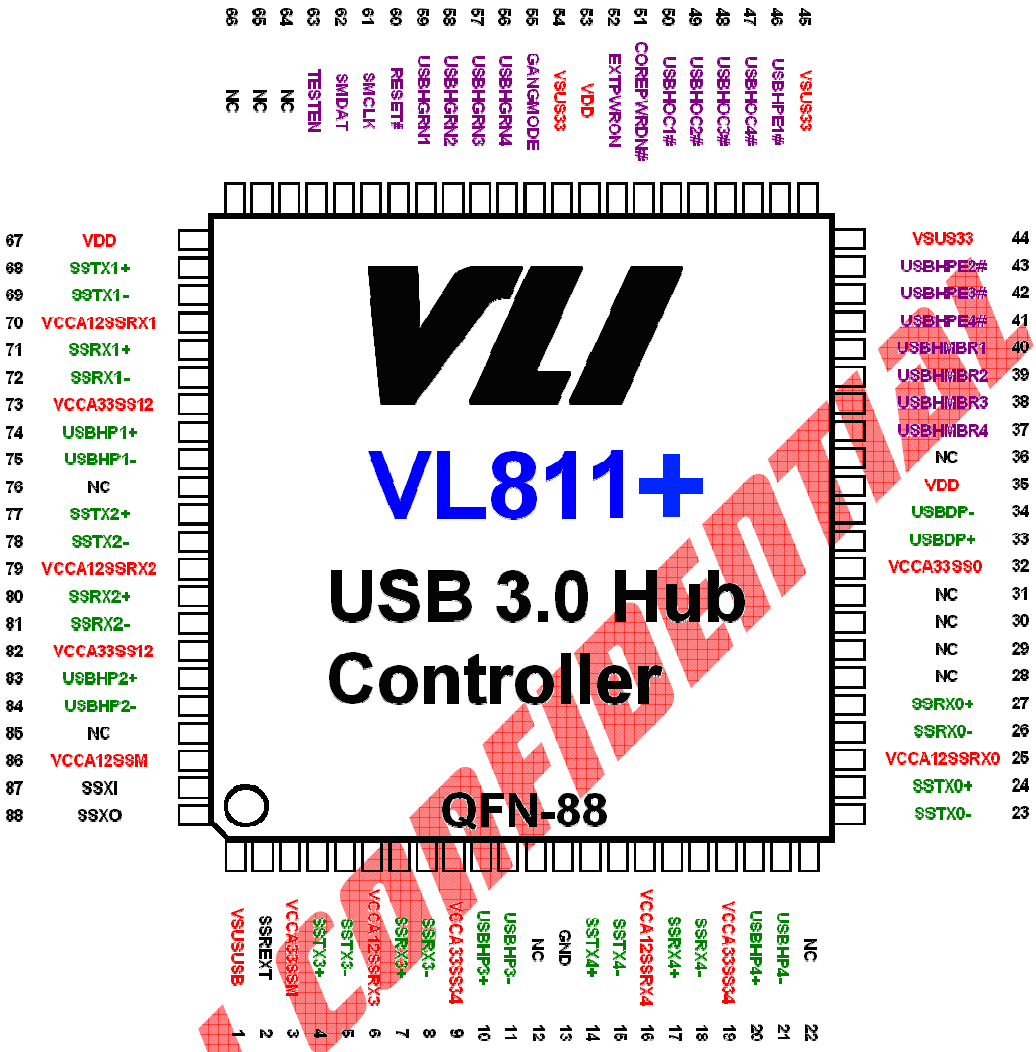


Figure 2 – VL811+ Pin Diagram (QFN-88)

Pin List

Table 1 – VL811+ Pin List (QFN-88)

Pin	Pin Name	Pin	Pin Name
1	VSUSUSB	45	VSUS33
2	SSREXT	46	USBHPE1#
3	VCCA33SSM	47	USBHOC4#
4	SSTX3+	48	USBHOC3#
5	SSTX3-	49	USBHOC2#
6	VCCA12SSRX3	50	USBHOC1#
7	SSRX3+	51	COREPWRDN#
8	SSRX3-	52	EXTPWRON
9	VCCA33SS34	53	VDD
10	USBHP3+	54	VSUS33
11	USBHP3-	55	GANGMODE
12	NC	56	USBHGRN4
13	GND	57	USBHGRN3
14	SSTX4+	58	USBHGRN2
15	SSTX4-	59	USBHGRN1
16	VCCA12SSRX4	60	RESET#
17	SSRX4+	61	SMCLK
18	SSRX4-	62	SMDAT
19	VCCA33SS34	63	TESTEN
20	USBHP4+	64	NC
21	USBHP4-	65	NC
22	NC	66	NC
23	SSTX0-	67	VDD
24	SSTX0+	68	SSTX1+
25	VCCA12SSRX0	69	SSTX1-
26	SSRX0-	70	VCCA12SSRX1
27	SSRX0+	71	SSRX1+
28	NC	72	SSRX1-
29	NC	73	VCCA33SS12
30	NC	74	USBHP1+
31	NC	75	USBHP1-
32	VCCA33SS0	76	NC
33	USBDP+	77	SSTX2+
34	USBDP-	78	SSTX2-
35	VDD	79	VCCA12SSRX2
36	NC	80	SSRX2+
37	USBHMBR4	81	SSRX2-
38	USBHMBR3	82	VCCA33SS12
39	USBHMBR2	83	USBHP2+
40	USBHMBR1	84	USBHP2-
41	USBHPE4#	85	NC
42	USBHPE3#	86	VCCA12SSM
43	USBHPE2#	87	SSXI
44	VSUS33	88	SSXO

Pin Descriptions

Signal Type Definition

Name	Type	Signal Description
Input	I	A logic input-only signal
Output	O	A logic output only signal
Input/Output	I/O	A logic bi-directional signal
Power	PWR	A power pin
Ground	GND	A ground pin

USB 3.0 Interface

Pin Name	Pin #	I/O	Signal Description
SSTX0+	24		USB 3.0 UP Port Differential Transmit Data +
SSTX0-	23		USB 3.0 UP Port Differential Transmit Data -
SSRX0+	27		USB 3.0 UP Port Differential Receive Data +
SSRX0-	26		USB 3.0 UP Port Differential Receive Data -
VCCA12SSRX0	25	PWR	Analog 1.2V
SSTX1+	68		USB 3.0 DP1 Port Differential Transmit Data +
SSTX1-	69		USB 3.0 DP1 Port Differential Transmit Data -
SSRX1+	71		USB 3.0 DP1 Port Differential Receive Data +
SSRX1-	72		USB 3.0 DP1 Port Differential Receive Data -
VCCA12SSRX1	70	PWR	Analog 1.2V
VCCA33SS12	73	PWR	Analog 3.3V
SSTX2+	77		USB 3.0 DP2 Port Differential Transmit Data +
SSTX2-	78		USB 3.0 DP2 Port Differential Transmit Data -
SSRX2+	80		USB 3.0 DP2 Port Differential Receive Data +
SSRX2-	81		USB 3.0 DP2 Port Differential Receive Data -
VCCA12SSRX2	79	PWR	Analog 1.2V
VCCA33SS12	82	PWR	Analog 3.3V
SSTX3+	4		USB 3.0 DP3 Port Differential Transmit Data +
SSTX3-	5		USB 3.0 DP3 Port Differential Transmit Data -
SSRX3+	7		USB 3.0 DP3 Port Differential Receive Data +
SSRX3-	8		USB 3.0 DP3 Port Differential Receive Data -
VCCA12SSRX3	6	PWR	Analog 1.2V
VCCA33SS34	9	PWR	Analog 3.3V
SSTX4+	14		USB 3.0 DP4 Port Differential Transmit Data +
SSTX4-	15		USB 3.0 DP4 Port Differential Transmit Data -
SSRX4+	17		USB 3.0 DP4 Port Differential Receive Data +
SSRX4-	18		USB 3.0 DP4 Port Differential Receive Data -
VCCA12SSRX4	16	PWR	Analog 1.2V
VCCA33SS34	19	PWR	Analog 3.3V
VCCA33SSM	3	PWR	USB 3.0 Master Block Analog 3.3V

USB 2.0 Interface

Pin Name	Pin #	I/O	Signal Description
USBDP+	33		USB 2.0 UP Bus Data Plus (D+)
USBDP-	34		USB 2.0 UP Bus Data Minus (D−)
VCCA33SS0	32	PWR	Analog 3.3V
USBHP1+	74		USB 2.0 DP1 Bus Data Plus (D+)
USBHP1-	75		USB 2.0 DP1 Bus Data Minus (D−)
USBHP2+	83		USB 2.0 DP2 Bus Data Plus (D+)
USBHP2-	84		USB 2.0 DP2 Bus Data Minus (D−)
USBHP3+	10		USB 2.0 DP3 Bus Data Plus (D+)
USBHP3-	11		USB 2.0 DP3 Bus Data Minus (D−)
USBHP4+	20		USB 2.0 DP4 Bus Data Plus (D+)
USBHP4-	21		USB 2.0 DP4 Bus Data Minus (D−)

Analog Command Block

Pin Name	Pin #	I/O	Signal Description
SSXI	87		25M crystal input
SSXO	88		25M crystal output
VCCA12SSM	86	PWR	Analog 1.2V
SSREXT	2		Connect to reference resistor for Super speed mode

Side Band signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
USBHMBR1	40	O	DP1 Amber (Over Current) LED Indicator and SPISO share pin. For LED, Output high when active
USBHMBR2	39	O	DP2 Amber (Over Current) LED Indicator and SPISI share pin. For LED, Output high when active
USBHMBR3	38	O	DP3 Amber (Over Current) LED Indicator / SPISCLK share pin. For LED, Output high when active
USBHMBR4	37	O	DP4 Amber (Over Current) LED Indicator / SPICS# share pin. For LED, Output high when active
USBHGRN1	59	O	DP1 Green (Port Connect) LED Indicator. Output high when active.
USBHGRN2	58	O	DP2 Green (Port Connect) LED Indicator. Output high when active.
USBHGRN3	57	O	DP3 Green (Port Connect) LED Indicator. Output high when active.
USBHGRN4	56	O	DP4 Green (Port Connect) LED Indicator. Output high when active.
USBHPE1#	46	O	DP1 Power Enable. Low: Port Power On. High: Port Power Off.
USBHPE2#	43	O	DP2 Power Enable. Low: Port Power On. High: Port Power Off.
USBHPE3#	42	O	DP3 Power Enable. Low: Port Power On. High: Port Power Off.
USBHPE4#	41	O	DP4 Power Enable. Low: Port Power On. High: Port Power Off.
USBHOC1#	50	I	DP1 Over Current Detect Low: Port Over Current High: Port Power Normal Open Drain
USBHOC2#	49	I	DP2 Over Current Detect Low: Port Over Current High: Port Power Normal Open Drain
USBHOC3#	48	I	DP3 Over Current Detect Low: Port Over Current High: Port Power Normal Open Drain
USBHOC4#	47	I	DP4 Over Current Detect Low: Port Over Current High: Port Power Normal Open Drain
EXTPWRON	52	I	Upstream Port VBUS Detection for Upstream port plug-in
COREPWRDN#	51	O	Core power down (Reserved for controlling external core power switch)
GANGMODE	55	I	Downstream Ports Gang/Individual Mode Select. Low: Downstream ports Individual Power Mode. High: Downstream ports Gang Power Mode.
RESET#	60	I	System reset Low: Reset High: Normal Operation

Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	63	I	Test Mode Enable Pull Low for normal operation. Low: Normal mode. High: Test mode.
SMCLK	61	I	SMBus clock for debug only. It is not a standard SMBus interface. Open Drain
SMDAT	62	I/O	SMBus data for debug only. It is not a standard SMBus interface. Open Drain

Power and Ground

Pin Name	Pin #	I/O	Signal Description
GND	13	GND	Ground
VDD	35,53,67	PWR	1.2V Core power
VSUS33	44,45,54	PWR	3.3V suspend power
VSUSUSB	1	PWR	1.2V suspend power

Product Features (QFN-48)

VL811+
Super-Speed USB Hub Controller

USB 3.0 Compliant
- Compliant to Universal Serial Bus 3.0 Specification Rev 1.0, including Hub errata
- Compliant to Universal Serial Bus Specification Revision 2.0
- Supports simultaneous Super-speed(SS), high-speed (HS), full-speed (FS) traffic, and low-speed (LS) traffic
- Two down-stream ports, one up-stream port
- In-house USB PHY employs advanced CMOS process for low power consumption
- Supports USB Low-Power States such as Ux states and Selective Suspend

Full Sideband Signal Support
- Supports either individual mode or gang mode operation for power enable and over current detection on down-stream ports
- Supports VBus and External Power detect
- Optional Support for LED status indicators
- 2x GPIO, reserved for special functions

Comprehensive USB Battery Charging Support
- Supports USB Battery Charging Specification v1.2 (SDP, CDP, DCP)
- Adds DCP Support
- Adds Support for Vendor Specific Charging Modes eg. Apple, RIM, etc.
- Supports YD/T 1591-2009
- Supports "Sleep Charging" (DCP + Apple Mode)
- Support charging across all down-stream ports, depending on configuration

Physical
- QFN 48 green package (6x6x0.85 mm)

Certification
- Earned USB 2.0 USB-IF certification
- Earned USB 3.0 USB-IF certification
- Passed Windows HCK Logo for Windows 8, RT

Applications
- Standalone USB hub
- Desktop/Notebook motherboard on-board hub
- Integrated Hub in Embedded Devices
- Notebook/Ultrabook Docking Station / Port Replicator
- USB hub compound device with keyboard, mouse, display, etc.

Platform and Operating System Support
- General support across all major OS and platforms that offer USB such as PC, MAC, Linux, etc.
- FW Update over USB
- USB hub function is dependent upon the USB Host Controller
- No proprietary driver needed, even for Battery Charging Function

Misc
- Optimized for Low Power consumption
- 3.3 V and 1.2 V power supply
- PLL embedded with external 25MHz crystal
- Support external SPI flash for firmware upgrade

Pinout

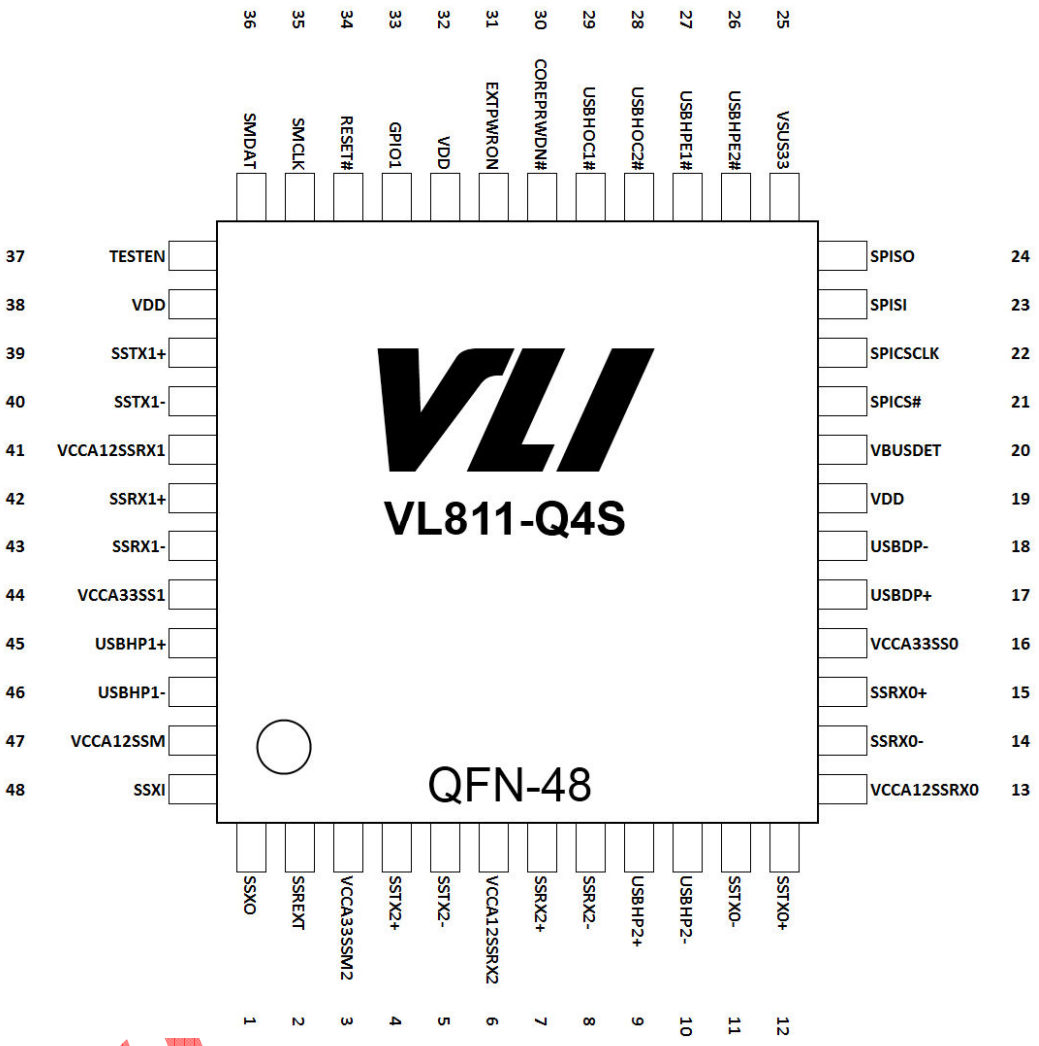


Figure 3 – VL811-Q4S Pin Diagram (QFN-48)

Pin List

Table 2 – VL811-Q4S Pin List (QFN-48)

Pin	Pin Name	Pin	Pin Name
1	SSXO	25	VSUS33
2	SSREXT	26	USBHPE2#
3	VCCA33SSM2	27	USBHPE1#
4	SSTX2+	28	USBHOC2#
5	SSTX2-	29	USBHOC1#
6	VCCA12SSRX2	30	COREPRWDN#
7	SSRX2+	31	EXTPWRON
8	SSRX2-	32	VDD
9	USBHP2+	33	GPIO1
10	USBHP2-	34	RESET#
11	SSTX0-	35	SMCLK
12	SSTX0+	36	SMDAT
13	VCCA12SSRX0	37	TESTEN
14	SSRX0-	38	VDD
15	SSRX0+	39	SSTX1+
16	VCCA33SS0	40	SSTX1-
17	USBDP+	41	VCCA12SSRX1
18	USBDP-	42	SSRX1+
19	VDD	43	SSRX1-
20	VBUSDET	44	VCCA33SS1
21	SPICS#	45	USBHP1+
22	SPICSCLK	46	USBHP1-
23	SPISI	47	VCCA12SSM
24	SPISO	48	SSXI

Pin Descriptions

Signal Type Definition

Name	Type	Signal Description
Input	I	A logic input-only signal
Output	O	A logic output only signal
Input/Output	I/O	A logic bi-directional signal
Power	PWR	A power pin
Ground	GND	A ground pin

USB 3.0 Interface

Pin Name	Pin #	I/O	Signal Description
SSTX0+	12		USB 3.0 UP Port Differential Transmit Data +
SSTX0-	11		USB 3.0 UP Port Differential Transmit Data -
SSRX0+	15		USB 3.0 UP Port Differential Receive Data +
SSRX0-	14		USB 3.0 UP Port Differential Receive Data -
VCCA12SSRX0	13	PWR	Analog 1.2V
SSTX1+	39		USB 3.0 DP1 Port Differential Transmit Data +
SSTX1-	40		USB 3.0 DP1 Port Differential Transmit Data -
SSRX1+	42		USB 3.0 DP1 Port Differential Receive Data +
SSRX1-	43		USB 3.0 DP1 Port Differential Receive Data -
VCCA12SSRX1	41	PWR	Analog 1.2V
SSTX2+	4		USB 3.0 DP2 Port Differential Transmit Data +
SSTX2-	5		USB 3.0 DP2 Port Differential Transmit Data -
SSRX2+	7		USB 3.0 DP2 Port Differential Receive Data +
SSRX2-	8		USB 3.0 DP2 Port Differential Receive Data -
VCCA12SSRX2	6	PWR	Analog 1.2V
VCCA12SSM	47	PWR	Master Block Analog 1.2V

USB 2.0 Interface

Pin Name	Pin #	I/O	Signal Description
USBDP+	17		USB 2.0 UP Bus Data Plus (D+)
USBDP-	18		USB 2.0 UP Bus Data Minus (D–)
VCCA33SS0	16	PWR	Analog 3.3V
USBHP1+	45		USB 2.0 DP1 Bus Data Plus (D+)
USBHP1-	46		USB 2.0 DP1 Bus Data Minus (D–)
VCCA33SS1	44	PWR	Analog 3.3V
USBHP2+	9		USB 2.0 DP2 Bus Data Plus (D+)
USBHP2-	10		USB 2.0 DP2 Bus Data Minus (D–)
VCCA33SSM2	3	PWR	Master Block Analog 3.3V

Analog Command Block

Pin Name	Pin #	I/O	Signal Description
SSXI	48		25M crystal input
SSXO	1		25M crystal output
SSREXT	2		Connect to reference resistor for Super speed mode

Side Band signal and Miscellaneous

Pin Name	Pin #	I/O	Signal Description
SPISO	24	O	SPISO
SPISI	23	O	SPISI
SPICLK	22	O	SPISCLK
SPICS#	21	O	SPICS#
USBHPE1#	27	O	DP1 Power Enable. Low: Port Power On. High: Port Power Off.
USBHPE2#	26	O	DP2 Power Enable. Low: Port Power On. High: Port Power Off.
USBHOC1#	29	I	DP1 Over Current Detect Low: Port Over Current High: Port Power Normal Open Drain
USBHOC2#	28	I	DP2 Over Current Detect Low: Port Over Current High: Port Power Normal Open Drain
EXTPWRON	31	I	External Power Source Presence Detect
COREPWRDN#	30	O	Core power down (Reserved for controlling external core power switch)
RESET#	34	I	System Reset Low: Reset High: Normal Operation
VBUSDET	20	I	5V USB VBus Presence Detect
GPIO1	33	I/O	GPIO Pin reserved for special function

Test Pin

Pin Name	Pin #	I/O	Signal Description
TESTEN	37	I	Test Mode Enable Pull Low for normal operation. Low: Normal mode. High: Test mode.
SMCLK	35	I	SMBus clock for debug only. It is not a standard SMBus interface. Open Drain
SMDAT	36	I/O	SMBus data for debug only. It is not a standard SMBus interface. Open Drain

Power and Ground

Pin Name	Pin #	I/O	Signal Description
VDD	19,32,38	PWR	1.2V Core power
VSUS33	25	PWR	3.3V suspend power

Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
V_{33}	3.3V Power Supply Voltage	-0.5	3.63	V	—
V_{12}	1.2V Input Voltage	-0.5	1.26	V	—
V_{IN}	Input voltage at I/O pins	-0.5	(≦ 3.63) and (≦ V_{33}+0.3)	V	—
V_{ESD}	Electrostatic Discharge	-2000	2000	V	Human Body Model
θ_{jc}	Thermal resistance between junction and case		● For 4-layer PCB: 9.1 ● For 2-layer PCB: 11.3	°C/W	2L & 4L PCB definitions follow JESD51-7
θ_{ja}	Thermal resistance between junction and ambient		● For 4-layer PCB: 21.8 ● For 2-layer PCB: 56.8	°C/W	
P_D	Max Power Dissipation	—	1.0 0.6	W	Q8P 4-Port Q4S 2-Port

Note: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.

Note: About thermal factors, T_a is the concerned ambient temperature, and
$\theta_{ca} = \theta_{ja} - \theta_{jc}$
$T_J = \theta_{ja} * P_D + T_a$
$T_c = \theta_{ca} * P_D + T_a$

Operating Conditions

Symbol	Parameter	Min	Max	Unit	Note
T_A	Ambient Temperature	0	70	°C	—
T_j	Junction Temperature	0	125	°C	—
V_{33}	3.3V Power Supply Voltage	3.0	3.6	V	—
V_{10}	1.2V Input Voltage	1.14	1.25	V	1.2 Nominal
V_{IL}	Input Low Voltage	—	0.8	V	—
V_{IH}	Input High Voltage	2.0	—	V	—
V_{OL}	Output Low Voltage	—	0.4	V	I_{OL}=4mA
V_{OH}	Output High Voltage	2.4	—	V	I_{OH}=4mA
I_{IL}	Input Leakage Current	—	+/-10	µA	$0<V_i<V_{33}$
I_{OZ}	Tristate Leakage Current	—	+/-20	µA	$0<V_o<V_{33}$

Timing Requirements for SPI Flash

SPI flash ROM is used to store the FW data for VL811+. Timing guidelines are provided to assist in selection of appropriate and compatible SPI flash. To ensure SPI flash suitability, not only should the timing requirements conform to the provided guidelines, but actual testing with VL811+ should also be done.

VL811+ has a built-in FW Update Fail-Safe mechanism where if a FW update fails, VL811+ can still continue to function normally by loading a Backup FW. In order to utilize this feature, two conditions must be met: The SPI Flash ROM must support either Page or Block erase instead of just Chip Erase, and the software tool used to program/update VL811+ must also be aware of this feature.

Symbol	Parameters	Condition	Value	Unit
f_{CT}	Clock Frequency for fast read mode(*)	Max value must larger than	15	MHz
f_{C}	Clock Frequency for read mode	Max value must larger than	15	MHz
t_{RI}	Input Rise time	Max value must larger than	5	ns
t_{FI}	Input Fall time	Max value must larger than	5	ns
t_{CKH}	SCK High Time	Min value must smaller than	20	ns
t_{CKL}	SCK Low Time	Min value must smaller than	20	ns
t_{CEH}	CE# High Time	Min value must smaller than	100	ns
t_{CS}	CE# Setup Time	Min value must smaller than	20	ns
t_{CH}	CE# Holde Time	Min value must smaller than	100	ns
t_{DS}	Data In Setup Tiime	Min value must smaller than	20	ns
t_{DH}	Data In Hold Time	Min value must smaller than	20	ns
t_{HS}	Hold Setup Time	Not Utilized		
t_{HD}	Hold Time	Not Utilized		
t_{V}	Output Valid	Max value must smaller than	20	ns
t_{OH}	Output Hold Time Normal Mode	Not Utilized		
t_{LZ}	Hold to Output Low Z	Not Utilized		
t_{HZ}	Hold to Output High Z	Not Utilized		
t_{DIS}	Output Disable Time	Not Utilized		
t_{EC}	Erase Time	Max value must smaller than	100	ms
t_{PP}	Page Program Time	Max value must smaller than	100	ms
t_{VCS}	Vcc Setup Time	Min value must smaller than	1	ms
t_{w}	Write Status Register Time (Flash bit)	Max value must smaller than	100	ms

*Fast read mode must be supported.

SERIAL INPUT/OUTPUT TIMING

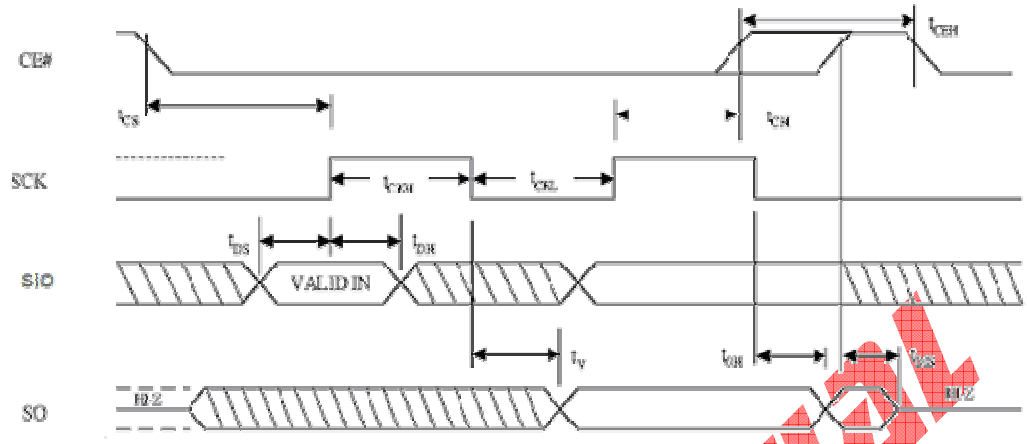


Figure 4 – Illustration of SPI Flash Interface Timing – (1)

HOLD TIMING

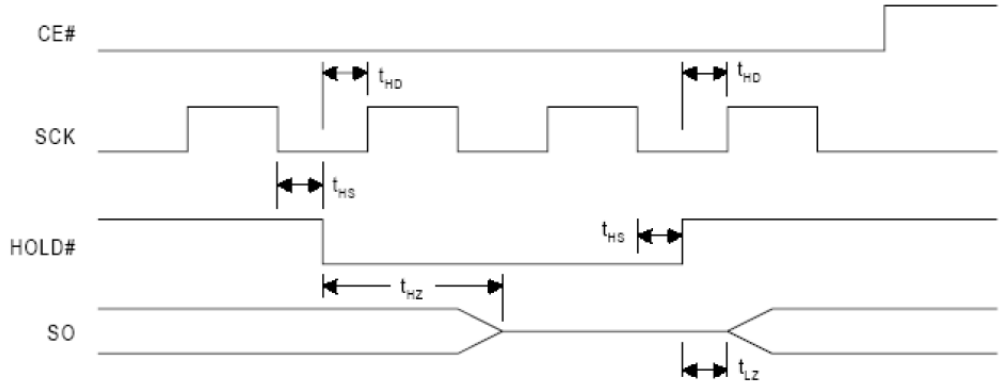
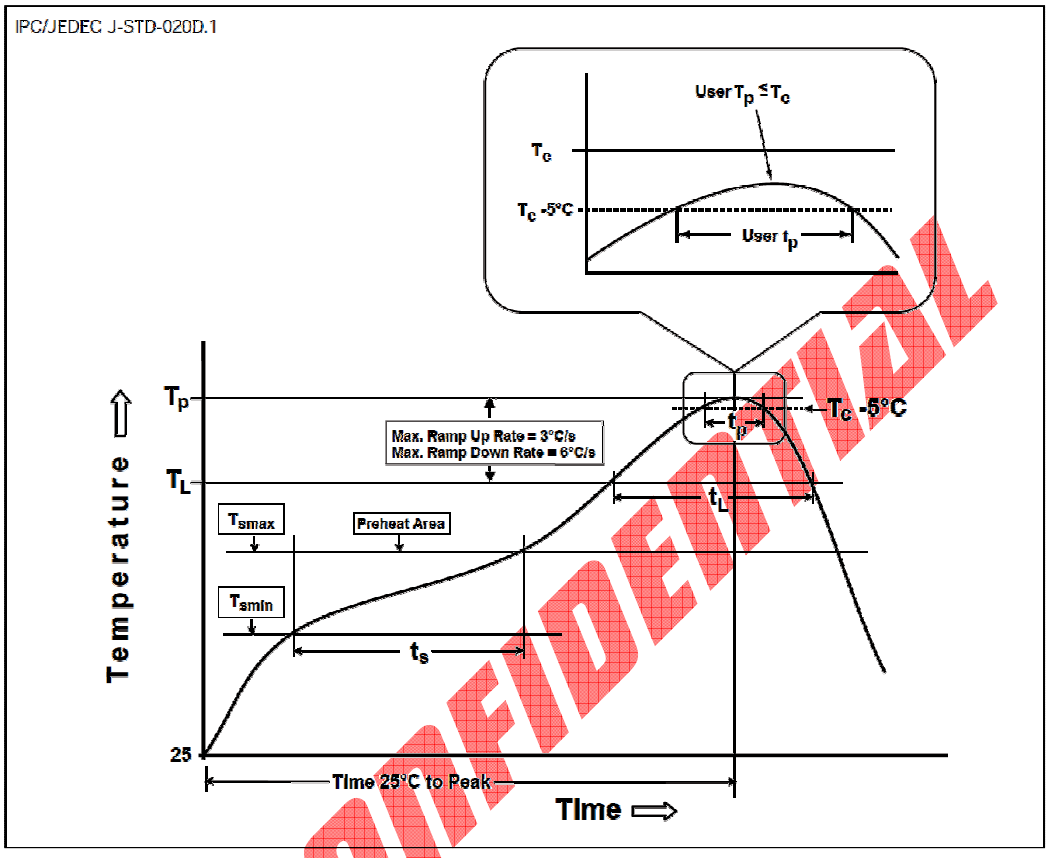


Figure 5 – Illustration of SPI Flash Interface Timing – (2)

General Reflow Profile Guidelines.

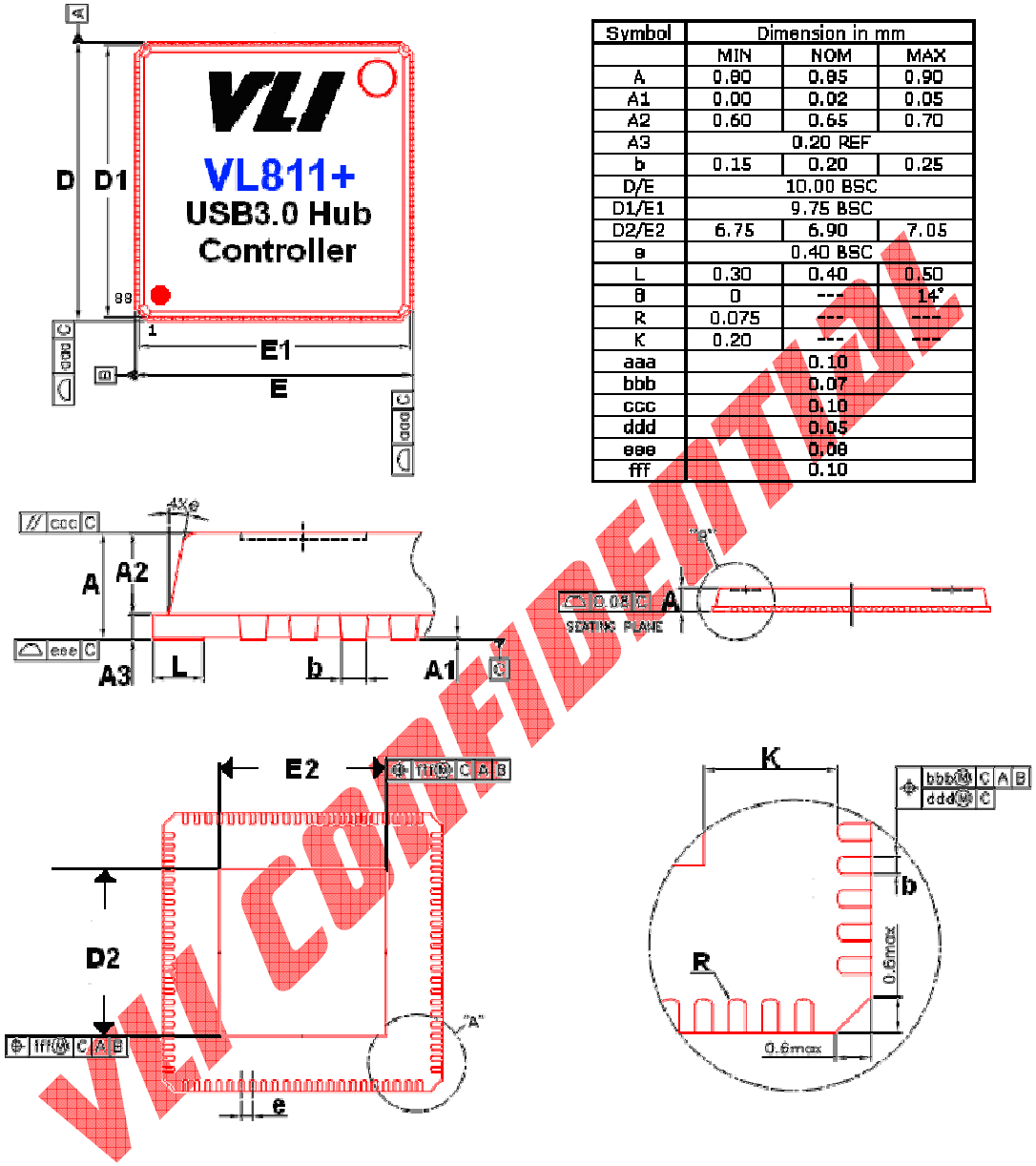


Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	225 °C	250 °C
Classification temperature (T_c)	230 °C	255 °C
Time (t_p)* within 5 °C of the specified classification temperature (T_c)	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug).

Figure 6 –Reflow

Package Mechanical Specifications (QFN-88)



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3		0.20 REF	
b	0.15	0.20	0.25
D/E		10.00 BSC	
D1/E1		9.75 BSC	
D2/E2	6.75	6.90	7.05
e		0.40 BSC	
L	0.30	0.40	0.50
θ	0	---	14°
R	0.075	---	---
K	0.20	---	---
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure 7 – Mechanical Specification – QFN 88L 10x10x0.85 mm Package

Package Top Side Marking & Ordering Information

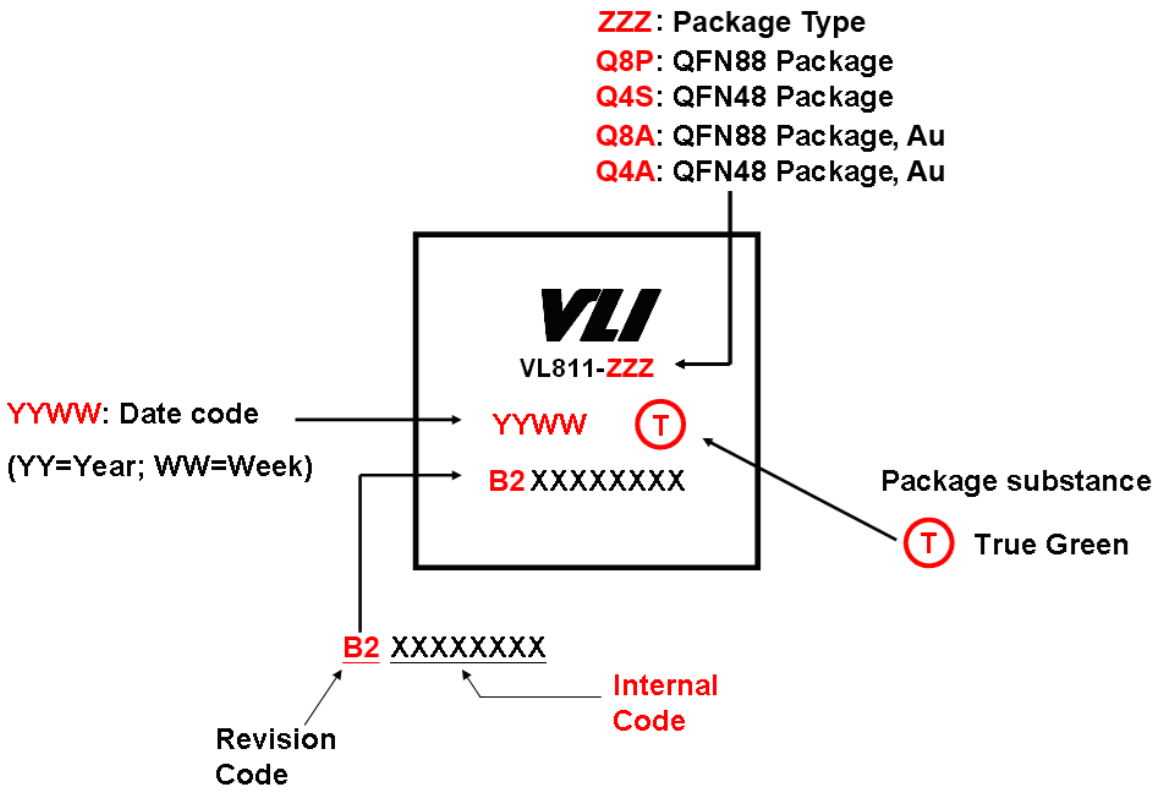
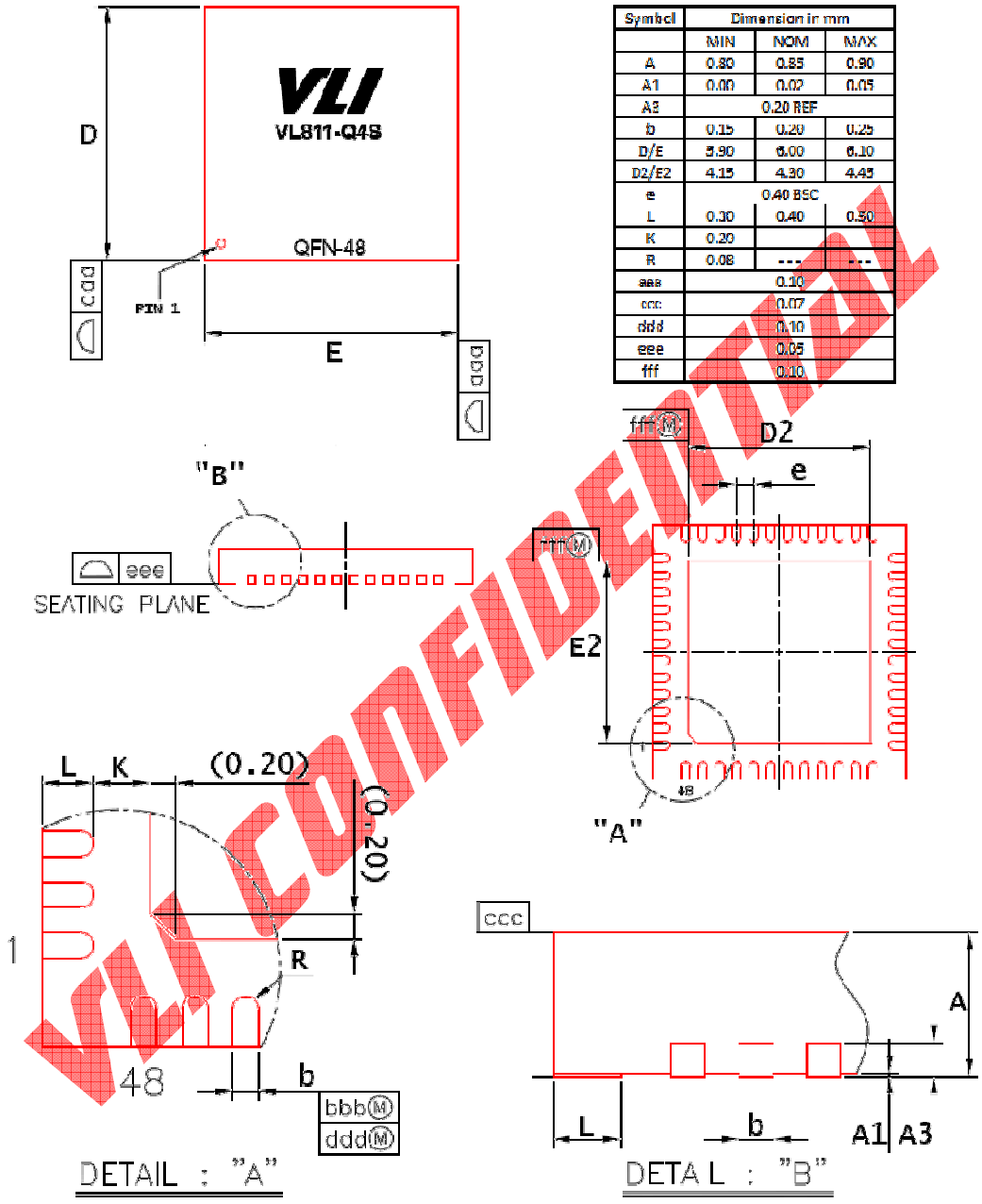


Figure 8 –Package Top Side Marking

Ordering Information	Description	Package Type
VL811-Q8P (B2)	4-Port Hub	QFN88 10x10 mm
VL811-Q4S	2-Port Hub	QFN48 6x6 mm
VL811-Q8A	4-Port Hub, Au Bonding Wire	QFN88 10x10 mm
VL811-Q4A	2-Port Hub, Au Bonding Wire	QFN48 6x6 mm

Package Mechanical Specifications (QFN-48)



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D/E	5.90	6.00	6.10
D2/E2	4.15	4.30	4.45
e		0.40 BSC	
L	0.30	0.40	0.50
K	0.20		
R	0.08	---	---
aaa		0.10	
ccc		0.07	
ddd		0.10	
eee		0.05	
fff		0.10	

Figure 9 – Mechanical Specification –QFN 48 6x6x0.85 mm Package

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