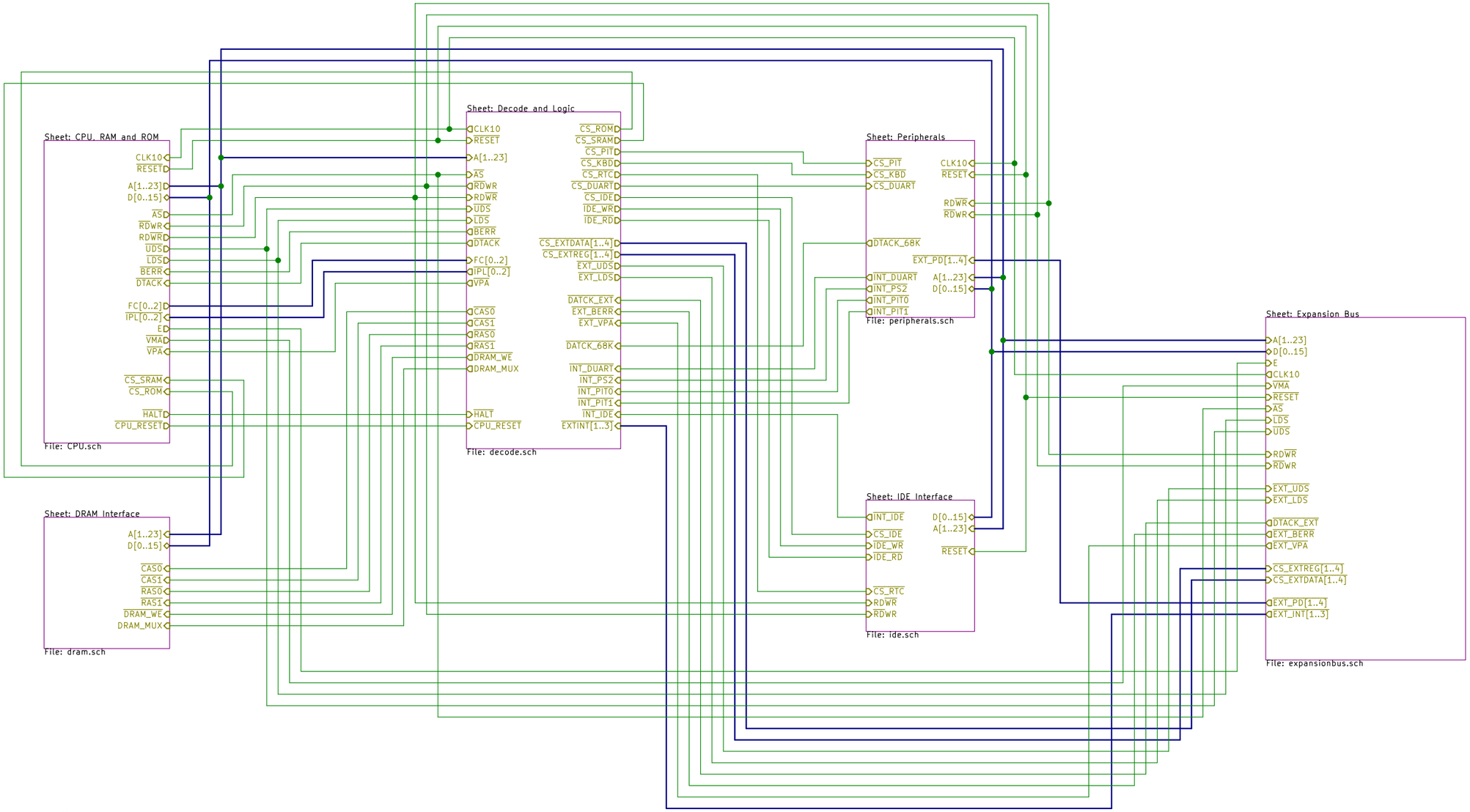
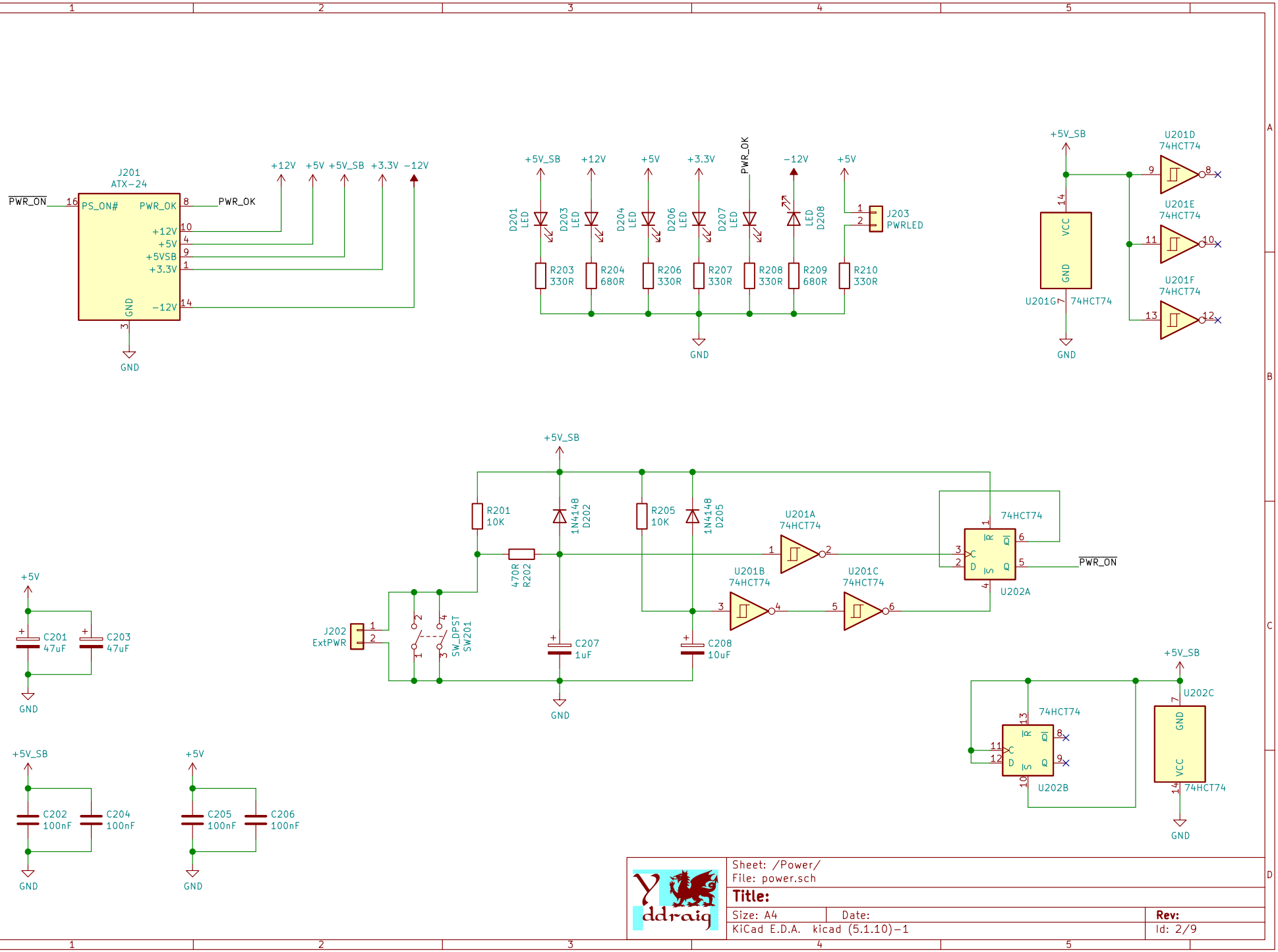
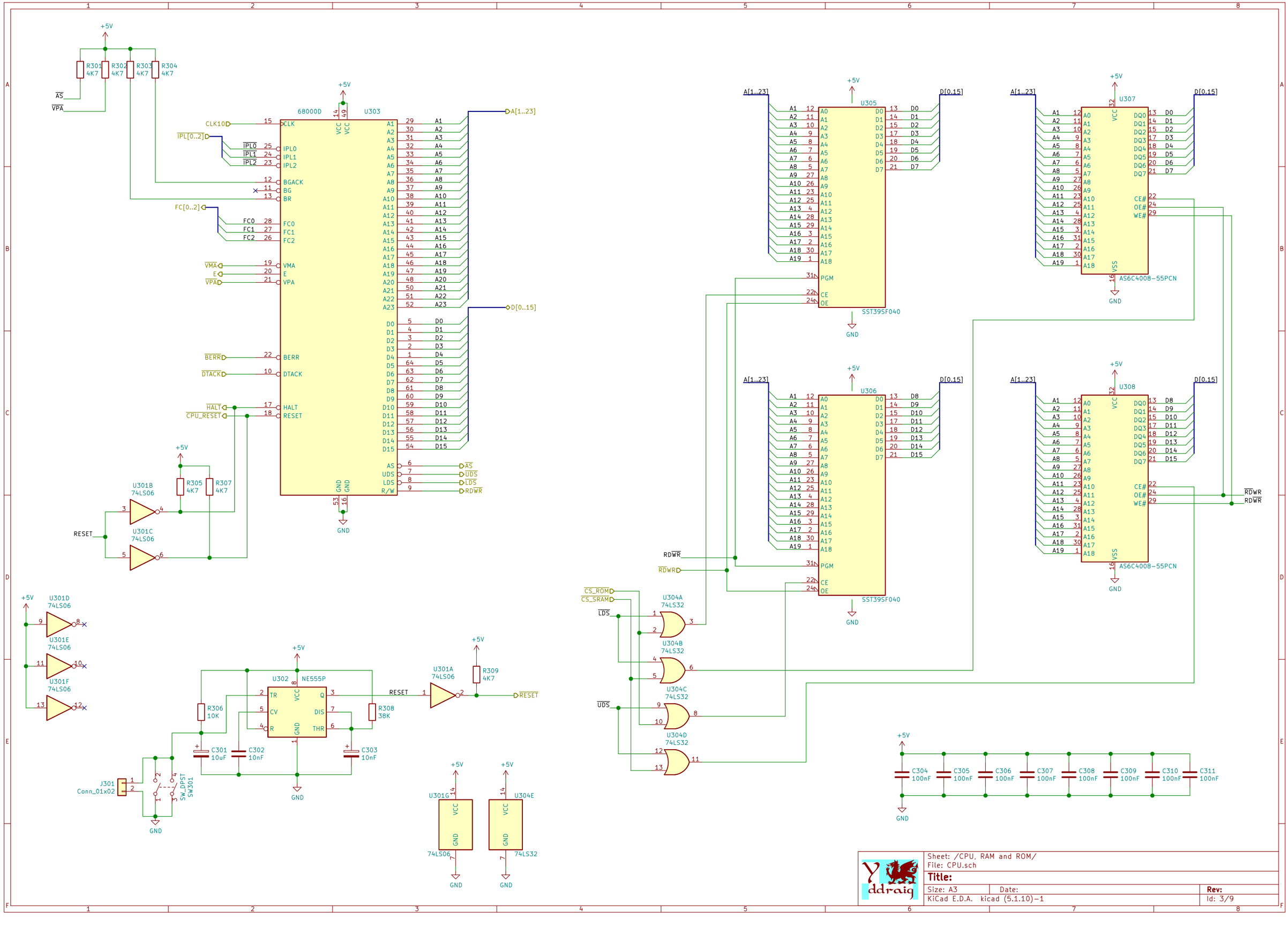
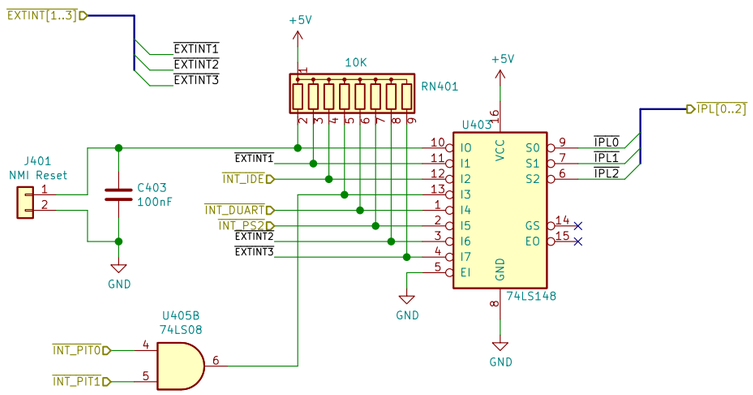
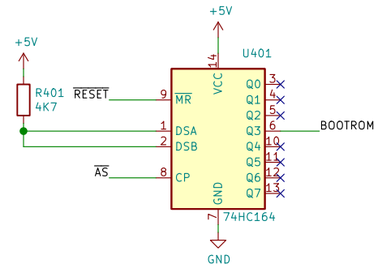
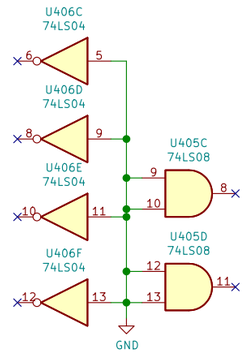

Sheet: CPU, RAM and ROM
CLK10
RESET
A[1..23]
D[0..15]
AS
RDWR
RDWR
UDS
LDS
BERR
DTACK
FC[0..2]
IPL[0..2]
E
VMA
VPA
CS_SRAM
CS_ROM
HALT
CPU_RESET
File: CPU.sch
Sheet: Decode and Logic
CLK10
RESET
A[1..23]
AS
RDWR
RDWR
UDS
LDS
BERR
DTACK
FC[0..2]
IPL[0..2]
VPA
CAS0
CAS1
RAS0
RAS1
DRAM_WE
DRAM_MUX
HALT
CPU_RESET
CS_ROM
CS_SRAM
CS_PIT
CS_KBD
CS_RTC
CS_DUART
CS_IDE
IDE_WR
IDE_RD
CS_EXTDATA[1..4]
CS_EXTREG[1..4]
EXT_UDS
EXT_LDS
DATCK_EXT
EXT_BERR
EXT_VPA
DATCK_68K
INT_DUART
INT_PS2
INT_PIT0
INT_PIT1
INT_IDE
EXTINT[1..3]
File: decode.sch
Sheet: Peripherals
CS_PIT
CS_KBD
CS_DUART
CLK10
RESET
RDWR
RDWR
DTACK_68K
EXT_PD[1..4]
INT_DUART
INT_PS2
INT_PIT0
INT_PIT1
A[1..23]
D[0..15]
File: peripherals.sch
Sheet: Expansion Bus
A[1..23]
D[0..15]
E
CLK10
VMA
RESET
AS
LDS
UDS
RDWR
RDWR
EXT_UDS
EXT_LDS
DTACK_EXT
EXT_BERR
EXT_VPA
CS_EXTREG[1..4]
CS_EXTDATA[1..4]
EXT_PD[1..4]
EXT_INT[1..3]
File: expansionbus.sch
Sheet: IDE Interface
INT_IDE
CS_IDE
IDE_WR
IDE_RD
CS_RTC
RDWR
RDWR
D[0..15]
A[1..23]
RESET
File: ide.sch
Sheet: DRAM Interface
A[1..23]
D[0..15]
CAS0
CAS1
RAS0
RAS1
DRAM_WE
DRAM_MUX
File: dram.sch
Sheet: Power
File: power.sch
H101
MountingHole
H102
MountingHole
H103
MountingHole
H104
MountingHole
H105
MountingHole
H106
MountingHole
Sheet: /
File: yddraig68k.sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad (5.1.10)-1
Id: 1/9

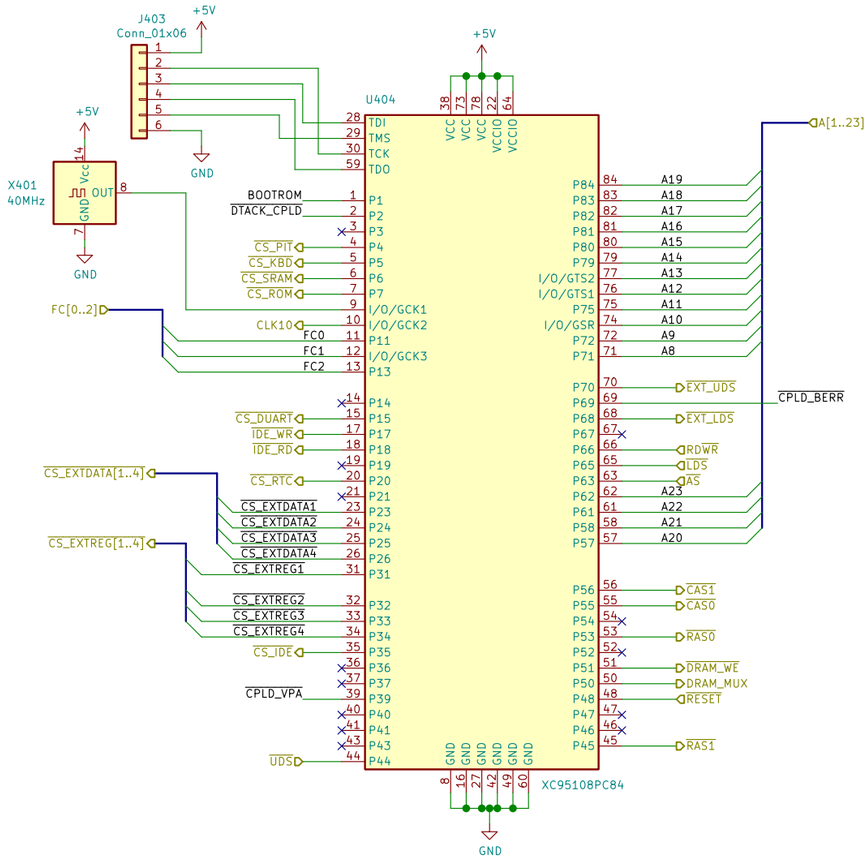

J201
ATX-24
PWR_ON
PS_ON#
PWR_OK
+12V
+5V
+5VSB
+3.3V
GND
−12V
+12V +5V +5V_SB +3.3V −12V
+5V_SB +12V +5V +3.3V PWR_OK −12V +5V
D201 LED
D203 LED
D204 LED
D206 LED
D207 LED
D208 LED
R203 330R
R204 680R
R206 330R
R207 330R
R208 330R
R209 680R
R210 330R
J203 PWRLED
U201D 74HCT74
U201E 74HCT74
U201F 74HCT74
U201G 74HCT74
VCC
GND
J202 ExtPWR
SW_DPST SW201
R201 10K
R205 10K
470R R202
1N4148 D202
1N4148 D205
U201A 74HCT74
U201B 74HCT74
U201C 74HCT74
74HCT74
U202A
PWR_ON
C201 47uF
C203 47uF
C202 100nF
C204 100nF
C205 100nF
C206 100nF
C207 1uF
C208 10uF
U202B
U202C
Yddraig
Sheet: /Power/
File: power.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.10)-1
Id: 2/9

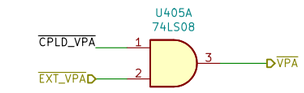

+5V
R301 4K7
R302 4K7
R303 4K7
R304 4K7
AS
VPA
68000D
U303
CLK10
IPL[0..2]
IPL0
IPL1
IPL2
BGACK
BG
BR
FC[0..2]
FC0
FC1
FC2
VMA
E
VPA
BERR
DTACK
HALT
RESET
CPU_RESET
VCC
GND
A[1..23]
D[0..15]
AS
UDS
LDS
R/W
RDWR
U301B 74LS06
U301C 74LS06
R305 4K7
R307 4K7
U301D 74LS06
U301E 74LS06
U301F 74LS06
U302 NE555P
TR
CV
R
Q
DIS
THR
R306 10K
R308 38K
C301 10uF
C302 10nF
C303 10nF
U301A 74LS06
R309 4K7
RESET
J301 Conn_01x02
SW301 SW_DPST
U301G 74LS06
U304E 74LS32
U305 SST39SF040
U306 SST39SF040
U307 AS6C4008-55PCN
U308 AS6C4008-55PCN
PGM
CE
OE
CE#
OE#
WE#
CS_ROM
CS_SRAM
U304A 74LS32
U304B 74LS32
U304C 74LS32
U304D 74LS32
C304 100nF
C305 100nF
C306 100nF
C307 100nF
C308 100nF
C309 100nF
C310 100nF
C311 100nF
Sheet: /CPU, RAM and ROM/
File: CPU.sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad (5.1.10)-1
Id: 3/9

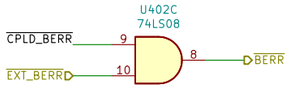

EXTINT[1..3]
EXTINT1
EXTINT2
EXTINT3
+5V
10K
RN401
U403
74LS148
IPL[0..2]
IPL0
IPL1
IPL2
J401
NMI Reset
C403
100nF
GND
INT_IDE
INT_DUART
INT_PS2
U405B
74LS08
INT_PIT0
INT_PIT1

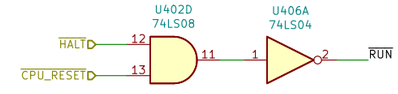

+5V
U401
R401
4K7
RESET
BOOTROM
AS
74HC164
GND

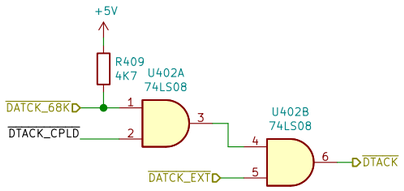

U406C
74LS04
U406D
74LS04
U406E
74LS04
U406F
74LS04
U405C
74LS08
U405D
74LS08
GND

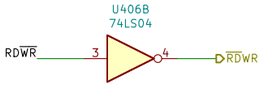

J403
Conn_01x06
+5V
GND
X401
40MHz
U404
XC95108PC84
BOOTROM
DTACK_CPLD
CS_PIT
CS_KBD
CS_SRAM
CS_ROM
FC[0..2]
CLK10
FC0
FC1
FC2
CS_DUART
IDE_WR
IDE_RD
CS_RTC
CS_EXTDATA[1..4]
CS_EXTREG[1..4]
CS_IDE
CPLD_VPA
UDS
A[1..23]
EXT_UDS
EXT_LDS
RDWR
LDS
AS
CPLD_BERR
CAS1
CAS0
RAS0
DRAM_WE
DRAM_MUX
RESET
RAS1

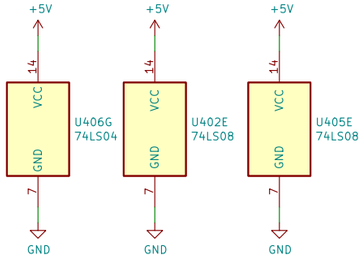

U405A
74LS08
CPLD_VPA
EXT_VPA
VPA

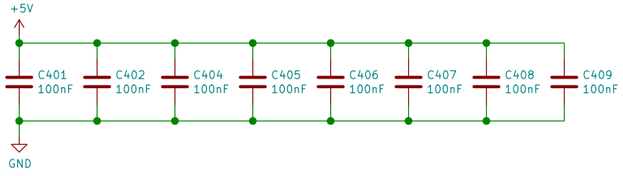

U402C
74LS08
CPLD_BERR
EXT_BERR
BERR

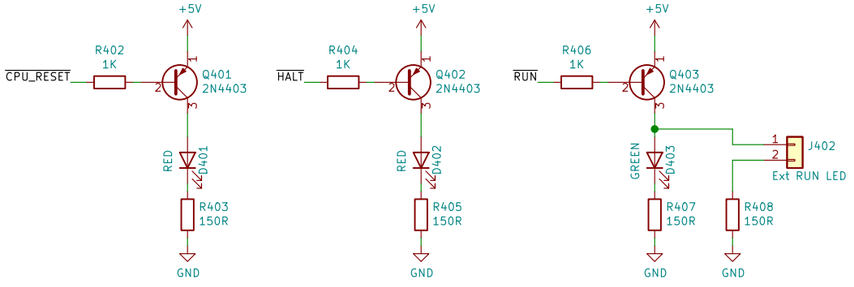

U402D
74LS08
U406A
74LS04
HALT
CPU_RESET
RUN

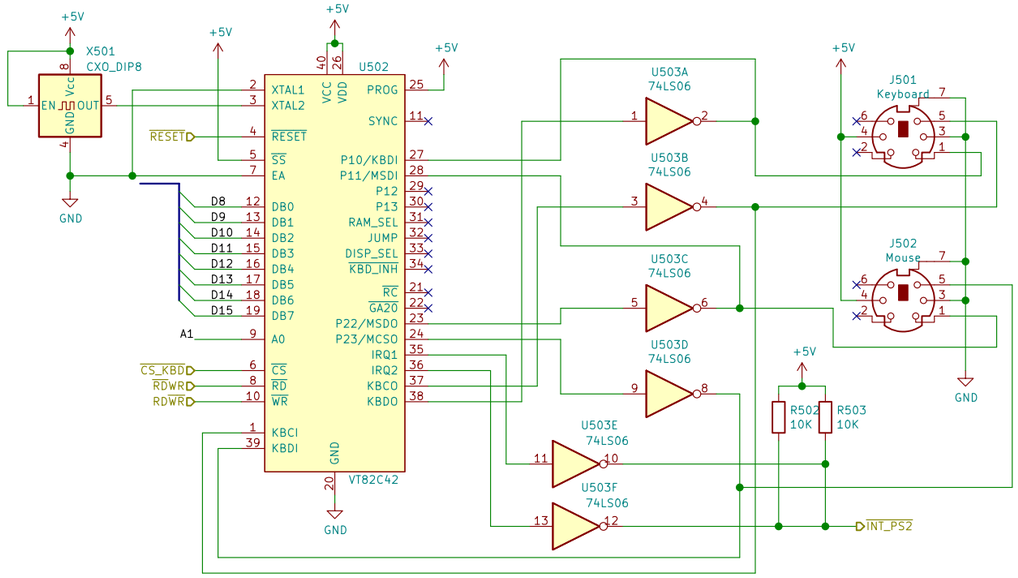

+5V
R409
4K7
U402A
74LS08
U402B
74LS08
DATCK_68K
DTACK_CPLD
DATCK_EXT
DTACK

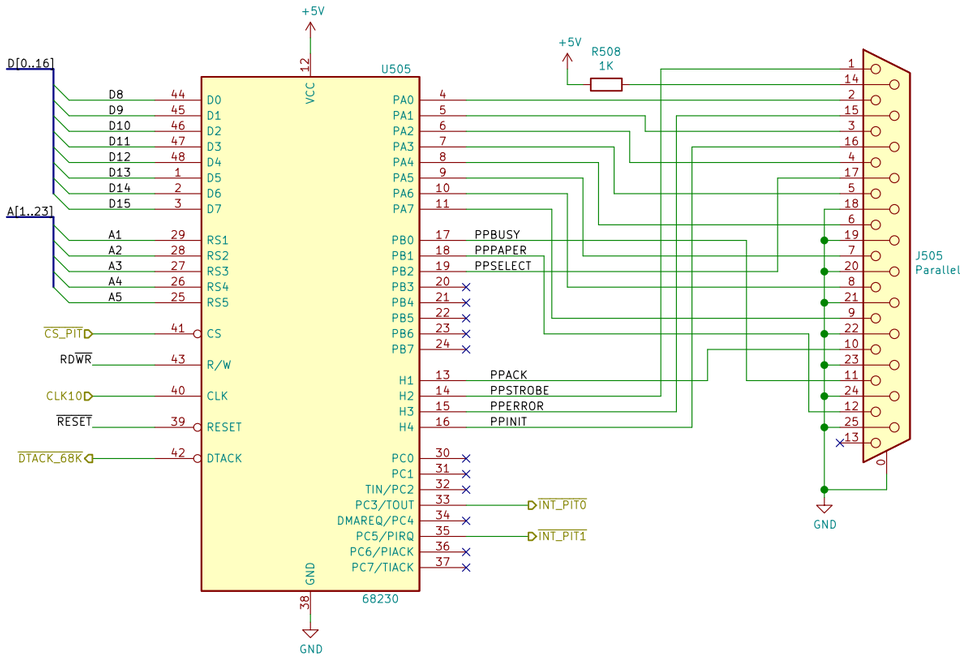

U406B
74LS04
RDWR

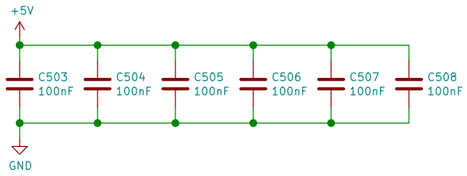

+5V
U406G
74LS04
U402E
74LS08
U405E
74LS08
GND

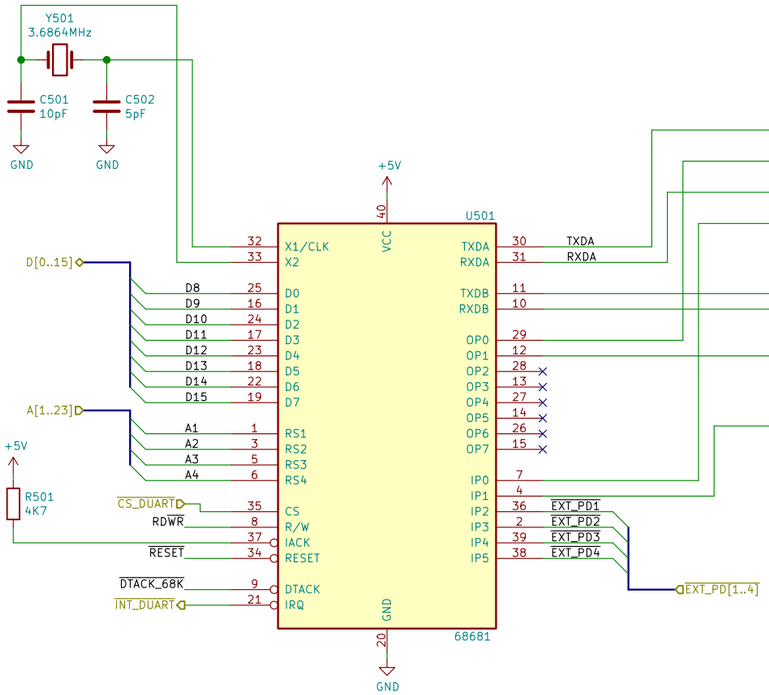

+5V
C401
100nF
C402
100nF
C404
100nF
C405
100nF
C406
100nF
C407
100nF
C408
100nF
C409
100nF
GND

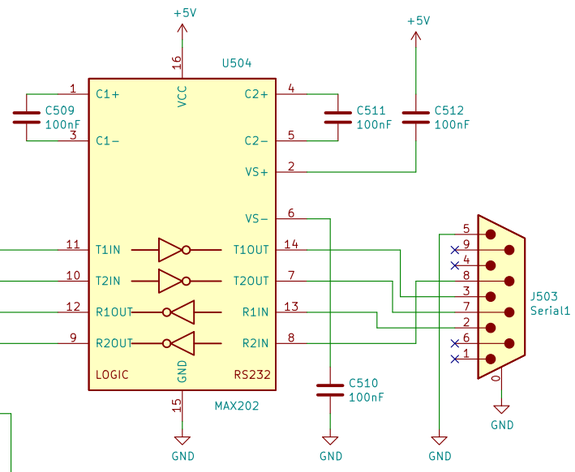

+5V
CPU_RESET
R402
1K
Q401
2N4403
RED
D401
R403
150R
HALT
R404
1K
Q402
2N4403
D402
R405
150R
RUN
R406
1K
Q403
2N4403
GREEN
D403
R407
150R
R408
150R
J402
Ext RUN LED
GND

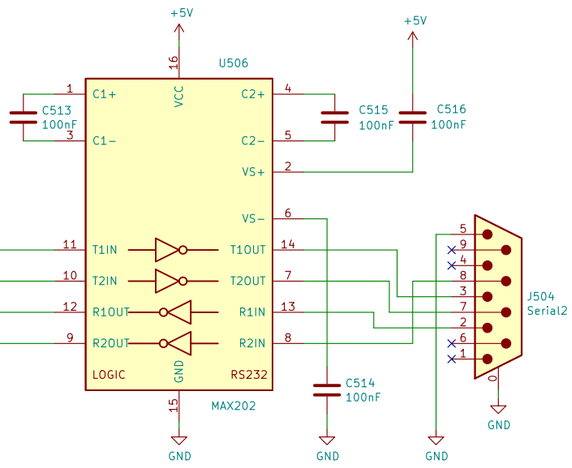


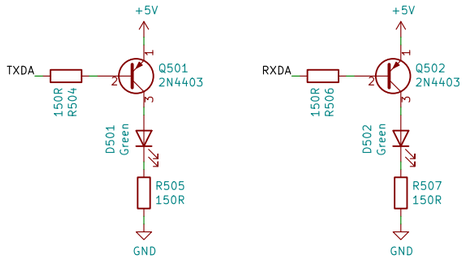


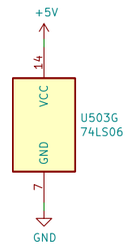












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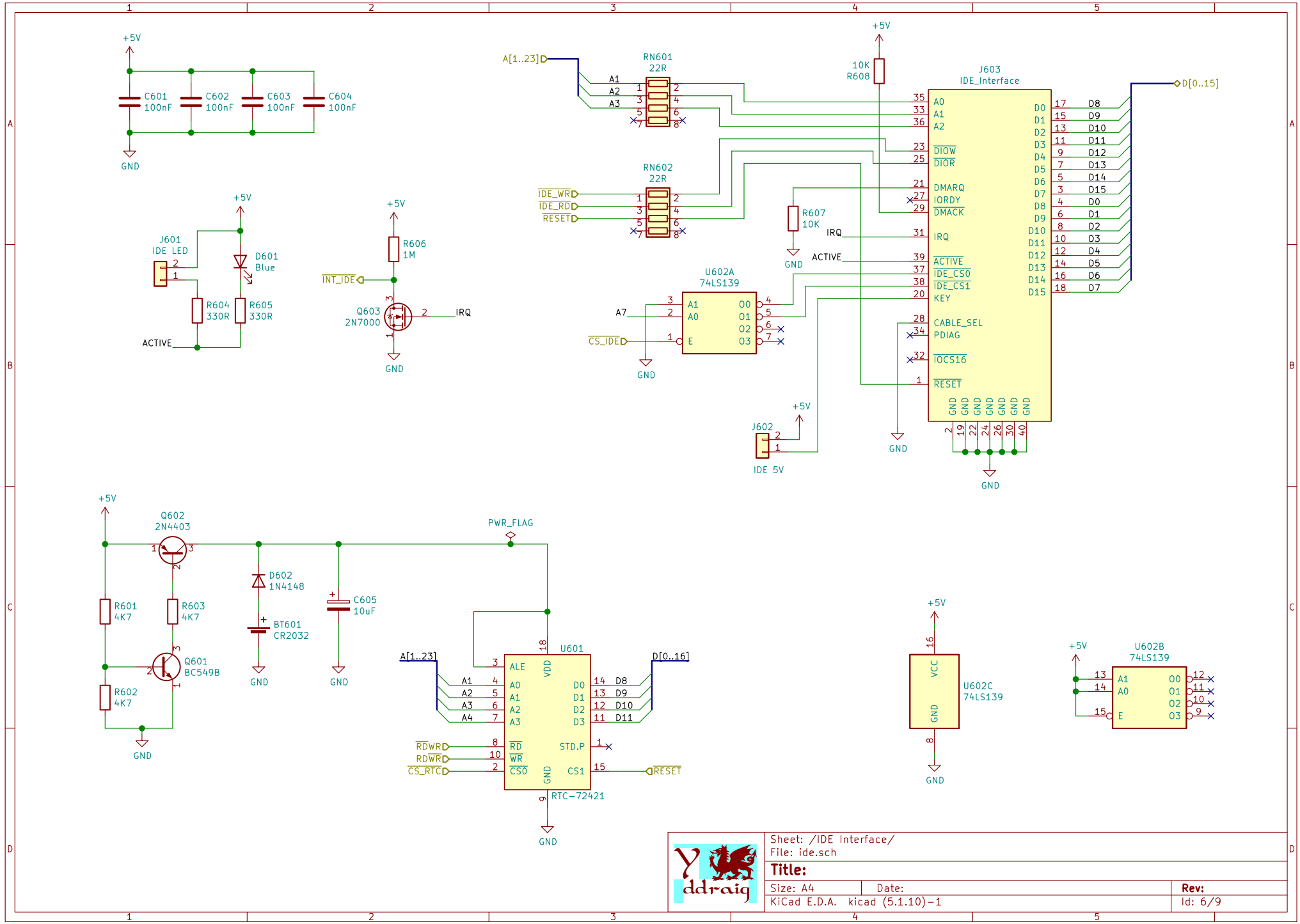
KiCad E.D.A. kicad (5.1.10)-1		Id: 5/9


+5V
C601 100nF
C602 100nF
C603 100nF
C604 100nF
GND
A[1..23]
RN601 22R
A1
A2
A3
RN602 22R
IDE_WR
IDE_RD
RESET
10K R608
R607 10K
IRQ
ACTIVE
J603 IDE_Interface
D[0..15]
A0
A1
A2
DIOW
DIOR
DMARQ
IORDY
DMACK
IRQ
ACTIVE
IDE_CS0
IDE_CS1
KEY
CABLE_SEL
PDIAG
IOCS16
RESET
D0 D8
D1 D9
D2 D10
D3 D11
D4 D12
D5 D13
D6 D14
D7 D15
J601 IDE LED
D601 Blue
R604 330R
R605 330R
R606 1M
INT_IDE
Q603 2N7000
U602A 74LS139
A7
CS_IDE
J602
IDE 5V
Q602 2N4403
R601 4K7
R603 4K7
R602 4K7
Q601 BC549B
D602 1N4148
BT601 CR2032
C605 10uF
PWR_FLAG
U601
ALE
VDD
STD.P
RDWR
CS_RTC
CS0
CS1
RTC-72421
U602C 74LS139
U602B 74LS139
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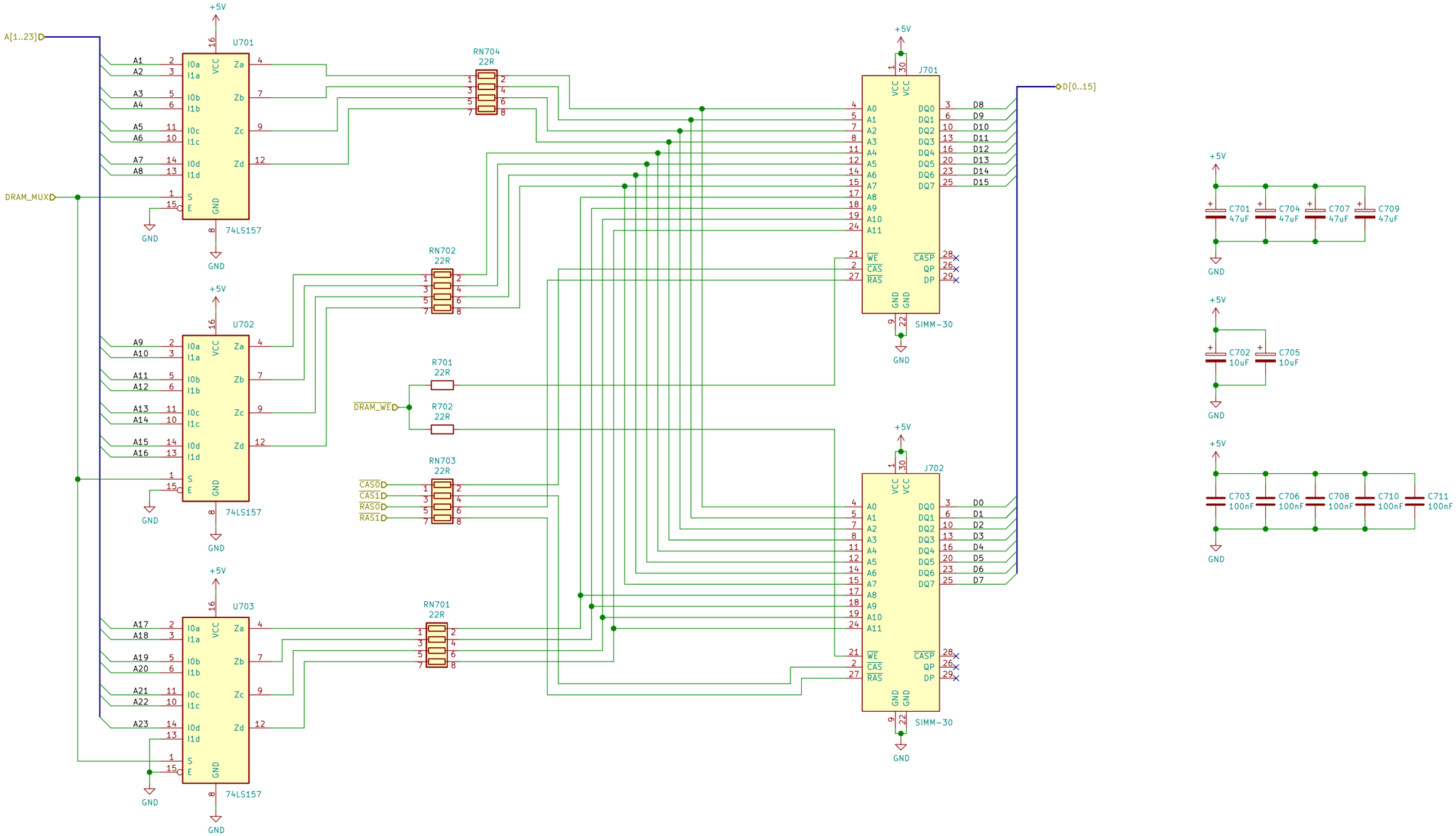
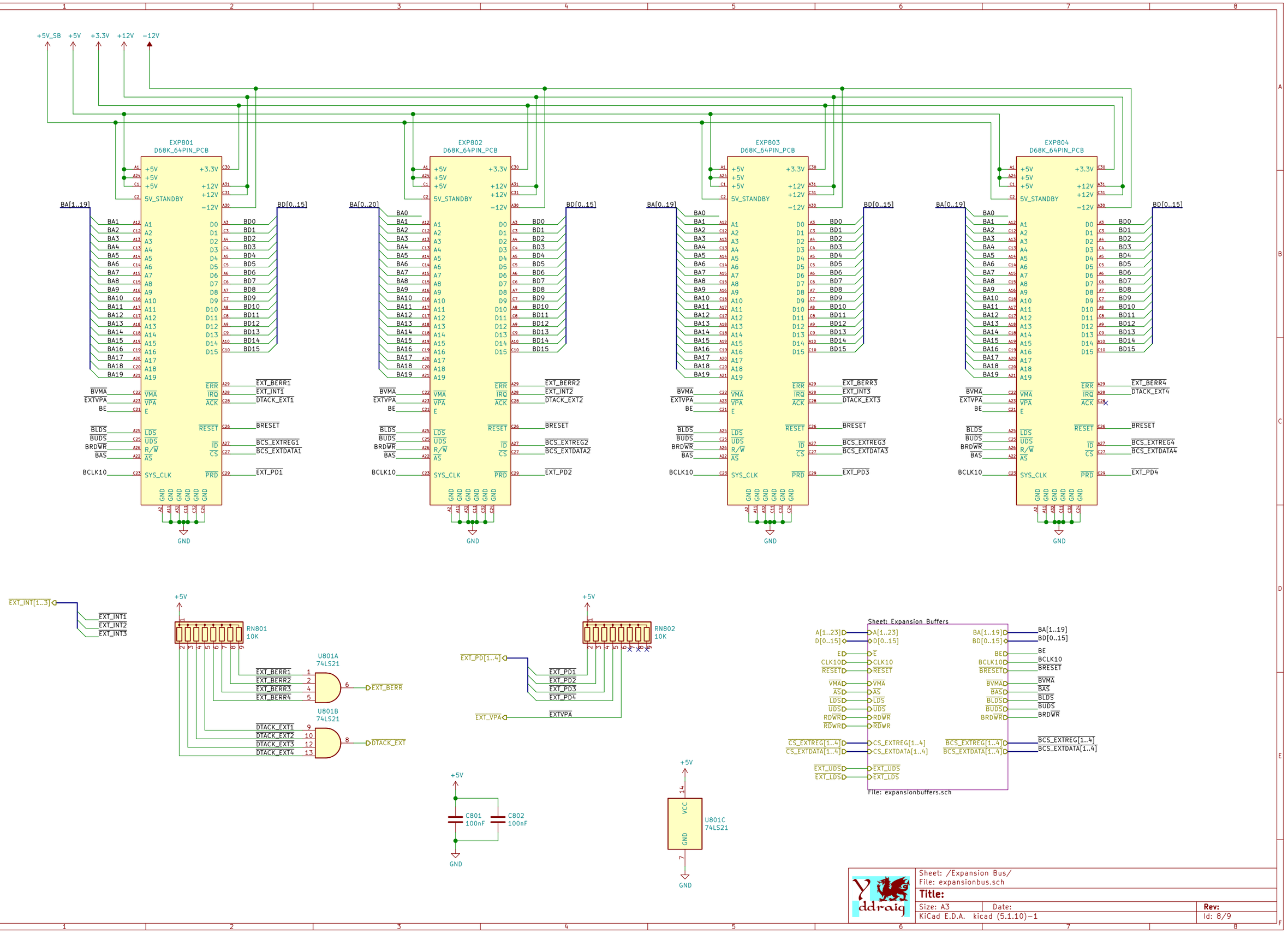
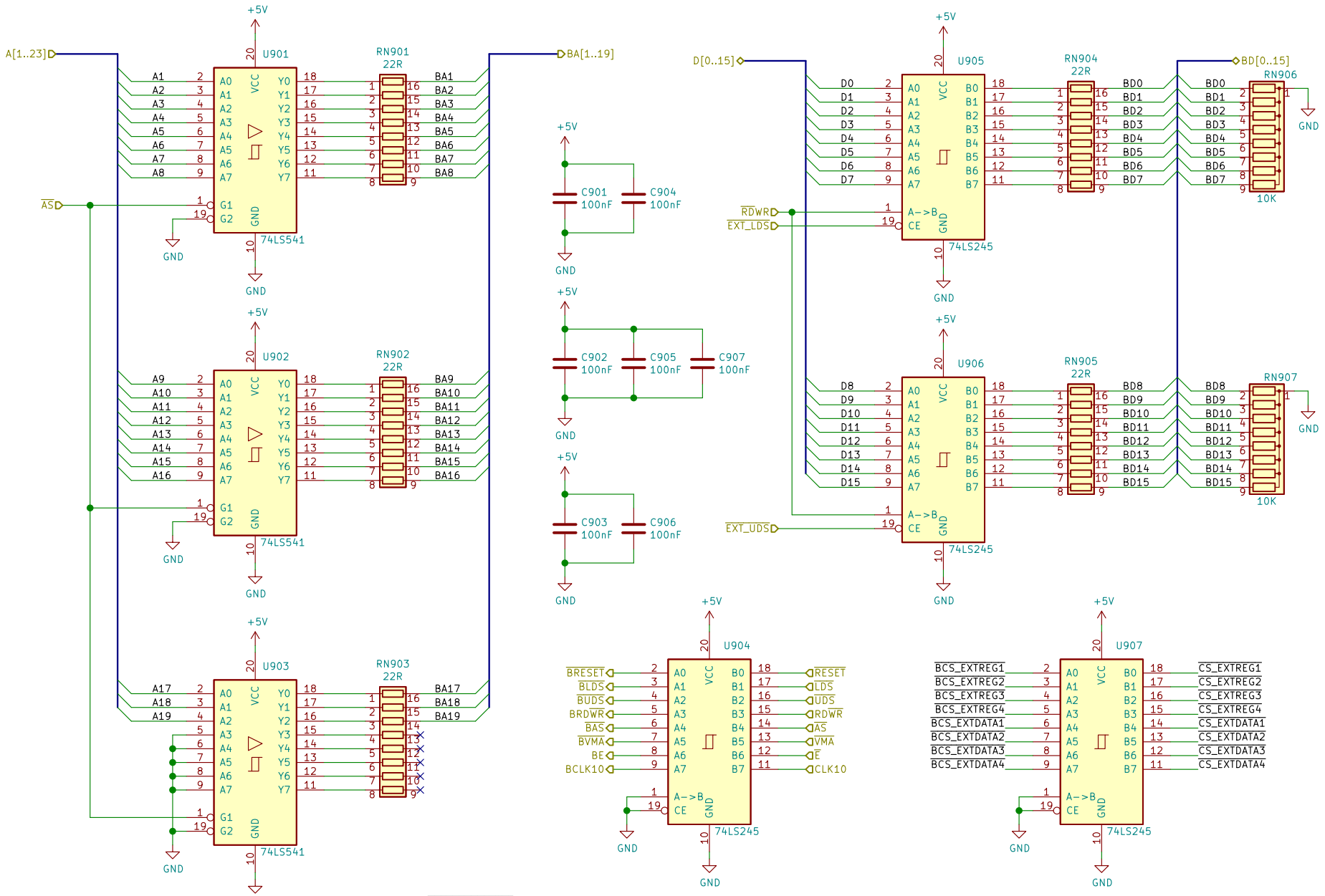
File: ide.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad (5.1.10)-1
Id: 6/9



Sheet: /DRAM Interface/		
File: dram.sch		
Title:		
Size: A3	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.10)-1		Id: 7/9


+5V_SB
+5V
+3.3V
+12V
−12V
EXP801
D68K_64PIN_PCB
EXP802
D68K_64PIN_PCB
EXP803
D68K_64PIN_PCB
EXP804
D68K_64PIN_PCB
5V_STANDBY
BA[1..19]
BA[0..20]
BA[0..19]
BD[0..15]
EXT_BERR1
EXT_BERR2
EXT_BERR3
EXT_BERR4
EXT_INT1
EXT_INT2
EXT_INT3
DTACK_EXT1
DTACK_EXT2
DTACK_EXT3
DTACK_EXT4
BRESET
BCS_EXTREG1
BCS_EXTREG2
BCS_EXTREG3
BCS_EXTREG4
BCS_EXTDATA1
BCS_EXTDATA2
BCS_EXTDATA3
BCS_EXTDATA4
EXT_PD1
EXT_PD2
EXT_PD3
EXT_PD4
GND
EXT_INT[1..3]
RN801
10K
RN802
10K
U801A
74LS21
U801B
74LS21
U801C
74LS21
EXT_BERR
DTACK_EXT
EXT_PD[1..4]
EXT_VPA
EXTVPA
C801
100nF
C802
100nF
Sheet: Expansion Buffers
File: expansionbuffers.sch
CS_EXTREG[1..4]
CS_EXTDATA[1..4]
EXT_UDS
EXT_LDS
Sheet: /Expansion Bus/
File: expansionbus.sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad (5.1.10)-1
Id: 8/9



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File: expansionbuffers.sch

Title:

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KiCad E.D.A. kicad (5.1.10)-1		Id: 9/9