Lab #6 Final Project: Analog-to-Digital Convertor

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1. Objective

In previous experiments we have learned about different aspects of analog and digital circuits and how they function. For the final lab, it is time to combine all of that knowledge and implement a working analog-to-digital convertor (ADC) circuit. We will be using some of the devices we have investigated previously in this course and some devices we have not seen. Examples of devices we have worked with are NOT gates, Op-Amps, NAND gates, flip-flops, transistors, and counters. A device that we have not seen before is a Schmitt-trigger Inverter. The analog-to-digital convertor will be capable of converting an analog voltage in a digital (binary) representation. The components of the ADC that will be constructed are a trigger pulse generator, short pulse rectifier, clock pulse generator, counter, voltage ramp generator, voltage comparator, and control logic. For each component, we will be talking about how the circuit was constructed, tested, and how it functions with pictures and explanations. These components working together will be able to convert analog signals to digital signals.

2. Introduction

Analog signals are very common in the real world and can have many applications. They are known to produce noise which can affect reading of the signals. Examples of these analog signals are the human voice, light power levels, and thermometers. These types of signals can be used for many purposes such as reading/ loading such data into computers for monitoring, processing, storing, and transmission. These tasks require the analog information to be first converted into its digital equivalent. Digital circuits are known to not produce noise compared to analog circuits. The conversion between analog signals to digital signals is where the use of an analog-to-digital convertor can be seen. For the purpose of this lab we will be constructing an ADC from many different components, but an ADC can be purchased with all its components integrated into a single IC.

An analog-to-digital converter is a very useful feature that converts an analog voltage on a pin to a digital number. By converting from the analog world to the digital world, we can begin to use electronics to interface to the analog world around us. Analog signals are signals that have a continuous sequence with continuous values, but there are some cases where it can be finite. Digital signals are represented by a sequence of discrete values where the signal is broken down into sequences that depend on the time series or sampling rate (sampling rate is the number of data points acquired per second). There are many techniques utilized by commercial ADCs to perform the conversion. One of the simplest methods, which is still sometimes used in practice, involves an analog to time converter. The process of the analog to time converter can be described as follows. Upon receiving an appropriate trigger pulse, a second stop pulse is generated at a time "t" later, where "t" is proportional to the voltage level being digitized. This is done using the trigger pulse generator and clock pulse generator components of the circuit. By gating a free-running clock pulse train with this triggered pulse, whose time duration is equal to "t", and counting the number of clock pulses under the gate with an appropriate counter, or scaler, the desired analog-to-digital conversion is obtained. This is achieved with the counter and analog to time converter components of the circuit. This all functions in the circuit with the connection of control logic. This is the type of ADC which we will assemble in this experiment.

More specifically, there are five components that will be integrated into this analog-to-digital converter circuit. Each of these components will be tested individually so that when they are all properly connected, they will form the ADC. For each of the components we will be building it, confirming its operation, describing how it works, and then keeping it assembled on its own in the proto-board for eventual integration into your ADC. Listed below are the five components along with designation in the overall schematic. Figure 1 shows how every component will be constructed and connected to each other.

- Trigger Pulse Generator (TPG)
- Clock Pulse Generator (CPG)
- Counter
- Analog to Time Converter (ATC)
- Control Logic (CL)

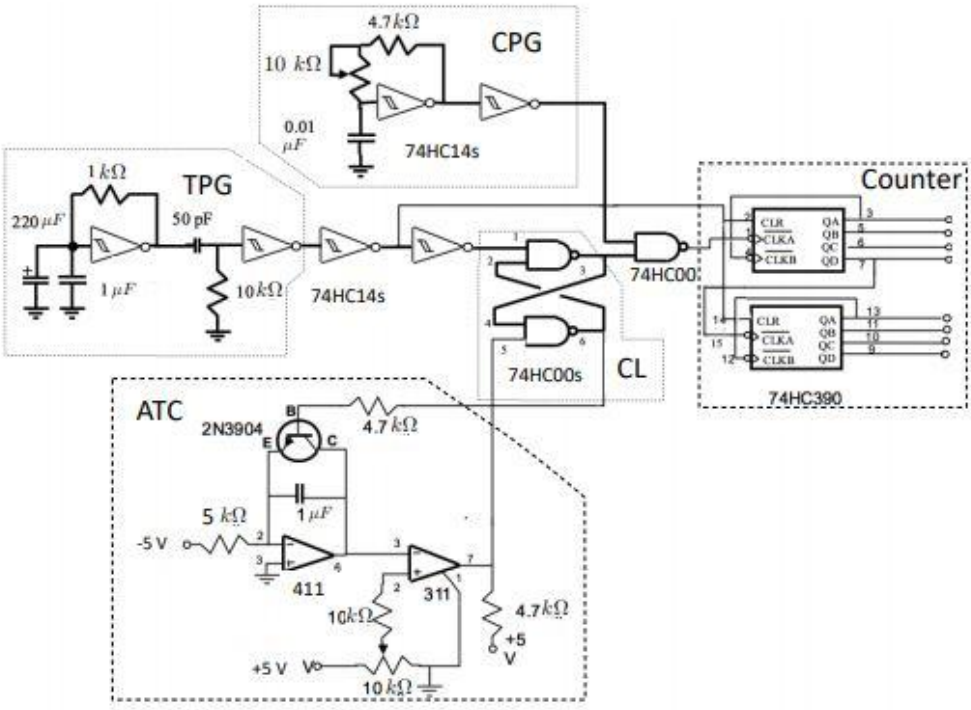


Figure 1: This diagram shows the layout of the different components (from the list above) to form the ADC.

3. Background

Digital electronics is a field of electronics involving the study of digital signals and the engineering of devices that use or produce them. This is in contrast to analog electronics and analog signals which we have seen in previous labs. In digital electronics the FALSE (or Lo or 0) logical level is typically represented by a voltage level of 0 Volts, while the TRUE (or Hi or 1) logical level is usually +5 Volts. In newer circuits the latter is sometimes +3.3 Volts. An advantage digital electronics has over analog electronics is that digital signals can only take two values so they are much more immune to noise corrupting the signals. This could lead to less noisy measurements and allow for more clear comparisons. A disadvantage is that only two states can be represented. However, this is easily addressed by using the binary number system in which more than one bit is used. It is important to note that each bit takes on a value of 0 or 1. Analog circuits operate or work with continuous valued signals or continuously varying signals. These signals are commonly referred to as analog signals and examples of these signals are sound and light. Digital circuits operate or work on signals whose values exist at two levels only or has only two values (zeros and ones). These signals are commonly referred to as digital signals and at any given instant of time the value of a digital signal can be either high (one) or low (zero). Examples of these are computers and digital phones. Graphs of Analog and Digital signals can be seen below.

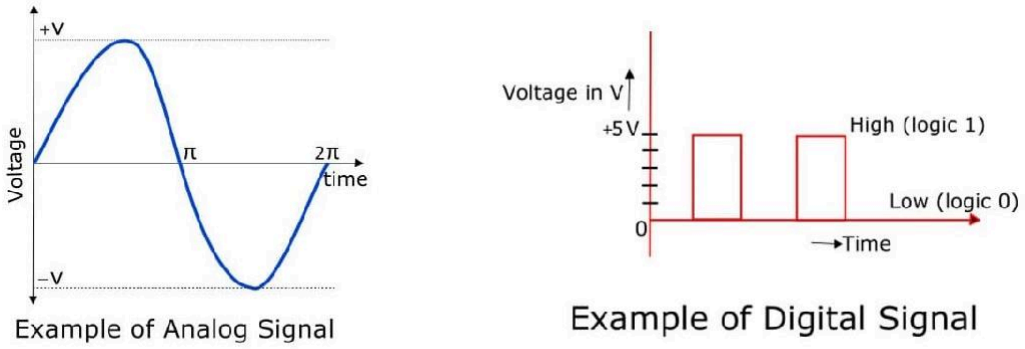


Figure 2: This image shows the differences between an Analog signal and a Digital signal. As seen on the left, Analog circuits operate with continuous valued signals or continuously varying signals. As seen on the right, Digital circuits operate on signals whose values exist at two levels only or has only two values (zeros and ones).

Digital logic gates are constructed in Integrated Circuits (IC) and these packages which usually contain more than one such device. An integrated circuit or monolithic integrated circuit (also referred to as an IC, a chip, or a microchip) is a set of electronic circuits on one small flat piece, or chip, of semiconductor material that is normally made of silicon. There are many different types of digital IC technology. The IC's which I will be using in this experiment are called silicon-gate CMOS FETs (Complementary Metal Oxide Semiconductor Field Effect Transistor) and are members of the MC54/74 series. I will be using the pin layouts that are provided in the given data sheets. It is important to note that in addition to the signal connections, all of the IC's must be connected to both ground and a +5V, or +3.3V, power supply. The layout diagrams that will be used are provided below.

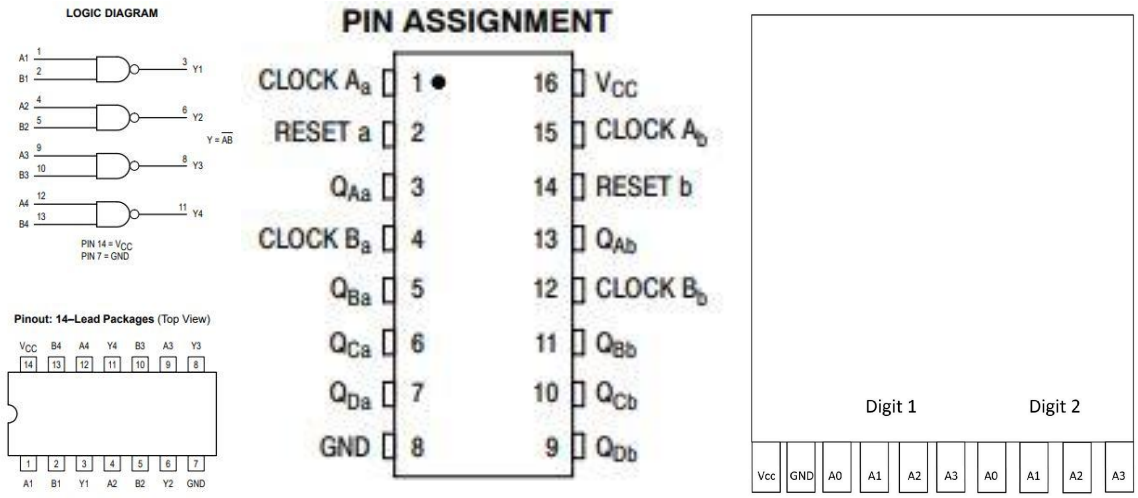


Figure 3: These diagrams show the pin layouts for the 74HC00 Quad 2-Input NAND Gate (left top and bottom), the 74HC390 Binary Ripple Counter (middle), and the 2 Digit 7 Segment Display Rev 1.0 W0#E20-011 from UBC (right).

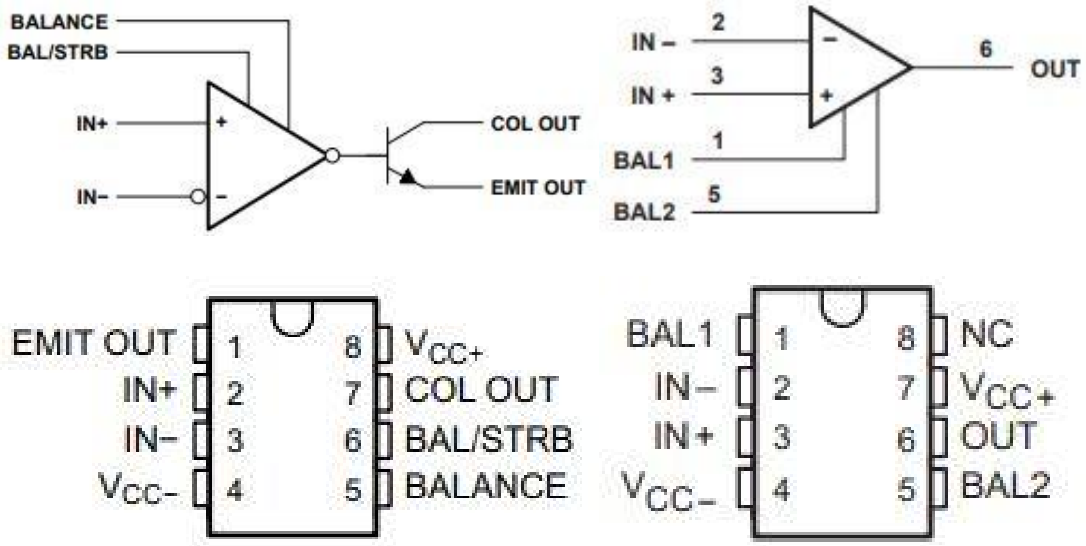
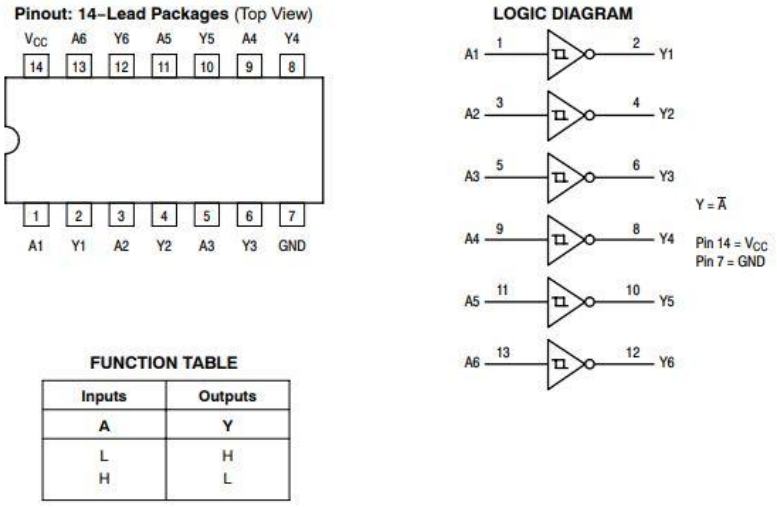


Figure 4: These diagrams show the pin layouts for the LM311 Operational Amplifier (left top and bottom) and the LM 411 Operational Amplifier (right top and bottom) respectively.



FUNCTION TABLE

Inputs	Outputs
A	Y
L	H
H	L

Figure 5: These diagrams show the pin layout for the 74HC14A Inverters. The function table and logic diagrams are also included.

Additionally, we can look at the clocks function table to justify if the circuit constructed is correct. The function table can be seen below. We will be working with ÷2 counters and a ÷5 counters to create a ÷100 counter so it is important to notice how the falling edge of the clock position changed the position of the clocks output wave. This table will also come in handy when looking at counters that use combinations of the ÷2 counters and a ÷5 counters, for example the ÷100 counter.

FUNCTION TABLE

Clock A	Clock B	Reset	Action
X	X	H	Reset +2 and +5
↓	X	L	Increment +2
X	↓	L	Increment +5

Figure 6: This table shows the relation between the clock, reset, and output of the 74HC390 “Dual 4-Stage Binary Ripple Counter”. I will be referring to this table in the counter section.

Such equipment that will be used are an oscilloscope, arbitrary waveform generator (AWG), logic analyzer, and voltage power supply. Additionally, we will be using a digital multimeter (DMM) that has a resistance uncertainty measurement of $\pm 1\%$ and a breadboard. We will be working with a analog to digital convertor circuit while using the Analog Discovery 2 instrument which has an internal resistance of 1MΩ (found in manual). The program Waveforms will be simulating the voltages and digital I/O signals that we will be using to test each components functionality. This will be done using a DC power supply and ground. AC power will also be used to test the individual components of the circuit. The uncertainty of the oscilloscope depends on if the cursors or the quick measure tool is used when finding values. It also depends on the scale of the axis, for example how many volts per division.

4. Trigger Pulse Generator

4.1 Schmitt-Trigger Hysteresis

There are many types of inverters that can be used for different purposes. The type of inverter we will be focusing on in this lab is called a Schmitt-Trigger Inverter. We will be using this type of inverter to construct the trigger pulse generator (TPG). This type of inverter incorporates hysteresis in the input triggering characteristic. In other words, the input voltage level that is needed to cause the output to make a transition from one state to the other depends on which output state the inverter is currently in. This is shown in figure 7. Hysteresis can be described as the history dependence of physical systems. For example, if you push something in, does it spring back completely? If it doesn't, it is exhibiting hysteresis in a sense. When testing the Schmitt-Triggers we can find the threshold levels of the unit. That is, determine the amount of hysteresis characterizing the device. We can do this by generating a triangle wave using the Analog Discovery 2 unit as the input to one of the inverters. The threshold levels of the unit can be described as when the output switches from HI to Lo and Lo to HI. This can be seen in the figure 9. The presence of hysteresis of this kind increases the versatility of the unit. The wave that was used to find these thresholds was a triangle wave of amplitude 5V and frequency 1kHz. The circuit construction can be seen in figure 8 and the pins of the inverter were connected according to the pin layout diagram in the background section. The scales of the oscilloscope that were used to measure the threshold values were 200us/div and 1V/div. The Vcc used for the inverter was also 5V. Using the quick measure tool of the oscilloscope the upper (Lo to HI) and lower (HI to Lo) threshold values were found to be $2.964 \pm 2.887\text{x}10^{-4}\,V$ and $1.832 \pm 2.887\text{x}10^{-4}\,V$ respectively. This means that when the voltage starts below

both thresholds, it has to increase to above the high threshold in order for the output to be HI. If the voltage starts out higher than both thresholds, it has to decrease to below the lower threshold in order for the output to become Lo. The uncertainty of these measurements were found by dividing half the least uncertain digit by the square root of three. This formula was used because the value was not flickering for either measurement. This means that we can find the amount of hysteresis characterizing the device by finding the difference between the two threshold values. Therefore, the value is $1.132 \pm 2.887\text{x}10^{-4}\,V$. It is important to note that Schmitt-trigger circuits provide excellent noise immunity and the ability to square up signals with long rise and fall times as seen in figure 9. It provides great noise immunity because certain voltage jumps will not pass both thresholds, meaning that the noise will not affect the output. This is caused because of the Schmitt-triggers use of hysteresis that we talked about before. One thing to note is that the negative values for the input voltage seen in figure 9 get clipped before it can reach its minimum value. This does not really have any effect on the measurements taken for the hysteresis because the square waves were still generated as intended.

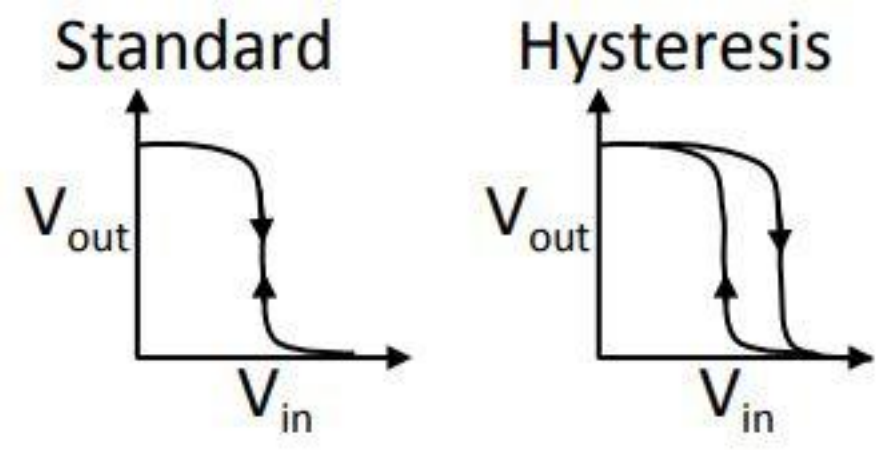


Figure 7: This figure shows how the input voltage level that is needed to cause the output to make a transition from one state to the other depends on which output state the inverter is currently in.

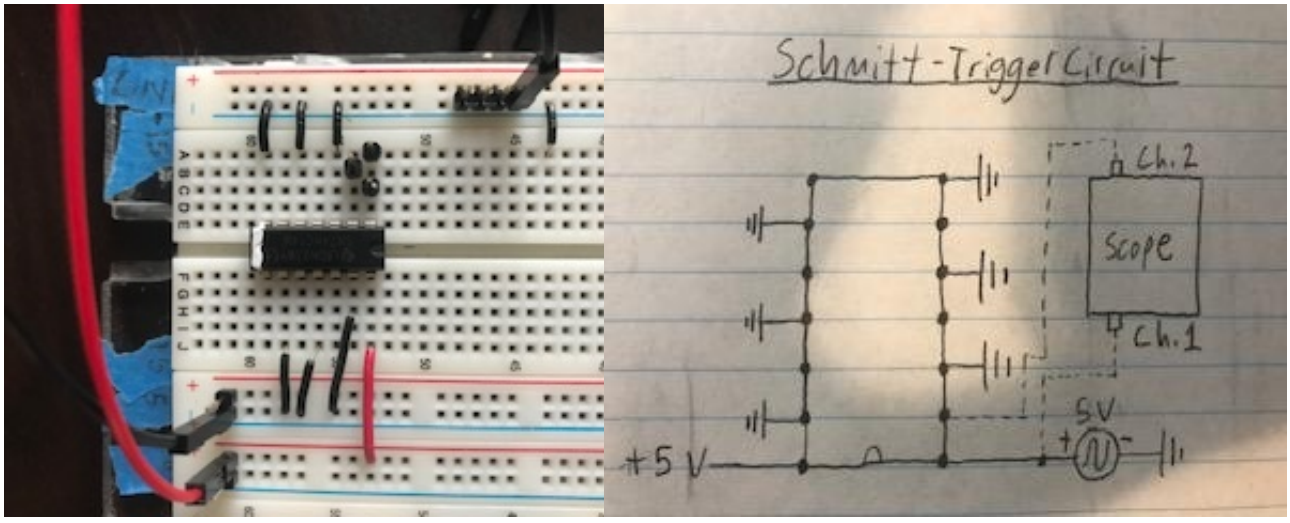


Figure 8: These diagrams show the design for the Schmitt-trigger circuit using a 74HC14A inverter (small black rectangle with silver stripe). It has a 5V power supply (red wire), multiple ground wires (black wire), channel 1 and channel 2 wires of the oscilloscope. It also uses the waveform generator to generate a triangular wave

(yellow wire) but the wire has been removed for clarity. The wires of the oscilloscope have also been taken out for circuit clarity but their respective black connection pins have been left in.

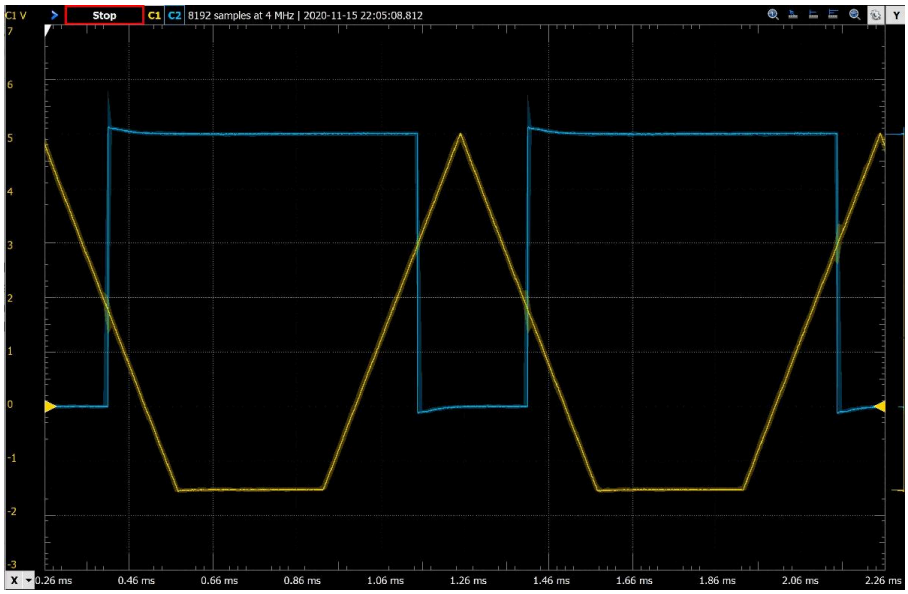


Figure 9: This diagram shows the input (yellow) and output (blue) of the Schmitt-trigger inverter (74HC14A inverter) that was tested. We can see the Lo to HI and HI to Lo thresholds as the intersections between the input and output lines. The triangle wave generated had a amplitude of 5V and frequency of 1kHz. The voltage supply (Vcc) was 5V. The scales of the oscilloscope were 200us/div and 1V/div.

4.2 Square Wave Oscillator

Next, I constructed the trigger pulse generator, which was composed of two parts. The first part that was built and tested was the square wave oscillator. The circuit design for this component can be seen in figure 10. The same Schmitt-trigger inverter was used but now with the added components of a 1kΩ resistor and a 10nF capacitor. The pins of the inverter were also set up according to the pin layout diagram (74HC14A inverter) in the background section. This circuit can be described as a Schmitt trigger RC oscillator because of its use of a Schmitt trigger inverter gate with RC elements. We tested the input and output of the square wave generator using the channel 1 and 2 wires of the oscilloscope and the results can be seen in figure 12. When comparing figure 12 to the expected graph of a Schmitt trigger RC oscillator seen in figure 11, we can see that the results are very similar. As seen in the diagram below, the resistor connects the circuit in a positive feedback loop that is necessary for the oscillation. Considering the diagram in figure 11, when V_C is less than V_{T-}, V_O goes HI and starts charging the capacitor through the resistor. When V_C crosses the threshold voltage V_{T+}, V_O goes Lo and starts to discharge the capacitor through the resistor. When V_C crosses the threshold V_{T-}, the first step is repeated. This behavior creates the output oscillation. It is important to note that an external input voltage is not needed for the circuit to run because of the provided V_{CC} of 5V in the inverter. I next recorded the input and output voltage values for the square wave oscillator. There is no initial input voltage because of what was previously stated but the voltage output of the square wave was found to be $V_{O+} = 4.893 \pm 0.100\,V$ and $V_{O-} = -4.913 \pm 0.100\,V$. These values were measured using the cursors. For the positive measurement, multiple values (between and including the possible min and max) were recorded and then averaged to come

to the values stated. The uncertainty was found by computing half the distance from the max and min. These steps were repeated for the negative measurement.

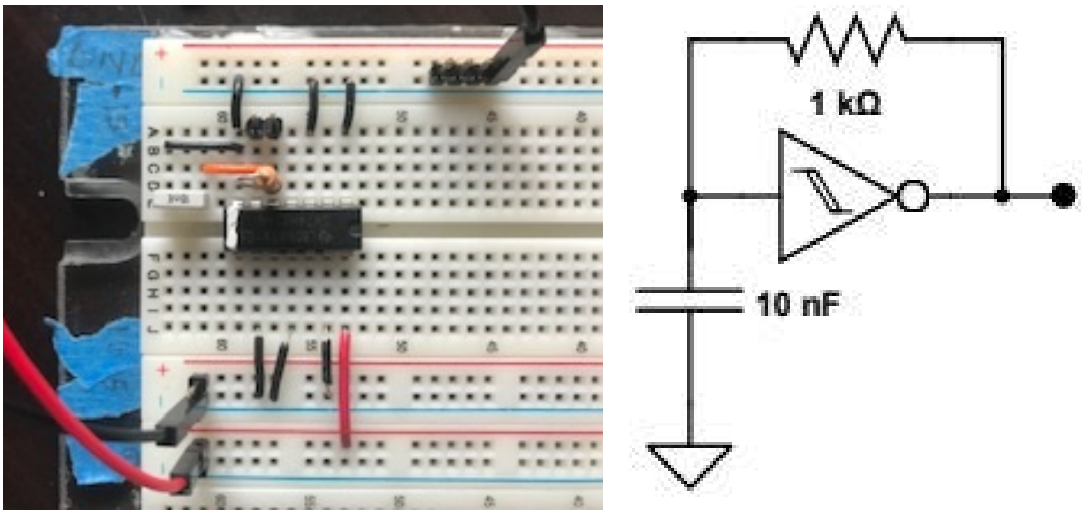


Figure 10: These diagrams show the design for the square wave oscillator using a Schmitt-trigger circuit using a 74HC14A inverter (small black rectangle with silver stripe). It has a 5V power supply (red wire), a 1kΩ resistor (gold red black and brown stripes), a 10nF capacitor (small grey rectangle), multiple ground wires (black wire), channel 1 and channel 2 wires of the oscilloscope. The wires of the oscilloscope have been taken out for circuit clarity but their respective black connection pins have been left in.

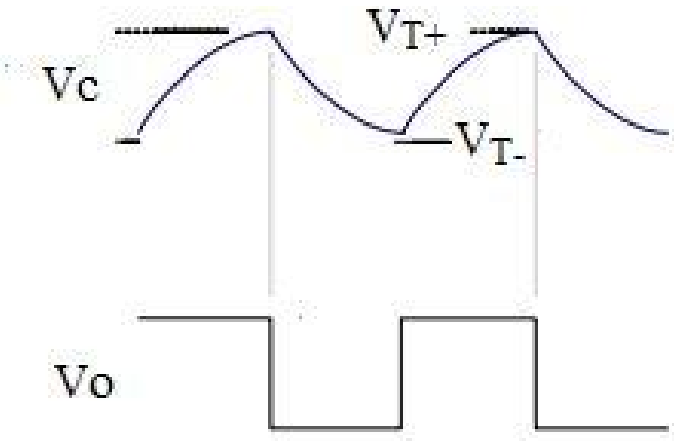


Figure 11: This diagram shows the expected voltage oscillation relation of the square wave oscillator. It also shows the upper and lower thresholds of the inverter and the built-in hysteresis. V_C and V_O are the supply and output voltage waves respectively. V_{T+} and V_{T-} are the voltage levels of the upper and lower thresholds respectively.

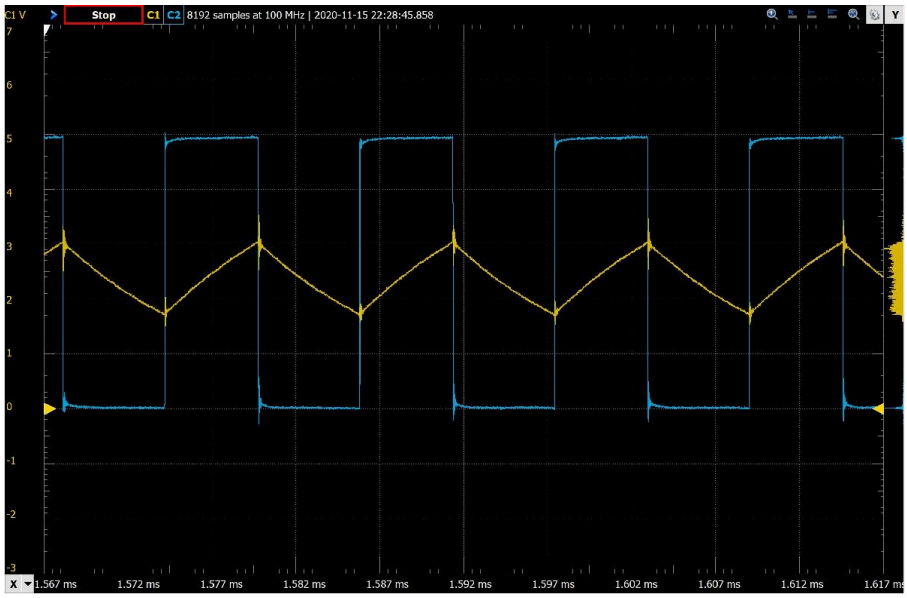


Figure 12: This graph shows the input (yellow) and output (blue) of the square wave generator that uses the same Schmitt-trigger inverter. As seen from the graph, the input oscillates between the upper and lower thresholds of the inverter. When comparing this image to figure 6 we can see that they are similar. No input wave was used but the supplies that was used was 5V. The scales of the oscilloscope were 5us/div and 1V/div.

4.3 Short Pulse Rectifier

For the ADC we will need a trigger pulse generator (TPG) providing short pulses every few seconds, rather than a square wave. This is required in order to trigger the ADC into performing measurements of the input analog signal repetitively, a few times a second. These short pulses are generated by the adding the short pulse rectifier to the output of your square wave. Therefore, I next constructed the second component of the trigger pulse generator. This component being the short pulse rectifier. The circuit design for this component can be seen in figure 13. The same square wave oscillator was used but now with the added components of the short pulse rectifier. The short pulse rectifier consists of a 10kΩ resistor, a Schmitt-trigger inverter, and a 50pF capacitor. The pins of the inverter were also set up according to the pin layout diagram (74HC14A inverter) in the background section. As seen in the diagram below, once part b of the circuit was constructed, its input was attached to the output of part a of the circuit.

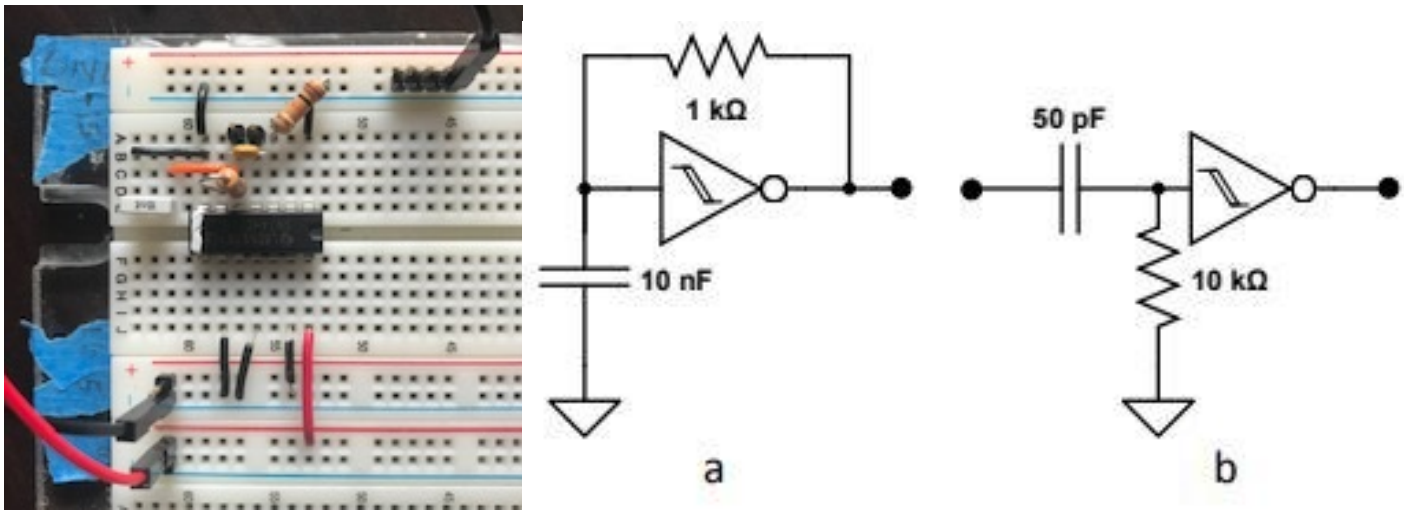


Figure 13: These diagrams show the design for the square wave oscillator combined with the short pulse rectifier using two Schmitt-trigger circuits using a 74HC14A inverter (small black rectangle with silver stripe). It has a 5V power supply (red wire), a 1kΩ resistor (gold red black and brown stripes), a 10kΩ resistor (gold orange black and brown stripes) , a 10nF capacitor (small grey rectangle), a 50pF capacitor (small yellow rectangle), multiple ground wires (black wire), channel 1 and channel 2 wires of the oscilloscope. The wires of the oscilloscope have been taken out for circuit clarity but their respective black connection pins have been left in.

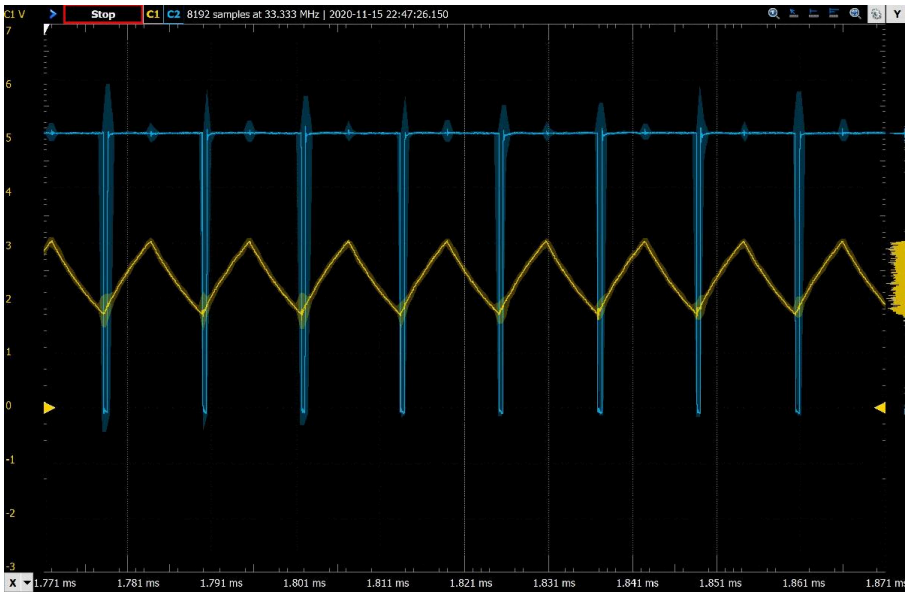


Figure 14: This graph shows the input of the square wave oscillator (yellow) and output of the short pulse rectifier (blue) that uses the same two Schmitt-trigger inverters. As seen from the graph, the input oscillates between the upper and lower thresholds of the inverter. No input wave was used but the supplies that was used was 5V. The scales of the oscilloscope were 10us/div and 1V/div.

4.4 Final TPG

Now that the square wave oscillator and short pulse rectifier are correct and working together, we next want to decrease the oscillation frequency of the square wave oscillator by first changing the 0.01 µF capacitor to a 1.0

µF capacitor and then connecting a 220 µF capacitor in parallel with it. When dealing with large capacitors it is important to note that ones with large values (100s of µF) of capacitance are electrolytic capacitors which have a polarity. They must be inserted into the circuit properly or else they will not work as intended. In this case, I connected the negative (black) side of the capacitor to ground. The circuit design can be seen below with the replacement components described above. The expected output is a pulse from HI to Lo and back to HI which can be seen in figure 16. This validifies the circuit functionality. As it is difficult to trigger the oscilloscope with the decreased frequency of the TPG, in order to confirm its operation I used the single-shot trigger capability of the oscilloscope. This involved changing the source to channel 2 and moving the arrow on the right side of the graph upwards. This can be seen in figure 16.

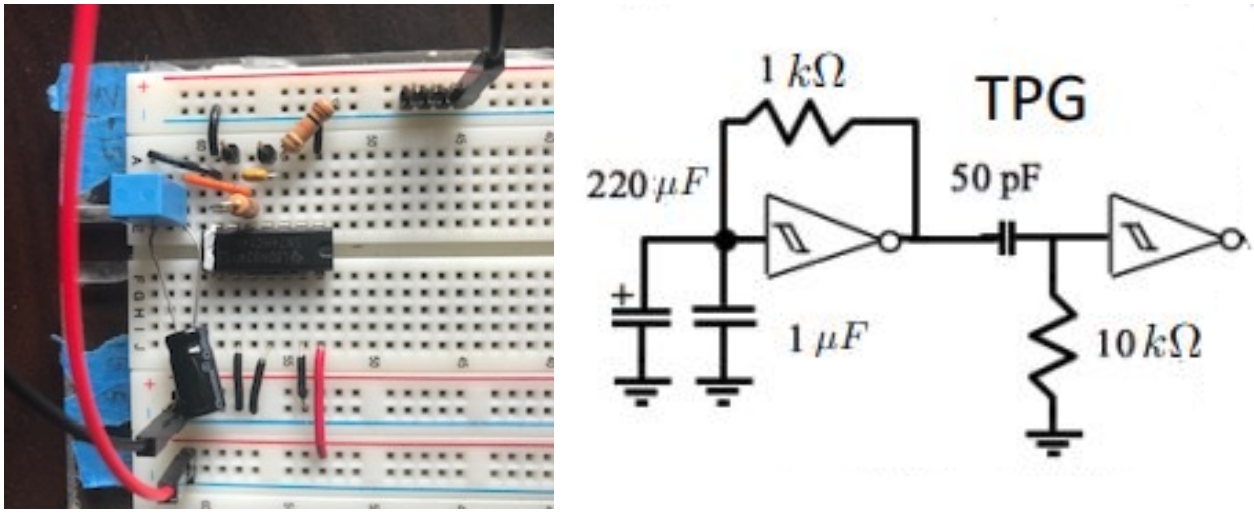


Figure 15: This diagram has the same components as the diagram for the combination of the square wave oscillator and short pulse rectifier but changing the 0.01 µF capacitor to a 1.0 µF capacitor and then connecting a 220 µF capacitor in parallel with it. This is the final design for the trigger pulse generator. The wires of the oscilloscope have been taken out for circuit clarity but their respective black connection pins have been left in.

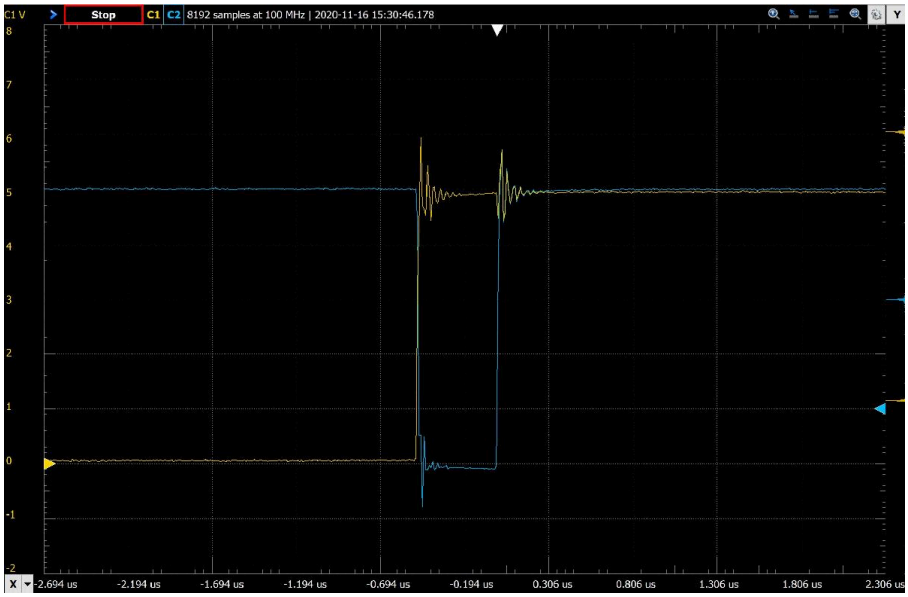


Figure 16: This graph shows the input (channel 1) and output (channel 2) of the complete trigger pulse generator. The pulse generated by the TPG can be seen when the blue waves goes from HI to Lo and back to

HI. No input wave was used but the supplies that was used was 5V. The scales of the oscilloscope were 500ns/div and 1V/div.

5. Clock Pulse Generator

5.1 Square Pulse Generator

Now we will be constructing a second square pulse generator but this time acting without the short pulse rectifier. The clock pulse generator generates a train of clock pulses which when counted by a scaler will generate the digital output of the device. The circuit was constructed according to figure 17 shown below. The CPG can be described as creating a sequence of fast square pulses which passes through a inverter and then gets sent to a NAND gate where it then gets sent to ClockA of the counter. As seen in the diagram, the 10 kΩ variable resistor enables us to tune the frequency of the oscillator. I tuned the potentiometer and verified that the circuit produces a square wave with a frequency that is ≈ 6 kHz to 19 kHz. When tuning to the extreme maximum and minimum values of the resistor, the maximum and minimum period of the square wave was measured. The periods were found to be $153.0 \pm 0.03\,s$ and $51.39 \pm 0.003\,s$. The values were measured using the quick measure tool of the oscilloscope, so the uncertainty was calculated by dividing half the last digit by the square root of 3. These values can now be turned into frequency using the equation $f = \frac{1}{T}$. Therefore, the maximum and minimum frequency were found to be $19.46 \pm 0.001\,\text{kHz}$ and $6.54 \pm 0.001\,\text{kHz}$. The uncertainties were calculated by finding the percentage of the period uncertainty with the period and applying that percentage to the frequency. When comparing these values to the expected values along with the oscilloscope output, we can see that the square pulse generator functions as expected. The output of the CPG measured by the oscilloscope is shown in figure 18. Additionally, the pins layout of the two Schmitt-Triggers are consistent with the pin layout diagram of the 74HC14A inverter in the background section.

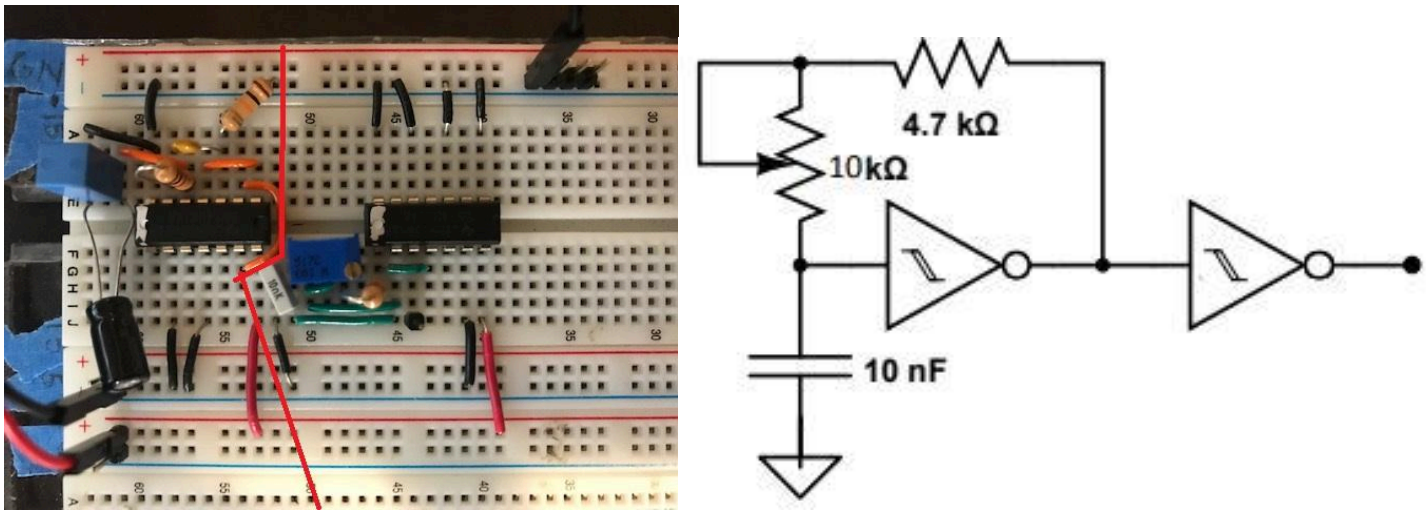


Figure 17: The left image to the right of the red line shows the clock pulse generator and the right image shows the circuit diagram. The design uses a 74HC14A inverter (small black rectangle with silver stripe). It has a 5V power supply (red wires), a 4.7kΩ resistor (silver red purple and yellow stripes), a 10kΩ variable resistor (blue box) , a 10nF capacitor (small grey rectangle), a potentiometer (blue box), multiple ground wires (black wire),

and channel 1 wire of the oscilloscope. The wires of the oscilloscope have been taken out for circuit clarity but their respective black connection pins have been left in.

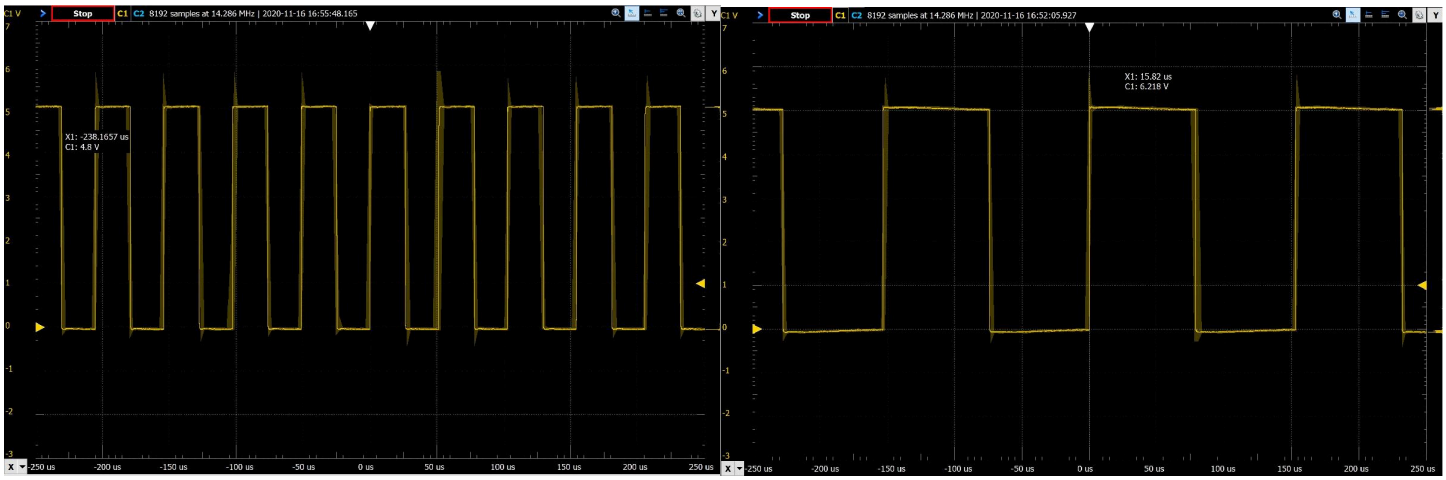


Figure 18: These graphs show the output square pulses from the CPG when tuning the variable resistor to its maximum and minimum. The left corresponds to the minimum period (maximum frequency) and the right corresponds to the maximum period (minimum frequency). The CPG had a 5V supply and the scales of the graph were both 50us/div and 1V/div.

6. Counter

6.1 ÷100 Counter With 7 Segment Decimal Display

Next, a ÷100 counter was constructed by connecting the two decade counters to each other as seen in figure 19. To verify the operation of the whole counting system, the ÷100 counter was connected to the 2 Digit 7 Segment Display Rev 1.0 W0#E20-011 from UBC and a negative feedback train was fed into the clock input. The expected output is to see the numeric display increment in the usual base-10 fashion from 0 to 99. In order to reset the decade counter, the appropriate inputs of the decade counters, pins 2 and 14, were connected to a second push-button whose output resides at ground to enable one to reset the counter by depressing the button. The Logic tool was used to see all the different states together. After the circuit was verified with a logic timing diagram, I then connected the output to the 7 segment LED display, or number display, in order to display the counter's state in decimal form (from 0 to 99). A video of this in operation can be found on YouTube: https://youtu.be/Ddsm04EE5Yg. The pulse frequency was made low enough, around 1 Hz, in order to see the counter count up until it was reset. The state of the reset was always off (zero) and when switched to on (one) the counter would go back to 0.

To set up the circuit, I first connected the +5V supply to Vcc and the ground wire to GND. I then connected the DIO 0 wire to pin 1 as the main input. The DIO 1 wire was set to Lo connected to pin 2 as well as pin 14 for the other reset pin. DIO 2 was connected to pin 3 as the output representing the 0th index of the binary number. Pin 3 was also connected to pin 4. Pin 5 was output representing the first index of the binary number. Pin 6 was output representing the second index of the binary number. Pin 7 was output representing the third index of the binary number and was also connected to pin 15. Pin 13 was output representing the 0th index of the second binary number and was also connected to pin 12. Pin 11 was output representing the first index of the second binary number. Pin 10 was output representing the second index of the second binary number. Pin 9 was output

representing the third index of the second binary number. These connections can be seen visually in the figures below. A 100 counter is basically just two 10 counters at each digit. This means that the binary numbers are read the same way and the wires are connected the same way as for a 10 counter but now just double the connections for a second digit. It is important to note that the digital LED counter used to display the numbers consists of 8 inputs which represent 2 four digit binary numbers which each range from zero to nine. This allows us to show two numbers that can counter up to 99. It is also important that both reset pins be connected so that when activated, both digits reset at the same time to the same state. When the reset button is clicked it is set to HI so the value of the counter goes to 0.

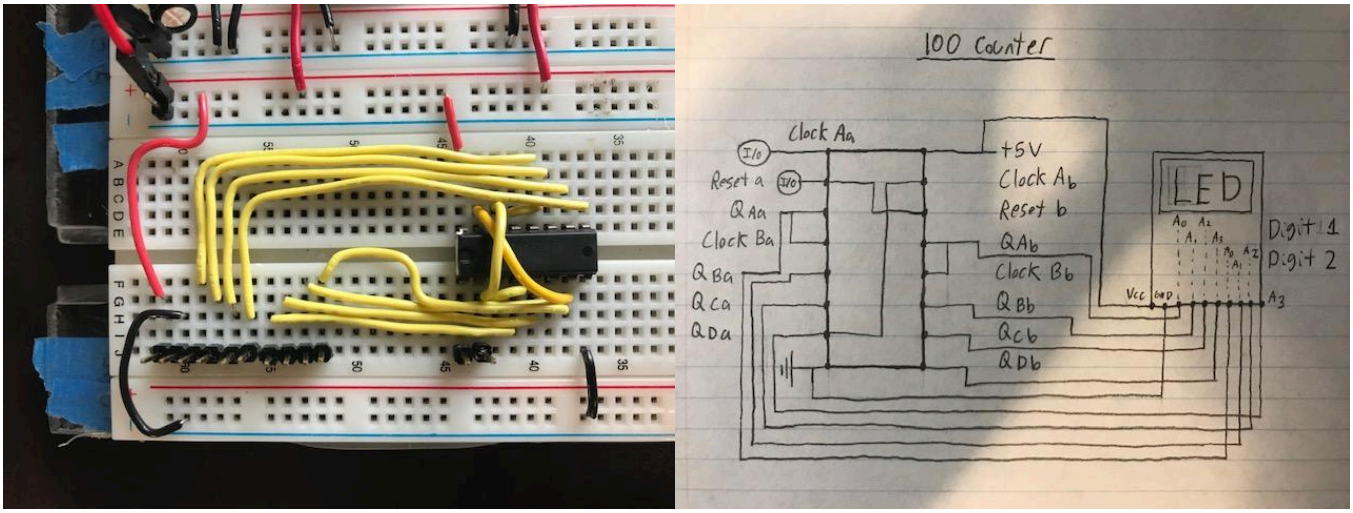


Figure 19: This figure shows the constructed circuit and circuit diagram of the 100 counter. The circuit uses a 74HC390 “Dual 4-Stage Binary Ripple Counter” with ÷2 and ÷5 Sections (black rectangle), a +5V source (red wire), two digital I/O signal wires (pink, and green), and a ground wire (black wire). All the other wires are used to connect the counter outputs with the LED display. The logic wires of the oscilloscope have been taken out for circuit as well as the 7 segment decimal display for clarity but their respective black connection pins have been left in.

7. Analog to Time Converter

7.1 Voltage Ramp Generator

The next component of the ADC that was constructed was the analog to time converter (ATC). The ATC consists of two parts. The first part is a circuit which, on receipt of a start pulse that is produced by the TPG, generates a voltage ramp. A voltage ramp can be described as a voltage signal that increases linearly with time. The voltage ramp circuit is an op-amp current integrator in which a constant 1.5 mA DC current is integrated on the 1 µF feedback capacitor, yields a positive ramp voltage output signal which can be seen in figure 21. The OpAmp Integrator is an operational amplifier circuit that performs the mathematical operation of Integration. This means that we can cause the output to respond to changes in the input voltage over time as the op amp integrator produces an output voltage which is proportional to the integral of the input voltage. This can we been in figure 22. When a step voltage, V_I is first applied to the input of an integrating amplifier, the uncharged capacitor C has very little resistance and acts like a short circuit allowing maximum current to flow from the input resistor. This is what causes the voltage ramp to be produced. The BJT transistor in parallel with the

feedback capacitor is an electronic switch controlled by the logic circuit when fully connected with the final circuit. Bipolar Transistors are current regulating devices that control the amount of current flowing through them from the emitter to the collector terminals in proportion to the amount of biasing voltage applied to their base terminal. This means that they can act like a current-controlled switch. As a small current flowing into the base terminal controls a much larger collector current forming the basis of transistor action. When the switch is open, resulting when a Lo level is applied to its input at its Base, the integrator operates in the fashion described. Thus, producing the required ramp voltage at its output. However, when the switch is closed, resulting when a HI level is applied to its input, the feedback capacitor is shorted out. Since the 1.5 mA current flowing through the switch results in an insignificant potential drop, a zero voltage or logic level Lo is produced at the output of the LF411 OpAmp. The voltage ramp generator circuit design can be seen in figure 20. The setup pins of the LF411 can be seen in the background section.

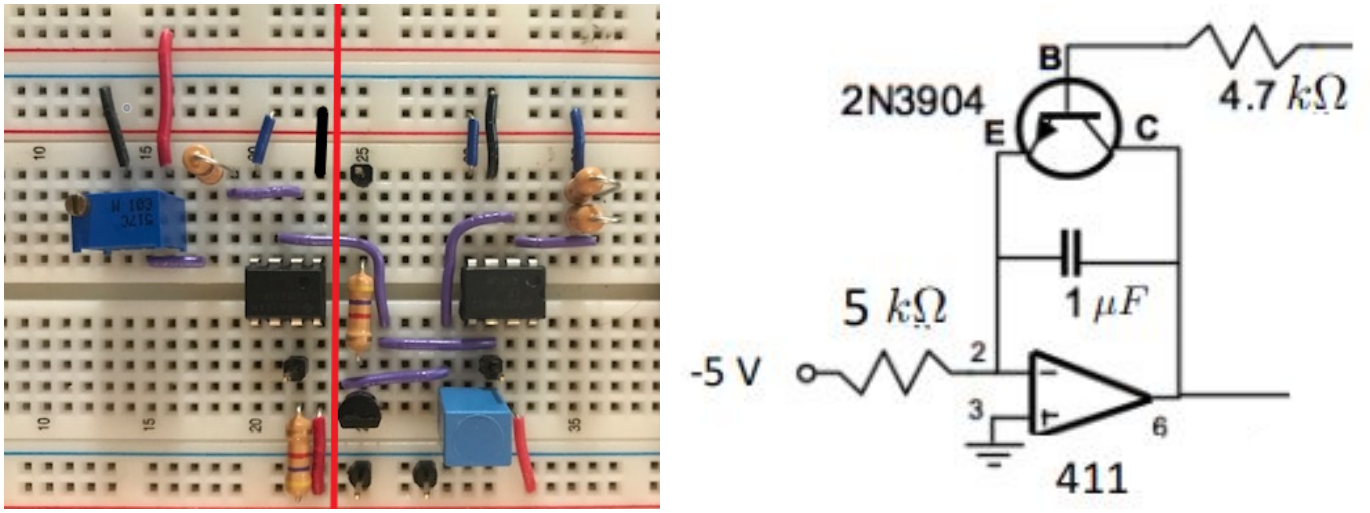


Figure 20: This figure shows the circuit layout for the voltage ramp generator component (right side of the red divider line). The circuit uses a LF411 JFET-INPUT Operational Amplifier (black rectangle), a +5V source (red wire), a -5V source (blue wire), one BJT (small black cylinder with a flat portion), a 1uF capacitor (blue rectangle), two 10kΩ resistors (gold orange black and brown stripes), a 4.7kΩ resistor (silver red purple and yellow stripes), channel 1 and channel 2 wires of the oscilloscope, and ground wires (black wires). All the other wires are used to connect the component parts. The wires of the oscilloscope have been taken out for circuit clarity but their respective black connection pins have been left in.

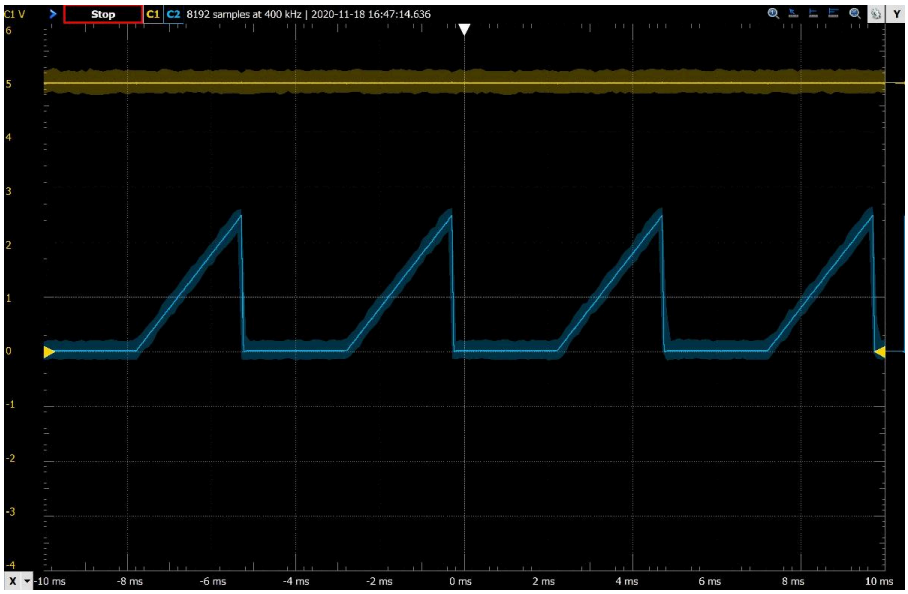


Figure 21: This graph shows the +5V supplies (yellow) and output (blue) of the voltage ramp generator that uses the LF411 OpAmp. As seen from the graph, the integrator OpAmp generates a voltage ramp that can be sent to the comparator circuit. The scales of the oscilloscope were 2ms/div and 1V/div.

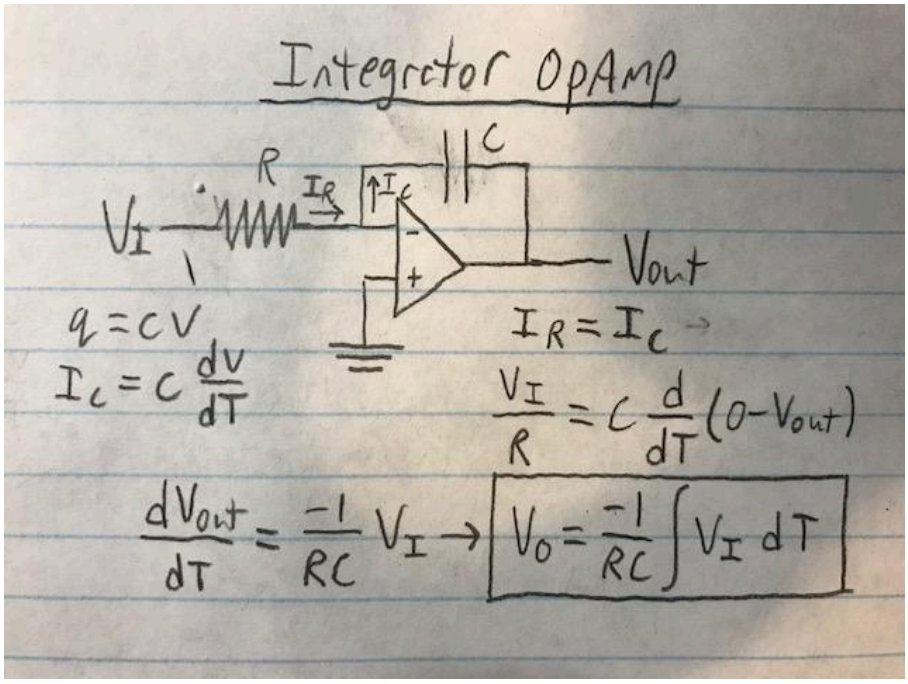


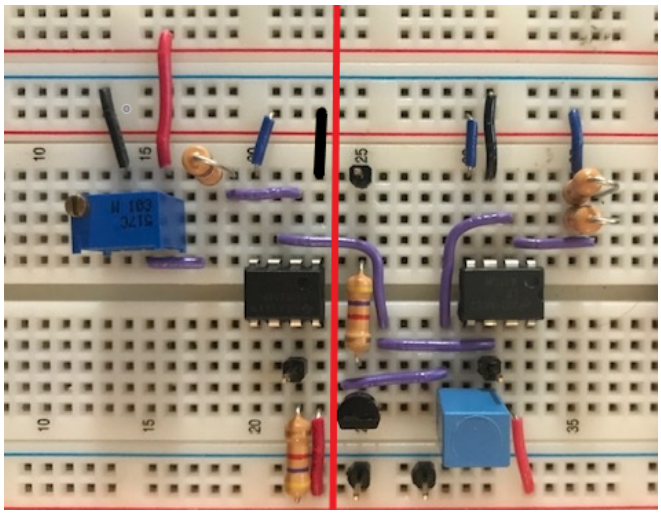
Figure 22: This figure shows how we know that the OpAmp in the voltage ramp generator is a Integrator OpAmp. It can be seen that the output voltage is proportional to the integral of the input voltage

7.2 Voltage Comparator

The second part of the ATC is a voltage comparator which uses a LM311 differential comparator. It compares the input DC voltage signal whose value is to be determined, with this voltage ramp (generated in the previous section) and generates an output pulse or the stop signal, when the voltage ramp exceeds the input voltage level. This differential comparator differs from the usual type of OpAmp, such as the 411, in that it is very fast,

has a large input resistance, yet is still cheap. The ATC generates a time window whose length is proportional to the analog voltage. For example, if you measure 1V the time window is very short but if you measure 5V the time window is 5 times as long. This device counts the number of pulses within that time window. To make the ATC we needed a starting point in time, a linear relation between the time and voltage, and a stopping point. Further, it is designed so that it can be coupled to almost anything, meaning a wide variety of input resistances and logic devices. In this circuit the comparator yields an HI or Lo voltage level (+5V or GND) depending on whether the value of the input ramp voltage is less than or greater than the input DC voltage set by the 10 kΩ potentiometer. Operationally, as the ramp voltage moves past the input DC voltage level, the output of the comparator makes a sudden transition from HI to Lo. This can be seen in figure 25. It is important to note that pin 1 of the LM311 Comparator must be connected to ground in order for the comparator to function properly. Additionally, the variable input DC voltage signal can be derived using the 10 kΩ (blue box) potentiometer. This set up can be seen in figure 23.

To make sure the circuit worked before moving on to the next component of the ADC, we tested the output to make sure its correct. To test the circuit, I adjusted the potentiometer so that a DC input voltage level between GND and +5V was provided to the LM311 and then I applied a pulse wave signal to the input of the transistor switch. This was done using the pulse function of the Wave Generator from the Analog Discovery 2. I should note that the duration of the pulses should be long enough for the value of the ramp to exceed the input DC signal level before the Lo to HI transition of the square wave Trigger Input occurs to the Base of the transistor. At the instant the ramp exceeds the DC signal level, the output of the Comparator will be observed to switch from a HI level to a Lo level. It then switches back to HI when the ramp is turned off by the Trigger Input square wave returning from Lo to HI. It is important to note that when the voltage of the negative pin of the comparator is higher than the positive pin, the output is Lo.



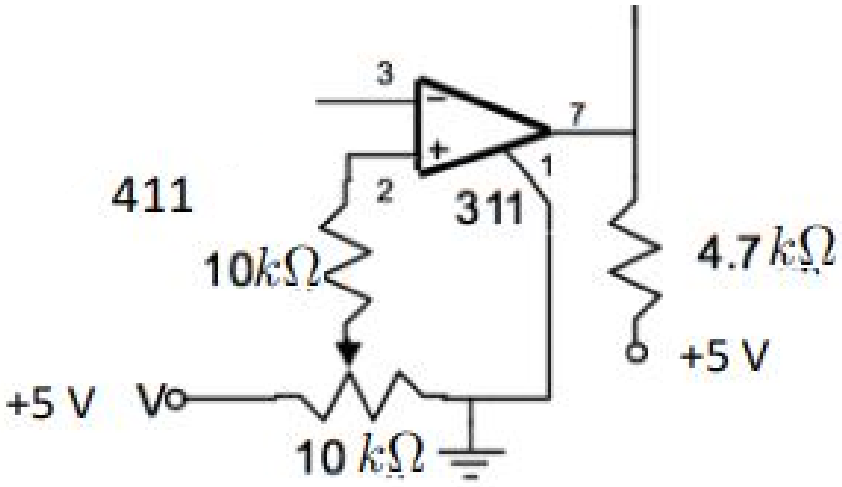


Figure 23: This figure shows the circuit layout for the voltage comparator component (left side of the red divider line). The circuit uses a LM311 differential comparator (black rectangle), a +5V source (red wire), a -5V source (blue wire), one 10kΩ resistors (gold orange black and brown stripes), one 4.7kΩ resistor (silver red purple and yellow stripes), a potentiometer (blue box), channel 1 and channel 2 wires of the oscilloscope, and ground wires (black wires). All the other wires are used to connect the component parts. The wires of the oscilloscope have been taken out for circuit clarity but their respective black connection pins have been left in.

7.3 Final ATC

Now that both the voltage ramp generator and the voltage comparator are constructed, we can connect them together to form the Analog to Time Converter as seen in figure 24. The maximum and minimum pulse widths were measured to be 2.5 ± 0.1 ms and minimum approaching 0ms respectively. This can be seen in figure 25. The width can be varied by adjusting the potentiometer.

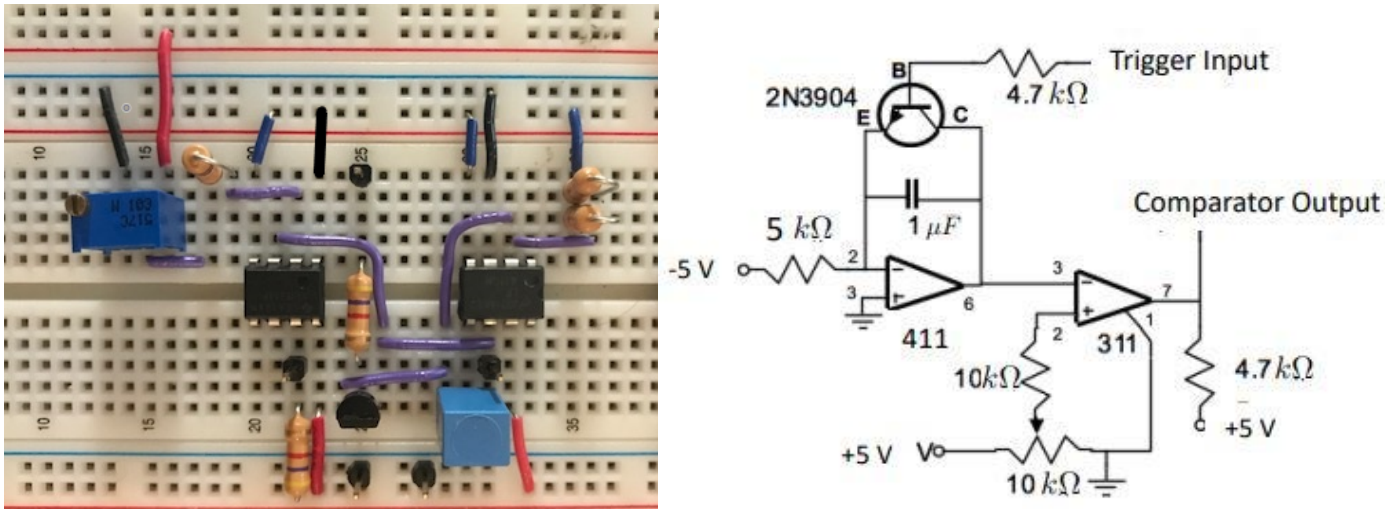


Figure 24: This figure shows the circuit layout for the Analog to Time Converter. The circuit uses a LM311 differential comparator (left black rectangle), a LF411 JFET-INPUT Operational Amplifier (right black rectangle), a +5V source (red wire), a -5V source (blue wire), three 10kΩ resistors (gold orange black and brown stripes), two 4.7kΩ resistor (silver red purple and yellow stripes), a potentiometer (blue box), one BJT (small black cylinder with a flat portion), channel 1 and channel 2 wires of the oscilloscope, and ground wires (black wires). All the other wires are used to connect the component parts. The wires of the oscilloscope have been taken out for circuit clarity but their respective black connection pins have been left in.

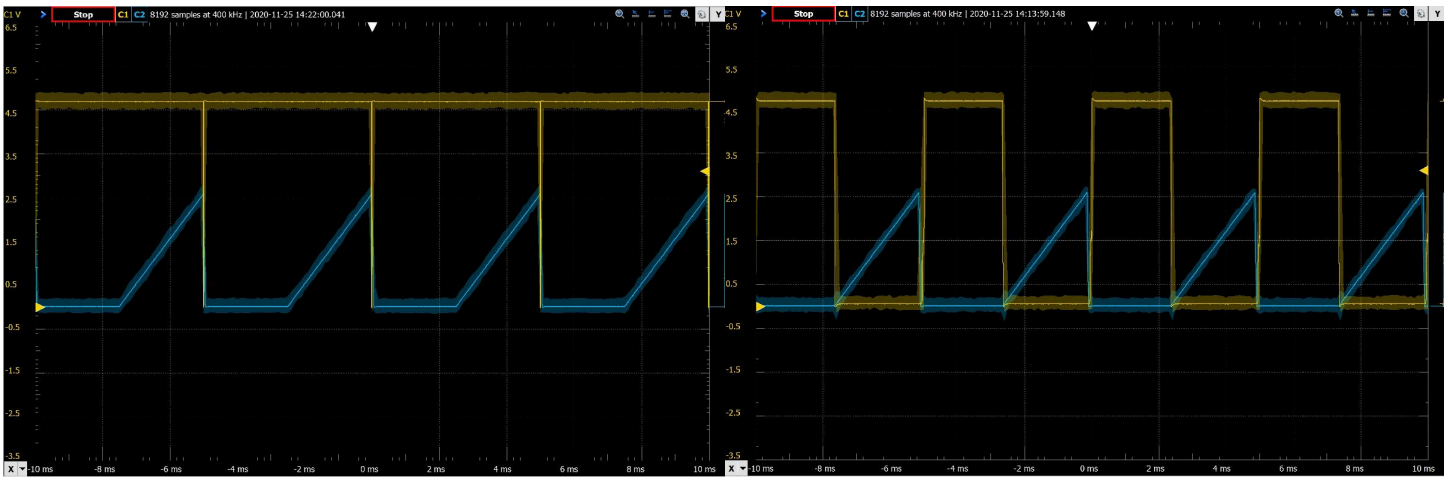


Figure 25: This graph shows the pulse wave (yellow) and output (blue) of the voltage ramp generator that uses the LF411 OpAmp. The pulse length can be controlled by the potentiometer which can be seen in both images. The left image shows the shortest pulse length and the right image shows the longest pulse length. The frequency of the pulse wave was 200Hz and had a 5V amplitude. As seen from the graph, the integrator

OpAmp generates a voltage ramp that can be sent to the comparator circuit. The scales of the oscilloscope were 2ms/div and 1V/div.

8. Control Logic

8.1 NAND Gate FlipFlop

The next component to be constructed was a flipflop with two NAND gates. An SR flip flop can be designed by the cross coupling of two NAND gates as seen in figure 26. The SR flip-flop can be considered as a 1-bit memory, since it stores the input pulse even after it has passed. The SR flipflop's operation can be described as follows. When both the S and R inputs are HI, then the Q output remains in the previous state, meaning it holds the previous data. When the S input is HI and the R input is Lo, then the flipflop will be in the reset state. Since the low input of NAND gate with R input drives the other NAND gate with 1, as its output is 1. So both the inputs of the NAND gate with S input are 1. This will cause the output of the flipflop to settle in reset state. Next, when S input is Lo and R input is HI, then the flipflop will be in set state. Since the low input of NAND gate with S input drives the other NAND gate with 1, as its output is 1. So both the inputs of the NAND gate with R input are 1. This will cause the output of the flipflop to settle in set state. When both the S and R inputs are low, then the flip flop will be in undefined state. Because the low inputs of S and R, violates the rule of flipflop's that the outputs should complement to each other. So the flip flop is in undefined state. These behaviors can also be seen in the logic diagram and the truth table in figure 27. Additionally, the control logic controls the counting of the clock pulses starting at the trigger pulse for the length of a specific time window.

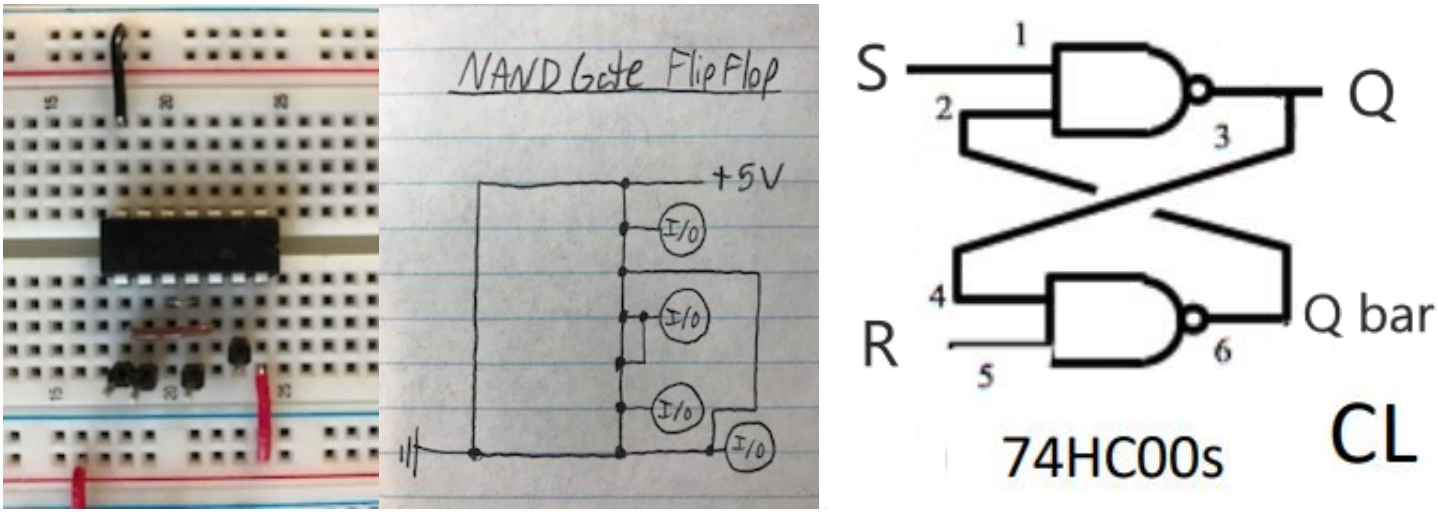
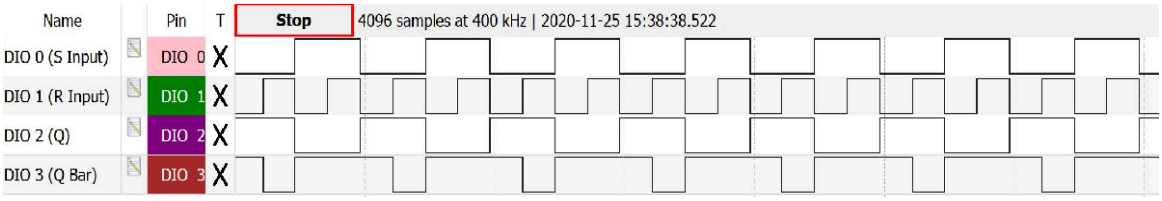


Figure 26: This figure shows the constructed circuit and circuit diagram of the SR flipflop. The circuit uses a 74HC00 Quad 2-Input NAND Gate (black rectangle), a +5V source (red wire), four digital I/O signal wires (pink, green, purple, and brown wires), and a ground wire. The two images can be connected as follows: The pink and green wires are input and the purple and brown wires are output. This can be verified from the pin layout in the background section.



$\bar{S}$	$\bar{R}$	Q	State
1	1	Previous State	No change
1	0	0	Reset
0	1	1	Set
0	0	?	Forbidden

Figure 27: This shows the digital input and output signals for each pin of the circuit. To the right is the SR flipflop truth table. As shown above, pins 0 and 1 represent digital input signals, and can be either Hi or Lo. Pins 2 and 3 represent digital output signals, and can also be HI or Lo based off the input signals. The frequency of DIO 1 was set to double that of DIO 0 so that we are able to see every combination of states. The output can be seen to match the truth table.

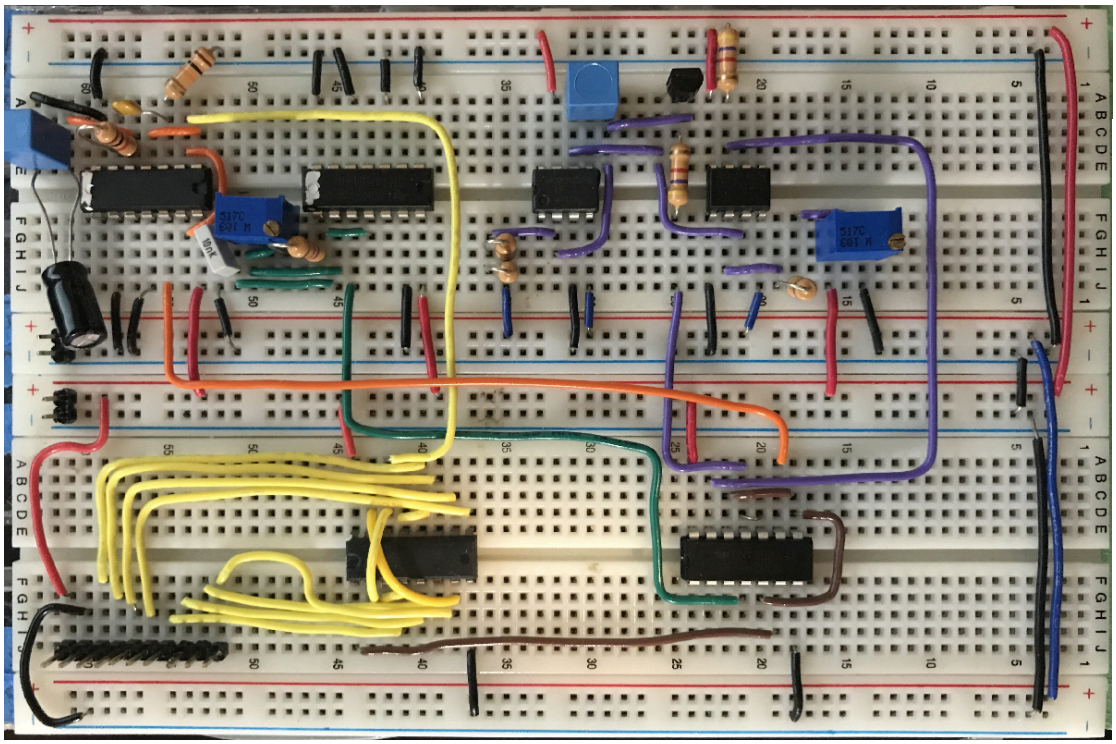
9. Integration of Components into an ADC

9.1 Combination of Previous Components

The next step was to assemble the whole ADC circuit, by inserting two more inverters, an extra NAND gate and inter-connecting various components according to the circuit diagram shown in figure 28. After these connections were made, I carefully rechecked that all required interconnections have been made. Luckily the first time I tried the final ADC together it worked so no troubleshooting was needed. A video of the final completed circuit operation can be found on YouTube: https://youtu.be/8hn0zoCUXGs.

The general operation of the ADC can be described as follows. First, I will discuss the Trigger Pulse Generator. The TPG is the device which determines the frequency at which the DC input signal is sampled. Its short negative going output is used for the following operations. It clears the decade counter, but since the decade counter requires a positive reset (CLR pulse), an additional digital inverter is added between the TPG and the decade counter which can be seen in the figure below. The TPG is also used to set the control flipflop which in turn opens a gate to allow the clock pulses, from the CPG, to pass to the decade counter. This is done with the use of NAND gates in an IC. Since negative-going signals are required to set the flip-flop, the necessary signal could have been obtained directly at the output of the TPG circuit. However this is not the case, in order to be certain that no gated clock pulses can arrive at the decade counter before the counter has been cleared, a slight time delay is provided by using a second inverter. This pre-caution helps with the functionality of the overall circuit. This inverter changes the short positive output pulse back to the short negative pulse required to set the flipflop to the desired state. In addition, the control flip-flop opens the BJT transistor switch on the ramp generator to initiate the ATC. When the ramp voltage reaches the threshold set by the DC input voltage, the negative transition at the output of the LM311 differential comparator resets the SR flipflop which in turn closes the gate at the output of the clock. This prevents any more clock pulses from reaching the counter. It also closes the BJT transistor switch thereby shorting the 1 µF integrating capacitor meaning that no charges flow through the capacitor. This terminates the production of the ramp and returns the output level of the integrating LF411 OpAmp to ground. At this instant, the LM311 comparator responds by changing its output to a HI value. It is important to note that when the voltage of the negative pin of the comparator is higher than the positive pin, the output is Lo. Since this whole process that occurs after the ramp voltage reaches the threshold set by the DC input level takes such a short time, the duration of the negative output pulse from the comparator is short

as well. The whole cycle which was described is then repeated when the next trigger pulse is produced by the TPG.



TPG: Orange
CPG: Green
Counter: Yellow
ATC: Purple
CL: Brown
+5 Source: Red
-5 Source: Blue
Ground: Black

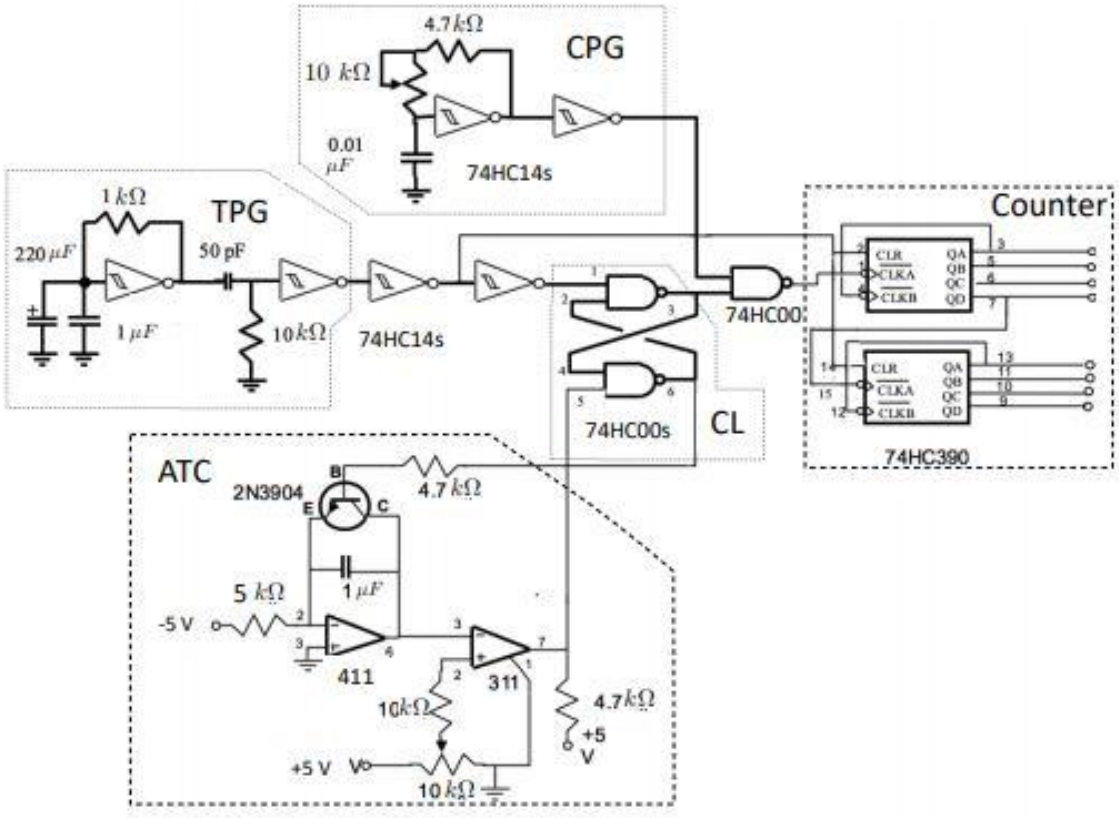


Figure 28: The top image shows the final ADC circuit where the components are defined by colour. The bottom image shows the finals ADC circuit design and all the values of the components.

9.2 Complete Circuit Measurements

Now that the circuit was completed and behaving properly, it was time to take measurements and make a timing diagram. I first measured the DC voltage level of the input signal (with the DMM) and then varied the clock frequency by adjusting the 10kΩ variable resistor in the CPG so that the decade counter displays the correct value of the input voltage. I measured the input signal to be 2.006 V and then varied the 10kΩ variable resistor so that the counter displayed the number 20. I then took a set of five data points for the input signal (using the DMM) and the LED output and then created a voltage conversion table which can be seen in figure 30.

Next a timing diagram was made so that each component's operation in the circuit can be seen. I tried to make this diagram with the logic analyzer for all digital components at once but that method was not working for me. The TA mentioned that drawing the timing diagram and explaining its operation would also work. The timing diagram can be seen in figure 29. What follows is an explanation of the circuit function with the timing diagram. As seen in the bottom waveform, the CPG creates a sequence of fast square pulses which passes through a inverter and then gets sent to a NAND gate where it then gets sent to ClockA of the counter. In the second waveform, the TPG creates a low frequency pulse train that has two paths. The first path being through the Schmitt-trigger inverter which resets the counter by giving a HI pulse to the clear pins of the counters. The second path being that it passes through another inverter and is the S input to the control logic. The TPG's start pulse signals the ACT to generate a voltage ramp which then provides a HI output back to the control logic while the ramp voltage is below the threshold of the comparator or input voltage. It is important to note that when the voltage of the negative pin of the comparator is higher than the positive pin, the output is Lo. The ATC generates a time window whose length is proportional to the analog voltage. For example, if you measure 1V the time window is very short but if you measure 5V the time window is 5 times as long. This device counts the number of pulses within that time window. To make the ATC we needed a starting point in time, a linear relation between the time and voltage, and a stopping point. The control logic is a modified flipflop that controls the counting of the clock pulses starting at the trigger pulse for the length of the time window. The time window can be seen in the 7th waveform. The counter keeps track of the number of pulses within that time window and displays it on the LED (8-bit number). Each counter waveform can be seen (top 8 waveforms, top being the 8th counter). The 2nd and 6th waveform represent the starting and ending points for the time window. The 4th waveform represents the combination of the CPG with the time window which is the number of pulses that needs to be counted i.e. voltage.

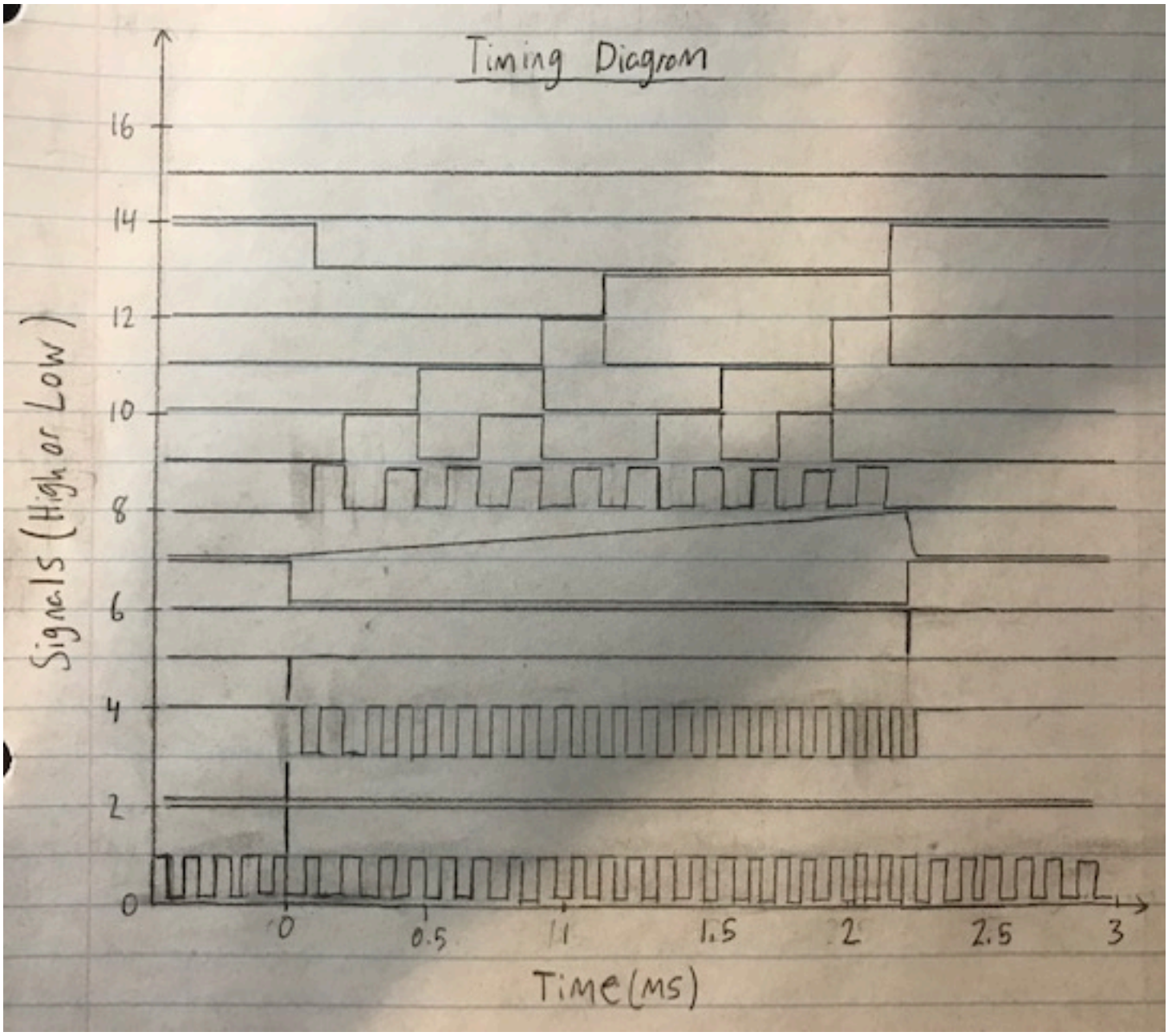


Figure 29: This figure shows the timing diagram for different components of the final ADC circuit. Each waveform can be characterized as follows. The top 8 waveforms are the counters with counter 8 at the top. Now from bottom to top the waveforms are CPG, TPG, CLKCLR, CLKA, CLInputOne, Comparator, ATC Trigger, and Integrator. The scales of the axis are in ms and HI / Lo.

Voltage Conversion Table

Input/DMM (V)	Output/LED
1.006	10
1.496	15
2.011	20
2.503	25
3.009	30

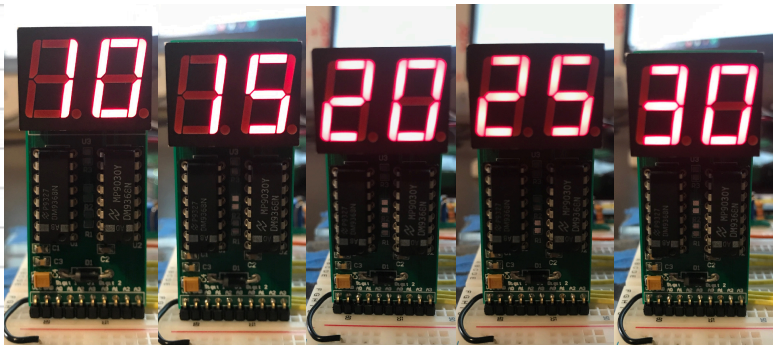


Figure 30: This figure shows the voltage conversion table of the input signal and LED output. The uncertainty of the DMM voltage measurements were $\pm 2.9\text{x}10^{-4}\,V$ because it is a digital device. Meaning that the uncertainty can be found by dividing half the least uncertain digit by square root of 3.

10. Problems Encountered

Overall, there were not many problems that I encountered in this lab but there were some minor bumps. The two problems that I encountered both had to do with incorrect wiring. The first problem I ran into was incorrect wiring of the counter. The output was only showing the rightmost digit and the leftmost digit was incorrect. The way I found the error was by re-checking all the connections with the circuit diagram and I found that two of the wires went to the same counter pin where one should have not gone there. The second problem that I ran into was that the output of the voltage comparator (of the ATC) was not showing up correctly on the oscilloscope when tested. The voltage ramp was working correctly so I knew to debug the comparator. To debug this problem, I first re-checked all the wiring for the 311 and realized that pin 1 of the 311 was not grounded. Once I grounded pin 1 the problem was fixed. Luckily when all the components came together to make the final ADC it worked on the first try.

11. Conclusion

In previous experiments we have learned about different aspects of analog and digital circuits and how they function. We combined all of that knowledge and implement a working analog-to-digital convertor (ADC) circuit. We used some of the devices we have investigated previously in this course and some devices we have not seen. A device that we had not seen before was a Schmitt-trigger Inverter. The analog-to-digital convertor is capable of converting an analog voltage in a digital (binary) representation. The components of the ADC that were constructed were the trigger pulse generator, short pulse rectifier, clock pulse generator, counter, voltage ramp generator, voltage comparator, and control logic. For each component, we talked about how the circuit was constructed, tested, and how it functions with pictures and explanations.