```verilog
always @ (addr)
 begin
    if(addr<16'h0100)
        {rom_sel, ram_sel}=2'b10;
    else if(addr>=16'h0100&&addr<16'h0300)
        {rom_sel, ram_sel}=2'b01;
    else
        {rom_sel, ram_sel}=2'b00;
 end
```