

```
module cu_contr1(  
    input clk,  
    input fetch,  
    input rst,  
    output reg cu_ena  
);  
always @ (posedge clk)  
begin  
    if(!rst)  
    begin  
        cu_ena=0;  
    end  
    else if(fetch)  
    begin  
        cu_ena=1;  
    end  
end  
end  
endmodule
```