```verilog
module flags(
    input clk,
    input rst,
    input flag_set,
    input [7:0] flag_in,
(* DONT_TOUCH= "1" *)    output reg [7:0] flag_value
    );
    always @ (posedge clk or negedge rst)
    begin
        if(!rst)
        begin
            flag_value=8'h00;
        end
        else if(flag_set)
        begin
            flag_value=flag_in;
        end
    end
endmodule
```