

```
reg [15:0] ram [767:256];  
.....  
assign outdata=(read&&ena)?ram[addr]:16'hzzzz;  
always @ (posedge write)  
    begin  
        ram[addr]=indata;  
    end  
.....  
reg [15:0] rom [255:0];  
assign data=(read&&ena)?rom[addr]:16'hzzzz;
```