```
module clock(
    input clk,
    input reset,
    output reg fetch,
    output clk_r
    );
    integer cnt=0;

    assign clk_r=~clk;
    always @ (negedge clk)
    begin
        if(!reset)
        begin
            cnt=0;
            fetch=0;
        end
        else
        begin
            if(cnt==3)
            begin
                cnt=cnt+1;
                fetch=1;
            end
            else if(cnt==7)
            begin
                cnt=0;
                fetch=0;
            end
            else
            begin
                cnt=cnt+1;
            end
        end
    end
endmodule
```