Something something something physics

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for the degree of Doctor of Philosophy

Abstract

This thesis describes the optimisation of the calorimeter design for collider experiments at the future Compact LInear Collider (CLIC) and the International Linear Collider (ILC). The detector design of these experiments is built around high-granularity Particle Flow Calorimetry that, in contrast to traditional calorimetry, uses the energy measurements for charged particles from the tracking detectors. This can only be realised if calorimetric energy deposits from charged particles can be separated from those of neutral particles. This is made possible with fine granularity calorimeters and sophisticated pattern recognition software, which is provided by the PandoraPFA algorithm. This thesis presents results on Particle Flow calorimetry performance for a number of detector configurations. To obtain these results a new calibration procedure was developed and applied to the detector simulation and reconstruction to ensure optimal performance was achieved for each detector configuration considered.

This thesis also describes the development of a software compensation technique that vastly improves the intrinsic energy resolution of a Particle Flow Calorimetry detector. This technique is implemented within the PandoraPFA framework and demonstrates the gains that can be made by fully exploiting the information provided by the fine granularity calorimeters envisaged at a future linear collider.

A study of the sensitivity of the CLIC experiment to anomalous gauge couplings that effect vector boson scattering processes is presented. These anomalous couplings provide insight into possible beyond standard model physics. This study, which utilises the excellent jet energy resolution from Particle Flow Calorimetry, was performed at centre-of-mass energies of 1.4 TeV and 3 TeV with integrated lumi-

nosities of 1.5ab^{-1} and 2ab^{-1} respectively. The precision achievable at CLIC is shown to be approximately one to two orders of magnitude better than that currently offered by the LHC.

Finally, a study into various technology options for the CLIC vertex detector is described.

Declaration

This dissertation is the result of my own work, except where explicit reference is made to the work of others, and has not been submitted for another qualification to this or any other university. This dissertation does not exceed the word limit for the respective Degree Committee.

Andy Buckley

Acknowledgements

Of the many people who deserve thanks, some are particularly prominent, such as my supervisor…

Preface

This thesis describes my research on various aspects of the LHCb particle physics program, centred around the LHCb detector and LHC accelerator at CERN in Geneva.

For this example, I'll just mention Chapter **??** and Chapter **??**.

Contents

"Writing in English is the most ingenious torture ever devised for sins committed in previous lives."

— James Joyce

Chapter 1

Capacitively Coupled Pixel Detectors for the CLIC Vertex Detector

"There, sir! that is the perfection of vessels!"
— Jules Verne, 1828–1905

1.1 Introduction

Successful identification of heavy-flavour quarks and tau-leptons relies upon precise reconstruction of the secondary displaced vertices produced in the decay of these particles as well as accurate association of the daughter tracks to those vertices. To achieve this for the CLIC experiment very high spatial resolution, of approximately 3 μm and good geometric coverage extending to low θ values are essential. The vertex detector must also have a low material budget, less than 0.2 X_0 per layer, as to not impact the performance of the other sub detectors and a low occupancy, aided by time-tagging to an accuracy of 10 ns, to counteract the high beam-induced backgrounds found near the impact point.

There are no commercially available technology options that fulfil all the criteria for the vertex detector, which had led the CLIC experiment to consider a variety of new technology options. The focus of this chapter is the use of high voltage complementary metal-oxide-semiconductor (HV-CMOS) active sensors coupled to a separate readout ASIC for the CLIC vertex detector.

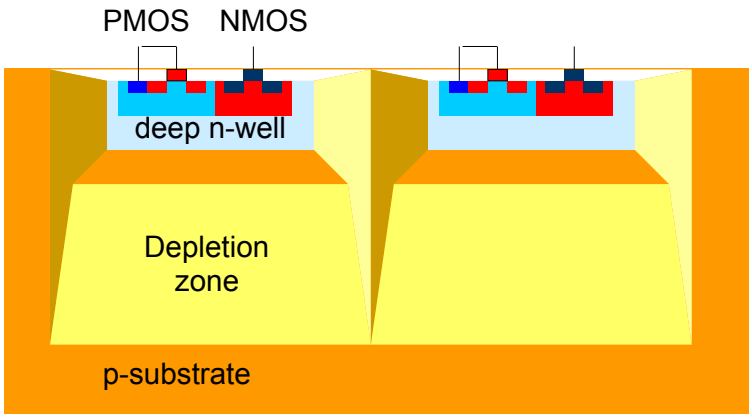


Figure 1.1: HV-CMOS diagram.

1.1.1 HV-CMOS

There are two classifications for pixel detectors; hybrid detectors where a passive sensor is bump-bonded to a separate readout chip and fully integrated where the collection diode is built upon the same wafer as the readout circuitry. Both of these technology options find the CLIC experimental conditions extremely challenging. Hybrid technologies struggle to achieved both the radiation tolerance and the functionality in the readout circuitry, while fully integrated circuits have too slow readout times due to limitations on the applied bias voltage.

HV-CMOS is adapted to the CLIC experimental conditions as the n-MOS and p-MOS transistors forming the integrated amplifier (or generic in-pixel logic operations in general) for collecting the signal are embedded within a deep n-well, as shown in figure 1.1. This acts as both the collection diode as well as providing shielding to the circuitry from the beam induced radiation. With the integrated circuitry shielded from the p-substrate it becomes possible to apply a large bias voltage to the substrate to widen the depletion region meaning that the main part of any signal deposited in the detector will be transferred via drift as opposed to diffusion, which provides the fast readout times required by the CLIC experiment.

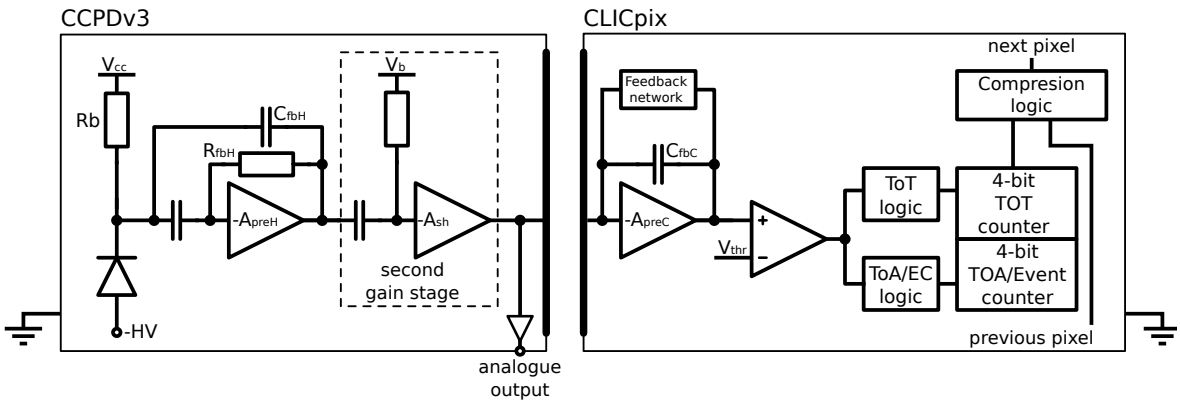


Figure 1.2: Schematic of CCPDv3 and CLICpix pixels.

HV-CMOS devices are strong candidates for the CLIC vertex detector, however, they do have limitations such as noise from interference between the n and p doped wells of the n-MOS and p-MOS transistors that sit within the deep n well. This noise will grow with the number of n-MOS and p-MOS devices on the wafer and so ultimately restricts the complexity of the in-pixel operations that can be performed. There are also topological difficulties such as the difficulty of applying the CMOS process to all sizes and the fact that the deep n well does not occupy the full space of the pixel.

To minimise the material budget for the vertex detector, the pixels used are designed to be as thin as possible. This means the signal from the HV-CMOS will be small as the depletion region will be thin. To counter this, in-pixel signal amplification was applied to the HV-CMOS devices, as shown in figure 1.2. This increases the signal going to the readout ASIC, which also counteracts the intrinsically small capacitance between the HV-CMOS and readout ASIC.

1.1.2 CLICpix

The readout ASIC in this study is the CLICpix, which is a charge integrating amplifier connected to a discriminator as shown in figure 1.2. The output to this discriminator is then used as the input for further logic operations that record the magnitude, using a Time over Threshold (ToT) measurement, and time of arrival of the collected charge.

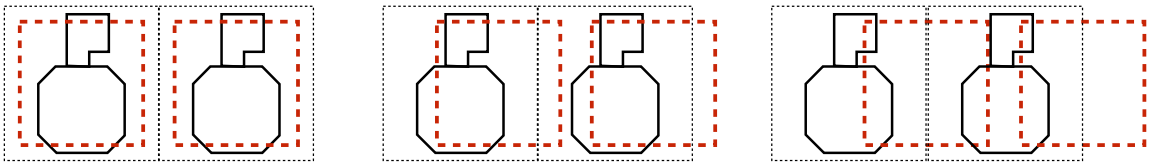


Figure 1.3: Schematic of alignment of CCPDv3 and CLICpix sensors studied in this analysis. The red dotted line represents the CCPDv3 and the solid black line represents the CLICpix. From left to right; centred pixels, 1/4 offset (6.25 μm) and 1/2 offset (12.5 μm).

1.1.3 Capacitive Coupling

Solder bump-bonding is the typical method that is used for connecting active pixel sensors to the readout ASIC, however, the solder adds to the thickness of the sensor significantly as well as raising the cost. A viable alternative to this procedure is the replacement of the bump-bonding with a thin uniform layer of glue that forms a capacitive connection between the active pixel and readout ASIC. The mechanical tolerances on the alignment of the active pixel sensor and readout ASIC when applying this glueing procedure are the focus of this study.

1.2 Construction

While replacing solder bump-bonding with a thin layer of glue in the construction of the sensors for the vertex detector offers benefits, such as reductions in the material budget and cost, the manufacturing procedure could lead to misalignments between the active pixel sensor and the readout ASIC. To determine the impact of these misalignments a number of sensors were constructed using the gluing procedure that contained offsets between the HV-CMOS and CLICpix, as shown in figure 1.3. A table 1.1 contains a summary of all the samples used in this study.

The pitch of the pixels produced was 25 μm and the matrix size was 64×64. The full details of the gluing process can be found here (CERN NOTE CITE) along with a study into the absolute precision of the manufacturing procedure. It was found that for devices constructed in an identical fashion to those considered here, the glue layer thicknesses were less than 1 μm and the precision on the pixel positioning was less than 0.5 μm.

Assembly	Alignment
SET9	Centred
SET10	$\frac{1}{4}$ Offset
SET11	$\frac{1}{2}$ Offset
SET12	Centred
SET13	Centred
SET14	$\frac{1}{2}$ Offset
SET15	Centred
SET16	$\frac{1}{2}$ Offset

Table 1.1: Description of alignment of sensors.

1.3 Device Characterisation

This section describes the electrical tests that were performed on the sensor designed to determine the properties of the HV-CMOS and CLICpix.

1.3.1 CLICPix Calibration

Experimental Setup

A radioactive source, Sr^{90}, calibration that was applied to the sensors is presented here. In this procedure the unstable Sr^{90} undergoes β^- decay to form Y^{90}. The Y^{90}, as it too is unstable, undergoes β^- decay to form Z^{90}, which is stable. Each β^- decays produce an e^- and a $\bar{\nu_e}$, and it is the e^- that are used to test the sensitivity of the sensor. The Sr^{90} source used had an activity of 29.6 MBq.

This radioactive source was positioned directly on top of the sensors and measurements were made of both the ToT output from the CLICpix and the HV-CMOS analogue signal for individual pixels on the sensor. The on-pixel event counter was used to veto all events where multiple hits occurred within the time window for a given event.

The HV-CMOS was biased to 60V during this experiment. The HV-CMOS analogue output has a DC output of ≈ 1.15 V and saturation occurs around a signal height of 700 mV. Examples of the HV-CMOS output can be found in figure 1.4.

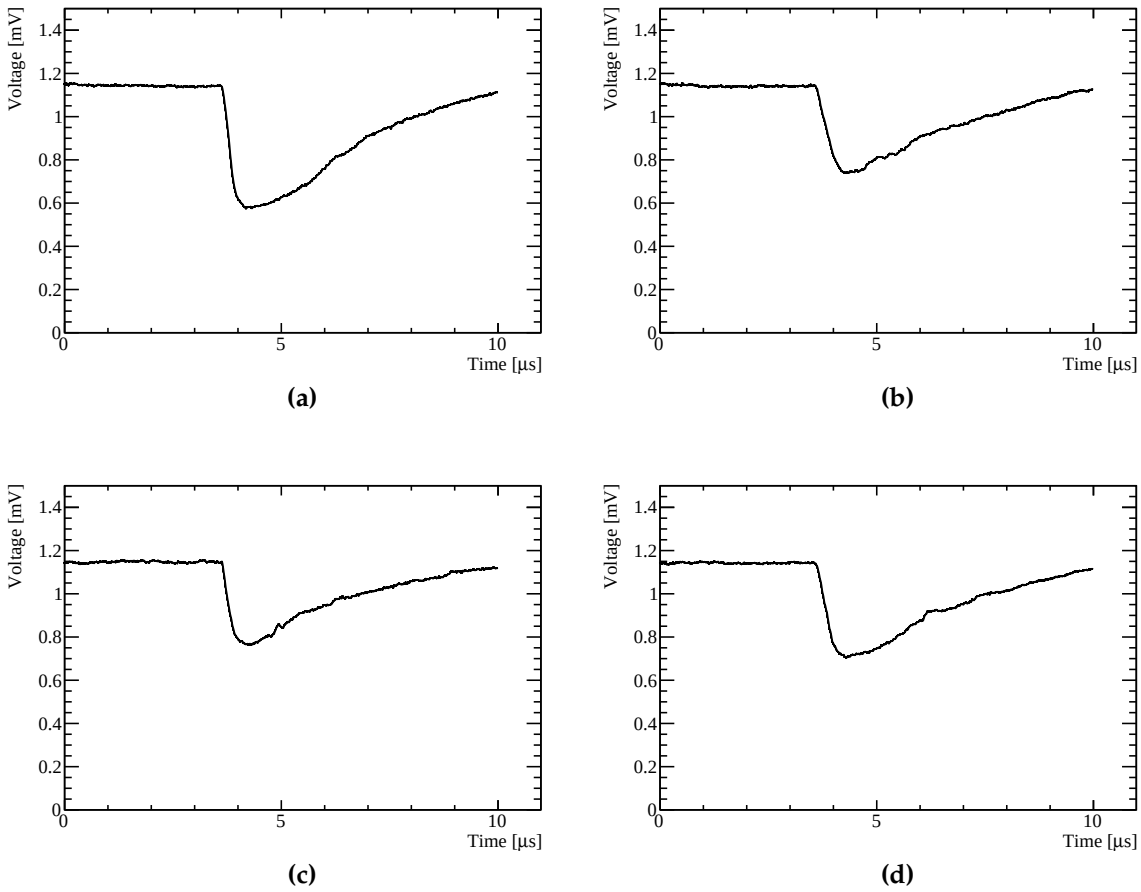
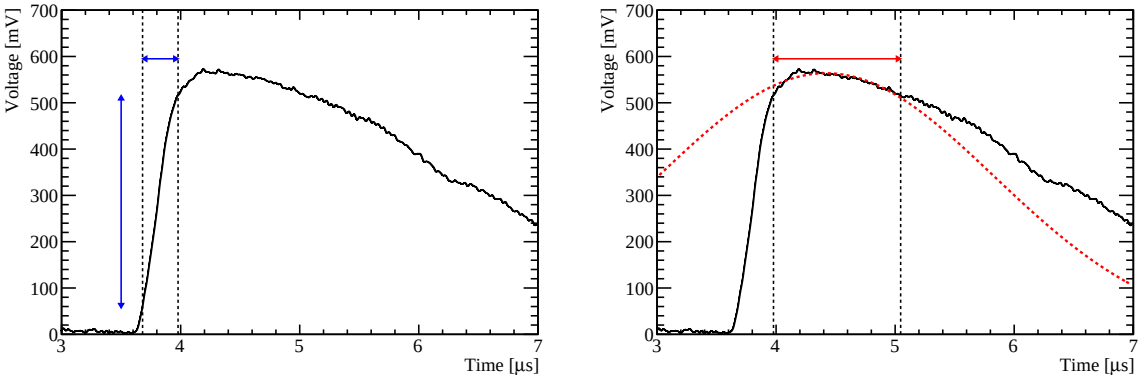


Figure 1.4: HV-CMOS voltage as a function of time for pulses created by radioactive Sr^{90} source.



(a) Rise time. The arrows show the change in time and voltage as the pulse goes from 10% to 90% of the raw pulse height. This time is used as the definition of the rise time in the subsequent analysis.

(b) Pulse height. The red dotted line is a Gaussian fit to the peak of the pulse. The peak is defined as data points where the voltage is in excess of 90% of the raw pulse height.

Figure 1.5: Analysis of HV-CMOS voltage as a function of time for pulses created by radioactive Sr^{90} source.

Analysis

The quantities of interest related to the HV-CMOS output are the pulse height and a rise time. The offset voltage was subtracted from the HV-CMOS analogue output and the pulse height inverted before the following analysis was applied.

The pulse height was taken as the mean of a Gaussian fit to the peak of the HV-CMOS output voltage distribution. Such peaks were defined as the data points set that were at or above 90% of the raw peak height, the maximum voltage change recorded. The application of a Gaussian fit provides a more robust metric for categorising the pulse height that is not dependant on minor fluctuations in the voltage. The rise time was calculated as the time taken for the voltage to go from 10% to 90% of the raw peak height. This definition also makes the rise time metric more robust against fluctuations changing the absolute peak height. Examples of the calculation of these metrics for a given pulse are shown in figure 1.5.

For each device the HV-CMOS pulse output was recorded for 15 pixels running along one edge of the 64 $\times$ 64 matrix and in the subsequent analysis the data for all 15 pixels was combined.

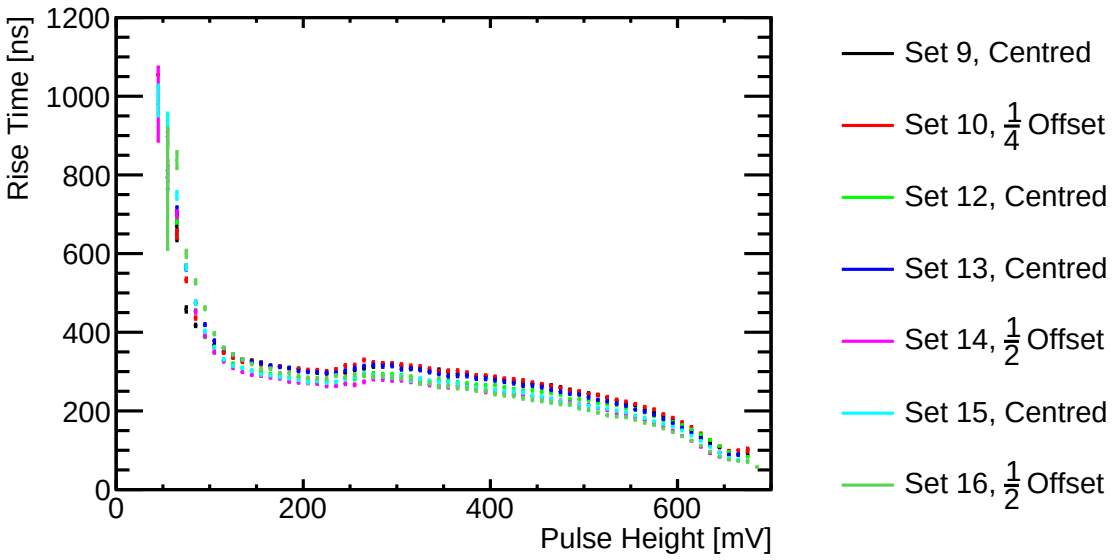


Figure 1.6: HV-CMOS voltage rise time as a function of pulse height.

Results - Rise Time vs Pulse Height

The mean rise time as function of pulse height is shown in figure 1.6. This was determined by binning the events in terms of pulse height and determining the mean rise time for events in each of those bins. The pulse height was binned using a bin width of 4 mV ranging from 0 to 700 mV. At least 100 measurements per pulse height bin were used for the calculation of the average rise time. The error bars on this figure show the standard error in the mean rise time.

The data in figure 1.6 indicates that the rise time is approximately 300 ns across all samples considered and that this is largely independent of pulse height for all but the largest and smallest values. For large pulse heights the rise time is reduced while for low pulse heights the rise time is much larger. This is to be expected as the pulse heights is proportional to the signal from the e^- and the larger this signal the larger the rate of change of output voltage from the HV-CMOS and so the lower the rise time. As all HV-CMOS devices in this analysis were constructed in the same manor it is expected that all devices behave similarly, which is what we observe.

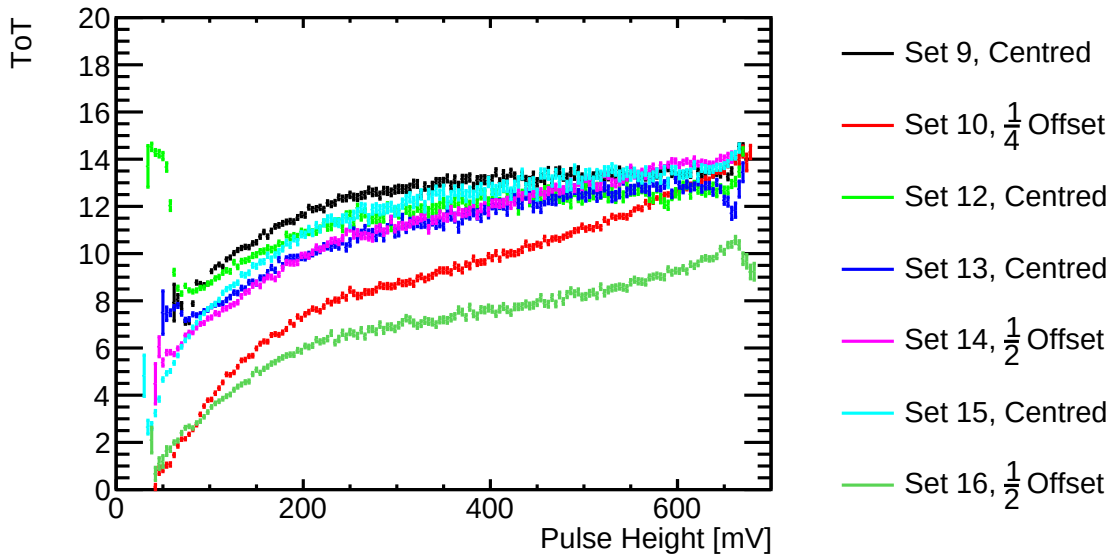


Figure 1.7: CLICpix ToT as a function of HV-CMOS voltage pulse height.

Results - ToT vs Pulse Height

Figure 1.7 shows the mean ToT as a function of pulse height. The determination of the mean and error bars for the ToT measurement is identical to that described in section 1.3.1 for the rise time measurement.

The distribution of mean ToT against pulse height show that for centred samples the ToT increases with pulse height up to pulse heights of approximately 300 mV upon which the mean ToT saturates at ≈ 13. The ToT uses a four-bit readout and so is confined to the range 0 to 15. It is expected that the $\frac{1}{4}$ and $\frac{1}{2}$ offset samples should have a lower ToT than the centred samples. This is due to the splitting of the HV-CMOS signal between adjacent CLICpix ASICs. The greater the offset the smaller the signal to the target CLICpix and the lower the ToT. This is what is observed when comparing the centred samples to the $\frac{1}{4}$ offset sample and one, Set 16, of the $\frac{1}{2}$ offset samples. The other $\frac{1}{2}$ offset sample, Set 14, appears to behave as a centred sample indicating that this sample may have been manufactured with no offset.

Results - Cross Couplings

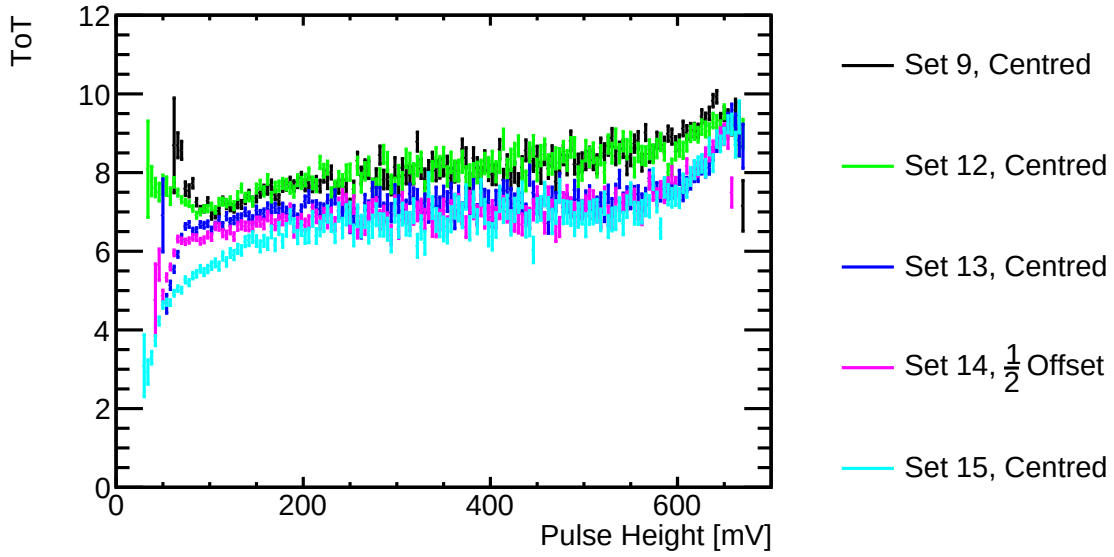
It is possible to further understand the splitting of the HV-CMOS signal between multiple CLICpix ASICs by examining the ToT on adjacent pixels, along the direction of the offset, as a function of the HV-CMOS pulse height. This is shown in figure 1.8a for all devices that are centred and Set 14, which behaves as a centred device, and in figure 1.8b for the $\frac{1}{4}$ offset sample and the remaining $\frac{1}{2}$ offset sample, Set 16.

No correlation between the adjacent pixel ToT and the HV-CMOS pulse height is observed for the samples shown in figure 1.8a for all but the lowest values of pulse height. The correlation observed at low pulse heights may arise due to the signal e^-, which is primarily recorded in the target pixel, depositing a small amount of charge in the adjacent adjacent pixel as the e^- may not be traveling normal to the pixel surface. However, as this is not present in all samples this could also indicate a small offset in the samples showing the correlation that may fall within the manufacturing tolerances.

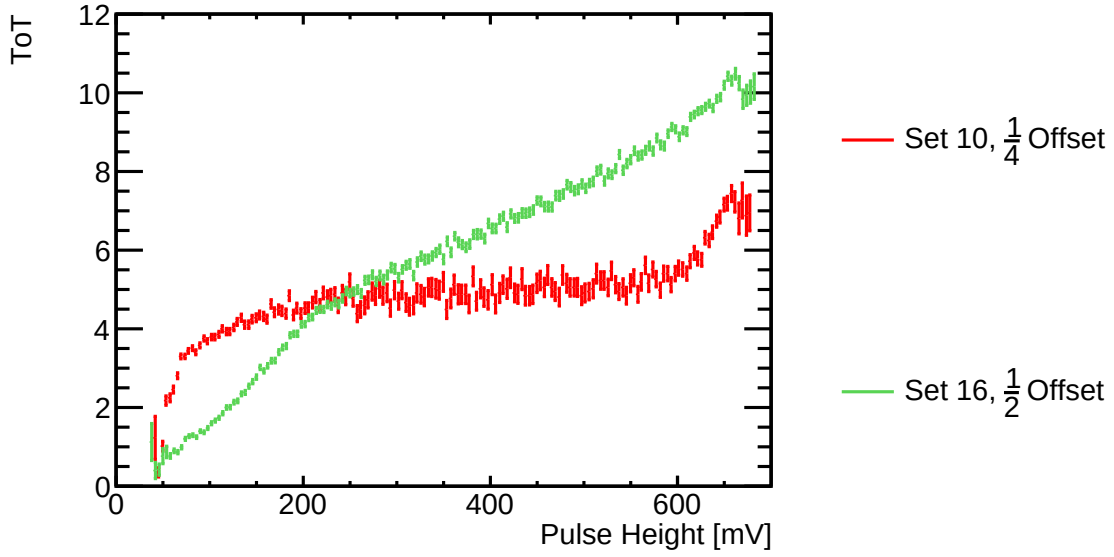
There is, however, a strong correlation, shown in figure 1.8b, between adjacent pixel ToT and the HV-CMOS pulse height for Set 16, which is one of the $\frac{1}{2}$ offset samples. This distribution is almost identical to the the target pixel ToT distribution as a function of HV-CMOS pulse height, which is what would be expected given an equal signal charge sharing between the two readout ASICs. This indicates the charge sharing is well understood for this $\frac{1}{2}$ offset sample.

For the $\frac{1}{4}$ offset sample correlation is present only for low pulse heights as was the case for the centred samples. However, the mean ToT within the uncorrelated region is centred around ≈ 5 units of ToT, which is lower than was observed for the centred samples. This is due to the offset reducing the total capacitance between the HV-CMOS and CLICpix in comparison to the centred samples and thus reducing the ToT recorded.

Cross coupling was observed in one of the $\frac{1}{2}$ offset samples and, assuming that the other $\frac{1}{2}$ offset sample was manufactured incorrectly, then charge sharing was well understood for these $\frac{1}{2}$ offset samples. No cross coupling was observed for any of the other samples considered in this analysis.



(a)



(b)

Figure 1.8: CLICpix ToT on adjacent pixel along the direction of the offset as a function of HV-CMOS voltage pulse height.

1.3.2 Test Pulse Calibration

The next test that was performed involved directly injecting a voltage pulse of fixed height directly into the CLICpix ASIC, which gives a measure of the performance of the CLICpix independently of the HV-CMOS sensor. Due to the construction of the sensor it was not possible to access the HV-CMOS to perform a similar test to isolate its performance.

1.3.3 Experimental Setup

In this study a voltage pulse of fixed height was injected into 1 out of every 16 pixels from the matrix, while masking the others, and the ToT from the CLICpix recorded. This repeated 15 more times using different mask configurations until the entire matrix had been samples. The masking of pixels was done as to not overload the matrix by running all pixels at ones. This procedure was repeated 100 times so that average ToTs could be recorded. The pulse height injected into the CLICpix varied from 2 to 180 mV in steps of 2 mV.

TODO: Describe surrogate function fit and column structure.

1.4 Test Beam Analysis

1.4.1 Test Beam Area

Description of test beam, site and telescope.

1.4.2 Efficiency

- Description of masks and why they need to be applied.
- Alignment description.
- Efficiency calculations and conclusions.

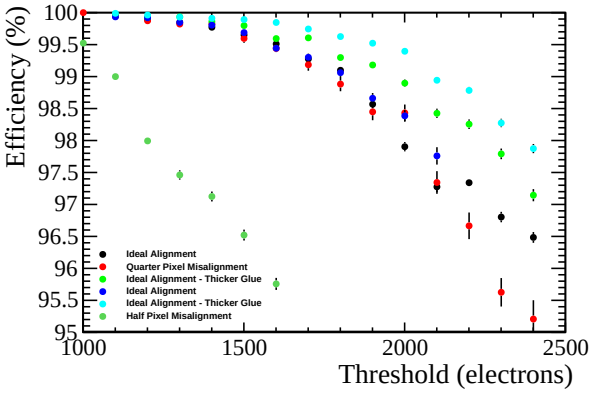


Figure 1.9: Efficiency vs threshold.

Colophon

This thesis was made in LaTeX 2_ε using the "hepthesis" class [1].

Bibliography

[1] Andy Buckley. The hepthesis LaTeX class.

List of figures

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