CECS 460 – System on a Chip Design (Spring 2017)
California State University, Long Beach
College Of Engineering
Department of Computer Engineering and Computer Science

Instructor: John Tramel

Office:	T-Th:	5:00 to	5:55	ECS-532
Lecture:	T-Th:	6:00 to	6:50	ECS-302 (5638)
Lab:	T-Th:	7:00 to	7:15	ECS-412 (5639)

Email: John.Tramel@csulb.edu- Please put "460" in title

Grading:
Midterm 1…….15%
Midterm 2…….15%
Final Exam……30%
Lab Assignments……30%
Homework and Quizzes……10%

Please note that this is a project oriented class and performance on the projects is essential to mastering this class. Chronically late or incomplete projects will be devalued. To ensure that you receive the most credit for your efforts please complete all projects in a timely manner.

Course Stated Goals

- System on Chip (SOC) design applications. Variety of SOC designs built as class project involving both hardware & software with hardware/software integration problems. Design reviews, specification, team design implementation stressed with project planning & tracking for system level design problems.
- I consider this course a capstone class regarding digital design and hope that all of you will put forth the effort to make all of the concepts and techniques presented in the class your own.

Tentative Course Outline

Week	Topics
Weeks 1 – 5	Introduction to SOC. Discussion of methodology, practices and tools. Review of SOC design flow. Introduction to TramelBlaze processor.
Weeks 6 – 10	System on a chip architecture development. Device specification and project planning. Partitioning of design. Device interconnect. Allocation of functionality between hardware and software.
Weeks 11 – 15	System on a chip implementation and execution. Interfacing to external devices. Design reviews and presentations.

Textbook and Materials

Instructor's notes and handouts.

Primary Text

FPGA Prototyping by Verilog Examples Pong P. Chu Wiley (3rd Edition)
"Digilent Nexys Prototyping Board" – www.digilentinc.com

Secondary Text

Reuse Methodology Manual for System-on-a-chip Designs by Michael Keating

Homework and Quizzes

Homework will be assigned from both the textbook and from instructor designed problems. The purpose of the homework is to help constitute the student with the important, and sometimes difficult, concepts related to lectures and/or assigned reading. Note: due dates will be given when homework is assigned -- late homework will not be accepted. "Pop quizzes" will be given to help solidify lecture/reading material. Missed quizzes may not be made up.

Lab Assignments

The due dates for each lab assignment will be announced when assigned. Students should plan ahead for difficulties and not put off working on the assignments until the last minute. I *strongly* suggest that you start to work on your lab assignments as soon as you receive them. The *secret to success* is putting some careful work "up front," solidifying your design, and finishing it as soon as possible. **The maximum score on late projects will drop one letter grade every week (No projects accepted after two weeks).**

Scheduled Lab Hours

The time that our class is scheduled to be in one of the CECS labs is primarily used for the instructor to assist you in your lab assignments and to review them once completed. In order to successfully complete the projects you will need to work on them outside of the scheduled lab time. If the lab assignment involves using one of the EDA tools on the computers in a CECS lab, then you will have to find your own time to work on those computers. If the lab assignment involves the prototyping/building of a digital circuit, then you will have to do the work on your own time, and come into our scheduled lab time with the assignment completed and ready to be checked (graded).

General Comments

This class is a conclusion to the digital design sequence here at CSULB which started with 201, proceeded to 301 through 360 and now 460. The student is expected to begin the class fairly conversant in Verilog and to end the class more than competent in Verilog. This means that if you are lacking in Verilog skills you need to work extra hard at the beginning of the semester to catch up. It is expected that all students will successfully master the class and lab material.

Goals and Expectations

The goals and expectations for CECS460 are stated here. Each student will be expected to adhere to the stated guidelines in order to receive the desired grade.

All Students

1. Project due date is for full credit - Dropbox close date is final. No work will be accepted after the close date.
2. All project work will be submitted as follows:
   1. Complete report including description and source code submitted to instructor when demonstrated
   2. Demonstrate the project proper operation running on the Digilent board.
   3. Submit the report (as pdf) and the code (text files) to the dropbox.

Expected Class Grade of A/B

- In order to receive an A or a B **every** project will need to be completed in a timely manner
- The documentation will be completed in a professional manner according to the expectations presented in class.
- The final report submitted will be created according to the chip specification template presented in class.

Expected Class Grade of C

In order to receive a C a majority of the projects will need to be completed in a timely manner. For projects not completed a report must be submitted prior to the dropbox closing that explains the work accomplished and discusses the problems encountered.

- The documentation will be completed in a professional manner according to the expectations presented in class.
- The final report submitted will be created according to the chip specification template presented in class.

Comments

I acknowledge that this course material is not easy to master. If it was there would be a lot more students studying Computer Engineering and companies would be paying a lot less to successful graduates of Computer Engineering programs.

I do not take attendance in class but be forewarned that mastering the information in class is essential for doing well on the class projects and exams. I do lecture periodically in the lab. If for some reason you miss a class please do not contact me regarding what you have missed. You should have study partners in class and you can work with them for any material missed.

Please note that if for any reason you decide to drop this course that it is your responsibility to process the withdrawal. I will not take the initiative to drop students who stop attending class.

In the case of excused absence please contact the instructor immediately in order to make plans for your keeping up with the class during your absence. If you are unable to make an exam, it is your responsibility to contact either the instructor or the office prior to the exam.

Cover Sheet Format

Name
Class
Project Number and Title
Date Demonstrated

The cover sheet must be an 8.5x11” paper with no serrated edges. The cover sheet must be stapled to the project report and source code. The accompanying documentation to a project must be written in a professional manner with the intention of conveying to the reader: 1) What is the technical content of the project, 2) What is the applicability of the project, 3) Any issues encountered during the development, and 4) any suggestions for further investigation.

No grade will be issued until the files have been uploaded to the dropbox in BeachBoard.

Academic Honesty

Cheating on exams will have zero tolerance. Any student found cheating on the exam will be excused from class and will not be welcome to return this semester. In order to assist in ensuring academic honesty there will be no cell phones or other electronic devices during exams, no headphones, no hats or hoodies. Your desk should be cleared of everything except that needed to take the exam.

With respect to technical content of the projects there may be times when you incorporate other’s work product (not other students). When these circumstances arise please make sure that you give credit where credit is due. If used within reason this is an acceptable practice. Utilizing other people’s work product without acknowledging it as such is considered to be plagiarism and will be dealt with on a case by case basis.

I have added a header to the Admin folder on BeachBoard. Every file you create should have this header. The header should be updated as the development of the file progresses. Filling in the header is an acknowledgement that the work contained in the file is your own and nobody else’s.