Pre-lab [30 marks]

1. 64M = 64 * 2^{20} bytes
   Convert to hex: 1048576 = 64 * 16^5 = 0x0400 0000
   So the highest byte address of the SRDRAM chip is **0x04000 000**

2. Since the word size used in this lab is **16-bit, or 2-byte**. Thus, the addresses seen by the chip will only be multiples of 2-byte word type, or even multiples of types. For example, when requesting data from the lowest byte in the memory, the address seen by the chip should be 0x0000 0000, as shown below, then 0x0000 0002, 0x0000 0004

0x0000 0000	← First Word
0x0000 0001	
0x0000 0002	← Second Word
0x0000 0003	
……	……
0x03FF FFFE	
0x03FF FFFF	← Last Word
0x0400 0000	

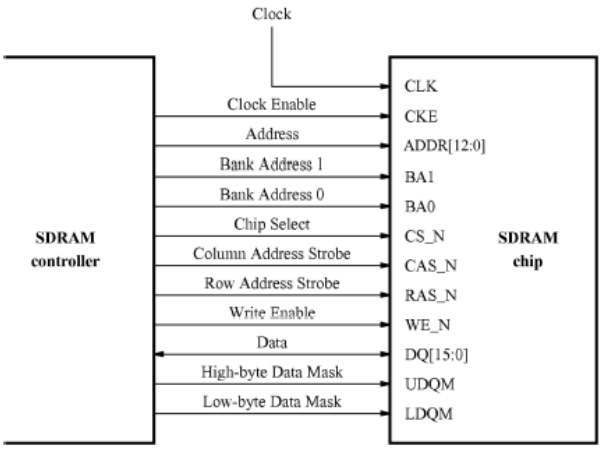
   and so on. When requesting data from the highest byte in the memory, the address seen by the chip should be the original address of the second last byte in the memory, which is **0x03ffffff**.

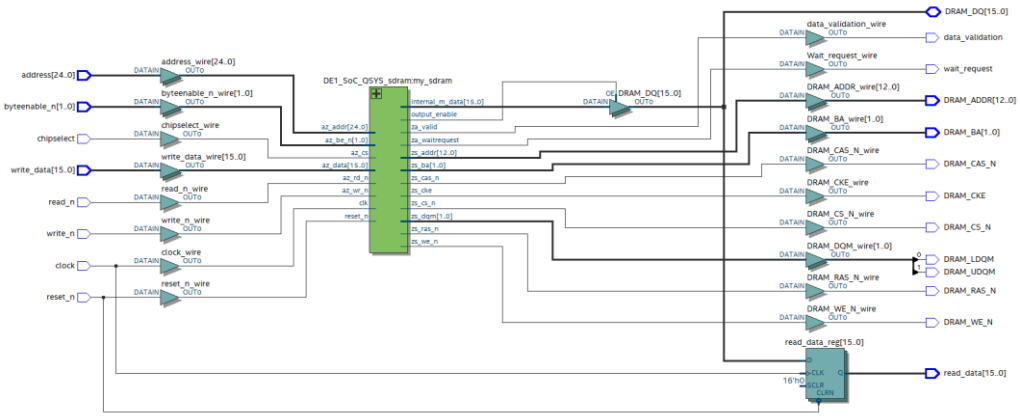
3. The address appearing on the SDRAM address line when the second byte is accessed will be the combined address of the first word, or the first and second byte, in the form of

   FIRST-WORD [15:0] ← SECOND-BYTE [7:0]:FIRST-BYTE [7:0]

   which makes the address **0x0000 0000,** pointing to the first word in the SDRAM.

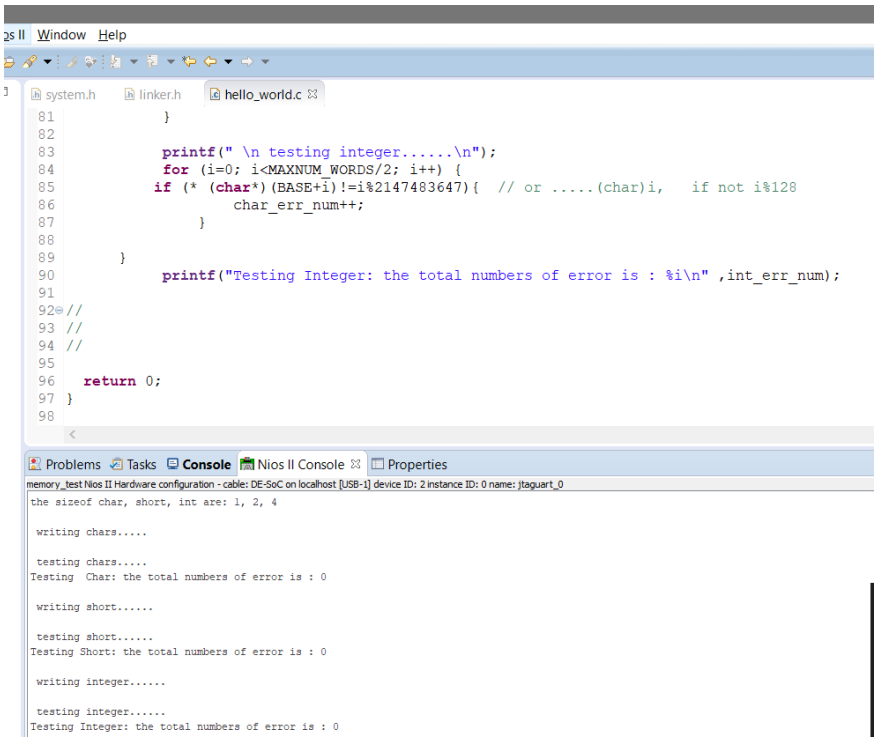
4. schematic of the circuit that is needed to implement SDRAM Controller.v.





Lab Report (Part 2)[15 marks]

1. the screenshots in the “Develop Software” part are provided below.

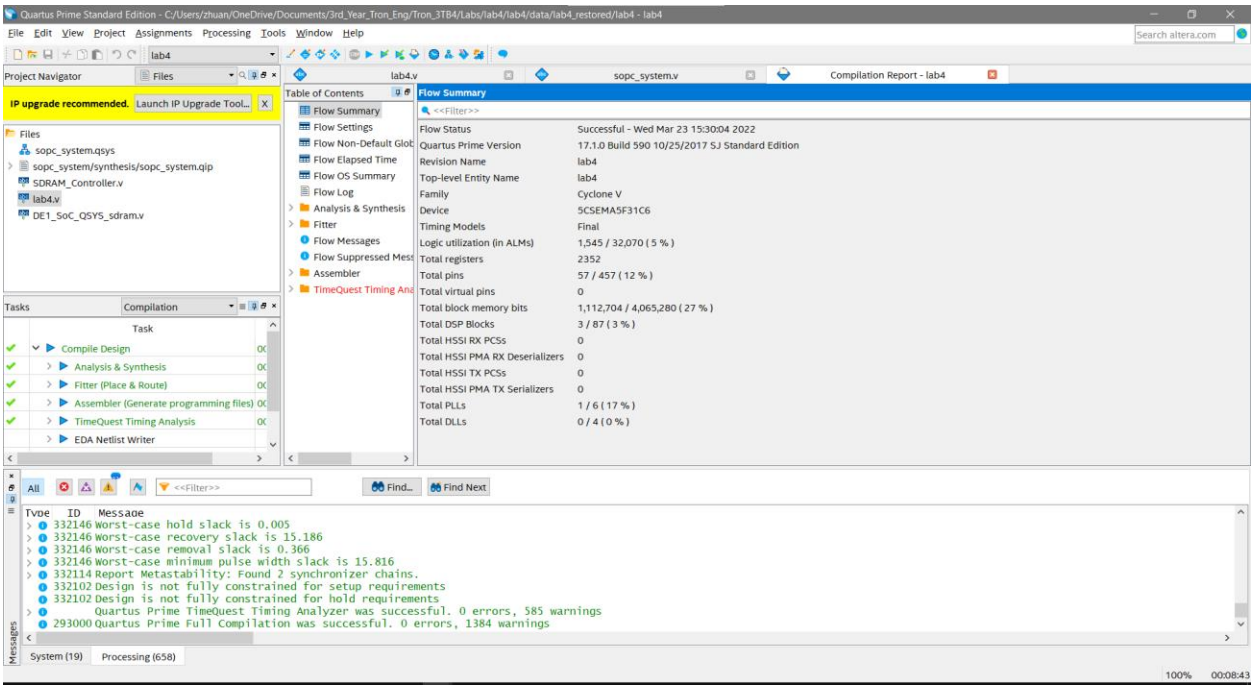


   (a) Writing into memory takes less clock cycles than reading because the writing process is conducted by the registers into main memory, where register operated with a larger bandwidth, while reading takes data from the main memory with a smaller bandwidth, which makes it slower.
   (b) Because it’s writing multiple values at the same time into the memory.
   (c) Because the data width for the SDRAM is 16-bit, whereas the C compiler uses data of 8-bit width, thus the Avalon interconnect takes two data location at the same time and combine it into one 16-bit location.
2. The steps the Avalon interconnect takes to write a 32-bit integer into the 16-bit SDRAM memory are:

   a. The compiler takes the 32 bit integer and splits it up into an upper and lower half word
   b. The compiler then writes each word separately
   c. Once it has been sent, the words are joined on the memory itself

3. On the compilation report,
   (a) Total number of logic elements used: 1847/32070(6%)
   (b) Total number of memory bits used: 1126376/4065280(28%)
   (c) Total number of pins used: 57/457(12%)
   (d) The maximum number of logic elements that can fit in the FGPA: 32070
4. Considering just the maximum number of logic elements on the FPGA, approximately 32070/1847 ≅ 17.36 ≅ 17 SOPC systems like this could fit on the FPGA.
5. Considering just the maximum amount of memory on the FPGA, approximately 4065280/1126376 ≅ 3.57 ≅ 3 SOPC systems like this could fit on the FPGA.
6. Considering just the maximum number of pins on the FPGA, approximately 457/57 ≅ 8..02 ≅ 8 SOPC systems like this could fit on the FPGA.

Compilation Result


Quartus Prime Standard Edition - C:/Users/zhuan/OneDrive/Documents/3rd_Year_Tron_Eng/Tron_3TB4/Labs/lab4/lab4/data/lab4_restored/lab4 - lab4
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Files
IP upgrade recommended.
Launch IP Upgrade Tool...
sopc_system.qsys
sopc_system/synthesis/sopc_system.qip
SDRAM_Controller.v
lab4.v
DE1_SoC_QSYS_sdram.v
Tasks
Compilation
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Table of Contents
Flow Summary
Flow Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Flow Messages
Assembler
Flow Summary
Flow Status Successful - Wed Mar 23 15:30:04 2022
Quartus Prime Version 17.1.0 Build 590 10/25/2017 SJ Standard Edition
Revision Name lab4
Top-level Entity Name lab4
Family Cyclone V
Device 5CSEMA5F31C6
Timing Models Final
Logic utilization (in ALMs) 1,545 / 32,070 (5 %)
Total registers 2352
Total pins 57 / 457 (12 %)
Total virtual pins 0
Total block memory bits 1,112,704 / 4,065,280 (27 %)
Total DSP Blocks 3 / 87 (3 %)
Total HSSI RX PCSs 0
Total HSSI PMA RX Deserializers 0
Total HSSI TX PCSs 0
Total HSSI PMA TX Serializers 0
Total PLLs 1 / 6 (17 %)
Total DLLs 0 / 4 (0 %)
Find... Find Next
Type ID Message
332146 Worst-case hold slack is 0.005
332146 Worst-case recovery slack is 15.186
332146 Worst-case removal slack is 0.366
332146 Worst-case minimum pulse width slack is 15.816
332114 Report Metastability: Found 2 synchronizer chains.
332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus Prime TimeQuest Timing Analyzer was successful. 0 errors, 585 warnings
293000 Quartus Prime Full Compilation was successful. 0 errors, 1384 warnings
System (19)
Processing (658)
100%
00:08:43