NANYANG TECHNOLOGICAL UNIVERSITY

CZ3001

LAB 3 (50 POINTS)

REPORT DUE: 27/10/2013,11:59PM

I. SIMPLE CONTROL & DATAPATH SPECIFICATION

In this assignment we will put together the ALU from the first assignment and the register file from the second assignment to make a simple Control/Datapath of a processor. Rather than directly feeding data inputs to the ALU or RF, we will now use an instruction and Control unit to perform a sequence of operations. As in the first two assignments, we will have 16-bit data, and a 16-bit instruction word.

The ADD, SUB, AND and OR instructions have a three address format.

opcode Rd, Rs, Rt (Execution is Rd ← Rs (OP) Rt). Rd is the destination register, and Rs and Rt are the source registers for operand 1 and 2, respectively. The bit-level format for the three-address format is:

opcode	Rd	Rs	Rt
15 12	11 8	7 4	3 0

The SLL, SRL, SRA, and RL instructions have a two address and one immediate format.

opcode Rd, Rs, imm (Execution is Rd ← Rs (OP) imm). Rd is the destination register, Rs is the source register and imm is used as the shift amount for ALU. The bit-level format for the two address plus immediate format is:

opcode	Rd	Rs	imm
15 12	11 8	7 4	3 0

A block diagram of the expected design is shown in Figure 1.

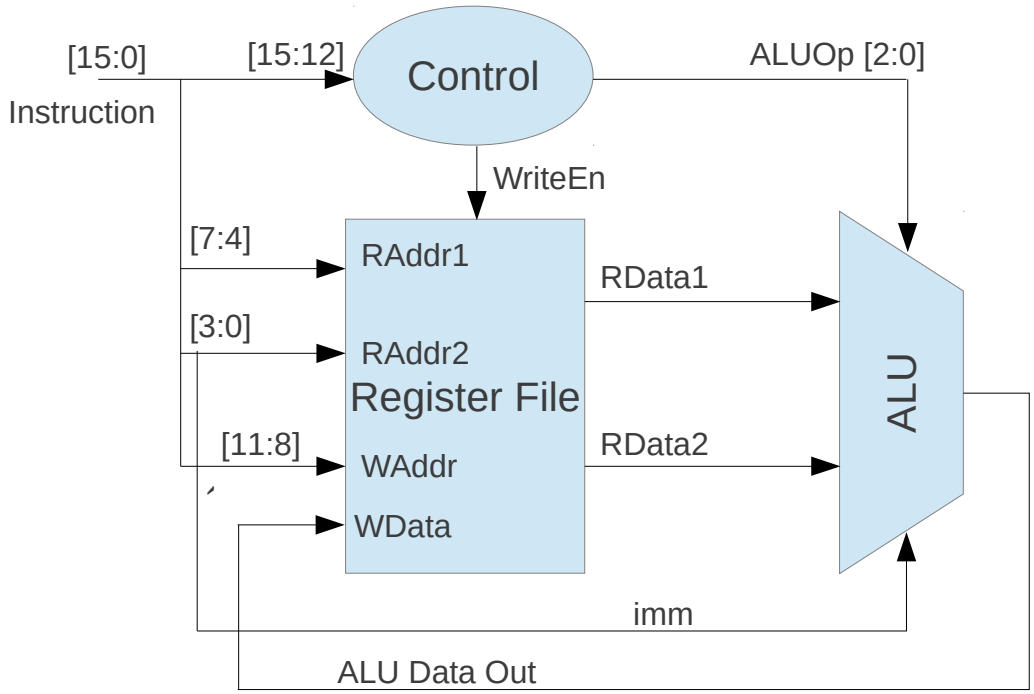

Figure 1 - Block Diagram of Single-Cycle Simple Control & Datapath

Table 1 - Port List Specification

Port Name	Port Direction	Size	Description
Instruction	Input	16-bit	Instruction word
DataInit	Input	16-bit	Initialization Data
InitSel	Input	1-bit	Select bit for Initialization data
ALUOut	Output	16-bit	Data Output from the ALU

II. IMPLEMENTATION AND TESTING

You should implement the simple Control and Datapath to put together your RF and ALU as shown above in Figure 1. Because we have not yet implemented memory operations, we will use an external data bus to initialize your register file, which you will need to remove later for your final project. Therefore use a multiplexor to select the source of the write data input, where '0' indicates initialization (the testbench can provide data to put into the RF), and '1' indicates testing (the write data is provided by the output of the ALU). The grading for this assignment will be as follows:

60% - A written report describing what you implemented, and showing annotated simulation waveforms that demonstrate that you have implemented and verified all of the operation types for the ALU and correct operation together with the register file. In addition the specified ports, your simulations may need to show additional (internal) signals in order to clearly demonstrate that you have verified operation.
40% - Verilog correctness; we will use a testbench (not provided) to verify the operation of your circuit according to the above specifications.