For the coding section of the lab, the overall experience wasn't entirely smooth because SystemVerilog is relatively limited in terms of online documentation. The SystemVerilog PDF provided on Blackboard was very helpful, but some concepts were either not explained clearly or not covered at all. That's when I started using GPT, for example, learning how to perform bitwise shifts, declare signed signals, and use shorthand to pad a series of bits with zeros. (I still had to cross-check some of its answers because a few were outdated.)

In addition to writing the code, I also noticed that negative integers appear as hexadecimal values in the waveform viewer, which initially made it tricky to validate my testbench results.

Here are some screenshots of the waveforms :), this was also a bit tricky to navigate. Figured out in the last few tasks that I can just drag the waveforms to see more details.