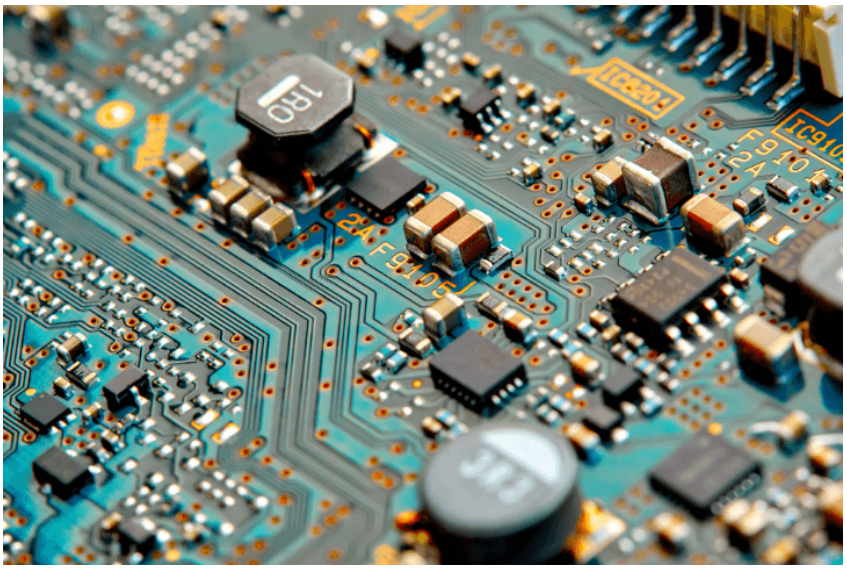
THE UNIVERSITY of EDINBURGH

Analogue Electronics (Project) 4
Simulation Project Report



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1 Exercise 1: Transistor parameter extraction

In this section of exercise, I'm going to simulate the transistors in Cadence Virtuoso, and extract some parameters from the simulation result using a simple transistor model. Finally, I'll analysis some questions based on the extracted parameters and the theoretical model. The first simulation is a plot of a group of I_d against V_{DS} under different value of V_{GS}, this is shown in Figure 1.

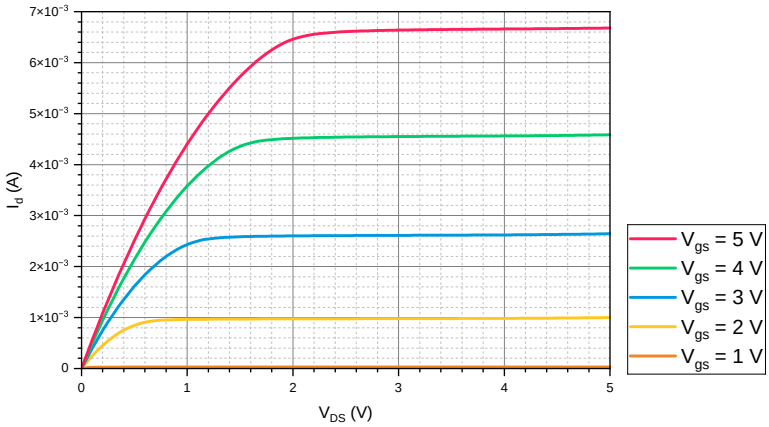


Figure 1: The plot of I_d against V_{DS} under 5 different V_{GS}

Considering the plot which $V_{GS} = 2\,\text{V}$, the curve in the saturation region could be expressed as equation (1). The parameter λ in the equation is used to model the channel-length modulation effect of the transistor.

$$I_{DS} = \beta \left(V_{GS} - V_T\right)^2 \left(1 + \lambda V_{DS}\right) \tag{1}$$

Substitute two groups of V_{DS} and I_{DS} and take the ratio of them:

$$\frac{I_{DS1}}{I_{DS2}} = \frac{9.781 \times 10^{-4}}{9.805 \times 10^{-4}} = \frac{1 + \lambda V_{DS1}}{1 + \lambda V_{DS2}} = \frac{1 + 3\lambda}{1 + 3.5\lambda} \tag{2}$$

Simplify this equation to get $\lambda = 4.981 \times 10^{-3}\ \text{V}^{-1}$. The output resistance of the transistor can be calculated using equation (3).

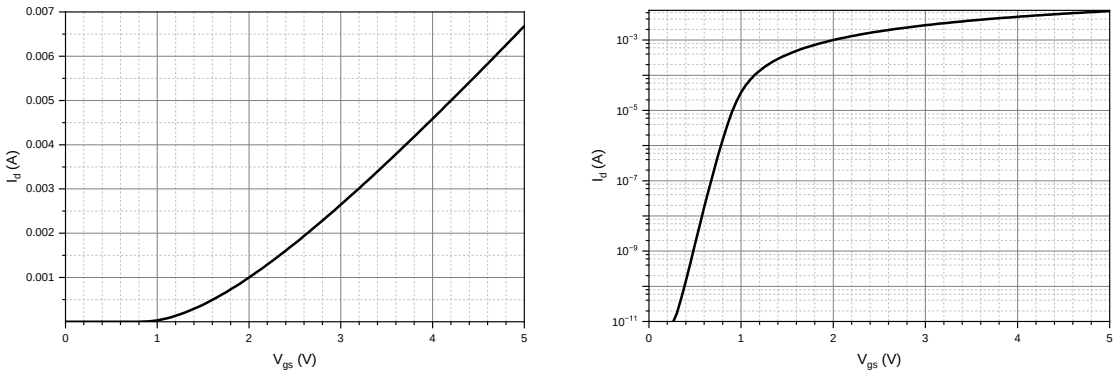
$$r_o = \frac{\delta V_{DS}}{\delta I_{DS}} \approx \frac{1 + \lambda V_{DS}}{\lambda I_{DS}} \tag{3}$$

If here we assume that $\lambda V_{DS} \ll 1$, the current I_{DS} is the average current in the range, then substitute the value into equation (3):

$$r_o \approx \frac{1}{4.981 \times 10^{-3} \times \frac{9.781+9.805}{2} \times 10^{-4}} = 205\,\text{k}\Omega \tag{4}$$

Taking $V_{DS} = 5\,\text{V}$, the transistor will be saturated for all V_{GS} between $0\,\text{V}$ and $5\,\text{V}$.

Figure 2(a) shows a plot of I_d against V_{GS} simulated under this V_{DS} voltage in linear scale and Figure 2(b) is a plot in log scale.



(a) (b)

Figure 2: Plot of I_D against V_{GS} in (a) linear scale and (b) log scale when $V_{DS} = 5\,\text{V}$

The sub-threshold slope is defined as:

$$S = \frac{\partial V_{GS}}{\partial\,(\log I_D)} \approx \frac{\Delta V_{GS}}{\Delta\,(\log I_D)} \tag{5}$$

To get the slope, I choose to substitute in the value of $\log(I_D)$ when $V_{GS} = 0.4\,\text{V}$ and $0.8\,\text{V}$:

$$S \approx \frac{0.8 - 0.4}{-5.835 - (-9.852)} = 99.6 \times 10^{-3}\ \text{V dec}^{-1} \tag{6}$$

When $V_{GS} = 0\,\text{V}$, there's a finite size of current, which is measured to be around 5.01 pA. This current is caused due to the internal structure of the MOSFET. When switched off, the diodes are formed between bulk and drain and bulk and source as shown in Figure 3. As source and bulk are connected together in this case, the diode between source and bulk is shorted, and only left with the diode between drain and bulk or equivalently drain and source. When there's voltage applied between drain and source, the diode will be reverse biased and there will be a small reverse saturation current. The measured 5.01 pA is probably caused by this.

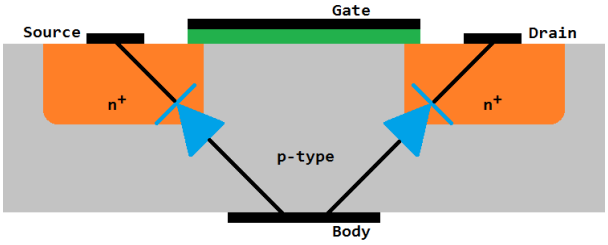
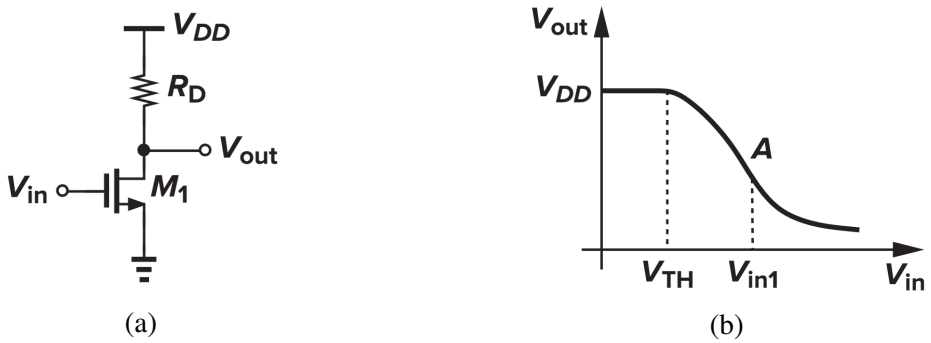


Figure 3: The diode formed between drain and bulk and source and bulk

2 Exercise 2: Common-Source Amplifier

The circuit shown in Figure 4(a) is called the inverting amplifier or common-source amplifier, Figure 4(b) shows it's large signal DC input output characteristic. In saturation region of this amplifier, the output voltage changes largely for even a small change in input voltage, and thus it could be used for amplifying signal.



(a) (b)

Figure 4: (a) The circuit of common-source amplifier (b) The large signal DC response of amplifier

The small signal gain of this amplifier is given as:

$$A_v = \frac{V_{out}}{V_{in}} = -g_m \left(R_D \parallel r_o\right) \tag{7}$$

In which R_D is the resistor connected between V_{DD} and drain of NMOS, and r_o is the output resistance calculated in equation (4). Taking $R_D = 100\,\text{k}\Omega$, the DC simulation shows the input operating point to be $V_{in,DC} = 0.983\,\text{V}$ and the amplitude to be 0.1 mV to make sure the maximum dynamic range and linearity. The transient simulation at 1 kHz is shown in Figure 5.

The gain of the amplifier is measured via the quotient of peak to peak of input and peak to peak of output. The peak to peak input is twice of amplitude, which is 0.2 mV. The output peak to peak value is measured to be 5.33 mV. This gives the overall transient gain:

$$A_v = \frac{V_{out,\text{ peak to peak}}}{V_{in,\text{ peak to peak}}} = \frac{5.33}{0.2} = -26.65 \tag{8}$$

As mentioned in equation (7), the gain is directly proportional to the parallel resistance of output resistance r_o and the resistance of the resistor R_D. If R_D keep increases, the parallel resistance will be smaller, and thus reduce the gain.

The frequency response of the amplifier could be measured using the AC simulation, a Bode diagram that measures the frequency response of the circuit between 1 Hz and 1 GHz is shown in Figure 6. The low frequency gain of this amplifier is measured to be −26.80, which matches the result calculated in transient analysis (equation (8)). The gain starts to drop at high frequency, the −3 dB bandwidth of the amplifier is measured to be around 65 MHz.

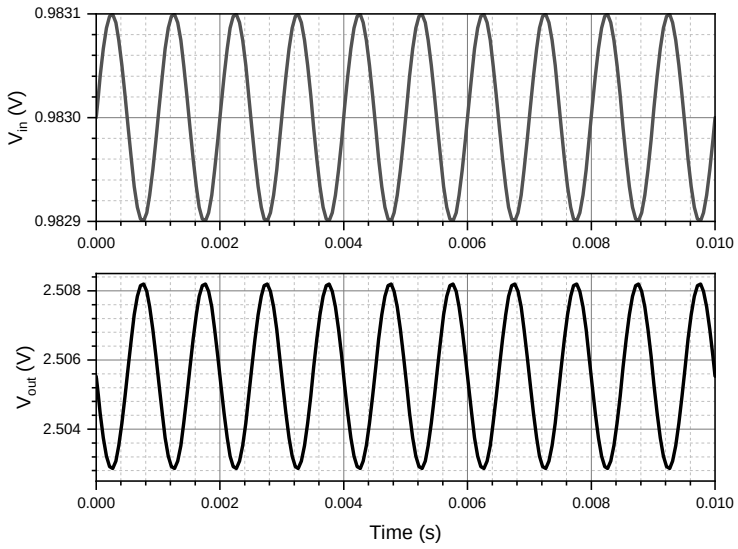


Figure 5: Transient simulation of amplifier with input signal at frequency of 1 kHz

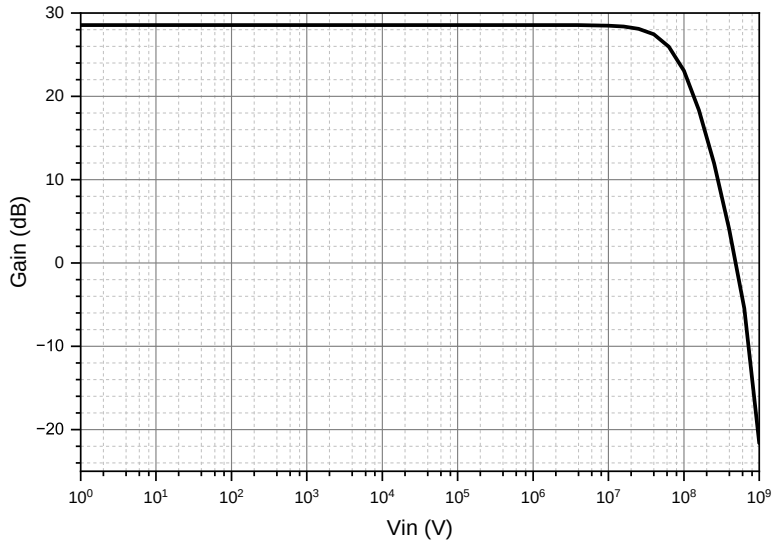


Figure 6: Transient simulation of amplifier with input signal at frequency of 1 kHz

Another transient simulation is taken to measure the gain of the amplifier at 100 MHz, which is outside the bandwidth of the amplifier, this gives the gain to be 19.05, which is different from the measured value 14.23 in AC simulation.

If the circuit is built in reality, the actual frequency response of the circuit would possibly be way worse than the measured result. This is because in reality, there's more capacitance between pins and wires while the model here only considers the parasitic capacitance in the MOSFET.

3 Exercise 3: Current Mirror

The circuit of the current mirror is shown in Figure 7, ideally the current flowing through the two MOSFET should be exactly the same as their gate voltage is the same and in saturation region the voltage is almost constant. In the simulation, the drain terminal of MOSFET M_2 is connected to V_{DD} and I_{REF} is set to 100 µA. The measured output current is 109.64 µA which shows a slight offset.

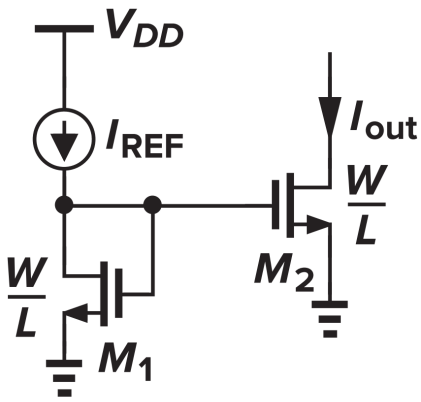
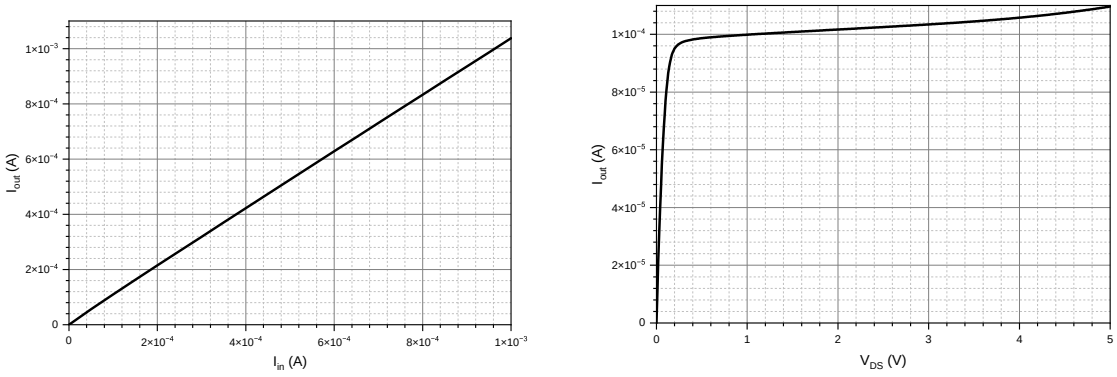


Figure 7: Basic current mirror circuit

Figure 8(a) shows the plot of I_{out} against I_{in} when the MOSFET M_2 has it's drain connected to V_{DD}, and Figure 8(b) shows the plot of I_{out} against V_{DS} under a constant value of $I_{in} = 100$ µA.



(a) (b)

Figure 8: Plot of (a) output current against input current and (b) output current against V_{DS}