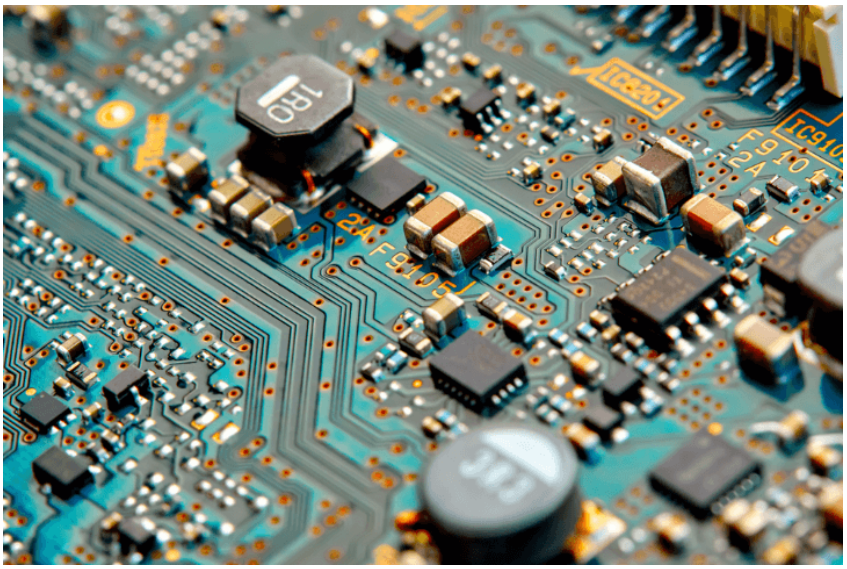
THE UNIVERSITY of EDINBURGH

Analogue Electronics (Project) 4
Simulation Project Report



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October 25, 2025

1 Exercise 1: Transistor parameter extraction

In this section of exercise, I'm going to simulate the transistors in Cadence Virtuoso, and extract some parameters from the simulation result using a simple transistor model. Finally, I'll analysis some questions based on the extracted parameters and the theoretical model. The first simulation is a plot of a group of I_d against V_{DS} under different value of V_{GS}, this is shown in Figure 1.

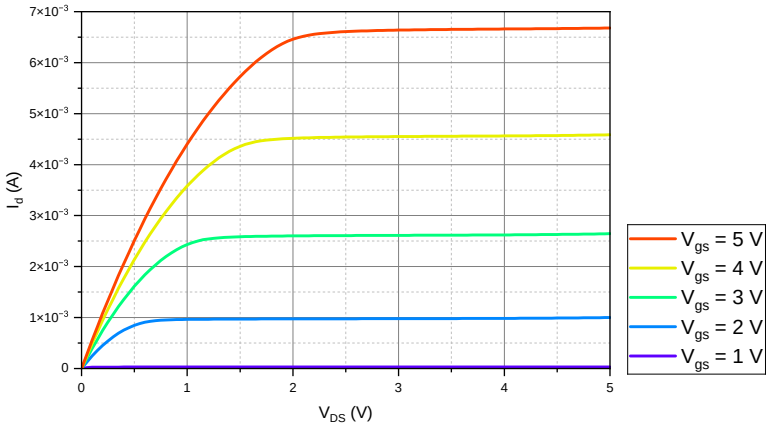


Figure 1: The plot of I_d against V_{DS} under 5 different V_{GS}

Considering the plot which $V_{GS} = 2\,\text{V}$, the curve in the saturation region could be expressed as equation (1). The parameter λ in the equation is used to model the channel-length modulation effect of the transistor.

$$I_{DS} = \beta \left(V_{GS} - V_T\right)^2 \left(1 + \lambda V_{DS}\right) \tag{1}$$

Substitute two groups of V_{DS} and I_{DS} and take the ratio of them:

$$\frac{I_{DS1}}{I_{DS2}} = \frac{9.781 \times 10^{-4}}{9.805 \times 10^{-4}} = \frac{1 + \lambda V_{DS1}}{1 + \lambda V_{DS2}} = \frac{1 + 3\lambda}{1 + 3.5\lambda} \tag{2}$$

Simplify this equation to get $\lambda = 4.981 \times 10^{-3}\ \text{V}^{-1}$. The output resistance of the transistor can be calculated using equation (3).

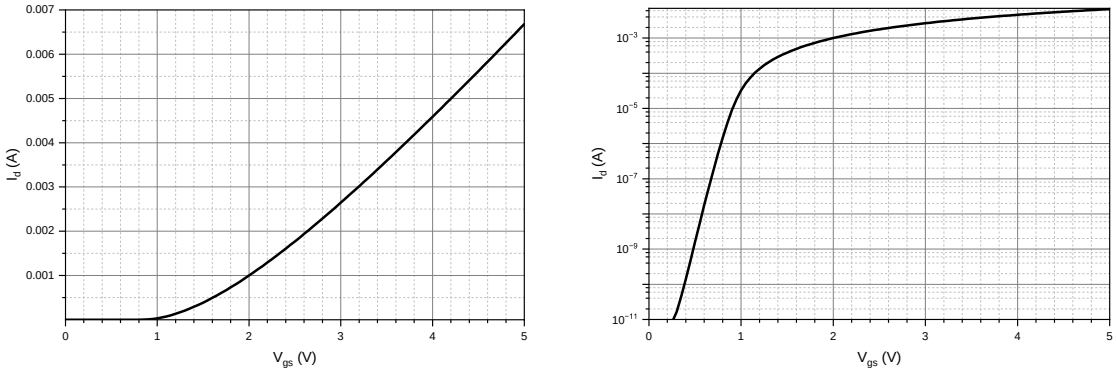
$$r_o = \frac{\delta V_{DS}}{\delta I_{DS}} \approx \frac{1 + \lambda V_{DS}}{\lambda I_{DS}} \tag{3}$$

If here we assume that $\lambda V_{DS} \ll 1$, the current I_{DS} is the average current in the range, then substitute the value into equation (3):

$$r_o \approx \frac{1}{4.981 \times 10^{-3} \times \frac{9.781+9.805}{2} \times 10^{-4}} = 205\,\text{k}\Omega \tag{4}$$

Taking $V_{DS} = 5\,\text{V}$, the transistor will be saturated for all V_{GS} between $0\,\text{V}$ and $5\,\text{V}$.

Figure 2(a) shows a plot of I_d against V_{GS} simulated under this V_{DS} voltage in linear scale and Figure 2(b) is a plot in log scale.



(a) (b)

Figure 2: Plot of I_D against V_{GS} in (a) linear scale and (b) log scale when $V_{DS} = 5\,\text{V}$

The sub-threshold slope is defined as:

$$S = \frac{\partial V_{GS}}{\partial\,(\log I_D)} \approx \frac{\Delta V_{GS}}{\Delta\,(\log I_D)} \tag{5}$$

To get the slope, I choose to substitute in the value of $\log(I_D)$ when $V_{GS} = 0.4\,\text{V}$ and $0.8\,\text{V}$:

$$S \approx \frac{0.8 - 0.4}{-5.835 - (-9.852)} = 99.6 \times 10^{-3}\ \text{V dec}^{-1} \tag{6}$$

2 Exercise 2: Common-Source Amplifier