Project Proposal

#45 Ultra-Fast Failure Test Unit

Capstone Project

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List of Abbreviations

ADC	Analog to Digital Converter
ADI	Analog Devices Incorporated
DUT	Device Under Test
DMA	Direct Memory Access
FFT	Fast Fourier Transform
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
GSPS	Giga Samples Per Second
HPC	High Pin Count
LPC	Low Pin Count
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signalling
RF	Radio Frequency
SoC	System on Chip

Background

The Ivanov Group at the University of British Columbia's System-on-Chip lab studies integrated circuit reliability as chips degrade and fail with age. Transistor aging is the process in which transistors develop flaws overtime, degrading their performance and reliability, and eventually failing altogether. The Ivanov group induces aging in transistors by placing CMOS inverters in a test environment with various stresses, such as increased temperature, magnetic field strength and supply voltage. During these tests, the output voltage is monitored to better understand characteristics of aging. More specifically, this output voltage is measured across the drain of the PMOS to the drain of the NMOS. In an ideal transistor, voltage transitions between levels are instantaneous, as observed in Figure 1 (a). In reality there is a small rise time delay and fall time delay which takes place, as observed in Figure 1 (b). With age, these delays increase. While small delays are acceptable, large delays can violate timing constraints of any logic design. Even in an aged transistor these delays are so small that ultra-fast sampling rates are necessary in order to detect them in the time-domain. A solution to this problem is reducing the sampling rates slightly and performing a Fast Fourier Transform (FFT) post testing. The current method of gathering measurements on transistor output voltage includes expensive equipment shared between multiple lab groups. This greatly restricts the number of tests that can be run by the Ivanov group. Our team is working on developing a testing unit which measures output transistor voltage in the test environment at a rate fast enough so that timing delays between transitions can be observed in the frequency domain by way of an FFT. Developing a budget-friendly alternative allows the Ivanov group to replicate our proposed solution multiple times in order to run multiple tests in parallel.

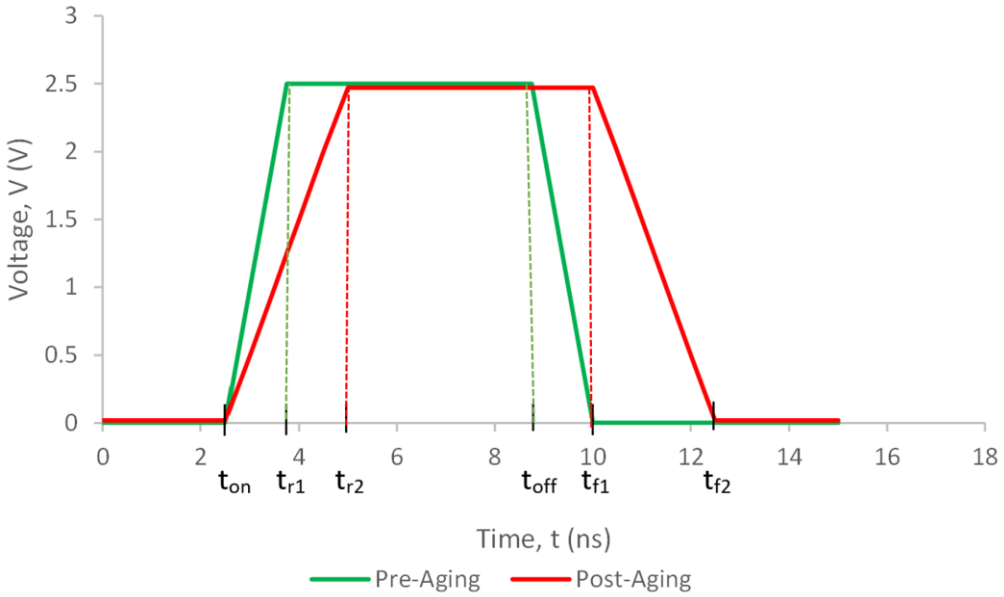

Figure 1: (Red) Transistor output voltage waveform post-aging, (Gree) Transistor output voltage waveform pre-aging

Objectives/Goals

For this project, we have the following primary goals:

1. Gather data at an adequately fast sampling rate to ensure that voltage transition delays are observable in the frequency domain.

2. Design a system which is affordable and scalable, so that our client can replicate it for future parallel testing.

The process begins as a user configures parameters for a test to be performed on the device under test. The parameters are then sent to a board which generates the desired test environment. These steps are represented by the two blue boxes in the diagram below. The Existing Board is a device which has previously been created by members of the Ivanov Group and is configured to generate the test environment. The Device Under Test is the transistor whose aging we would like to monitor. The scope of this project is to develop the two modules represented as purple boxes below. The output voltage coming from the Device Under Test is an analog signal. This signal gets passed through an Analog to Digital Converter, then to an FPGA or development board, where it is placed into memory. Once the testing has completed, the data in memory is placed into a form of storage and passed to a Personal Computer where any necessary post-processing can be completed by the user.

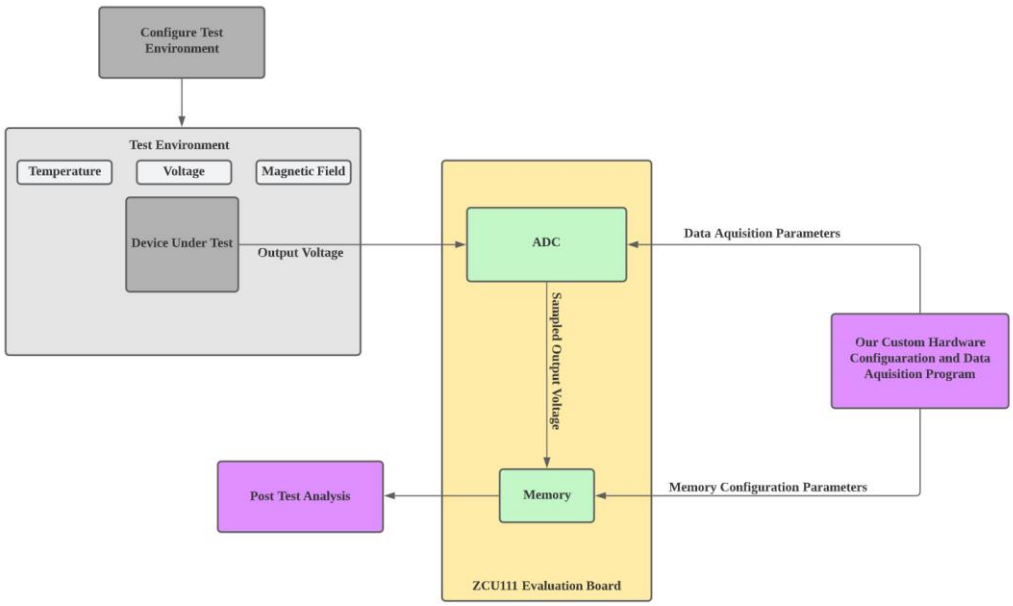

Figure 2: High Level System Architecture Diagram

There are certain trade-offs associated with achieving our goals through the system described above. First, as we increase our target sampling rate, we must also consider more expensive hardware. Increasing sampling rate especially increases the cost of an ADC. As we sample

more data quickly, the amount of memory required to store that data also increases, and consequently so does the cost of an FPGA or development board which can support the amount of incoming data. In order to both achieve our system goals, and remain within our allotted budget, we have done extensive research as a team to ensure we find a middle ground between affordability and functionality.

Preliminary System Design

Our weekly meetings with our client played an essential role in determining which specifications to filter for when doing research on some system components. A detailed explanation for exactly how important specifications were determined and quantified is available in our Requirements, Constraints and Goals document section 2. Below we have outlined some of the components which met the standards we had set out to find. At the end of this document, we outline which of the following components we have chosen for the implementation of our system design, as well as a justification for our choices.

Component	Key Specifications	Datasheet	Cost
DE10-Standard	**Cyclone V** SX SoC **ARM Cortex-A9 MP Duo Core** **DDR3** 1GB 16-bit **DMA**	SoC Platform - Cyclone - DE10-Standard	$490CAD
Eclypse Z7 (410-393)	**Xilinx XC7Z020** 1CLG484C **Cortex-A9 Duo Core processor** **DDR3L** 1 GiB 32-bit **DMA**	Eclypse Z7	$632CAD
AXU3EG	**Xilinx XCZU3EG** 1SFVC784I **ARM Cortex-A53 x4** **DDR4 4 GB** 64-bit **DMA**	http://www.alinx.vip:81/ug_en/AXU3EG_User_Manual.pdf	$734CAD
MYD-CZU3EG-4E4D-1200-C	**Xilinx XCZU3EG** 1SFVC784E **Quad ARM Cortex-A53** **Dual-Core ARM Cortex-R5** **DDR4 4 GB** 64-bit **DMA** FMC LPC Port	MYD-CZU3EG/4EV/5EV Development Board	$759CAD
AXKU040	**Xilinx XCKU040-2FFVA1156I** **4x 1GB DDR4** 64-bit **DMA** FMC HPC Port	http://www.alinx.vip:81/ug_en/AX7325_User_Manual.pdf	$849CAD

Table 1: FPGA Comparison Table

Component	Key Specifications	Datasheet	Cost*
AD9094-1000EBZ	**8-bit ADC** input **Four channels** **1 GSPS** 1.6W power (400mW per channel) **JESD204B interface**	8-Bit, 1 GSPS, JESD204B, Quad ADC AD9094 AD9094 Datasheet and Product Info	$500CAD
AD9680-LF5000EBZ	**12-bit ADC** input **Two channels** **1 GSPS** 1.5W power per channel **JESD204B interface**	AD9234 (Rev. B)	$729CAD
TSW1405EVM	**16-bit ADC input** **8 channels** **1 GSPS** Includes Lattice ECP3 FPGA Parallel **LVDS** interface	TSW1405EVM Evaluation board | TI.com	$125CAD
* Note cost of ADC includes cost of an evaluation board, not IC.			

Table 2: ADC Comparison Table

An important consideration when conducting research on viable components to incorporate into our design was the compatibility, or communication protocol required for interconnections. The following section evaluates the differences between the Series LVDS and JESD204B communication protocols in the context of our project.

Comparison Between Communication Protocols

Communication Protocol	Advantages	Disadvantages
JESD204B	- Can support up to a 12.5Gbps data transfer rate - Low pin count means smaller overall packages thus reduced cost - Deterministic latency - Allows frame clock (ADC sampling clock) to be the same as the device clock - Lower power consumption (with reference to other communication protocols)	- Requires an FMC connector in order to work with an FPGA
LVDS	- Differential voltage signal reduces effect of noise on system	- Recommended maximum data transfer rate is 655Mbps - Theoretical maximum data transfer rate is 1.923Gsps

Table 3: Comparison Between Serial LVDS and JESD204

As discussed in Section 2 of our Requirements, Constraints and Goals document, we wish to sample data at a rate of 1 GSPS, which means we need a communication protocol capable of transferring 8Gbps. This means finding an ADC which uses the JESD204B is more suitable for our project.

Considering that we are dealing with ultra-fast sampling rates, we wish to have a deterministic latency to ensure accurate measurements and accurate consideration of timing constraints. Note that latency of an ADC is defined as the number of clock cycles between the instant of sampling edge of the input signal until the digital signal is available at the output.

A challenge of digital design is clock domain synchronisation, therefore by ensuring that we can use the device clock to run the ADC, we eliminate the need for overcoming this challenge.

The main disadvantage of connecting an ADC and FPGA together via an JESD204B protocol is the need for an FMC connector. Many FPGAs with a built-in FMC connector are higher in cost and purchasing a separate FMC connector also introduces additional costs.

Given the analysis above, we decided that the JESD204B is the best option for our project.

Primary Design Choice

After research and analysis, we created a list of the most important desired specifications for each component.

ADC

- 1 GPSP
- JESD204B communication protocol

FPGA

- 1GB memory size
- HPC FMC port

We chose the Analog Devices AD9094-1000EBZ ADC and the Alinx AXKU040 FPGA board because they meet all the necessary specifications outlined above.

Secondary Design Choice

The Ivanov Group initially had plans to designate a team to work on developing a similar project to ours, using a Xilinx Evaluation kit with an RFSoC which was donated to them for research purposes. The board has very strong capabilities, and exceeds the requirements established for our project. This project was set to be completed in parallel with ours but was never initiated. As such, the Xilinx ZCU111 is currently unused, and available to our team as a design alternative. Though the hardware is expensive, it is still a large margin below the shared lab oscilloscope in cost and would be a viable option to conduct transistor aging research. The main advantage of this board is that it includes both an ADC with a very fast sampling rate, and an FPGA with enough memory and processing power. The detailed specifications of the board are included in Figure 3.

Using this design alternative, would result in some changes in our design requirements as well as the scope of our project. Firstly, we will be able to provide a much higher sampling rate, 4 GSPS. Secondly, we will be able to have a larger ADC input bit-width, consequently allowing for a lower voltage resolution. Finally, we will introduce the FFT analysis process into the scope of our project.

Our team has decided that we will work on this board in parallel to implementing the connection of an ADC and FPGA board. To ensure this endeavour is managed effectively, we have designated each team member to work on two separate tasks, one specific to our primary design choice, and another specific to our secondary design choice.

Component	Key Specifications	Datasheet	Cost
Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit	Includes ADC and FPGA 8 ADC channels 12-bit ADC input 4 GSPS 4GB DDR4 memory DMA	ZCU111 Evaluation Board User Guide (UG1271)	$16,309CAD

Table 5: FPGA Board provided by the Client

Project Outcome

The Ivanov Group at the UBC SoC Lab currently relies on ultra-high speed test equipment to collect the data they require. Of the limited supply of capable oscilloscopes at UBC, only one is available to the Ivanov Group. By successfully designing a highly specialized device to do exactly what our client needs, our team aims to significantly reduce operating costs for the UBC SoC Lab and provide them with a design which can be duplicated to allow parallel testing environments.

By implementing multiple parallelized data acquisition benches at a small fraction of the cost, the Ivanov group will be able to accelerate their research on device aging to better support their primary sponsor, Huawei.

Project Implications

Our project audience is targeted specifically at the Ivanov Group. If completed successfully, our product will have an impact on the Ivanov Group's ability to conduct testing on the aging of transistors. As outlined in previous sections, the group is limited in their research due to expensive testing equipment which is shared amongst many lab groups. Due to these limitations, research on the aging of transistors moves forward at a relatively slow pace. We hope that we can facilitate more frequent testing by providing a budget-friendly testing alternative which can be easily replicated.

Scope Risks

COVID-19 is an important risk that needs to be considered while running this project. Even though it has been almost two years since it first started, it has not ended yet. Due to strict restrictions on campus, such as keeping the number of people in a room limited, keeping a distance from people around you, and wearing a mask while working indoors, teamwork and collaboration are harder. In case of any unexpected increase in daily cases, there is always a possibility that entire facilities can be shut down. Such a situation may cause severe delays to our deliverables because we rely heavily on lab equipment such as a signal generator and oscilloscope.

Finding the desired hardware is another challenge for such a project with a limited budget and high-performance requirements. In addition, there is always a possibility that any purchased hardware may not be compatible with each other. That is why it is important to have a backup plan. Having a backup plan can minimize delays if any kind of incompatibility situation is encountered.

Budget Analysis

Below is a budget analysis of both of the two design options outlined in this proposal.

Primary Design Choice – Separate FPGA and ADC Development Boards

Category	Cost (CAD)
Budget provided by UBC ECE	+$650.00
Budget provided by Ivanov Group	+$1000.00
FPGA (includes shipping)	-$1218.00
ADC (includes shipping)	-$675.00
Total Cost	$1893
Remaining Budget	-$243.00

Table 6: Cost Estimation for Primary Design Choice

This is the lowest price we could get that satisfies our requirements. Memory space is one of the most expensive elements in a development board. Since we will be sampling a high data rate, we will need a temporary location to store it. We obtain 1GB of data per second which means we will need a memory space of slightly more than 1GB to allow a margin for error. Another key element on our FPGA board is the I/O Pins. We planned to connect our ADC and the FPGA development board through the FMC port. Most low-budget boards do not have an FMC port, this introduces two new challenges: purchasing a high-cost FMC adapter and configuring internal connection pins.

After researching various FPGAs, we found that we could lower our overall costs by finding an FPGA with an existing FMC port. We have decided to pick the AXKU040 FPGA board which is manufactured by Alinx. Alinx provides many modules and tutorials that will be very useful throughout the project. Although we encountered some FPGA development boards that satisfied our requirements at lower costs, we focused on finding a board from reliable manufacturers such as Terasic, Xilinx, and Alinx.

Generally, as ADC sampling rates increase, so do their costs. We have picked the AD9094 ADC board which has an 8-bit channel with 1 GSPS. This ADC meets our necessary specification requirements while still being within our budget.

Option 2 – Xilinx ZCU111 Evaluation Board

Category	Cost (CAD)
Budget provided by UBC ECE	+$650.00
Budget provided by Ivanov Group	+$1000.00
FPGA	-$0.0
ADC	-$0.0
Adapters	-$0.0
Total Cost	$0.0
Remaining Budget	$1650.00

Table 6: Cost Estimation for Option 2

For this option, the FPGA development board and the ADC board will be provided by the client. It is a $16,321 board that includes its own ADC board and has a faster sampling rate than any ADC we could consider within our budget. This option eliminates the need to spend any money and to integrate two different components. We have decided to work on both of these designs simultaneously. Both designs will follow a similar functional digital system. Since our team's main goal is to come up with an affordable and replicable design, our main focus will be the ALINX development board.

Evaluation of Design Options Based on Budget

Although option 1 exceeds our current budget by 14.7%, our team is confident that the cost is justified. By purchasing the cheapest possible ADC and FPGA boards available from reliable vendors which meet our requirements, we will be able to design an easily scalable solution which will allow our client to parallelize their test benches and increase their productivity.

An additional consideration is that the listed prices in the budget analysis of option 1 do not account for the possibility of receiving discounts and/or donated evaluation boards for research purposes. Our team will be reaching out to Analog Devices to see if there is anything they are able to do to help us stay within our budget.

It is for these reasons that we are proposing to move forward with option 1 upon confirmation from the Ivanov Group that the increase in budget is able to be accommodated, or a discount from ADI allows us to stay within the current budget.