Requirement Document

Ultra-Fast Failure Test Unit

Capstone Project #45

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1 Background

The Ivanov Group at the University of British Columbia's System-on-Chip lab studies integrated circuit reliability as chips degrade and fail with age. Transistor aging is the process in which transistors develop flaws overtime, degrading their performance and reliability, and eventually failing altogether. The Ivanov group induces aging in transistors by placing CMOS inverters in a test environment with various stresses, such as increased temperature, magnetic field strength and supply voltage. During these tests, the output voltage is monitored to better understand characteristics of aging.

In an ideal transistor, voltage transitions between levels are instantaneous. In reality there is a small rise time delay and fall time delay which takes place, as observed in Figure 1. With age, these delays increase. While small delays are acceptable, large delays can violate timing constraints of any logic design. Even in an aged transistor these delays are so small that ultra-fast signal sampling rates are necessary in order to detect them in the time-domain.

2 Project Outcome

Currently the Ivanov group conducts their research by using the Teledyne HDO4104A oscilloscope, which costs $45,000 CAD. Not only is this equipment very expensive, but it is also shared between multiple lab groups. This greatly restricts the number of tests that can be run by the Ivanov group. Our project is developing a testing unit which replaces the current testing method with an affordable solution. The successful completion of our project will allow the Ivanov group to replicate our design in order to increase the number of simultaneous tests which can be conducted.

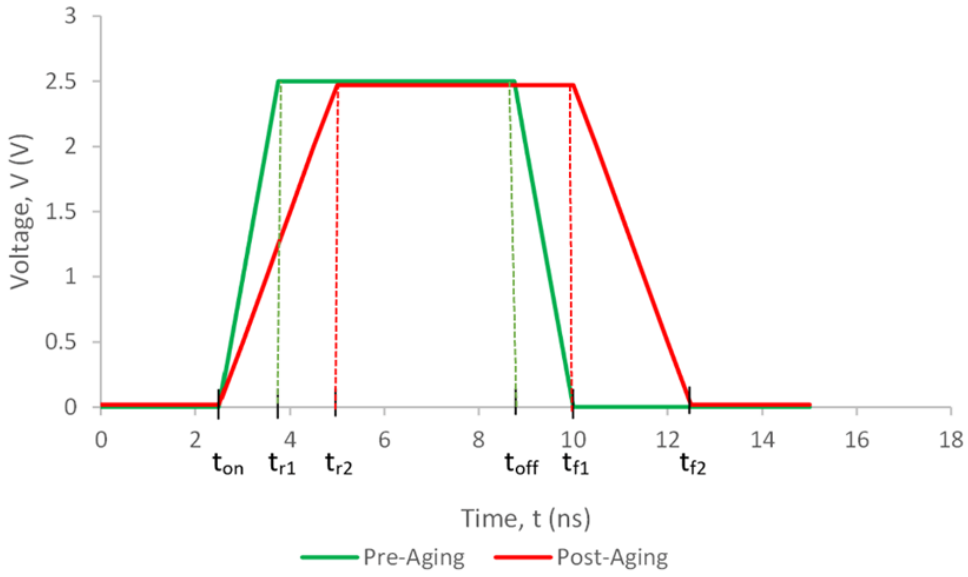


Figure 1: Transistor output voltage waveform pre-aging and post-aging

3 Goals

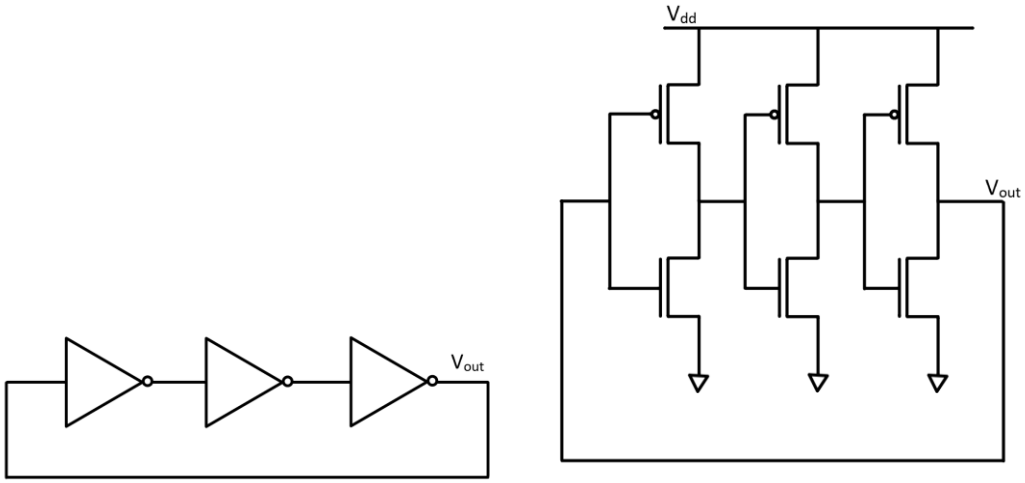
3.1 General Goals

Goal 1: Create a solution which is more affordable than the current standard for data measurement.

The Xilinx Zynq Ultrascale+ RFSoC ZCU111 evaluation board [3] which we are using to develop our solution can be purchased for $10,794.00 USD [4]. This is a 76% reduction in cost relative to the current oscilloscope being used for testing. We hope that this reduction of cost will allow the client to replicate our project affordably in order to run tests more frequently and run many tests in parallel.

Goal 2: Measure output voltage of DUT

The output voltage is measured across the drain of the PMOS to the drain of the NMOS (see Figure 2).



(a) Symbol Schematic (b) Transistor-level Schematic

Figure 2: Schematics representing a ring oscillator, similar to the DUT

Goal 3: Convert the analog signal measured to a digital signal.

The output voltage we measure from the DUT is an analog signal. We wish to convert this analog signal to a digital signal so that we can store and process the information using the ZCU111 FPGA board. The board operates in the digital domain, and therefore our signal must first be run through an ADC.

Goal 4: Export measured data from the ZCU111 board to User's Computer

In order to allow post-processing and analysis of the signal measured, data must be presented to the client in some format. The most efficient way to achieve this is to transfer the data to the user's computer where it can be viewed and analyzed.

Goal 5: Plot data in both the time-domain and frequency domain (FFT) using a Python script

To confirm that we have successfully measured the output voltage signal, the data should be plotted in both the time-domain and frequency domain (by providing a FFT). This will be completed using a Python script which can be easily run by the client without any additional configurations.

3.2 Stretch Goals

Stretch Goal 1: Provide an easily accessible solution

Our project should be accessible from any computer running on a Windows OS. It should be implemented and run without the need for downloading any specific development tools or software. Our client has expressed that they wish to plug in the board, open a terminal, initiate our custom program and configure the necessary parameters to run the project without additional intermediary steps.

4 Requirements

4.1 Functional Requirements

For the purpose of this project, a functional requirement is a function or capability our system serves. Without the successful completion of these functionalities, our system will not achieve the overall goals.

Functional Requirement 1: Our system design must connect to the DUT

The DUT is a PCB designed by the members of the Ivanov Group. We will probe the output voltage node on the PCB, and connect it to our ADC channel using an SMA cable. This cable is standard for sending RF signals, and both the ADC and the ZCU111 are compatible with this form of transmission.

Functional Requirement 2: Our system must measure analog voltage signal from the DUT

The output voltage we measure is a 2.5V LVCMOS signal. This means we want to measure continuous changes of the voltage between 0V and 2.5V. The number of bits we are able to measure in a single sample impacts the accuracy of sampling. The ADC we will be using has eight 12-bit channels, each capable of sampling up to a rate of 4 GSPS. Please see Constraint 3 and 4 for the implications of resolution on our project.

Functional Requirement 3: Our system must convert the analog voltage signal to a digital signal

The ZCU111 Evaluation board stores and processes data digitally. To ensure the data we gather is compatible with our hardware, we must first pass the signal measured through an ADC.

Functional Requirement 4: Our system must prevent any aliasing that may occur during sampling

We want to ensure that the analog signal we measure can be accurately reconstructed after data is converted in the digital domain. Please refer to section 6.1 in the Design Key Document for a description of aliasing, as well as design choices we make to avoid the phenomenon.

Functional Requirement 5: Our system must temporarily store the data in memory

Incoming data will be placed in memory over the sampling time. This ensures that no sampled data is lost during testing. Please see Non-Functional Requirement 3 for an in depth numerical representation.

Functional Requirement 6: Our system must store data in .csv format in order to be processed in Python

In order to successfully complete Goal 5 we must export the data in a format which is compatible with the Python programming language. We will be using .csv file types to store the data.

4.2 Non-Functional Requirements

For the purpose of this project, a non-functional requirement is the quality attributes which our system must exhibit. We have defined these qualities by giving them quantitative values by which they can be assessed.

Non-Functional Requirement 1: Sampling rate of 1 GSPS

Sampling refers to the process of extracting the instantaneous value at the corresponding moment of continuous analog signal $x(t)$ at a certain time interval T. The sampling period determines the quality and amount of the sampled signal.

The sampling theorem specifies the minimum-sampling rate at which a continuous-time signal needs to be uniformly sampled so that the original signal can be completely recovered or reconstructed by these samples alone [2].

If a continuous time signal contains no frequency components higher than W Hz, then it can be completely determined by uniform samples taken at a rate f_s samples per second where $f_s \geq 2W$ or, in terms of the sampling period $T \leq 1/2W$.

The minimum sampling rate allowed by the sampling theorem ($f_s = 2W$) is called the Nyquist rate. In this project, the signal to be sampled is equivalent to a 250 MHz square wave. The minimum sampling frequency is $f_s = 2 \cdot 250 = 500\ \mathrm{MHz}$.

In order to ensure the quality of the signal, we decided to use a sampling rate of 1 GSPS.

Non-Functional Requirement 2: Sample data for a duration of 1ms

In order to accurately observe a trend in voltage transition delays we need to observe a signal over several periods. The period of our signal is $T = 4ns$. If we sample data for 1ms we are able to observe 250 thousand periods of oscillation:

$$Number\ of\ Periods = \frac{Sampling\ Time}{Period} = \frac{1\ ms}{4\ ns} = 250{,}000\ periods$$

Upon confirmation with our client, we have concluded that this is a sufficient amount of data to gather.

Non-Functional Requirement 3: Fill 15.4 MB of memory with data

Our ADC sampling rate has an impact on our necessary memory size. If we sample at 1 GSPS, we receive 12 Gb of data per second of sampling. Given that our sample time is 1ms we do the following calculations:

$$\frac{data}{millisecond} = \frac{1 \times 2^{30} samples}{second} \times \frac{1\ second}{100\ milliseconds} \times \frac{12\ bits}{sample} \times \frac{1\ byte}{8\ bits} = 15.4\ MB/ms$$

We find that we will need at least 15.4 MB of memory.

5 Constraints

Constraint 1: Total available budget

We are provided $650 CAD from the ECE Capstone Program and $1,000 CAD from the Ivanov Group. This adds to a total budget of $1,650 CAD which we must not exceed.

Constraint 2: Our timeline is restricted to 8 months

The Capstone project spans two university terms, and therefore we have only 8-months to complete a significant engineering project.

Constraint 3: Can only provide 12-bit samples of data

The RF Data Converter provided with the ZCU111 Evaluation Board has 12-bit ADC channels. Therefore we are constrained to 12-bit samples and do not have any freedom in changing this. As bit-width increases, so does the required size of memory to store all the sampled data, as per Non-Functional Requirement 3.

Constraint 4: Smallest change in voltage level which can be measured is constrained to 0.61mV

We can determine the resolution for an n-bit ADC with the following formula:

$$resolution\ (V) = \frac{2.5}{2^n}$$

We know achieving the lowest possible resolution is ideal because we wish to accurately measure changes in the output voltage level. Resolution represents the smallest change in the ADC input signal (note the input to the ADC is our output voltage) which can be detected. Smaller resolution gives us more granular and therefore more accurate readings.

Our resolution will be 0.61mV and 12'b0000_0000_0001 is equivalent to 0.61mV.

$$\frac{2.5}{2^{12}} = 0.61mV\ resolution$$

Constraint 5: We must design our project to work on the ZCU111 development board

This board has been provided by our client, as is the platform which we must use to complete our project. We considered an alternate FPGA board in the early stages of our design, but due to some physical compatibility issues we were forced to shift our focus to the ZCU111 board. We have further outlined this change in section 8 of the Design Key Document.

References

[1] Emilio M.D.P. (2013) Introduction. In: Data Acquisition Systems. Springer, New York, NY. https://doi.org/10.1007/978-1-4614-4214-1_1

[2] Edmund Lai (2003) Converting analog to digital signals and vice versa, Practical Digital Signal Processing, Newnes, Pages 14-49. https://doi.org/10.1016/B978-075065798-3/50002-3.

[3] Xilinx Zynq Ultrascale+ RFSoC ZCU111 User Guide

https://docs.xilinx.com/v/u/en-US/ug1287-zcu111-rfsoc-eval-tool

[4] Xilinx Zynq Ultrascale+ RFSoC ZCU111 evaluation board purchase price

https://www.xilinx.com/products/boards-and-kits/zcu111.html