

Electronic Devices and Circuits

Jimmie J. Cathey

January 18, 2026

Editor: Stewart Nash

1 Circuit Analysis

1.1 Spice Elements

The passive and active circuit elements introduced in the previous section are all available in SPICE modeling; however, the manner of node specification and the voltage and current sense or direction are clarified for each element by Figure 1. The universal ground node is assigned the number 0. Otherwise, the node numbers n_1 (positive node) and n_2 (negative node) are positive integers selected to uniquely define each node in the network. The assumed direction of positive current flow is from the node n_1 to node n_2 . The four controlled sources—voltage-controlled voltage source (VCVS), current-controlled voltage source (CCVS), voltage-controlled current source (VCCS), and current-controlled current source (CCCS)—have the associated controlling element also shown with its nodes indicated by cn_1 (positive) and cn_2 (negative). Each element is described by an *element specification statement* in the SPICE netlist code. Table 1 presents the basic format for the element specification statement for each of the elements in Figure 1. The first letter of the element name specifies the device and the remaining characters must assure a unique name.

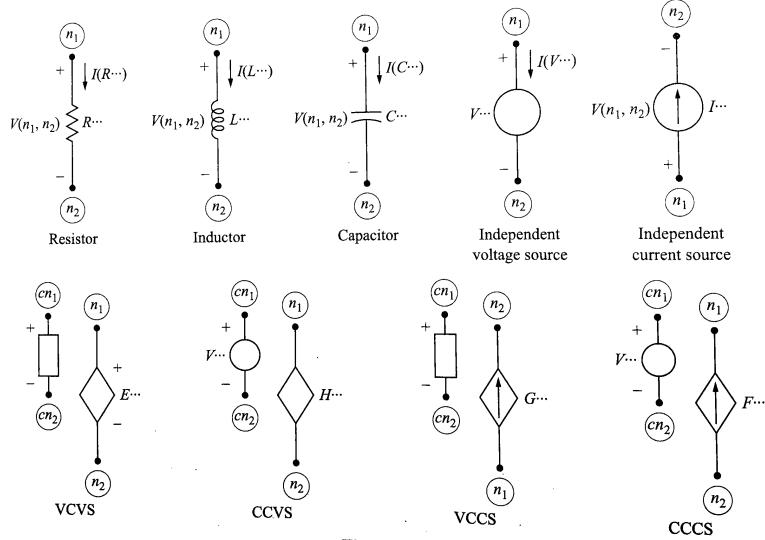


Fig. 1-2

Figure 1:

Table 1:

Element	Name	Signal Type	Control Source	Value
Resistor	R...			Ω
Inductor	L...			H
Capacitor	C...			F
Voltage source	V...	AC or DC ^a		V ^b
Current source	I...	AC or DC ^a		A ^b
VCVS	E...		(cn ₁ , cn ₂)	V/V
CCVS	H...		V...	V/A
VCCS	G...		(cn ₁ , cn ₂)	A/V
CCCS	F...		V...	A/A

a. Time-varying signal types (SIN, PULSE, EXP, PWL, SFFM) also available.
b. AC signal types may specify phase angle as well as magnitude.

1.2 Network Theorems

Example 1.1. Use SPICE methods to determine the Thévenin equivalent circuit looking to the left through terminals 3,0 for the circuit of Figure 2. In SPICE independent source models, an ideal voltage source of 0V acts as a

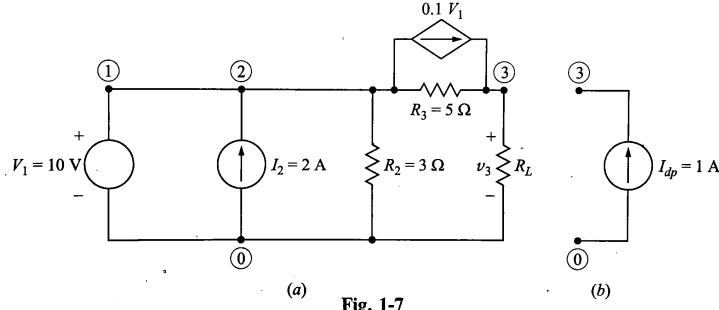


Fig. 1-7

Figure 2:

short circuit and an ideal current source of 0 A acts as an infinite impedance or open circuit. Advantage will be taken of these two features to solve the problem.

Load resistor R_L of Figure 2(a) is replaced by the driving point current source I_{dp} of Figure 2(b). The netlist code that follows forms a SPICE description of the resulting circuit. The code is set up with parameter-assigned values for V_1 , I_2 , and I_{dp} .

```
Ex1_5.CIR - Thevenin equivalent circuit
.PARAM V1value=0V I2value=0A Idpvalue=1A
V1 1 0 DC {V1value}
R1 1 2 1ohm
I2 0 2 DC {I2value}
R2 2 0 3ohm
R3 2 3 5ohm
G3 2 3 (1,0) 0.1 ; Voltage-controlled current-source
Idp 0 3 DC {Idpvalue}
.END
```

If both V_1 and I_2 are deactivated by setting $V1value=I2value=0$, current $I_{dp}=1$ A must flow through the Thévenin equivalent impedance $Z_{Th} = R_{Th}$ so that $v_3 = I_{dp}R_{Th} = R_{Th}$. Execution of <Ex1_5.CIR> by a SPICE program writes the values of the node voltages for nodes 1, 2, and 3 with respect to the universal ground node 0 in a file <Ex1_5.OUT>. Poll the output file to find $v_3 = V(3) = R_{Th} = 5.75 \Omega$.

In order to determine V_{Th} (open-circuit voltage between terminals 3,0), edit <Ex1_5.CIR> to set $V1value=10V$, $I2value=2A$, and $Idpvalue=0A$. Execute <Ex1_5.CIR> and poll the output file to find $V_{Th} = v_3 = V(3) = 14$ V.

1.3 Two-Port Networks

The z parameters and the H parameters can be numerically evaluated by SPICE methods. In electronics applications, the z and h parameters find application in analysis when small ac signals are impressed on circuits that exhibit limited-range linearity. Thus, in general, the test sources in the SPICE analysis should be of magnitudes comparable to the impressed signals of the anticipated application. Typically, the devices used in an electronic circuit will have one or more dc sources connected to bias or that place the device at a favorable point of operation. The input and output ports may be coupled by large capacitors that act to block the appearance of any dc voltages at the input and output ports while presenting negligible impedance to ac signals. Further, electronic circuits are usually frequency-sensitive so that any set of z or h parameters is valid for a particular frequency. Any SPICE-based evaluation of the z and h parameters should be capable of addressing the above outlined characteristics of electronics circuits.

Example 1.2. A sinusoidal source, a dc source, and a 10Ω resistor are connected as shown in Fig. 1-12. If $v_s = 10 \sin(\omega t - 30^\circ)$ V and $V_B = 20$ V, use SPICE methods to determine the average value of $i(I_0)$, the RMS value of $i(I)$, and the average value of power (P_0) supplied to R .

The netlist code below describes the circuit. Notice that the two sources have been combined as a 10 V sinusoidal source with a 20 V DC bias. The frequency has been arbitrarily chosen as 100 Hz as the solution is independent of frequency.

The Probe feature of PSpice is used to display the instantaneous values of $i(t)$ and $p_R(t)$. The running average and running RMS features of PSpice have been implemented as appropriate. Both features give the correct full-period values at the end of each period of the source waveform. Figure 1-13 shows the marked values as $I_0 = 2.0$ A, $I = 2.1213$ A, and $P_0 = 45.0$ W.

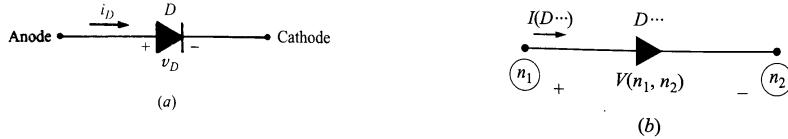


Fig. 2-1

Figure 3:

2 Semiconductor Diodes

2.1 The Ideal Diode

2.2 Diode Terminal Characteristics

Use of the Fermi-Dirac probability function to predict charge neutralization give the *static* (non-time-varying) equation for diode junction current:

$$i_D = I_0(e^{v_D/\eta V_T} - 1) \text{ A} \quad (1)$$

where

$$V_T \equiv kT/q, \text{ V}$$

v_D \equiv diode terminal voltage, V

I_0 \equiv temperature-dependent saturation current, A

T \equiv absolute temperature of $p-n$ junction, K

k \equiv Boltzmann's constant ($1.38 \times 10^{-23} \text{ J/K}$)

q \equiv electron charge ($1.6 \times 10^{-19} \text{ C}$)

η \equiv empirical constant, 1 for Ge and 2 for Si

2.3 The Diode SPICE Model

The element specification statement for a diode must explicitly name a model even if the default model parameters are intended for use. The general form of the diode specification statement is as follows, where the *model name* is arbitrarily chosen:

$D \cdots n_1 n_2$ *model name*

Node n_1 is the anode and node n_2 is the cathode of the diode. Positive current and voltage directions are clarified by Figure 3(b).

In addition, the .MODEL control statement must be added to the netlist code even if the default parameters are acceptable. This control statement is

MODEL *model name D (parameters)*

If the parameters field is left blank, default values are assigned. Otherwise, the parameters field contains the number of desired specifications in the format *parameter name = value*. Specific parameters of concern in this book are documented by Table 2.

Table 2:

Parameter	Description	Reference	Default	Units
I_s	saturation current	I_0 of (1)	1×10^{-14}	A
n	emission coefficient	η of (1)	1	
BV	reverse breakdown voltage	V_R of Figure ??	∞	V
IBV	reverse breakdown current	I_R of Figure ??	1×10^{-10}	A
R_s	ohmic resistance	Subsection 2.2)	0	Ω

3 Characteristics of Bipolar Junction Transistors

3.1 BJT SPICE Model

The element specification statement for a BJT must explicitly name a model even if the default model parameters are intended for use. The general form of the transistor specification statement is as follows:

$Q \cdots n_1 n_2 n_3$ *model name*

Nodes n_1 , n_2 , and n_3 belong to the collector, base, and emitter, respectively. The *model name* is an arbitrary selection of alpha and numeric characters to uniquely identify the model. Positive current and voltage directions for the *pnp* and *npn* transistor are clarified by Figure ??.

In addition, a .MODEL control statement must be added to the netlist code.

This control statement specifies whether the transistor is *pnp* or *npn* and thus has one of the following two forms:

```
MODEL model name PNP (parameters)
MODEL model name NPN (parameters)
```

If the parameter field is left blank, default values are assigned. Non-default desired parameter specifications are entered in the parameter field using the format *parameter name = value*. Specific parameters that are of concern in this book are documented in Table 3.

All parameter values are entered with positive values regardless of whether the transistor is *pnp* or *npn*. Two transistor models will be used in this chapter—*generic model* and *default model*—as introduced in Example 3.1.

Table 3:

Parameter	Description	Major Impact	Default	Units
Is	saturation current	$\uparrow I_s, \downarrow V_{BEQ}$	1×10^{-16}	A
Ikf	high current roll-off	$\downarrow I_{kf}, \downarrow I_C$	∞	A
Isc	base-collector leakage	$\uparrow I_{sc}, \uparrow I_C$	0	A
Bf	forward current gain	$\uparrow B_f, \uparrow I_C$	100	
Br	reverse current gain	$\uparrow B_r, \uparrow \text{rev. } I_C$	1	
Rb	base resistance	$\uparrow R_b, \downarrow dI_B/dV_{BE}$	0	Ω
Rc	collector resistance	$\uparrow R_c, \uparrow V_{CEsat}$	0	Ω
Va	forward Early voltage	$\uparrow V_a, \uparrow dI_C/dt$	∞	V
Cjc	base-collector capacitance	high freq. response	0	F
Cje	base-emitter capacitance	high freq. response	0	F

Example 3.1. Use SPICE methods to generate the CE collector characteristics for an *npn* transistor characterized by (a) the default parameter values and (b) a reasonable set of values for the parameters appearing in Table 3.

```
Ex3_2.CIR
Ib 0 1 OuA
Q 2 1 0 QNPN
*Q 2 1 0 QNPNG
VC 2 0 OV
.MODEL QNPN NPN() ; Default BJT
*.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf=150
** Br=3 Rb=1ohm Rc=1ohm Va=30V Cjc=10pF Cje=15pf)
.DC VC OV 15V 1V Ib OuA 150uA 25uA
.PROBE
.END
```

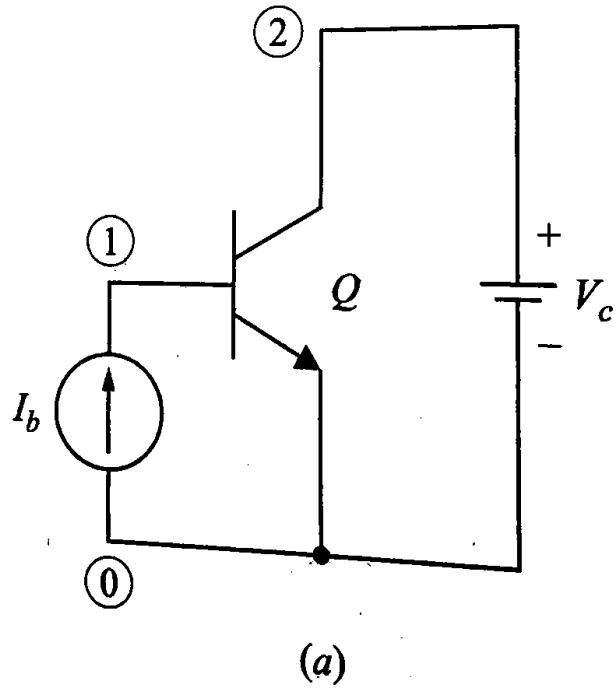


Fig. 3-5

Figure 4:

4 Characteristics of Field-Effect Transistors and Triodes

4.1 JFET SPICE Model

The element specification statement for a JFET must explicitly assign a *model name* that is an arbitrary selection of alpha and numeric characters. The general form is

`J...n1n2n3 model name`

Nodes n_1 , n_2 , and n_3 belong to the drain, gate, and source, respectively. Only the n -channel JFET is addressed in this book. Positive voltage and current directions for the device are clarified by Figure 5. A .MODEL control

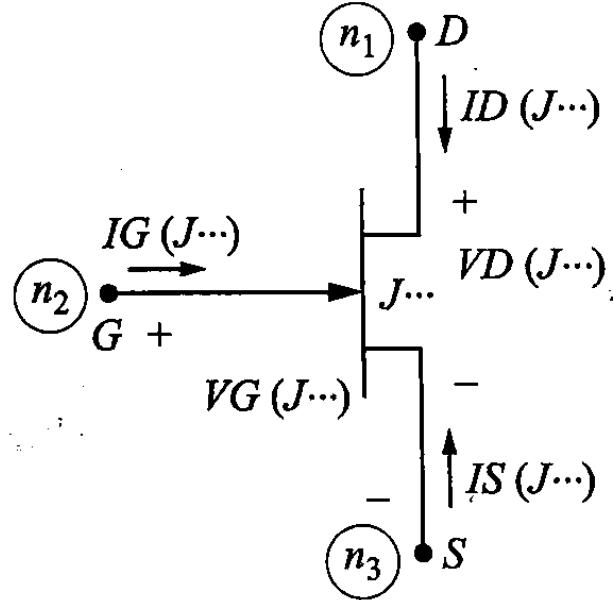


Fig. 4-3

Figure 5:

statement must appear in the netlist code for a JFET circuit. The control statement has the following format:

MODEL *model name* NJF (*parameters*)

If the parameter field is left blank, default values are assigned. Nondefault parameters are entered in the parameter field using the format *parameter name* = *value*. The specific parameters of concern in the book are documented by Table 4. The SPICE model describes the JFET in the pinchoff region by

$$i_d = \frac{I_{DSS}}{(V_{to})^2} (V_{to} + v_{GS})^2 = Beta(V_{to} + v_{GS})^2 \quad (2)$$

Table 4:

Parameter	Description	Major Impact	Default	Units
Vto	pinchoff voltage	shorted-gate current	-2	V
Beta	transcond. coeff.	shorted-gate current	0.0001	A/V ²
Rd	drain resistance	current limit	0	Ω
Rs	source resistance	current limit	0	Ω
CGS	gate-source cap.	high frequency	0	F
CGD	gate-drain cap.	high frequency	0	F

Example 4.1. Use SPICE methods to generate (a) the CS drain characteristics and (b) the transfer characteristic for an *n*-channel JFET that has the parameter values Vto= -4V, Beta = 0.0005 A/V², Rd = 1 Ω , Rs = 1 Ω , and CGS = CGD = 2pF.

(a) Figure 4.1(a) shows a connection method for measurement of both the drain characteristics and the transfer characteristic. The following netlist code generates the drain characteristics that have been plotted using the Probe feature of PSpice as Figure 4.1(b).

```
Ex4_1a.CIR - JFET drain characteristics
vGS 1 0 OV
vDS 2 0 OV
J 2 1 0 NJFET
.MODEL NJFET NJF ( Vto=-4V Beta=0.0005ApVsq
+ Rd=1ohm Rs=1ohm CGS=2pF CGD=2pF)
.DC vDS OV 25V 0.5V vGS OV -4V 0.5V
.PROBE
.END
```

4.2 MOSFET SPICE Model

The element specification statement for a MOSFET must explicitly assign a *model name* (an arbitrary selection of alpha and numeric characters) having the general form

$$M \cdot \cdot n_1 n_2 n_3 n_4 \text{ model name}$$

Nodes n_1 , n_2 , n_3 , and n_4 belong to the drain, gate, source, and substrate, respectively. Only the *n*-channel MOSFET is addressed where the device positive voltage and current directions are clarified by Figure 6. Format of

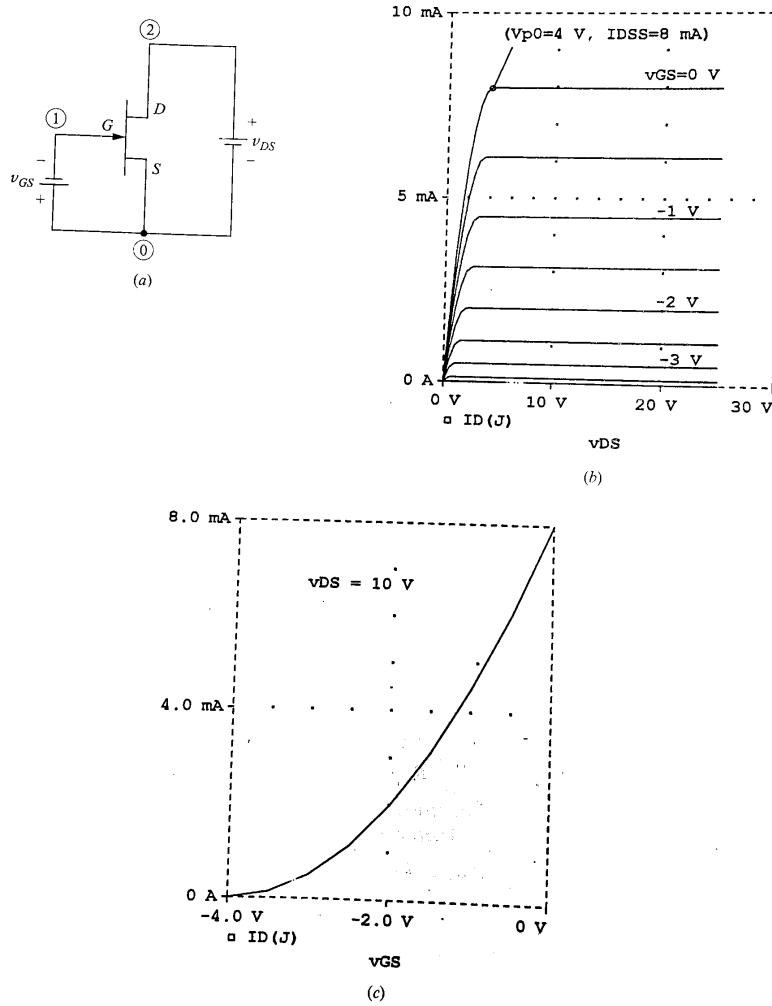


Fig. 4-4

the .MODEL control statement that must appear in the netlist code for a MOSFET circuit is as follows:

MODEL *model name* NMOS (*parameters*)

A blank parameter field results in assignment of default parameter values. Nondefault parameters are entered in the parameter field as *parameter name* = *value*. The specific parameters of concern in the book are documented by

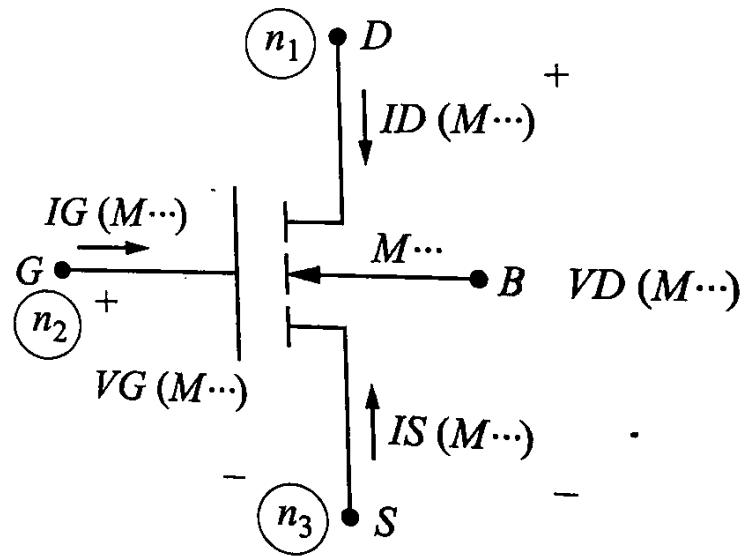


Fig. 4-10

Figure 6:

Table 5. The SPICE model characterizes the enhancement mode MOSFET in the pinchoff region by

$$i_d = \frac{I_{D_{on}}}{(V_T^2)}(v_{GS} - V_T)^2 = \frac{K_p}{2}(v_{GS} - V_T)^2 \quad (3)$$

Table 5:

Parameter	Description	Default	Units
Vto	Threshold voltage	0	V
Kp	Transcond. coeff.	2×10^{-5}	A/V ²
Rd	Drain resistance	0	Ω
Rg	Gate resistance	0	Ω

5 Transistor Bias Considerations

5.1 Stability-Factor Analysis

$$S_I = \frac{\Delta I_{CQ}}{\Delta I_{CBO}} \Big|_Q \approx \left. \frac{\partial I_{CQ}}{\partial I_{CBO}} \right|_Q \quad (4)$$

5.2 Parameter Variation Analysis with SPICE

PSpice offers two features that allow direct study of circuit performance change due to parameters variation. The first of these features is simply called *sensitivity analysis*. It is invoked by a control statement of the following format:

```
.SENS sensitive variable
```

The *sensitive variable* can be any node voltage or the current through any independent voltage source. A table is generated in the output file that gives the sensitivity of the sensitive variable to each parameter (specified or default) in the model of all BJTs and diodes that are directly comparable with (4) and

6 Small-Signal Midfrequency BJT Amplifiers

6.1 BJT Amplifier Analysis with SPICE

Since SPICE models of the BJT (see Chapter 3) provide the device terminal characteristics, a transistor amplifier can be properly biased and a time-varying input signal can be directly applied to the completely modeled amplifier circuit. Any desired signal that results can be measured directly in the time domain to form signal ratios that yield the current and voltage gains. With such modeling, any signal distortion that results from nonlinear operation of the BJT is readily apparent from inspection of the signal-time plots. Such an analysis approach is the analytical equivalent of laboratory operation of the amplifier where the time plot of signals is analogous to oscilloscope observation of the amplifier circuit signals.

SPICE capabilities also lend themselves to BJT amplifier analysis using the small-signal equivalent circuits. In such case, the voltage-controlled voltage source (VCVS) and the current-controlled current source (CCCS) introduced

in section 1.3 find obvious application in the small-signal equivalent circuits of the type shown in Fig. 6-1. Either time-varying analysis (.TRAN command statement) or sinusoidal steady-state analysis (.AC command statement) can be performed on the small-signal equivalent circuit.

Example 6.1. For the amplifier of Fig. 3-10(a), let $v_i = 0.25 \sin(2000\pi t)$ V, $V_{CC} = 15$ V, $CC_1 = CC_2 = CC = 100 \mu F$, $R_1 = 6 k\Omega$, $R_2 = 50 k\Omega$, $R_C = R_L = 1 k\Omega$, and $R_i = R_E = 100 \Omega$. The transistor is characterized by the model of Problem 5.4. Use SPICE methods to determine the CE hybrid parameters of (6.5) through (6.8) for this transistor at the point of operation. The netlist code below describes the circuit.

```
EX6_5.CIR
vi 1 0 SIN(0V 250mV 10kHz)
Ri 1 2 100ohm
CC1 2 3 1000uF
CC2 4 7 1000uF
R1 3 0 6kohm
R2 3 6 50kohm
RC 6 4 1kohm
RE 5 0 100ohm
RL 7 0 1kohm
VCC 6 0 15V
Q 4 3 5 QNPNG
.MODEL QNPNG NPN(Is=10fA Ikf=150mA Isc=10fA Bf=150
+ Br=3 Rb=1ohm Rc=1ohm Va=75V Cjc=10pF Cje=15pF)
.TRAN 1us 0.1ms
.PROBE
.END
```

After executing `jEx6_5.CIR`, the plots of Fig. 6-8 can be generated by use of the Probe feature of PSpice. The resulting h -parameter value is indicated on each of the four plots of Fig. 6-8.

7 Small-Signal Midfrequency FET and Triode Amplifiers

7.1 FET Amplifier Gain Calculation with SPICE

SPICE models of the JFET and MOSFET (introduced in Chapter 4) provide the terminal characteristics of the devices; thus, an amplifier can be properly biased and time-varying input signal directly applied to the completely modeled amplifier circuit. Such a simulation is the analytical equivalent of laboratory amplifier circuit operation. Any desired signal can be measured directly in

the time domain to form signal ratios that yield current and voltage gains. Any signal distortion that may result from device nonlinearity is readily apparent from inspection of the signal time plots.

8 Frequency Effects in Amplifiers

8.1 Frequency Response Using SPICE

SPICE methods offer a frequency sweep option that allows a small-signal, sinusoidal steady-state analysis of a circuit. The frequency sweep is invoked by a control statement of the following format:

.AC DEC points start freq end freq

Node voltages and device current are inherently complex number values. The magnitudes and phase angles of calculated quantities can be retrieved by the Probe feature of PSpice by appending a *p* and *n*, respectively, to the variable. For example, magnitude and phase angle of the voltage between nodes 2 and 3 are specified by $Vm(2,3)$ and $Vp(2,3)$.

Example 8.1. For the BJT amplifier circuit of Fig. 3-10, assume $C_c \rightarrow \infty$. The small-signal equivalent circuit is given by Fig. 8-4 where $R_B = R_1 \parallel R_2$. Let $h_{oe} = h_{re} = 0$, $h_{fe} = 90$, $R_1 = 1\text{k}\Omega$, $R_2 = 16\text{k}\Omega$, $R_E = 500\Omega$, $C_E = 330\mu\text{F}$, $R_C = 1\text{k}\Omega$, and $R_L = 10\text{k}\Omega$. Use SPICE methods to determine the low-frequency cutoff point.

The netlist code that follows describes the circuit

```
Ex8_9.CIR
vi 1 0 AC 0.250V
R1 1 0 1kohm
R2 1 0 16kohm
Vsen 1 2 DC 0V
Rhie 2 3 200ohm
Fhfe 3 4 Vsen 90
RE 3 0 500ohm
CE 3 0 330uF
RC 4 0 1kohm
RL 4 0 10kohm
.AC DEC 25 10Hz 10kHz
.PROBE
.END
```

Execute *Ex8_9.CIR* and use the Probe feature of PSpice to yield the plots of Fig. 8-13. From the marked points, it is seen that the low-frequency cutoff is $f_L = 214.4\text{Hz}$, where the voltage gain has a value of $A_{vL} = 289.7$.

The above example utilized the small-signal equivalent circuit. Small-signal analysis frequency sensitivity can also be implemented using the SPICE model of the transistor directly.

9 Operational Amplifiers

9.1 SPICE Op Amp Model

Figure 9-1(a) presents the equivalent circuit model of the op amp using a VCVS to implement the gain. This circuit is easily realized by SPICE methods using the VCVS model of Fig. 1-2 and Table 1-1. It is frequently convenient to describe the op am through the use of a subcircuit as illustrated by the following netlist code:

```
.SUBCKT OPAMP 1 2 3 4
*      Model Inv NInv Out Com
Rd 1 2 500kohm
E 5 4 (1,2) -1e5
Ro 5 3 100ohm
.ENDS OPAMP
```

The nodes are labeled in Fig. 9-1(a). Input impedance ($R_d = 500 \text{ k}\Omega$), output impedance ($R_o = 100 \Omega$), and open-loop voltage gain ($A_{OL} = -1 \times 10^5$) are typical values that can be changed if an application warrants. Also, SPICE libraries usually contain subcircuit models of commercially available op amps that can be utilized.

Example 9.1. Use SPICE methods to model the noninverting amplifier of Fig. 9-3 if the op amp has the parameter values of the subcircuit OPAMP above. Let $v_s = 0.5 \sin(200\pi t)$ V, $R_1 = 1 \text{ k}\Omega$, and $R_2 = 10 \text{ k}\Omega$. Verify that the voltage gain predicted by (9.7) results.

Netlist code describing the circuit is shown below:

```
Ex9_11.CIR
vs 1 0 SIN(0V 0.5V 1kHz)
R1 2 0 1kohm
R2 3 2 10kohm
XA 1 2 3 0 OPAMP
.SUBCKT OPAMP 1 2 3 4
*      Model Inv NInv Out Com
Rd 1 2 500kohm
E 5 4 (1,2) -1e5
```

```

Ro 5 3 100ohm
.ENDS OPAMP
.TRAN 1us 2ms
.PROBE
.END

```

Execute `jEx9_11.CIR` and use the Probe feature of PSpice to plot Fig. 9-10. By use of the marked values Fig. 9-10,

$$A_v = \frac{5.5}{0.5} = 11 \quad (5)$$

The voltage gain predicted by (9.7) is

$$A_v = 1 + \frac{R_2}{R_1} = 1 + \frac{10 \times 10^3}{1 \times 10^3} = 11 \quad (6)$$

Hence, (9.7) is validated.

10 Switched Mode Power Supplies

10.1 Buck Converter

The SMPS circuit of Figure 7, known as a *buck converter*, produces an average value output voltage $V_2 = \langle v_2 \rangle \leq V_1$.

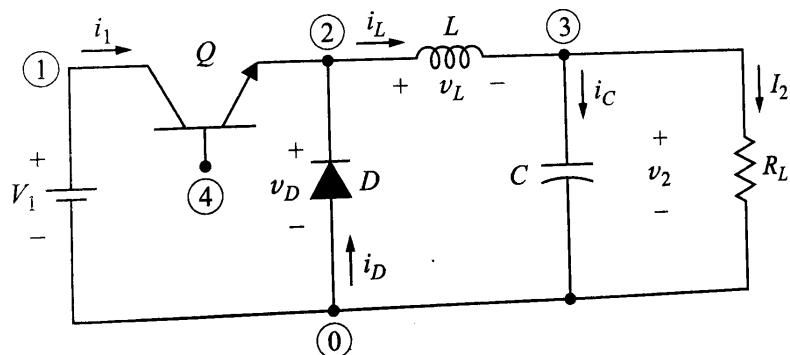


Fig. 10-2 Buck converter

Figure 7: Buck converter

10.2 Boost Converter

The *boost converter* SMPS circuit of Figure 8 produces an average value output voltage $V_2 = \langle v_2 \rangle > V_1$.

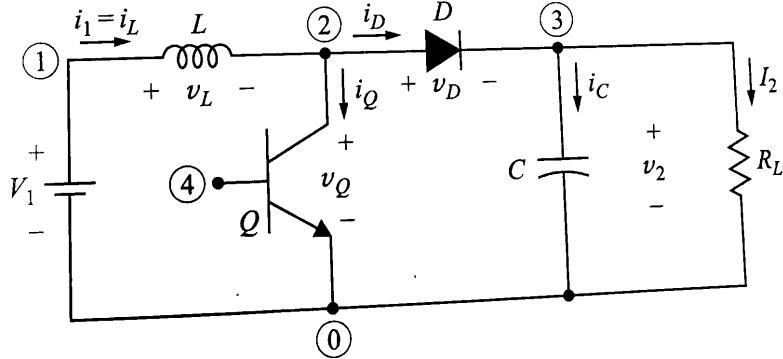


Fig. 10-4 Boost converter

Figure 8: Boost converter

10.3 SPICE Analysis of SMPS

For simulation of near ideal (lossless) SMPS, the switch element Q can readily be modeled using the PSpice voltage-controlled switch. The element specification statement for the voltage-controlled switch has the form

S...n₁ n₂ c₁ c₂ VCS

Any alpha-numeric combination suffix can follow S to uniquely specify the voltage-controlled switch. The nodes are clarified by Figure ???. A fast rise and fall time (5 ns), 1-V pulse should be used for the control voltage v_{SW} . Accepting the default ON state and OFF state control voltages of 1 V and 0 V, respectively, results in duty cycle ON time approximately equal to the pulse duration. For minimum conduction losses, the ON state resistance of the voltage control switch should be specified in the .MODEL statement by

.MODEL VCS VSWITCH (RON = 1e-6)

Example 10.1. Use SPICE methods to model the buck converter of Figure 7; let $D = 0.5$, $f_s = 25$ kHz, $L = 100 \mu\text{H}$, $C = 50 \mu\text{F}$, and $R_L = 5 \Omega$. Generate

the set of waveforms analogous to Figure ??.

The netlist code follows, where the initial conditions on inductor current and capacitor voltage were determined after running a large integer number of cycles to find the repetitive values.

```
Ex10_5.CIR
* BUCK CONVERTER
* D=DUTY CYCLE, fs=SWITCHING FREQUENCY
.PARAM D=-.5 fs=25e3Hz
V1 1 0 DC 12V
SW 1 2 4 2 VCS
VSW 4 2 PULSE(0V 1V 0s 5ns 5ns {D/fs} {1/fs})
L 2 3 100uH IC=0.6A
D 0 2 DMOD
C 3 0 50uF IC=6V
RL 3 0 5ohm
.MODEL DMOD D(N=0.01)
.MODEL VCS VSWITCH (RON=1e-6ohm)
.TRAN 5us 0.2ms 0s 100ns UIC
.PROBE
.END
```

Execute Listing 10.1 <Ex10_5.CIR> and use the Probe feature of PSpice to plot the waveforms of Figure 10.1.

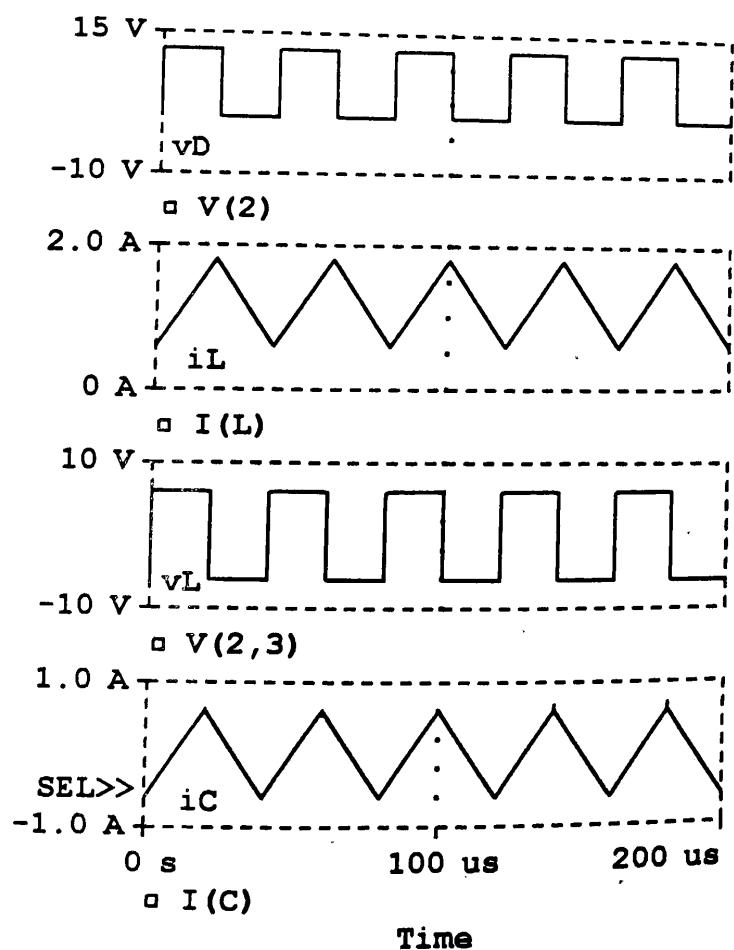


Fig. 10-9