University of California, Santa Cruz
ECE Department

EE-157 Winter-2019

Midterm Exam.
Due: Monday, 2/25/2019 (online via electronic pdf submission)

Name: Stephen Kemp

HONOR CODE: After finishing this test, please certify the integrity of the exam by signing below:

In recognition of the integrity of the engineering profession and the UCSC Honor Code, I certify that I have kept the contents of this exam personal and confidential, and have neither given nor received unauthorized aid.

Signature:

This midterm, to be completed outside of class, will test what you have learned about the engineering design of RF circuits / systems by having you begin serious work on your laboratory project for this quarter and answer questions about distributed circuit theory. Collaborating with other students is permitted and encouraged, but the intellectual content of the written work you submit must be wholly and originally your own. If you discussed any of these problem with other students, indicate who they were and what role they played in your understanding.

Please include this cover page with your online submission and restate questions 2 and 3 with your answers.

Midterm

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EE 157/L
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1 Problem 1: AM Reciever Initial Design Report

My goal for this project is to build an AM receiver that receives the KSCO radio station on 1080kHz AM broadcast. My initial block diagram is shown in Figure 1. The parts of the block diagram that I plan to buy pre-made are the down mixer, which already is in our lab kits as an SA602, the LM386 audio amplifier because this is an RF hardware course and not an audio hardware design course, and the loop-stick antenna. Everything else I plan to design at least partially. My goal is to have an output power of between 10 and 30 dBm because most of the speakers I have seen report reliable operation at 1W.

My plan is to design from output to input, so I'll start with the product detector SSB demodulator. I plan to implement the product detector as a diode-ring oscillator (basic schematic drawn out on page 149 of my notebook). One important note that I found from Hayward is that the diode ring mixer needs to have a solid matched impedance termination to work properly. Hayward recommends an IF termination with better than a 2:1 VSWR, or 10-dB return loss because reflected signals will enter back into the mixer and create imaging and phase-shifts.

I'm planning to implement the BFO for the product detector as a 455kHz Colpitts oscillator using a JFET, possibly with a tunable capacitor to tune the BFO frequency once I have audible signal feedback. I plan on deadbugging this oscillator before the demodulator, potentially on the same board. The BFO needs to be very accurate **very stable**. I haven't been able to find any quartz crystals at 455kHz, so I may just have to make due with an LC tank. The LPF on the input to the LM386 may not be necessary because the sum image from the product detector will be in the MHz range, and should be filtered out by the speaker itself. The LM386 datasheet reports reliable gains of 20dB, so that's the nominal gain I'm assuming for that block.

Working backwards, there is the IF amplification stage. I'm planning to implement up to 4 cascaded amplifier stages with a total gain of between 80dB and 100dB. From looking through the IF amplifier designs in Hayward, 20-30dB per stage seems like a reasonable nominal value. I'm looking specifically at modifying a version of the common-emitter BJT amplifier seen in figure 6.41 of Hayward. I'm planning to do one of these stages using deadbug and test it to figure out what is a reasonable gain I can expect from this amplifier, then duplicate it up to 4 times in the final design. Most likely there will need to be impedance matching between the stages to prevent power loss.

The narrow BPF shown in the block diagram will be given to us as a 455kHz 25kHz-BW ceramic filter. This informed my decision to make the IF 455kHz. We are also given the SA602 to use as an IF down-mixer. The datasheet for the SA602 gives several possible oscillator configurations to attach to pins 6 and 7 to implement a local oscillator (represented in my block diagram as 'LO'). The mixer has a built-in amplifier and buffer, so it just requires the passive tank circuit. I figure that I'll try out the Hartley oscillator and see if I can get it working reliably on deadbug before transferring it to a PCB. There will definitely need to be impedance matching both before and after the SA602.

As for the low-noise-amplifier preceding the SA602, Hayward seems skeptical at their use and recommends not using them 'just to make the signal louder'. I'm still concerned about the recoverability of the signal from the loop-stick antenna, so I'm going to try to implement one anyway. The common-gate JFET circuit from figure 6.33 in Hayward seems interesting and I could re-tune it for use at 1080kHz. Hayward claims that this circuit can produce a gain of 12dB or 14dB at 21MHz depending on the input-network values with a noise figure of 1.5dB and 5dB respectively. Another option suggested by Hayward would be a source-follower JFET circuit like the one shown in figure 6.34.

The main purpose of the preselect filter is that of image rejection from the down-mixer. This

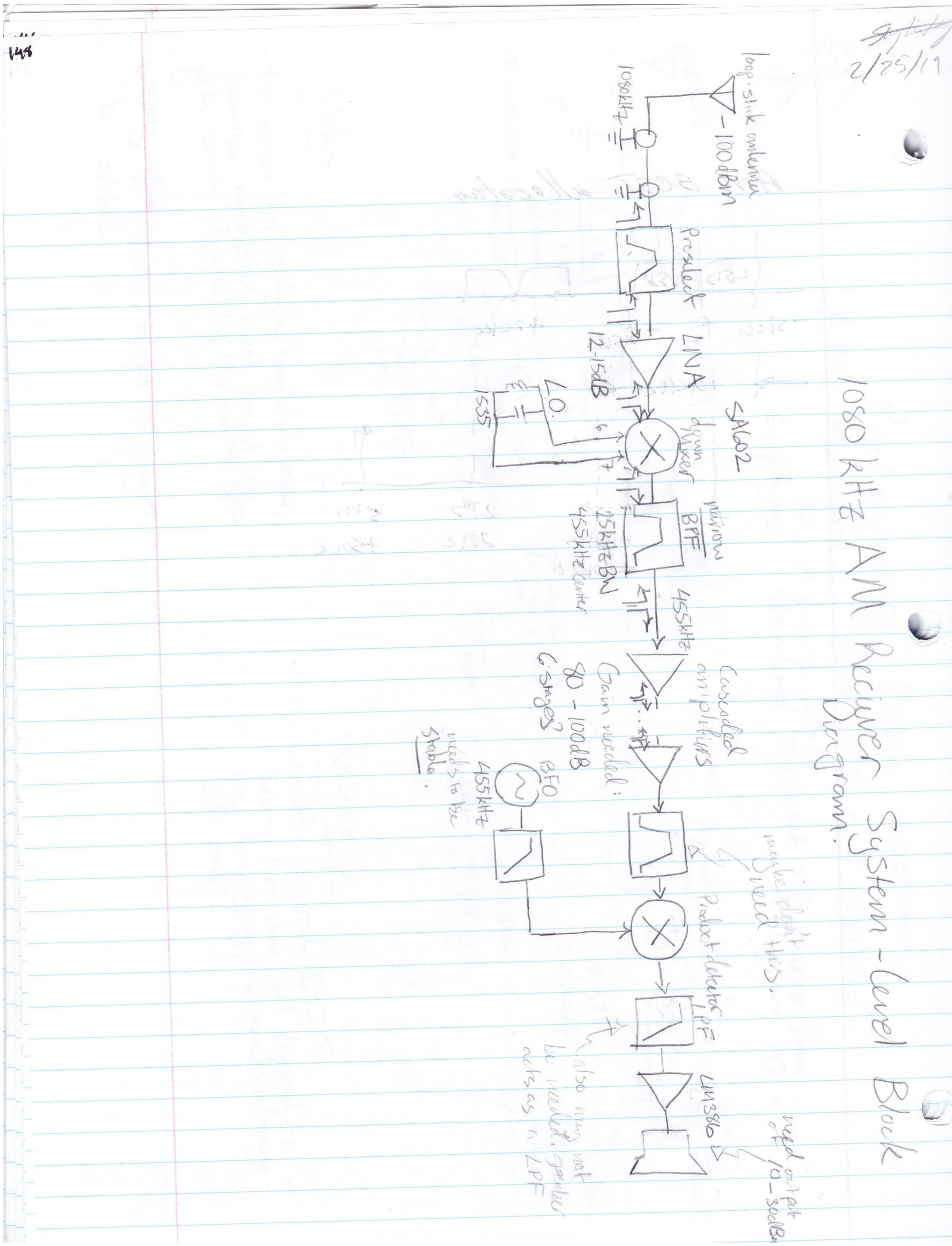

Figure 1: Annotated system level block diagram of the AM receiver

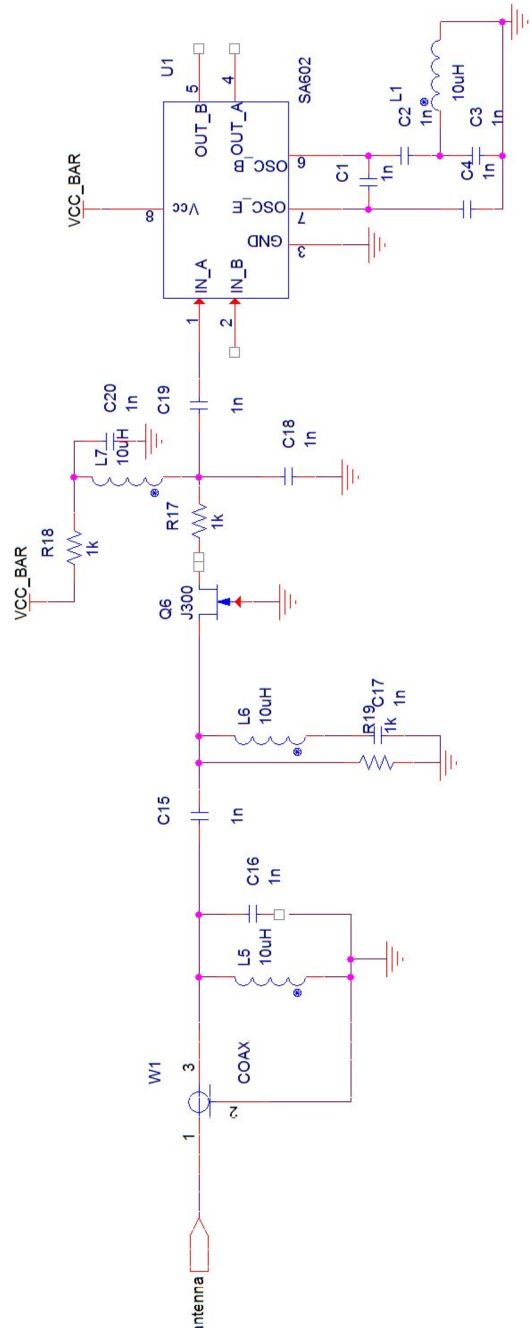

Figure 2: Capture Schematic of Image rejection filter, LNA and SA602 with surrounding circuit PROTOTYPE TOPOLOGY, COMPONENT VALUES ARE PLACEHOLDER

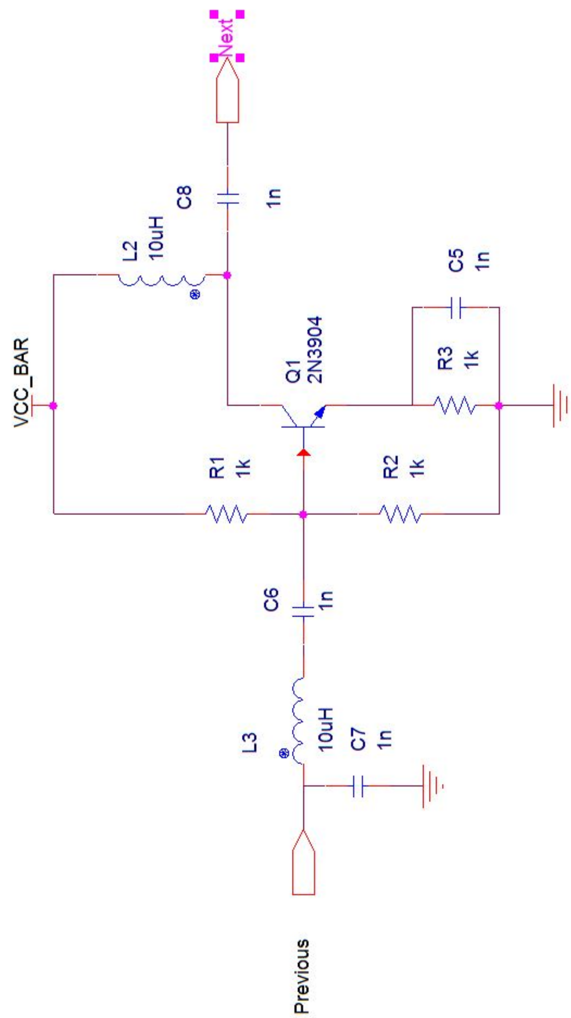

Figure 3: Capture Schematic of IF amplifier with impedance matching on input and output
PROTOTYPE TOPOLOGY, COMPONENT VALUES ARE PLACEHOLDER

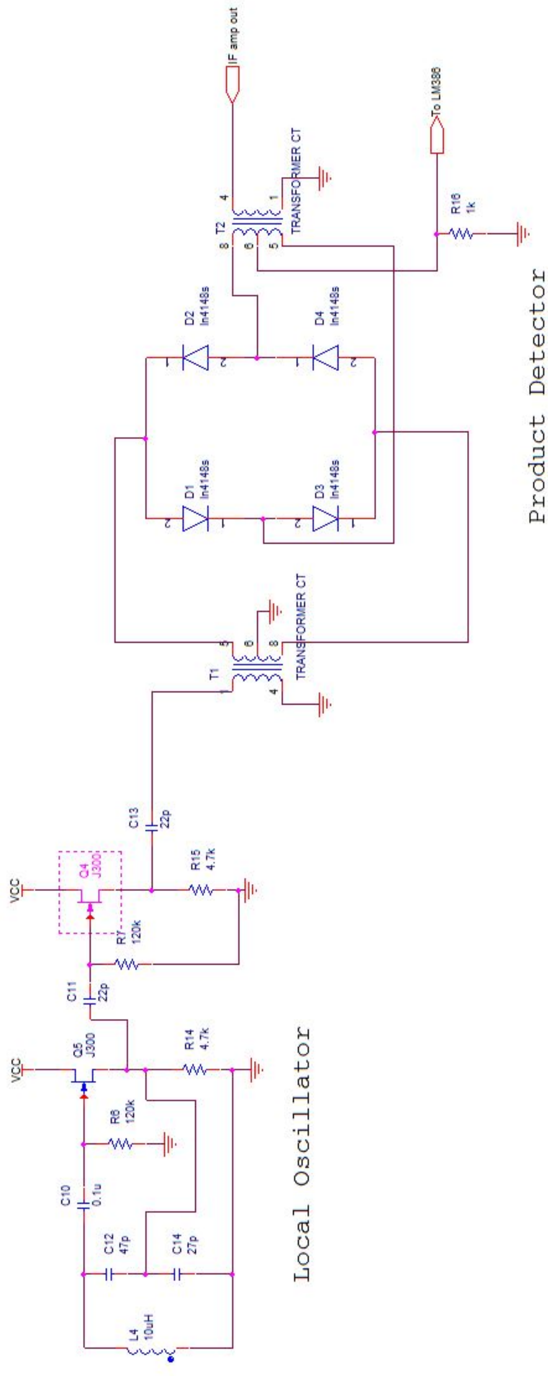

Figure 4: Capture Schematic of diode ring product detector with BFO
PROTOTYPE TOPOLOGY, COMPONENT VALUES ARE PLACEHOLDER

means I need a filter that will eliminate signals in the 2.5 MHz range as these will produce images with the 1535 kHz oscillator and project them down into the 1080kHz range. It should be fairly easy to make a filter centered at 1MHz with .5MHz or less bandwidth just with a single-stage LC bandpass filter. I should be able to do this simply with an LC shunt.

The loop-stick antenna is the component that I'm least concerned about at this point. I would like to do some research into this topic by reading the antenna theory book provided by Petersen in the lab at some point in the next 2 weeks. This is the last thing I'm planning on focusing on after I implement the rest of the receiver with signals generated using the lab RF signal generators.

At this point, my capture schematics show the prototype topologies I plan to use. I haven't gone through the actual circuit design to determine component values, and as such, the shown component values do not in any way reflect the actual values of the components when the prototype is actually implemented. Figure 2 shows the low-noise amplifier topology I plan to use, this is the topology from Hayward figure 6.33. If this doesn't work out, I plan to use a common-source JFET instead. Also shown is the my rendering of the SA602. One question I still don't know the answer to is whether or not I can use the SA602 as a single-line signal by just grounding INB and ignoring OUTB, which I'll have to look further into. Also not pictured are the impedance matching circuits that will be connecting these stages.

Figure 3 shows the IF amplifier topology I plan to use, the common source JFET. This circuit includes a simple impedance matching circuit on the input and the output. Figure 4 shows the diode-ring product detector topology I plan to use as well as the Colpitts oscillator I plan to use for the BFO. One feature I will probably need to add in implementation is a low-pass filter on the output of the local oscillator to reduce the harmonic noise to provide a less noisy LO signal for the Product detector.

2 Problem 2

The engineering model of an unbalanced coaxial transmission line is discussed on pg 6 in Section 4 of my lecture notes. At first glance, it appears to be simply a lumped circuit model composed of ideal circuit elements. What specifically makes this model applicable to a transmission line? In the math that follows identify where and justify why time-domain voltage and current gradients must exist on the line for the later phasor-domain travelling wave solutions to have any meaning.

The specificity that makes this a distributed circuit, and applicable to a transmission line, rather than a lumped circuit is that the seemingly 'lumped' circuit components are actually defined as distributed quantities. Rather than being defined as an L Henry inductor, the ideal inductor has a value of L Henrys/meter, thus the values of the components have no meaning without specifying the 1 dimensional distance the distributed components occupy.

If there were no time-domain voltage or current gradients on the line, then the time-derivatives of voltage and current on the line go to zero. If this is the case, then equation 1 shown on page 7 of section 4 goes to

$$\frac{\delta v}{\delta z} = iR \tag{1}$$

$$\delta v = iR\delta z \tag{2}$$

Which becomes Ohm's law when you integrate with respect to space across the whole transmission line. This causes the concept of time-frequency to become meaningless, and the time-harmonic phasor domain representation of equation 1 also reduces to Ohm's law because ω goes to 0. Likewise equation 2 on the same page also reduces to Ohm's law when the time-gradient of voltage = 0. This especially breaks down in the process of obtaining equation 3 on page 8 because the voltage and current cannot be treated as phasors when they are not harmonic-time varying and also, the propagation constant γ reduces to $\sqrt{G * R} = 1$ when $\omega = 0$.

3 Problem 3

The reflection coefficient can be plotted on the complex plane (see text, eqn 3.1 and Fig. 3-1) with the center at 0. Discuss the conceptual meaning of this chart, and then proceed to show how it can then be modified to create the Smith Chart along with the necessary mathematics.

All of the equation and figure references in this section will refer to the LB course text.

The reflection coefficient Γ plotted on the complex plane (shown in Fig. 3-1 of LB) shows all of the possible values of Γ that can be generated from possible line and load impedances Z_L and Z_0 from equation 3.1. All possible values of Γ can be mapped onto this circle in the complex plane of radius 1. This is because the reflection coefficient is measure of signal power reflected back into a transmission line at a point of impedance discontinuity. The circle of radius 1 describes the amplitude attenuation and phase shift of a reflected signal relative to the incident signal at the discontinuity, with 1 indicating full in-phase reflection, -1 being full opposite-phase reflection and 0 being full transmission (Z_L and Z_0 are matched). The circle only has radius 1 because if the reflection coefficient phasor had amplitude greater than 1, then power would have been added to the transmission line by the load impedance, meaning the impedance was negative. This could be relevant for an active load, but the plot is only trying to account for passive loads.

To create the smith chart from the reflection coefficient plot, we want to add representations of the normalized input resistance and reactance. We can do this by mapping constant values of resistance and reactance from the input impedance, $z_i n$ plane to the reflection coefficient plane. These mappings are presented in equation 3.10 for resistance and equation 3.11 for reactance. Both of these relations are derived from the relation of input impedance to the complex reflection coefficient shown in equation 3.3. Equation 3.10 shows that if the input resistance is held constant, then that is represented on the Γ plane as a circle centered at $\frac{r}{r+1}$ on the real axis, with a radius of $\frac{1}{r+1}$. Equation 3.11 shows that if the input reactance is held constant, that is represented on the Γ plane as a circle centered at $(1, \frac{1}{x})$ with radius $\frac{1}{x}$.

Now that we have general normalized impedances represented on the Γ plane, we can use this tool to determine transformed load impedances seen through a transmission line. You can find the normalized complex load impedance r + jx as the point where the corresponding resistance and reactance circles intersect, and travel about the center of the circle by a number of degrees equal to $2\beta d$ and find the normalized input impedance as the two circles that intersect at the resulting point.