*Computer Organization and Architecture*

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Keywords—component, formatting, style, styling, insert (key words)

# Overview

The design problem was to implement a standard five-stage pipelined 32-bit MIPS processor. The proposed processor is able to implement a subset of 27 instructions of the MIPS instruction set architecture. In addition, the processor implements early branching meaning that branch instructions are resolved at the decoding stage rather than the execution stage. This optimization reduces delays imposed by each branch instruction and thereby reduces the performance loss. We will provide a brief overview of each stage in this section.

The instruction fetch stage mainly consists of the program counter, instruction memory, and an ALU. At the beginning of the program, machine code instructions are loaded into the instruction memory module. The ALU and program counter work in tandem to reference the next instruction address. Since each instruction is 32-bits and MIPS uses byte addressing, the ALU adds four to the program counter value to fetch the next instruction. There is also a 2:1 mux that selects between the ALU output and the decoded branch address. This allows our processor to move to another instruction address if our program must branch or jump.

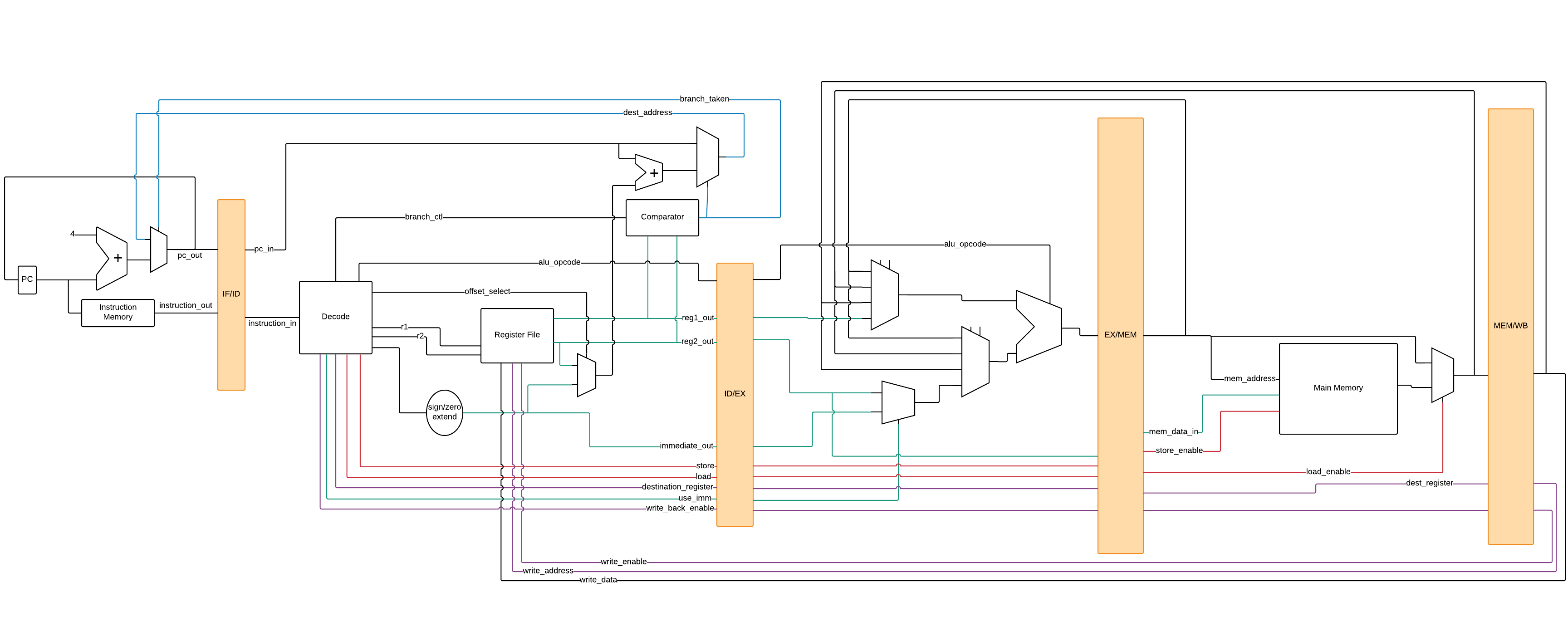
The decode stage mainly consists of our decoder and register file. The decoder interprets the fetched instruction and then outputs the register addresses that the register file will use for referencing and outputting the required data. Since we implemented early branching, branching instructions are resolved in this stage. The decoder outputs the target address of branch instructions and sends it to the comparator which decides if the program must branch/jump. If the program indeed needs to branch, the target address is added to the current instruction address and sent back to the IF stage for updating the program counter. Finally, there is also a sign/zero extender for sign extending immediate values from 16 bits to 32.

The execute stage mainly consists of a comparator, 4:1 mux’s, a 2:1 mux, and the ALU. The ALU is the most important component of this stage since it performs the arithmetic necessary to execute the instruction. If we are performing a load or store, the ALU adds the offset (forwarded from ID stage) with the register data to create the necessary memory address. If we are performing an add, subtract etc. the ALU performs the necessary arithmetic on the data that has been presented to it by the ID stage. The 2:1 mux is used to toggle between feeding the ALU register contents, or an immediate value based on the decoded instruction. It is controlled by the decoder which outputs a signal to indicate whether the mux should select the register data or the immediate value. Finally, the comparator and 4:1 mux’s implement our data forwarding mechanism. The 4:1 mux’s are connected to the EX, MEM, and WB stage. The comparator checks the register addresses to see if any of the following instruction make references to the same register address that is in the EX, MEM, or WB stages and then sends a control signal to the 4:1 mux’s so that they can select the appropriate register data.

The MEM stage houses our main memory block and either retrieves data on a load instruction or re-writes the referenced memory address on store instructions (in which case, a write enable request has been submitted by the decoder and sent to the memory block). Furthermore, there is a 2:1 mux at the output controlled by the load signal which controls the output of the MEM stage. If we are executing a load instruction, the data from the desired memory location is selected and sent to the register file for write-back. Otherwise, the output of the ALU is selected for writing back to the register file since that data will be the result of executing the instruction.

At the very end of our processor is the WB stage which forwards the resulting data of an instruction to the required location such as the register file and the EX stage (for data forwarding). Figure 1 shows the high-level organization of our processor. It details the connections and signals within and between each stage.

1. Block diagram of the pipelined processor. Components between the latches (in orange) were organized into module blocks. The top level module manages signals and data that are used by multiple stages.



# Procedure

## Design Approach

As this is a large project with five stages and several components per stage, we took a multi-step approach to design. First, we needed a complete block diagram detailing all the components needed for each stage, as seen in *Figure 1*. After verifying with the course material and online sources that we had all the necessary components and control signals, we wrote the descriptions of these components stage by stage. As we were a group of four, we could do the component design in parallel. Upon completion of the components of a stage, they were integrated together as a single block in a higher-level module. This module contained all the input and output signals of its respective stage and connected the ports of each component to the necessary signals. We should note that the latches dividing each of the five stages were written as modules of their own. Finally, after each stage had successfully integrated the components within them, a top-level module was designed for connecting the entire pipeline together. In this top-level module, inter-stage signals such as forwarding signals, write enabling and write back signals were implemented and connected to their required ports.

## Testing and Evaluation

Identify applicable funding agency here. If none, delete this text box.

The pipelined processor was tested in several stages. The first testing stage was to evaluate each individual component separately to ensure that they behaved as expected. For example, the adder component was tested in ModelSim by forcing two inputs and an enable signal and verifying that it outputted the correct value. The next testing stage was to evaluate groups of components that corresponded to each of the five pipeline stages. This was done to verify that given the correct inputs and signals, each pipeline stage would be able to produce the correct outputs. Lastly, the entire pipelined processor was tested. A set of MIPs instructions was loaded into the system and the results of the output file were used to verify that all the operations and procedures performed as expected.

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# Optimizations

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*a**b* 

Note that the equation is centered using a center tab stop. Be sure that the symbols in your equation have been defined before or immediately following the equation. Use “(1)”, not “Eq. (1)” or “equation (1)”, except at the beginning of a sentence: “Equation (1) is . . .”

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* The word “data” is plural, not singular.
* The subscript for the permeability of vacuum **0, and other common scientific constants, is zero with subscript formatting, not a lowercase letter “o”.
* In American English, commas, semicolons, periods, question and exclamation marks are located within quotation marks only when a complete thought or name is cited, such as a title or full quotation. When quotation marks are used, instead of a bold or italic typeface, to highlight a word or phrase, punctuation should appear outside of the quotation marks. A parenthetical phrase or statement at the end of a sentence is punctuated outside of the closing parenthesis (like this). (A parenthetical sentence is punctuated within the parentheses.)
* A graph within a graph is an “inset”, not an “insert”. The word alternatively is preferred to the word “alternately” (unless you really mean something that alternates).
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An excellent style manual for science writers is [7].

# Conclusions

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1. Table Type Styles

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##### References

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1. G. Eason, B. Noble, and I. N. Sneddon, “On certain integrals of Lipschitz-Hankel type involving products of Bessel functions,” Phil. Trans. Roy. Soc. London, vol. A247, pp. 529–551, April 1955. *(references)*

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1. J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68–73.
2. I. S. Jacobs and C. P. Bean, “Fine particles, thin films and exchange anisotropy,” in Magnetism, vol. III, G. T. Rado and H. Suhl, Eds. New York: Academic, 1963, pp. 271–350.
3. K. Elissa, “Title of paper if known,” unpublished.
4. R. Nicole, “Title of paper with only first word capitalized,” J. Name Stand. Abbrev., in press.
5. Y. Yorozu, M. Hirano, K. Oka, and Y. Tagawa, “Electron spectroscopy studies on magneto-optical media and plastic substrate interface,” IEEE Transl. J. Magn. Japan, vol. 2, pp. 740–741, August 1987 [Digests 9th Annual Conf. Magnetics Japan, p. 301, 1982].
6. Figure 1 reference