**LAB 3**

**4-bit Counter**

* Verification plan

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Section** | **Item** | **Description** | **Testcase name** | **Owner** | **Status** |
| 1 | Reset | Khi rst\_ni = 0 ouput bằng 0, khi rst\_ni =1, output sẽ được cập nhật ở cạnh lên xung clock, đếm lên nếu sel\_i = 1, đếm xuống nếu sel\_i = 0. | cnt\_rst\_test | Tâm | PASS |
| 2 | Max count | Khi output là 4’b1111 và sel\_i = 1 thì ở cạnh lên xung clock tiếp theo output sẽ là 4’0000 | cnt\_max\_test | Tâm | PASS |
| 3 | Min count | Khi output là 4’b0000 và sel\_i = 0 thì ở cạnh lên xung clock tiếp theo output sẽ là 4’b1111 | cnt\_min\_test | Tâm | PASS |
| 4 | Count up | Khi rst\_ni = 1 và sel\_i = 1, output sẽ tăng thêm 1 ở mỗi cạnh lên xung clock | cnt\_up\_test | Tâm | PASS |
| 5 | Count down | Khi rst\_ni = 1 và sel\_i = 0, output sẽ giảm 1 ở mỗi cạnh lên xung clock | cnt\_down\_test | Tâm | PASS |

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal** | **Width** | **Type** | **Description** |
| clk | 1 | Input | Clock signal |
| rst\_n | 1 | Input | Negative edge reset. If rst\_n = 0, output will be set to 0. Else, it will start the nomal operation. |
| sel | 1 | Input | Mode selection signal. If sel = 1, the design will start counting up. Else, it will start counting down from current output value. |
| out | 4 | output | Result of the counter |

Table 1: Port definitions

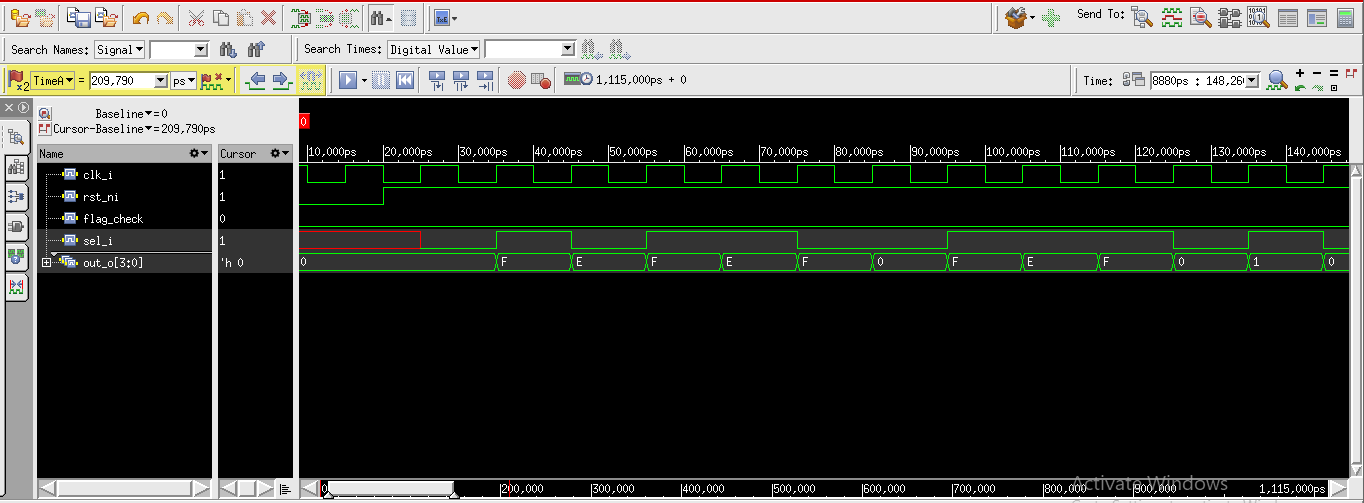


Figure 1.1: Waveform of 4bit-counter

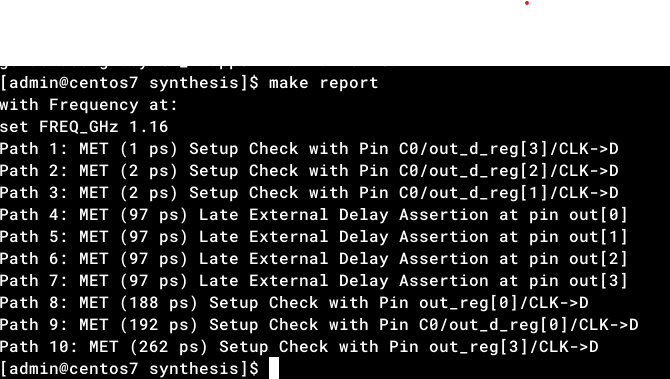


Figure 1.2: Highest frequency and timing report of the synthesized design

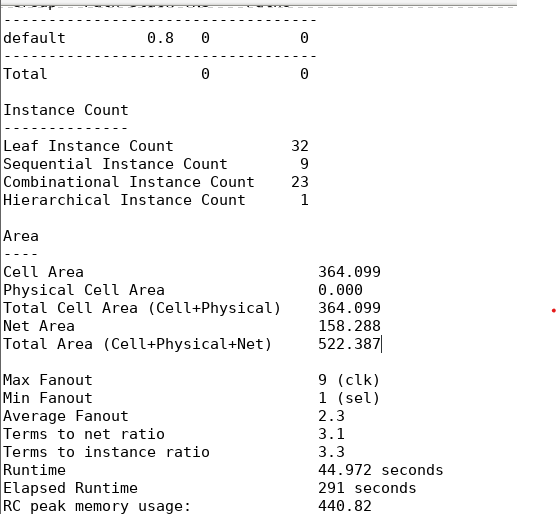


Figure 1.3: Total are used in the design

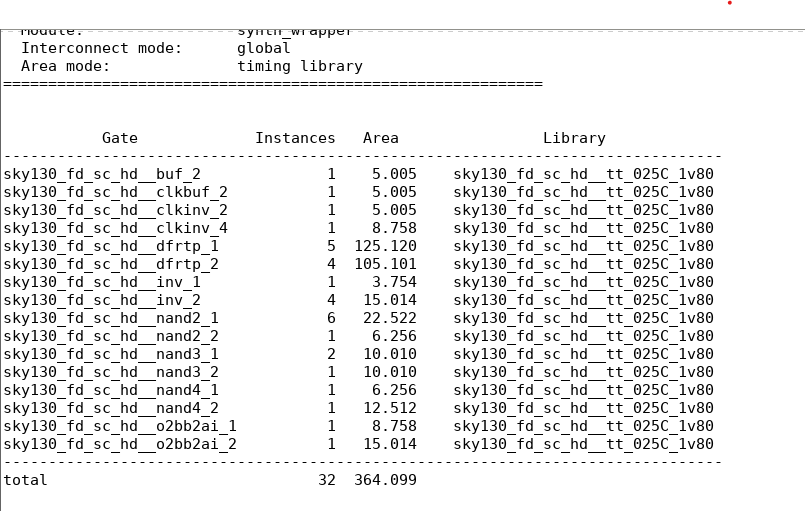


Figure 1.4: Gates resources used in the design

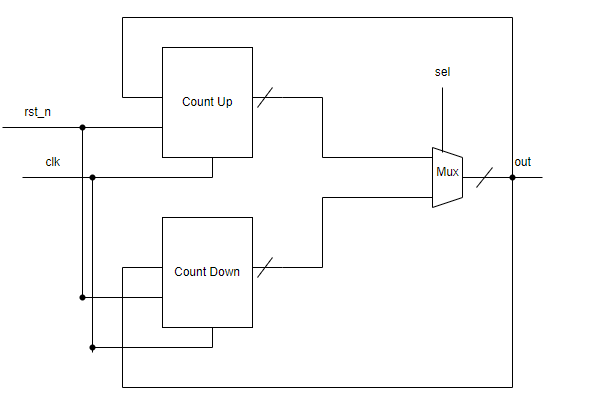


Figure 1.5: Block diagram of counter 4 bit

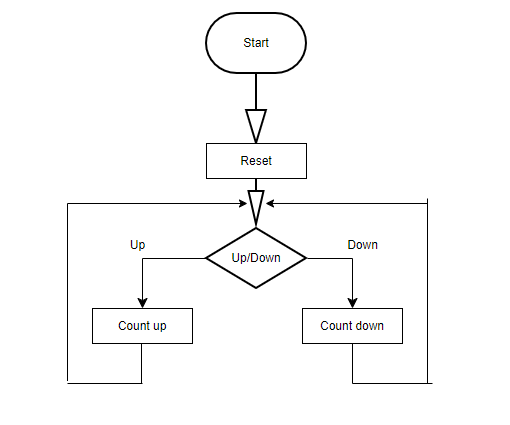


Figure 1.6: Flow chart of counter 4 bit

**ALU**

* Verification plan

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Section** | **Item** | **Description** | **Testcase name** | **Owner** | **Status** |
| 1 | Reset | Khi rst\_ni = 0 ouput bằng 0, khi rst\_ni =1, output sẽ được cập nhật ở cạnh lên xung clock. | alu\_rst\_test | Tâm | PASS |
| 2 | Sum | Khi rst\_ni = 1 và op\_i = 3’000, result\_o = a\_i + b\_i, carry\_o là cờ tràn khi a\_i + b\_i lớn hơn 15 | sum\_test | Tâm | PASS |
| 3 | Subtract | Khi rst\_ni = 1 và op\_i = 3’001, result\_o = a\_i - b\_i, carry\_o là cờ tràn khi a\_i bé hơn b\_i. | sub\_test | Tâm | PASS |
| 4 | And | Khi rst\_ni = 1 và op\_i = 3’010, result\_o = a\_i & b\_i, carry\_o bằng 0. | and\_test | Tâm | PASS |
| 5 | Or | Khi rst\_ni = 1 và op\_i = 3’011, result\_o = a\_i | b\_i, carry\_o bằng 0. | or\_test | Tâm | PASS |
| 6 | Xor | Khi rst\_ni = 1 và op\_i = 3’100, result\_o = a\_i ^ b\_i, carry\_o bằng 0. | xor\_test | Tâm | PASS |
| 7 | Not | Khi rst\_ni = 1 và op\_i = 3’101, result\_o = ~a\_i, carry\_o bằng 0. | not\_test | Tâm | PASS |
| 8 | Shift right | Khi rst\_ni = 1 và op\_i = 3’110, result\_o = a\_i >> b\_i, carry\_o bằng 0, khi b\_i > 3 thì result\_o = 0. | Shift\_right\_test | Tâm | PASS |
| 9 | Shift left | Khi rst\_ni = 1 và op\_i = 3’111, result\_o = a\_i << b\_i, carry\_o bằng 0, khi b\_i > 3 thì result\_o = 0. | Shift\_left\_test | Tâm | PASS |

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal** | **Width** | **Type** | **Desciption** |
| clk | 1 | Input | Clock signal |
| rst\_n | 1 | Input | Negative edge reset. If rst\_n = 0, result and carry will be set to 0. Else the design will work normally based on the input arguments. |
| a | 4 | Input | First argument. |
| b | 4 | Input | Second argument. |
| op | 3 | Input | Select the operation. |
| result | 4 | Output | Result of ALU. |
| carry | 1 | Output | Carry flag. |

Table 2: Port definitions

|  |  |
| --- | --- |
| **Operation (Op)** | **Description** |
| 3’b000 | {carry, result} = a + b |
| 3’b001 | {carry, result} = a - b |
| 3’b010 | carry = 0; result = and(a, b) |
| 3’b011 | carry = 0; result = or(a, b) |
| 3’b100 | carry = 0; result = xor(a, b) |
| 3’b101 | carry = 0; result = not(a) |
| 3’b110 | carry = 0; result = a >> b |
| 3’b111 | carry = 0; result = a << b |

Table 3: Functional description

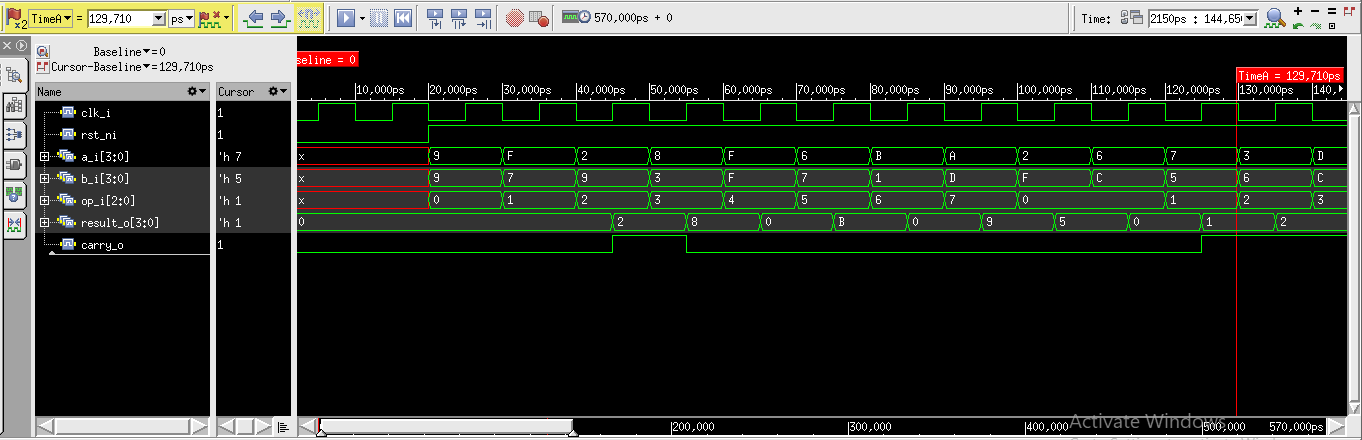


Figure 2.1: Waveform of ALU

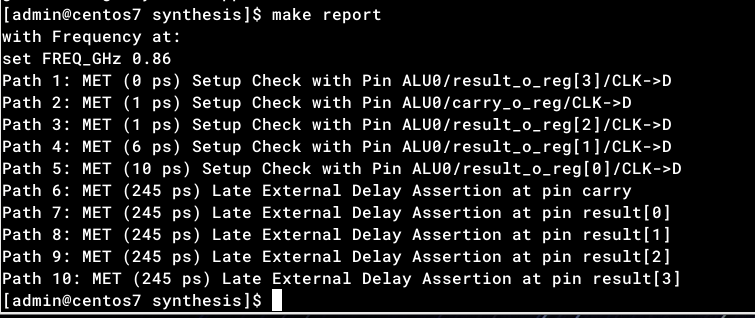


Figure 2.2: Highest frequency and timing report of the synthesized design

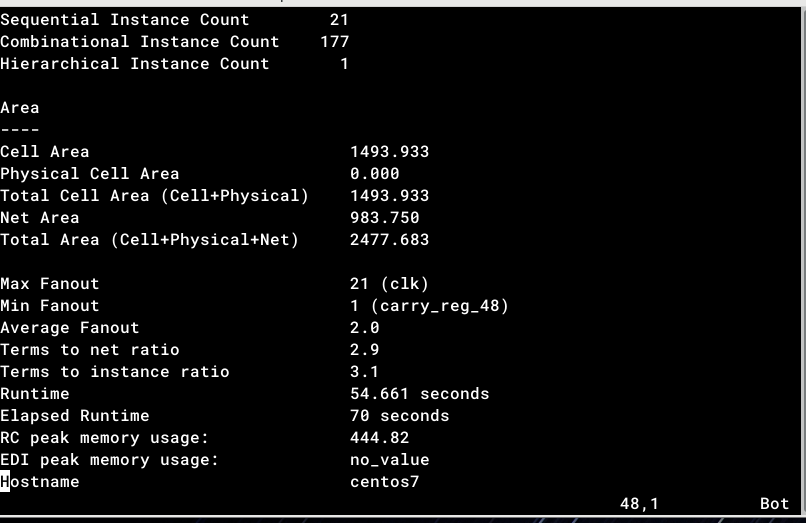


Figure 2.3: Total area used in the design

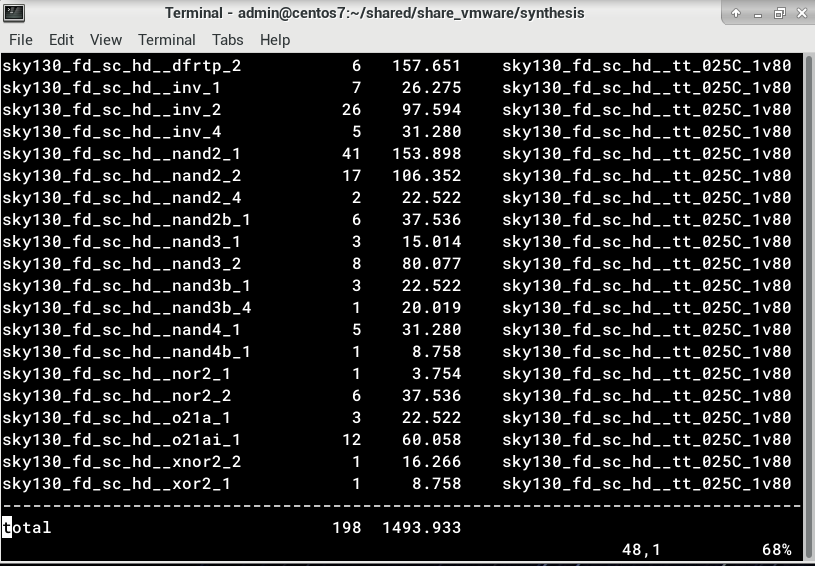


Figure 2.4: Gates resources used in the design

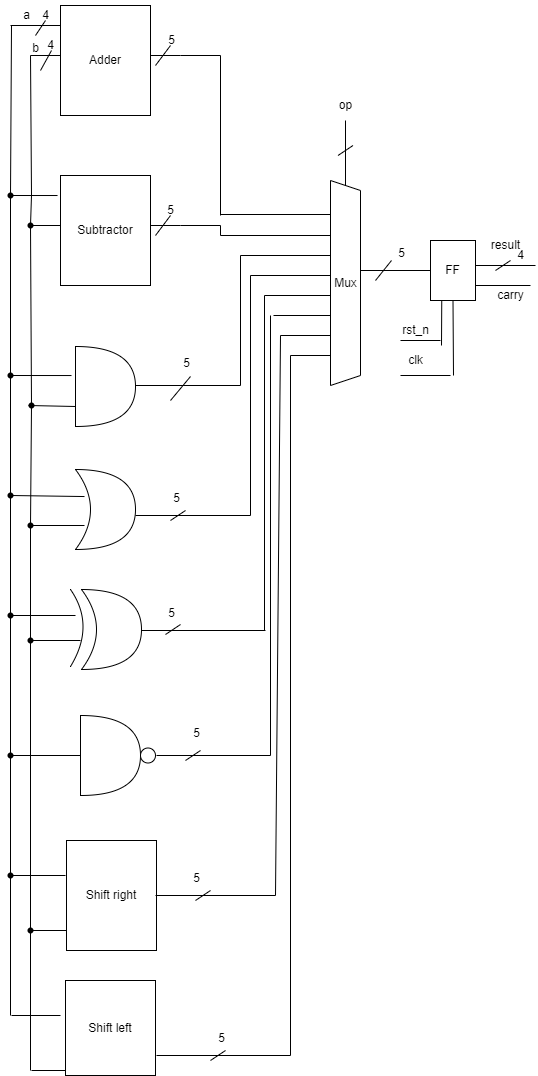


Figure 2.5: Block diagram of ALU