Question 1. (4)

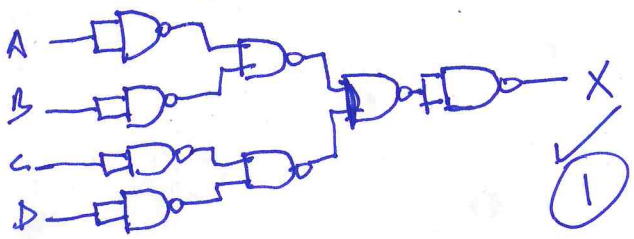
a) Gates that can be used to implement any logic function by themselves ✓(1)

b). $X = (A+B)(C+D)$.

i) NAND gates only.

$$X = \overline{(A+B)(C+D)} = \overline{A+B} + \overline{C+D} = \overline{A}\cdot\overline{B}\cdot\overline{C}\overline{D}$$

✓(1) ✓(1)

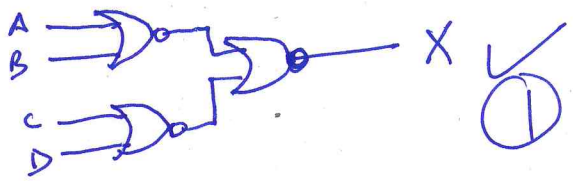


✓(1)

ii) NOR Gates only.

$$X = \overline{\overline{(A+B)(C+D)}} = \overline{(\overline{A+B}) + (\overline{C+D})}$$

✓(1) ✓(1)



✓(1)

c) $\bar{A}\bar{B}C + \overline{(A+B+\bar{C})} + \bar{A}\bar{B}\bar{C}D = \bar{A}\bar{B}(C+\bar{C}D) + \bar{A}\bar{B}C$ ✓(1)

$= \bar{A}\bar{B}(C+D+C)$. ✓(1)

$= \bar{A}\bar{B}C + \bar{A}\bar{B}D$. ✓(1)

d) i) $-10V \Rightarrow 1111111111111111_2$ ✓(½)

$10V \Rightarrow 0111111111111111_2$ ✓(½)

ii) $-32767 \Rightarrow (2^{15}-1)$ ✓(1)

$32767 \Rightarrow (2^{15}-1)$ ✓(1)

sign + magnitude

iii) The number is out of 16-bit range. No representation. ✓(1)

Question 1:

e) $X = AB + CD + EF$ ✓

Rule 1: $AB = 1$, $X = 1$ ✓

Rule 2: $AB = EF = 1$, $X = 1$ ✓ $\frac{1}{2} \times 4$

Rule 3: $EF = 1$, $X = 1$ ✓

Therefore, all three output pulses are correct.

f)

$$\begin{array}{r} 1001 \\ +\ 0011 \\ \hline 1100 \end{array}$$ ✓ (1)

→ no carry, convert to 2's complement & add sign bit

10100 ✓ (1)

g) - Analog processing is generally faster (speed). ✓

- Noise limited resolution (~~low~~ in low noise circuits, resolution high) ✓

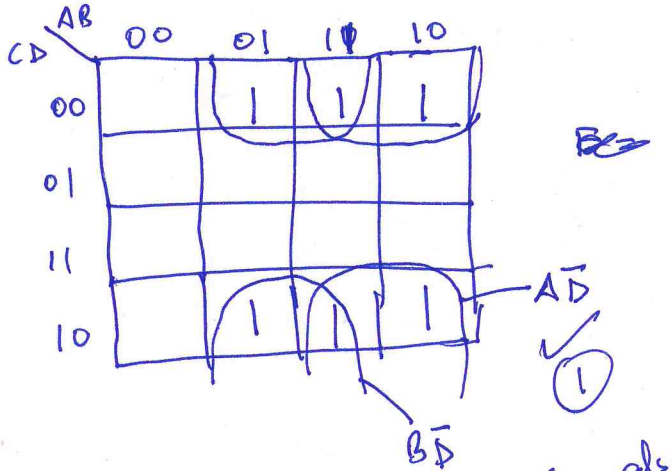
any 1 or related

h) - Fewer inputs. (advantage) ✓ (1)

- More complicated processing circuits, increased susceptibility to noise (disadvantage). ✓ (1)

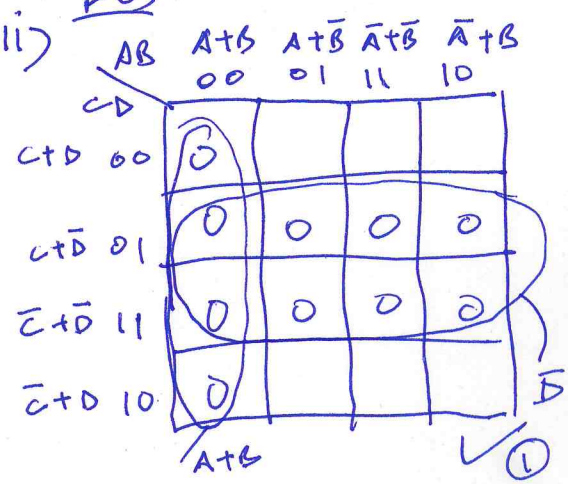
i)

i) SOP



$F = A\bar{D} + B\bar{D}$ ✓ (1)

ii) POS



✓ (1)

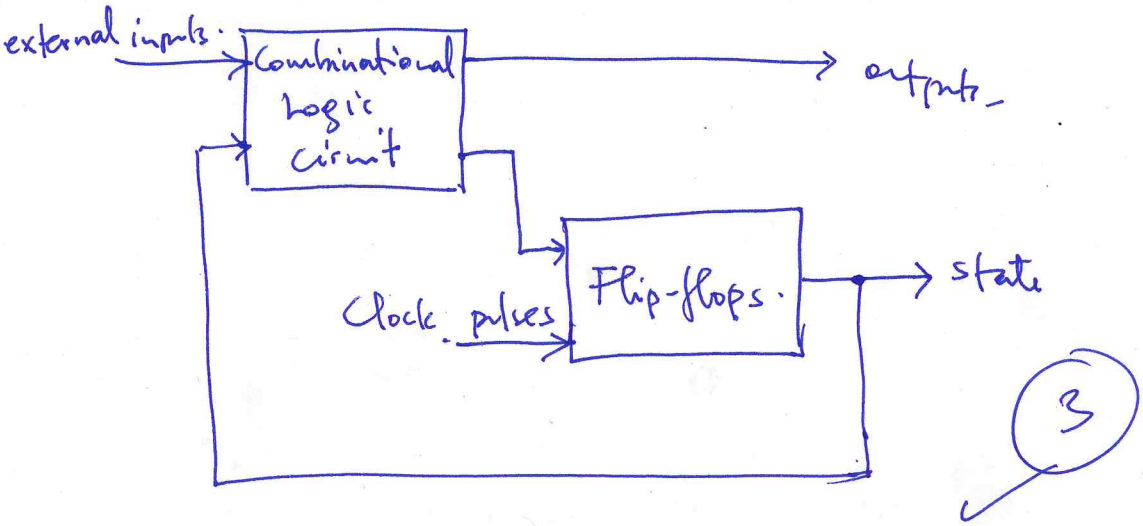
also, one can write ⇒ $F = \bar{D}(A+B)$ ✓ (1)

Question 1

j) bistable – 2 stable states ✓
monostable – 1 stable state ✓
Astable – Oscillator, no stable state ✓

1 mark (all correct)
½ mark (missing 1)

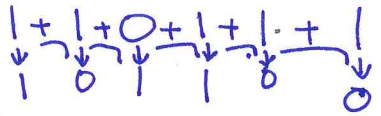
k)



3

Sequential logic circuits are circuits whose outputs are functions of present as well as previous ~~outputs~~ inputs. ✓ (1)

l) 110111_2 to Gray code.



✓ (2)

∴ 110111_2 is ~~1001~~ 101100_2 in Gray code.

Any correct conversion is ok.

m) – Frequency division
– timing
– Waveform synthesis
– triggering.
– many other valid answers.

✓ (1) any valid answer.

Question 2

a) – even parity ✓①
– counts odd number of 1's to add a 1. ✓①

b) – Summing 3 bits, discarding carry

$\therefore P_j = A \oplus B \oplus C$ ✓① where A, B and C represent appropriate bits.

$\therefore P_j = \bar{A}(B \oplus C) + A(\overline{B \oplus C})$ ✓①

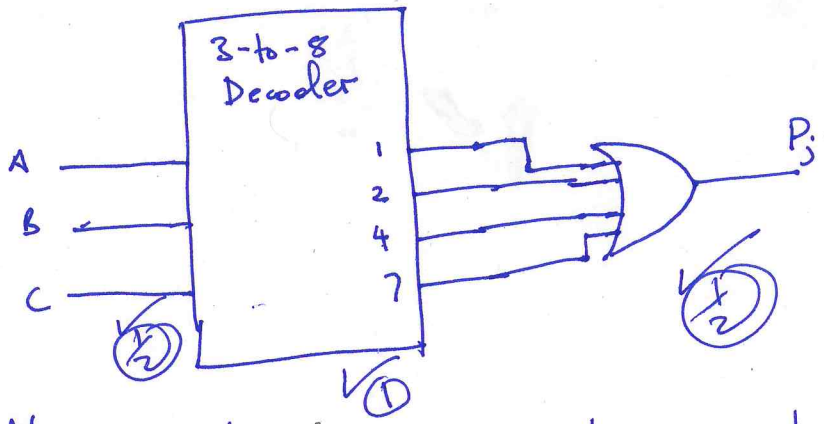
$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$ ✓①

$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$ ✓①

001 010 100 111

1 2 4 7.

or use a truth table.



c)

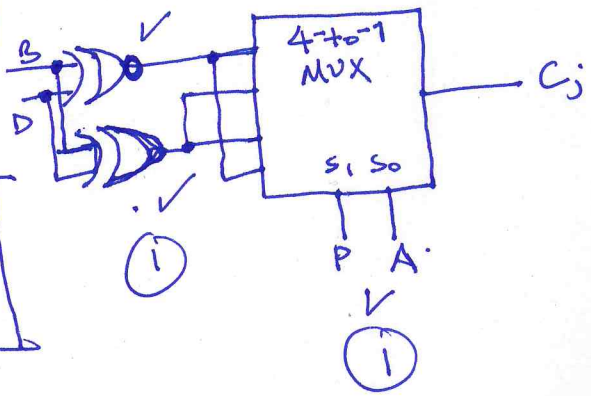
Truth table

P	A	B	D	C_j	F(D)	F(B,D)
0	0	0	0	1	$\bar{D}$	$\bar{B}\bar{D} + BD = \overline{D \oplus B}$
0	0	0	1	0		
0	0	1	0	0	D	
0	0	1	1	1		
0	1	0	0	0	D	$\bar{B}D + B\bar{D} = D \oplus B$
0	1	0	1	1		
0	1	1	0	1	$\bar{D}$	
0	1	1	1	0		
1	0	0	0	0	D	$\bar{B}D + B\bar{D} = D \oplus B$
1	0	0	1	1		
1	0	1	0	1	$\bar{D}$	
1	0	1	1	0		
1	1	0	0	1	$\bar{D}$	$\bar{B}\bar{D} + BD = \overline{D \oplus B}$
1	1	0	1	0		
1	1	1	0	0	D	
1	1	1	1	1		

✓② ✓② ②

Implementation:

Select: P, A.



Question 2 (3)

	P	A	B	D	$B \oplus D$	$\overline{B \oplus D}$	C_2
$\therefore C_2$	1	0	0	1	1	0	1
C_1	0	1	0	1	1	0	1
C_0	1	1	0	1	1	0	0

(from MUX circuit).

select $\overline{B \oplus D}$

selects $B \oplus D$

$\therefore C_2 C_1 C_0 = 110$, bit error at position 6.

Correct transmitted code: 0011001

Question 3

a). i)

S_1	S_0	SO_1	SO_2	SO_3	SO_4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	0	0	0	0	1

✓ (2)

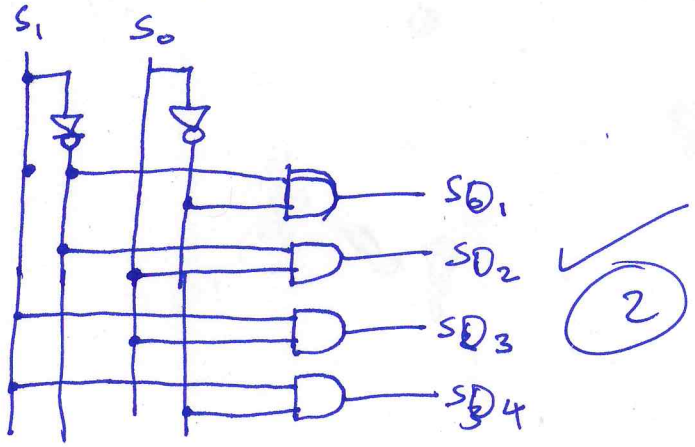
$\therefore SO_1 = \bar{S}_1 \bar{S}_0$

$SO_2 = \bar{S}_1 S_0$

$SO_3 = S_1 S_0$

$SO_4 = S_1 \bar{S}_0$

✓ (2)



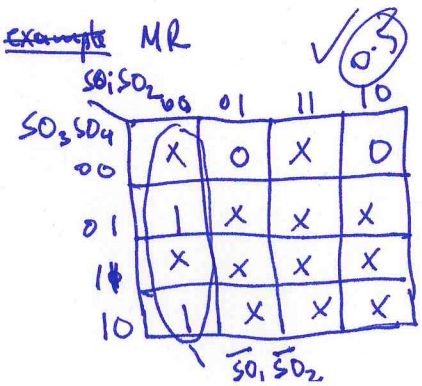
✓ (2)

ii)

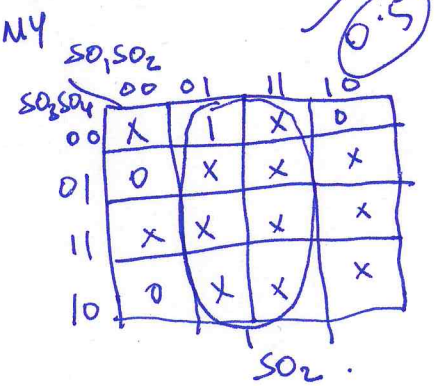
SO_1	SO_2	SO_3	SO_4	MR	MY	MG	NR	SY	SG
1	0	0	0	0	0	1	1	0	0
0	1	0	0	0	1	0	1	0	0
0	0	1	0	1	0	0	0	0	1
0	0	0	1	1	0	0	0	1	0
All other combinations are invalid.				x	x	x	x	x	x

✓ (2)

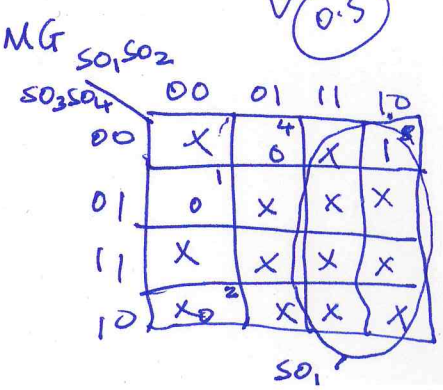
example MR ✓ (0.5)



MY ✓ (0.5)



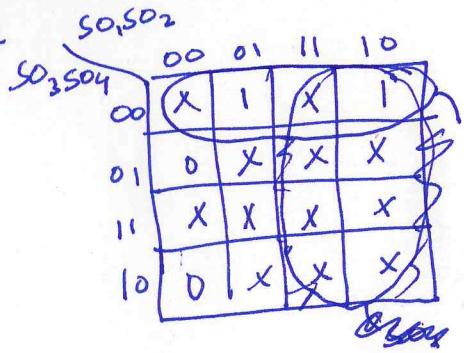
MG ✓ (0.5)



Question 3

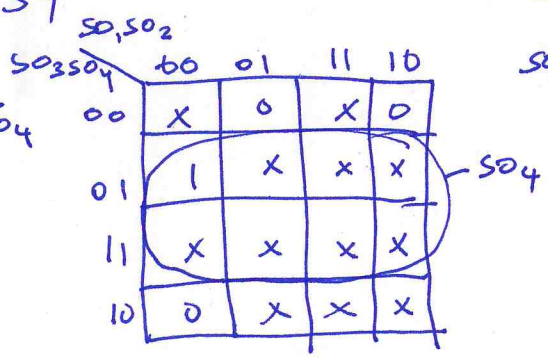
(2)

SR



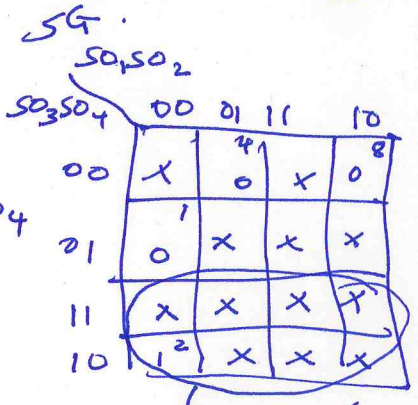
✓ 0.5

SY

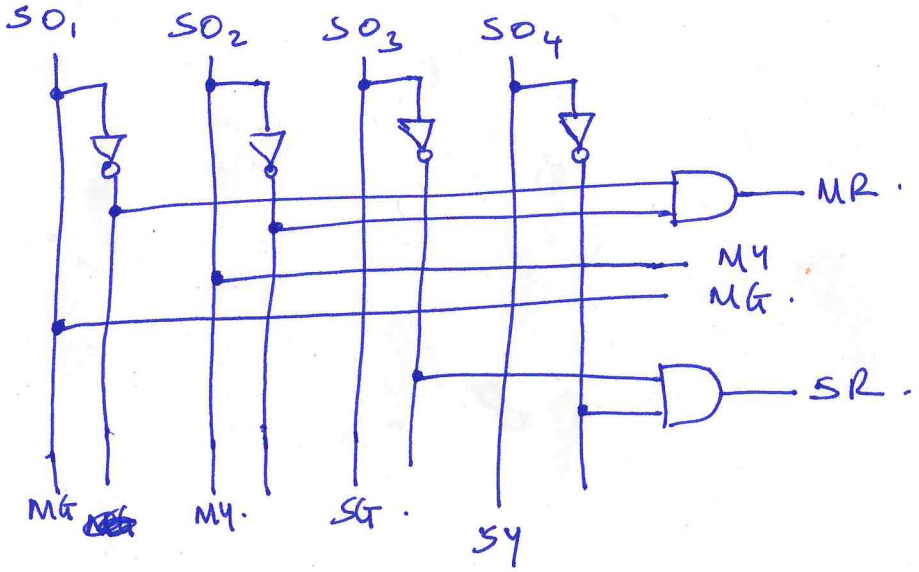


✓ 0.5

SG.



✓ 0.5



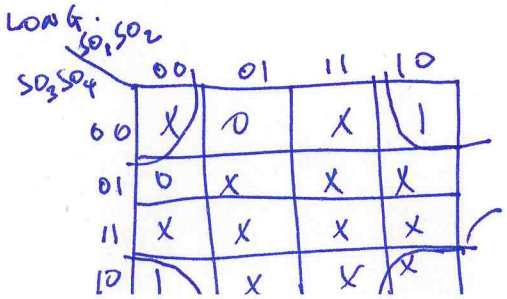
✓ (2)

iii) · Inputs: SO_1, SO_2, SO_3, SO_4.
Outputs: LONG, SHORT.

SO_1	SO_2	SO_3	SO_4	LONG	SHORT.
1	0	0	0	1	0
0	1	0	0	0	1
0	0	0	0	1	0
0	0	0	1	0	1
All other states invalid				X	X

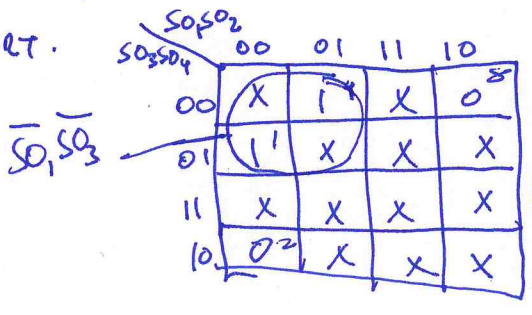
1

LONG.



✓ 1/2

SHORT.

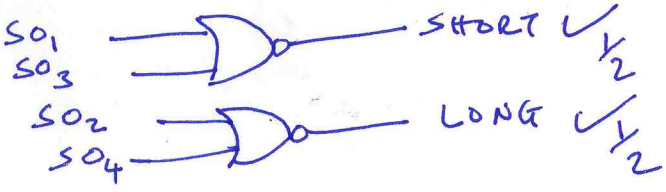


✓ 1/2

Question 3

$SHORT = \overline{S_0}\,\overline{S_3} = \overline{S_0 + S_3}$ ✓½

$LONG = \overline{S_2}\,\overline{S_4} = \overline{S_2 + S_4}$ ✓½



b). Level triggering – triggering when the clock pulse is level. (high or low). ✓ (1)

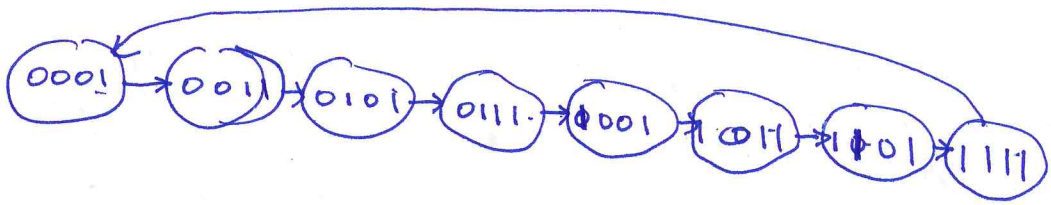
Edge triggering – triggering when the clock pulse is transitioning from high to low (~~pos~~ negative edge) or low to high ✓ (positive edge). (1)

Question 4

a) Synchronous counters – each flip-flop driven by the clock signal ✓ (1)

asynchronous counter – One of the two flip-flops is driven by the clock pulse while the others are controlled by outputs from preceeding flip flops or other inputs ✓ (1)

b). State diagram.



✓ (2)

State table

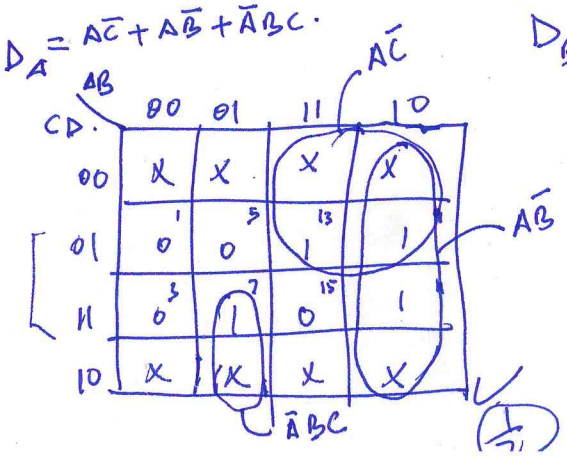
Present A	B	C	D	Next A^+	B^+	C^+	D^+	Flip-flop excitation D_A	D_B	D_C	D_D
0	0	0	1	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	1	1	0	1	1
1	0	1	1	1	1	0	1	1	1	0	1
1	1	0	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	0	1	0	0	0	1

✓ (4)

All other states are invalid

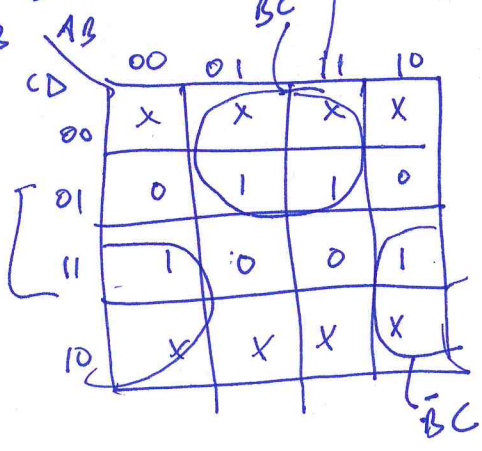
✓ (½) $D_D = 1$

$D_A = A\bar{C} + A\bar{B} + \bar{A}BC$



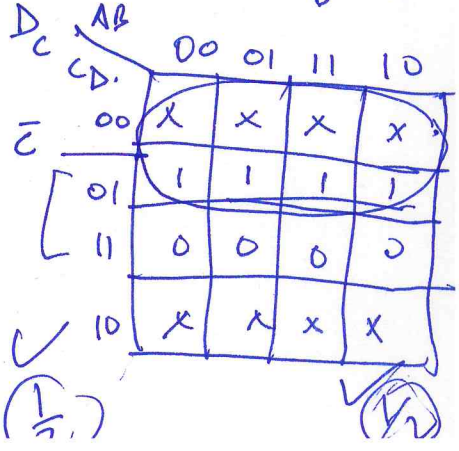
✓ (1½)

$D_B = \bar{B}C + B\bar{C}$



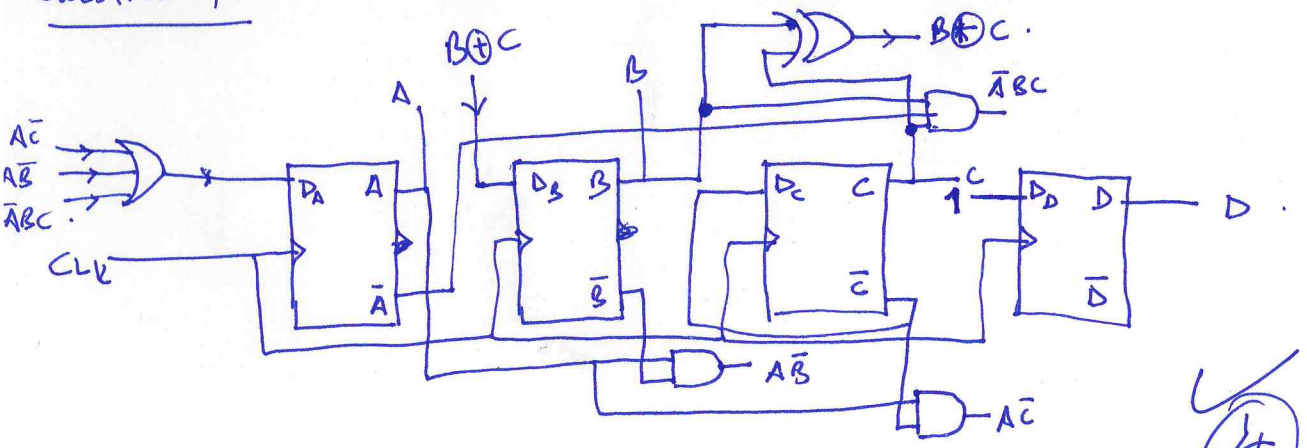
✓ (1½)

$D_C = \bar{C}$



✓ (½)

Question 4



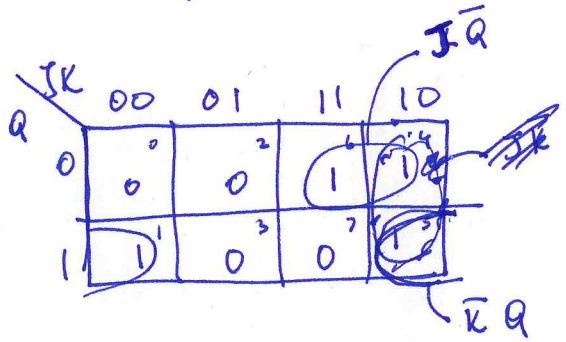
4

c). JK flip-flop using A D flip-flop.

Required Function			Flip-flop Used.
J	K	Q_n	Q_{n+1}	D.
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

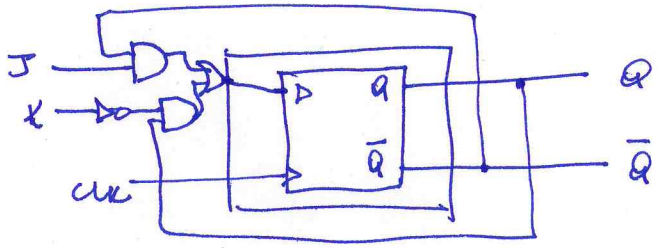
3

D



$D = \bar{K}Q + J\bar{Q}$

1



2