Model Solutions
EEE 3104 / ETI 3104 CAT II

Question 1

a) Flip-flops – can be synchronized using a clock
latches – cannot be synchronized using a clock.

b) sequential circuits – outputs functions of current & past inputs.
Combinational logic circuits – outputs functions of current inputs only.

c) Level triggering – triggering using logic level 1 or 0
Edge triggering – triggering using ~~clock~~ transitions

Question 2

– Design has to cater for changes in circuit state in the duration of the triggering level, before the next ~~clock~~ trigger comes.

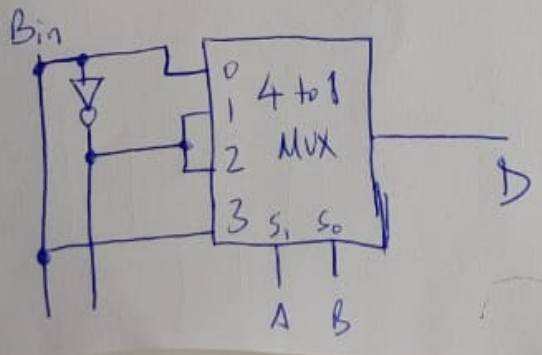
Question 3

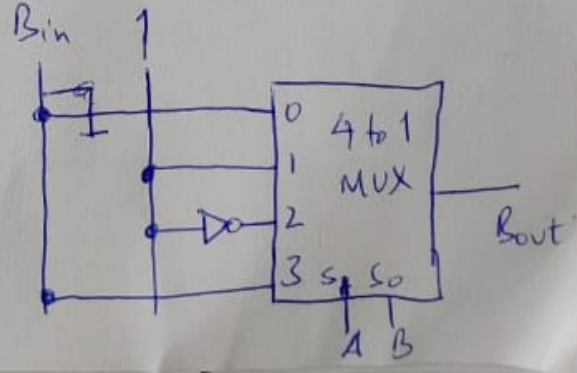
Truth Table

Partitioning.

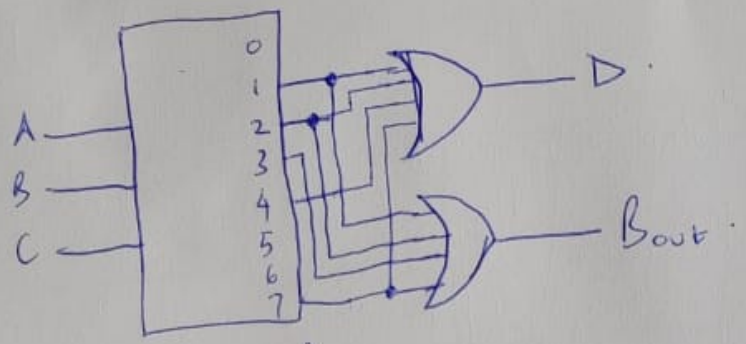
A	B	Bin	D	Bout	D(Bin)	Bout(Bin)
0	0	0	0	0		
0	0	1	1	1	Bin	Bin
0	1	0	1	1		
0	1	1	0	1	$\overline{Bin}$	1
1	0	0	1	0		
1	0	1	0	0	$\overline{Bin}$	0
1	1	0	0	0		
1	1	1	1	1	Bin	Bin.

a) 4 to 1 Mux implementation.





b) 3 to 8 decoder required (8 combinations).



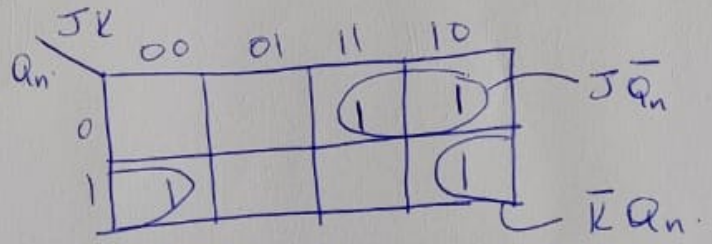
3 to 8 Decoder

Question 4.

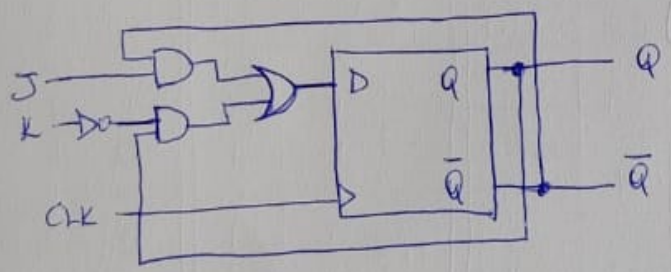
Truth table.

J	K	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

D

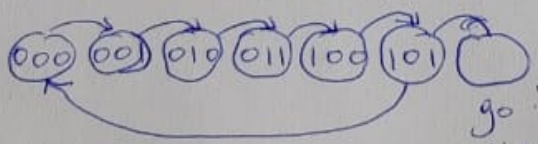


$\therefore$



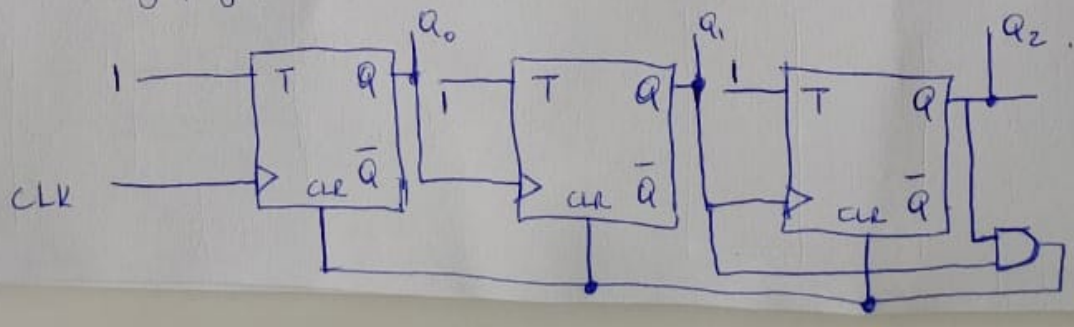
Question 5.

Case I) 0–5 – States



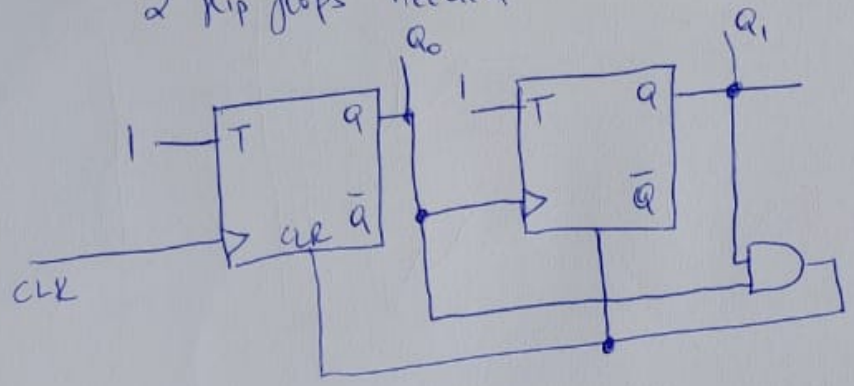
go back to 0 when you detect 110 (~~bit~~ upper 2 bits all 1's)

– Need 3 flip-flops.



(case 2) 0–2) States: 00 → 01 → 10 goes back to 0 when 11 appears

2 flip flops needed.



Question 6.

Even numbers: 10, 12

States: 1010 → 1100

Flip-flops required: 4.

Truth table:

Present state	Next state	Inputs
$Q_3\ Q_2\ Q_1\ Q_0$	$Q_3^+\ Q_2^+\ Q_1^+\ Q_0^+$	$D_3\ D_2\ D_1\ D_0$
1 0 1 0	1 1 0 0	1 1 0 0
1 1 0 0	1 0 1 0	1 0 1 0
All others	All others	x x x x

Kmap for D_3 will have 1s and Xs only $\therefore D_3 = 1$

Kmap for D_0 will have 0s and Xs only $\therefore D_0 = 0$

D_2 (Q_3Q_2 vs Q_1Q_0):

Q_1Q_0 \ Q_3Q_2	00	01	11	10
00	x	x	0	x
01	x	x	x	x
11	x	x	x	x
10	x	x	x	1

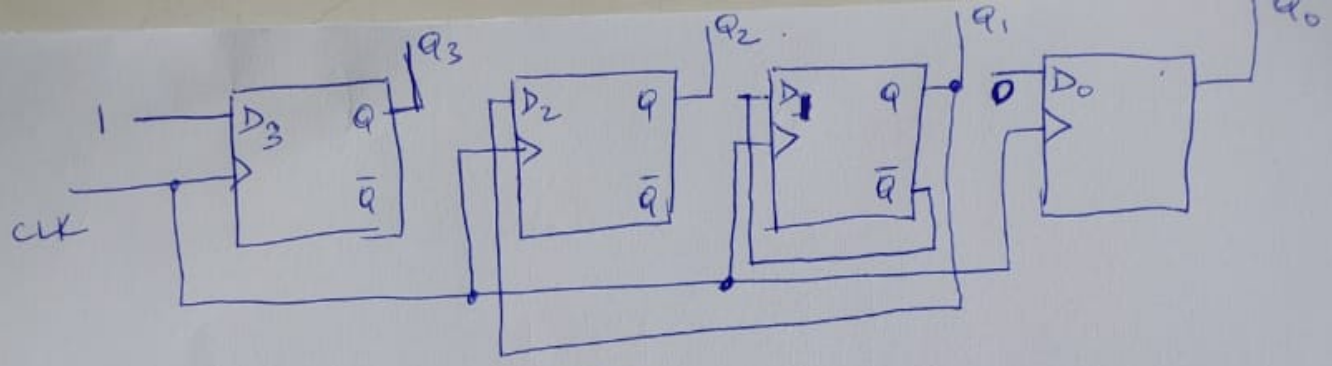
$= Q_1$

D_1 (Q_3Q_2 vs Q_1Q_0):

Q_1Q_0 \ Q_3Q_2	00	01	11	10
00	x	x	1	x
01	x	x	x	x
11	x	x	x	x
10	x	x	x	0

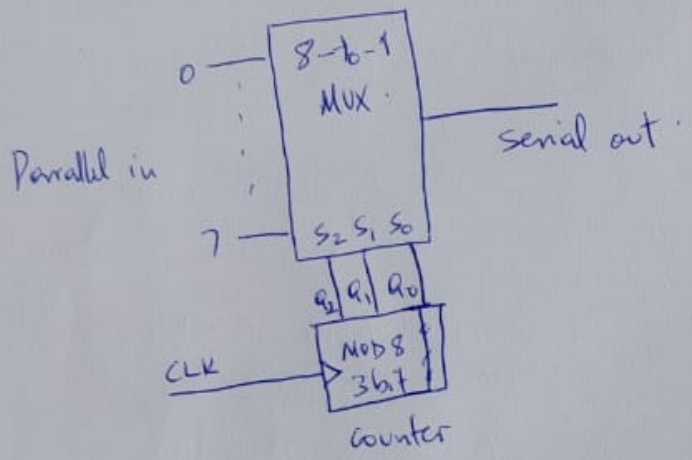
$= \bar{Q}_1$

$D_2 = Q_1$ and $D_1 = \bar{Q}_1$



Question 7.

- You can serialize outputs using clock pulses ie.



Question 8

Gray-to-binary

Truth table.

Gray G_1	Gray G_0	Binary B_1	Binary B_0
0	0	0	0
0	1	0	1
1	1	1	0
1	0	1	1

B_1

G_0 \ G_1	0	1
0	0	1
1	0	1

G_1

$B_1 = G_1$

B_0

G_0 \ G_1	0	1
0	0	1
1	1	0

$\bar{G}_0 G_1$ $G_0 \bar{G}_1$

$B_0 = G_1 \oplus G_0$