

19

Field Effect Transistors

19.1 Types of Field Effect Transistors

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INTRODUCTION

In the previous chapters, we have discussed the circuit applications of an ordinary transistor. In this type of transistor, both holes and electrons play part in the conduction process. For this reason, it is sometimes called a bipolar transistor. The ordinary or bipolar transistor has two principal disadvantages. First, it has a low input impedance because of forward biased emitter junction. Secondly, it has considerable noise level. Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few megaohms. The field effect transistor (*FET*) has, by virtue of its construction and biasing, large input impedance which may be more than 100 megaohms. The *FET* is generally much less noisy than the ordinary or bipolar transistor. The rapidly expanding *FET* market has led many semiconductor market-

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ing managers to believe that this device will soon become the most important electronic device, primarily because of its integrated-circuit applications. In this chapter, we shall focus our attention on the construction, working and circuit applications of field effect transistors.

19.1 Types of Field Effect Transistors

A bipolar junction transistor (*BJT*) is a current controlled device *i.e.*, output characteristics of the device are controlled by base current and not by base voltage. However, in a field effect transistor (*FET*), the output characteristics are controlled by input voltage (*i.e.*, electric field) and not by input current. This is probably the biggest difference between *BJT* and *FET*. There are two basic types of field effect transistors:

- (i) Junction field effect transistor (*JFET*)
- (ii) Metal oxide semiconductor field effect transistor (*MOSFET*)

19.27 Metal Oxide Semiconductor FET (MOSFET)

The main drawback of *JFET* is that its gate *must* be reverse biased for proper operation of the device *i.e.* it can only have negative gate operation for *n*-channel and positive gate operation for *p*-channel. This means that we can *only* decrease the width of the channel (*i.e.* decrease the *conductivity of the channel) from its zero-bias size. This type of operation is referred to as **depletion-mode operation. Therefore, a *JFET* can only be operated in the depletion-mode. However, there is a field effect transistor (*FET*) that can be operated to enhance (or increase) the width of the channel (with consequent increase in conductivity of the channel) *i.e.* it can have *enhancement-mode* operation. Such a *FET* is called *MOSFET*.

*A field effect transistor (FET) that can be operated in the enhancement-mode is called a **MOSFET**.*

A *MOSFET* is an important semiconductor device and can be used in any of the circuits covered for *JFET*. However, a *MOSFET* has several advantages over *JFET* including high input impedance and low cost of production.

19.28 Types of MOSFETs

There are two basic types of *MOSFETs* viz.

1. **Depletion-type MOSFET or D-MOSFET.** The *D-MOSFET* can be operated in both the depletion-mode and the enhancement-mode. For this reason, a *D-MOSFET* is sometimes called *depletion/enhancement MOSFET*.
2. **Enhancement-type MOSFET or E-MOSFET.** The *E-MOSFET* can be operated *only* in enhancement-mode.

The manner in which a *MOSFET* is constructed determines whether it is *D-MOSFET* or *E-MOSFET*.

1. D-MOSFET. Fig. 19.43 shows the constructional details of *n*-channel *D-MOSFET*. It is similar to *n*-channel *JFET* except with the following modifications/remarks :

(i) The *n*-channel *D-MOSFET* is a piece of *n*-type material with a *p*-type region (called *substrate*) on the right and an *insulated gate* on the left as shown in Fig. 19.43. The free electrons (Q if it is *n*-channel) flowing from source to drain must pass through the narrow channel between the gate and the *p*-type region (*i.e.* substrate).

(ii) Note carefully the gate construction of *D-MOSFET*. A thin layer of metal oxide (usually silicon dioxide, SiO_2) is deposited over a small portion of the channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor. One plate of this capacitor is the gate and the other plate is the channel with SiO_2 as the dielectric. Recall that we have a gate diode in a *JFET*.

(iii) It is a usual practice to connect the substrate to the source (*S*) internally so that a *MOSFET* has three terminals viz *source* (*S*), *gate* (*G*) and *drain* (*D*).

(iv) Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore, *D-MOSFET* can be operated in both depletion-mode and enhancement-mode. However, *JFET* can be operated only in depletion-mode.

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- * With the decrease in channel width, the X-sectional area of the channel decreases and hence its resistance increases. This means that conductivity of the channel will decrease. Reverse happens if channel width increases.
 - ** With gate reverse biased, the channel is depleted (*i.e.* emptied) of charge carriers (free electrons for *n*-channel and holes for *p*-channel) and hence the name depletion-mode. Note that depletion means decrease. In this mode of operation, conductivity decreases from the zero-bias level.

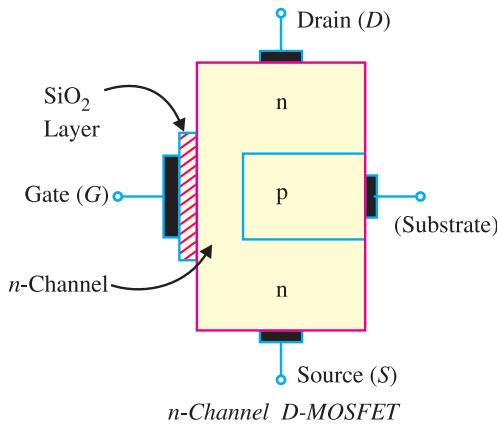


Fig. 19.43

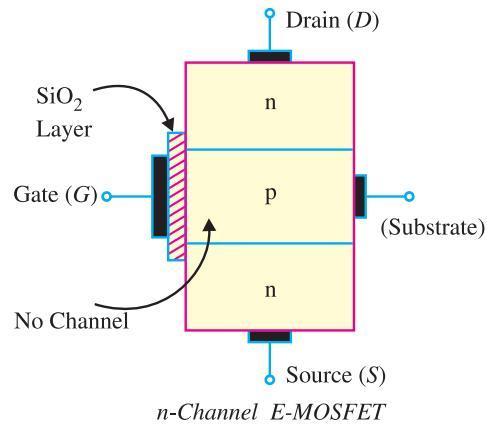


Fig. 19.44

2. E-MOSFET. Fig. 19.44 shows the constructional details of *n*-channel E-MOSFET. Its gate construction is similar to that of D-MOSFET. The E-MOSFET has no channel between source and drain unlike the D-MOSFET. Note that the substrate extends completely to the SiO_2 layer so that no channel exists. The E-MOSFET requires a proper gate voltage to *form* a channel (called induced channel). It is reminded that E-MOSFET can be operated *only* in enhancement mode. In short, the construction of E-MOSFET is quite similar to that of the D-MOSFET except for the absence of a channel between the drain and source terminals.

Why the name MOSFET? The reader may wonder why is the device called *MOSFET*? The answer is simple. The SiO_2 layer is an insulator. The gate terminal is made of a metal conductor. Thus, going from gate to substrate, you have a *metal oxide semiconductor* and hence the name *MOSFET*. Since the gate is insulated from the channel, the *MOSFET* is sometimes called *insulated-gate FET (IGFET)*. However, this term is rarely used in place of the term *MOSFET*.

19.29 Symbols for D-MOSFET

There are two types of D-MOSFETs viz (i) *n*-channel D-MOSFET and (ii) *p*-channel D-MOSFET.

(i) **n-channel D-MOSFET.** Fig. 19.45 (i) shows the various parts of *n*-channel D-MOSFET. The *p*-type substrate constricts the channel between the source and drain so that only a small passage

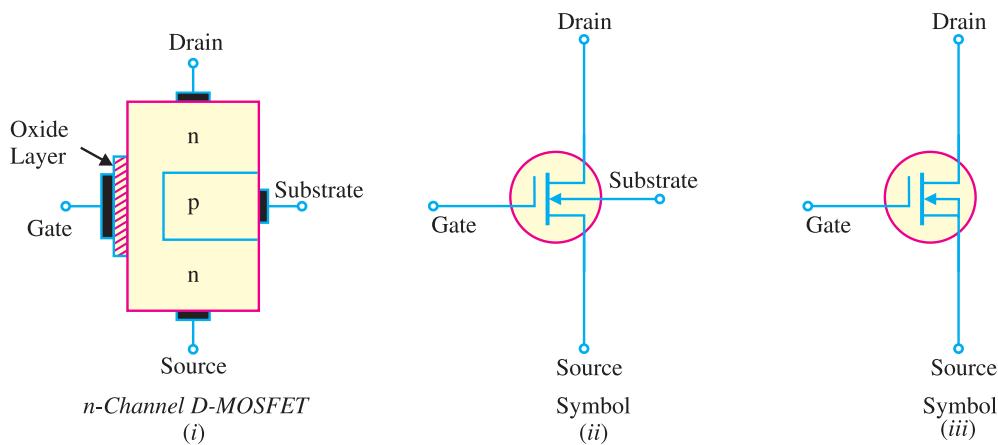


Fig. 19.45

remains at the left side. Electrons flowing from source (when drain is positive w.r.t. source) must pass through this narrow channel. The symbol for *n*-channel D-MOSFET is shown in Fig. 19.45 (ii). The gate appears like a capacitor plate. Just to the right of the gate is a thick vertical line representing the channel. The drain lead comes out of the top of the channel and the source lead connects to the bottom. The arrow is on the substrate and points to the *n*-material, therefore we have *n*-channel D-MOSFET. It is a usual practice to connect the substrate to source internally as shown in Fig. 19.45 (iii). This gives rise to a three-terminal device.

(ii) *p*-channel D-MOSFET. Fig. 19.46 (i) shows the various parts of *p*-channel D-MOSFET. The *n*-type substrate constricts the channel between the source and drain so that only a small passage remains at the left side. The conduction takes place by the flow of holes from source to drain through this narrow channel. The symbol for *p*-channel D-MOSFET is shown in Fig. 19.46 (ii). It is a usual practice to connect the substrate to source internally. This results in a three-terminal device whose schematic symbol is shown in Fig. 19.46 (iii).

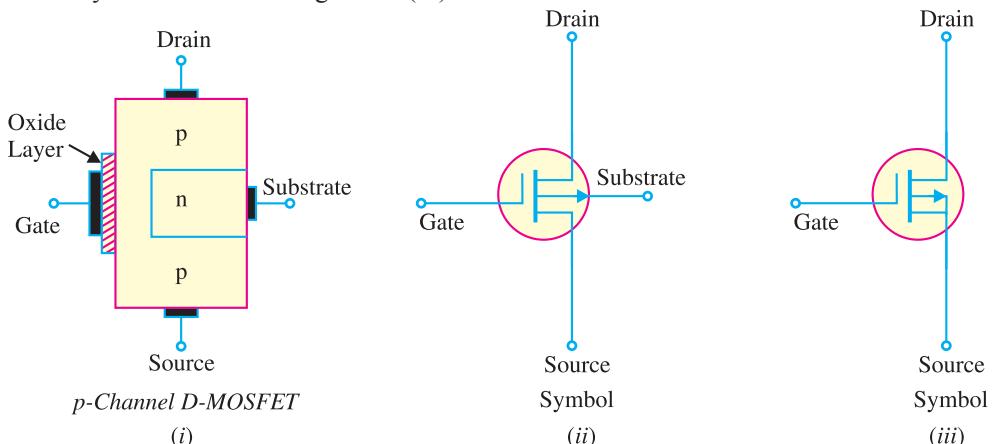


Fig. 19.46

19.30 Circuit Operation of D-MOSFET

Fig. 19.47 (i) shows the circuit of *n*-channel D-MOSFET. The gate forms a small capacitor. One plate of this capacitor is the gate and the other plate is the channel with metal oxide layer as the dielectric. When gate voltage is changed, the electric field of the capacitor changes which in turn changes the resistance of the *n*-channel. Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. The negative-gate operation is called *depletion mode* whereas positive-gate operation is known as *enhancement mode*.

(i) Depletion mode. Fig. 19.47 (i) shows depletion-mode operation of *n*-channel D-MOSFET. Since gate is negative, it means electrons are on the gate as shown in Fig. 19.47 (ii). These electrons *repel the free electrons in the *n*-channel, leaving a layer of positive ions in a part of the channel as shown in Fig. 19.47 (ii). In other words, we have depleted (*i.e.* emptied) the *n*-channel of some of its free electrons. Therefore, lesser number of free electrons are made available for current conduction through the *n*-channel. This is the same thing as if the resistance of the channel is increased. The greater the negative voltage on the gate, the lesser is the current from source to drain.

Thus by changing the negative voltage on the gate, we can vary the resistance of the *n*-channel and hence the current from source to drain. Note that with negative voltage to the gate, the action of D-MOSFET is similar to JFET. Because the action with negative gate depends upon depleting (*i.e.* emptying) the channel of free electrons, the negative-gate operation is called *depletion mode*.

* If one plate of the capacitor is negatively charged, it induces positive charge on the other plate.

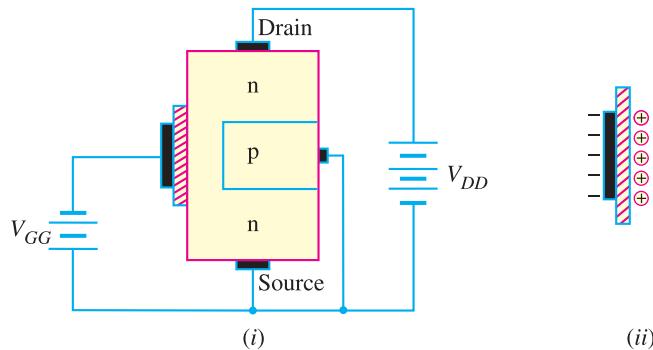


Fig. 19.47

(ii) Enhancement mode. Fig. 19.48 (i) shows enhancement-mode operation of *n*-channel *D-MOSFET*. Again, the gate acts like a capacitor. Since the gate is positive, it induces negative charges in the *n*-channel as shown in Fig. 19.48 (ii). These negative charges are the free electrons drawn into the channel. Because these free electrons are added to those already in the channel, the total number of free electrons in the channel is increased. Thus a positive gate voltage *enhances* or *increases* the conductivity of the channel. The greater the positive voltage on the gate, greater the conduction from source to drain.

Thus by changing the positive voltage on the gate, we can change the conductivity of the channel. The main difference between *D-MOSFET* and *JFET* is that we can apply positive gate voltage to *D-MOSFET* and still have essentially *zero current. Because the action with a positive gate depends upon *enhancing* the conductivity of the channel, the positive gate operation is called *enhancement mode*.

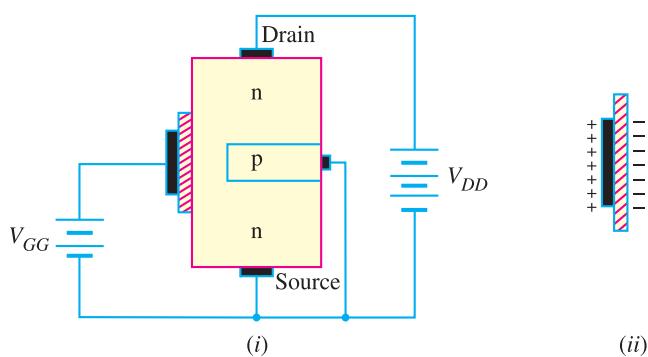


Fig. 19.48

The following points may be noted about *D-MOSFET* operation :

(i) In a *D-MOSFET*, the source to drain current is controlled by the electric field of capacitor formed at the gate.

(ii) The gate of *JFET* behaves as a reverse-biased diode whereas the gate of a *D-MOSFET* acts like a capacitor. For this reason, it is possible to operate *D-MOSFET* with positive or negative gate voltage.

(iii) As the gate of *D-MOSFET* forms a capacitor, therefore, negligible gate current flows whether

* Note that gate of *JFET* is always reverse biased for proper operation. However, in a *MOSFET*, because of the insulating layer, a negligible gate current flows whether we apply negative or positive voltage to gate.

positive or negative voltage is applied to the gate. For this reason, the input impedance of *D-MOSFET* is very high, ranging from 10,000 MΩ to 10,000,000 MΩ.

(iv) The extremely small dimensions of the oxide layer under the gate terminal result in a very low capacitance and the *D-MOSFET* has, therefore, a very low input capacitance. This characteristic makes the *D-MOSFET* useful in high-frequency applications.

19.31 D-MOSFET Transfer Characteristic

Fig. 19.49 shows the transfer characteristic curve (or transconductance curve) for *n*-channel *D-MOSFET*. The behaviour of this device can be beautifully explained with the help of this curve as under :

(i) The point on the curve where $V_{GS} = 0$, $I_D = I_{DSS}$. It is expected because I_{DSS} is the value of I_D when gate and source terminals are shorted i.e. $V_{GS} = 0$.

(ii) As V_{GS} goes *negative*, I_D decreases below the value of I_{DSS} till I_D reaches zero when $V_{GS} = V_{GS(off)}$ just as with *JFET*.

(iii) When V_{GS} is *positive*, I_D increases above the value of I_{DSS} . The maximum allowable value of I_D is given on the data sheet of *D-MOSFET*.

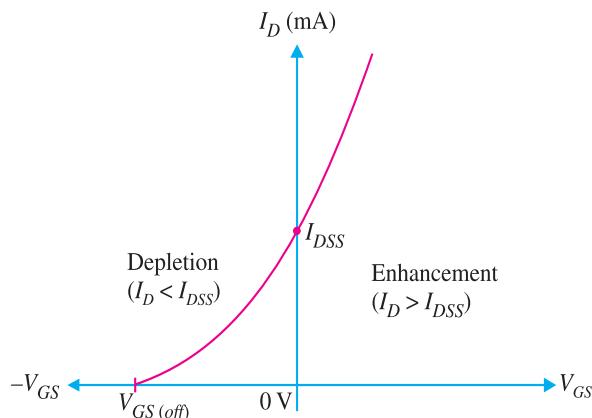


Fig. 19.49

Note that the transconductance curve for the *D-MOSFET* is very similar to the curve for a *JFET*. Because of this similarity, the *JFET* and the *D-MOSFET* have the same transconductance equation viz.

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$

Example 19.30. For a certain *D-MOSFET*, $I_{DSS} = 10 \text{ mA}$ and $V_{GS(off)} = -8 \text{ V}$.

- (i) Is this an *n-channel* or a *p-channel*?
- (ii) Calculate I_D at $V_{GS} = -3 \text{ V}$.
- (iii) Calculate I_D at $V_{GS} = +3 \text{ V}$.

Solution.

- (i) The device has a negative $V_{GS(off)}$. Therefore, it is *n-channel D-MOSFET*.

$$(ii) \quad I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$

$$= 10 \text{ mA} \left(1 - \frac{-3}{-8} \right)^2 = 3.91 \text{ mA}$$

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$$(iii) \quad I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2$$

$$= 10 \text{ mA} \left(1 - \frac{+3V}{-8V} \right)^2 = 18.9 \text{ mA}$$

Example 19.31. A D-MOSFET has parameters of $V_{GS(off)} = -6V$ and $I_{DSS} = 1 \text{ mA}$. How will you plot the transconductance curve for the device?

Solution. When $V_{GS} = 0 \text{ V}$, $I_D = I_{DSS} = 1 \text{ mA}$ and when $V_{GS} = V_{GS(off)}$, $I_D = 0 \text{ A}$. This locates two points viz I_{DSS} and $V_{GS(off)}$ on the transconductance curve. We can locate more points of the curve by *changing V_{GS} values.

$$\text{When } V_{GS} = -3V ; I_D = 1 \text{ mA} \left(1 - \frac{-3V}{-6V} \right)^2 = 0.25 \text{ mA}$$

$$\text{When } V_{GS} = -1V ; I_D = 1 \text{ mA} \left(1 - \frac{-1V}{-6V} \right)^2 = 0.694 \text{ mA}$$

$$\text{When } V_{GS} = +1V ; I_D = 1 \text{ mA} \left(1 - \frac{+1V}{-6V} \right)^2 = 1.36 \text{ mA}$$

$$\text{When } V_{GS} = +3V ; I_D = 1 \text{ mA} \left(1 - \frac{+3V}{-6V} \right)^2 = 2.25 \text{ mA}$$

Thus we have a number of V_{GS} – I_D readings so that transconductance curve for the device can be readily plotted.

19.32 Transconductance and Input Impedance of D-MOSFET

These are important parameters of a D-MOSFET and a brief discussion on them is desirable.

(i) **D-MOSFET Transconductance (g_m).** The value of g_m is found for a D-MOSFET in the same way that it is for the JFET i.e.

$$g_m = g_{mo} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)$$

(ii) **D-MOSFET Input Impedance.** The gate impedance of a D-MOSFET is extremely high. For example, a typical D-MOSFET may have a maximum gate current of 10 pA when $V_{GS} = 35V$.

$$\therefore \text{Input impedance} = \frac{35V}{10 \text{ pA}} = \frac{35V}{10 \times 10^{-12} \text{ A}} = 3.5 \times 10^{12} \Omega$$

With an input impedance in this range, D-MOSFET would present virtually no load to a source circuit.

19.33 D-MOSFET Biasing

The following methods may be used for D-MOSFET biasing :

- | | |
|----------------------------|----------------|
| (i) Gate bias | (ii) Self-bias |
| (iii) Voltage-divider bias | (iv) Zero bias |

The first three methods are exactly the same as those used for JFETs and are not discussed here. However, the last method of zero-bias is widely used in D-MOSFET circuits.

Zero bias. Since a D-MOSFET can be operated with either positive or negative values of V_{GS} , we can set its Q-point at $V_{GS} = 0V$ as shown in Fig. 19.50. Then an input a.c. signal to the gate can produce variations above and below the Q-point.

* We can only change V_{GS} because the values of I_{DSS} and $V_{GS(off)}$ are constant for a given D-MOSFET.

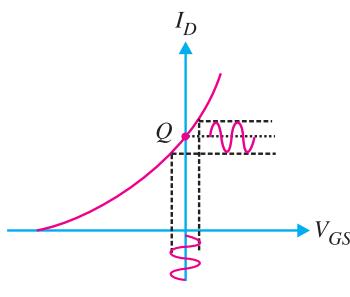


Fig. 19.50

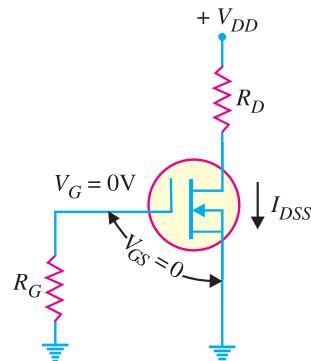


Fig. 19.51

We can use the simple circuit of Fig. 19.51 to provide zero bias. This circuit has $V_{GS} = 0V$ and $I_D = I_{DSS}$. We can find V_{DS} as under :

$$V_{DS} = V_{DD} - I_{DSS} R_D$$

Note that for the D-MOSFET zero bias circuit, the source resistor (R_S) is not necessary. With no source resistor, the value of V_S is 0V. This gives us a value of $V_{GS} = 0V$. This biases the circuit at $I_D = I_{DSS}$ and $V_{GS} = 0V$. For mid-point biasing, the value of R_D is so selected that $V_{DS} = V_{DD}/2$.

Example 19.32. Determine the drain-to-source voltage (V_{DS}) in the circuit shown in Fig. 19.51 above if $V_{DD} = +18V$ and $R_D = 620\Omega$. The MOSFET data sheet gives $V_{GS(off)} = -8V$ and $I_{DSS} = 12\text{ mA}$.

Solution. Since $I_D = I_{DSS} = 12\text{ mA}$, the V_{DS} is given by;

$$\begin{aligned} V_{DS} &= V_{DD} - I_{DSS} R_D \\ &= 18V - (12\text{ mA}) (0.62\text{ k}\Omega) = \mathbf{10.6V} \end{aligned}$$

19.34 Common-Source D-MOSFET Amplifier

Fig. 19.52 shows a common-source amplifier using *n*-channel D-MOSFET. Since the source terminal is common to the input and output terminals, the circuit is called *common-source amplifier. The circuit is zero biased with an a.c. source coupled to the gate through the coupling capacitor C_1 . The gate is at approximately 0V d.c. and the source terminal is grounded, thus making $V_{GS} = 0V$.

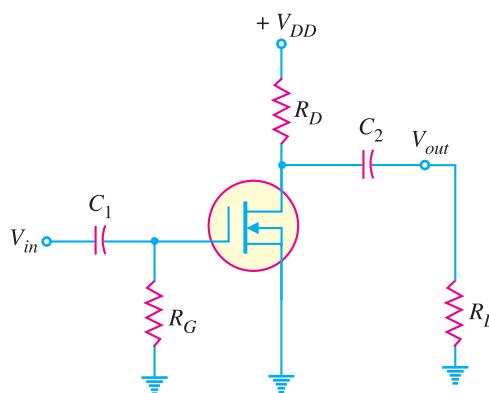


Fig. 19.52

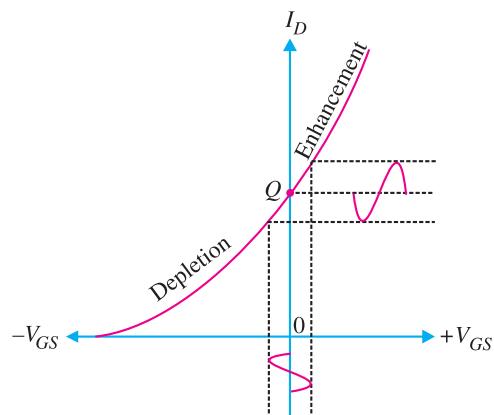


Fig. 19.53

* It is comparable to common-emitter transistor amplifier.

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Operation. The input signal (V_{in}) is capacitively coupled to the gate terminal. In the absence of the signal, d.c. value of $V_{GS} = 0V$. When signal (V_{in}) is applied, V_{gs} swings above and below its zero value (Q d.c. value of $V_{GS} = 0V$), producing a swing in drain current I_d .

(i) A small change in gate voltage produces a large change in drain current as in a *JFET*. This fact makes *MOSFET* capable of raising the strength of a weak signal; thus acting as an amplifier.

(ii) During the positive half-cycle of the signal, the positive voltage on the gate increases and produces the enhancement-mode. This increases the channel conductivity and hence the drain current.

(iii) During the negative half-cycle of the signal, the positive voltage on the gate decreases and produces depletion-mode. This decreases the conductivity and hence the drain current.

The result of above action is that a small change in gate voltage produces a large change in the drain current. This large variation in drain current produces a large a.c. output voltage across drain resistance R_D . In this way, *D-MOSFET* acts as an amplifier. Fig. 19.53 shows the amplifying action of *D-MOSFET* on transconductance curve.

Voltage gain. The a.c. analysis of *D-MOSFET* is similar to that of the *JFET*. Therefore, voltage gain expressions derived for *JFET* are also applicable to *D-MOSFET*.

$$\begin{aligned}\text{Voltage gain, } A_v &= g_m R_D && \dots \text{for unloaded D-MOSFET amplifier} \\ &= g_m R_{AC} && \dots \text{for loaded D-MOSFET amplifier}\end{aligned}$$

Note the total a.c. drain resistance $R_{AC} = R_D \parallel R_L$

Example 19.33. The *D-MOSFET* used in the amplifier of Fig. 19.54 has an $I_{DSS} = 12 \text{ mA}$ and $g_m = 3.2 \text{ mS}$. Determine (i) d.c. drain-to-source voltage V_{DS} and (ii) a.c. output voltage. Given $v_{in} = 500 \text{ mV}$.

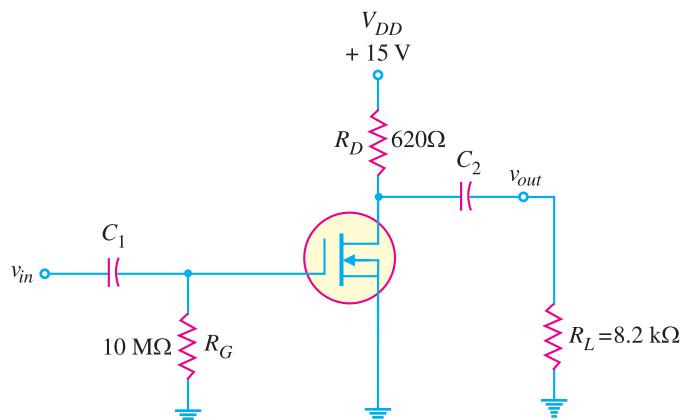


Fig. 19.54

Solution.

(i) Since the amplifier is zero biased, $I_D = I_{DSS} = 12 \text{ mA}$.

$$\begin{aligned}\therefore V_{DS} &= V_{DD} - I_{DSS} R_D \\ &= 15V - (12 \text{ mA}) (0.62 \text{ kΩ}) = 7.56 \text{ V}\end{aligned}$$

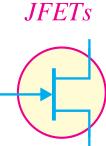
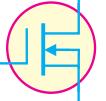
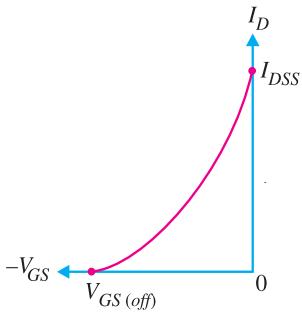
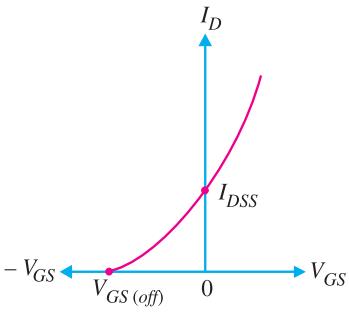
(ii) Total a.c. drain resistance R_{AC} of the circuit is

$$R_{AC} = R_D \parallel R_L = 620\Omega \parallel 8.2 \text{ kΩ} = 576\Omega$$

$$\begin{aligned}\therefore v_{out} &= A_v \times v_{in} = (g_m R_{AC}) (v_{in}) \\ &= (3.2 \times 10^{-3} \text{ S} \times 576 \text{ Ω}) (500 \text{ mV}) = 922 \text{ mV}\end{aligned}$$

19.35 D-MOSFETs Versus JFETs

Table below summarises many of the characteristics of *JFETs* and *D-MOSFETs*.

<i>Devices:</i>	<i>JFETs</i>	<i>D-MOSFETs</i>
<i>Schematic symbol:</i>		
<i>Transconductance curve:</i>		
<i>Modes of operation:</i>	Depletion only	Depletion and enhancement
<i>Commonly used bias circuits:</i>	Gate bias Self bias Voltage-divider bias	Gate bias Self bias Voltage-divider bias Zero bias
<i>Advantages:</i>	Extremely high input impedance.	Higher input impedance than a comparable <i>JFET</i> . Can operate in both modes (depletion and enhancement).
<i>Disadvantages:</i>	Bias instability. Can operate only in the depletion mode.	Bias instability. More sensitive to changes in temperature than the <i>JFET</i> .

19.36 E-MOSFET

Two things are worth noting about *E-MOSFET*. First, *E-MOSFET* operates *only* in the enhancement mode and has no depletion mode. Secondly, the *E-MOSFET* has no physical channel from source to drain because the substrate extends completely to the SiO_2 layer [See Fig. 19.55 (i)]. It is only by the application of V_{GS} (gate-to-source voltage) of proper magnitude and polarity that the device starts conducting. The minimum value of V_{GS} of proper polarity that turns on the *E-MOSFET* is called *Threshold voltage* [$V_{GS(th)}$]. The *n*-channel device requires positive $V_{GS} (\geq V_{GS(th)})$ and the *p*-channel device requires negative $V_{GS} (\geq V_{GS(th)})$.

Operation. Fig. 19.55 (i) shows the circuit of *n*-channel *E-MOSFET*. The circuit action is as under :

(i) When $V_{GS} = 0\text{V}$ [See Fig. 19.55(i)], there is no channel connecting the source and drain. The *p* substrate has only a few thermally produced free electrons (minority carriers) so that drain current is essentially zero. For this reason, *E-MOSFET* is normally *OFF* when $V_{GS} = 0\text{ V}$. Note that this behaviour of *E-MOSFET* is quite different from *JFET* or *D-MOSFET*.

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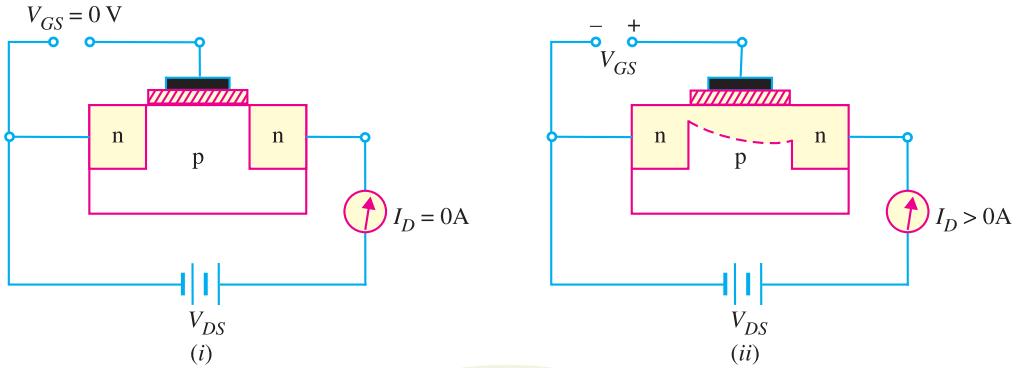


Fig. 19.55

(ii) When gate is made positive (i.e. V_{GS} is positive) as shown in Fig. 19.55 (ii), it attracts free electrons into the p region. The free electrons combine with the holes next to the SiO_2 layer. If V_{GS} is positive enough, all the holes touching the SiO_2 layer are filled and free electrons begin to flow from the source to drain. The effect is the same as creating a thin layer of n -type material (i.e. inducing a thin n -channel) adjacent to the SiO_2 layer. Thus the E -MOSFET is turned *ON* and drain current I_D starts flowing from the source to the drain.

The minimum value of V_{GS} that turns the E -MOSFET *ON* is called **threshold voltage** [$V_{GS(th)}$].

(iii) When V_{GS} is less than $V_{GS(th)}$, there is no induced channel and the drain current I_D is zero. When V_{GS} is equal to $V_{GS(th)}$, the E -MOSFET is turned *ON* and the induced channel conducts drain current from the source to the drain. Beyond $V_{GS(th)}$, if the value of V_{GS} is increased, the newly formed channel becomes wider, causing I_D to increase. If the value of V_{GS} decreases [not less than $V_{GS(th)}$], the channel becomes narrower and I_D will decrease. This fact is revealed by the transconductance curve of n -channel E -MOSFET shown in Fig. 19.56. As you can see, $I_D = 0$ when $V_{GS} = 0$. Therefore, the value of I_{DSS} for the E -MOSFET is zero. Note also that there is no drain current until V_{GS} reaches $V_{GS(th)}$.

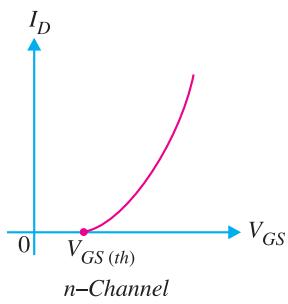


Fig. 19.56

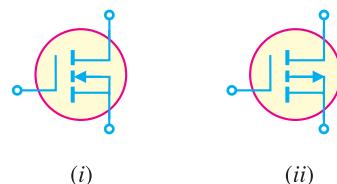


Fig. 19.57

Schematic Symbols. Fig. 19.57 (i) shows the schematic symbols for n -channel E -MOSFET whereas Fig. 19.57 (ii) shows the schematic symbol for p -channel E -MOSFET. When $V_{GS} = 0$, the E -MOSFET is *OFF* because there is no conducting channel between source and drain. The broken channel line in the symbols indicates the normally *OFF* condition.

Equation for Transconductance Curve. Fig. 19.58 shows the transconductance curve for n -channel E -MOSFET. Note that this curve is different from the transconductance curve for n -channel JFET or n -channel D-MOSFET. It is because it starts at $V_{GS(th)}$ rather than $V_{GS(off)}$ on the horizontal axis and never intersects the vertical axis. The equation for the E -MOSFET transconductance curve (for $V_{GS} > V_{GS(th)}$) is

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

The constant K depends on the particular E -MOSFET and its value is determined from the following equation :

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2}$$

Any data sheet for an E -MOSFET will include the current $I_{D(on)}$ and the voltage $V_{GS(on)}$ for one point well above the threshold voltage as shown in Fig. 19.58.

Example 19.34. The data sheet for an E -MOSFET gives $I_{D(on)} = 500 \text{ mA}$ at $V_{GS} = 10\text{V}$ and $V_{GS(th)} = 1\text{V}$. Determine the drain current for $V_{GS} = 5\text{V}$.

Solution. Here $V_{GS(on)} = 10 \text{ V}$.

$$I_D = K(V_{GS} - V_{GS(th)})^2 \quad \dots (i)$$

Here

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2} = \frac{500 \text{ mA}}{(10\text{V} - 1\text{V})^2} = 6.17 \text{ mA/V}^2$$

Putting the various values in eq. (i), we have,

$$I_D = 6.17(5\text{V} - 1\text{V})^2 = 98.7 \text{ mA}$$

Example 19.35. The data sheet for an E -MOSFET gives $I_{D(on)} = 3 \text{ mA}$ at $V_{GS} = 10\text{V}$ and $V_{GS(th)} = 3\text{V}$. Determine the resulting value of K for the device. How will you plot the transconductance curve for this MOSFET ?

Solution. The value of K can be determined from the following equation :

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2}$$

Here

$$I_{D(on)} = 3 \text{ mA} ; V_{GS(on)} = 10\text{V} ; V_{GS(th)} = 3\text{V}$$

∴

$$K = \frac{3 \text{ mA}}{(10\text{V} - 3\text{V})^2} = \frac{3 \text{ mA}}{(7\text{V})^2} = 0.061 \times 10^{-3} \text{ A/V}^2$$

Now

$$I_D = K(V_{GS} - V_{GS(th)})^2$$

In order to plot the transconductance curve for the device, we shall determine a few points for the curve by changing the value of V_{GS} and noting the corresponding values of I_D .

For $V_{GS} = 5\text{V}$; $I_D = 0.061 \times 10^{-3} (5\text{V} - 3\text{V})^2 = 0.244 \text{ mA}$

For $V_{GS} = 8\text{V}$; $I_D = 0.061 \times 10^{-3} (8\text{V} - 3\text{V})^2 = 1.525 \text{ mA}$

For $V_{GS} = 10\text{V}$; $I_D = 0.061 \times 10^{-3} (10\text{V} - 3\text{V})^2 = 3 \text{ mA}$

For $V_{GS} = 12\text{V}$; $I_D = 0.061 \times 10^{-3} (12\text{V} - 3\text{V})^2 = 4.94 \text{ mA}$

Thus we can plot the transconductance curve for the E -MOSFET from these V_{GS}/I_D points.

19.37 E-MOSFET Biasing Circuits

One of the problems with E -MOSFET is the fact that many of the biasing circuits used for $JFETs$ and D -MOSFETs cannot be used with this device. For example, E -MOSFETs must have V_{GS} greater than the threshold value ($V_{GS(th)}$) so that zero bias cannot be used. However, there are two popular methods for E -MOSFET biasing viz.

(i) Drain-feedback bias

(ii) Voltage-divider bias

(i) **Drain-feedback bias.** This method of E -MOSFET bias is equivalent to collector-feedback bias in transistors. Fig. 19.59 (i) shows the drain-feedback bias circuit for n -channel E -MOSFET. A

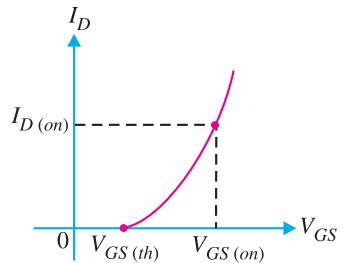


Fig. 19.58

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high resistance R_G is connected between the drain and the gate. Since the gate resistance is superhigh, no current will flow in the gate circuit (*i.e.* $I_G = 0$). Therefore, there will be no voltage drop across R_G . Since there is no voltage drop across R_G , the gate will be at the same potential as the drain. This fact is illustrated in the d.c. equivalent circuit of drain-feedback bias as in Fig. 19.59 (ii).

\therefore

$$V_D = V_G \text{ and } V_{DS} = V_{GS}$$

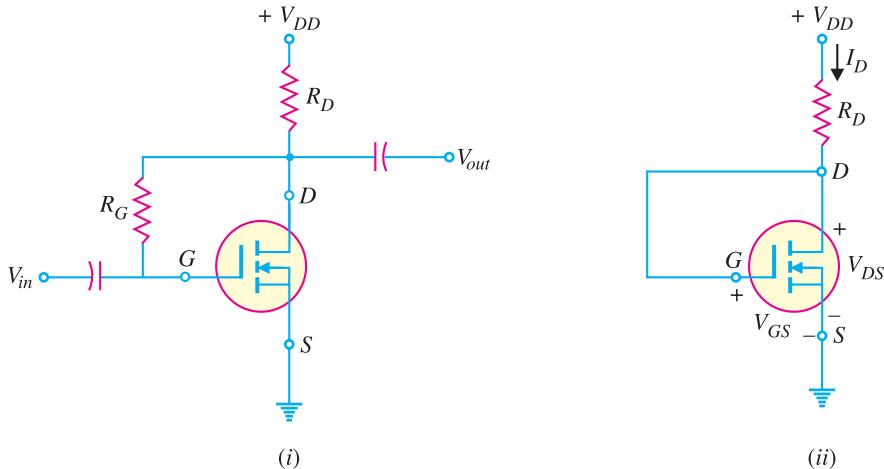


Fig. 19.59

The value of drain-source voltage V_{DS} for the drain-feedback circuit is

$$V_{DS} = V_{DD} - I_D R_D$$

$$\text{Since } V_{DS} = V_{GS}, V_{GS} = V_{DD} - I_D R_D$$

$$\text{Since in this circuit } V_{DS} = V_{GS}; I_D = I_{D(on)}$$

Therefore, the Q -point of the circuit stands determined.

(ii) Voltage-divider Bias. Fig. 19.60 shows voltage divider biasing arrangement for *n*-channel *E-MOSFET*. Since $I_G = 0$, the analysis of the method is as follows :

$$V_{GS} = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

and

$$V_{DS} = V_{DD} - I_D R_D$$

where

$$I_D = K (V_{GS} - V_{GS(th)})^2$$

Once I_D and V_{DS} are known, all the remaining quantities of the circuit such as V_D etc. can be determined.

Example 19.36. Determine V_{GS} and V_{DS} for the *E-MOSFET* circuit in Fig. 19.61. The data sheet for this particular MOSFET gives $I_{D(on)} = 500 \text{ mA}$ at $V_{GS} = 10 \text{ V}$ and $V_{GS(th)} = 1 \text{ V}$.

Solution. Referring to the circuit shown in Fig. 19.61, we have,

$$\begin{aligned} V_{GS} &= \frac{V_{DD}}{R_1 + R_2} \times R_2 \\ &= \frac{24 \text{ V}}{(100 + 15) \text{ k}\Omega} \times 15 \text{ k}\Omega = 3.13 \text{ V} \end{aligned}$$

The value of K can be determined from the following equation :

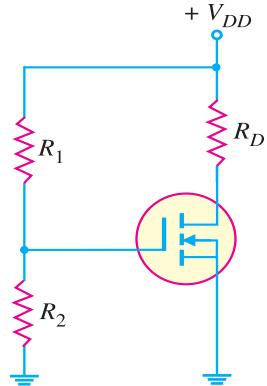


Fig. 19.60

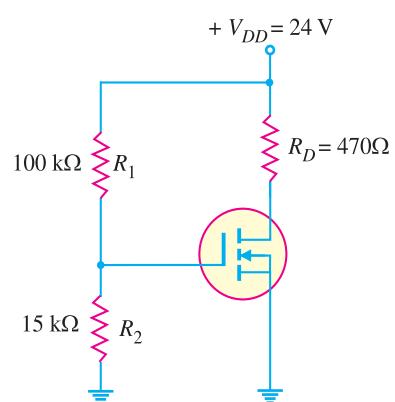


Fig. 19.61

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2}$$

$$= \frac{500 \text{ mA}}{(10\text{V} - 1\text{V})^2} = 6.17 \text{ mA/V}^2 \quad [\because V_{GS(on)} = 10\text{V}]$$

$$\therefore I_D = K(V_{GS} - V_{GS(th)})^2 = 6.17 \text{ mA/V}^2 (3.13\text{V} - 1\text{V})^2 = 28 \text{ mA}$$

$$\therefore V_{DS} = V_{DD} - I_D R_D = 24\text{V} - (28 \text{ mA})(470\Omega) = 10.8\text{V}$$

Example 19.37. Determine the values of I_D and V_{DS} for the circuit shown in Fig. 19.62. The data sheet for this particular MOSFET gives $I_{D(on)} = 10 \text{ mA}$ when $V_{GS} = V_{DS}$.

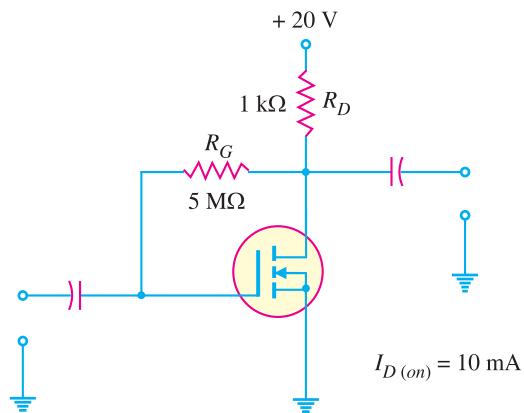


Fig. 19.62

Solution. Since in the drain-feedback circuit $V_{GS} = V_{DS}$,

$$\therefore I_D = I_{D(on)} = 10 \text{ mA}$$

The value of V_{DS} (and thus V_{GS}) is given by ;

$$V_{DS} = V_{DD} - I_D R_D$$

$$= 20\text{V} - (10 \text{ mA})(1 \text{ k}\Omega) = 20\text{V} - 10\text{V} = 10\text{V}$$

Example 19.38. Determine the value of I_D for the circuit shown in Fig. 19.63. The data sheet for this particular MOSFET gives $I_{D(on)} = 10 \text{ mA}$ at $V_{GS} = 10 \text{ V}$ and $V_{GS(th)} = 1.5 \text{ V}$.

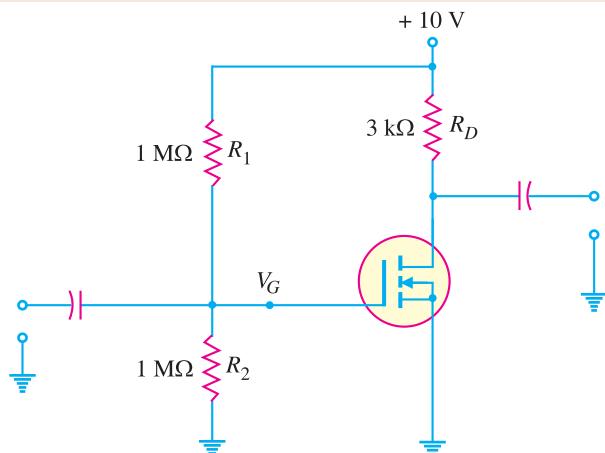


Fig. 19.63

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Solution. The value of K can be determined from the following equation :

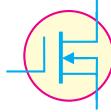
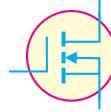
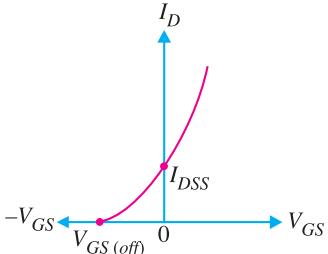
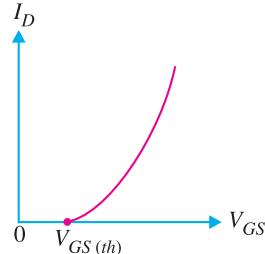
$$\begin{aligned} K &= \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(th)})^2} \\ &= \frac{10 \text{ mA}}{(10 \text{ V} - 1.5 \text{ V})^2} = 1.38 \times 10^{-1} \text{ mA/V}^2 \quad [\because V_{GS(on)} = 10 \text{ V}] \end{aligned}$$

From the circuit, the source voltage is seen to be 0V. Therefore, $V_{GS} = V_G - V_S = V_G - 0 = V_G$. The value of V_G ($= V_{GS}$) is given by ;

$$\begin{aligned} V_G \text{ (or } V_{GS}) &= \frac{V_{DD}}{R_1 + R_2} \times R_2 = \frac{10 \text{ V}}{(1+1) \text{ M}\Omega} \times 1 \text{ M}\Omega = 5 \text{ V} \\ \therefore I_D &= K(V_{GS} - V_{GS(th)})^2 \\ &= (1.38 \times 10^{-1} \text{ mA/V}^2)(5 \text{ V} - 1.5 \text{ V})^2 = 1.69 \text{ mA} \end{aligned}$$

19.38 D-MOSFETs Versus E-MOSFETs

Table below summarises many of the characteristics of *D-MOSFETs* and *E-MOSFETs*

Devices:	D-MOSFETs	E-MOSFETs
Schematic symbol:		
Transconductance curve:		
Modes of operation:	Depletion and enhancement.	Enhancement only.
Commonly used bias circuits:	Gate bias Self bias Voltage-divider bias Zero bias	Gate bias Voltage-divider bias Drain-feedback bias