



Delay Tables

- ❖ w/ AND, if other pin is 1, CLK moves. w/ OR, if other pin is 0, CLK moves
- ❖ Delay tables are used for cell timing models in lef files
- ❖ Output slew(depends on capacitive load and input slew) impacts delay majorly
- ❖ CT- process to design clock distribution network to minimize skew and ensure synchronous operation of the circuit (make sure everything happens when it should)
- ❖ Skew- variation in clock signal arrival times
- ❖ slew- rate of change of signal's voltage on time
- ❖ Latency -delay experienced by the clock signal

```

NFO]: Run 5.07.19
[STEP 9]
NFO]: Runns/RUN_2
[STEP 10]
NFO]: Run28/logs/
[STEP 11]
NFO]: Run .47.28/l
[STEP 12]

beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlan
% cd designs
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlan
design if {[info exists ::env(CLOCK_PORT)] && $::env(CLOCK_PORT) != ""} {
    create_clock [get_ports $::env(CLOCK_PORT)] -name $::env(CLOCK_PORT) -peri
OpenLanod $::env(CLOCK_PERIOD)
/design} else {
    create_clock -name __VIRTUAL_CLK__ -period $::env(CLOCK_PERIOD)
set ::env(CLOCK_PORT) __VIRTUAL_CLK__
OpenLan}
/design
OpenLane set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
/design set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
OpenLane puts "[INFO]: Setting output delay to: $output_delay_value"
/design puts "[INFO]: Setting input delay to: $input_delay_value"
/home/be
/sky130 set_max_fanout $::env(MAX_FANOUT_CONSTRAINT) [current_design]
[2] 26 if { [info exists ::env(MAX_TRANSITION_CONSTRAINT)] } {
    set_max_transition $::env(MAX_TRANSITION_CONSTRAINT) [current_design]
/design}
error:
set clk_input [get_port $::env(CLOCK_PORT)]
OpenLane set clk_indx [lsearch [all_inputs] $clk_input]
/design set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx ""]
#set rst_input [get_port resetn]
_base.sdc

```

runs/RUN_2025.07.19_01.47.28/logs/placement/15-dpl_sta.log)...
% set ::env(SYNTH_MAX_FANOUT) 4
4
% run_synthesis
[STEP 16]

- ❖ Timing ECO (engineering change order) - increase size for larger drive so less delay
- ❖

Timing Analysis w/ Ideal Clocks

- ❖ Clk signals sent by PLL
- ❖ Setup timing analysis eq : $\Theta < T - S$
- ❖ Θ - Combinational delay , includes clk to q, delay of launch flop and internal propagation delay of all gates between launch and capture flop
- ❖ T - Time period AKA required time
- ❖ S - Setup time
- ❖ Clk is expected to send at 0,T,2T, but might not do it exactly at these times bc of in-built clock variation (AKA jitter)
- ❖ Realistic eq : $\Theta < T - S - SU$
- ❖ SU - setup uncertainty bc of jitter
- ❖
- ❖ Some of the photos are in earlier section
- ❖
- ❖

Clock Tree Synthesis

- ❖ Skew should be close to 0
- ❖ H-Tree routing- Midpoint strategy - go to each midpoint so clock reaches at same time
- ❖ Clock skew happens bc: wire length diff, variation in signal routing path, variation in buffer delay, etc.
- ❖ Crosstalk - signal in one channel interferes w/ signal in nearby channel - causes errors BAD
- ❖ Clock nets - important in design
- ❖

```
% run_cts
[STEP 17]
[INFO]: Running Clock Tree Synthesis (log: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/logs/cts/17-cts.log)...
[STEP 18]
[INFO]: Running Single-Corner Static Timing Analysis (log: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/logs/cts/18-cts_sta.log)...
%
[OpenLane Container: /nq
/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/placement$ ] docker install requirements_dev.txt
OpenLane Launcher Open docs Jenkinsfile requirements_lint.txt
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane$ 
```

```
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/synthesis$ cd ../../../../..
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/synthesis$ log cd ../../scripts
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/scripts$ cd tcl_commands/
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/scripts/tcl_commands$ ls
all.tcl      floorplan.tcl    lvs.tcl       placement.tcl   routing.tcl
checkers.tcl init_design.tcl  magic.tcl     README.md      sta.tcl
cts.tcl      klayout.tcl     pkgIndex.tcl  refresh.tcl   synthesis.tcl
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/scripts/tcl_commands$ 
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/placement$ ] docker ps
[STEP 17]
[INFO]: Running Clock Tree Synthesis (log: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/logs/cts/17-cts.log)...
[STEP 18]
[INFO]: Running Single-Corner Static Timing Analysis (log: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/logs/cts/18-cts_sta.log)...
%
[OpenLane Container: /nq
/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/placement$ ] docker install requirements_dev.txt
OpenLane Launcher Open docs Jenkinsfile requirements_lint.txt
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane$ 
```

The screenshot shows a macOS desktop environment. In the foreground, there is a terminal window titled "Terminal" with the command "beaver@openlanevm: ~/Desktop/work/tools/openlane_working_dir/openlane..." running. The terminal displays log output from the OpenLane tool, specifically the "run" command, which includes the Apache License 2.0 and a proc definition for run_cts. Below the terminal, the status bar shows the date and time as "Jul 21 16:15".

In the background, there is a file browser window titled "OpenLane" showing a directory structure under "ng_dir/openlane/designs/ci/synthesis". The visible paths include "docs", "Jenkinsfile", and "requirements_lint.txt". The file browser has a sidebar with icons for "docs", "Jenkinsfile", and "requirements_lint.txt".

Timing Analysis w/ real clocks

- ❖ design satisfying slack (data required time - data arrival time) : ready to work in the given frequency.
- ❖ if eq is violated, then slack will become negative
- ❖ expect slack to be either zero or positive.
- ❖ Hold violation - when path is too fast - factors: combinational delay, clock buffer delay, hold time

The screenshot shows a macOS desktop environment with two terminal windows and a Jenkinsfile.

Terminal 1 (Left):

```
OpenROAD d423155d69de7f683a23f6916ead418a615ad4ad
Features included (+) or not (-): +Charts +GPU +GUI +Python
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
openroad>
openroad>
openroad> read_lef designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/tmp/merged.nom.lef
[INFO ODB-0227] LEF file: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/tmp/merged.nom.lef, created 13 layers, 25 vias, 442 library cells
openroad> read_def designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/cts/picorv32.def
[INFO ODB-0127] Reading DEF file: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/cts/picorv32.def
[INFO ODB-0128] Design: picorv32
[INFO ODB-0130]     Created 411 pins.
[INFO ODB-0131]     Created 14184 components and 81437 component-terminals.
[INFO ODB-0132]     Created 2 special nets and 48660 connections.
[INFO ODB-0133]     Created 9858 nets and 32671 connections.
[INFO ODB-0134] Finished DEF file: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/cts/picorv32.def
openroad>
```

Terminal 2 (Right):

```
working_dir/openlane$ cat picorv32.def | grep
working_dir/openlane$ cd ../synthesis
working_dir/openlane$ synthesis ls
working_dir/openlane$ cd ..
working_dir/openlane$ synthesis ls
working_dir/openlane$ cd cts
working_dir/openlane$ synthesis ls
working_dir/openlane$ pwd
_dir/openlane/designs/ci/picorv32
working_dir/openlane$
```

Jenkinsfile (Bottom):

```
docs Jenkinsfile requirements_lint.txt
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane$
```

OpenLane Launcher (Bottom Left):

```
beaver@openlanevm:~/Desktop/picorv32a/runs/RUN_2025.07.19_01.47.28/results/cts$
```

Console Output (Bottom):

```
merged.nom.lef, created 13 layers, 25 vias, 442 library cells
enroad> read_def designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/cts/picorv32.def
[INFO ODB-0127] Reading DEF file: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/cts/picorv32.def
[INFO ODB-0128] Design: picorv32
[INFO ODB-0130]     Created 411 pins.
[INFO ODB-0131]     Created 14184 components and 81437 component-terminals.
[INFO ODB-0132]     Created 2 special nets and 48660 connections.
[INFO ODB-0133]     Created 9858 nets and 32671 connections.
[INFO ODB-0134] Finished DEF file: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/cts/picorv32.def
enroad> write_db pico_cts.db
enroad>
```

Beaver Prompt (Bottom Right):

```
beaver@openlanevm:~/Desktop/picorv32a/runs/RUN_2025.07.19_01.47.28$
```

```

is licensed under th beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/
this
ored.
d_lef
[7] LEF
ef, cre
d_def
[7] Rea
ts/pic
[8] Des
[0]
[1]
[2]
[3]
[4] Fin
cts/p
te_db
openlan
er Open
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane$ ls -l
drwxr-xr-x 4 beaver beaver 4096 Jul 14 07:34 designs
drwxrwxr-x 2 beaver beaver 4096 Jul 14 07:34 docker
drwxr-xr-x 5 beaver beaver 4096 Jul 14 07:34 docs
drwxr-xr-x 3 beaver beaver 4096 Jul 14 07:34 regression_results
-rw-rw-r-- 1 beaver beaver 194 Jul 14 07:34 klayoutrc
-rwxrwxr-x 1 beaver beaver 3631 Jul 14 07:34 gui.py
-rwxrwxr-x 1 beaver beaver 12221 Jul 14 07:34 flow.tcl
-rw-rw-r-- 1 beaver beaver 2356 Jul 14 07:34 flake.nix
-rw-rw-r-- 1 beaver beaver 3162 Jul 14 07:34 flake.lock
-rwxrwxr-x 1 beaver beaver 6983 Jul 14 07:34 env.py
-rwxrwxr-x 1 beaver beaver 16594 Jul 14 07:34 run_designs.py
-rw-rw-r-- 1 beaver beaver 74 Jul 14 07:34 requirements.txt
-rw-rw-r-- 1 beaver beaver 61 Jul 14 07:34 requirements_lint.txt
-rw-rw-r-- 1 beaver beaver 90 Jul 14 07:34 requirements_dev.txt
drwxr-xr-x 13 beaver beaver 4096 Jul 14 07:34 scripts
drwxrwxr-x 23 beaver beaver 4096 Jul 14 07:34 tests
drwxr-xr-x 2 root root 4096 Jul 14 07:35 empty
drwxrwxr-x 5 beaver beaver 4096 Jul 14 07:35 dependencies
drwxr-xr-x 5 root root 4096 Jul 14 07:38 venv
drwxr-xr-x 2 root root 4096 Jul 14 07:40 install
-rw-rw-r-- 1 beaver beaver 6818 Jul 18 18:43 Makefile
drwxrwxr-x 6 beaver beaver 4096 Jul 20 16:15 vsdstdcelldesign
-rw-r--r-- 1 root root 8023523 Jul 21 17:34 pico_cts.db
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane$
```

❖ Echo \$::env(CTS_CLK_BUFFER_LIST)

```

❖ Echo $::env(CTS_CLK_BUFFER_LIST)

Terminal
openroad>
openroad> read_lef designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/tmp/merged.nom.lef
[INFO ODB-0227] LEF file: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/tmp/merged.nom.lef, created 13 layers, 25 vias, 442 library cells
openroad> read_def designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/cts/picorv32.def
[INFO ODB-0127] Reading DEF file: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/cts/picorv32.def
[INFO ODB-0128] Design: picorv32
[INFO ODB-0130]     Created 411 pins.
[INFO ODB-0131]     Created 14184 components and 81437 component-terminals.
[INFO ODB-0132]     Created 2 special nets and 48660 connections.
[INFO ODB-0133]     Created 9858 nets and 32671 connections.
[INFO ODB-0134] Finished DEF file: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/cts/picorv32.def
openroad> write_db pico_cts.db
openroad> read_db pico_cts.db
[ERROR ORD-0047] You can't load a new db file as the db is already populated
ORD-0047
while evaluating read_db pico_cts.db
openroad> read_verilog designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/synthesis/picorv32.v
openroad> read_liberty - max $::env(LIB_MAX)
beaver@openlan
nroad$ ls
drwxrwxr-x 6 beaver beaver 4096 Jul 20 16:15 vsdstdcelldesign
OpenLane Launcher OpenLane$ ls
drwxr--r-- 1 root root 8023523 Jul 21 17:34 pico_cts.db
```

```

openroad> exit
% openroad
OpenROAD d423155d69de7f683a23f6916ead418a615ad4ad
Features included (+) or not (-): +Charts +GPU +GUI +Python
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which
must be honored.
openroad> read_db pico_cts.db
openroad> read_verilog designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results
/synthesis/picorv32.v
openroad> read_liberty - max $::env(LIB_SYNTH_COMPLETE)
[ERROR STA-0565] read_liberty requires one positional argument.
STA-0565
while evaluating read_liberty - max $::env(LIB_SYNTH_COMPLETE)
openroad> read_liberty $::env(LIB_SYNTH_COMPLETE)
1
❖ openroad> link_design picorv32a

```

Routing and DRC

- ❖ Routing - best possible connection between two points- usually L
- ❖ Maze Routing - Lee's Algorithm, good for grid routing so good for IC design- expanding numbers around the source and go through those- not the best since it takes memory
- ❖ Wave expansion:
- ❖ Performs wave expansion from source outwards
- ❖ Algorithm examines neighboring cells (but not diagonal)
- ❖ Continues until target is reached or no more can be visited
- ❖ One drc rule is minimum distance,width, pitch, spacing needed for wires
- ❖ Another rule is a signal short- solve by changing layers
- ❖ Another rule is via width and via spacing

```

% prep -design designs/ci/picorv32a
[INFO]: Using configuration in 'designs/ci/picorv32a/config.json'...
[INFO]: PDK Root: /root/.volare
[INFO]: Process Design Kit: sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Optimization Standard Cell Library: sky130_fd_sc_hd
[INFO]: Run Directory: /home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.27_02.08.18
[WARNING]: SYNTH_MAX_FANOUT is now deprecated; use MAX_FANOUT_CONSTRAINT instead
.
[INFO]: Saving runtime environment...
[INFO]: Preparing LEF files for the nom corner...
[INFO]: Preparing LEF files for the min corner...
[INFO]: Preparing LEF files for the max corner...
[WARNING]: PNR_SDC_FILE is not set. It is recommended to write a custom SDC file for the design. Defaulting to BASE_SDC_FILE
[WARNING]: SIGNOFF_SDC_FILE is not set. It is recommended to write a custom SDC file for the design. Defaulting to BASE_SDC_FILE
% echo $::env(CURRENT_DEF)
/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/cts/picorv32.def
%
beaver@openlanewm:~$ ls -l . 18. Executing PROC_CLEAN pass (remove empty switches from decision trees).
-rw-rw-r-- 1 beaver beaver 4096 Jul 20 16:15 vsdstdcelldesign
drwxrwxr-x 6 beaver beaver 4096 Jul 20 16:15 pico_cts.db
-rw-r--r-- 1 root root 8023523 Jul 21 17:34 pico_cts.db
beaver@openlanewm:~/Desktop/work/tools/openlane_working_dir/openlane$ 

```

beaver@openlanewm:~\$ ls -l . 18. Executing PROC_CLEAN pass (remove empty switches from decision trees).

-rw-rw-r-- 1 beaver beaver 4096 Jul 20 16:15 vsdstdcelldesign

drwxrwxr-x 6 beaver beaver 4096 Jul 20 16:15 pico_cts.db

-rw-r--r-- 1 root root 8023523 Jul 21 17:34 pico_cts.db

beaver@openlanewm:~/Desktop/work/tools/openlane_working_dir/openlane\$

The screenshot shows a Linux desktop environment with a terminal window and a file browser window.

Terminal Window:

```

run_routing
STEP 20]
INFO]: Running Global Routing Resizer Design Optimizations (log: designs/ci/picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/20-resizer_design.log)...
STEP 21]
INFO]: Running Single-Corner Static Timing Analysis (log: designs/ci/picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/21-rsz_design_sta.log)...
STEP 22]
INFO]: Running Global Routing Resizer Timing Optimizations (log: designs/ci/picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/22-resizer_timing.log)...
STEP 23]
INFO]: Running Single-Corner Static Timing Analysis (log: designs/ci/picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/23-rsz_timing_sta.log)...
STEP 24]
INFO]: Running I/O Diode Insertion (log: designs/ci/picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/24-io_diodes.log)...
STEP 25]
INFO]: Running Detailed Placement (log: designs/ci/picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/25-io_diode_legalization.log)...
STEP 26]
INFO]: Running Heuristic Diode Insertion (log: designs/ci/picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/26-diodes.log)...
STEP 27]
INFO]: Running Detailed Placement (log: designs/ci/picrv32a/runs/RUN_2025.07.27_02.08.18/logs/floorplan.log)

```

File Browser Window:

The file browser window shows a list of files and folders in a directory. The visible items include:

- 7_14.44.10
- 7_15.33.20
- 9_01.47.28
- 7_02.08.18
- in.log
- it_buffer
- openlane/designs/ci/
- picrv32a/runs/RUN_2025.07.27_02.08.18/logs/floorplan
- picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing
- picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/20-resizer_design.log
- picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/21-rsz_design_sta.log
- picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/22-resizer_timing.log
- picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/23-rsz_timing_sta.log
- picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/24-io_diodes.log
- picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/25-io_diode_legalization.log
- picrv32a/runs/RUN_2025.07.27_02.08.18/logs/routing/26-diodes.log
- picrv32a/runs/RUN_2025.07.27_02.08.18/logs/floorplan.log

- ❖ Routing – fast/global route (separated into tiles, initial framework), detail route (fine tunes and finalizes paths)
- ❖ TritonRoute - performs initial detail route, follows preprocessed route guides, assumes they satisfy inter-guide connectivity(if they are on same metal layer w/ touching edges or on neighboring metal layers w/ overlapped area, unconnected terminal should have pin shape overlapped by route guide)
- ❖ Inputs - LEF, DEF, preprocessed route guide
- ❖ Output - detailed route solution w/ optimized wire-length and via count
- ❖ Constraints - drc, route guide honoring, connectivity constraints
- ❖ Access Point (AP), Access Point Cluster (APC)
- ❖ MILP - optimal solution to connect 2 APC

❖ tmp/routing/ fastroute.guide

```
[STEP 27]
[INFO]: Running Detailed Placement (log: designs/ci/picorv32a/runs/RUN_2025.07.2
7.02.08.18/logs/routing/28-globally_optimized_placer.log)
[STEP 28]
[INFO]: Running Global Placement (log: designs/ci/picorv32a/runs/RUN_2025.07.2
7.02.08.18/logs/routing/28-globally_optimized_placer.log)
[STEP 29]
[INFO]: Writing Verilog (log: designs/ci/picorv32a/runs/RUN_2025.07.2
7.02.08.18/logs/routing/28-globally_optimized_placer.log)
[STEP 30]
[INFO]: Running Step 30 (log: designs/ci/picorv32a/runs/RUN_2025.07.2
7.02.08.18/logs/routing/28-globally_optimized_placer.log)
[INFO]: Running Step 31 (log: designs/ci/picorv32a/runs/RUN_2025.07.2
7.02.08.18/logs/routing/28-globally_optimized_placer.log)
[INFO]: Running Step 32 (log: designs/ci/picorv32a/runs/RUN_2025.07.2
7.02.08.18/logs/routing/28-globally_optimized_placer.log)
[INFO]: No Magic Design (log: designs/ci/picorv32a/runs/RUN_2025.07.2
7.02.08.18/logs/routing/28-globally_optimized_placer.log)
[STEP 33]
[INFO]: Checking Wire Lengths (log: designs/ci/picorv32a/runs/RUN_2025.07.2
7.02.08.18/logs/routing/28-globally_optimized_placer.log)
1753583045
%
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/runs/RUN_2025.07.2$ git diff openlane_working_dir/openlane/designs/picorv32a/runs/RUN_2025.07.2
diff --git a/openlane_working_dir/openlane/designs/picorv32a/runs/RUN_2025.07.2 b/openlane/designs/picorv32a/runs/RUN_2025.07.2
index 1234567..8901234 100755
--- a/openlane_working_dir/openlane/designs/picorv32a/runs/RUN_2025.07.2
+++ b/openlane/designs/picorv32a/runs/RUN_2025.07.2
@@ -1 +1 @@

```

- ❖ Go to tools and SPEF_EXTRACTor and then python3 [main.py](#) and then address it should be in (forgot to take screenshot of this)