

```

ne/beave
ne/beave
gz open
ne/beave
#-----#
# uhrpoly (P+ poly resistor, 2kOhm/sq)
#-----#
ne/beave
width uhrpoly 350 "uhrpoly resistor width < %d (poly.9)"
# NOTE: uhrpoly resistor requires choice of discrete widths 0.35, 0.69, ... up to 350
#-----#
ne/beave
spacing uhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
    "uhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
spacing uhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
    "uhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
#-----#
# MOS Varactor device rules
#-----#
: nano
ne/beave
^G Help      ^O Write Out ^W Where Is ^K Cut      ^T Execute ^C Location
^X Exit       ^R Read File ^\ Replace   ^U Paste    ^J Justify ^/ Go To Line

```

tkcon 2.3 Main

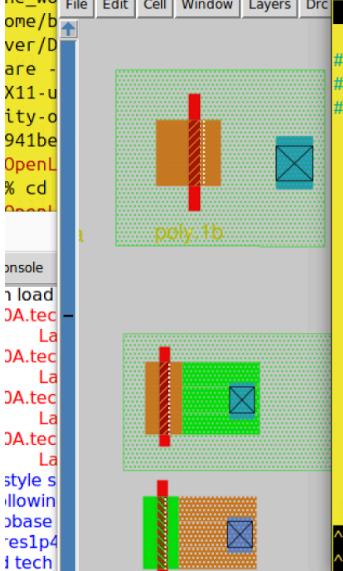
Console Edit Interp Prefs History Help

```

tech load sky130A.tech
/130A.tech: line 1875: section cifinput:
    Labels on layer "DIFF" attached to "mvvaractor" supersedes prior attachment to "nbase".
/130A.tech: line 1876: section cifinput:
    Labels on layer "DIFFTXT" attached to "mvvaractor" supersedes prior attachment to "nbase".
/130A.tech: line 1877: section cifinput:
    Labels on layer "DIFFPIN" attached to "mvvaractor" supersedes prior attachment to "nbase".
/130A.tech: line 2171: section cifinput:
    Labels on layer "TAPPIN" attached to "nsubdiff" supersedes prior attachment to "nbase".
out style sky130: scaleFactor=2, multiplier=2
the following types are not handled by extraction and will be treated as non-electrical types:
mvpbase nnmos obsactive mvobsactive obsli1 obsli1c obsm1 obsm2 obsm3 obsm4 obsm5 obsmrcl fillblock comm
69 res1p41 res2p85 res5p73
aled tech values by 2 / 1 to match internal grid scaling
sting layout may be invalid.
drc check

```

beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign%



GNU nano 7.2 sky130A.tech *

```

#-----
# POLY
#-----

width allpoly 150 "poly.width < %d (poly.1a)"
spacing allpoly allpoly 210 touching_ok "poly.spacing < %d (poly.2)"
spacing allpolynonfet alldifflynonfet 75 corner_ok allfets \
    "poly.spacing to Diffusion < %d (poly.4a)"
spacing npres alldiff 480 touching_illegal \
    "poly.resistor spacing to N-tap < %d (poly.9)"
spacing npres allpolynonres 480 touching_illegal \
    "poly.resistor spacing to N-tap < %d (poly.9)"
overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of nmos"
overhang *mvndiff,mvrndiff mvnfet,mvnnfet 250 \
    "N-Diffusion overhang of nmos < %d (poly.7)"
overhang *pdifff,rpdifff pfet,scpfet,ppu 250 "P-Diffusion overhang of pmos < %d (poly.8)"
overhang *mvpdiff,mvrpdifff mvpfet 250 "P-Diffusion overhang of pmos < %d (poly.8)"
overhang *poly allfets 130 "poly.overhang of transistor < %d (poly.8)"
rect_only allfets "No bends in transistors (poly.11)"

^G Help      ^O Write Out   ^W Where Is   ^K Cut       ^T Execute   ^C Location
^X Exit      ^R Read File   ^L Replace    ^U Paste     ^J Justify   ^I Go To Line

```

Terminal

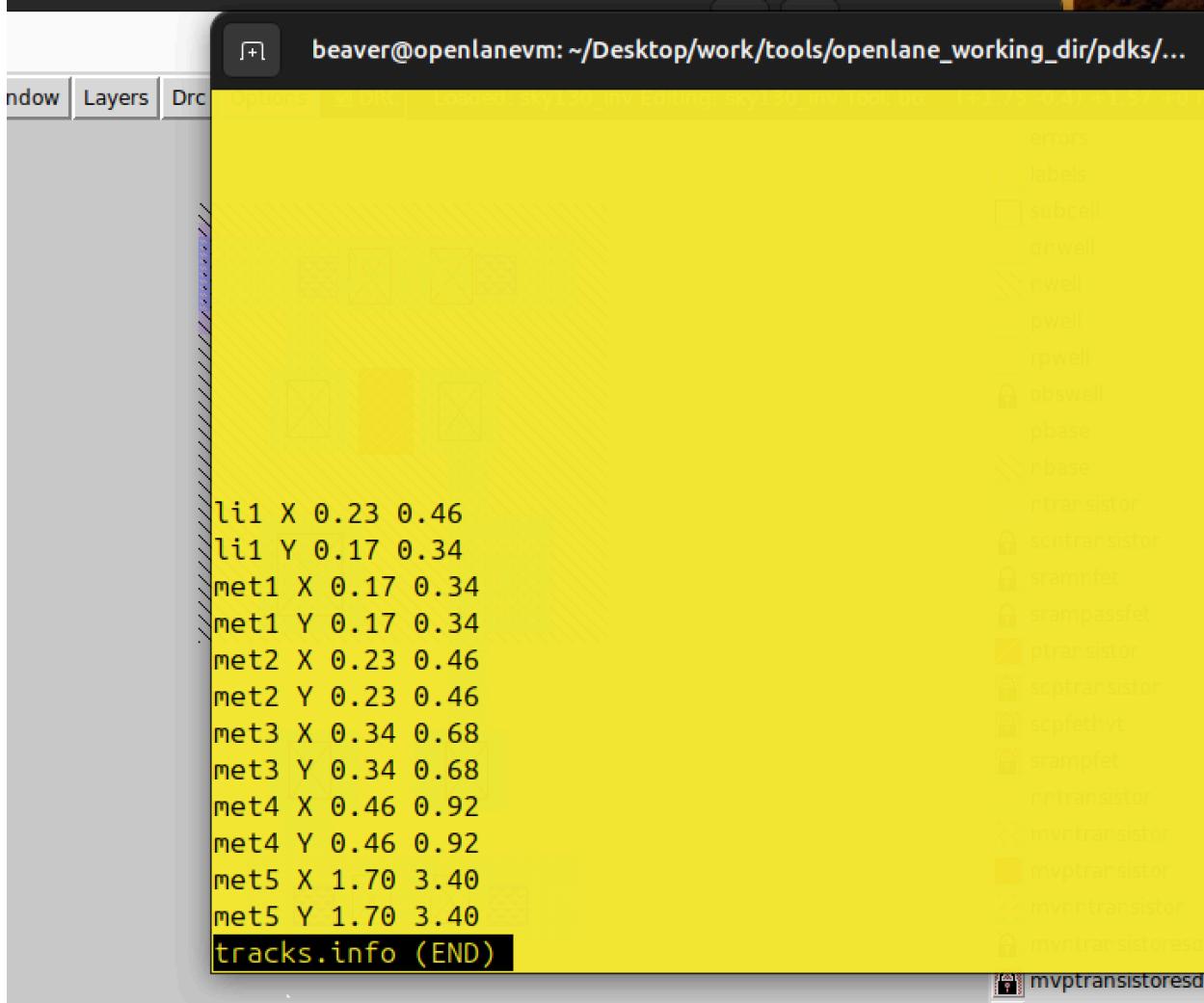
```

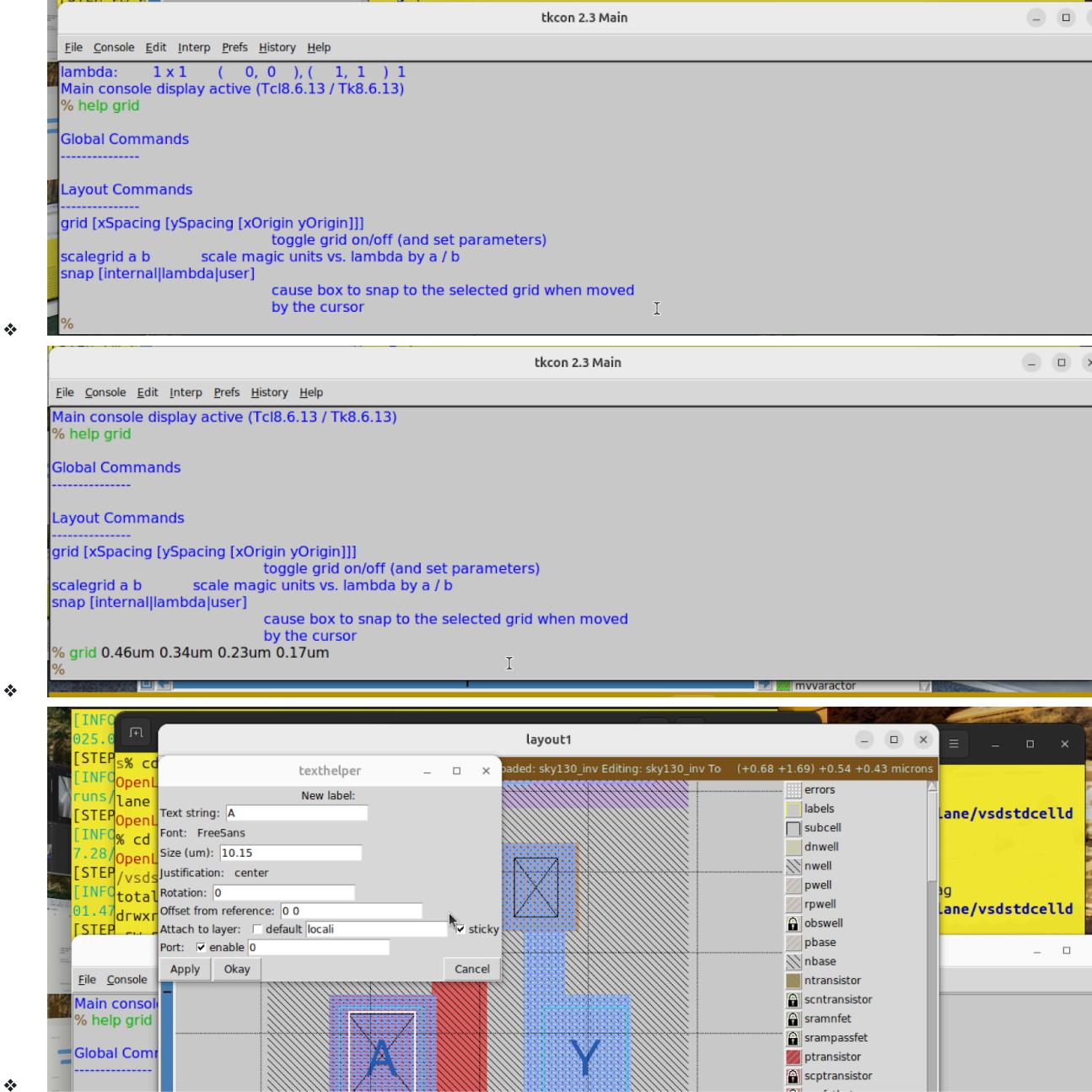
s% cd ..
OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir% cd openlane
OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane
% cd vsdstdcelldesign
OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign% ls -ltr
total 188
drwxrwxr-x 2 openlane-user-1000 1000 4096 Jul 17 15:38 Images
-rw-rw-r-- 1 openlane-user-1000 1000 13525 Jul 17 15:38 README.md
-rw-rw-r-- 1 openlane-user-1000 1000 11357 Jul 17 15:38 LICENSE
drwxrwxr-x 2 openlane-user-1000 1000 4096 Jul 17 15:38 extras
-rw-rw-r-- 1 openlane-user-1000 1000 2716 Jul 17 15:38 sky130_inv.mag
-rwxr-xr-x 1 openlane-user-1000 1000 136710 Jul 17 15:47 sky130A.tech
-rw-r--r-- 1 root          root 1365 Jul 18 01:26 sky130_inv.ext
drwxrwxr-x 2 openlane-user-1000 1000 4096 Jul 19 00:24 libs
-rw-r--r-- 1 root          root 584 Jul 19 00:36 sky130_inv.spice
OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign% magic -T sky130A.tech sky130_inv.mag &
[1] 16
OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign% Fontconfig error: Cannot load default config file: No such file: (null)

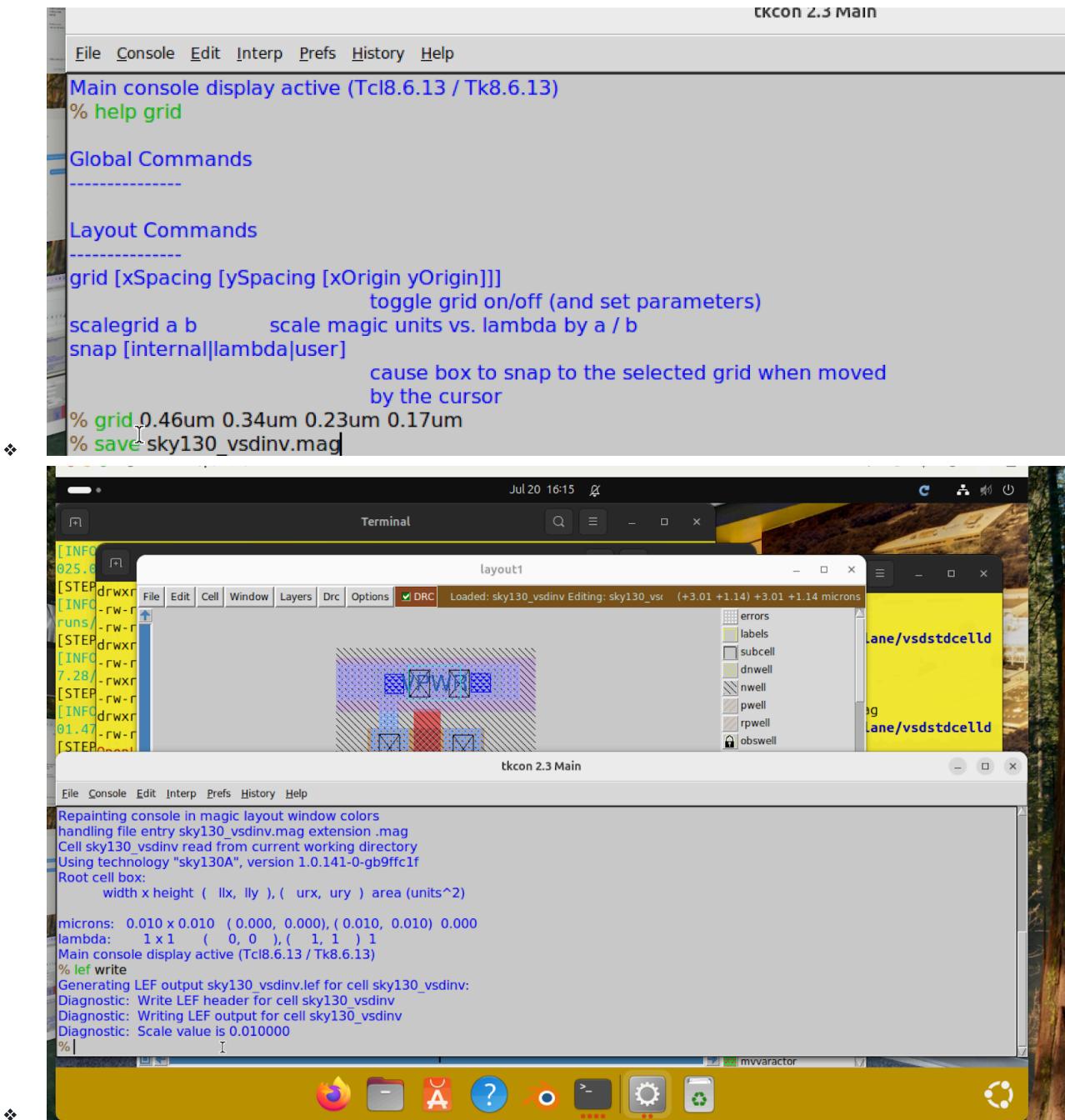
```

ja: console

```
sky130_fd_sc_hd/  sky130_fd_sc_hdll/ sky130_fd_sc_hs/  sky130_fd_sc_hvl/
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane$ cd ../pdks
/sky130A/libs.tech/openlane/sky130_fd_sc_hd
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.te
ch/openlane/sky130_fd_sc_hd$ less track.info
track.info: No such file or directory
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.te
ch/openlane/sky130_fd_sc_hd$ less tracks.info
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.te
ch/openlane/sky130_fd_sc_hd$ █
```







```
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 196
drwxrwxr-x 2 beaver beaver 4096 Jul 17 08:38 Images
-rw-rw-r-- 1 beaver beaver 13525 Jul 17 08:38 README.md
-rw-rw-r-- 1 beaver beaver 11357 Jul 17 08:38 LICENSE
drwxrwxr-x 2 beaver beaver 4096 Jul 17 08:38 extras
-rw-rw-r-- 1 beaver beaver 2716 Jul 17 08:38 sky130_inv.mag
-rwrxr-xr-x 1 beaver beaver 136710 Jul 17 08:47 sky130A.tech
-rw-r--r-- 1 root  root    1365 Jul 17 18:26 sky130_inv.ext
drwxrwxr-x 2 beaver beaver 4096 Jul 18 17:24 libs
-rw-r--r-- 1 root  root    584 Jul 18 17:36 sky130_inv.spice
-rw-r--r-- 1 root  root    2716 Jul 20 16:14 sky130_vsdinv.mag
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ less sky130_vsdinv.lef
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

The screenshot shows a macOS desktop environment with several open windows:

- Terminal Window 1:** Displays a command-line interface with the following text:

```
[INFO] 025.0
[STEP] runs/
[INFO] 7.28/
[STEP] MACRO sky130_vsdinv
[INFO] 01.47
[STEP] File C
[INFO] Repair
[STEP] handle: (
[INFO] Cell s
[INFO] Using
[Root] [1]
[OpenL] /vsds
[micro] lambd
[Main] % lef
[Genel] le: (
[Diagn] Diagnostic:
[Diagnostic] Diagnostic:
[%] sky130_vsdinv.lef
```
- Terminal Window 2:** Displays a command-line interface with the following text:

```
beaver@openlanevm: ~/Desktop/work/tools/openlane_working_dir/open...
VERSION 5.7 ;
  NOWIREEXTENSIONATPIN ON ;
  DIVIDERCHAR "/";
  BUSBITCHARS "[]";
  MACRO sky130_vsdinv
  CLASS CORE ;
  FOREIGN sky130_vsdinv ;
  ORIGIN 0.000 0.000 ;
  SIZE 1.380 BY 2.720 ;
  SITE unithd ;
  PIN A
    DIRECTION INPUT ;
    USE SIGNAL ;
    ANTENNAGATEAREA 0.165600 ;
    PORT
      LAYER li1 ;
      RECT 0.060 1.180 0.510 1.690 ;
    END
  END A
  PIN Y
    DIRECTION OUTPUT ;
    USE SIGNAL ;
    ANTENNADIFFAREA 0.287800 ;
```
- File Browser:** Shows a tree view of directory contents, including:
 - dir/openlane/vsdstdcelld
 - ith:
 - 30_inv.mag
 - dir/openlane/vsdstdcelld
 - dir/openlane\$ cd .. /pdks
 - dir/openlane\$ cd .. /pdks
 - sky130_fd_sc_hvl/
 - dir/openlane\$ cd .. /pdks
 - dir/pdks/sky130A/libs.te
 - dir/pdks/sky130A/libs.te
 - dir/pdks/sky130A/libs.te

```
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a.v
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/src$ ls -ltr
total 96
-rw-rw-r-- 1 beaver beaver 94474 Jul 15 16:44 picorv32a.v
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/src$ pwd
/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/src
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/src$ ls -ltr
total 100
-rw-rw-r-- 1 beaver beaver 94474 Jul 15 16:44 picorv32a.v
-rw-r--r-- 1 beaver beaver 1321 Jul 20 16:20 sky130_vsdinv.lef
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/src$ ls -ltr
total 37428
-rw-rw-r-- 1 beaver beaver 94474 Jul 15 16:44 picorv32a.v
-rw-r--r-- 1 beaver beaver 1321 Jul 20 16:20 sky130_vsdinv.lef
-rw-rw-r-- 1 beaver beaver 12753932 Jul 20 16:22 sky130_fd_sc_hd_fast.lib
-rw-rw-r-- 1 beaver beaver 12732258 Jul 20 16:22 sky130_fd_sc_hd_slow.lib
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/src$
```

Jul 21 07:57

Terminal

```
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% package require openlane
0.9
% prep -design designs/ci/picorv32a -tag RUN_2025.07.19_01.47.28 -overwrite
[INFO]: Using configuration in 'designs/ci/picorv32a/config.json'...
[INFO]: PDK Root: /root/.volare
[INFO]: Process Design Kit: sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Optimization Standard Cell Library: sky130_fd_sc_hd
[INFO]: Run Directory: /home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28
[INFO]: Removing existing /home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28...
[INFO]: Saving runtime environment...
[INFO]: Preparing LEF files for the nom corner...
[INFO]: Preparing LEF files for the min corner...
[INFO]: Preparing LEF files for the max corner...
[WARNING]: PNR_SDC_FILE is not set. It is recommended to write a custom SDC file for the design. Defaulting to BASE_SDC_FILE
[WARNING]: SIGNOFF_SDC_FILE is not set. It is recommended to write a custom SDC file for the design. Defaulting to BASE_SDC_FILE
%
```

Diagnostic: Write LEF header for cell sky130_fd_sc_hd
Diagnostic: Writing LEF output for cell sky130_fd_sc_hd

```
[INFO]: Using configuration in 'designs/ci/picorv32a/config.json'...
[INFO]: PDK Root: /root/.volare
[INFO]: Process Design Kit: sky130A
[INFO]: Standard Cell Library: sky130_fd_sc_hd
[INFO]: Optimization Standard Cell Library: sky130_fd_sc_hd
[INFO]: Run Directory: /home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28
[INFO]: Removing existing /home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28...
[INFO]: Saving runtime environment...
[INFO]: Preparing LEF files for the nom corner...
[INFO]: Preparing LEF files for the min corner...
[INFO]: Preparing LEF files for the max corner...
[WARNING]: PNR_SDC_FILE is not set. It is recommended to write a custom SDC file for the design. Defaulting to BASE_SDC_FILE
[WARNING]: SIGNOFF_SDC_FILE is not set. It is recommended to write a custom SDC file for the design. Defaulting to BASE_SDC_FILE
% set lefs [glob ${::env(DESIGN_DIR)}/src/*.lef]
/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/src/sky130_vsdinv.lef
%
```

```
16:20 sky130_vsdinv.lef  
openlane_working_dir/openlane/designs/  
  
15 16:44 picorv32a.v  
20 16:20 sky130_vsdinv.lef  
20 16:22 sky130_fd_sc_hd_fast.lib  
20 16:22 sky130_fd_sc_hd_slow.lib  
20 16:22 sky130_fd_sc_hd_typical.lib  
openlane_working_dir/openlane/designs/  
  
openlane_working_dir/openlane/designs/  
  
openlane_working_dir/openlane/designs/  
  
openlane_working_dir/openlane/designs/  
  
_03.09.01 RUN_2025.07.17_14.44.10  
19.45.14 RUN_2025.07.17_15.33.20  
_00.16.00 RUN_2025.07.19_01.47.28  
_01.16.59  
openlane_working_dir/openlane/designs/
```

```
[INFO]: Preparing LEF files for the min corner...
[INFO]: Preparing LEF files for the max corner...
[WARNING]: PNR_SDC_FILE is not set. It is recommended to write a custom SDC file
for the design. Defaulting to BASE_SDC_FILE
[WARNING]: SIGNOFF_SDC_FILE is not set. It is recommended to write a custom SDC
file for the design. Defaulting to BASE_SDC_FILE
% set lefs [glob $::env(DESIGN_DIR)/src/*.lef]
/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv3
2a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /home/beaver/Desktop/work/tools/openlane_working_dir/openlane/de
signs/ci/picorv32a/src/sky130_vsdinv.lef
% run_synthesis
[STEP 1]
[INFO]: Running Synthesis (log: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.2
8/logs/synthesis/1-synthesis.log)...
[STEP 2]
[INFO]: Running Single-Corner Static Timing Analysis (log: designs/ci/picorv32a/
runs/RUN_2025.07.19_01.47.28/logs/synthesis/2-sta.log)...
% echo $::env(SYNTH_STRATEGY)
AREA 0
% set ::env(SYNTH_STRATEGY) 1
1
%
```

```
enlane_working_dir/openlane...    
file  
n SDC  
.corv3  
ne/de  
792.249600  
.47.2  
rv32a/  
, CPU: user 2.48s system 0.22s,  
++ 16.0.6 -fPIC -Os)  
opt_expr (0 sec), ...  
openlane_working_dir/openlane/d
```

OpenLane

Terminal Jul 21 08:16

```
2a/src/sky130_vsdinv.lef
% add_lefs -src $lefs
[INFO]: Merging /home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/src/sky130_vsdinv.lef
% run_synthesis
[STEP 1]
[INFO]: Running Synthesis (log: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/logs/synthesis/1-synthesis.log)...
[STEP 2]
[INFO]: Running Single-Corner Static Timing Analysis (log: designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/logs/synthesis/2-sta.log)...
% echo $::env(SYNTH_STRATEGY)
AREA 0
% set ::env(SYNTH_STRATEGY) 1
1
% echo $::env(SYNTH_BUFFERING)
1
% echo $::env(SYNTH_SIZING)
0
% set ::env(SYNTH_SIZING) 1
1
```

792.249600

, CPU: user 2.48s system 0.22s, MEM

INFO]: Run 25.07.19_01.47.28/1

STEP 9] /vsdstdcelldesign% cd ..

OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/runs/RUN_2025.07.19_01.47.28/logs/

STEP 10] % cd designs

OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs% cd ci

OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci% cd picorv32a

OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a% cd runs

OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs% cd RUN_2025.07.19_01.47.28

OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28% cd results

OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results% cd placement

OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/placement% magic -T /home/beaver/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic/sky130A.tech lef read ../../tmp/merged.nom.lef def read picorv32.def &

[2] 26

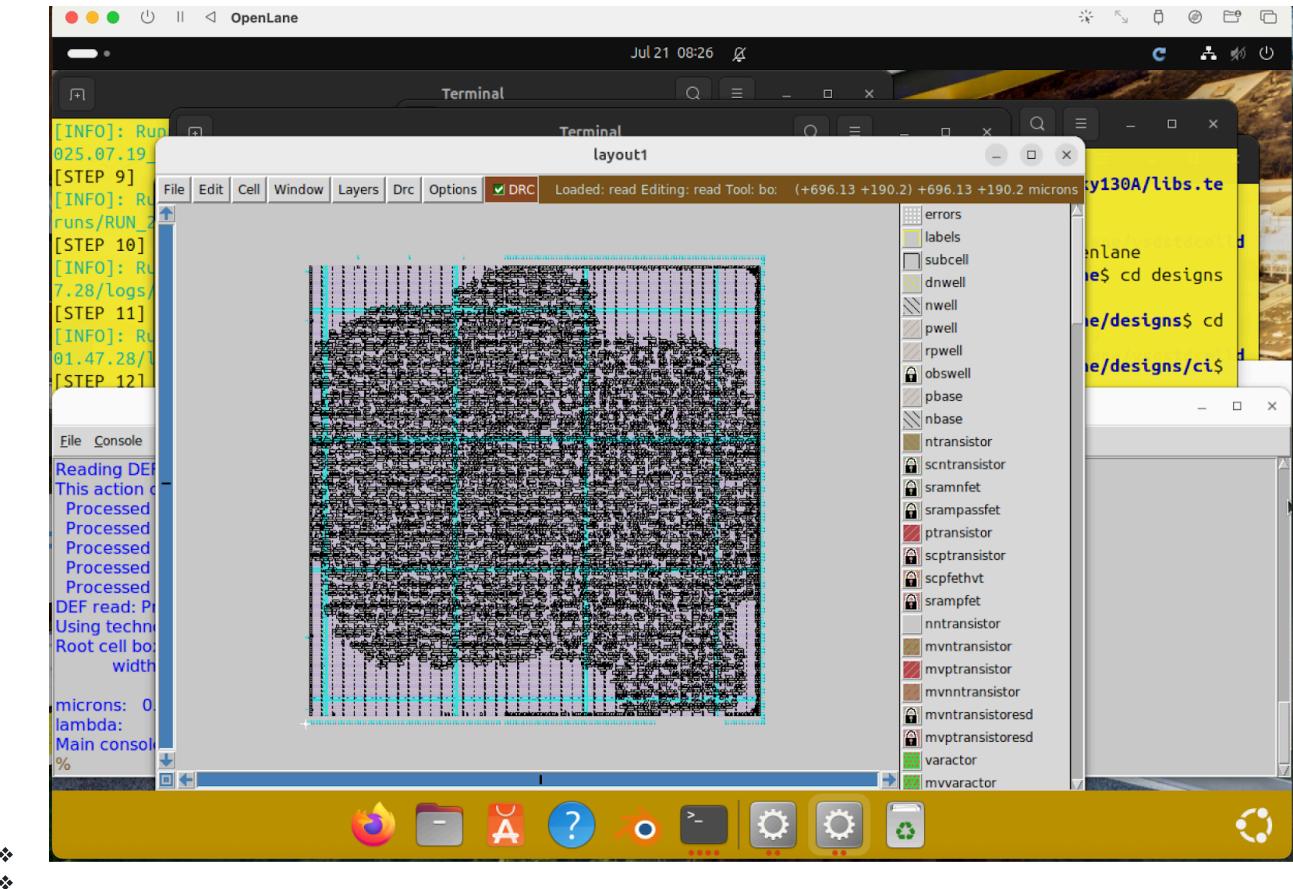
OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.19_01.47.28/results/placement% Fontconfig error: Cannot load default config file: No such file: (null)

microns: 0.6 microns

lambda: 0.00010000000000000002

main console

mvntransistored mvptransistored varactor mvvaractor



Delay Tables

- ❖ w/ AND, if other pin is 1, CLK moves. w/ OR, if other pin is 0, CLK moves
- ❖ Delay tables are used for cell timing models in lef files
- ❖ Output slew(depends on capacitive load and input slew) impacts delay majorly
- ❖ CT- process to design clock distribution network to minimize skew and ensure synchronous operation of the circuit (make sure everything happens when it should)
- ❖ Skew- variation in clock signal arrival times
- ❖ slew- rate of change of signal's voltage on time
- ❖ Latency -delay experienced by the clock signal