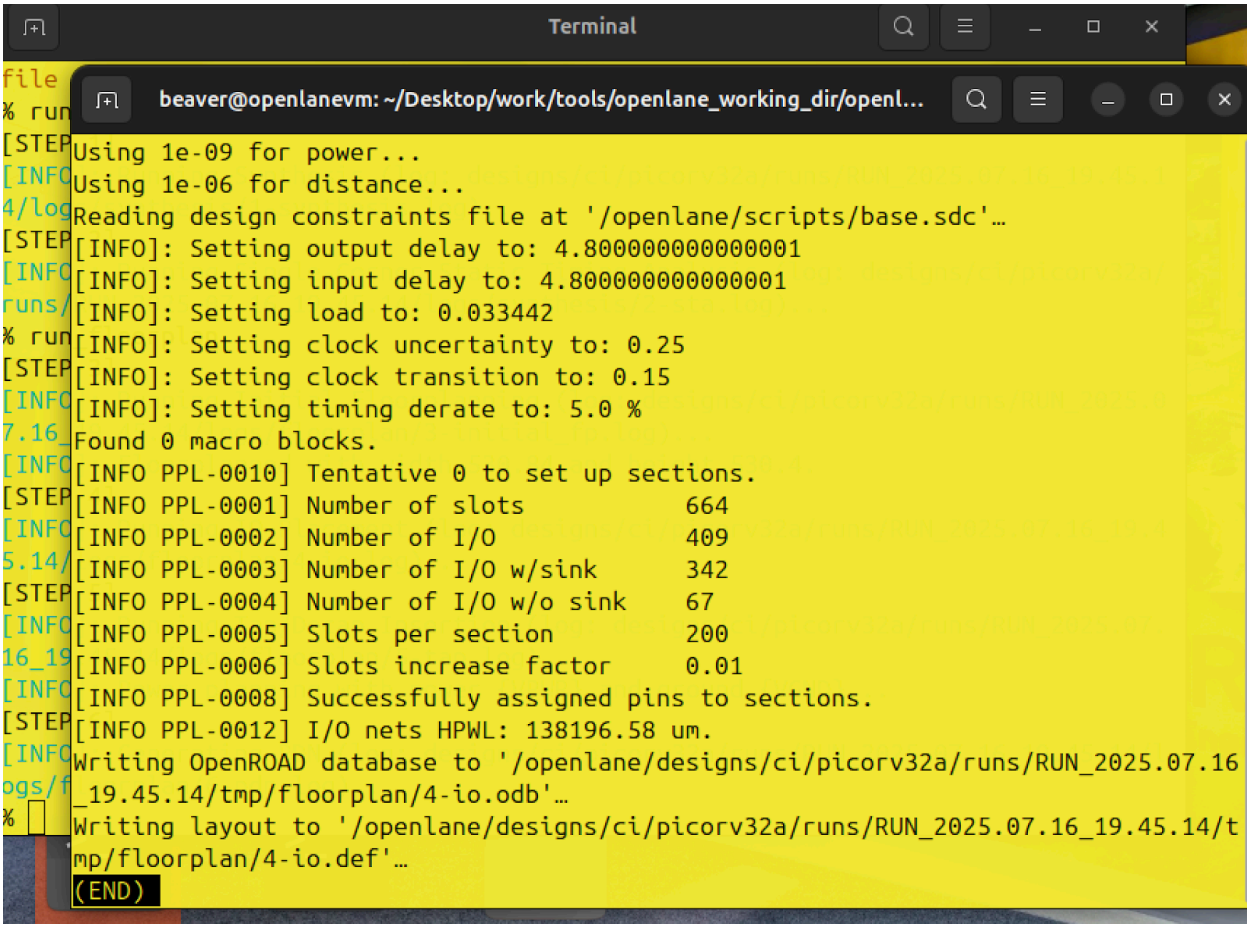


- Q to exit , shift g for end
- Cd .. twice and ls -ltr and then less config.tcl
-

```
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.16_19.45.14/logs/floorplan$ cd ../../
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/picorv32a/runs/RUN_2025.07.16_19.45.14$ less config.tcl
```

beaver@openlanevm: ~/Desktop/work/tools/openlane_working_dir/openl...

```
set ::env(signoff_tmpfiles) "/openlane/designs/ci/picorv32a/runs/RUN_2025.07.1
19.45.14/tmp/signoff"
set ::env(synthesis_logs) "/openlane/designs/ci/picorv32a/runs/RUN_2025.07.16_
.45.14/logs/synthesis"
set ::env(synthesis_reports) "/openlane/designs/ci/picorv32a/runs/RUN_2025.07.
_19.45.14/reports/synthesis"
set ::env(synthesis_results) "/openlane/designs/ci/picorv32a/runs/RUN_2025.07.
_19.45.14/results/synthesis"
set ::env(synthesis_tmpfiles) "/openlane/designs/ci/picorv32a/runs/RUN_2025.07
6_19.45.14/tmp/synthesis"
set ::env(timer_start) "1752695114"
set ::env(SYNTH_OPT) "0"
set ::env(PL_INIT_COEFF) "0.00002"
set ::env(PL_IO_ITER) "5"
set ::env(CURRENT_INDEX) 6
set ::env(CURRENT_DEF) /openlane/designs/ci/picorv32a/runs/RUN_2025.07.16_19.4
14/results/floorplan/picorv32.def
set ::env(CURRENT_GUIDE) "0"
set ::env(CURRENT_NETLIST) /openlane/designs/ci/picorv32a/runs/RUN_2025.07.16_
.45.14/results/synthesis/picorv32.v
set ::env(CURRENT_POWERED_NETLIST) "0"
set ::env(CURRENT_ODB) /openlane/designs/ci/picorv32a/runs/RUN_2025.07.16_19.4
14/results/floorplan/picorv32.odb
(END)
```

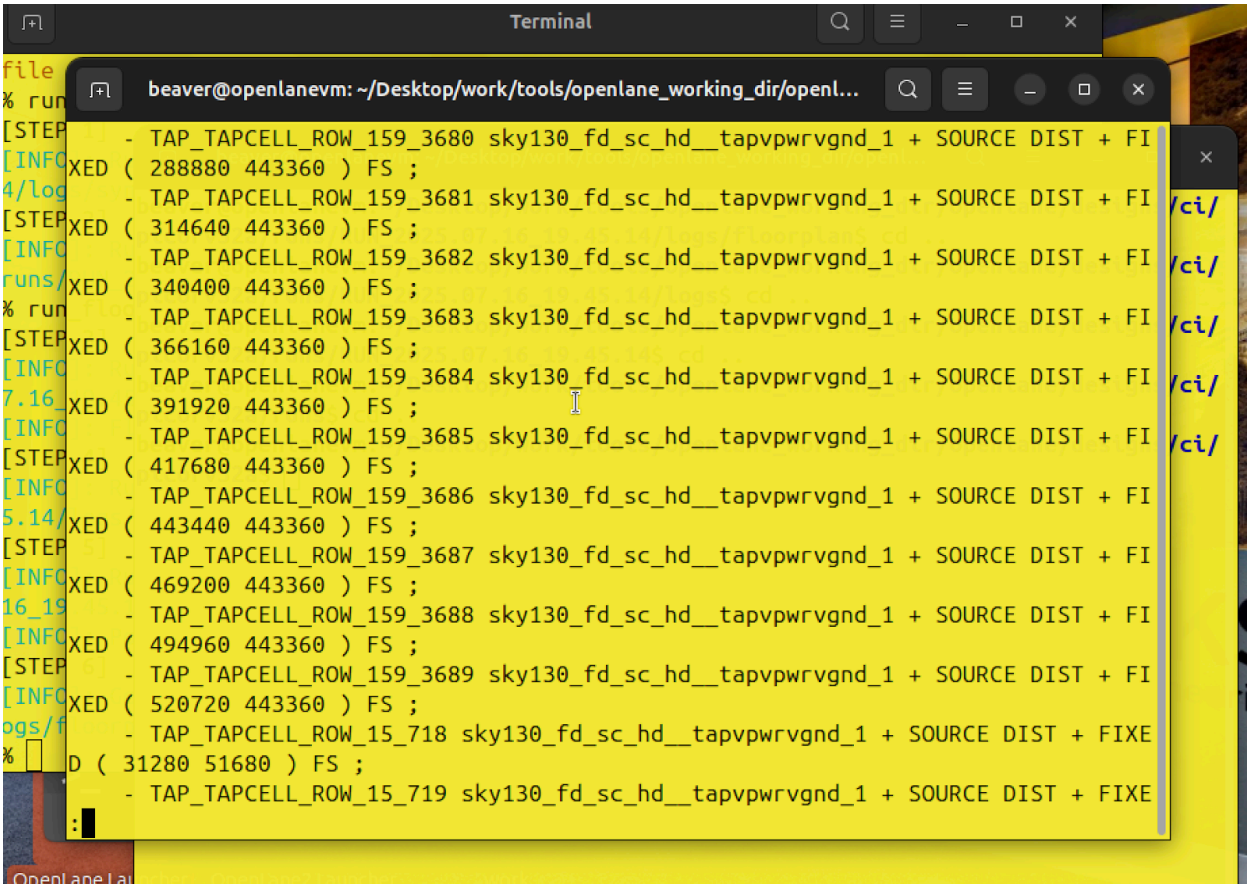
❖

❖ Cd results/floorplan

```
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/
picorv32a/runs/RUN_2025.07.16_19.45.14$ less config.tcl
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/
picorv32a/runs/RUN_2025.07.16_19.45.14$ ls -ltr
total 68
-rw-r--r-- 1 root root    51 Jul 14 07:39 PDK_SOURCES
-rw-r--r-- 1 root root   674 Jul 16 12:45 config_in.tcl
drwxr-xr-x 8 root root  4096 Jul 16 12:45 results
drwxr-xr-x 8 root root  4096 Jul 16 12:45 reports
drwxr-xr-x 8 root root  4096 Jul 16 12:45 logs
-rw-r--r-- 1 root root    50 Jul 16 12:45 OPENLANE_VERSION
-rw-r--r-- 1 root root   254 Jul 16 12:45 warnings.log
drwxr-xr-x 8 root root  4096 Jul 16 12:45 tmp
-rw-r--r-- 1 root root  1371 Jul 16 12:45 openlane.log
-rw-r--r-- 1 root root  7636 Jul 16 12:45 cmds.log
-rw-r--r-- 1 root root   572 Jul 16 12:45 runtime.yaml
-rw-r--r-- 1 root root 18862 Jul 16 12:45 config.tcl
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/
picorv32a/runs/RUN_2025.07.16_19.45.14$ cd results/floorplan/
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/
picorv32a/runs/RUN_2025.07.16_19.45.14/results/floorplan$
```

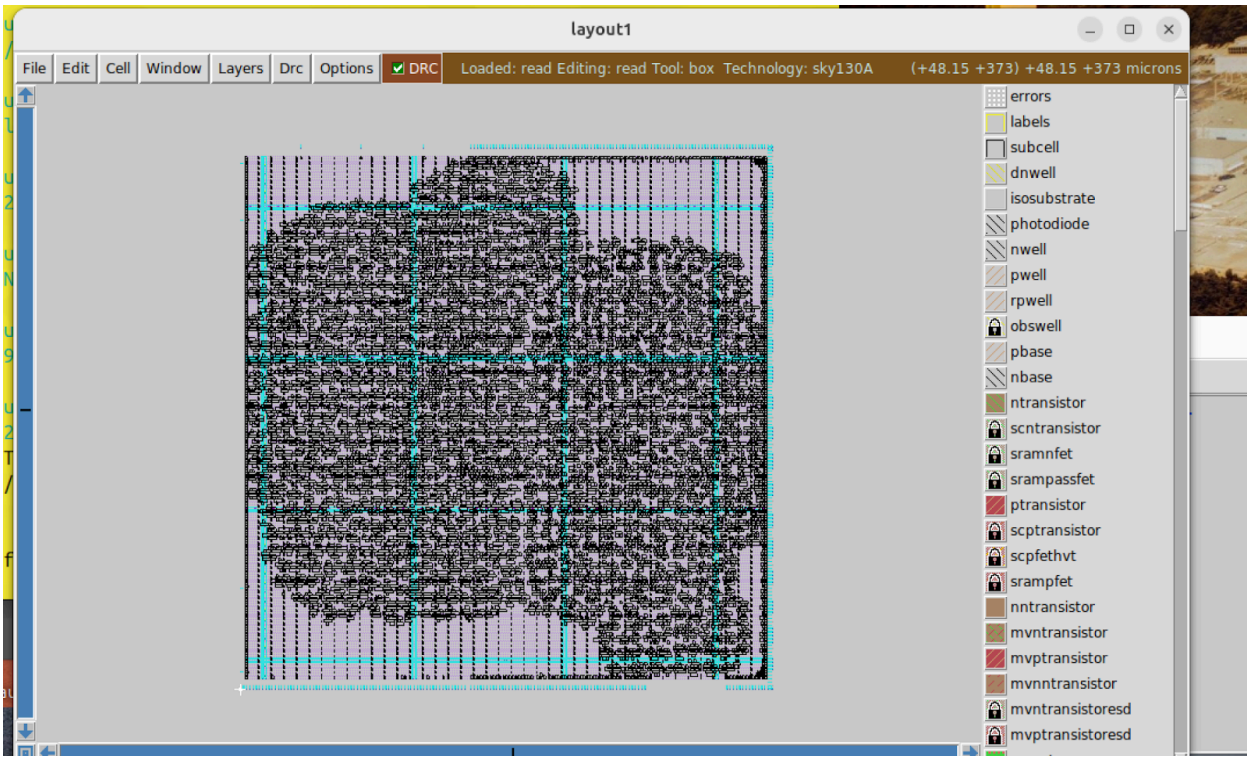
❖ Ls -ltr and the cd into def file

```
-rw-r--r-- 1 root root    51 Jul 14 07:39 PDK_SOURCES
-rw-r--r-- 1 root root   674 Jul 16 12:45 config_in.tcl
drwxr-xr-x 8 root root  4096 Jul 16 12:45 results
drwxr-xr-x 8 root root  4096 Jul 16 12:45 reports
drwxr-xr-x 8 root root  4096 Jul 16 12:45 logs
-rw-r--r-- 1 root root    50 Jul 16 12:45 OPENLANE_VERSION
-rw-r--r-- 1 root root   254 Jul 16 12:45 warnings.log
drwxr-xr-x 8 root root  4096 Jul 16 12:45 tmp
-rw-r--r-- 1 root root  1371 Jul 16 12:45 openlane.log
-rw-r--r-- 1 root root  7636 Jul 16 12:45 cmds.log
-rw-r--r-- 1 root root   572 Jul 16 12:45 runtime.yaml
-rw-r--r-- 1 root root 18862 Jul 16 12:45 config.tcl
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/
picorv32a/runs/RUN_2025.07.16_19.45.14$ cd results/floorplan/
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/
picorv32a/runs/RUN_2025.07.16_19.45.14/results/floorplan$ ls -ltr
total 9536
-rw-r--r-- 1 root root 7778272 Jul 16 12:45 picorv32.odb
-rw-r--r-- 1 root root 1984977 Jul 16 12:45 picorv32.def
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/
picorv32a/runs/RUN_2025.07.16_19.45.14/results/floorplan$ less picorv32.def
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/designs/ci/
picorv32a/runs/RUN_2025.07.16_19.45.14/results/floorplan$
```



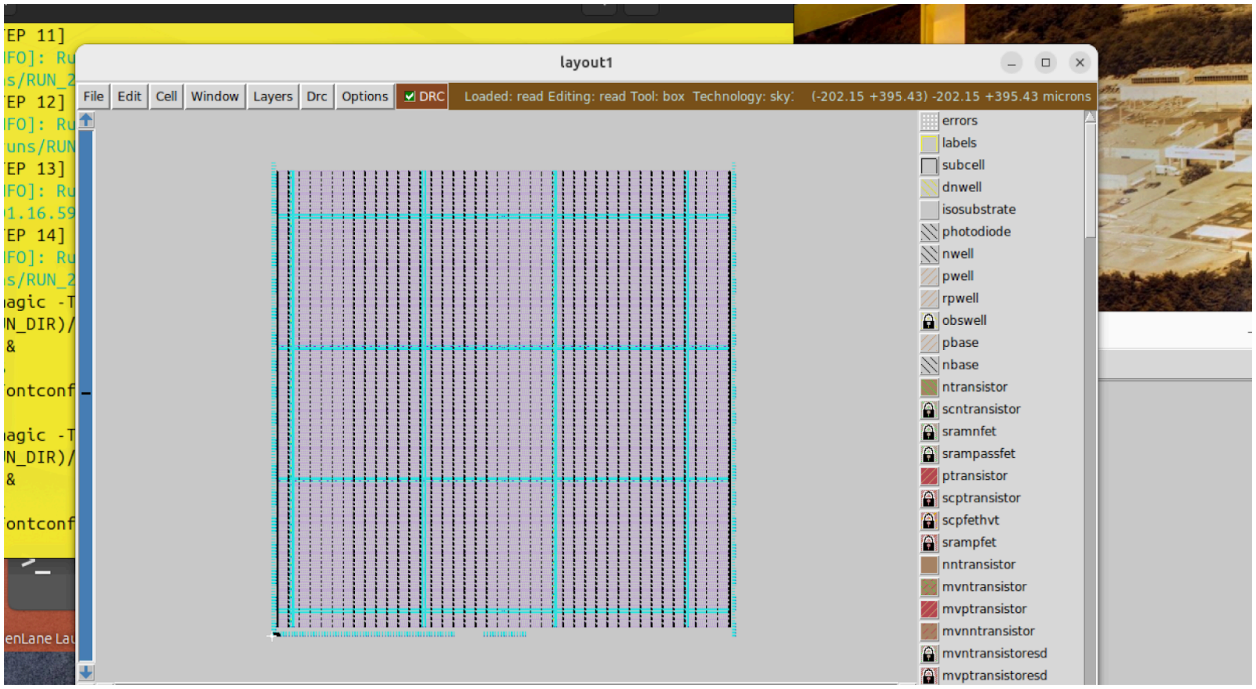
- Go through the whole flow tcl platform then run_synthesis, run_floorplan, run_placement, and then `magic -T $env(PDK_ROOT)/$env(PDK)/libs.tech/magic/$env(PDK).tech lef read $env(RUN_DIR)/tmp/merged.nom.lef def read $env(RUN_DIR)/results/placement/picorv32.def &`

- (placement output)



- With this command instead : magic -T $env(PDK_ROOT)/$env(PDK)/libs.tech/magic/$env(PDK).tech lef read $env(RUN_DIR)/tmp/merged.nom.lef def read $env(RUN_DIR)/results/floorplan/picorv32.def &

(floorplan output)



- S to select entire die, V to center view, Z to zoom
-
```
select: Topmost cell in the window
% what
Selected mask layers:
    metal3   ( Topmost cell in the window )
Selected label(s):
    "mem_la_addr[27]" is attached to metal3 in cell def picorv32
%
```
- select and what
-

Library Binding and Placement

Netlist binding and initial place design

- Bind netlist w/ physical cells (gates are not actually weird shapes like in a schematic - they're usually square/rectangle) - the blocks are sourced from library which includes shapes, delay info, size and other info

Optimize placement using estimated wire-length and capacitance

- Estimate wire length and capacitance to know where to insert repeaters (which recondition the same signal to be original strength, buffer)

Library characterization and modelling

- steps : logic synth, floor planning, placement, CTS, routing,

Cell design and characterization flows

Inputs for cell design flow

- Library is where u keep standard cells(and,or, buffer etc)
- Library has diff size of same functionality
- Library has cells of diff voltage too
- Cell design flow - inputs, design steps, output
- Inputs - pdks: drc and lvs rules, spice models, library and user-defined specs

Circuit design step and Layout design step

- Design Steps (circuit design - euler's path and stick diagram, layout design - pmos nmos network graph, draw stick diagram, characterization)
- Output (CDL, GDSII, lef - width and hight of cell, timing, noise, etc.)

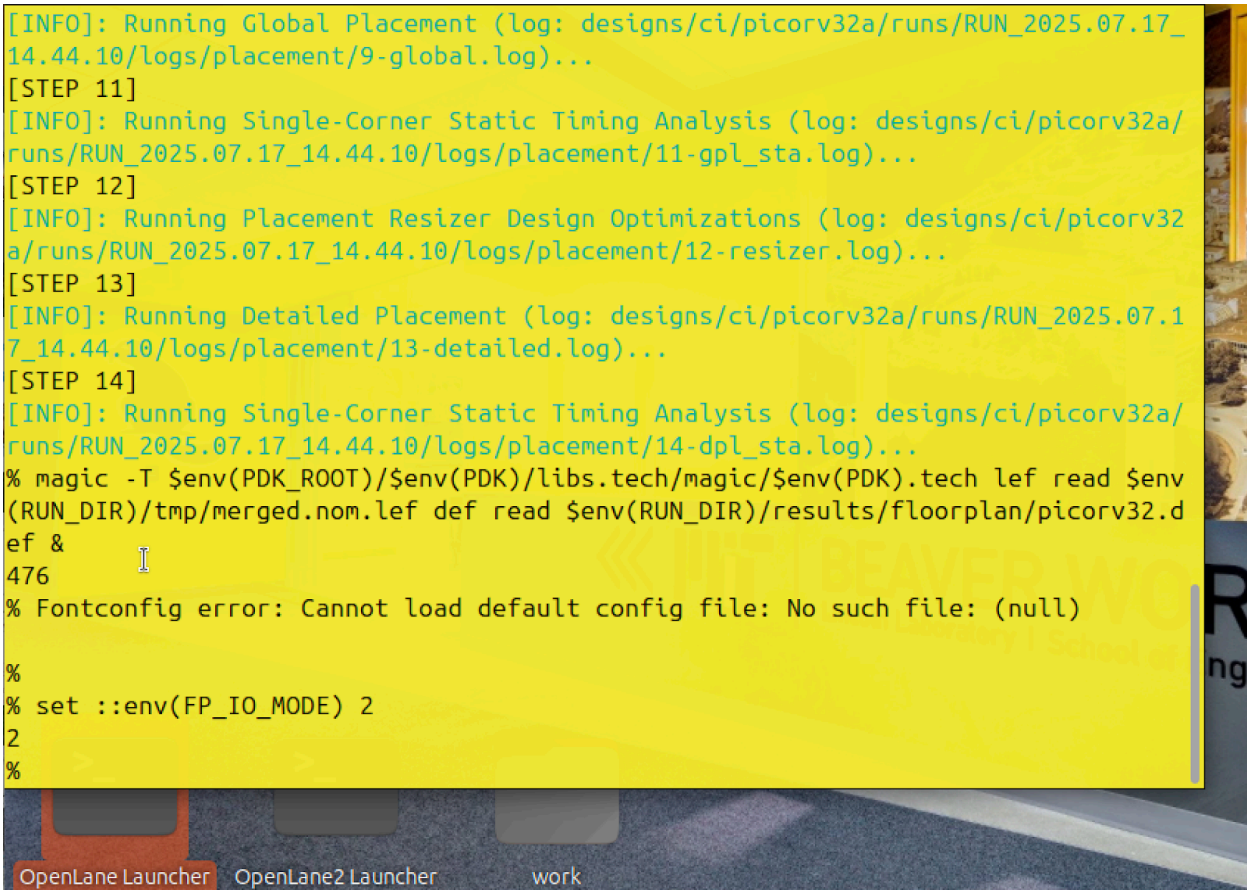
Typical characterization flows

- 1 - Reading of SPICE module files
- 2 - Reading of netlist extracted by SPICE
- 3 - Recognising buffer behaviour
- 4 - Reading subcircuits
- 5 - Attaching necessary power sources
- 6 - Applying stimulus
- 7 - Provision of of necessary output capacitance
- 8 - Provision necessary simulation command
- Feed into GUNA which will model, timing, noise ,power, .libs

General timing char para

- What is slew
- Propagation delay = time(ou_*_thr) - time (in_*_thr)
- The values should be chosen carefully, a neg prop delay can have weird results
- Transition time = time(slew_high_x_thr)-time(slew_low_x_thr)

Diff section



- Then run_flooplan after again

Labs for CMOS inverter ngspice simulations (includes earlier photo)

SPICE deck creation for CMOS inverter + simulation lab + switching thresh

- Create SPICE deck - component connectivity, component values, identify ‘nodes’, name ‘nodes’,
- Starts with *** - means comments
- Steps: 1 - Open the NGSPICE simulator
- 2 - Source the Circuit File through source command
- 3 - Execute it by the command run and then use setplot which allows one to view any plots possible from the simulations specified in the spice deck and will give you a choice for which simulation to be run
- 4 - Then, type display which will give you a choice of nodes to be plotted which when plot out vs in is typed will be plotted on a graph.
- Parameters for robust cmos is switching threshold (where input voltage = output voltage and both NMOS and PMOS are in saturation) and propagation delay

```
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane$ pwd
/home/beaver/Desktop/work/tools/openlane_working_dir/openlane
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane$ git clone https://github.com/nickson-jose/v
sdstdcelldesign.git
Cloning into 'vsdstdcelldesign'...
remote: Enumerating objects: 492, done.
remote: Counting objects: 100% (18/18), done.
remote: Compressing objects: 100% (18/18), done.
remote: Total 492 (delta 7), reused 0 (delta 0), pack-reused 474 (from 1)
Receiving objects: 100% (492/492), 24.08 MiB | 27.00 MiB/s, done.
Resolving deltas: 100% (210/210), done.
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane$ ls -ktr
LICENSE      CONTRIBUTING.md  docs                flake.nix         requirements_lint.txt  dependencies
README.md    configuration    regression_results  flake.lock        requirements_dev.txt   venv
Makefile     AUTHORS.md       klayoutrc           env.py            scripts                install
Jenkinsfile  designs          gui.py              run_designs.py    tests                  vsdstdcelldesign
default.nix  docker           flow.tcl            requirements.txt  empty
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane$ ls -ltr
total 164
-rw-r--r--  1 beaver beaver 11350 Jun 29  2021 LICENSE
-rw-rw-r--  1 beaver beaver  4557 Jul 14 07:34 README.md
-rw-rw-r--  1 beaver beaver  6642 Jul 14 07:34 Makefile
-rw-rw-r--  1 beaver beaver  5209 Jul 14 07:34 Jenkinsfile
-rw-rw-r--  1 beaver beaver  2467 Jul 14 07:34 default.nix
```

❖

```
-rw-rw-r--  1 beaver beaver  2356 Jul 14 07:34 flake.nix
-rw-rw-r--  1 beaver beaver  3162 Jul 14 07:34 flake.lock
-rwxrwxr-x  1 beaver beaver  6983 Jul 14 07:34 env.py
-rwxrwxr-x  1 beaver beaver 16594 Jul 14 07:34 run_designs.py
-rw-rw-r--  1 beaver beaver    74 Jul 14 07:34 requirements.txt
-rw-rw-r--  1 beaver beaver    61 Jul 14 07:34 requirements_lint.txt
-rw-rw-r--  1 beaver beaver    90 Jul 14 07:34 requirements_dev.txt
drwxr-xr-x 13 beaver beaver  4096 Jul 14 07:34 scripts
drwxrwxr-x 23 beaver beaver  4096 Jul 14 07:34 tests
drwxr-xr-x  2 root   root    4096 Jul 14 07:35 empty
drwxrwxr-x  5 beaver beaver  4096 Jul 14 07:35 dependencies
drwxr-xr-x  5 root   root    4096 Jul 14 07:38 venv
drwxr-xr-x  2 root   root    4096 Jul 14 07:40 install
drwxrwxr-x  6 beaver beaver  4096 Jul 17 08:38 vsdstdcelldesign
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane$ cd vsdstdcelldesign/
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 44
drwxrwxr-x 2 beaver beaver  4096 Jul 17 08:38 Images
-rw-rw-r-- 1 beaver beaver 13525 Jul 17 08:38 README.md
-rw-rw-r-- 1 beaver beaver 11357 Jul 17 08:38 LICENSE
drwxrwxr-x 2 beaver beaver  4096 Jul 17 08:38 extras
drwxrwxr-x 2 beaver beaver  4096 Jul 17 08:38 libs
-rw-rw-r-- 1 beaver beaver  2716 Jul 17 08:38 sky130_inv.mag
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```

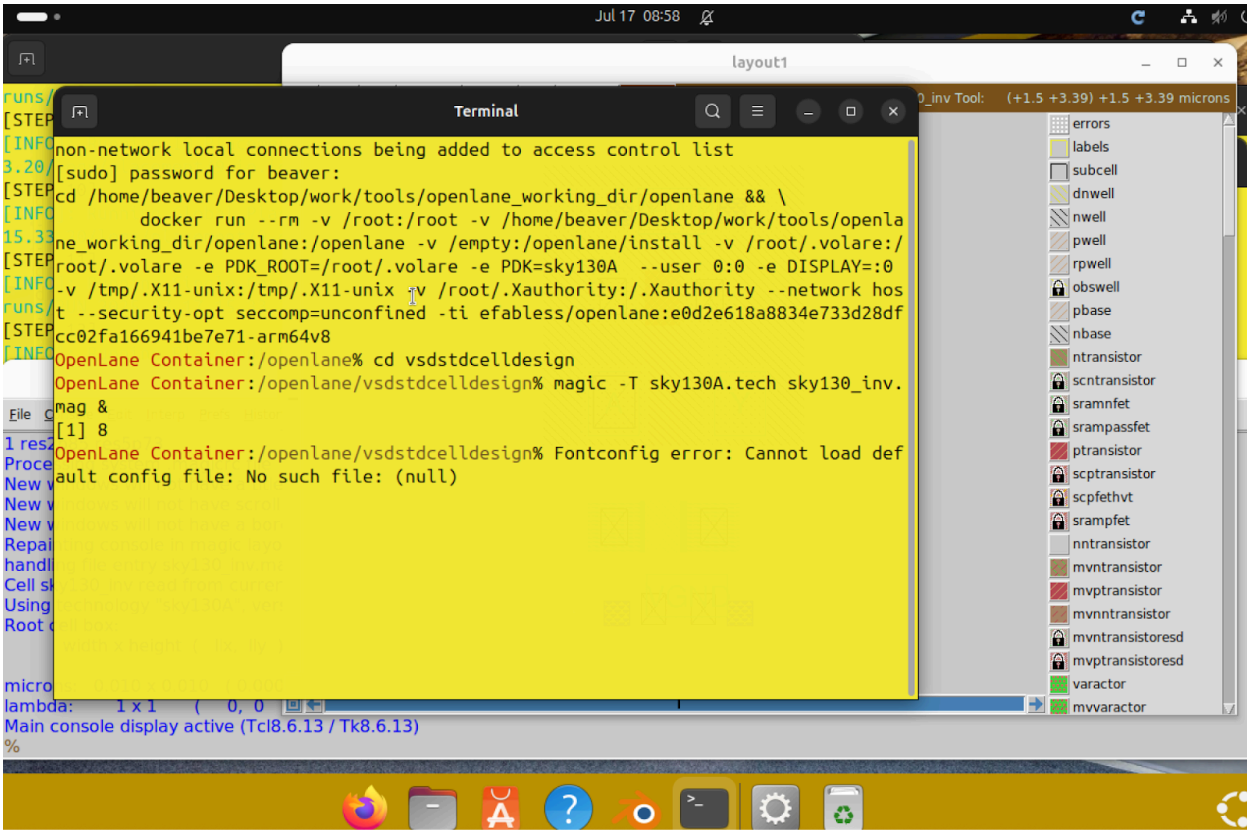
❖

beaver@openlanevm: ~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic

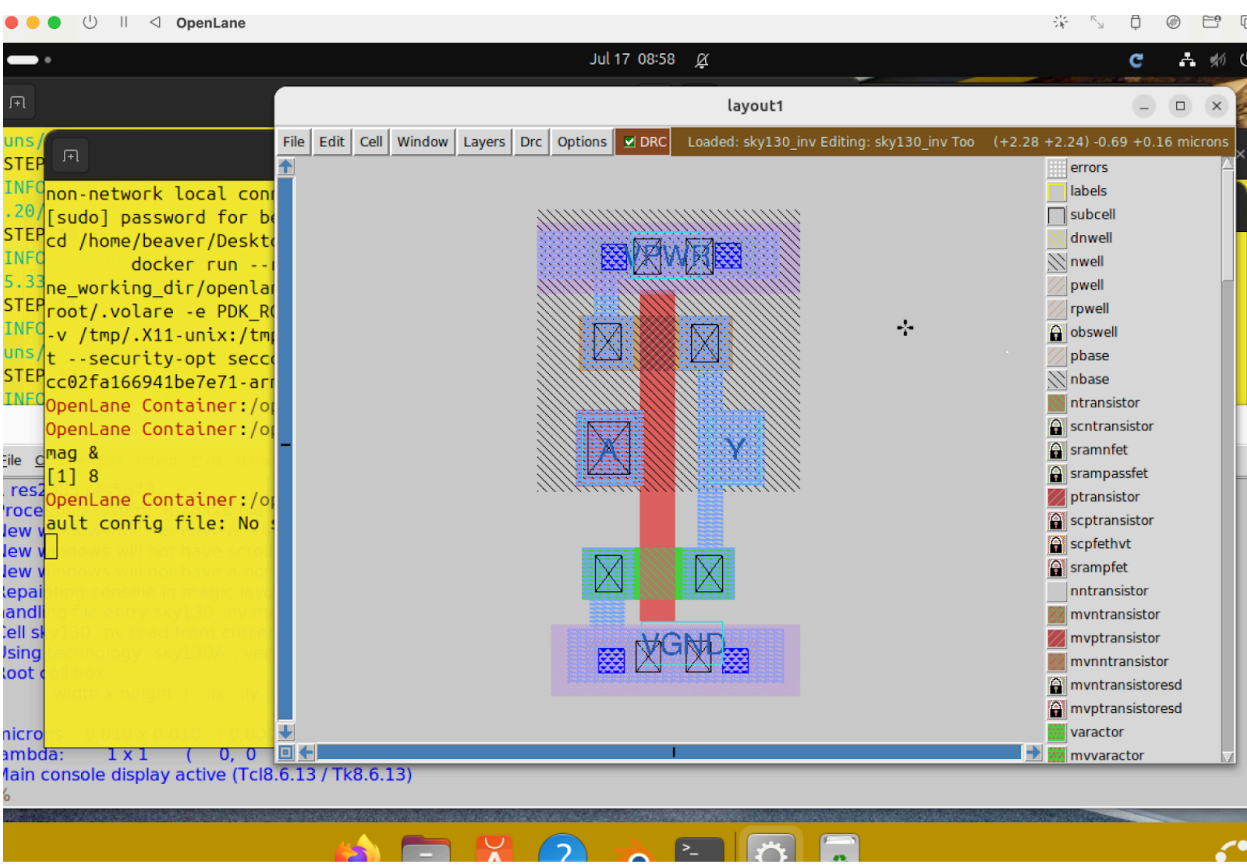
```
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cd ../../
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir$ cd pdks/sky130A/
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A$ ls -ltr
total 12
drwxr-xr-x 11 beaver beaver 4096 Jun 27  2021 libs.tech
drwxr-xr-x 14 beaver beaver 4096 Jun 27  2021 libs.ref
-rwxr-xr-x  1 beaver beaver  170 Jun 27  2021 SOURCES
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A$ cd libs.tech/magic
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic$ ls
bump_bond_generator  seal_ring_generator  sky130A.magicrc
check_density.py     sky130A-BindKeys     sky130A.tcl
generate_fill.py     sky130A-GDS.tech     sky130A.tech
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic$ ls -ltr
total 408
drwxr-xr-x 2 beaver beaver   4096 Jun 27  2021 seal_ring_generator
drwxr-xr-x 2 beaver beaver   4096 Jun 27  2021 bump_bond_generator
-rwxr-xr-x 1 beaver beaver 136710 Jun 27  2021 sky130A.tech
-rwxr-xr-x 1 beaver beaver 203669 Jun 27  2021 sky130A.tcl
-rwxr-xr-x 1 beaver beaver   3013 Jun 27  2021 sky130A.magicrc
-rwxr-xr-x 1 beaver beaver  11471 Jun 27  2021 sky130A-GDS.tech
-rwxr-xr-x 1 beaver beaver   5098 Jun 27  2021 sky130A-BindKeys
-rwxr-xr-x 1 beaver beaver  15144 Jun 27  2021 generate_fill.py
-rwxr-xr-x 1 beaver beaver  21168 Jun 27  2021 check_density.py
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic$ cp sky130A.tech
/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldebebebebebebebebebebebebebebebebebebe
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic$
-rw-rw-r-- 1 beaver beaver   2716 Jul 17 08:38 sky130_inv.mag
```

beaver@openlanevm: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign

```
drwxr-xr-x  5 root   root    4096 Jul 14 07:38 venv
drwxr-xr-x  2 root   root    4096 Jul 14 07:40 install
drwxrwxr-x  6 beaver beaver  4096 Jul 17 08:38 vsdstdcelldesign
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane$ cd vsdstdcelldesign/
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 44
drwxrwxr-x 2 beaver beaver  4096 Jul 17 08:38 Images
-rw-rw-r-- 1 beaver beaver 13525 Jul 17 08:38 README.md
-rw-rw-r-- 1 beaver beaver 11357 Jul 17 08:38 LICENSE
drwxrwxr-x 2 beaver beaver  4096 Jul 17 08:38 extras
drwxrwxr-x 2 beaver beaver  4096 Jul 17 08:38 libs
-rw-rw-r-- 1 beaver beaver  2716 Jul 17 08:38 sky130_inv.mag
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ pwd
/home/beaver/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 180
drwxrwxr-x 2 beaver beaver   4096 Jul 17 08:38 Images
-rw-rw-r-- 1 beaver beaver  13525 Jul 17 08:38 README.md
-rw-rw-r-- 1 beaver beaver  11357 Jul 17 08:38 LICENSE
drwxrwxr-x 2 beaver beaver   4096 Jul 17 08:38 extras
drwxrwxr-x 2 beaver beaver   4096 Jul 17 08:38 libs
-rw-rw-r-- 1 beaver beaver   2716 Jul 17 08:38 sky130_inv.mag
-rwxr-xr-x 1 beaver beaver 136710 Jul 17 08:47 sky130A.tech
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```


Jul 17 08:58
layout1
Terminal
non-network local connections being added to access control list
[sudo] password for beaver:
cd /home/beaver/Desktop/work/tools/openlane_working_dir/openlane && \
docker run --rm -v /root:/root -v /home/beaver/Desktop/work/tools/openlane_working_dir/openlane:/openlane -v /empty:/openlane/install -v /root/.volare:/root/.volare -e PDK_ROOT=/root/.volare -e PDK=sky130A --user 0:0 -e DISPLAY=:0 -v /tmp/.X11-unix:/tmp/.X11-unix -v /root/.Xauthority:/.Xauthority --network host --security-opt seccomp=unconfined -ti efabless/openlane:e0d2e618a8834e733d28dfcc02fa166941be7e71-arm64v8
OpenLane Container:/openlane% cd vsdstdcelldesign
OpenLane Container:/openlane/vsdstdcelldesign% magic -T sky130A.tech sky130_inv.mag &
[1] 8
OpenLane Container:/openlane/vsdstdcelldesign% Fontconfig error: Cannot load default config file: No such file: (null)
(+1.5 +3.39) +1.5 +3.39 microns
Main console display active (Tcl8.6.13 / Tk8.6.13)

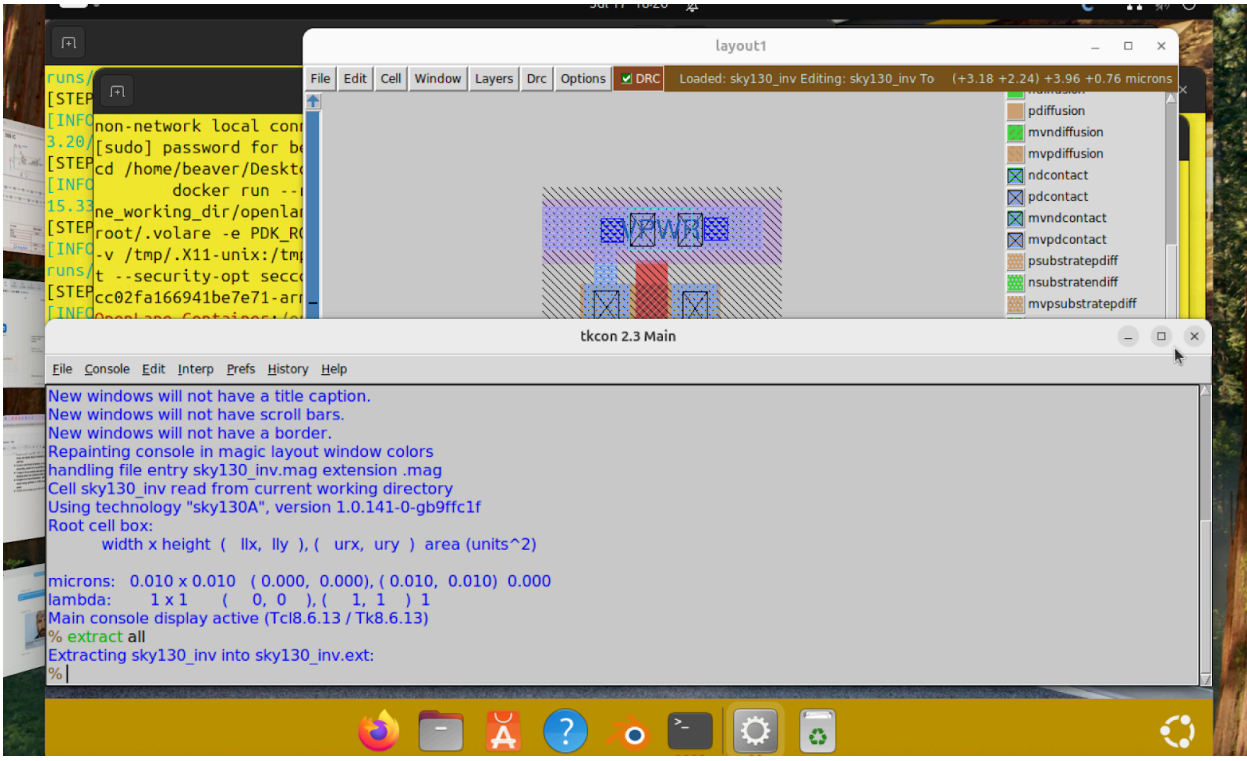
❖

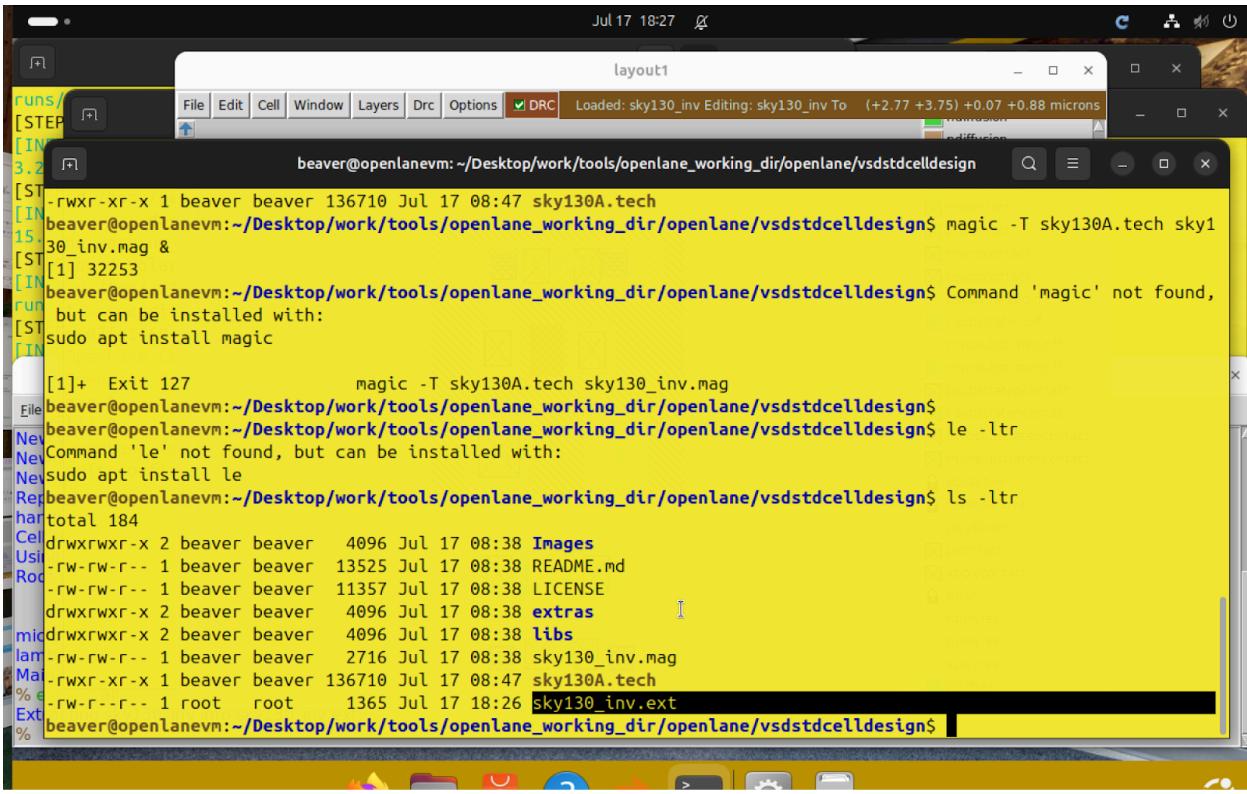

OpenLane
Jul 17 08:58
layout1
File Edit Cell Window Layers Drc Options DRC
Loaded: sky130_inv Editing: sky130_inv Too
(+2.28 +2.24) -0.69 +0.16 microns
VPWR
A
Y
VGND
Main console display active (Tcl8.6.13 / Tk8.6.13)

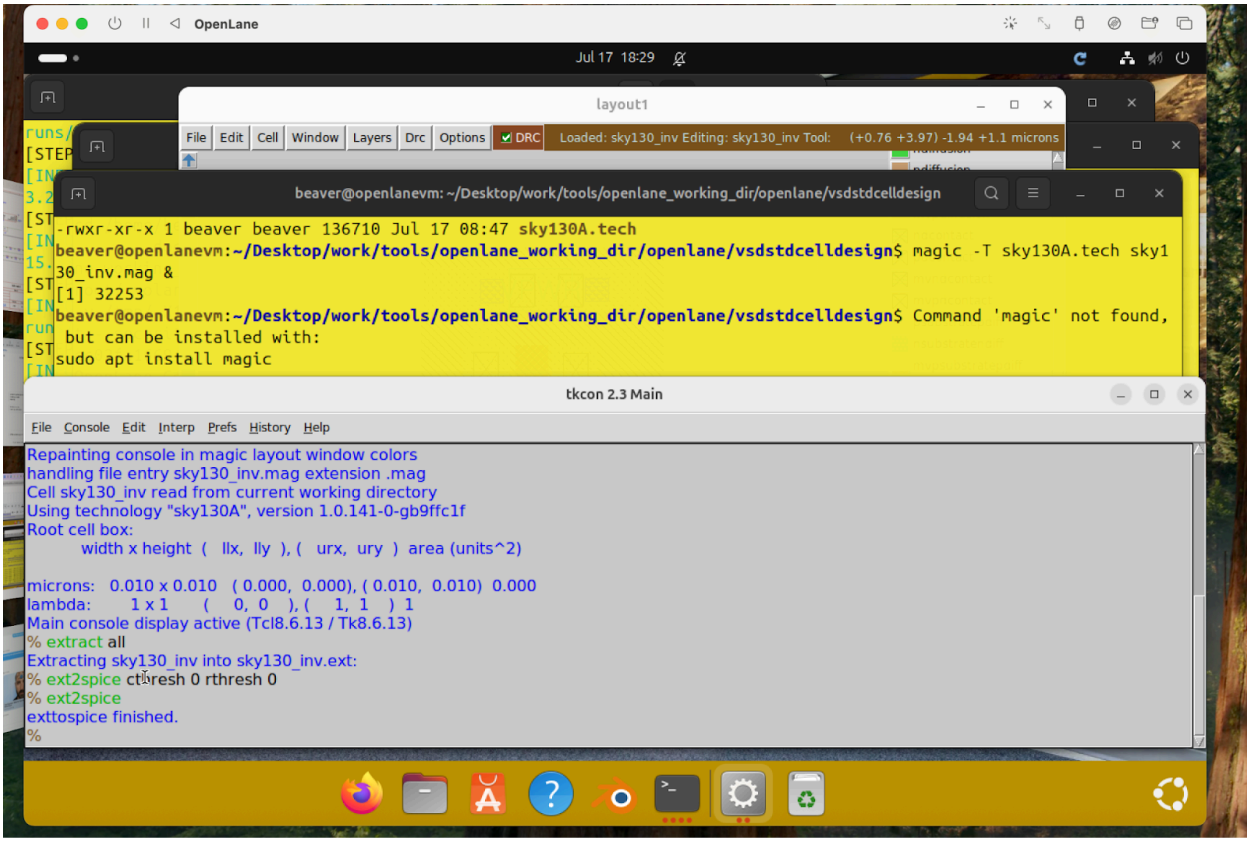
❖

Inception of Layout

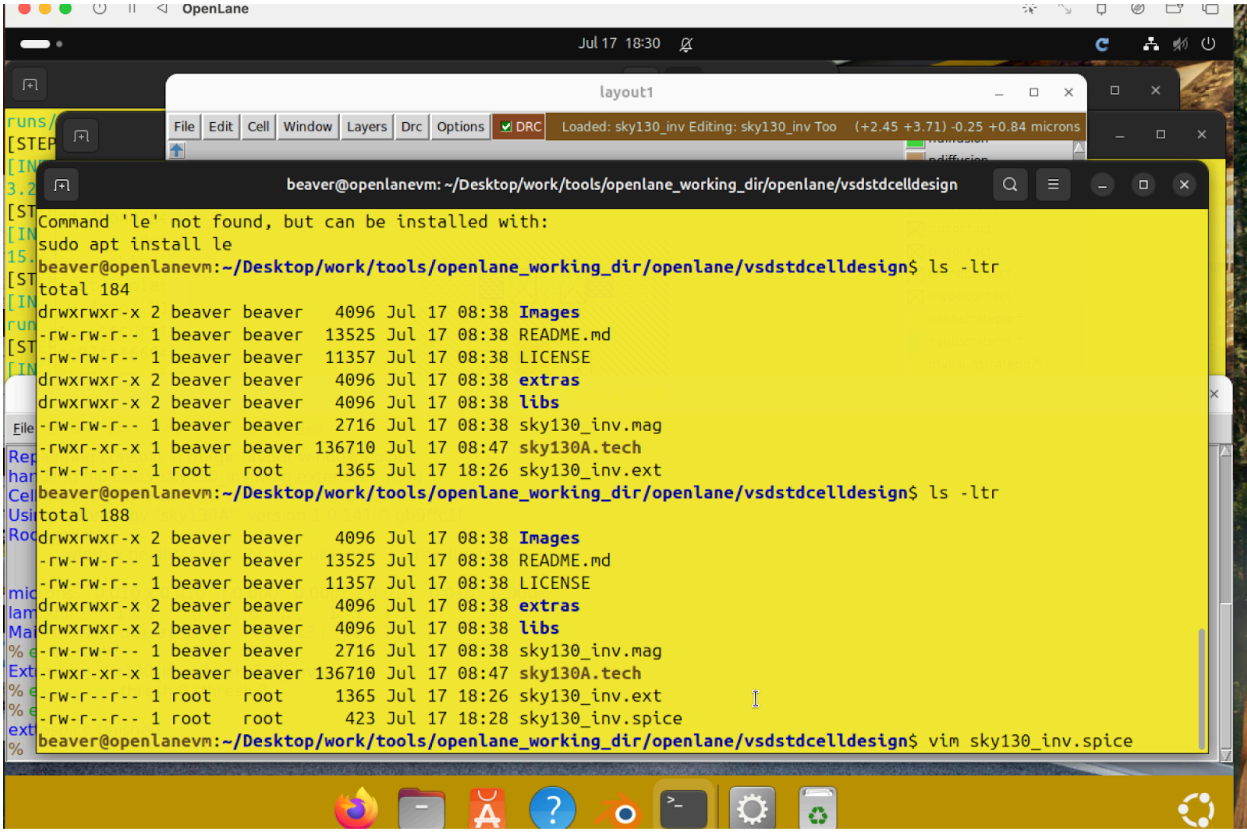
- **16-mask process**
- **1) Selecting a substrate - most common (p-type), less doped than wells**
- **2) Create active region for transistors - create isolation between each pocket (silicon dioxide, silicon nitride, photoresist, mask-1 layer, apply uv light, remover mask 1 and photoresist, put chip in furnace, remove silicon nitride)**
- **3)N-Well and P-Well Formation - photoresist, mask2 (n-well/pmos side), mask 3 (p-well/nmos side)**
- **4) Formation of Gate - most important terminal, where threshold voltage is controlled, - mask 4, implant low energy boron at p-well, implant phosphorous using mask 5 for n-well, fix damage by removing and regrowing SiO2, add polysilicon, mask6**
- **5? Lightly doped drain (LDD) formation - created to prevent hot electron so it cant break Si bond or create voltage, also to prevent short channel effect - mask7(nmos), mask8(pmos), heavy dope to source and drain, also lightly dope to maintain spac between source drain, als o add Sio2**
- **6) source and drain formation - screen oxide is added to avoid channeling, mask9 (n+), mask10(p+), high temp annealing**
- **7) steps to form contacts and interconnects - remove thin oxide, deposit titanium (since less resistance) thru sputtering, mask 11**
- **8) higher level metal formation - thick layer of sio2, doped (boron reduce temp), polished w/ CMP, create contact holes, use multiple masks**
- To find error on magic- go to drc and find error


layout1
File Edit Cell Window Layers Drc Options DRC Loaded: sky130_inv Editing: sky130_inv To (+3.18 +2.24) +3.96 +0.76 microns
pdiffusion
mvndiffusion
mvpdiffusion
ndcontact
pdcontact
mvndcontact
mvpdcontact
psubstratepdiff
nsubstratendiff
mvpsubstratepdiff
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
New windows will not have a title caption.
New windows will not have scroll bars.
New windows will not have a border.
Repainting console in magic layout window colors
handling file entry sky130_inv.mag extension .mag
Cell sky130_inv read from current working directory
Using technology "sky130A", version 1.0.141-0-gb9ffc1f
Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)
microns: 0.010 x 0.010 (0.000, 0.000), (0.010, 0.010) 0.000
lambda: 1 x 1 (0, 0), (1, 1) 1
Main console display active (Tcl8.6.13 / Tk8.6.13)
% extract all
Extracting sky130_inv into sky130_inv.ext:
%


Jul 17 18:27
layout1
File Edit Cell Window Layers Drc Options DRC Loaded: sky130_inv Editing: sky130_inv To (+2.77 +3.75) +0.07 +0.88 microns
beaver@openlanevm: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
-rwxr-xr-x 1 beaver beaver 136710 Jul 17 08:47 sky130A.tech
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ magic -T sky130A.tech sky130_inv.mag &
[1] 32253
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ Command 'magic' not found, but can be installed with:
sudo apt install magic
[1]+ Exit 127 magic -T sky130A.tech sky130_inv.mag
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ le -ltr
Command 'le' not found, but can be installed with:
sudo apt install le
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 184
drwxrwxr-x 2 beaver beaver 4096 Jul 17 08:38 Images
-rw-rw-r-- 1 beaver beaver 13525 Jul 17 08:38 README.md
-rw-rw-r-- 1 beaver beaver 11357 Jul 17 08:38 LICENSE
drwxrwxr-x 2 beaver beaver 4096 Jul 17 08:38 extras
drwxrwxr-x 2 beaver beaver 4096 Jul 17 08:38 libs
-rw-rw-r-- 1 beaver beaver 2716 Jul 17 08:38 sky130_inv.mag
-rwxr-xr-x 1 beaver beaver 136710 Jul 17 08:47 sky130A.tech
-rw-r--r-- 1 root root 1365 Jul 17 18:26 sky130_inv.ext
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$

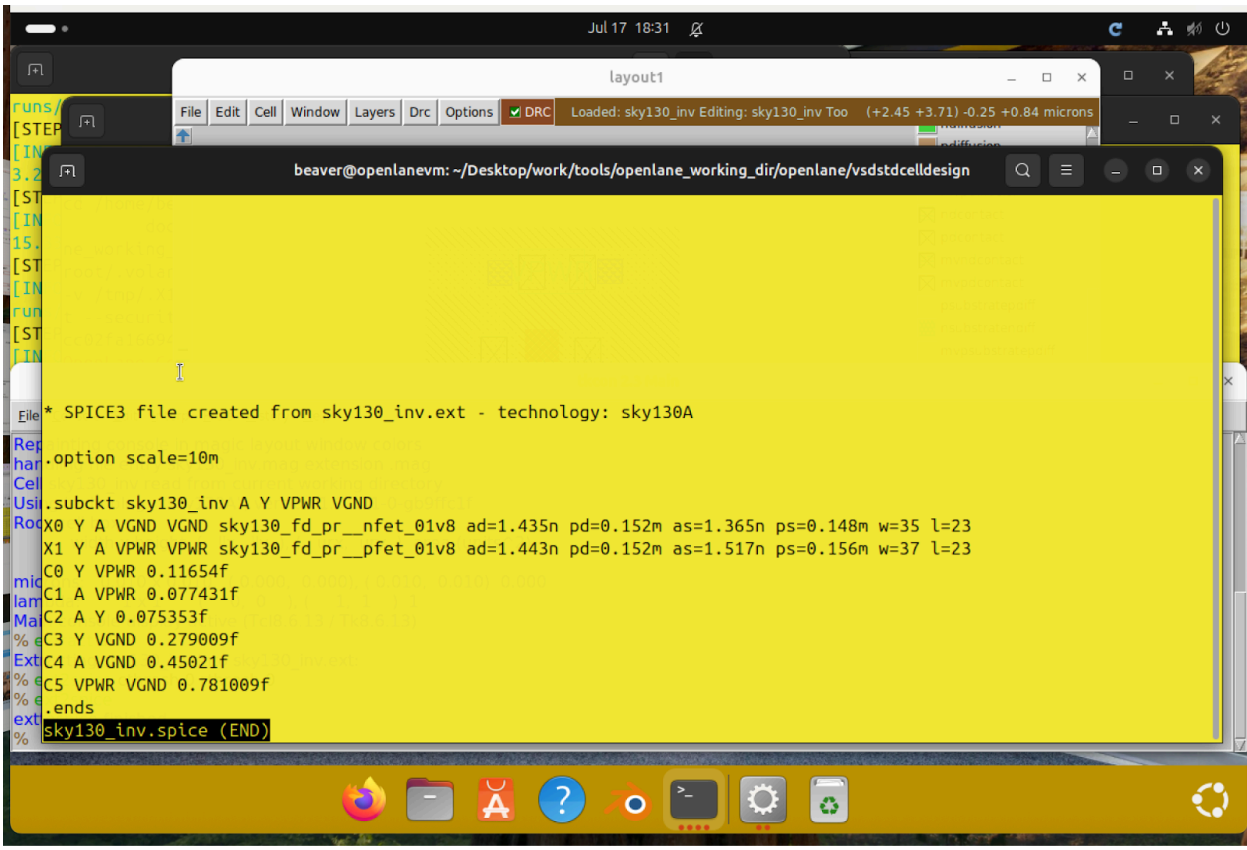

OpenLane
Jul 17 18:29
layout1
File Edit Cell Window Layers Drc Options DRC Loaded: sky130_inv Editing: sky130_inv Tool: (+0.76 +3.97) -1.94 +1.1 microns
beaver@openlanevm: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
-rwxr-xr-x 1 beaver beaver 136710 Jul 17 08:47 sky130A.tech
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ magic -T sky130A.tech sky130_inv.mag &
[1] 32253
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ Command 'magic' not found, but can be installed with:
sudo apt install magic
tkcon 2.3 Main
File Console Edit Interp Prefs History Help
Repainting console in magic layout window colors
handling file entry sky130_inv.mag extension .mag
Cell sky130_inv read from current working directory
Using technology "sky130A", version 1.0.141-0-gb9ffc1f
Root cell box:
width x height (llx, lly), (urx, ury) area (units^2)
microns: 0.010 x 0.010 (0.000, 0.000), (0.010, 0.010) 0.000
lambda: 1 x 1 (0, 0), (1, 1) 1
Main console display active (Tcl8.6.13 / Tk8.6.13)
% extract all
Extracting sky130_inv into sky130_inv.ext:
% ext2spice cthresh 0 rthresh 0
% ext2spice
exttospice finished.
%

❖


OpenLane
Jul 17 18:30
layout1
File Edit Cell Window Layers Drc Options DRC Loaded: sky130_inv Editing: sky130_inv Too (+2.45 +3.71) -0.25 +0.84 microns
beaver@openlanevm: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
Command 'le' not found, but can be installed with:
sudo apt install le
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 184
drwxrwxr-x 2 beaver beaver 4096 Jul 17 08:38 Images
-rw-rw-r-- 1 beaver beaver 13525 Jul 17 08:38 README.md
-rw-rw-r-- 1 beaver beaver 11357 Jul 17 08:38 LICENSE
drwxrwxr-x 2 beaver beaver 4096 Jul 17 08:38 extras
drwxrwxr-x 2 beaver beaver 4096 Jul 17 08:38 libs
-rw-rw-r-- 1 beaver beaver 2716 Jul 17 08:38 sky130_inv.mag
-rwxr-xr-x 1 beaver beaver 136710 Jul 17 08:47 sky130A.tech
-rw-r--r-- 1 root root 1365 Jul 17 18:26 sky130_inv.ext
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 188
drwxrwxr-x 2 beaver beaver 4096 Jul 17 08:38 Images
-rw-rw-r-- 1 beaver beaver 13525 Jul 17 08:38 README.md
-rw-rw-r-- 1 beaver beaver 11357 Jul 17 08:38 LICENSE
drwxrwxr-x 2 beaver beaver 4096 Jul 17 08:38 extras
drwxrwxr-x 2 beaver beaver 4096 Jul 17 08:38 libs
-rw-rw-r-- 1 beaver beaver 2716 Jul 17 08:38 sky130_inv.mag
-rwxr-xr-x 1 beaver beaver 136710 Jul 17 08:47 sky130A.tech
-rw-r--r-- 1 root root 1365 Jul 17 18:26 sky130_inv.ext
-rw-r--r-- 1 root root 423 Jul 17 18:28 sky130_inv.spice
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ vim sky130_inv.spice

❖

- Dont do vim like the photo above, do sudo nano sky(etc)



- extract all
- ext2spice cthresh 0 rthresh 0 --> This extracts the parasitic information
- Ext2spice

```
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelld
esign$ cd libs
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelld
esign/libs$ less pshort.lib
```

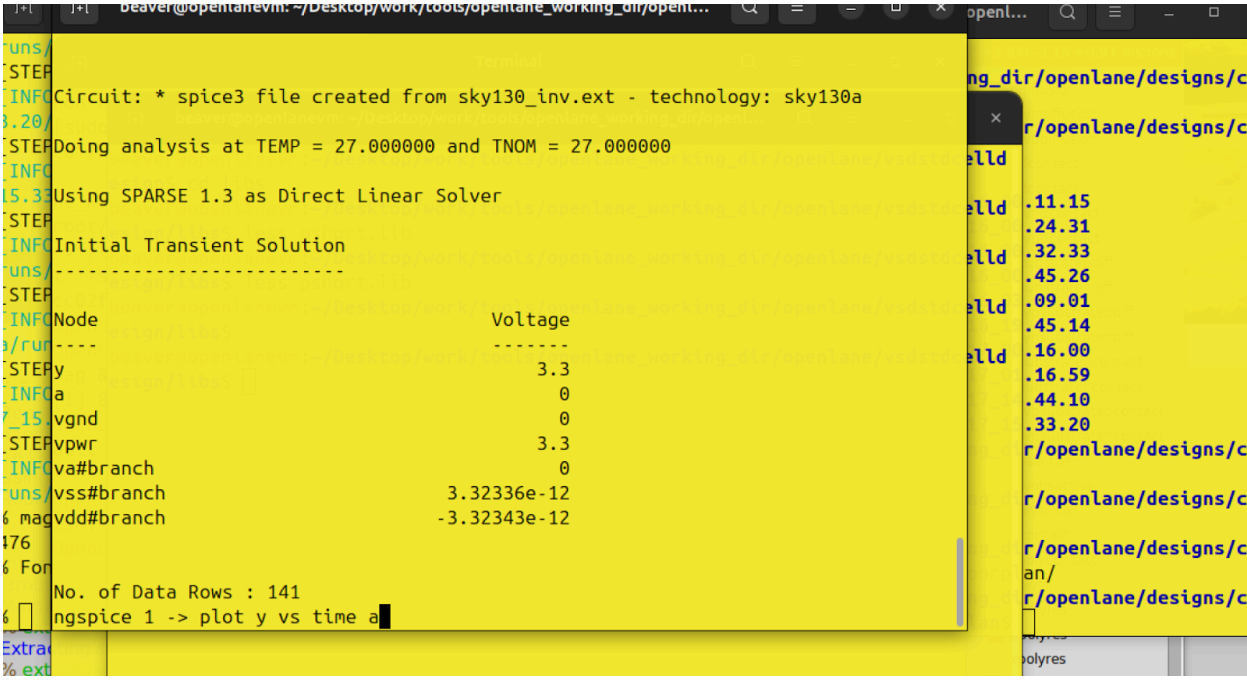
beaver@openlanevm: ~/Desktop/work/tools/openlane_working_dir/openl...

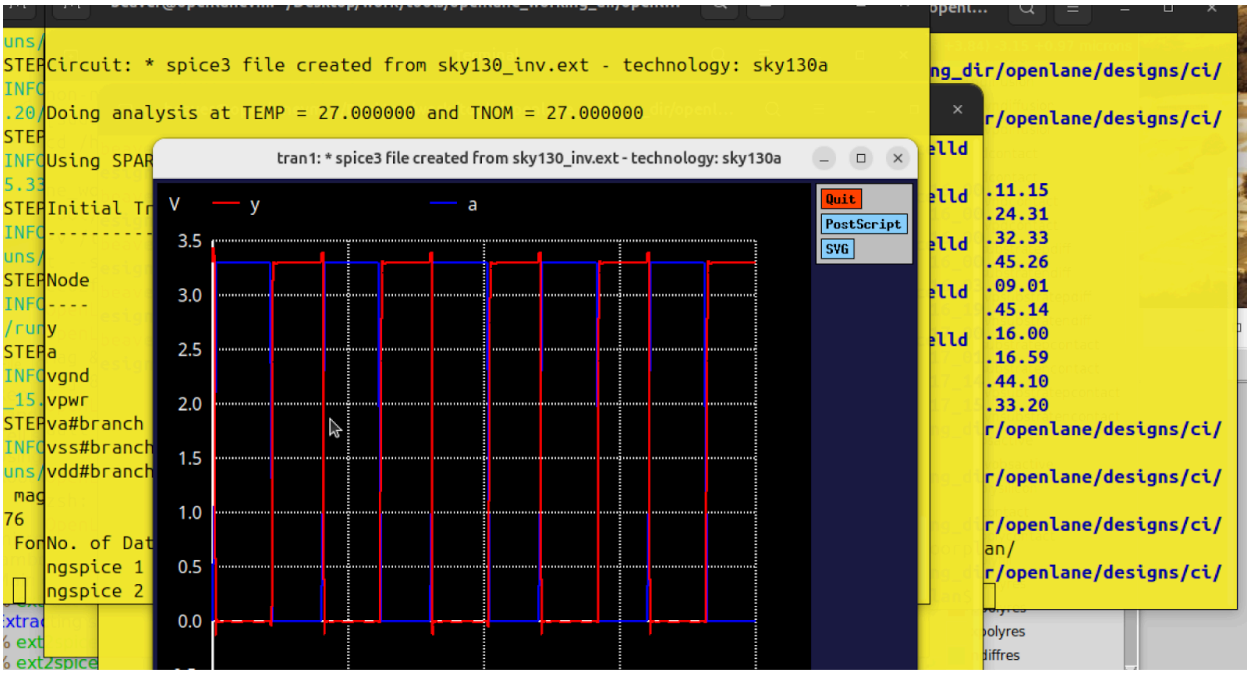
```
* Copyright 2020 The SkyWater PDK Authors
*
* Licensed under the Apache License, Version 2.0 (the "License");
* you may not use this file except in compliance with the License.
* You may obtain a copy of the License at
*
*     https://www.apache.org/licenses/LICENSE-2.0
*
* Unless required by applicable law or agreed to in writing, software
* distributed under the License is distributed on an "AS IS" BASIS,
* WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
* See the License for the specific language governing permissions and
* limitations under the License.
*
* SPDX-License-Identifier: Apache-2.0
*Auto-converted ../spectremodels/pshort.pm3 by model_spectre_mismatchmaker.rb
//  converted from amsmodels_s8x/pshort.pm3
*simulator lang=spectre
//  BSIMTran Version 0.1.24, Created on 4-26-2002
//  Username: hai
//  Command Line: /home/hai/config/cydir/bin/lnx86/bsimtran pmos_bsim4.rf pmos -
p -npshort pshort_modelnamechanged.pm3 pshort-overlap.pm PDIV1.PMD pdcv1.pm psho
rt_bsimtranoutput.pm3
:
```

❖

```
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelld
esign$ sudo nano sky130_inv.spice
beaver@openlanevm:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelld
esign$ ngspice sky130_inv.spice
******
** ngspice-42 : Circuit level simulation program
** Compiled with KLU Direct Linear Solver
** The U. C. Berkeley CAD Group
** Copyright 1985-1994, Regents of the University of California.
** Copyright 2001-2023, The ngspice team.
** Please get your ngspice manual from https://ngspice.sourceforge.io/docs.html
** Please file your bug-reports at http://ngspice.sourceforge.net/bugrep.html
** Creation Date: Sun Mar 31 20:15:14 UTC 2024
******

Note: No compatibility mode selected!


Circuit: * spice3 file created from sky130_inv.ext - technology: sky130a

Doing analysis at TEMP = 27.000000 and TNOM = 27.000000
```

❖

❖ 

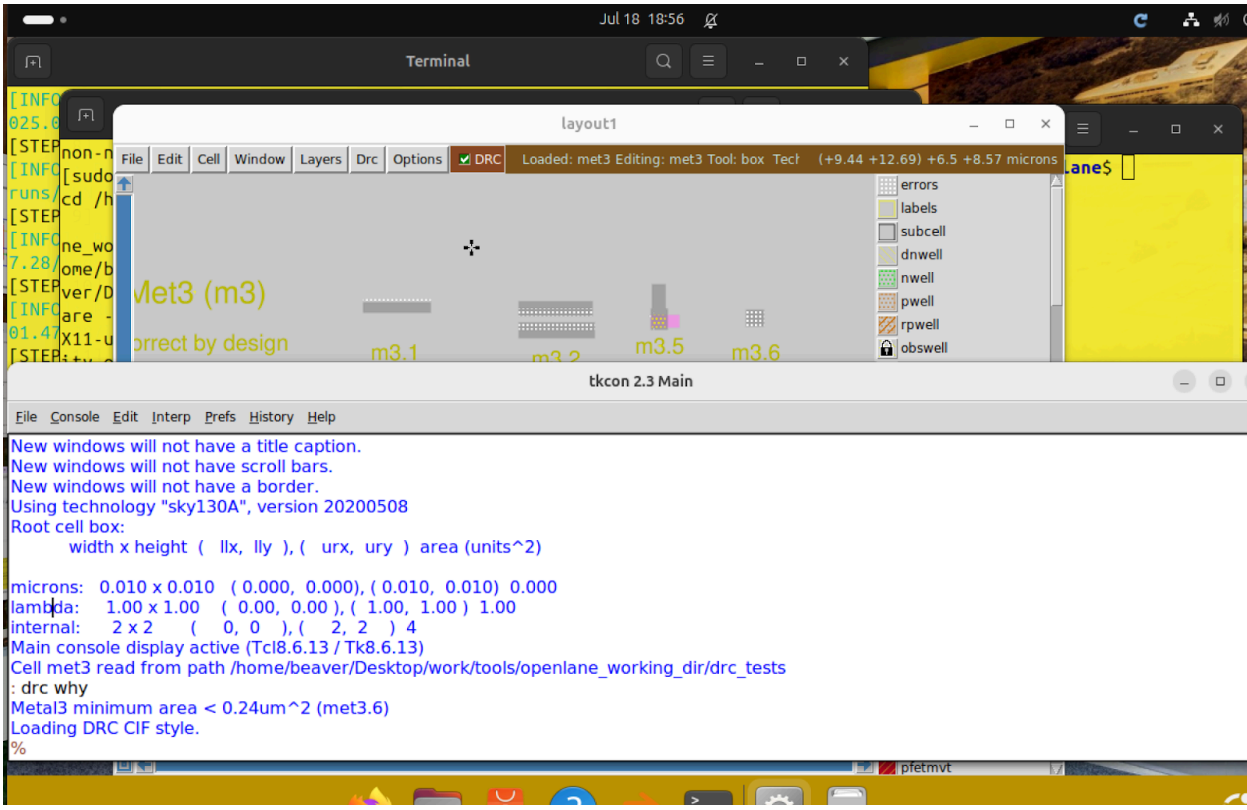
❖ 

❖ Type exit to leave ngspice

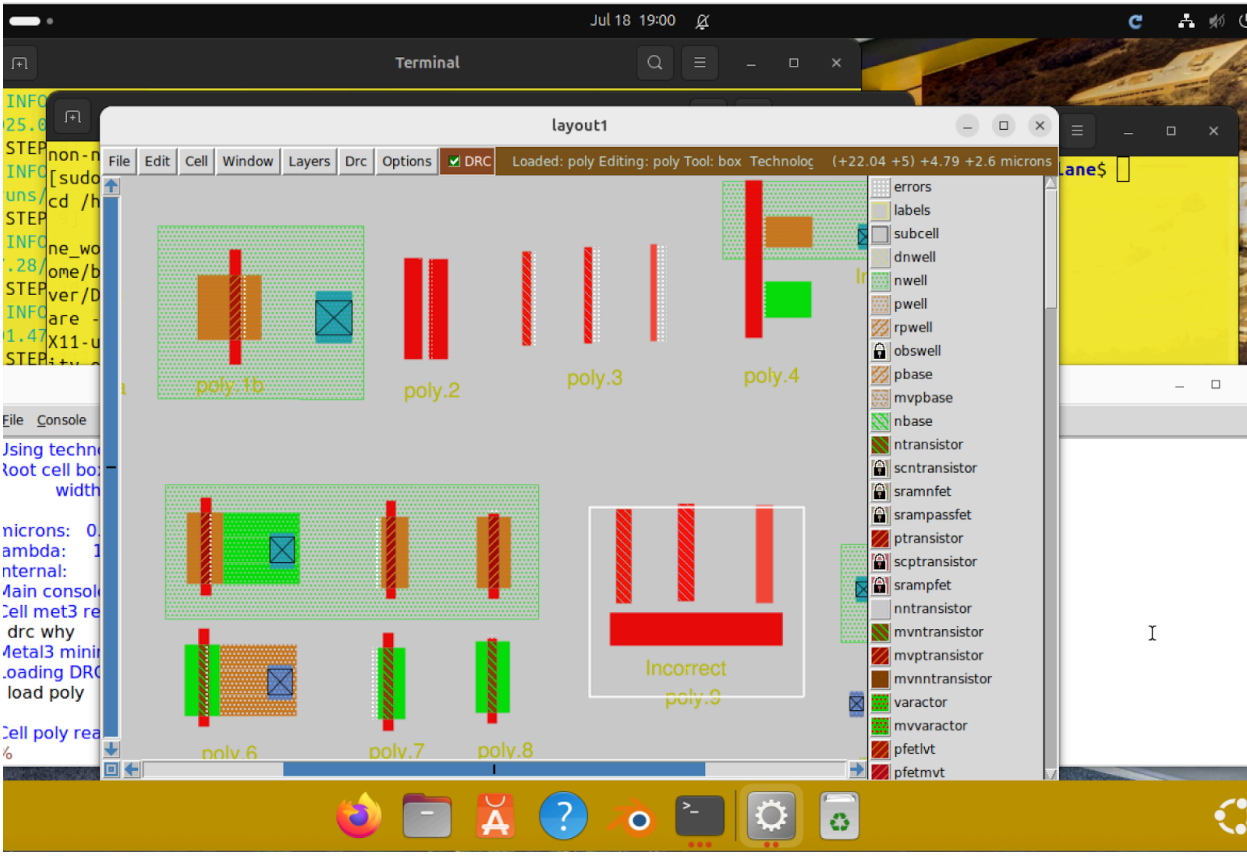
❖ go into the directory by *cd drc_tests* and then list the contents through *ls -al*. Then to open the magic tool, type *magic -d XR*

```
X11-unix:/tmp/.X11-unix -v /root/.Xauthority:/.Xauthority --network host --secur
ity-opt seccomp=unconfined -ti efabless/openlane:e0d2e618a8834e733d28dfcc02fa166
941be7e71-arm64v8
OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/openlane
% cd ..
OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir% ls
drc_tests  drc_tests.tgz  openlane  openlane2  openlane_old  pdks
OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir% cd drc_
tests
OpenLane Container:/home/beaver/Desktop/work/tools/openlane_working_dir/drc_test
s% magic -d XR &
```

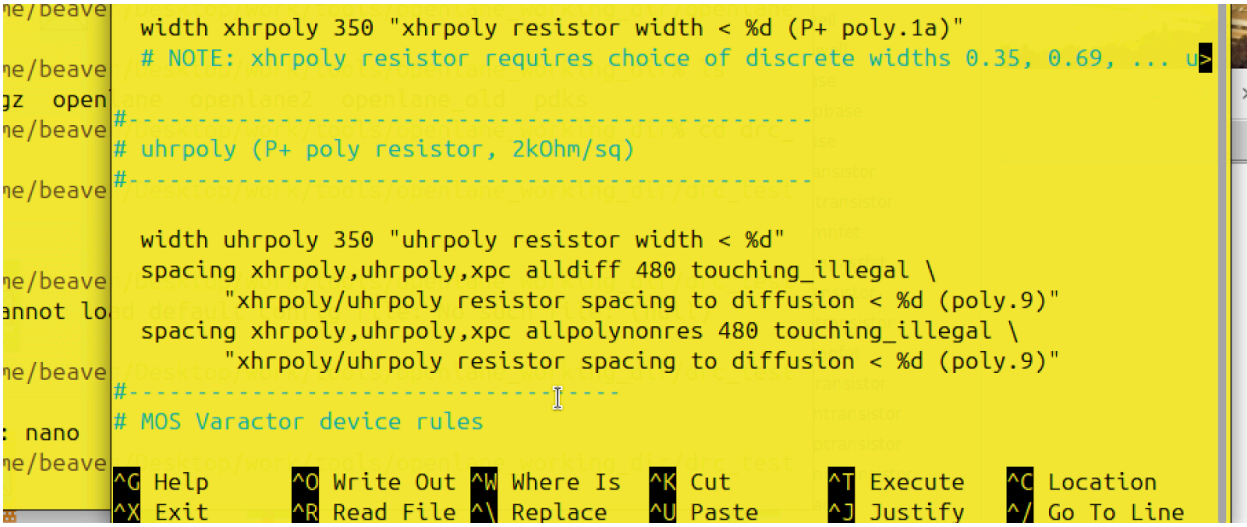
- ❖ : command to type commands while on magic screen



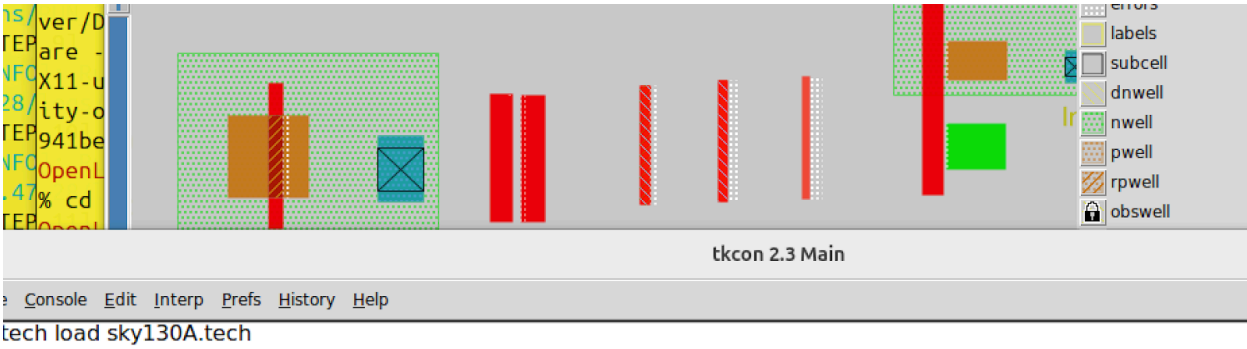
- ❖
- ❖ : box


Jul 18 19:00
Terminal
layout1
File Edit Cell Window Layers Drc Options DRC
Loaded: poly Editing: poly Tool: box Technolog (+22.04 +5) +4.79 +2.6 microns
poly.1b
poly.2
poly.3
poly.4
Incorrect
poly.9
poly.6
poly.7
poly.8
errors
labels
subcell
dnwell
nwell
pwell
rpwell
obswell
pbase
mvpbase
nbase
ntransistor
scntransistor
sramnfet
srampassfet
ptransistor
scptransistor
srampfet
nntransistor
mvntransistor
mvptransistor
mvnntransistor
varactor
mvvaractor
pfetlvt
pfetmvt
File Console
drc why
load poly

❖


width xhrpoly 350 "xhrpoly resistor width < %d (P+ poly.1a)"
NOTE: xhrpoly resistor requires choice of discrete widths 0.35, 0.69, ... u
#----------
uhrpoly (P+ poly resistor, 2kOhm/sq)
#----------
width uhrpoly 350 "uhrpoly resistor width < %d"
spacing xhrpoly,uhrpoly,xpc alldiff 480 touching_illegal \
"xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
spacing xhrpoly,uhrpoly,xpc allpolynonres 480 touching_illegal \
"xhrpoly/uhrpoly resistor spacing to diffusion < %d (poly.9)"
#----------
MOS Varactor device rules
^G Help ^O Write Out ^W Where Is ^K Cut ^T Execute ^C Location
^X Exit ^R Read File ^\ Replace ^U Paste ^J Justify ^/ Go To Line

❖


labels
subcell
dnwell
nwell
pwell
rpwell
obswell
tkcon 2.3 Main
Console Edit Interp Prefs History Help
tech load sky130A.tech
/130A.tech: line 1875: section cifinput:
Labels on layer "DIFF" attached to "mvvaractor" supersedes prior attachment to "nbase".
/130A.tech: line 1876: section cifinput:
Labels on layer "DIFFTXT" attached to "mvvaractor" supersedes prior attachment to "nbase".
/130A.tech: line 1877: section cifinput:
Labels on layer "DIFFPIN" attached to "mvvaractor" supersedes prior attachment to "nbase".
/130A.tech: line 2171: section cifinput:
Labels on layer "TAPPIN" attached to "nsubdiff" supersedes prior attachment to "nbase".
ut style sky130: scaleFactor=2, multiplier=2
e following types are not handled by extraction and will be treated as non-electrical types:
mvpbase nnmos obsactive mvobsactive obsli1 obsli1c obsm1 obsm2 obsm3 obsm4 obsm5 obsmrdl fillblock comme
69 res1p41 res2p85 res5p73
aled tech values by 2 / 1 to match internal grid scaling
sting layout may be invalid.

- drc check

File Edit Cell Window Layers Drc
GNU nano 7.2 sky130A.tech *
POLY
width allpoly 150 "poly.width < %d (poly.1a)"
spacing allpoly allpoly 210 touching_ok "poly.spacing < %d (poly.2)"
spacing allpolynonfet alldifflvnonfet 75 corner_ok allfets \
"poly.spacing to Diffusion < %d (poly.4a)"
spacing npres alldiff 480 touching_illegal \
"poly.resistor spacing to N-tap < %d (poly.9)"
spacing npres allpolynonres 480 touching_illegal \
"poly.resistor spacing to N-tap < %d (poly.9)"
overhang *ndiff,rndiff nfet,scnfet,npd,npass 250 "N-Diffusion overhang of nmos
overhang *mvndiff,mvrndiff mvnfet,mvnnfet 250 \
"N-Diffusion overhang of nmos < %d (poly.7)"
overhang *pdiff,rpdiff pfet,scpfet,ppu 250 "P-Diffusion overhang of pmos < %d
overhang *mvpdiff,mvrpdiff mvpfet 250 "P-Diffusion overhang of pmos < %d (poly
overhang *poly allfets 130 "poly.overhang of transistor < %d (poly.8)"
rect_only allfets "No bends in transistors (poly.11)"
^G Help ^O Write Out ^W Where Is ^K Cut ^T Execute ^C Location
^X Exit ^R Read File ^\ Replace ^U Paste ^J Justify ^/ Go To Line