.v file

```
setup> cirread -v design/SoCV/vending/vending-simple.v
Converted 0 1-valued FFs and 48 DC-valued FFs.

setup> print info
Modules in current design: \vendingMachine(242 wires, 71 cells)
#PI = 7, #PO = 7, #PIO = 0

setup> print info -verbose
Modules in current design: \vendingMachine(242 wires, 71 cells)
================================================
   MUX7
   AND3
   ADD22
   SUB9
   MUL8
   EQ9
   NOT2
   LT1
   GE8
------------------------------------------------
   PI7
   PO7
================================================

setup>
```

.blif file

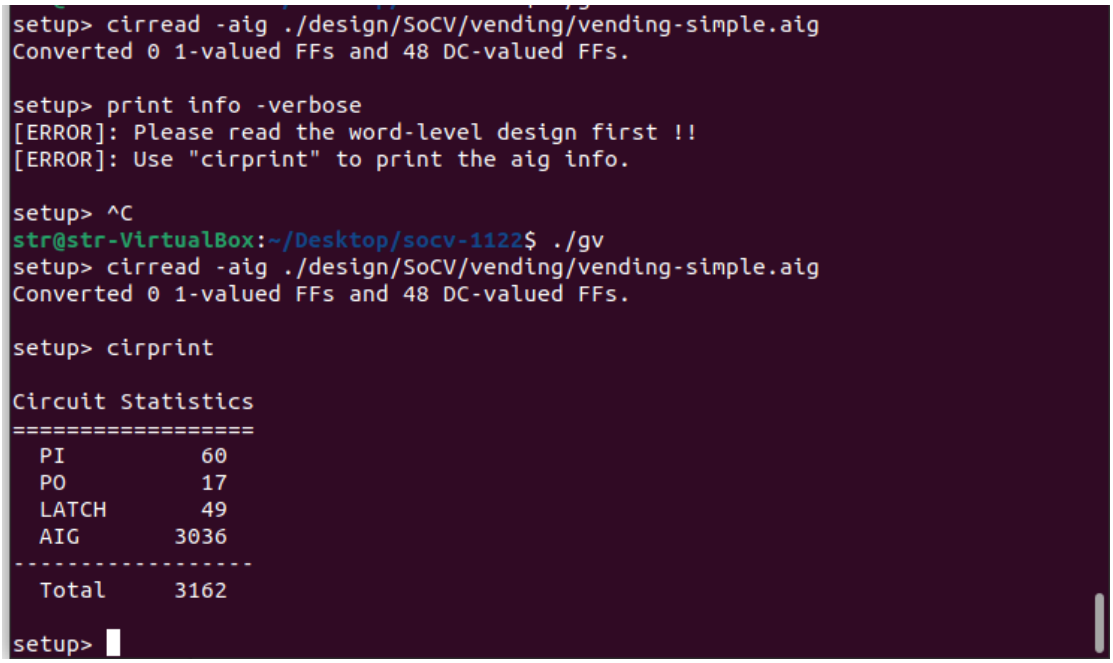
```
setup> cirread -v design/SoCV/vending/vending-simple.v
Converted 0 1-valued FFs and 48 DC-valued FFs.

setup> print info
Modules in current design: \vendingMachine(242 wires, 71 cells)
#PI = 7, #PO = 7, #PIO = 0

setup> print info -verbose
Modules in current design: \vendingMachine(242 wires, 71 cells)
================================================
   MUX7
   AND3
   ADD22
   SUB9
   MUL8
   EQ9
   NOT2
   LT1
   GE8
------------------------------------------------
   PI7
   PO7
================================================

setup>
```

.aig file


setup> cirread -aig ./design/SoCV/vending/vending-simple.aig
Converted 0 1-valued FFs and 48 DC-valued FFs.
setup> print info -verbose
[ERROR]: Please read the word-level design first !!
[ERROR]: Use "cirprint" to print the aig info.
setup> ^C
str@str-VirtualBox:~/Desktop/socv-1122$ ./gv
setup> cirread -aig ./design/SoCV/vending/vending-simple.aig
Converted 0 1-valued FFs and 48 DC-valued FFs.
setup> cirprint
Circuit Statistics
PI 60
PO 17
LATCH 49
AIG 3036
Total 3162
setup>