AN3551

PD70101 and PD70201 PD Device Layout Guidelines

Introduction

This application note provides a detailed layout guidelines for the implementation of a Power over Ethernet (PoE) PD device DC-DC PD system, based on Microchip's PD70101 and PD70201 combined PD and PWM controller devices.

Microchip's PD70101 and PD70201 devices are part of a device family, which are targeted for realizing the 802.3at standard PD interface.

The following table summarizes Microchip PD products offerings.

Table 1. Microchip Powered Device Products Offerings

Part	Type	Package	IEEE 802.3af	IEEE 802.3at	HDBaseT (PoH)	UPoE
PD70100	Front End	3 mm × 4 mm 12L DFN	x	—	—	—
PD70101	Front End + PWM	5 mm × 5 mm 32L QFN	x	—	—	—
PD70200	Front End	3 mm × 4 mm 12L DFN	x	x	—	—
PD70201	Front End + PWM	5 mm × 5 mm 32L QFN	x	x	—	—
PD70210	Front End	5 mm × 5 mm 16L DFN	x	x	x	x
PD70210A	Front End	4 mm × 5 mm 16L DFN	x	x	x	x
PD70210AL	Front End	5 mm × 7 mm 38L QFN	x	x	x	x
PD70211	Front End + PWM	6 mm × 6 mm 36L MLPQ	x	x	x	x
PD70224	Ideal Diode Bridge	7.5 mm × 10 mm 52L MLP	x	x	x	x

Note: Due to their high-power handling capability, ensure to follow the guidelines specified in this application note to have noise robustness and a solution with good thermal behavior.

Microchip offers PD devices that integrate the front-end PD and the PWM into the product package. Additionally, Microchip offers standalone front-end PD devices that require an external PWM IC to convert the high PoE voltage down to the regulated supply voltage used by the application. The front-end section provides the necessary detection, classification, power up functions, and operating current levels that are compliant with the listed standards. The PWM section controls the conversion of the PoE high voltage down to regulated supply voltage used by the application. Microchip offers a complementary product for PoE PD applications, the PD70224 Ideal Diode Bridge, which is a low-loss alternative to the dual diode bridges for input polarity protection.

Microchip offers complete reference design packages and Evaluation Boards (EVBs). For access to these design packages, device datasheets, or application notes, consult your local Microchip Client Engagement Manager or visit our website at www.microchip.com/poe. For technical support, consult your local Embedded Solutions Engineers or go to microchipsupport.force.com/s/.

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1. Layout Guidelines

The PD70101/PD70201 ICs have the following four types of ground.

- VPNI
  VPNI is the negative side of the voltage received from the PSE side. It is connected to VPNO through the isolation switch. This switch is ON till the voltage is a valid PSE voltage.
- VPNO
  VPNO is the negative side voltage, which is the output of the PD device front end. It is connected to VPNI through the isolation switch.
- PWM controller Power Ground (PGND)
  DC-DC power circuitry must be referenced to this ground. The DV/DT FETs gate driving signals are returned through this ground pin.
- Quiet ground (GND)
  PWM controller quiet ground used for the return path of the low power control signals. PWM controller quiet ground used for the return path of the low power control signals.

The GND and PGND pins are connected in a single point to the PCB to eliminate the high current signals affecting the control signals.

To realize IEEE 802.3at standard, PD system usually has another ground type, that is the secondary ground of the DC-DC converter. The secondary ground must obtain 1500Vrms isolation from all the preceding ground types.

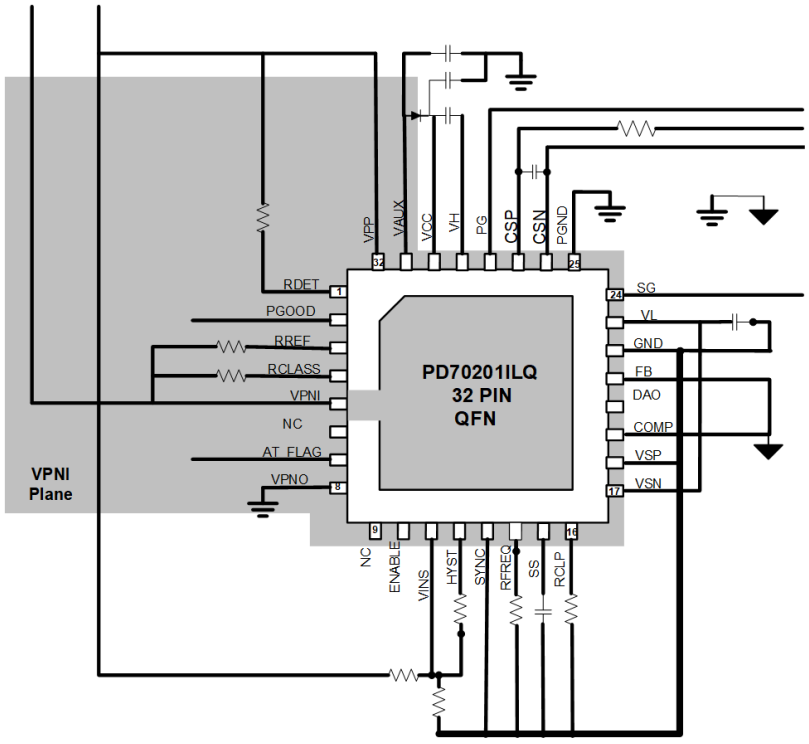
The PD70101/PD70201 structure is listed as follows.

- The device is comprised of dual dies such as, the PD front-end die and PWM controller die.
- Ten pins on the left-hand side of the package belong to PD front-end die. These are pin 31 to pin 32 and pin 1 to pin 8. In addition, the thermal pad—pin 33 in the schematics is also referenced to PD front-end and is internally connected to VPNI signal.
- The rest of the pins belong to PWM controller die.

Figure 1-3 shows the current flow through these stages for the PD70201EVB60F12 evaluation board.

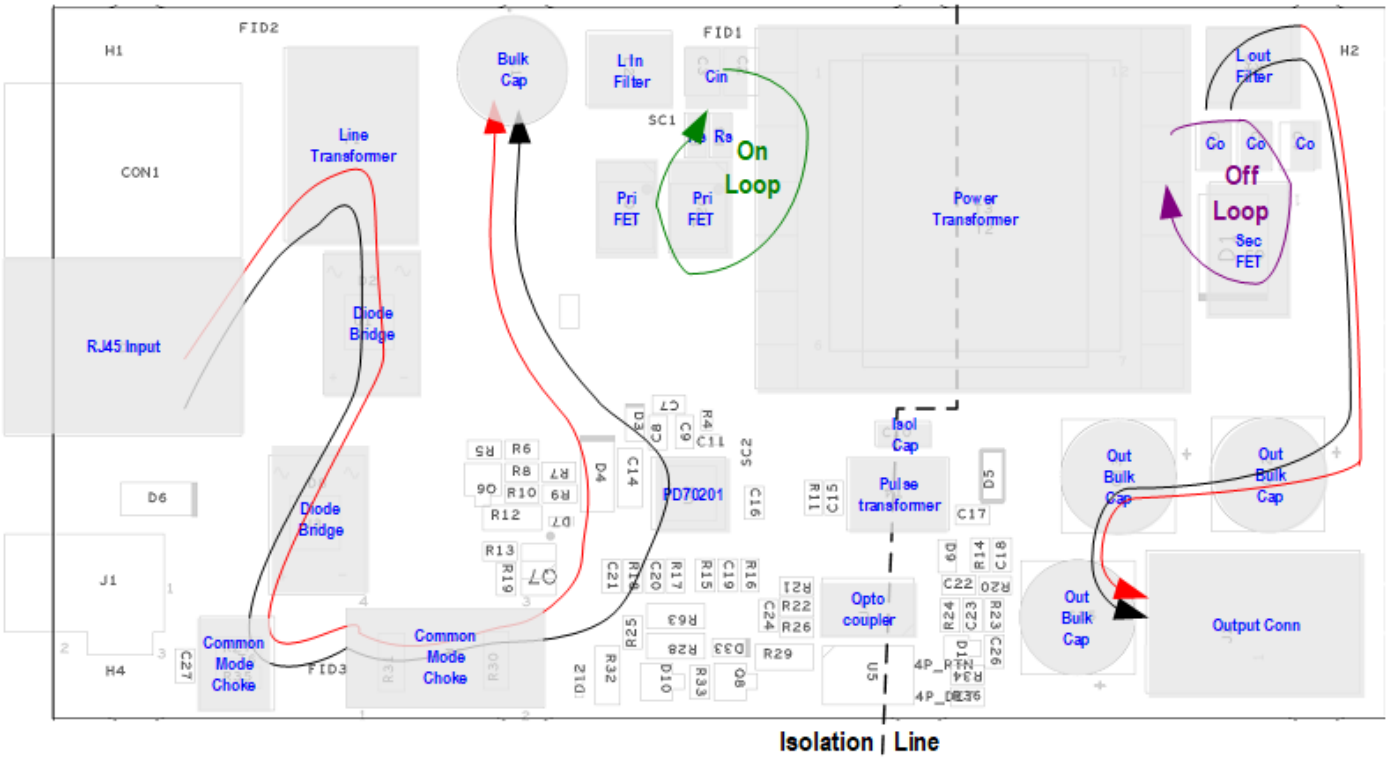
The following figure shows the PD70201 system details.

Figure 1-1. System Based on PD70201



The following figure shows the power loops and power flow of PD70201EVB60F12 EVB board.

Figure 1-2. PD70201EVB60F12 EVB Power Loops and Power Flow



The generic parts of PD are listed as follows.

- Input stage
- DC-DC converter stage
- Output stage

1.1 Input Stage

The input stage consists of the following elements.

- Input RJ45 connectors
- Line transformer
- Diode bridge
- Common mode choke
- PD70101/PD70201 device
- Bulk capacitor for DC-DC input filter

In this set of elements, the current floats in continuous form (non-switched).

Place the first four elements next to each other, to enable the common mode choke to filter the noise close to RJ45 connector.

To have low radiation design, the layout of the positive input and of the negative input should be in a differential form. That is, the positive rail must be tight as compared to the negative one. See the blue and the red lines in Figure 1-3.

Among the preceding elements, the diode bridges and PD device are the only elements that dissipate high power and get heated up. Therefore, the copper land for heat sinking must be maintained. Surge protection components must have shortest path to input RJ45 connector and to earth ground. They must be physically located before rectifier bridge and the remaining downstream components.

1.2 PD70101/PD70201

- The PD70101/PD70201 power dissipation is a function of the device's switching FET resistance and system current.
  P=SW_RDSon x (Maximum current)^2
- Place the PD70101/PD70201 device and its peripheral on top, so that the lower layer is used as a power dissipation layer. Keep it in as a solid VPNI potential.
- The vias under the device are used for heat transfer between the layers.
- If there are inner layers, use them for extended copper land under the device to improve heat dissipation.
- Place VPNi/Vpp capacitors close to the PD70101/PD70201, between pin 5 and pin 32.
- Place PD70101/PD70201 bypass capacitors close to the device.

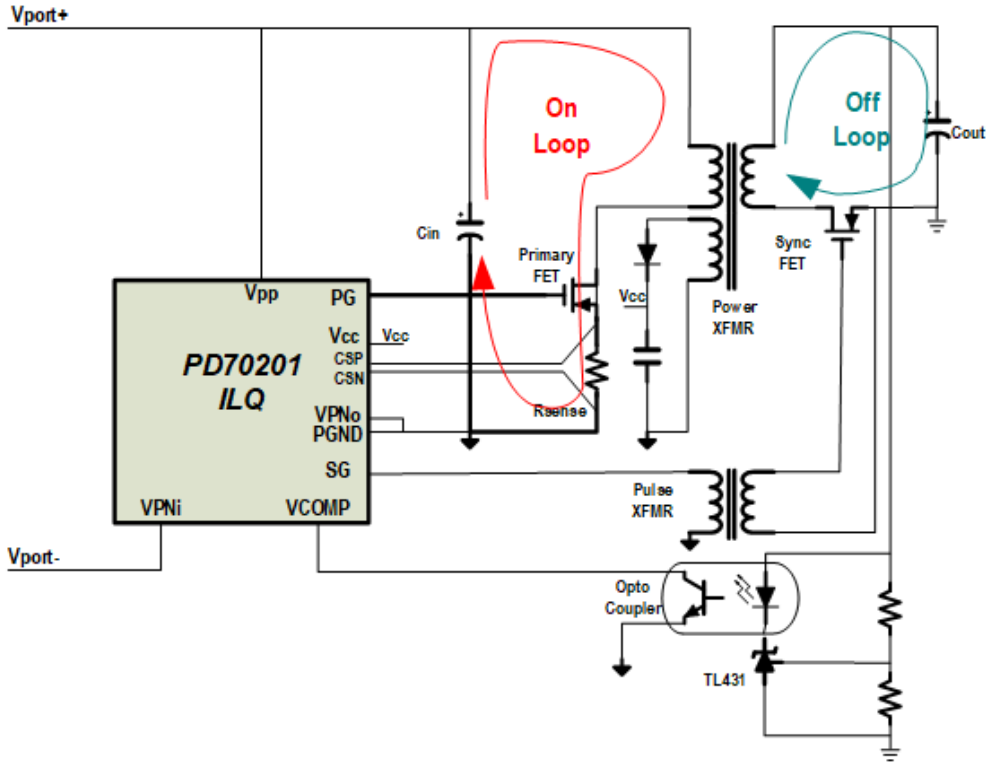
Note: Although the PD device is the controller of the DC-DC converter, its location must be determined by its conducting features. A proper layout allows the control from a distance.

1.3 DC-DC Converter Stage

The following figure shows two current pathways of driver's power section. When primary FET is ON, the current flows through input ON loop. When Primary FET is OFF, the current flows through output OFF loop.

Locating the components close to each other within a loop, allows a shorter current loop. As a result, high currents remain in the driver's power block (and out of ground return path of quiet components). For the ON loop, place Cin, power transformer, sense resistors, and primary FET close to each other. For the OFF loop, place power XFMR, Sync FET, and Cout close to each other.

Figure 1-3. Current Path During ON/OFF Times

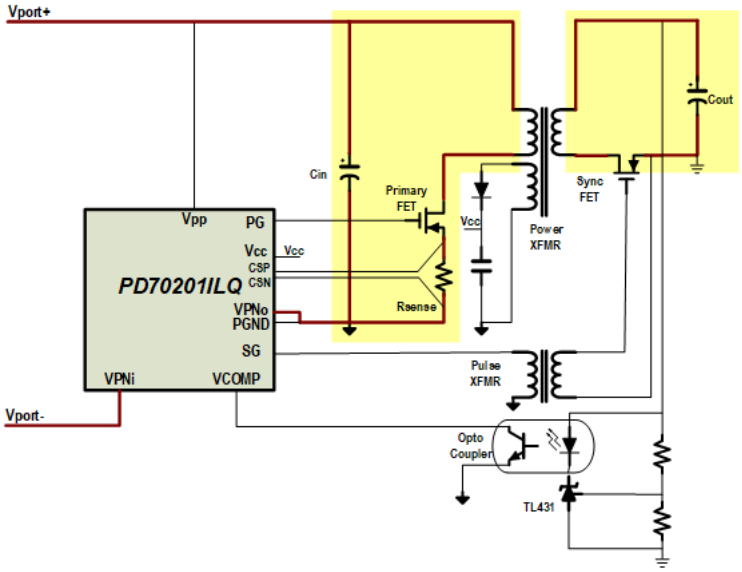


1.3.1 Traces

The following figure shows the high current traces. It is marked in red and highlighted by a yellow background.

Make all high current traces short and direct. The trace thickness must withstand its current values with low temperature rise.

Figure 1-4. High Current Traces Layout



Note: The power flows out of VPNo signal and not PGND.

1.4 Sense Resistors

Sensing the primary loop current is done using 1%, ±100 ppm low resistance resistors connected as a shunt.

The following figure shows the right way to layout the power supply sense resistors.

Calculate sense resistor power dissipation to choose the resistor size and the number of resistors according to the calculation result.

The sense resistors' voltage is in the range of 0 mV to 200 mV and exists in an environment of fast transitions of up to 160 V. The form of the current sense signal is important, and its integrity must be maintained. Thus, the sense voltage traces layout should be maintained carefully.

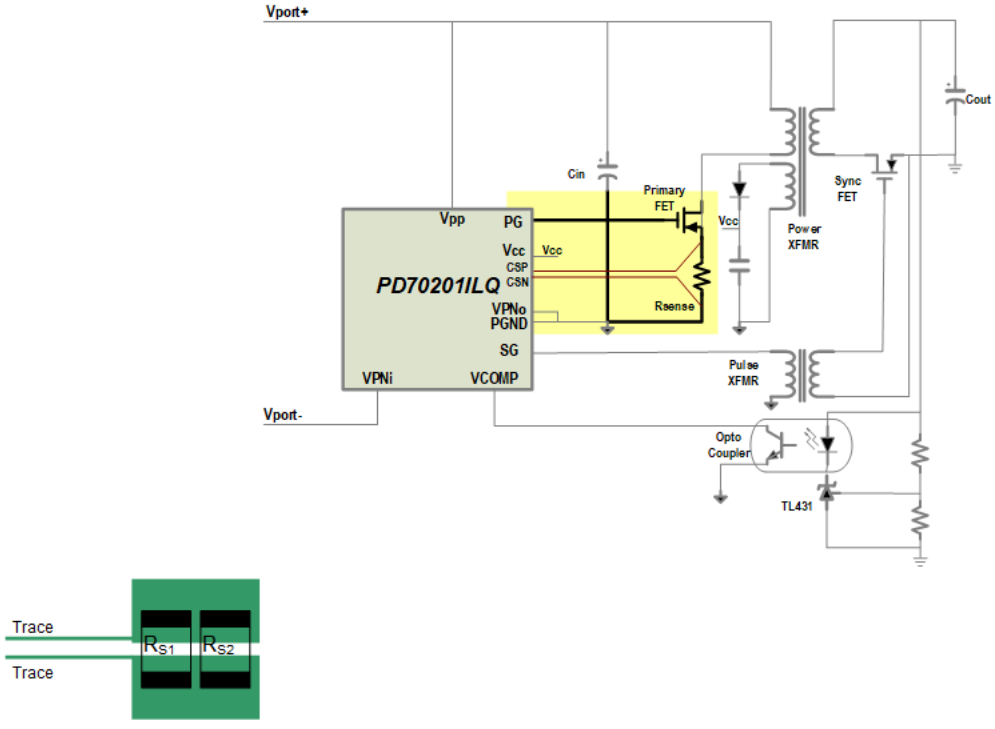
To simplify the integrity challenge, PD70101/PD70201 has a differential sampling mechanism built of CSP and CSN pins.

Route differential traces from sense resistor terminals to CSN and CSP input pins. They must be connected as a Kelvin connection, close to the resistor's pads and must not be a part of the high current path to the resistors. This way, the voltage measurement is not influenced by voltage drop on the high-power traces.

The two lines must be routed together, close to each other, to maintain good noise immunity. For the resistor high current trace, use a wide trace or copper planes to decrease trace voltage drop.

The following figure shows the sense resistor layout.

Figure 1-5. Sense Resistor Layout



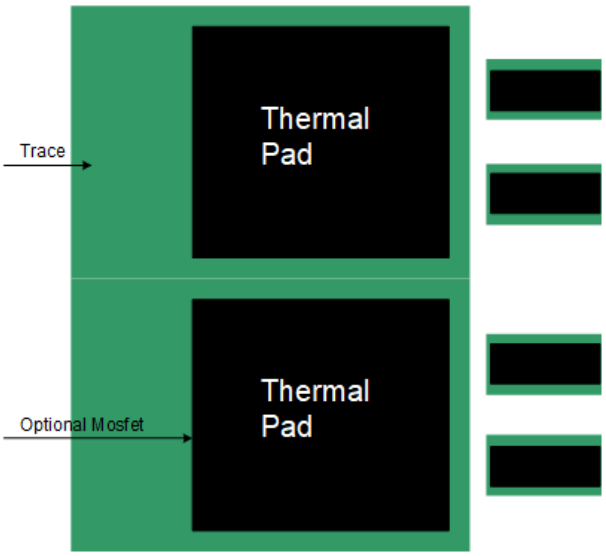
1.5 Primary and Secondary FETs

The primary and the secondary FETs are high power devices. FET must have a copper land to enable power dissipation from it to the environment.

Copper land is a function of the FET package power consumption and the system requirements.

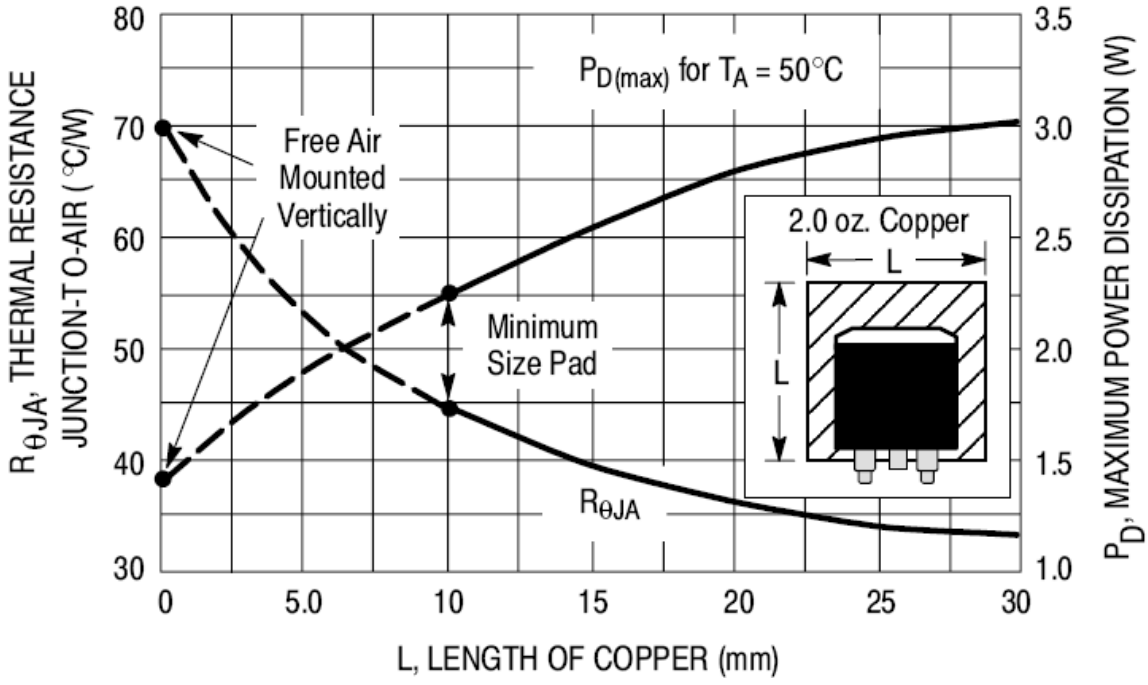
The following figure shows the DC-DC converter MOSFET layout. Calculate DC-DC converter FET power dissipation to choose MOSFET's package and thermal pad size according to calculation results. If two MOSFETs are used, connect them in parallel.

Figure 1-6. MOSFET Layout



Note: See MOSFET manufacturers information for designing proper thermal pads. There must be 1" x 1" thermal pad with vias to the opposite side of the board connecting to the additional thermal pads.

Figure 1-7. Thermal Resistance Versus Drain Pad Area for D2PAK Package



1.6 Isolation

For an isolated DC-DC design such as Flyback, the isolation level is based on IEEE 802.3at standard. IEEE 802.3at standard defines that the 1500Vrms isolation must be obtained between all the accessible external conductors including the frame ground (if any), RJ45 connector leads, and all internal leads of the PD such as the secondary side traces.

Isolation must be maintained between Flyback converter's primary and secondary sides and between the frame ground and the secondary side.

1500Vrms isolation is obtained by a gap of 60 mil between the traces of the primary domain and the secondary domain.

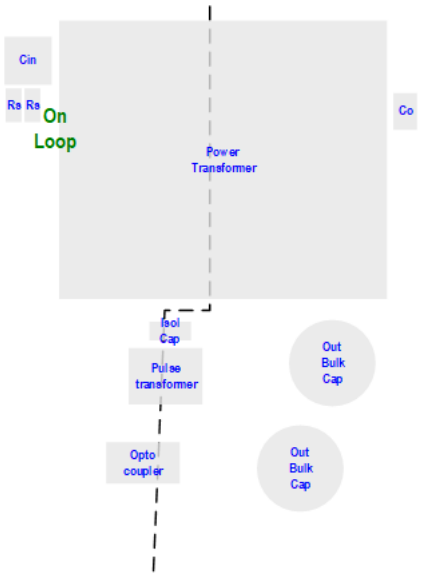
The isolation line of separation should include power transformer, secondary gate pulse transformer, opto-couplers, and primary/secondary 2000 V capacitor.

The capacitor must be placed close to the power transformer to help fight the conducted emission issues, if raised.

Do not mix the two isolated sides. Mixing the sides might cause the signals to mix and lead to difficulty in maintaining the isolation.

Use a physical isolation line as shown in the following figure.

Figure 1-8. Isolation Line



A plane layout under the primary and the secondary sides of the power transformer must not be present.

1.7 Driving

Gate drive pulses are supplied to the primary and secondary gates and are generated by the PWM controller section of the PD70101/PD70201 devices.

To increase the efficiency and decrease the temperature rise of the FETs, obtain the fast slew rate pulses.

The PD70101/PD70201 device drivers have internal serial output resistance. You may need to use extra driving components to overcome this internal resistance and the distance of the controller from the FETs. For proper operation of the driving elements, pull-up transistor, pull-down transistor, and bypass capacitor must be placed close to the referenced FET.

1.8 Snubbers

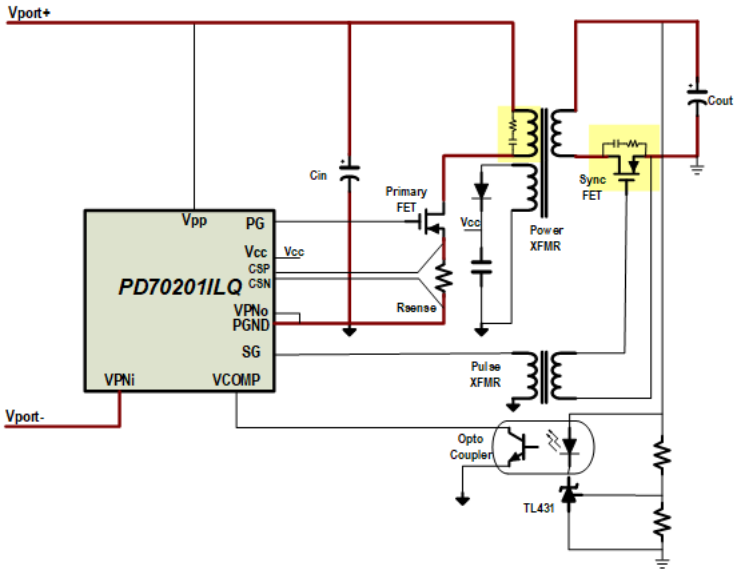
Snubbers are elements that protects the FETs from high voltage spikes, produced due to system parasite. For example, in the primary domain, the transformer inductance reaction to current switching creates high voltage spikes.

To overcome this issue, snubber is placed in parallel to the transformer's primary winding and must be placed close to it. The proximity is important to reduce the voltage spikes on the drain and source of the primary FET.

The lower side of the transformer yields a low inductance connection. The snubber consists of the serial resistor and capacitor (RC snubber), resistor-capacitor-diode (RCD), or active snubber that also uses inductor. The secondary side snubber is an RC snubber. It must be placed close to the secondary FET, between the drain and the source.

The following figure shows the snubbers location.

Figure 1-9. Snubbers Location



1.9 Heat Sinking

The following components dissipate the major power portion and result in heating up.

- Primary FET
- Secondary FET
- Power transformer
- PD70x01 device
- Primary snubber components
- Secondary snubber components

The board design must provide an adequate copper land for dissipating the heat of those components. Vias under the device are used for heat transfer between layers. Use 25 mil vias for effective heat transfer between the layers. Use the external layers for heat dissipation and the internal layers for good heat transfer.

1.10 Design Example

The following figures show the layout of PD70201EVB60F12 evaluation board. This board can be ordered from Microchip.

Figure 1-10. PD70201EVB60F12 EVB PCB Silk Top

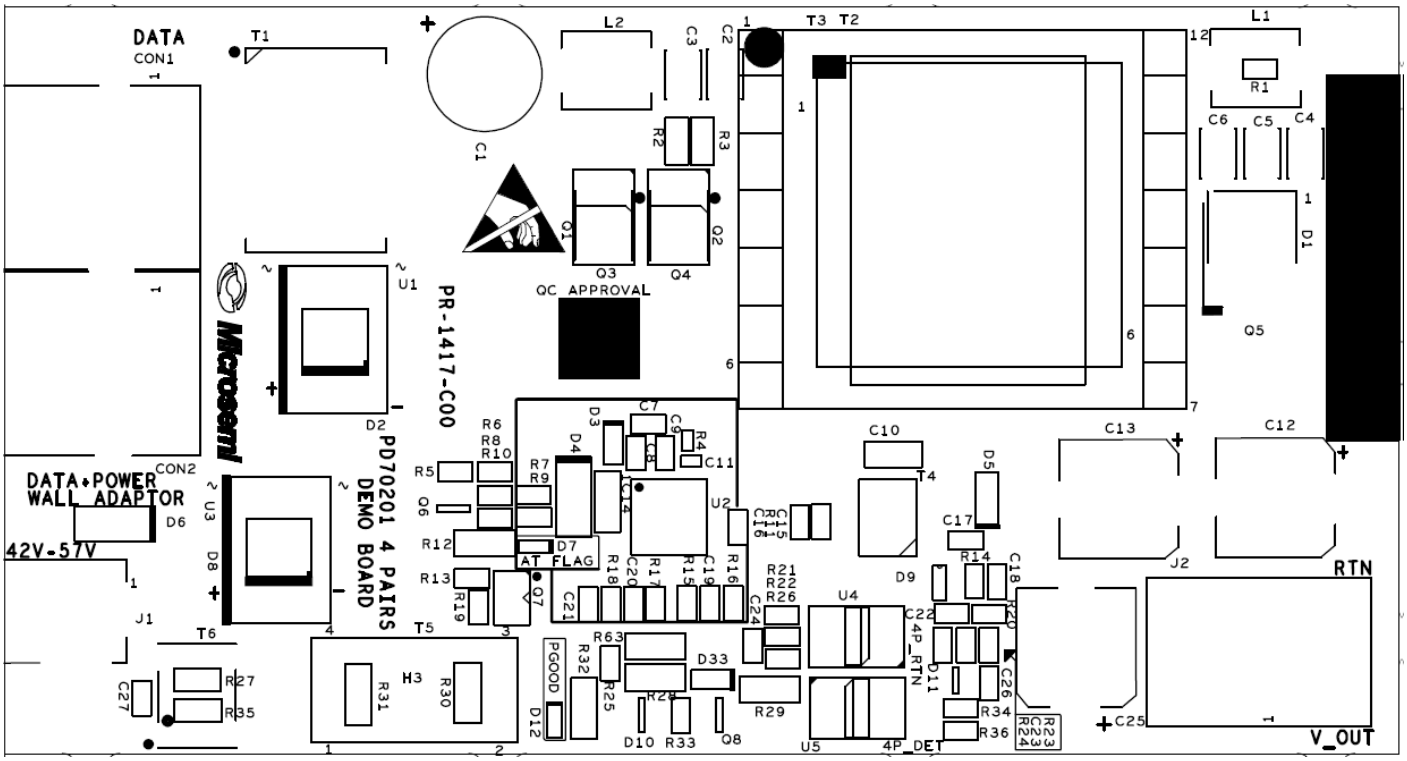


Figure 1-11. PD70201EVB60F12 EVB PCB Top

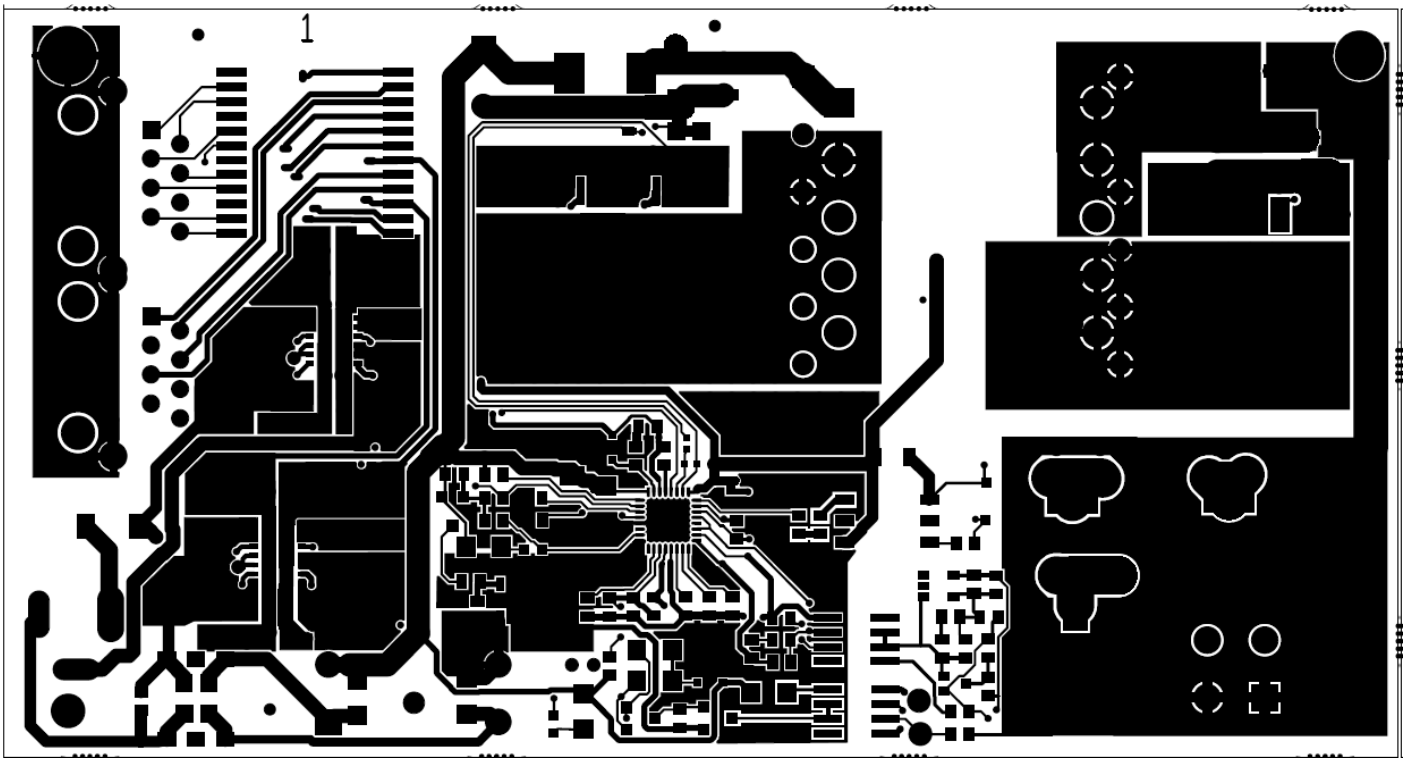


Figure 1-12. PD70201EVB60F12 EVB PCB Layer 2

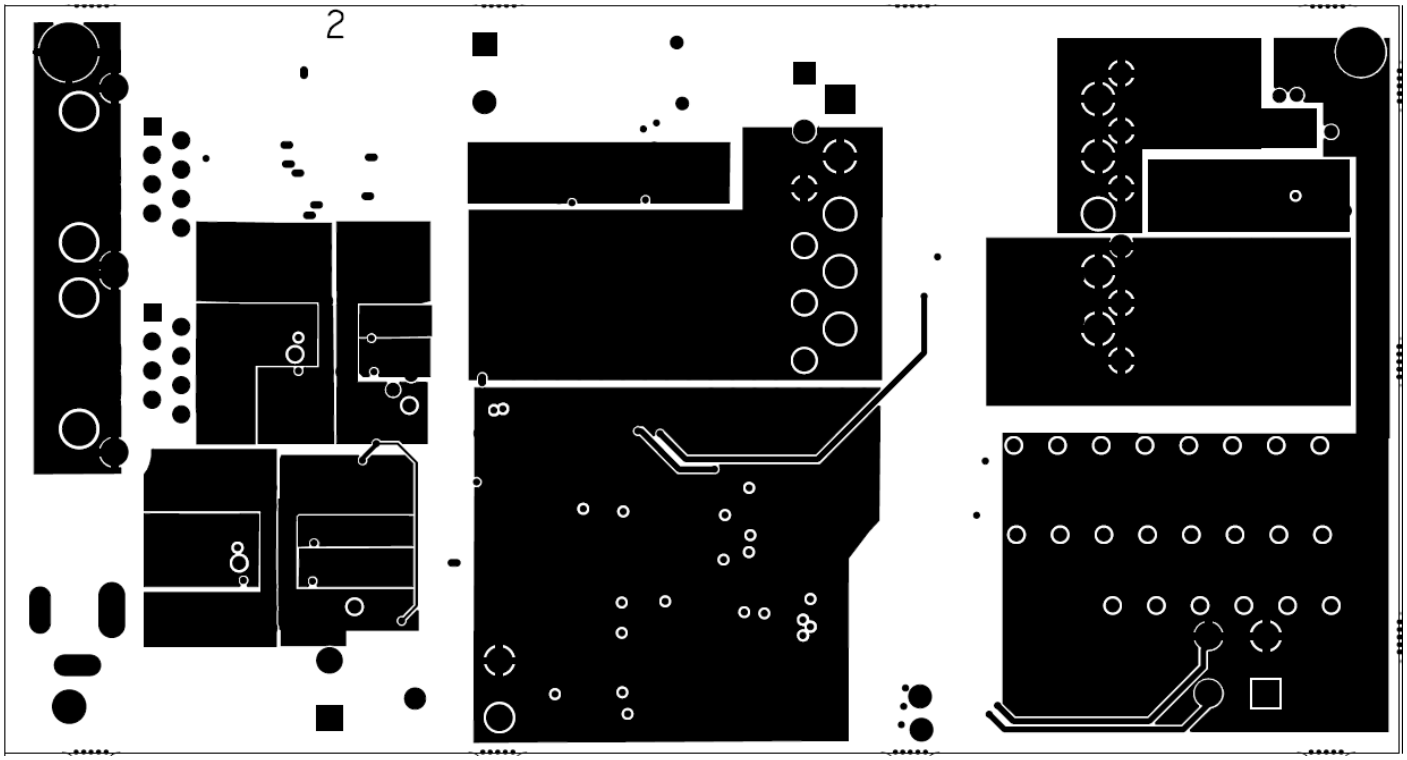


Figure 1-13. PD70201EVB60F12 EVB PCB Layer 3

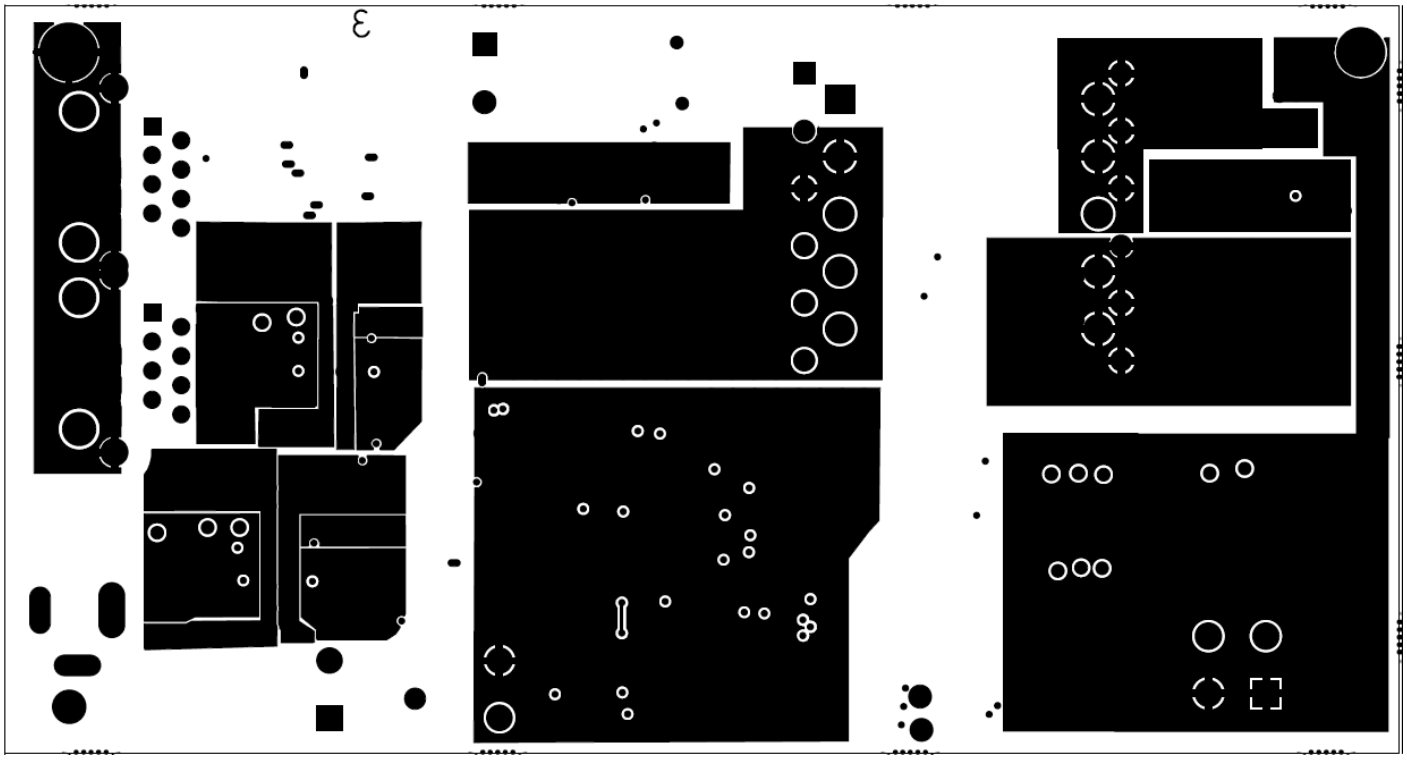


Figure 1-14. PD70201EVB60F12 EVB PCB Bottom Layer 4

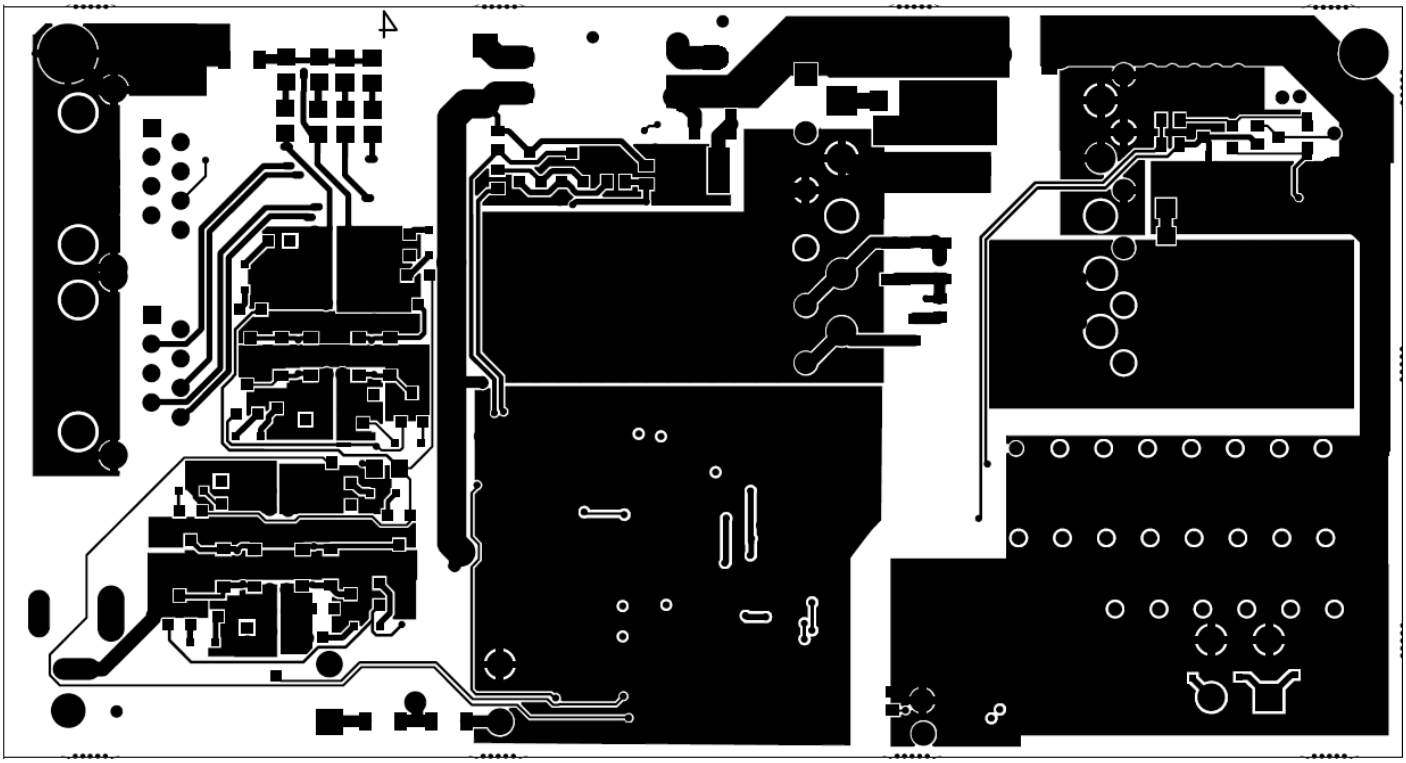
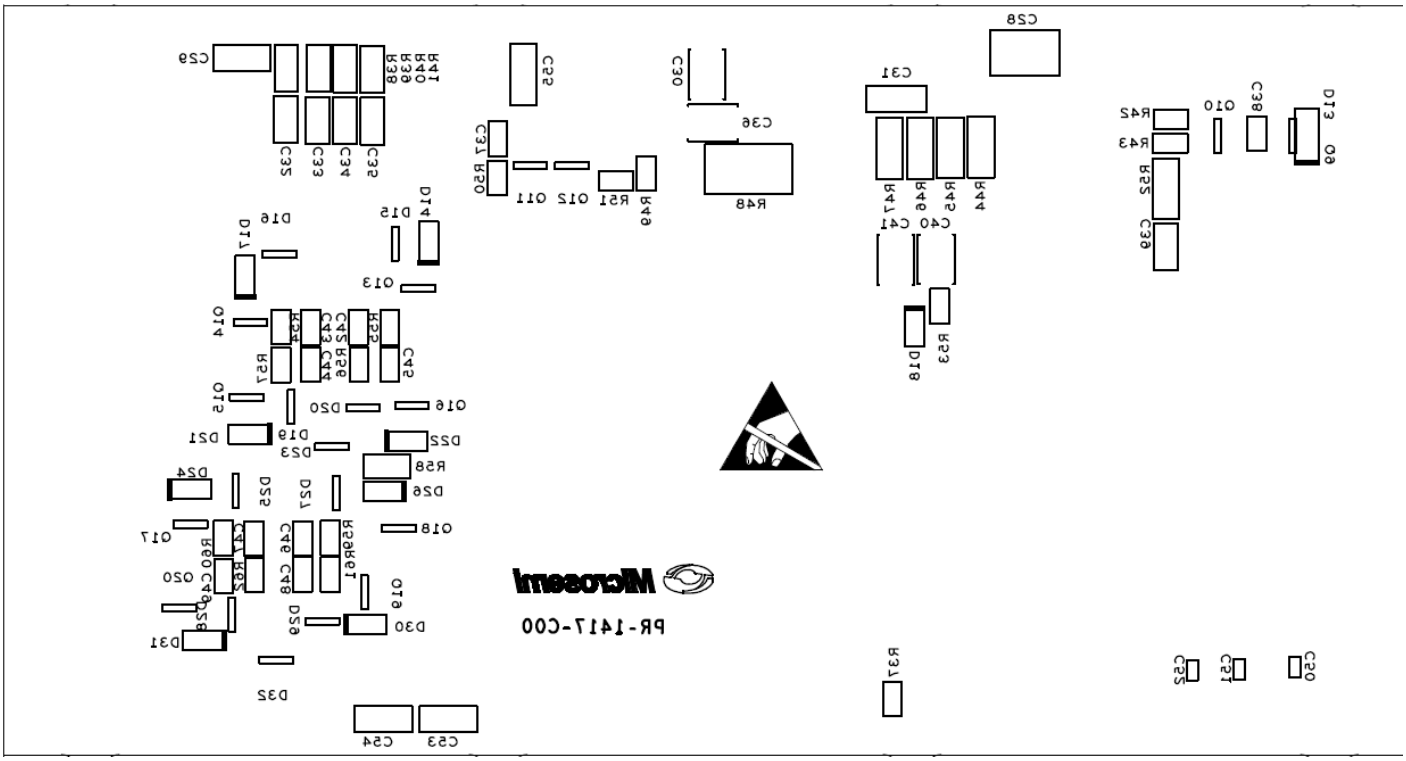


Figure 1-15. PD70201EVB60F12 EVB PCB Silk Bottom Mirror



2. References

- *PD70101/PD70201 Datasheet*
- *PD70201EVB60F12 Evaluation Board User Guide*
- *AN3468 Designing a Type 1/2 802.3 or HDBaseT Type 3 Powered Device Front End Using PD702x0 and PD701x0 ICs*
- *AN3471 Designing a Type 1/2 802.3 or HDBaseT Type 3 Powered Device Using PD702x1 and PD701x1 ICs*

3. Revision History

Revision	Date	Description
A	July 2020	The following is a summary of changes in revision A of this document. • The document was migrated to Microchip template. • The document number was changed from PD70101A_PD70201_AN208 to DS00003551 and AN-208 to AN3551. • Removed device footprint information and added it to the device datasheet.
1.0	December 2012	Initial release–preliminary version

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