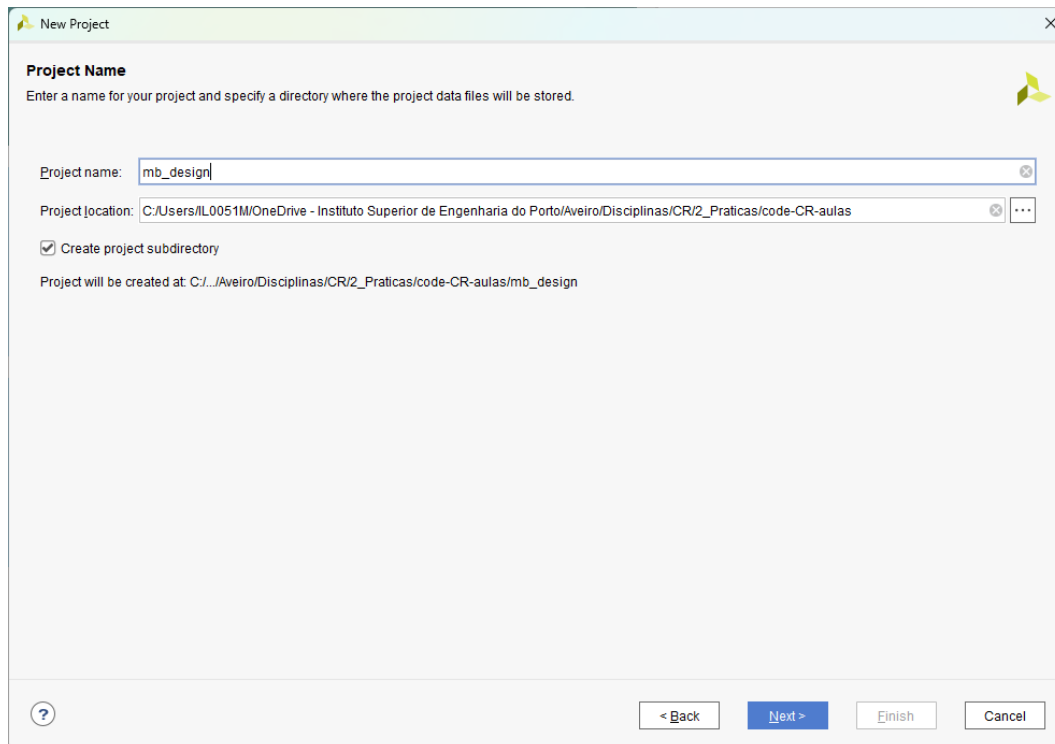
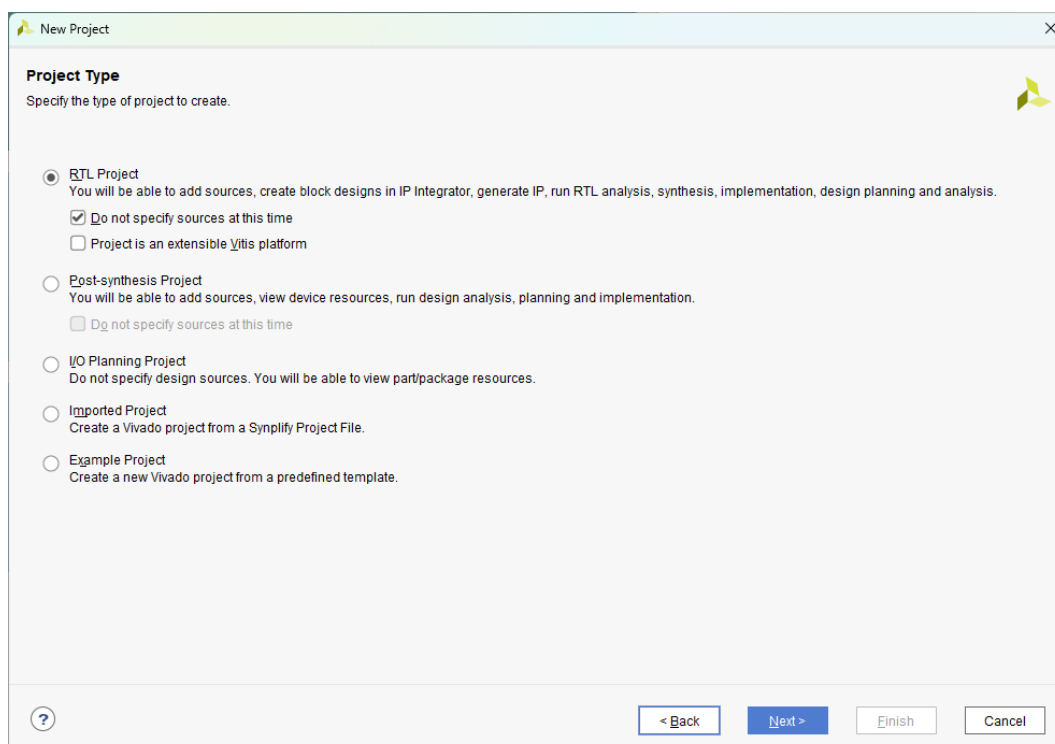


## Instructions to create the MicroBlaze design in Vivado

1. Start Vivado
2. Create a new project; name it at your discretion.



3. No need to specify sources.



4. Select the tab **Boards**, on the top of the white area.

**New Project**

**Default Part**  
Choose a default Xilinx part or board for your project.

**Parts | Boards**

[Reset All Filters](#)

Category:  Package:  Temperature:   
 Family:  Speed:  Static power:

Search:

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	HNICX	BUFGs
xc7vx415tffv1158-2L	1158	350	257600	515200	880	0	2160		32
xc7vx415tffv1158-1	1158	350	257600	515200	880	0	2160		32
xc7vx415tffv1927-3	1927	600	257600	515200	880	0	2160		32
xc7vx415tffv1927-2	1927	600	257600	515200	880	0	2160		32
xc7vx415tffv1927-2L	1927	600	257600	515200	880	0	2160		32
xc7vx415tffv1927-1	1927	600	257600	515200	880	0	2160		32
xc7vx485tffg1157-3	1157	600	303600	607200	1030	0	2800		32
xc7vx485tffg1157-2	1157	600	303600	607200	1030	0	2800		32
xc7vx485tffg1157-2L	1157	600	303600	607200	1030	0	2800		32
xc7vx485tffg1157-1	1157	600	303600	607200	1030	0	2800		32
xc7vx485tffg1158-3	1158	350	303600	607200	1030	0	2800		32

[? < Back](#) [Next >](#) [Finish](#) [Cancel](#)

5. Select your board. Click **Next**.

**New Project**

**Default Part**  
Choose a default Xilinx part or board for your project.

**Parts | Boards**

[To fetch the latest available boards from git repository, click on 'Refresh' button. Dismiss](#)

[Reset All Filters](#)

Vendor:  Name:  Board Rev:

Search:  (5 matches)

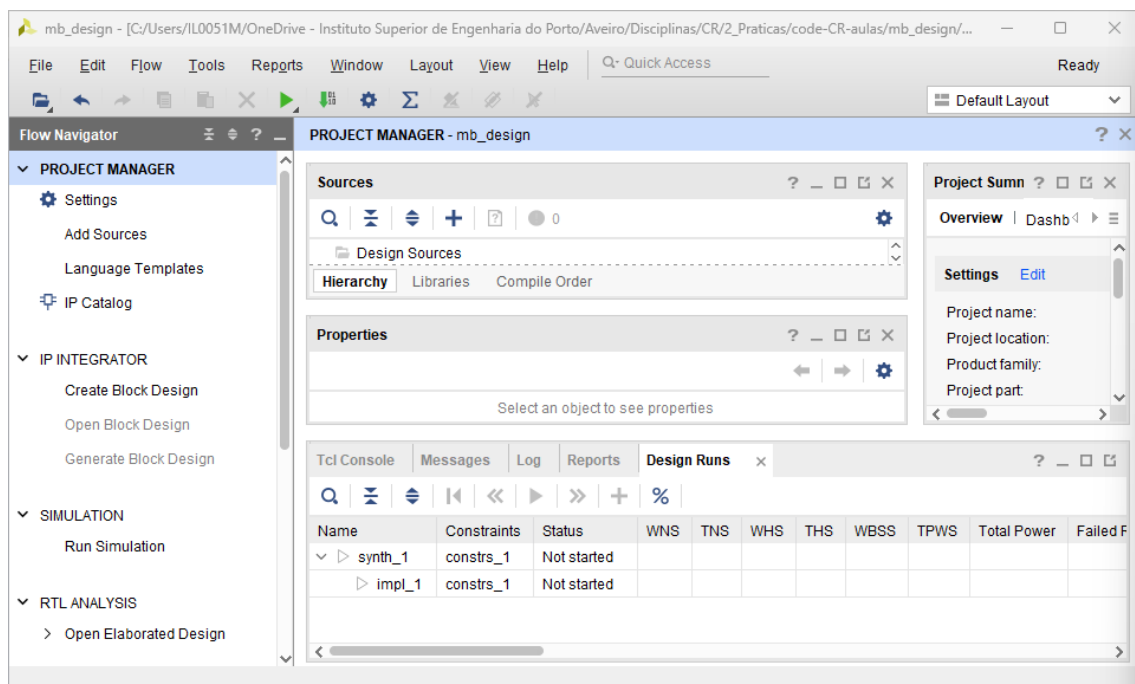
Display Name	Preview	Status	Vendor	File Version	Part	I/O Pin Count	Board Rev	
Nexys A7-100T		Installed	digilentinc.com	1.3	xc7a100tcsfg324-1	324	D.0	2
Nexys A7-50T		Installed	digilentinc.com	1.3	xc7a50tcsfg324-1L	324	D.0	2
Nexys4		Installed	digilentinc.com	1.1	xc7a100tcsfg324-1	324	B.1	2

[Refresh](#)

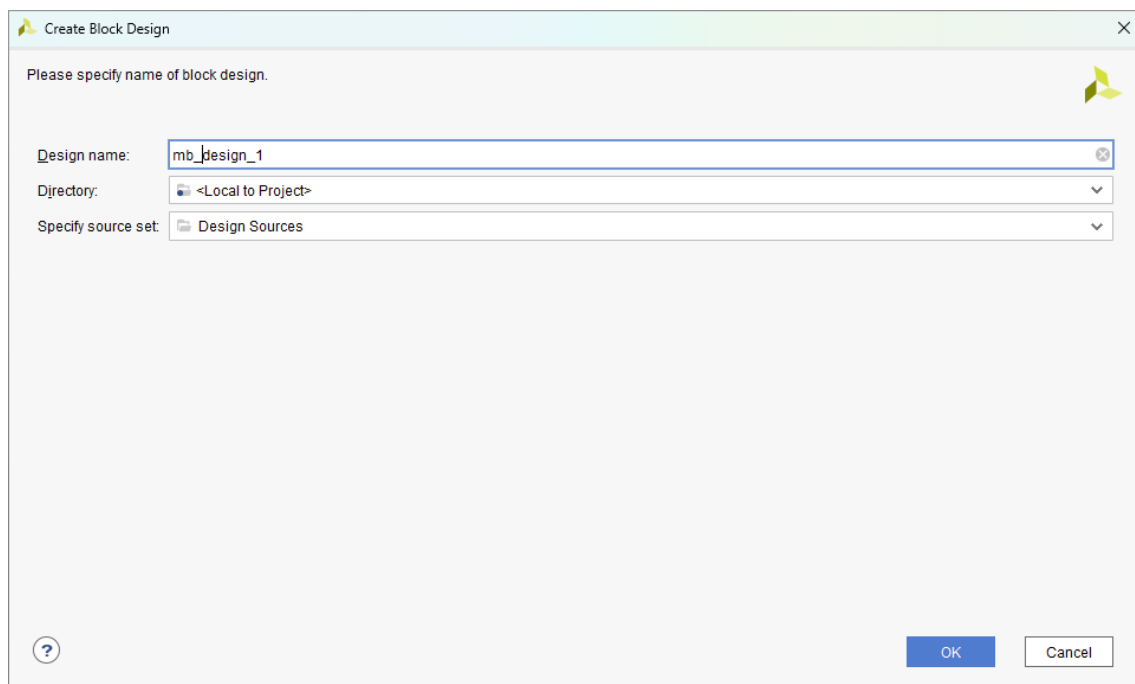
[? < Back](#) [Next >](#) [Finish](#) [Cancel](#)

6. Click **Finish**.

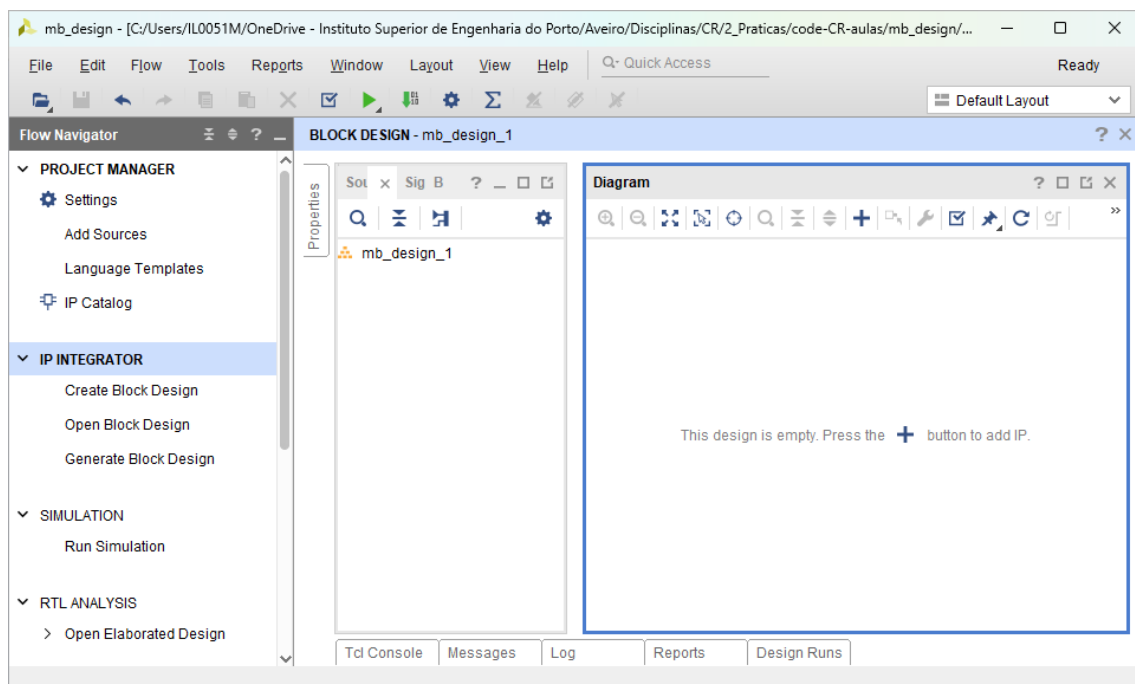
7. Click on **Create Block Design** on the **Flow Navigator** (left column).



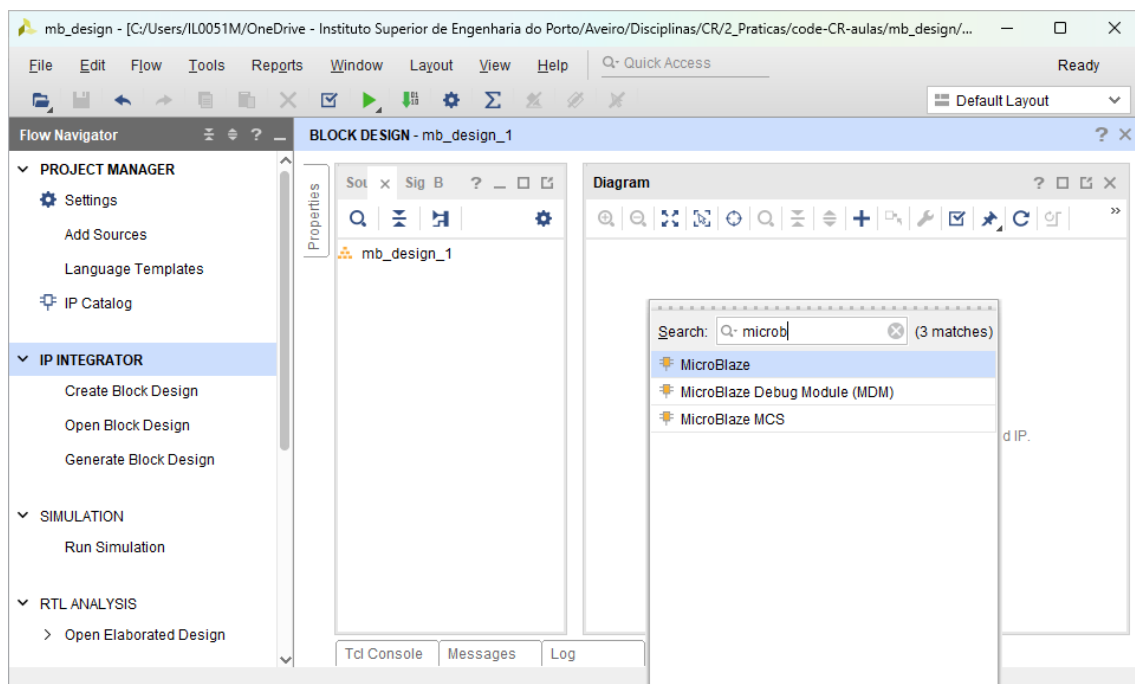
8. Name the new design at your discretion.



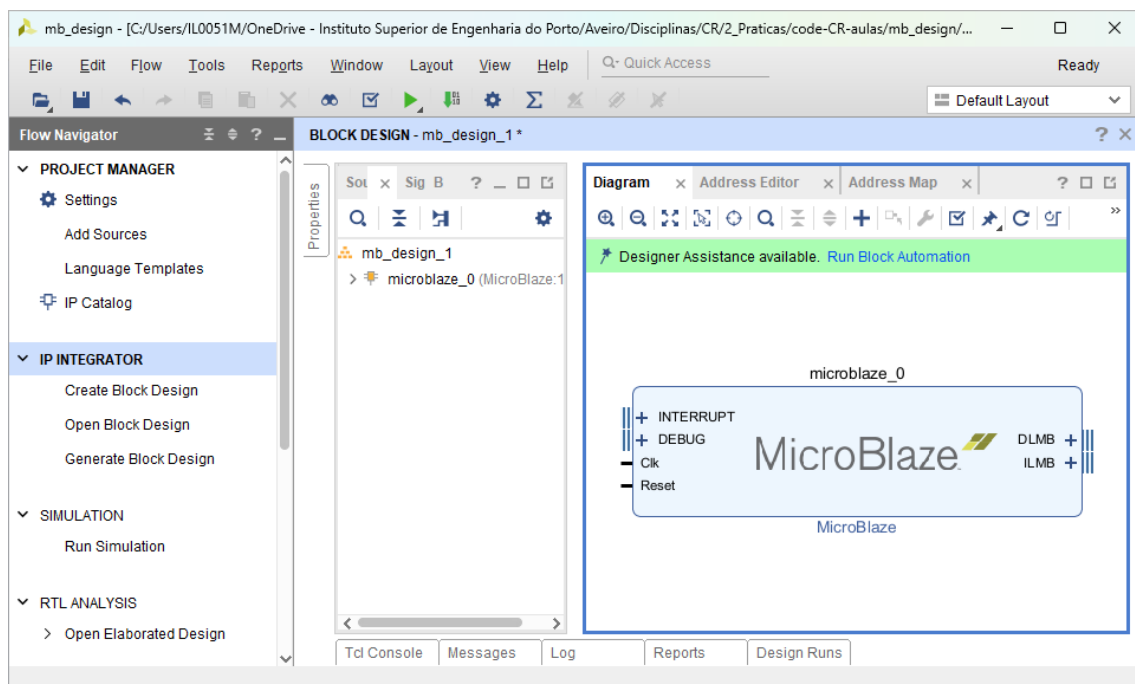
9. Click on the + sign to add a new block.



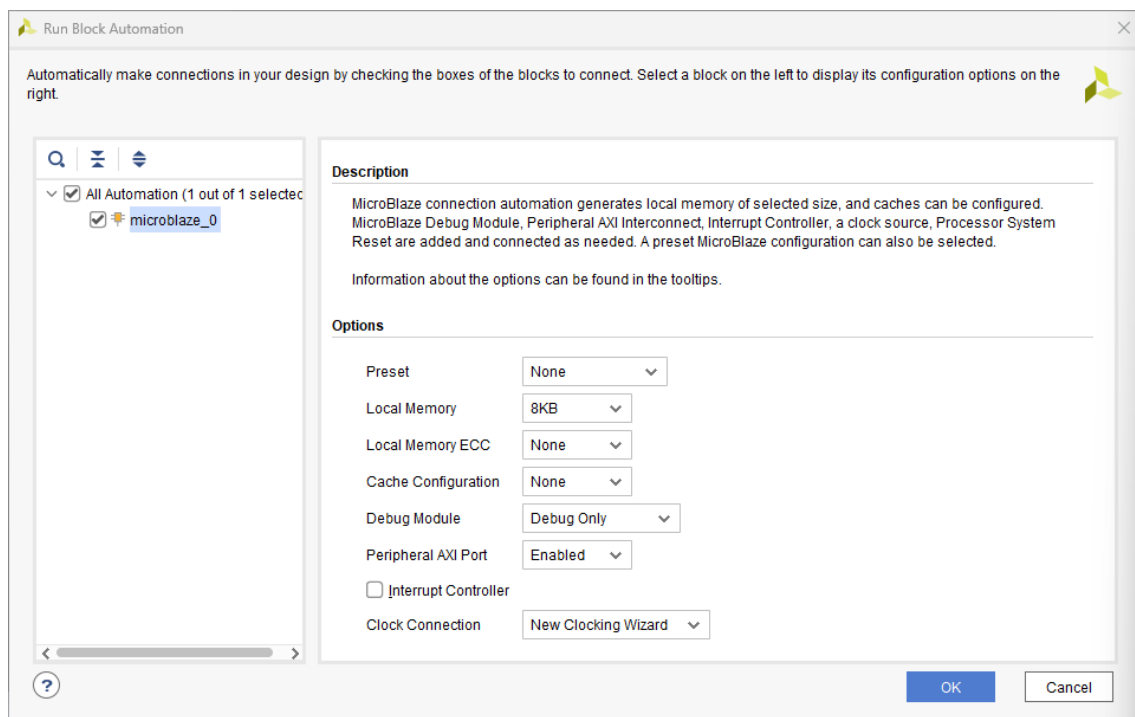
10. Select the **MicroBlaze** block from the dropdown menu.



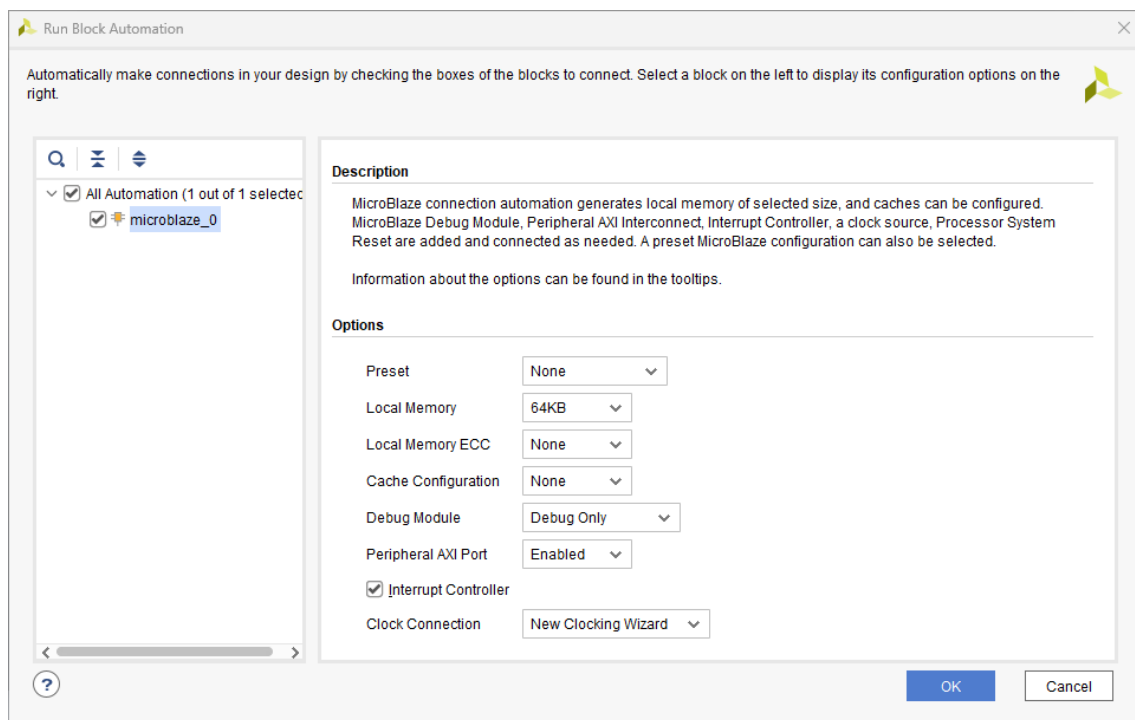
11. A green bar shows up providing access to the **Block Automation** helper. Click it.



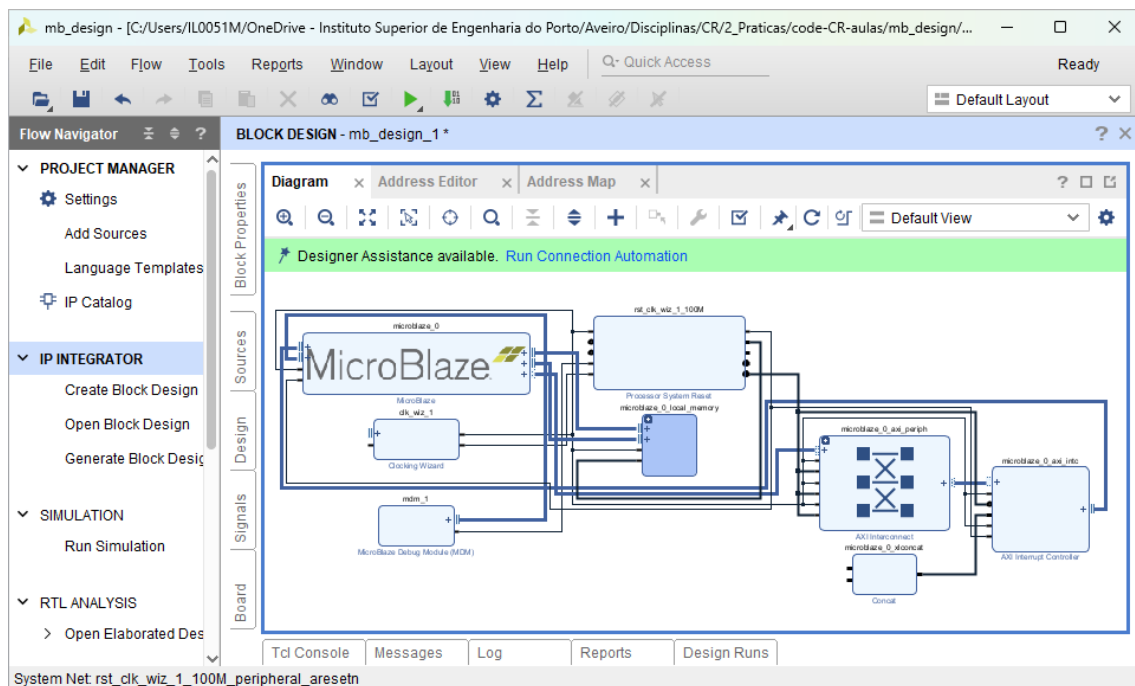
12. Options for configuring the MicroBlaze show up.



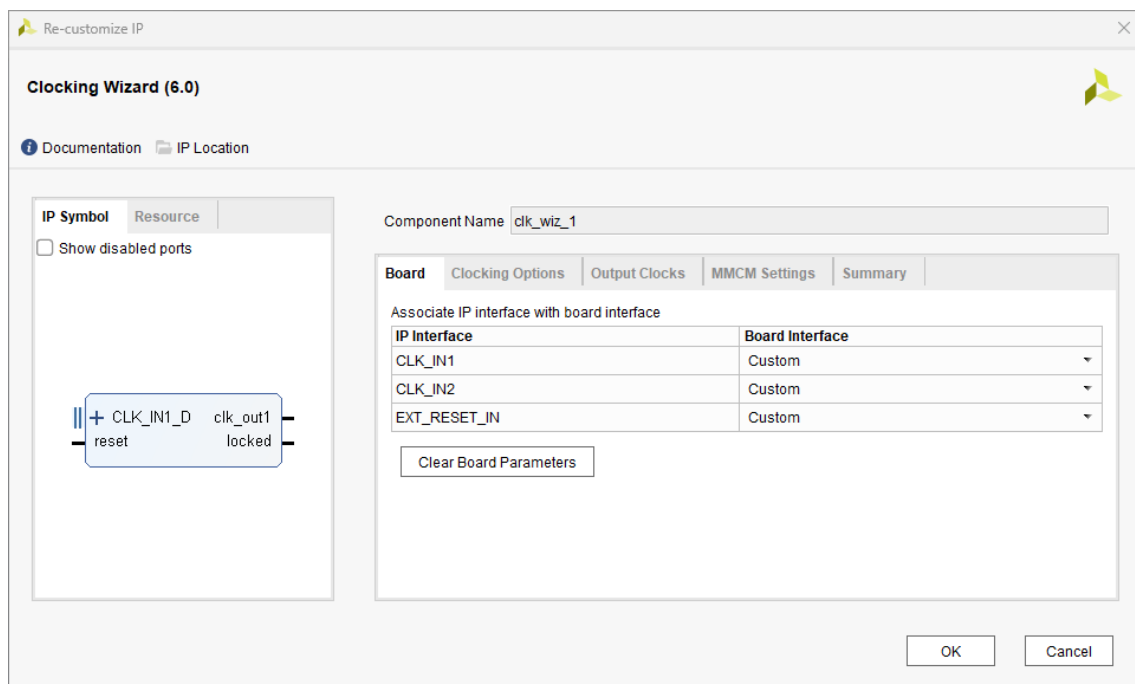
13. Select **Local Memory** to be **64KB**, and tick the **Interrupt Controller** tickbox.



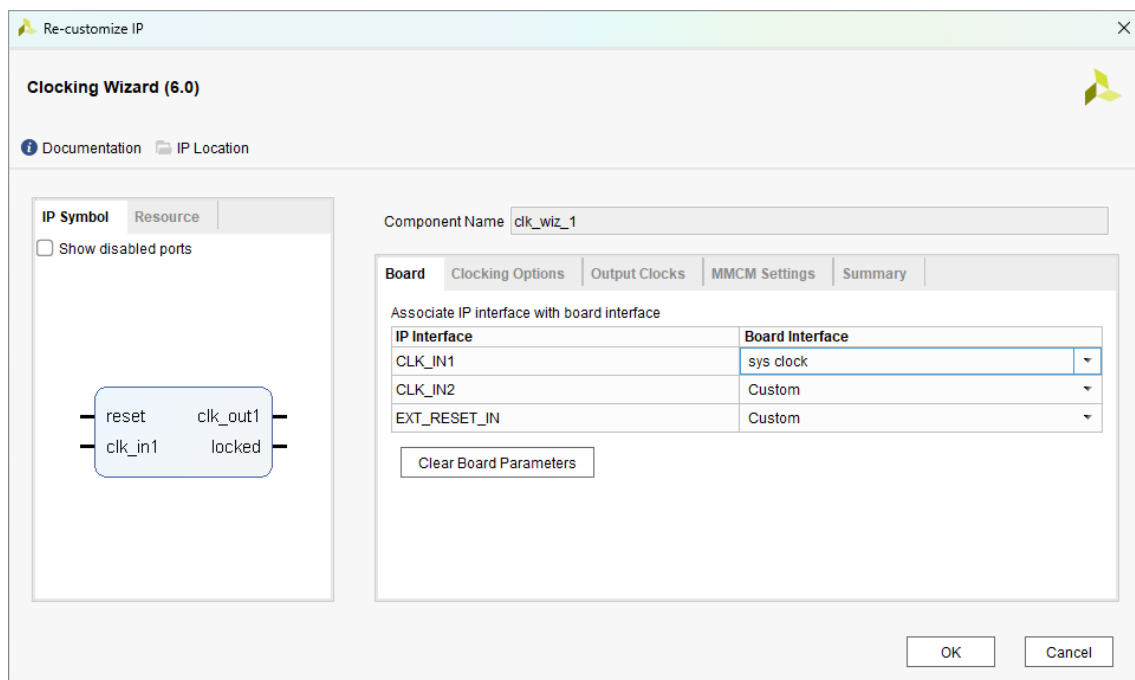
14. You should see new blocks that support the MicroBlaze's operation. There is also a green bar offering the Connection Automation helper. DO NOT CLICK IT RIGHT AWAY. Instead, right-click the **Clocking Wizard** block.



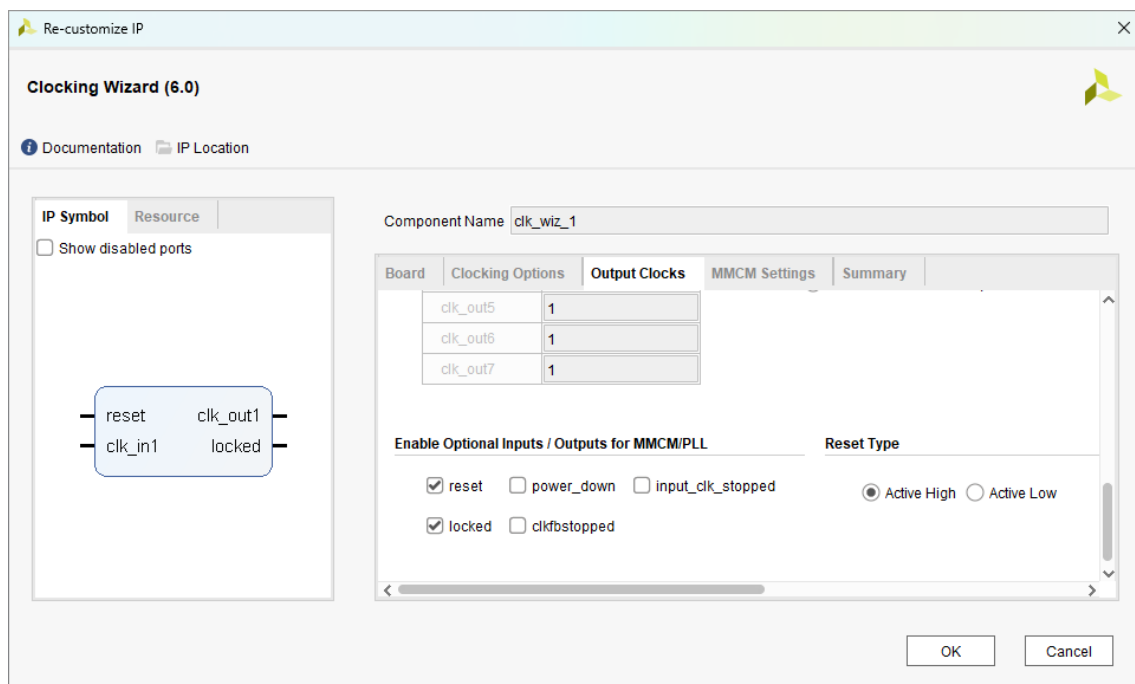
15. A new window pops up.



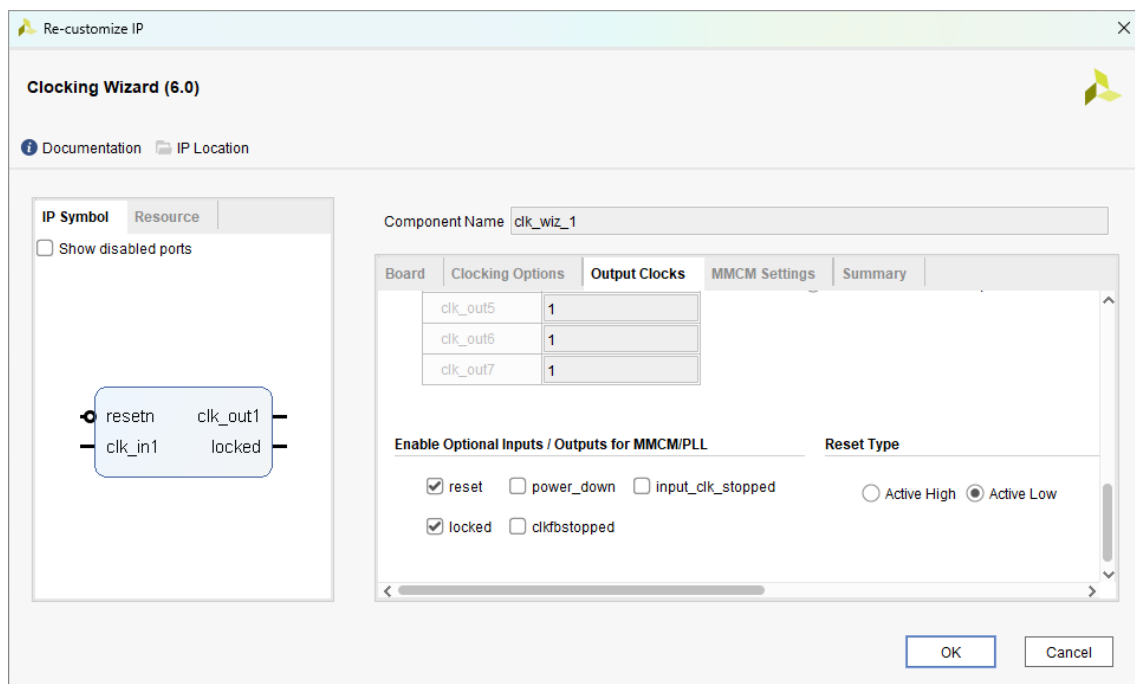
16. Set **CLK\_IN1** to **sys clock**. This is the signal corresponding to the board's clock signal.



17. In the tab **Output Clocks**, the following is shown.

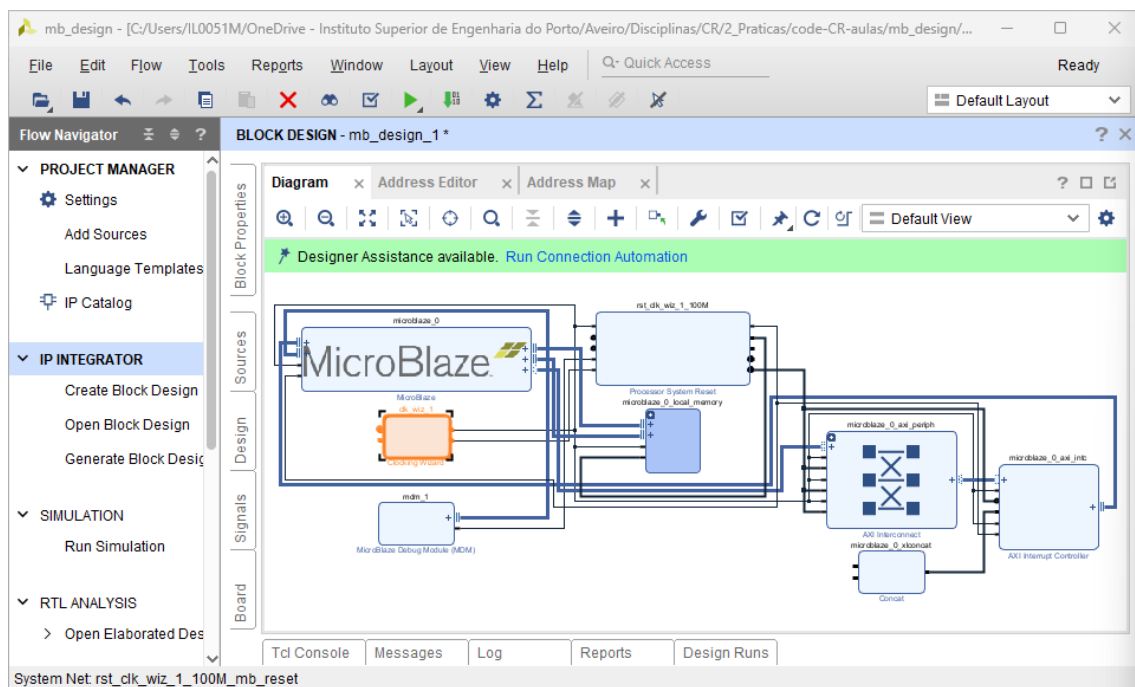


18. Tick the **Active Low** box for the **Reset Type** option. Close the window.

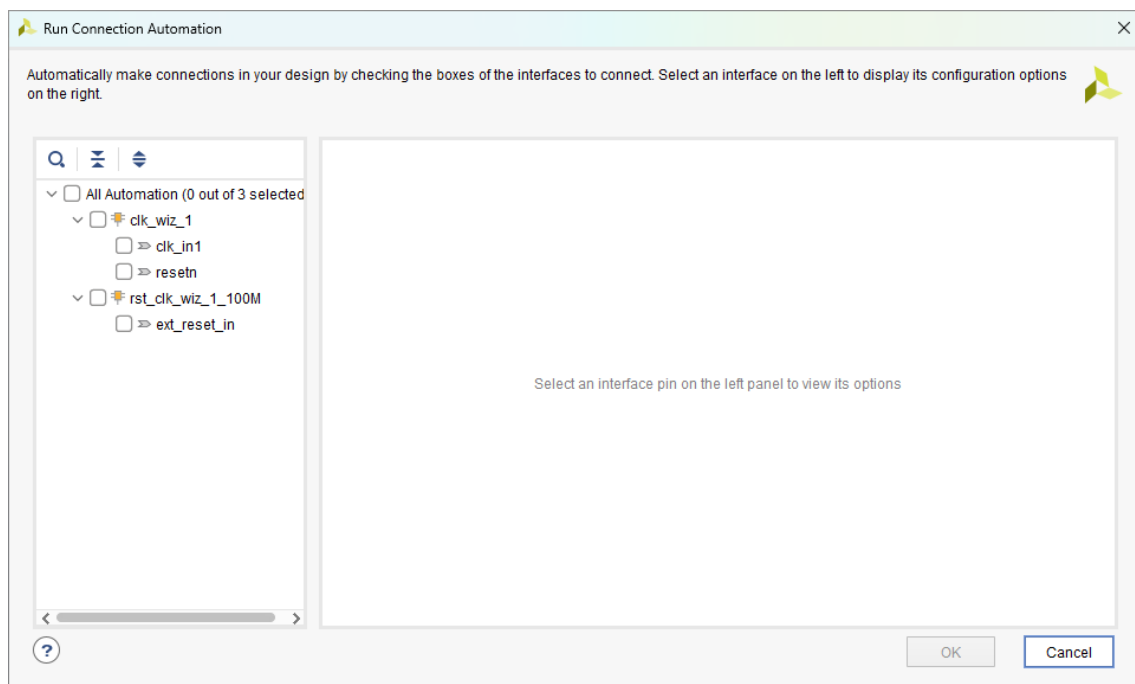




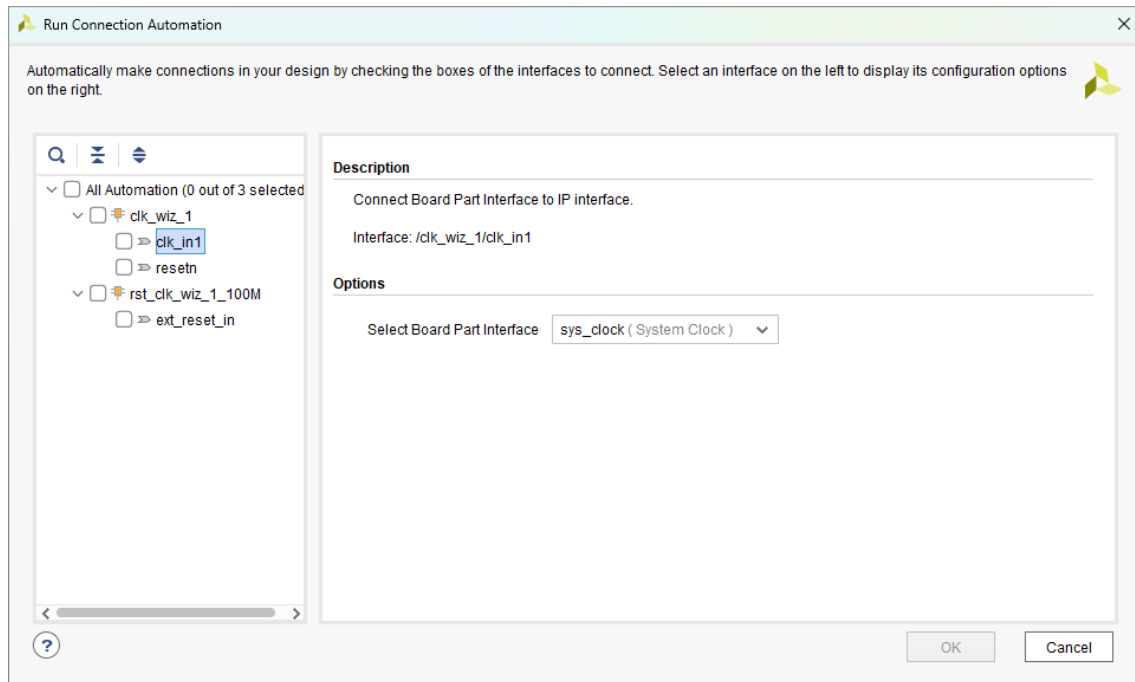
19. Now, run the **Connection Automation** helper.



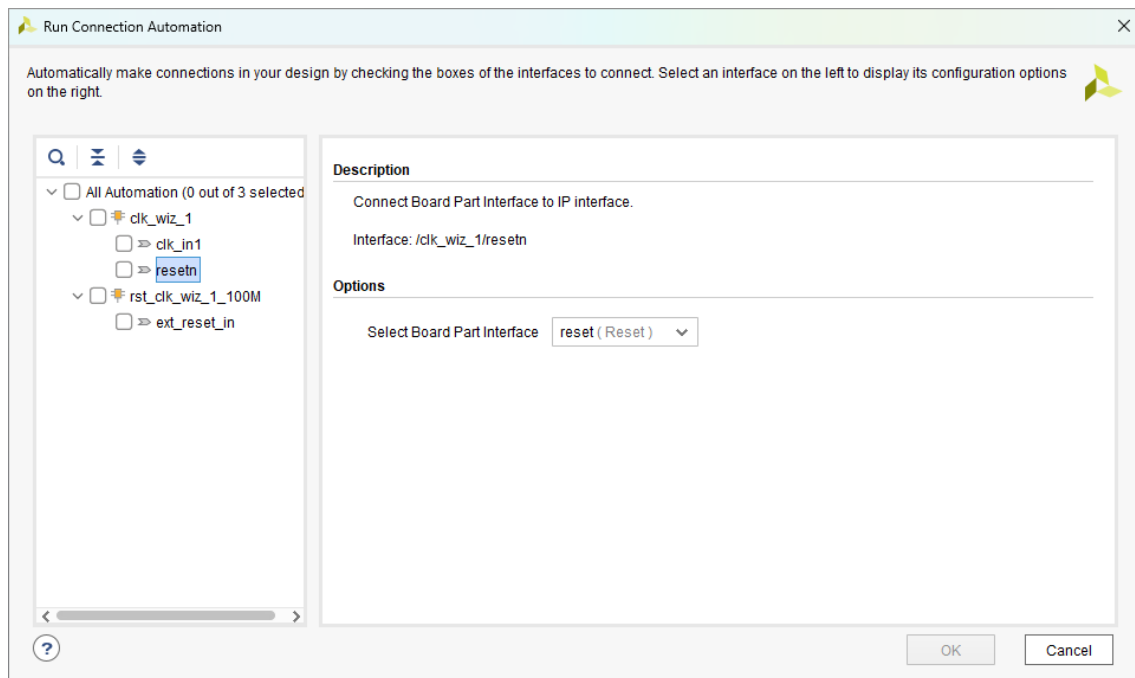
20. The new window shows you the module pins that have not been connected.



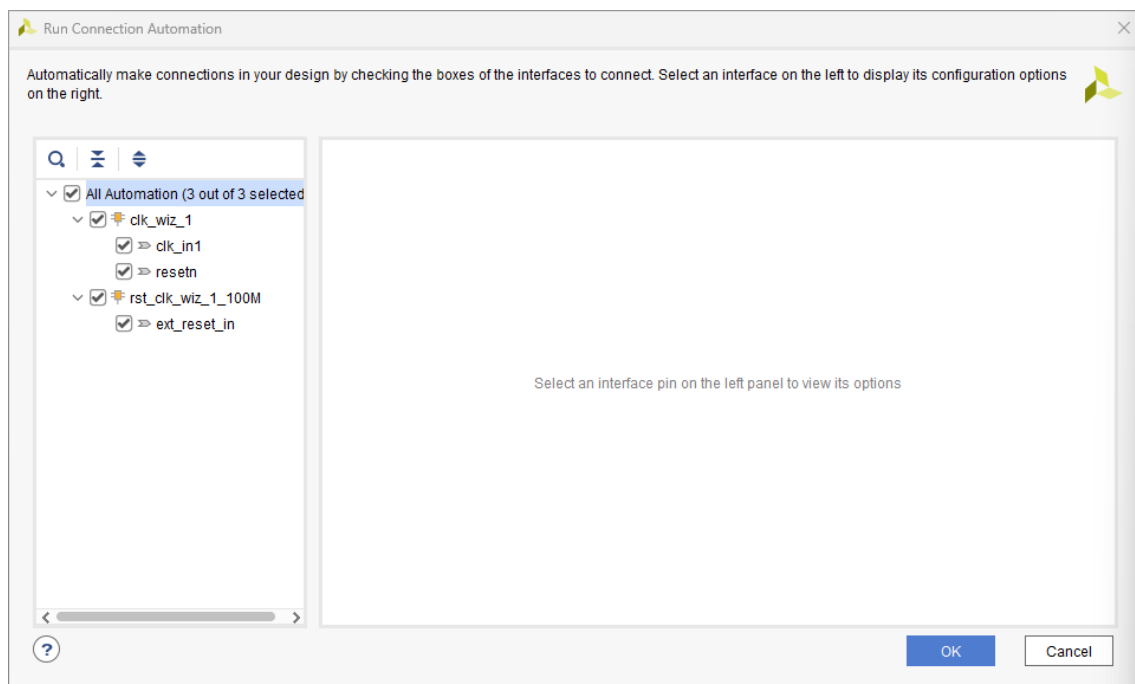
21. Verify for **clk\_in1** if the **Select Board Part Interface** matches **sys clock**; change it if not.



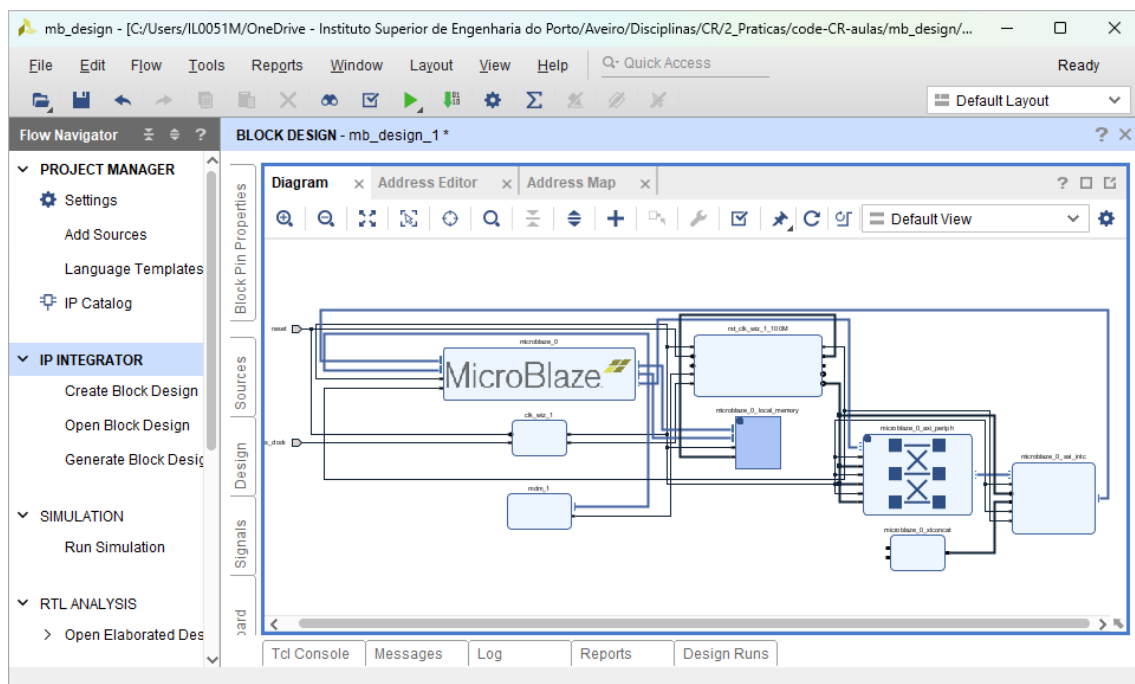
22. Similarly for the **reset** pins, check if it connects to the reset signal of the board.



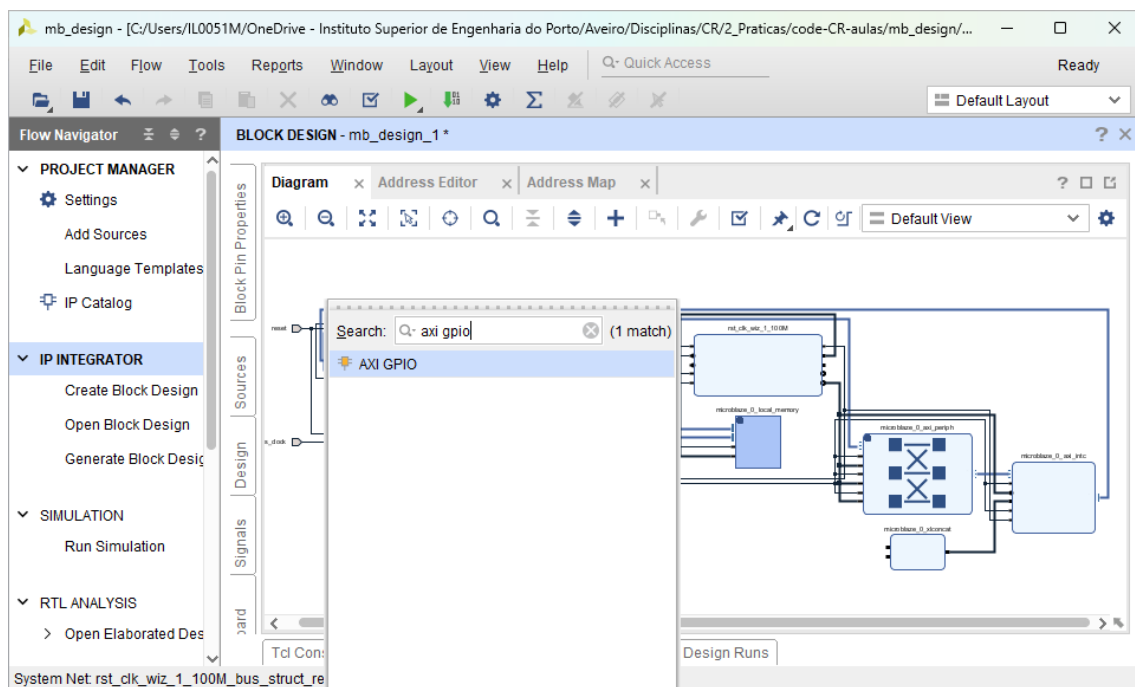
23. Tick all the boxes. Click **OK**.



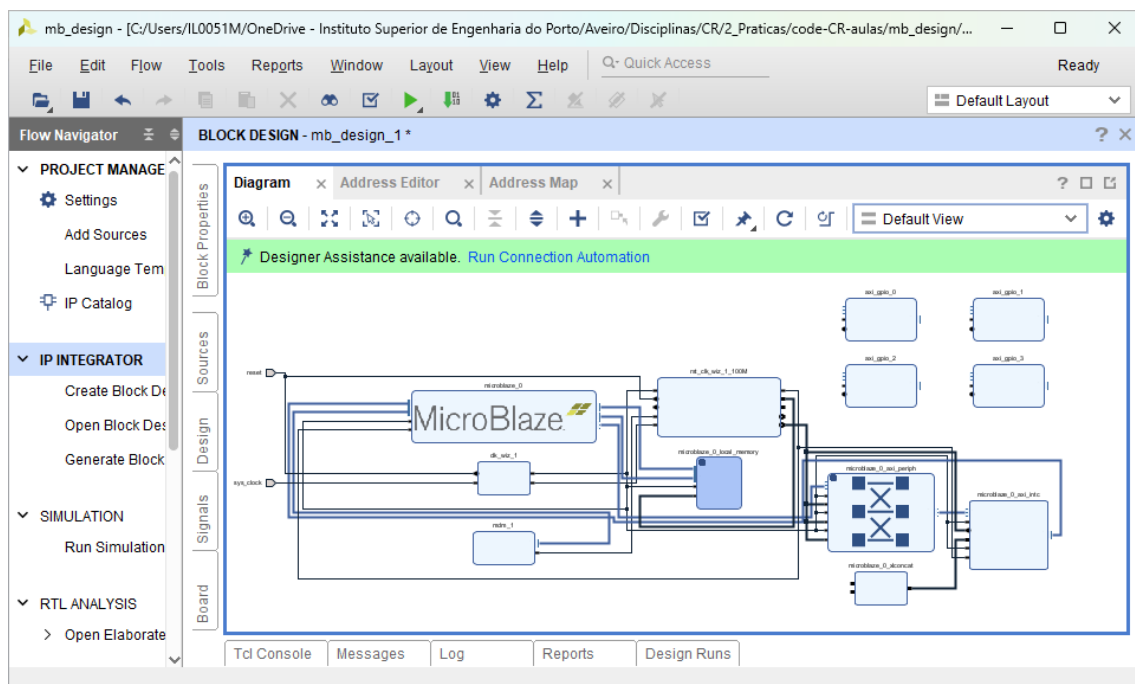
24. Click the + sign to add more blocks.



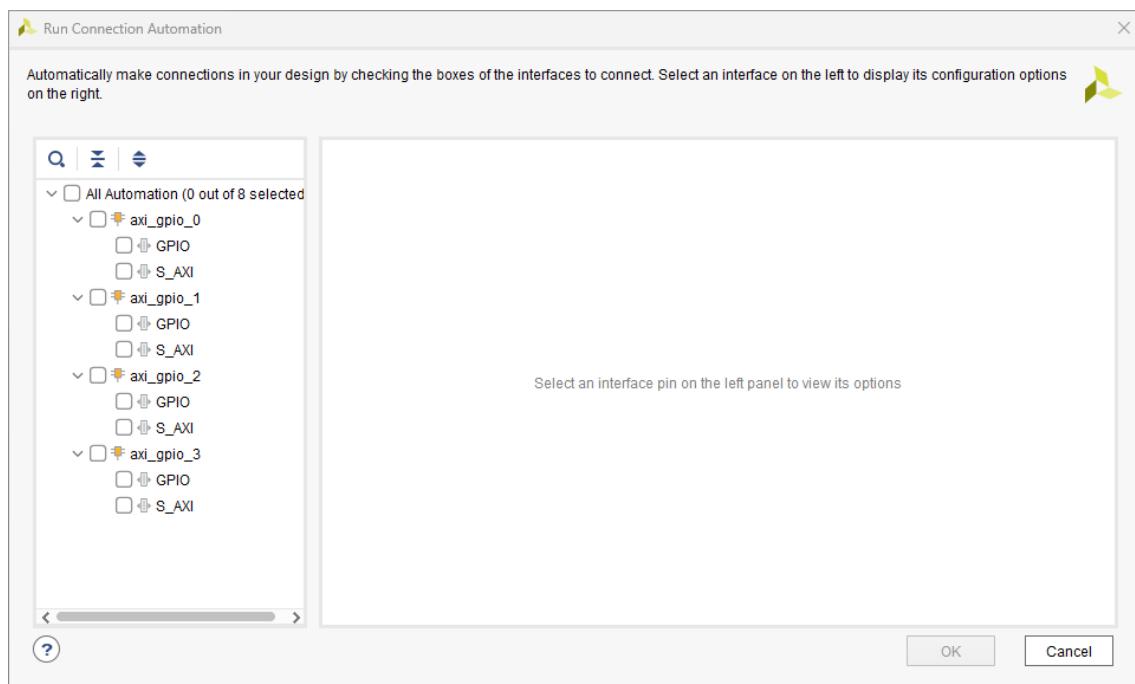
25. Add 4 **AXI GPIO** blocks.



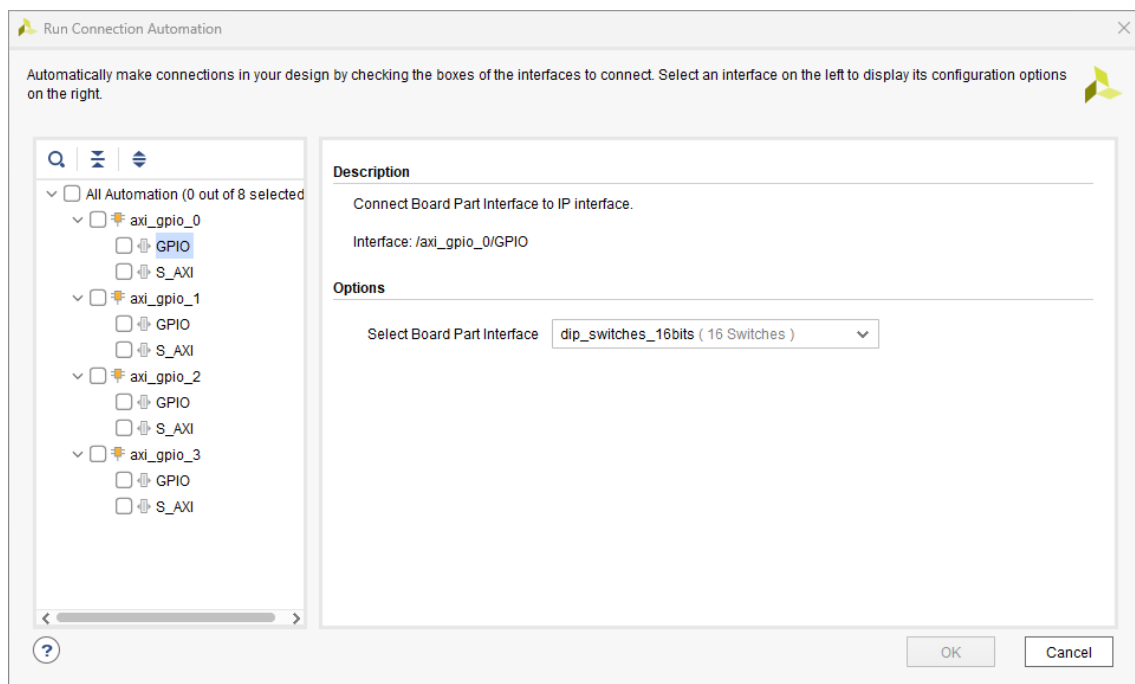
26. Click **Run Connection Automation**.



27. The list of unconnected pins shows up.



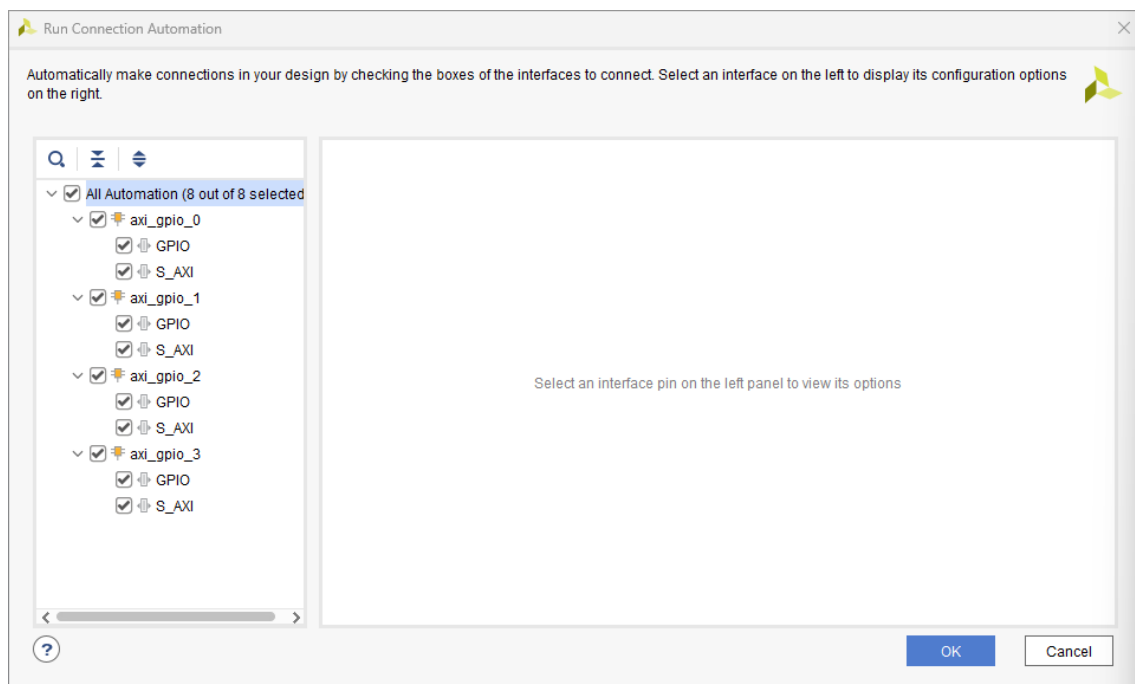
28. Select **dip\_switches\_16bits** for the first GPIO.



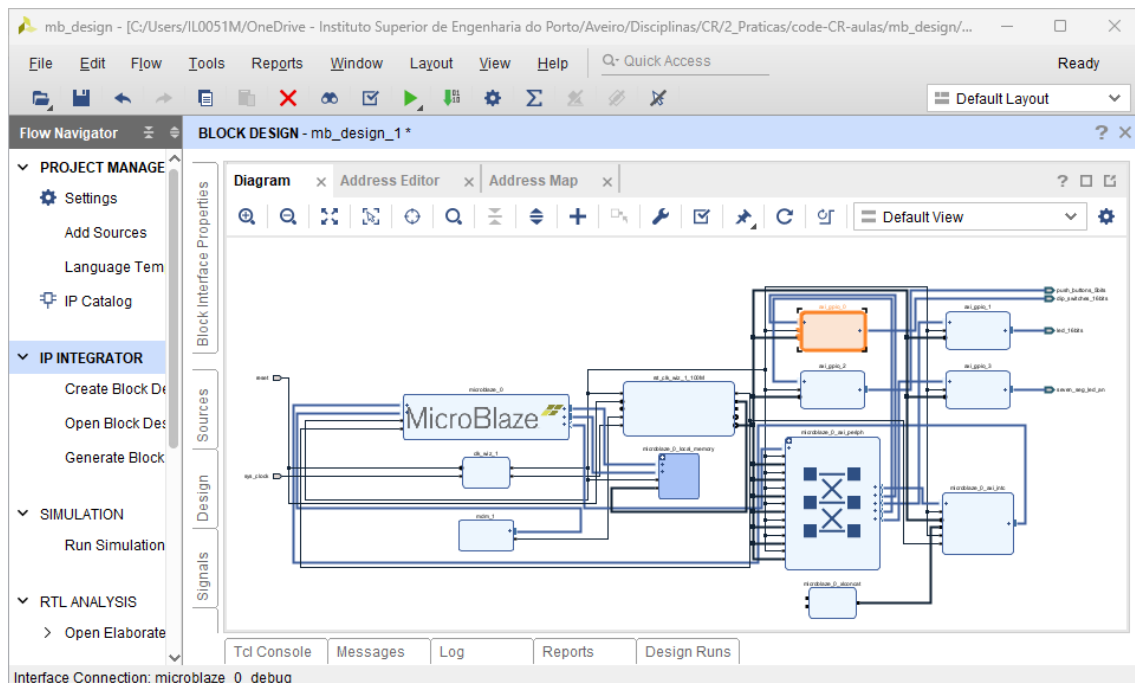
For the other 3, select:

1. **led\_16bits**
2. **push\_buttons**
3. **seven\_seg\_led\_an**

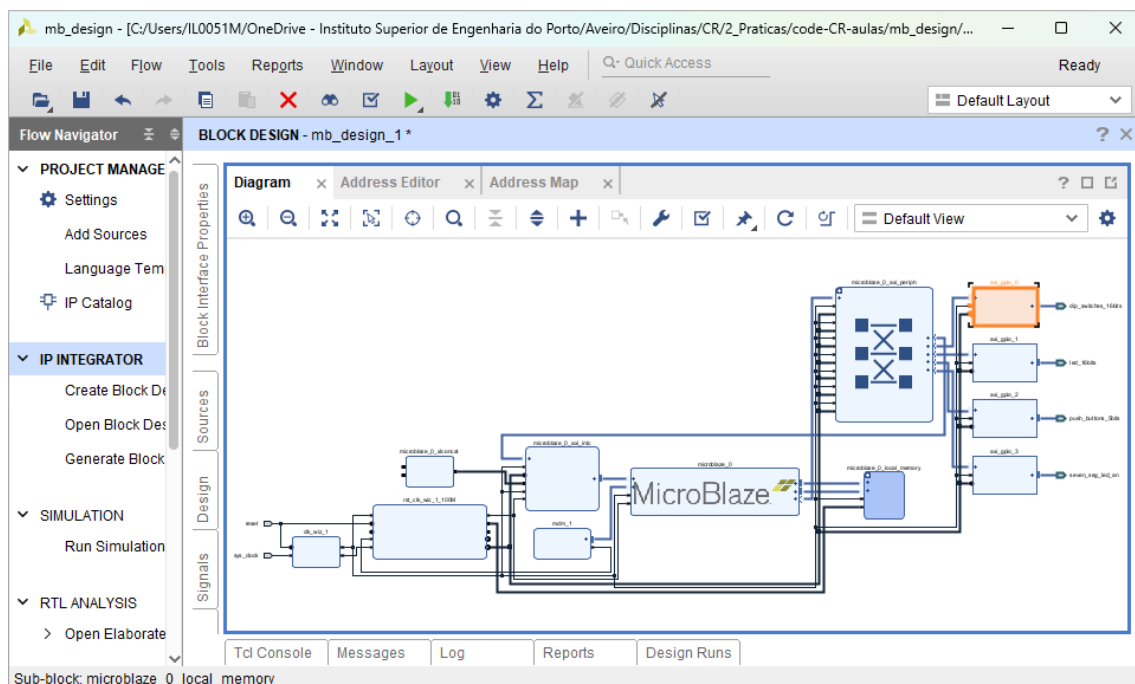
29. Tick all boxes. Click **OK**.



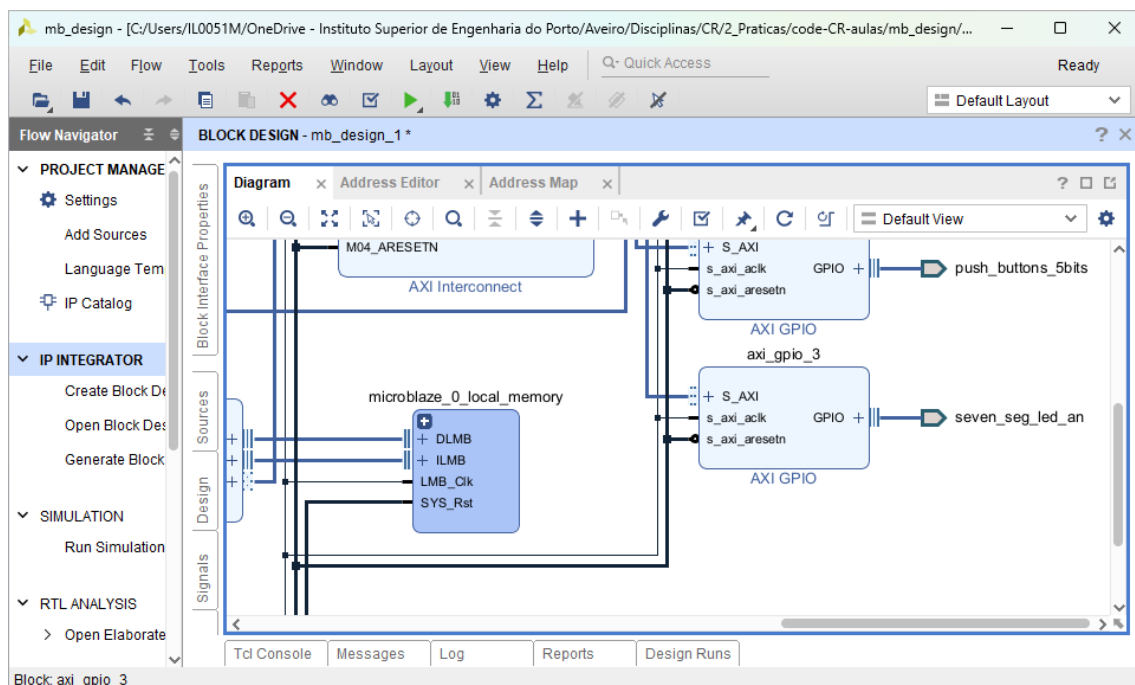
30. The new AXI GPIO blocks should appear connected. Hit the **Regenerate Layout** button.



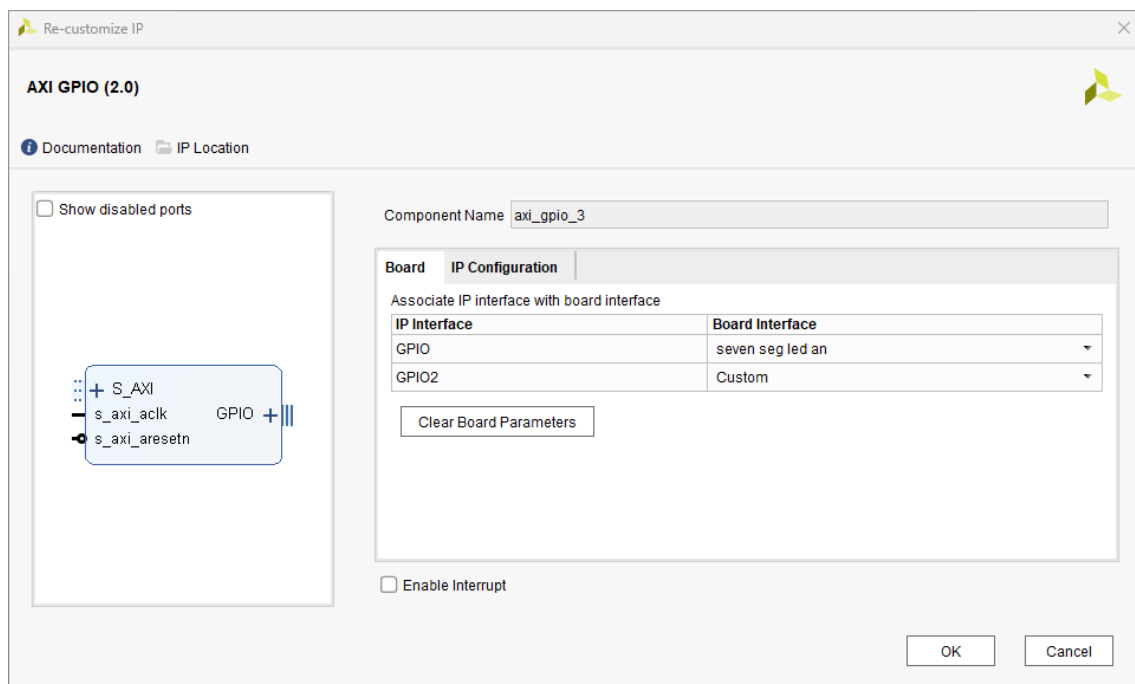
31. The new layout is presented.



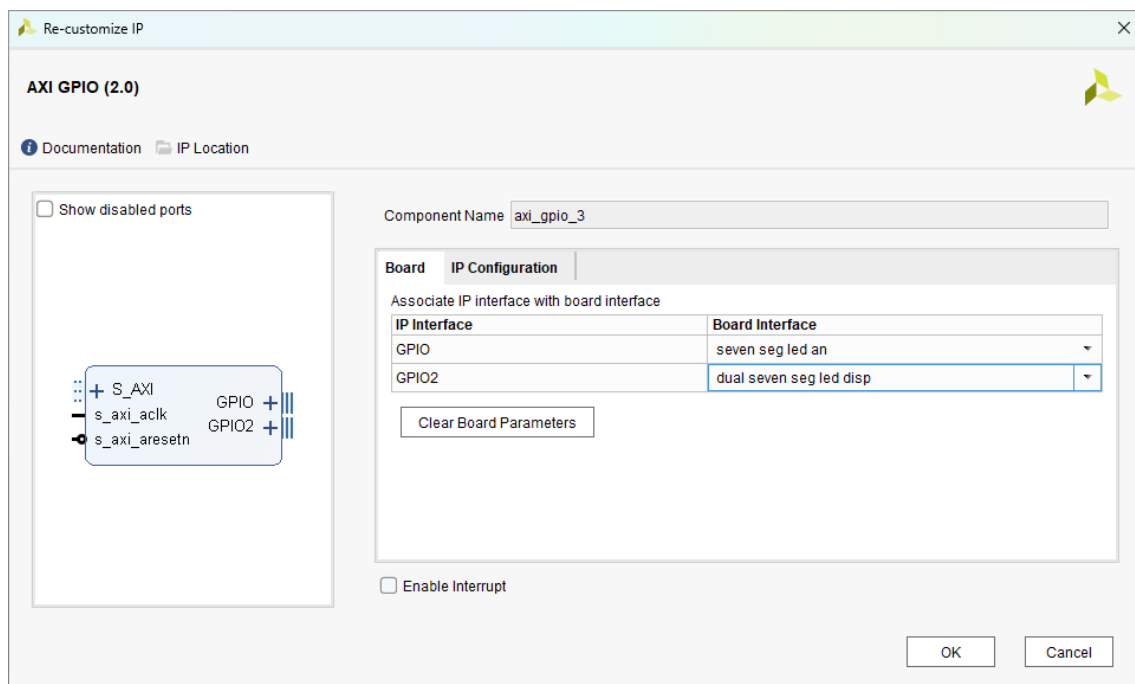
32. Zoom in on the AXI GPIO connected to the **seven\_seg\_led\_an** signal. Right-click on it.



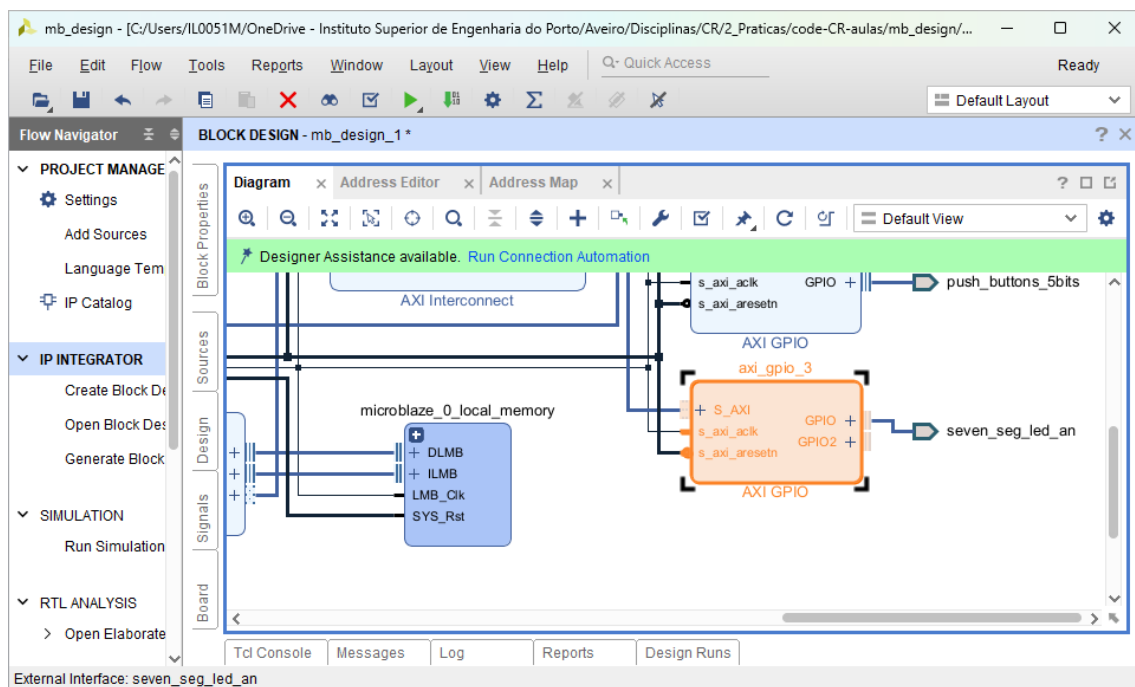
33. A new window shows up.



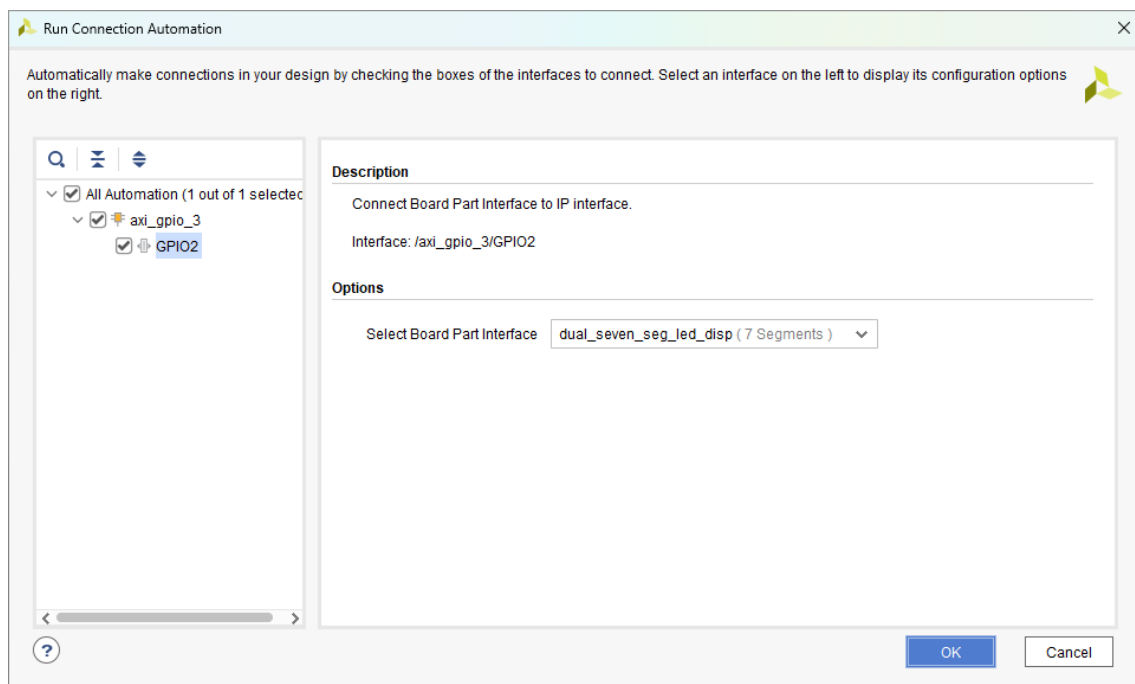
34. Select **dual\_seven\_seg\_led\_disp** for GPIO2. Click **OK**.



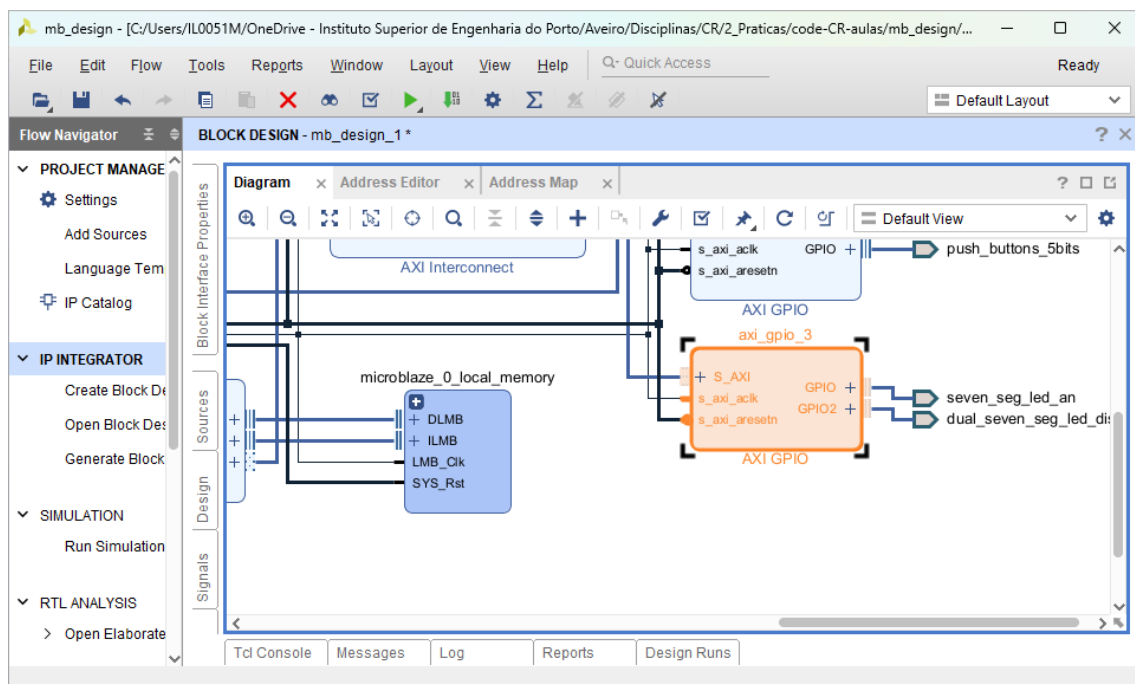


35. Click on **Run Connection Automation**.

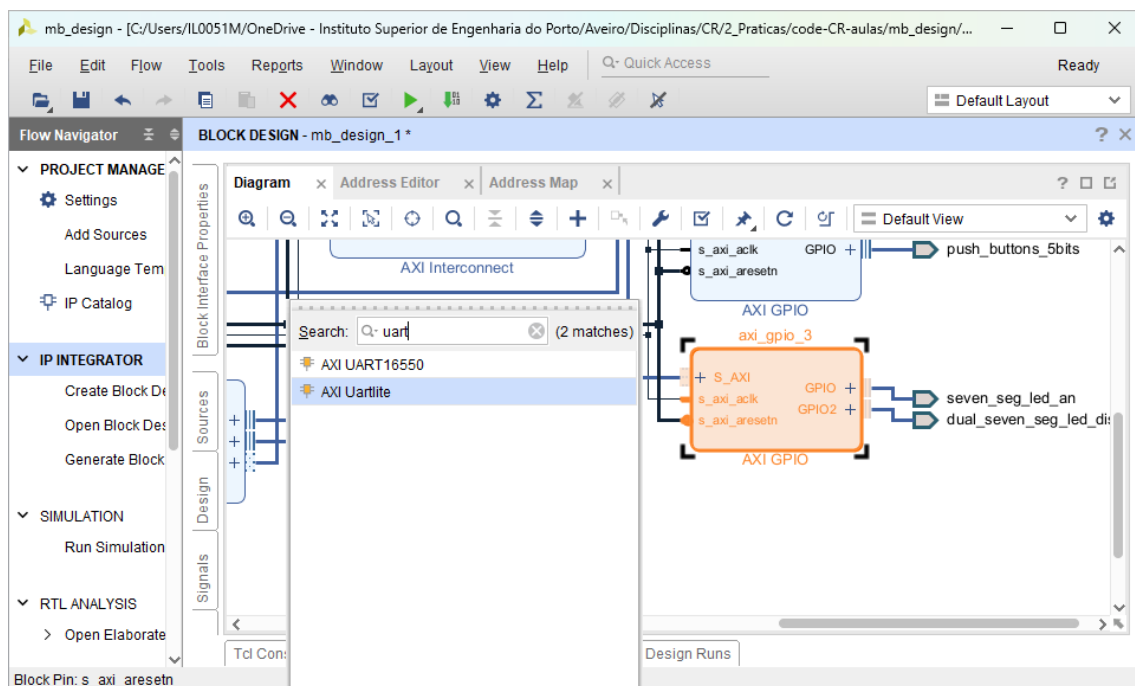
## 36. Select the same interface for the unconnected GPIO2 pins.



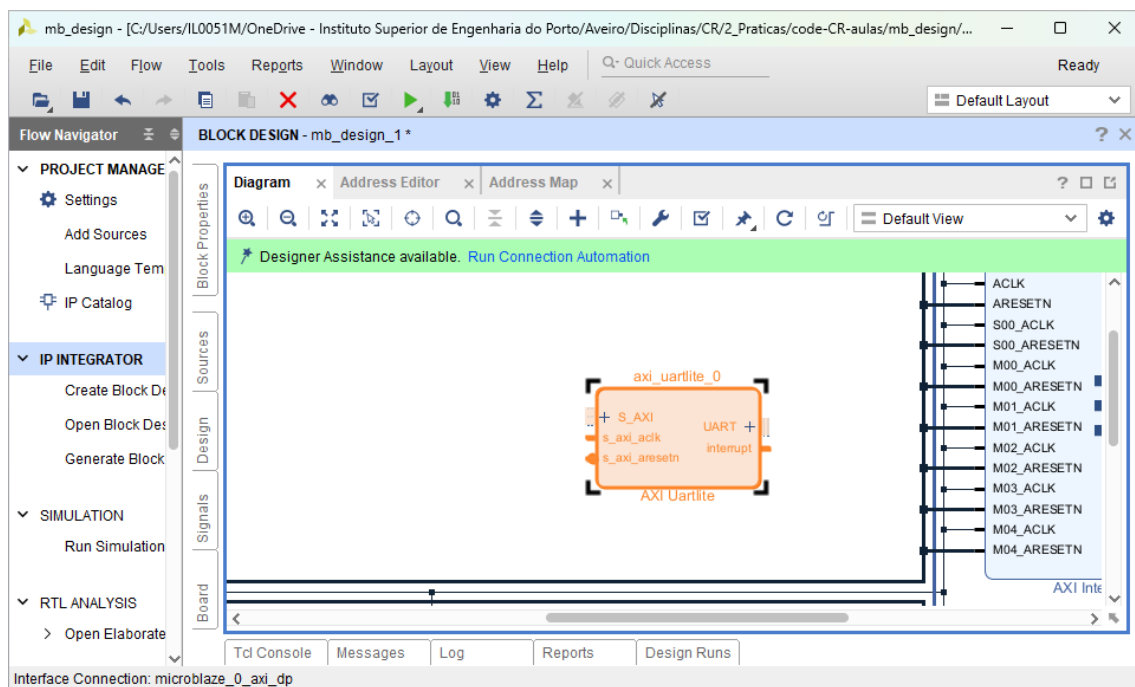
37. Click on the + sign to add a UART module.



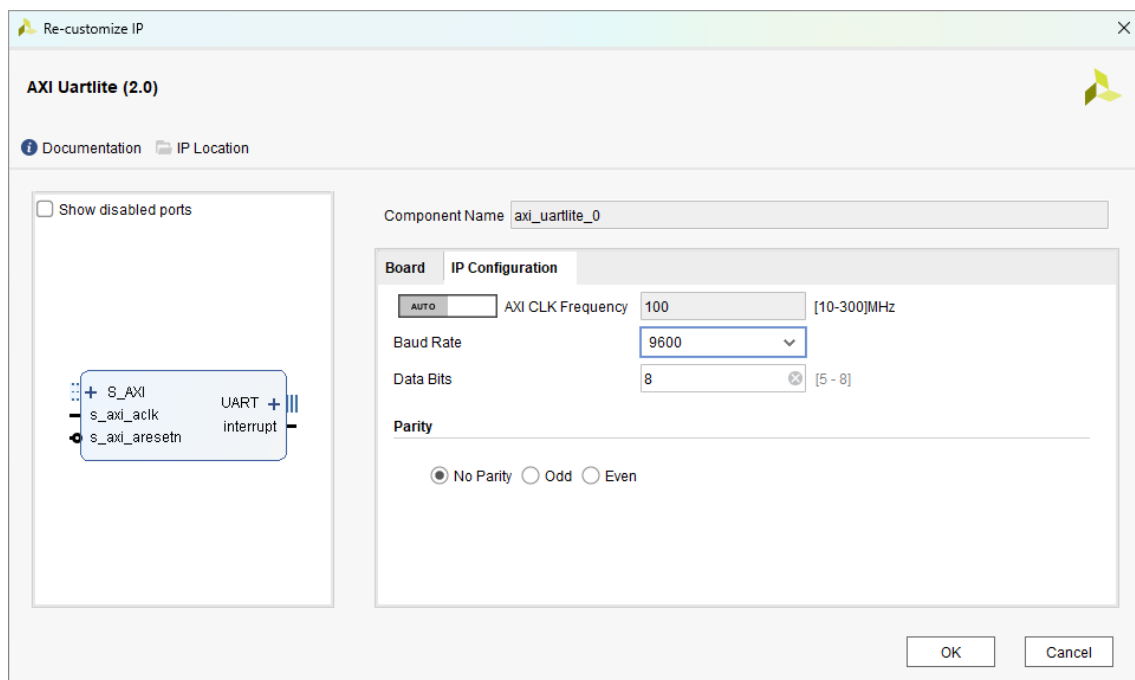
38. Select the **AXI Uartlite** from the dropdown menu.



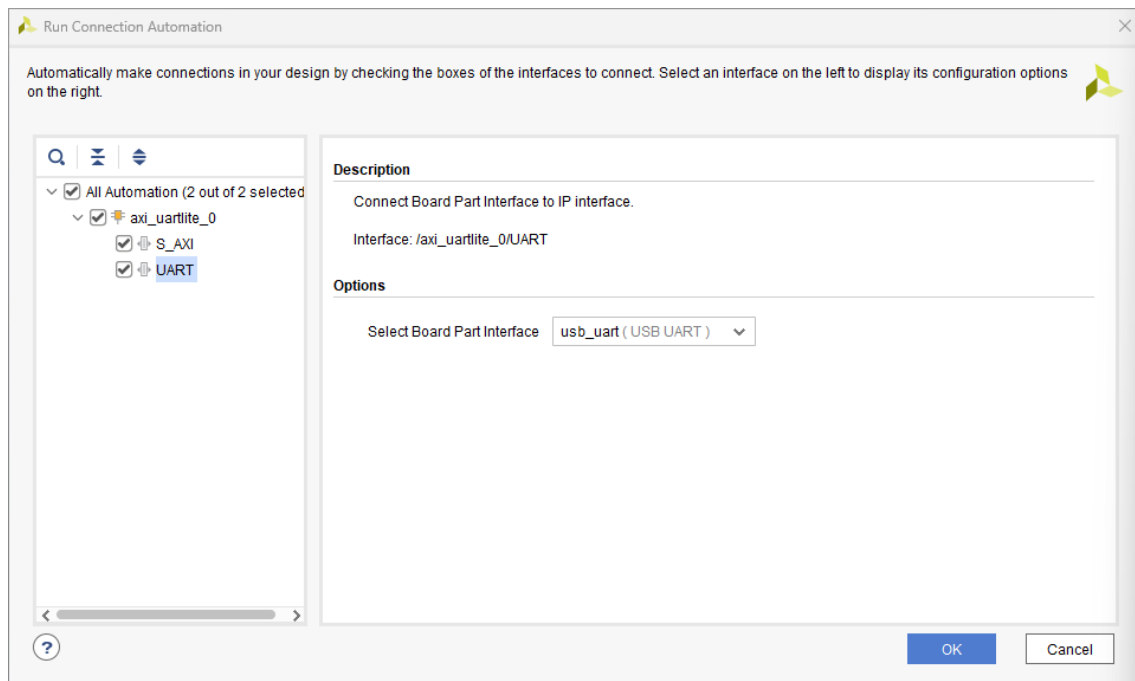
39. Right-click on it.



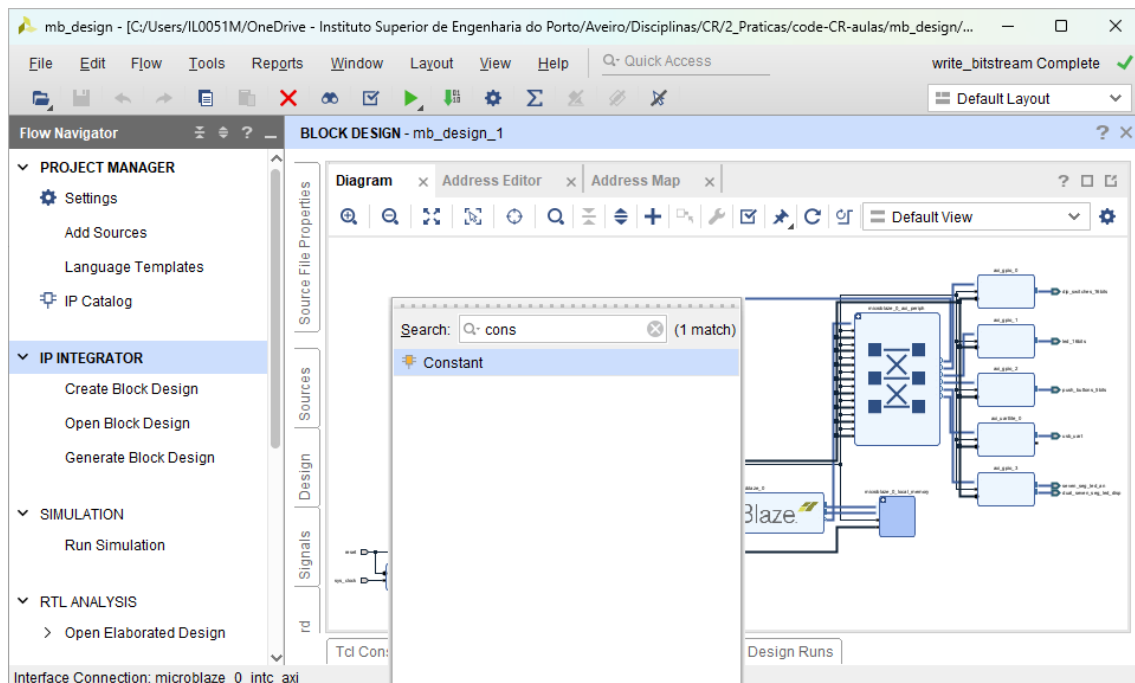
40. Inspect the serial communication parameters. Just register them, do not change anything. Click **OK**.



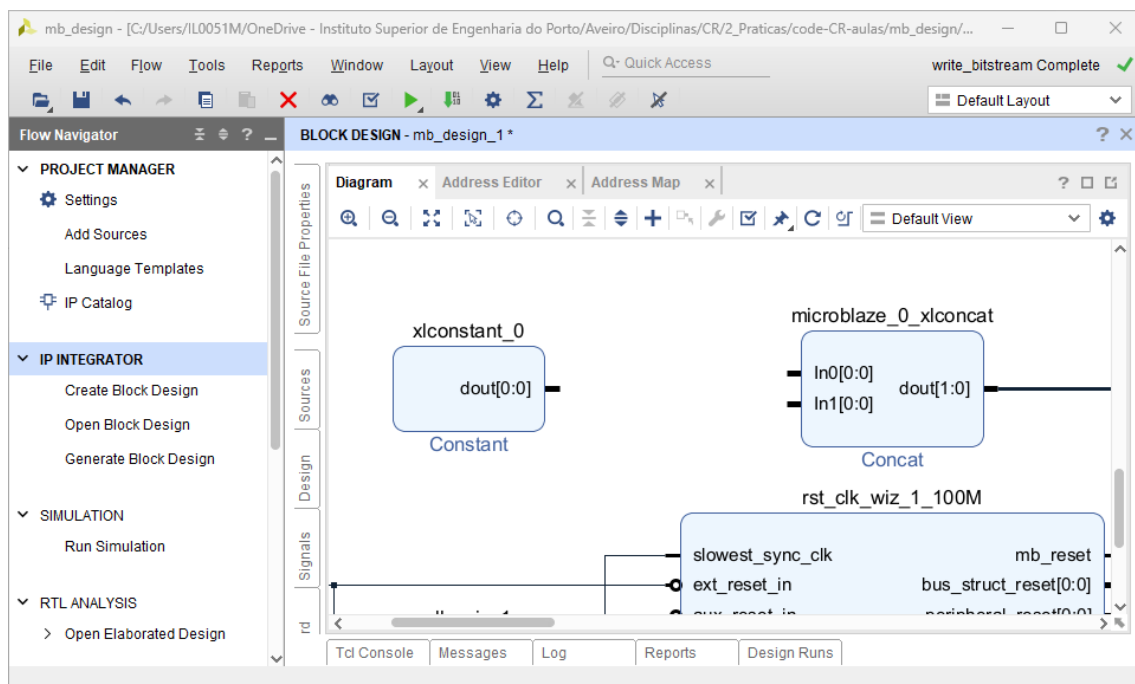
41. Click on **Run Connection Automation**. Connect the UART to the corresponding board interface.



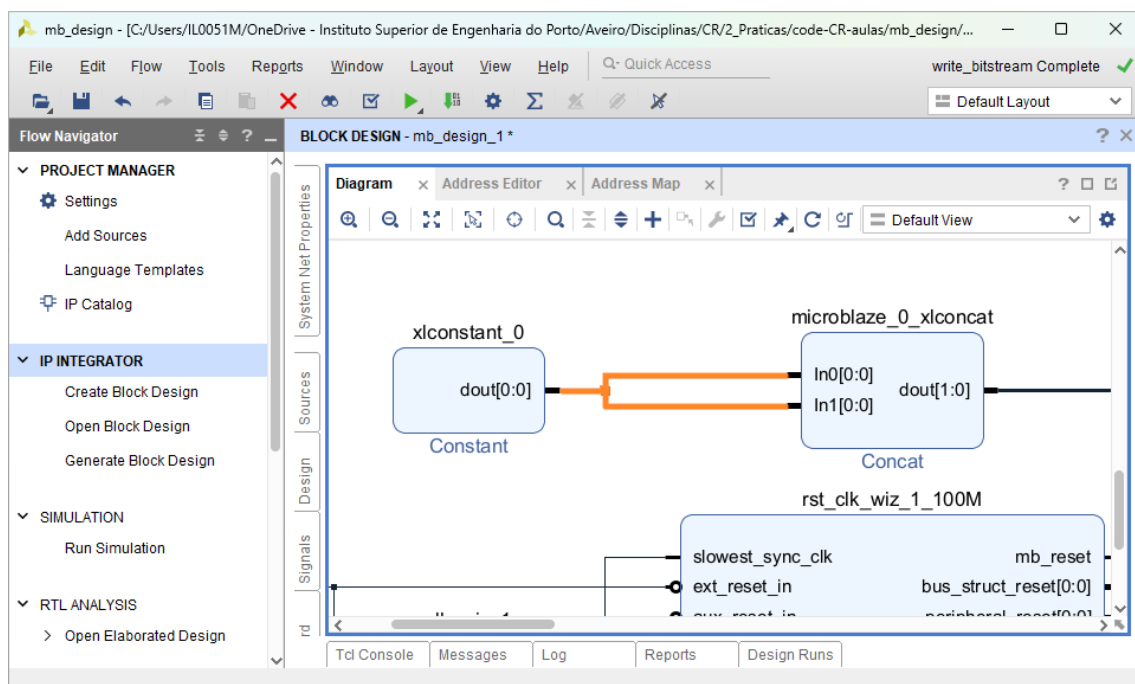
42. Click on the + sign. Add a **Constant** module.



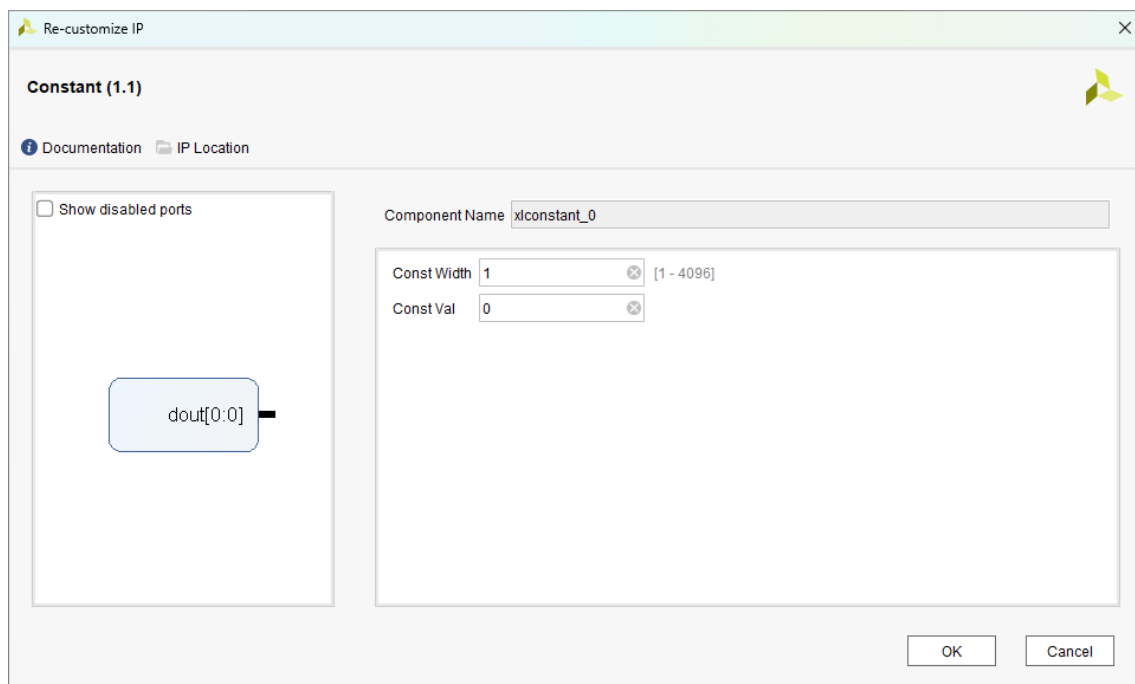
43. Place it next to the **xlconcat** module.



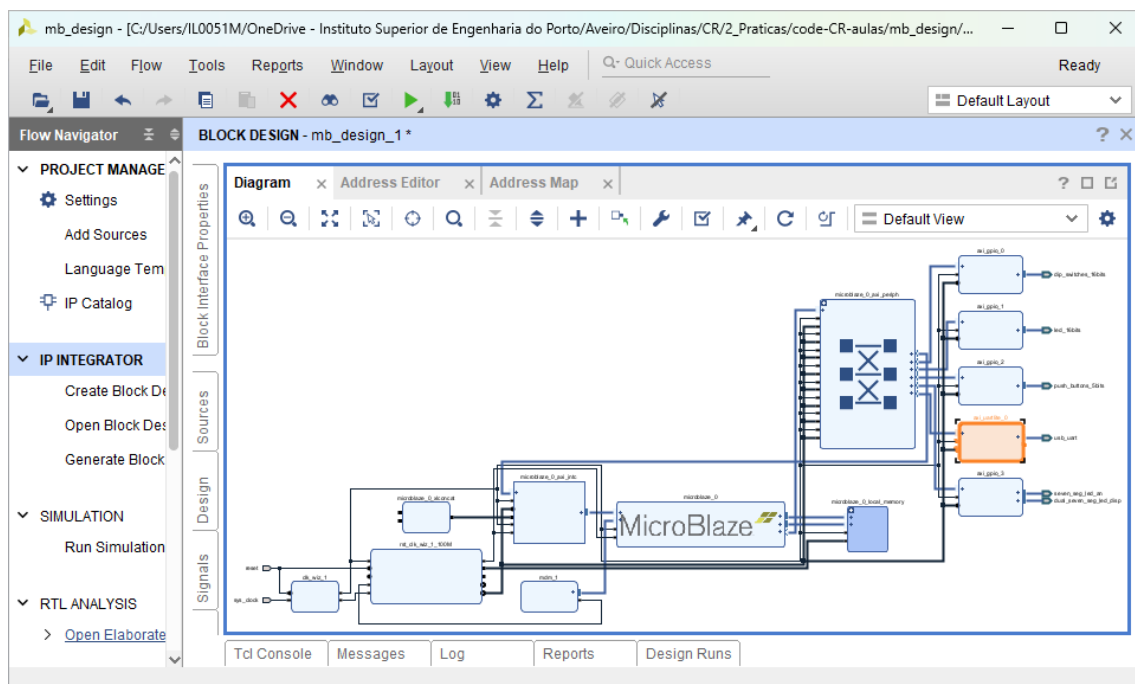
44. Connect its output to the inputs of the **xlconcat** module. Right click on the **xlconstant** module.

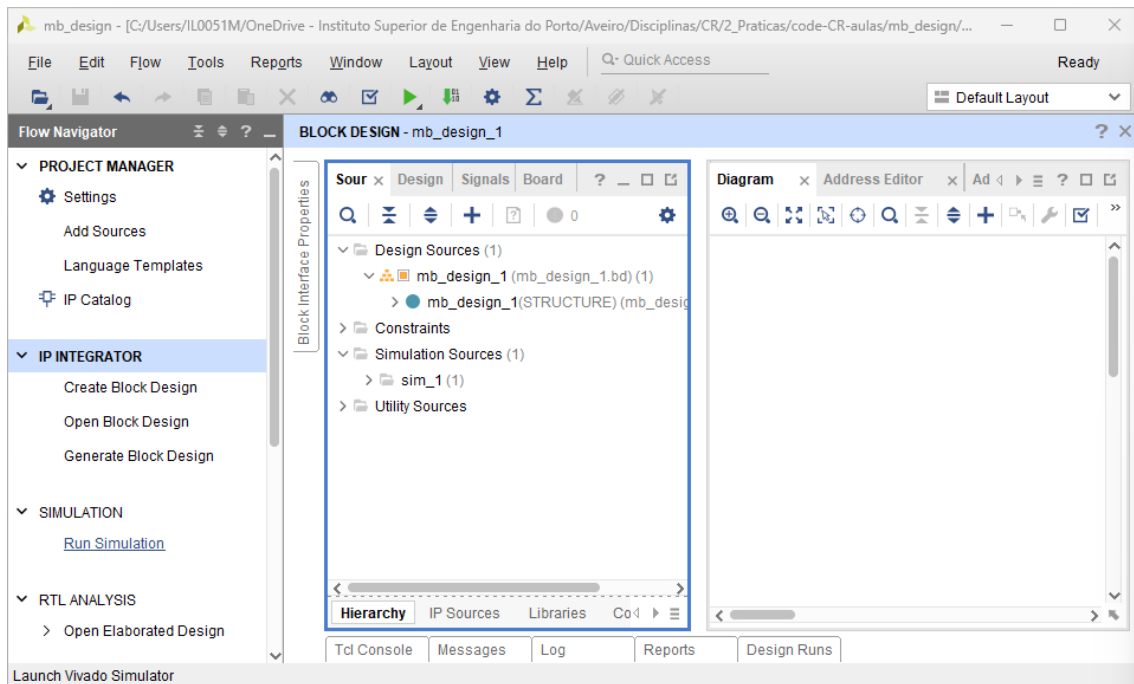
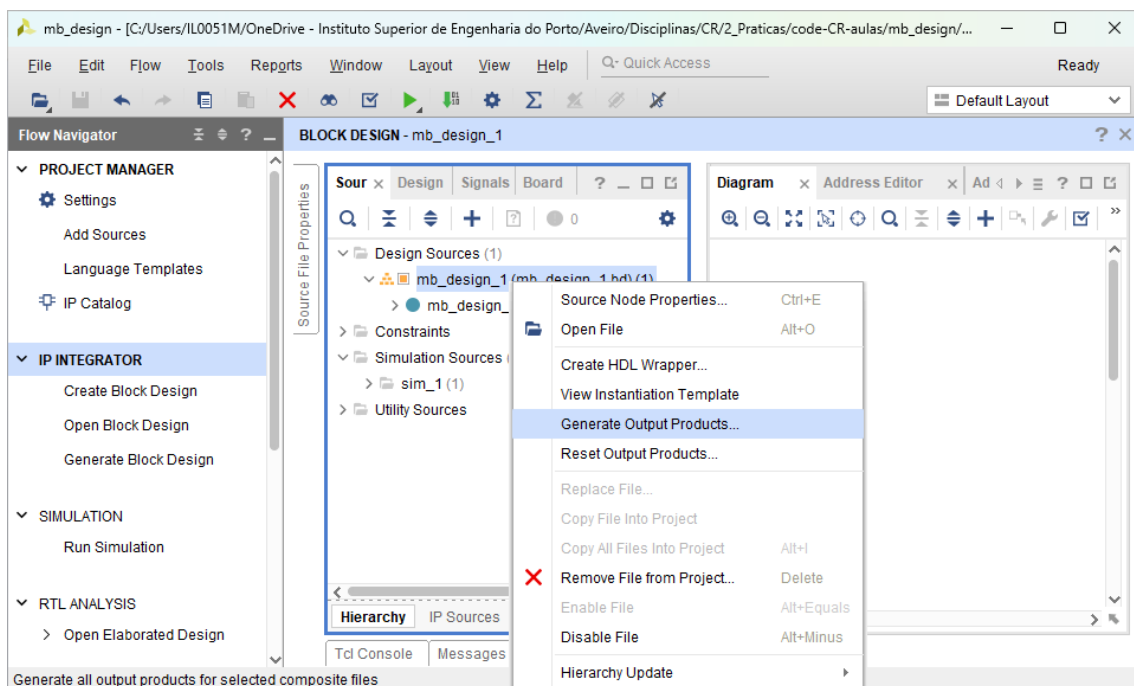


45. Change the **Const Val** field from **1** to **0**.

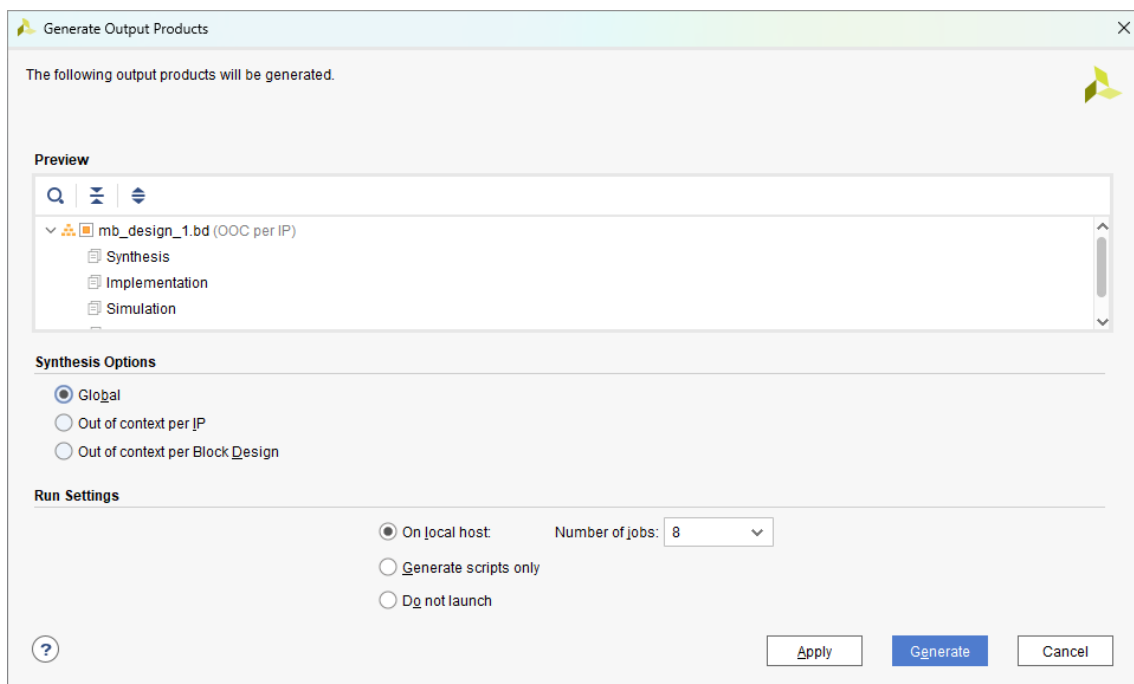


46. Click on **Regenerate Layout**.

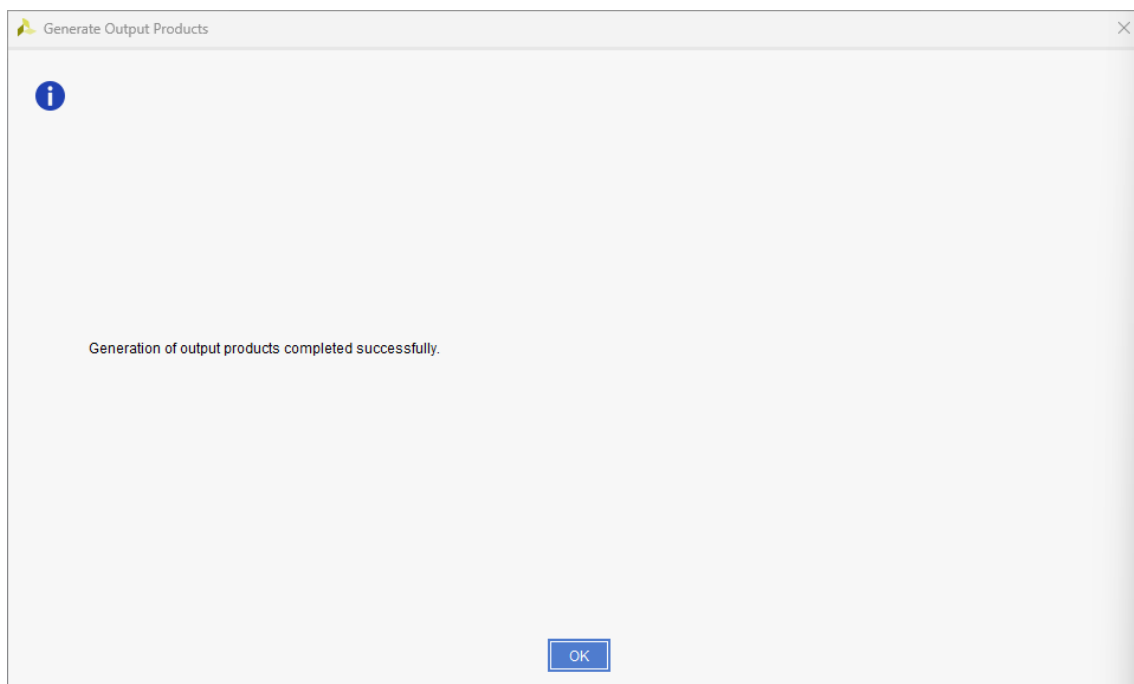


47. Open the **Sources** tab.48. Select **Generate Output Products**.

49. Under **Synthesis Options**, select **Global**. Click **Generate**.

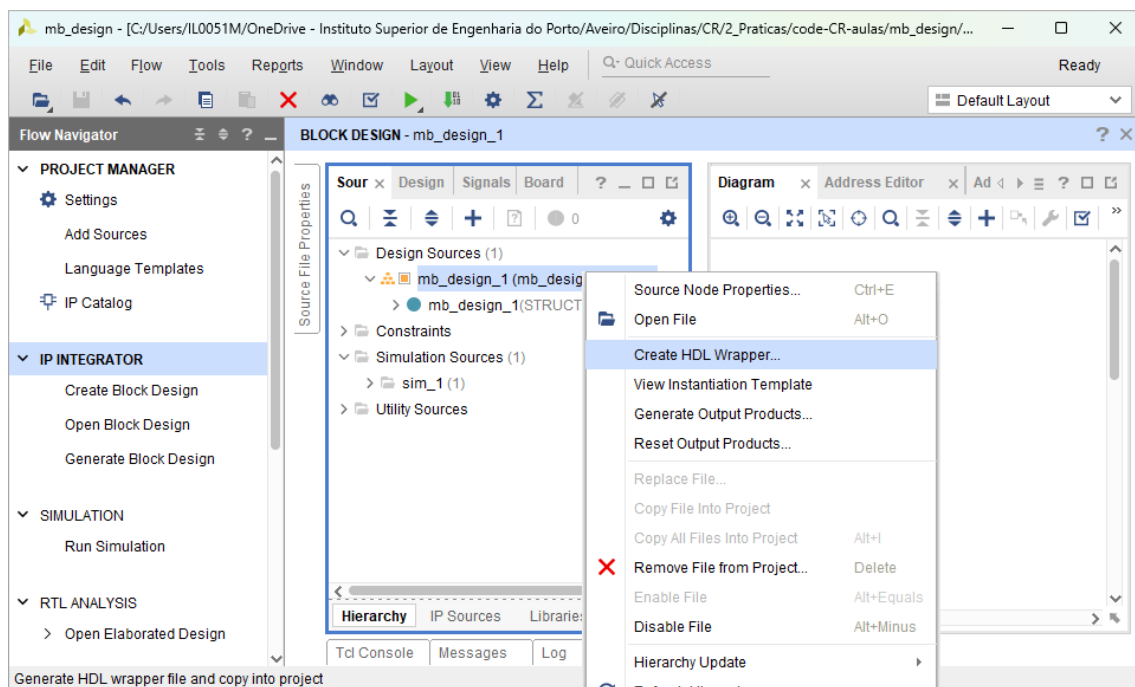


50. Click **OK**.

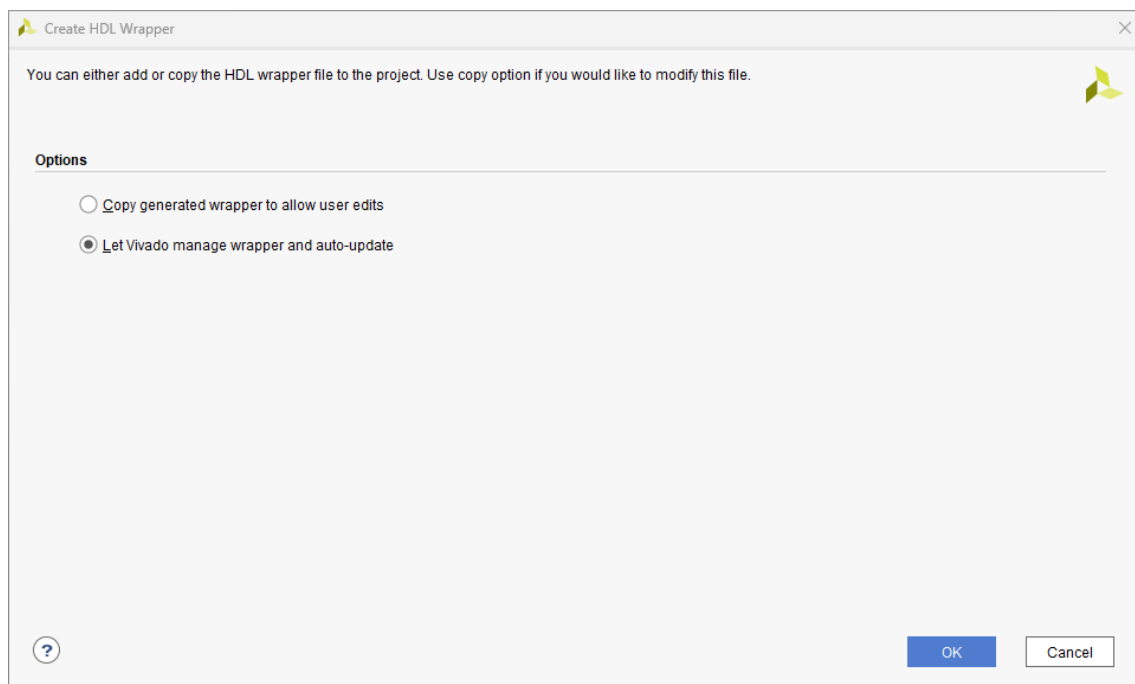




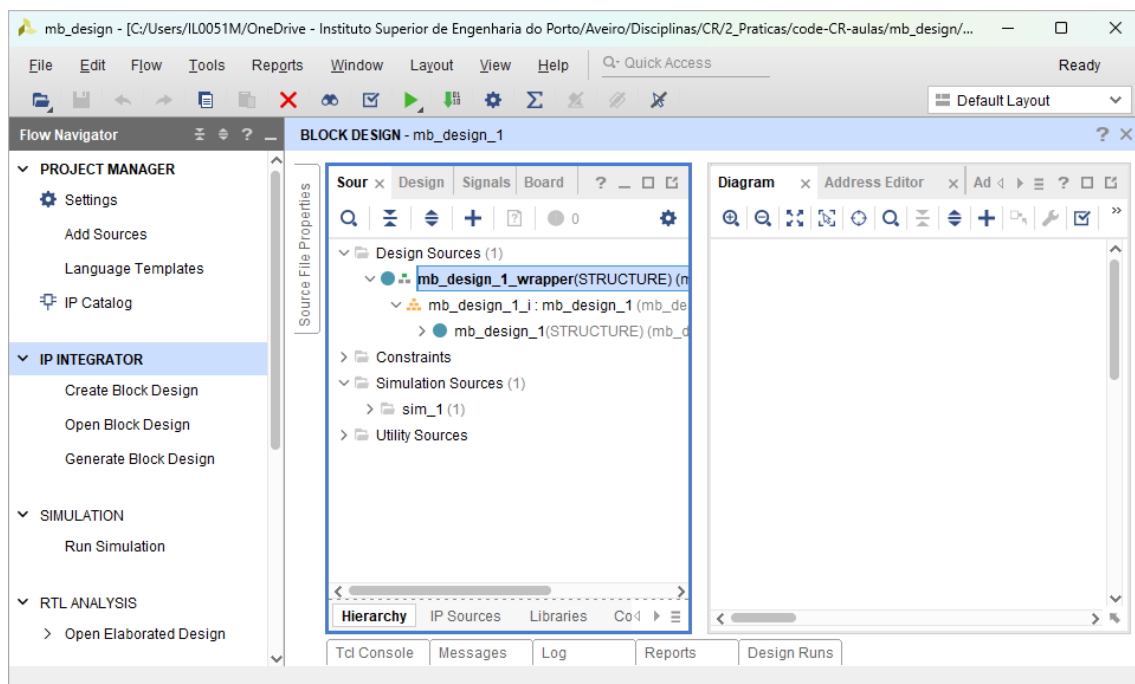
## 51. Select **Create HDL Wrapper**.



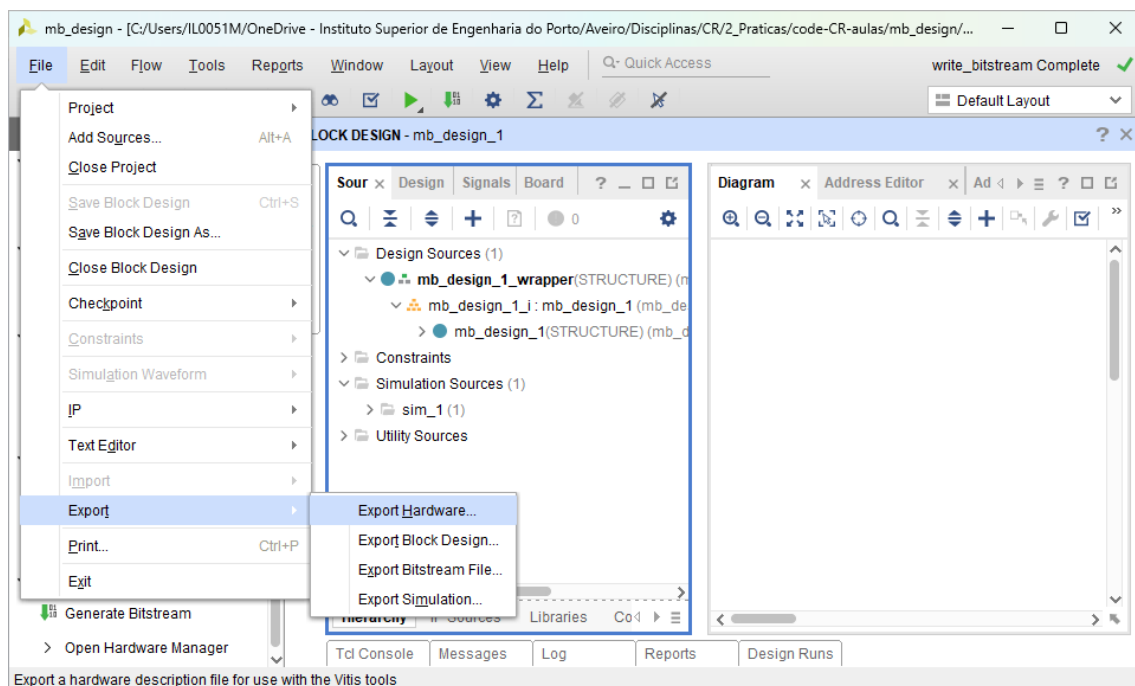
## 52. Verify this option. Click **OK**.

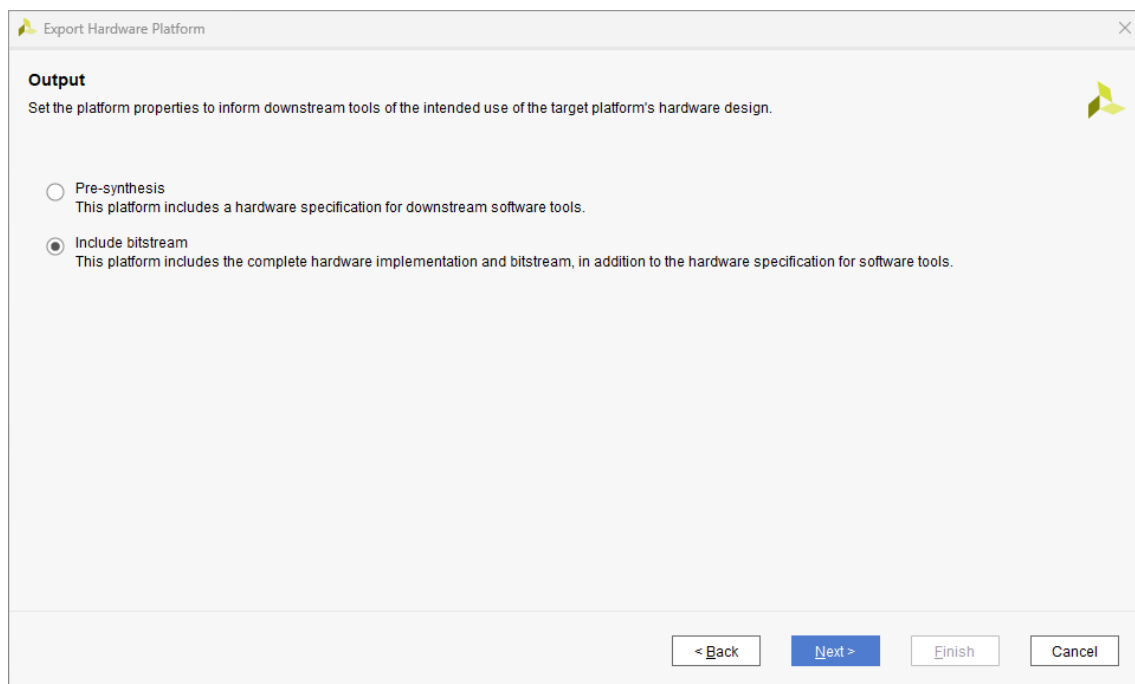
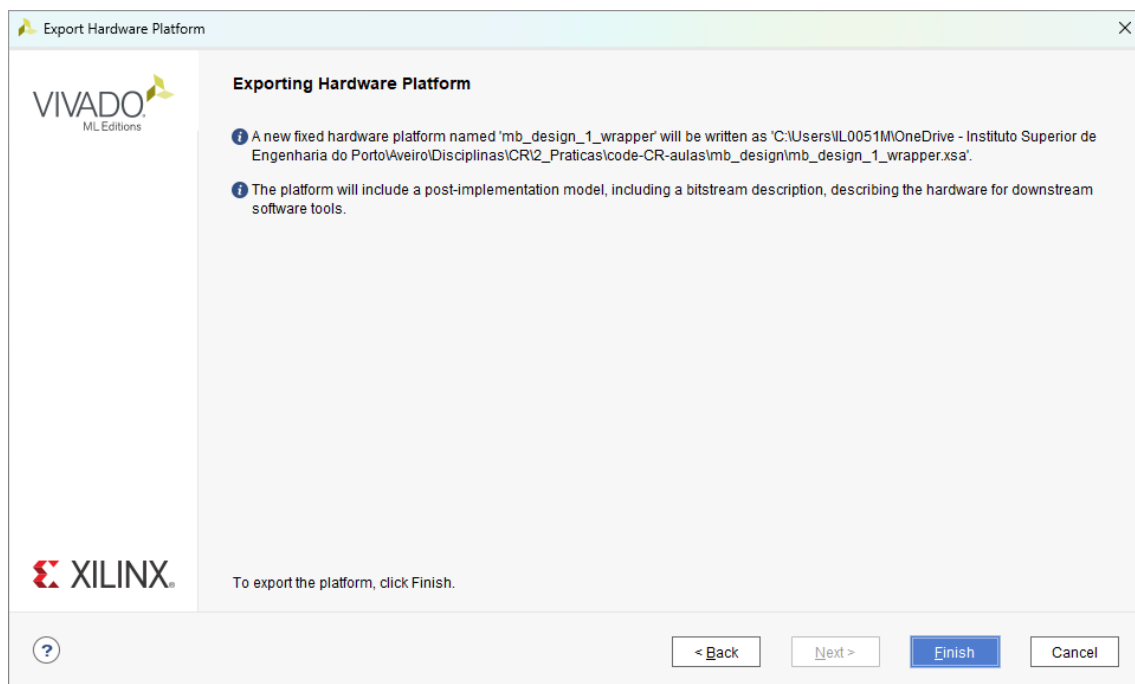


53. Run all flow steps. Click **Generate Bitstream**.



54. Once it is done, go to File > Export > Export Hardware.



55. Select **Include Bitstream**.56. Click **Finish**.

**Congratulations!**

Sources: AMD Xilinx documentation.