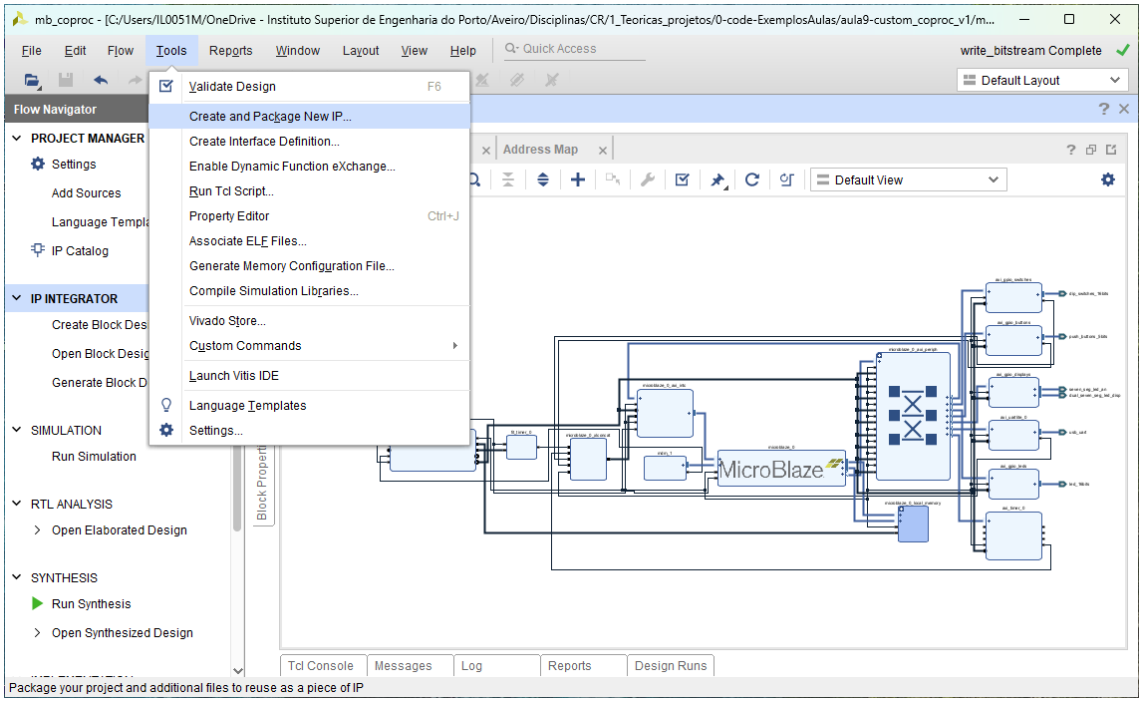
Tutorial 5

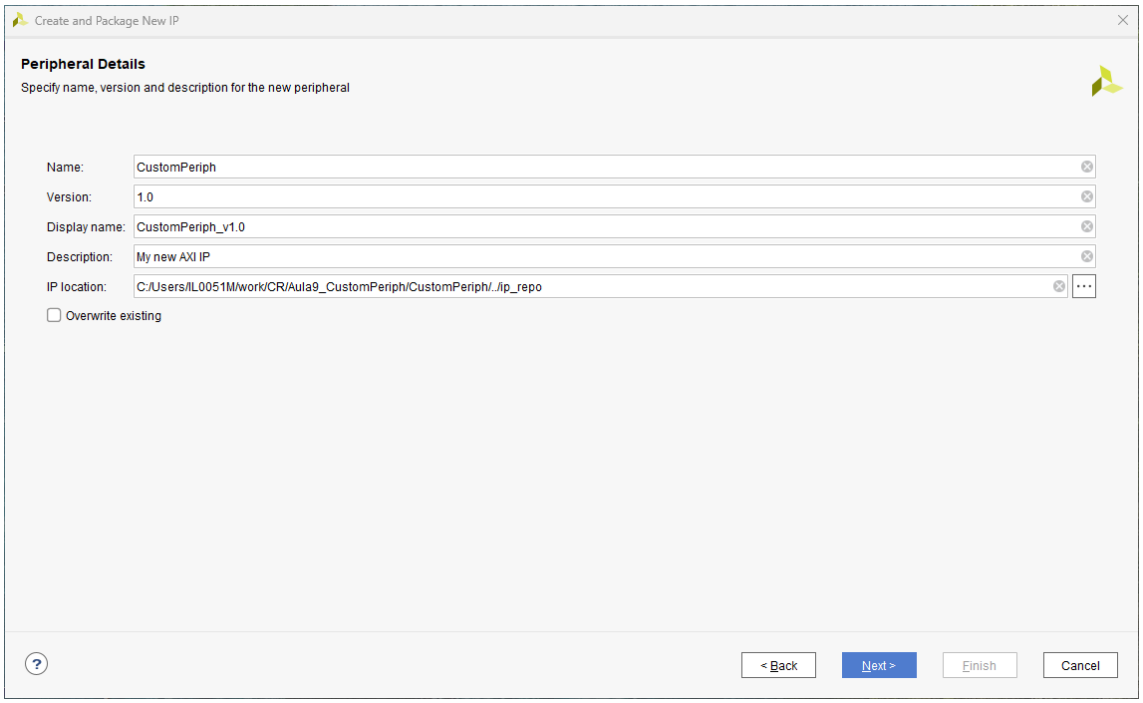
Update MicroBlaze Platform with a Custom Peripheral (RGB LED controller) connected via AXI-Lite – HW project (VIVADO)

Vivado version: 2022.2

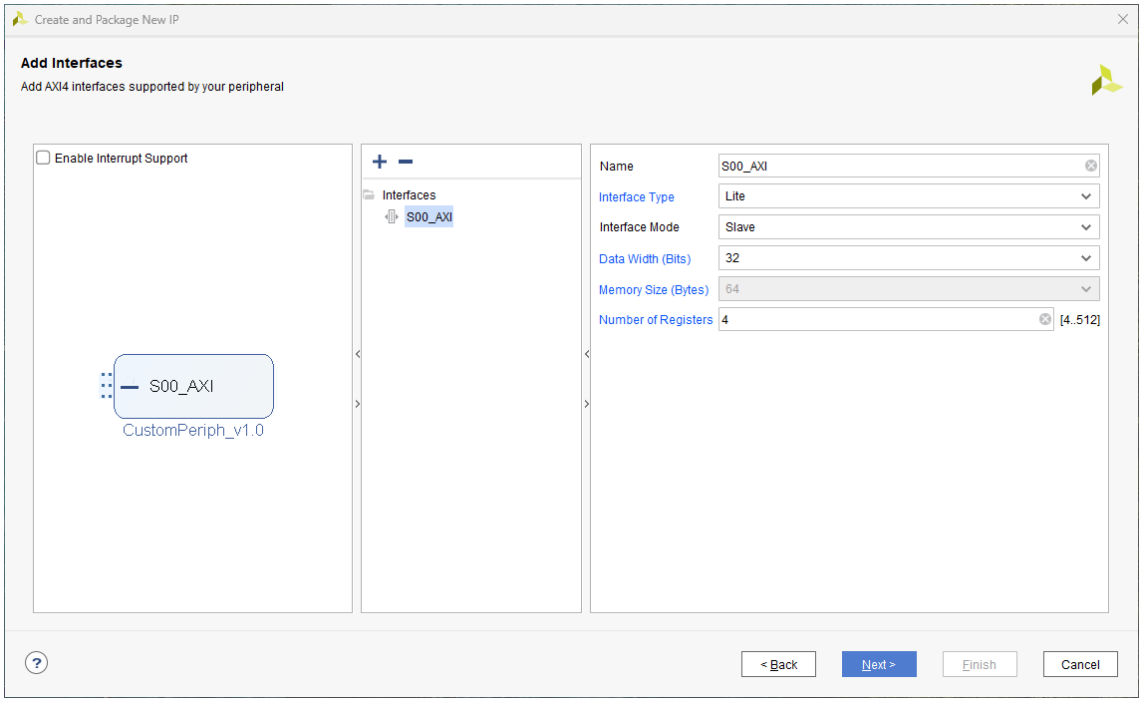
1. Open Vivado and the previous project. Add a new IP block by clicking **Tools** > **Create and Package IP**.



2. Call it **CustomPeriph**. Stick to this name to simplify future steps.

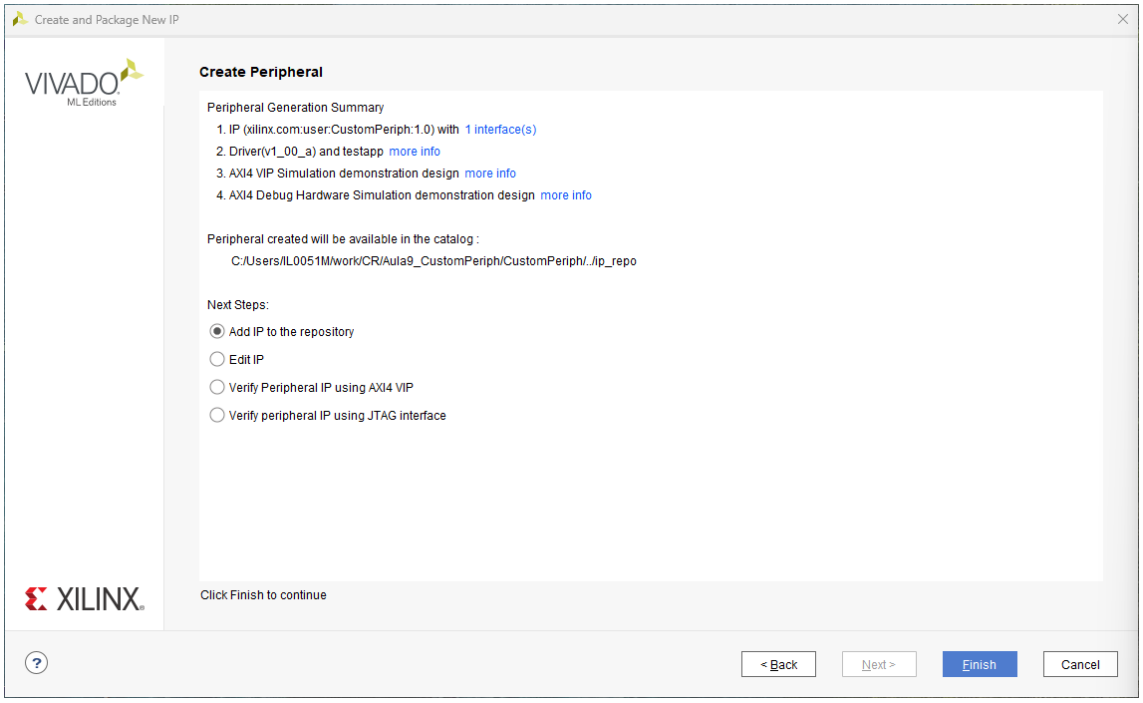


3. No changes in parameters are necessary.

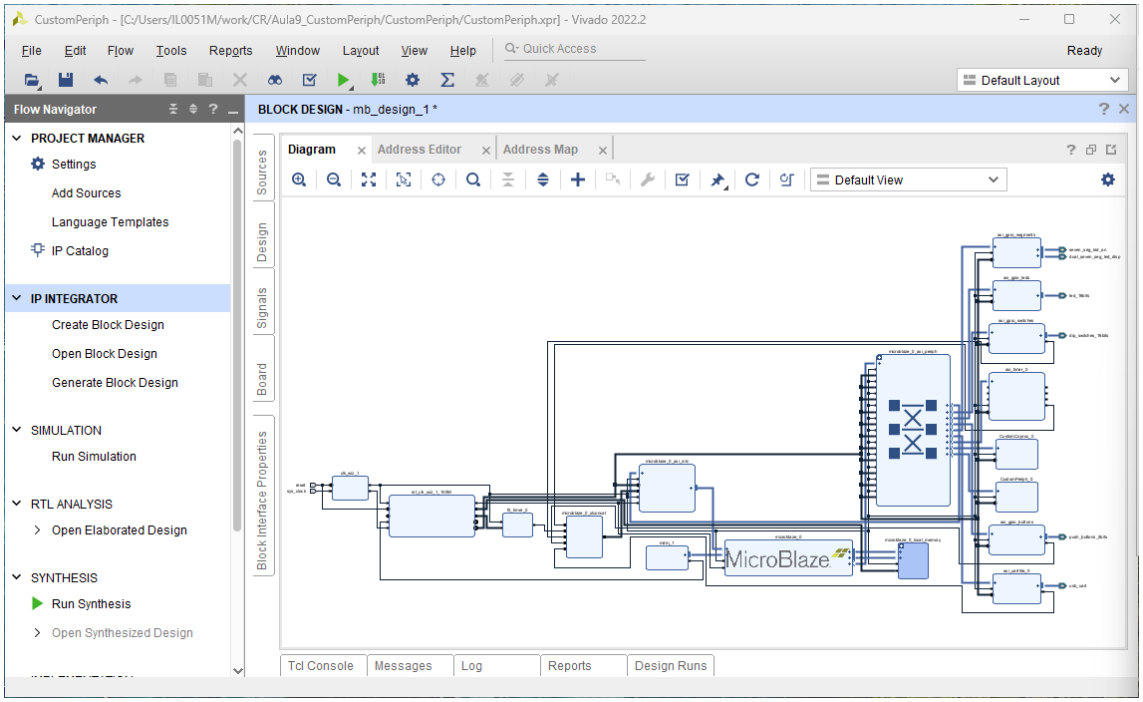


For our purpose, we don't need 4 registers. However, we cannot have less, so we leave it as is.

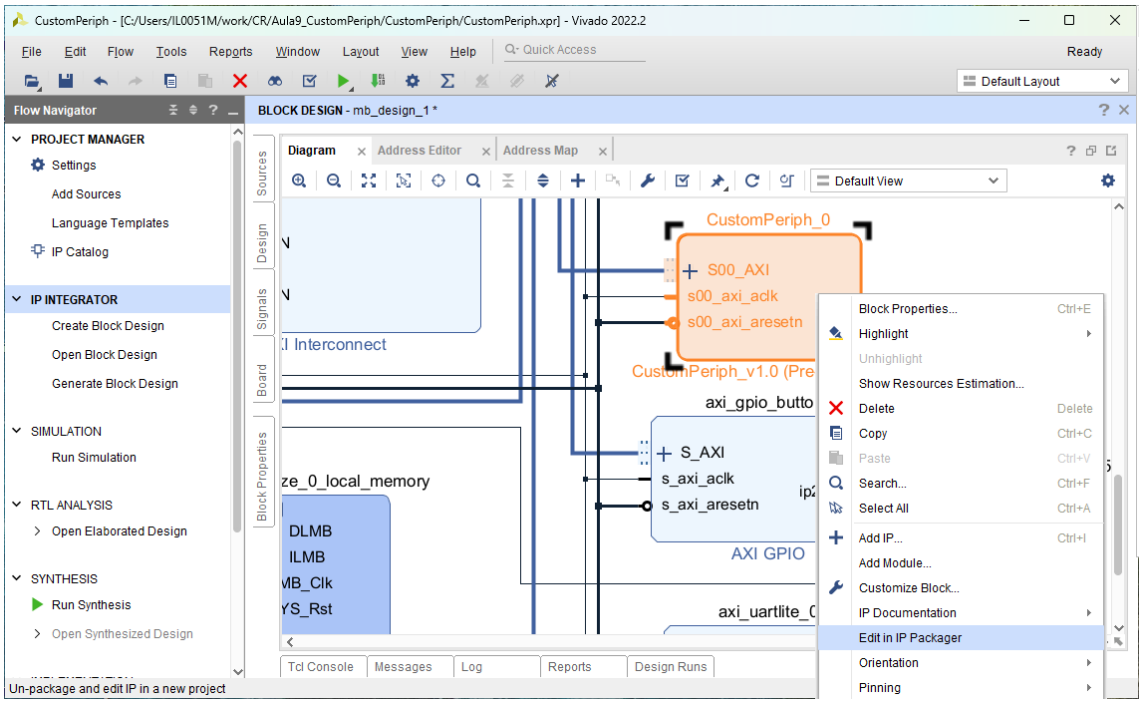
4. Click **Next**.



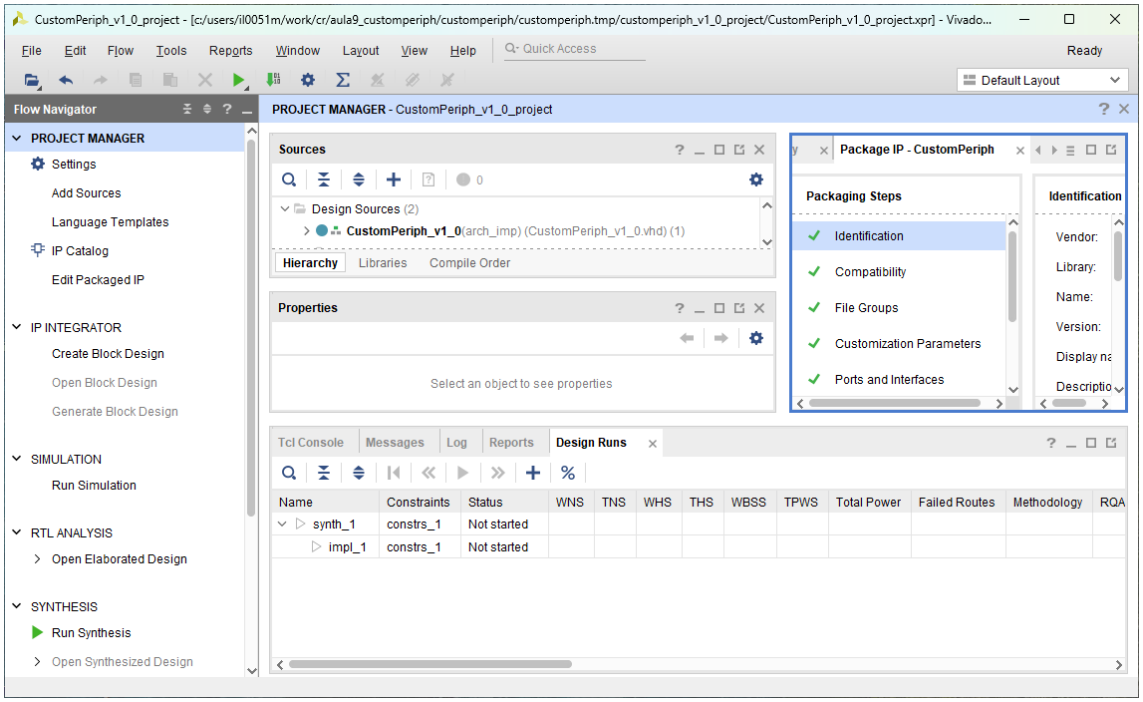
5. If available, click in **Run Connection Automation**. Click in **Regenerate Layout** (optional)



6. Right-click the new module. Click on **Edit in IP Packager**.

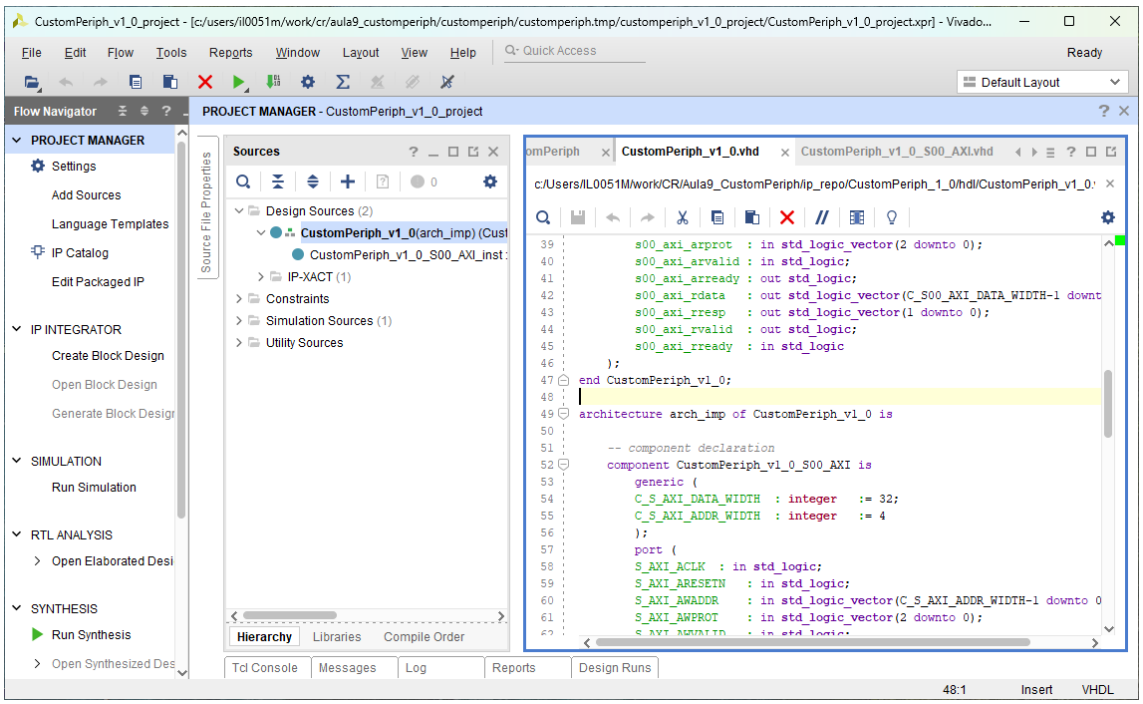


7. A new **Vivado** instance opens up.

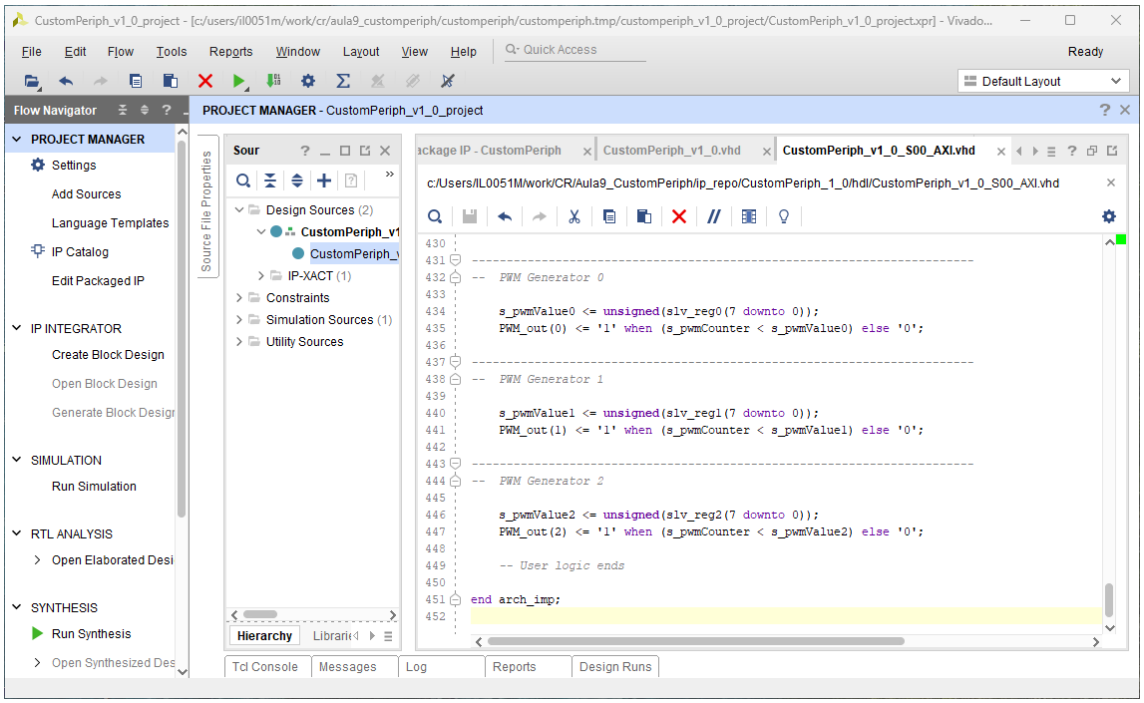


8. Identify the two source files of the project.

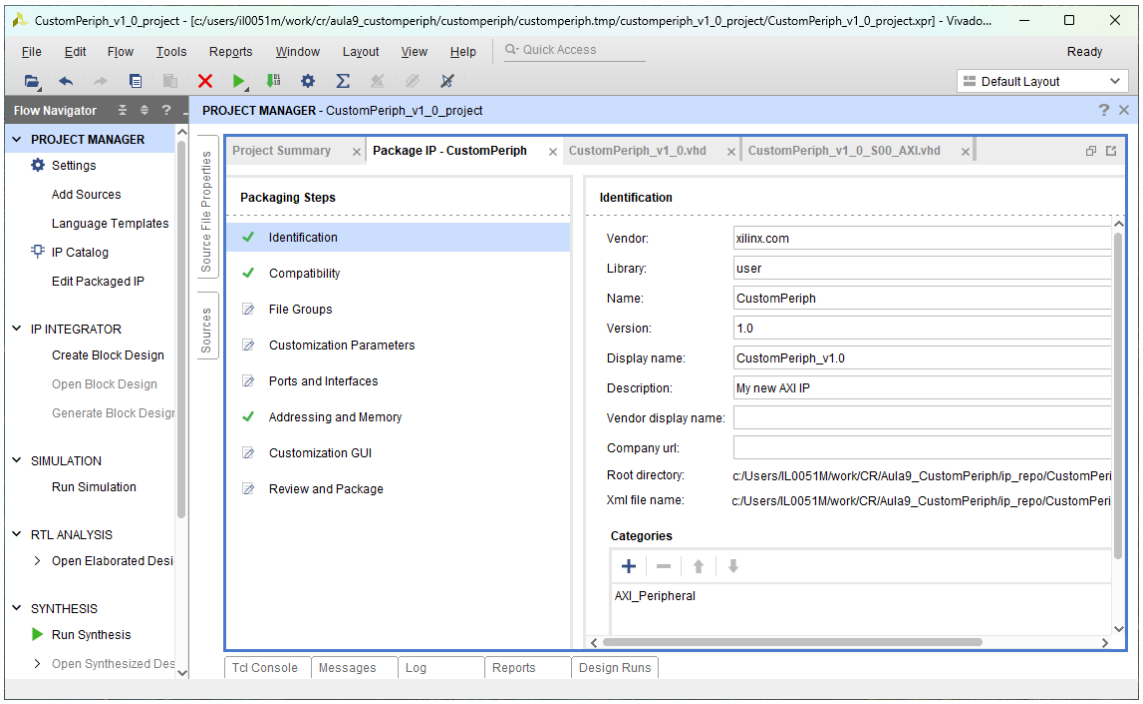
- **CustomPeriph_v1_0.vhd**
- **CustomPeriph_v1_0_S00_AXI.vhd**



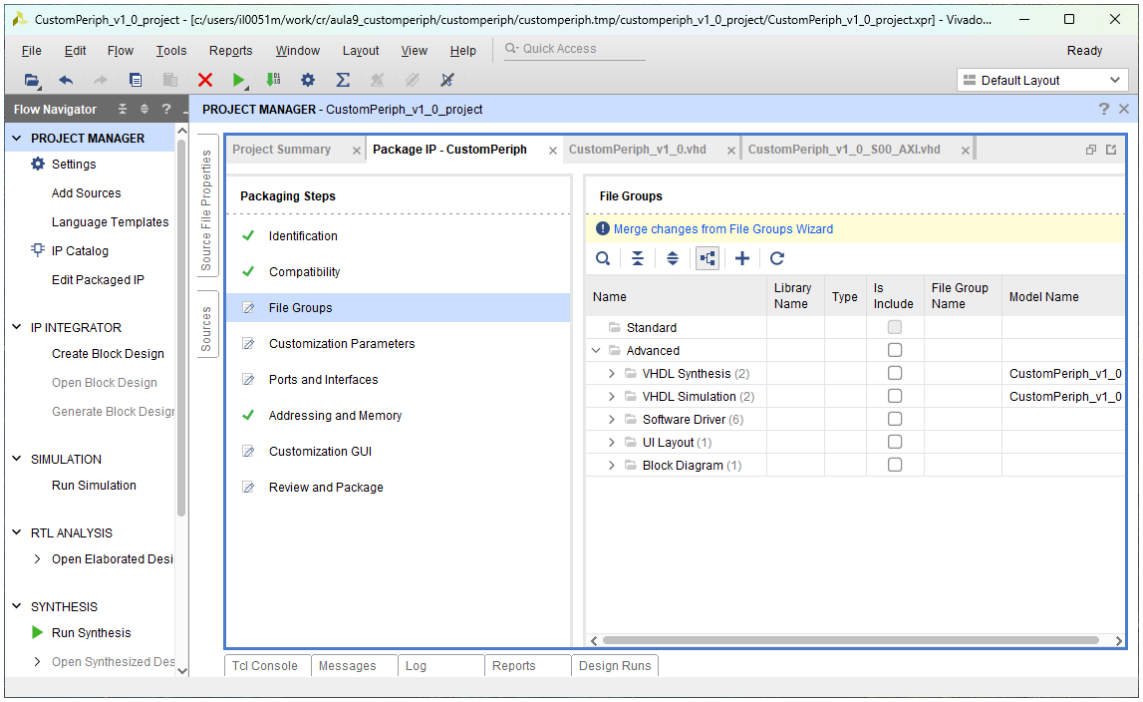
9. In the Moodle you will find the file **CustomPeriph (1).rar**, that has two source code files: **CustomPeriph_v1_0.vhd** and **CustomPeriph_v1_0_S00_AXI.vhd**. Replace the code.



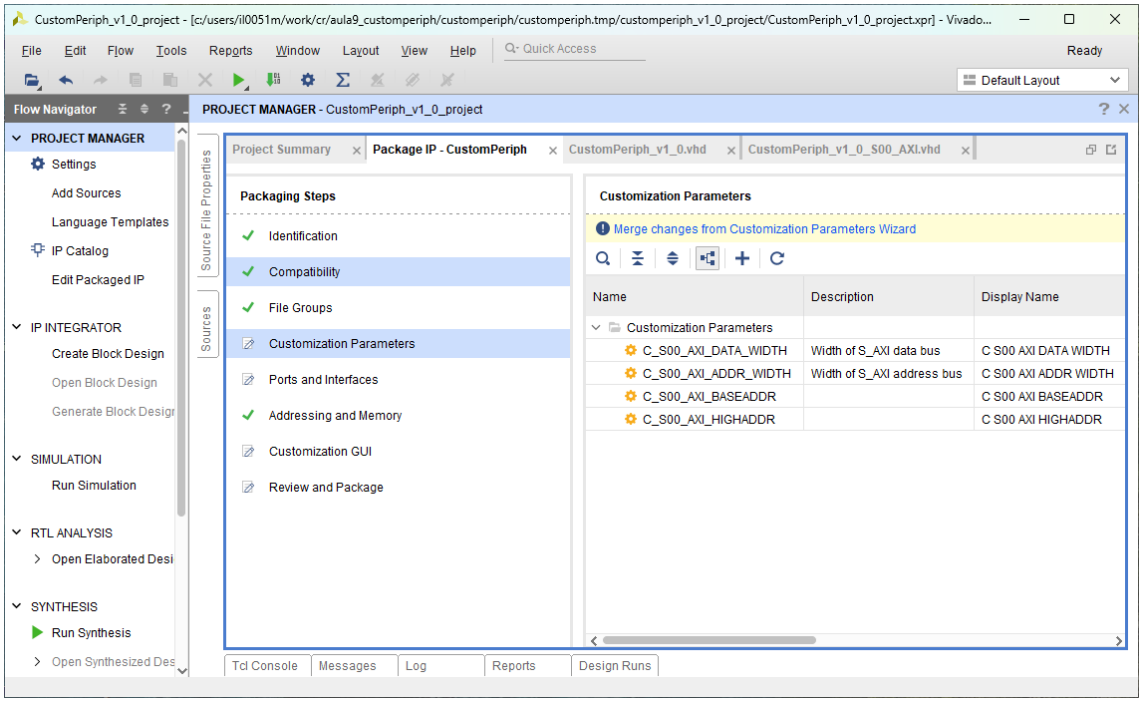
10. Select the **Package IP – CustomPeriph** tab.



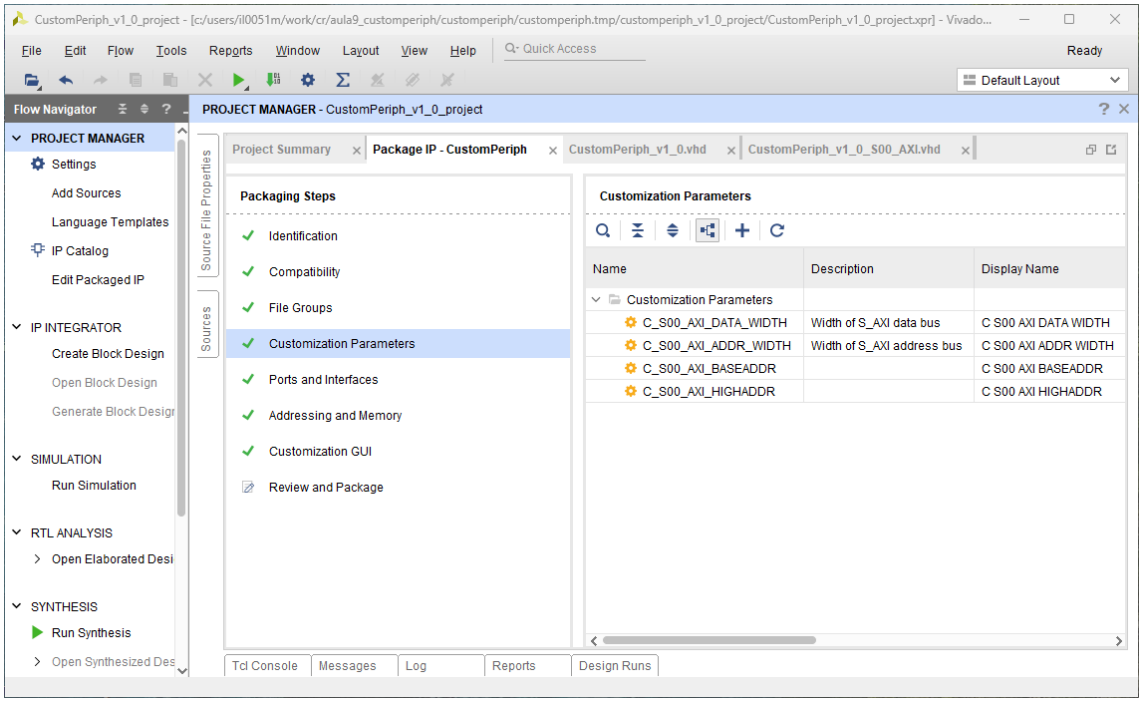
11. Click on **Merge changes from File Groups Wizard**.

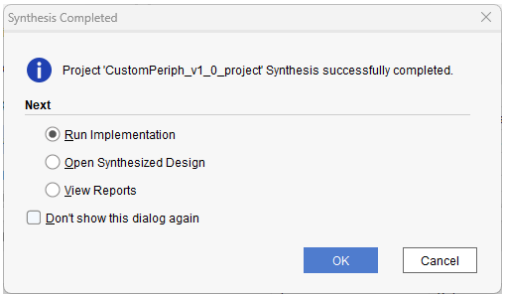


12. Click on **Merge changes from Customization Parameters Wizard**.

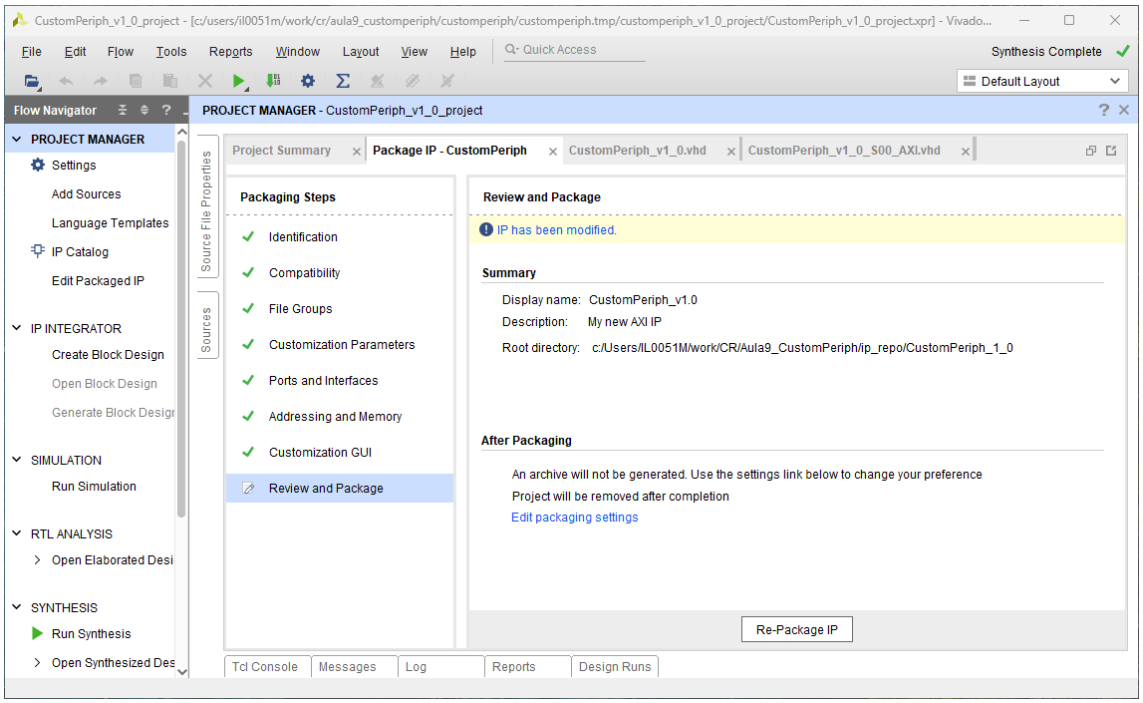


13. Click on **Synthesis**. Once over, close the pop-up window: click **Cancel** or top right **X**.

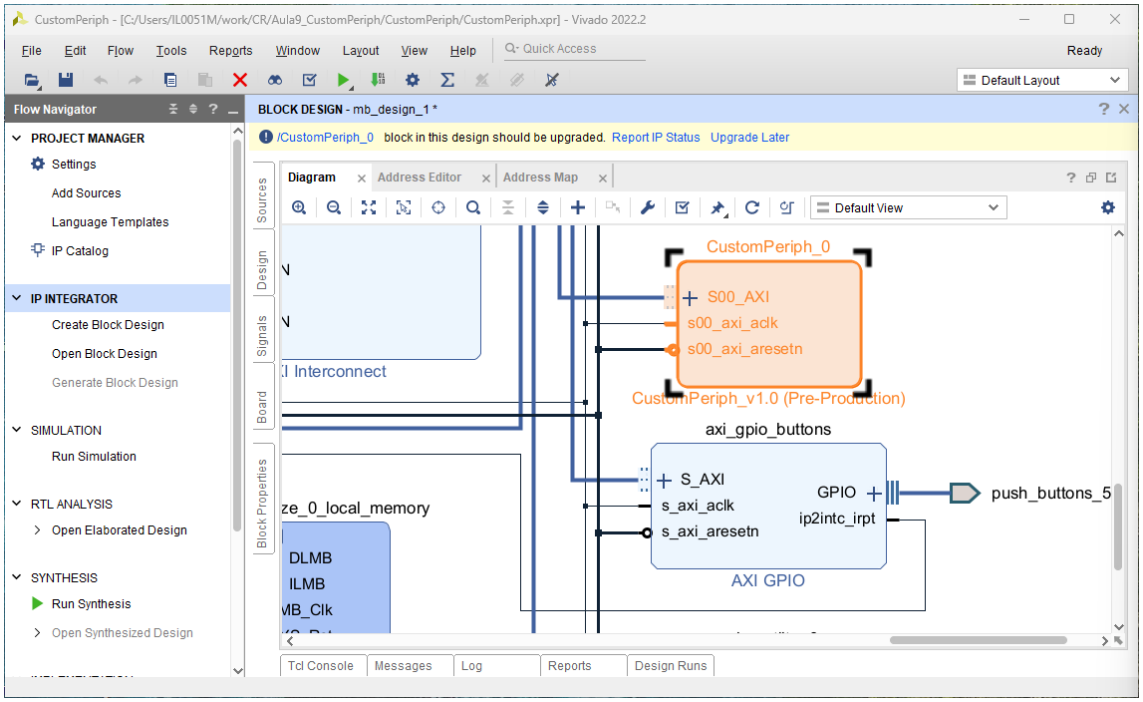




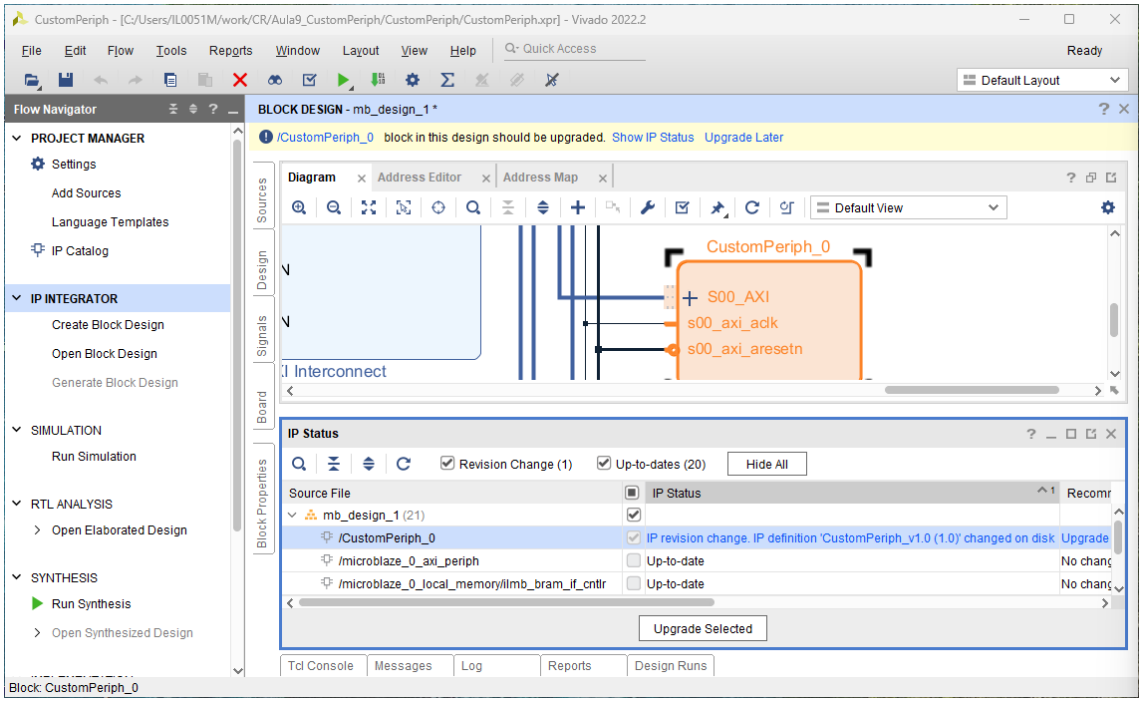
14. Click on **Re-Package IP**. Click **Yes** in the pop-up window.



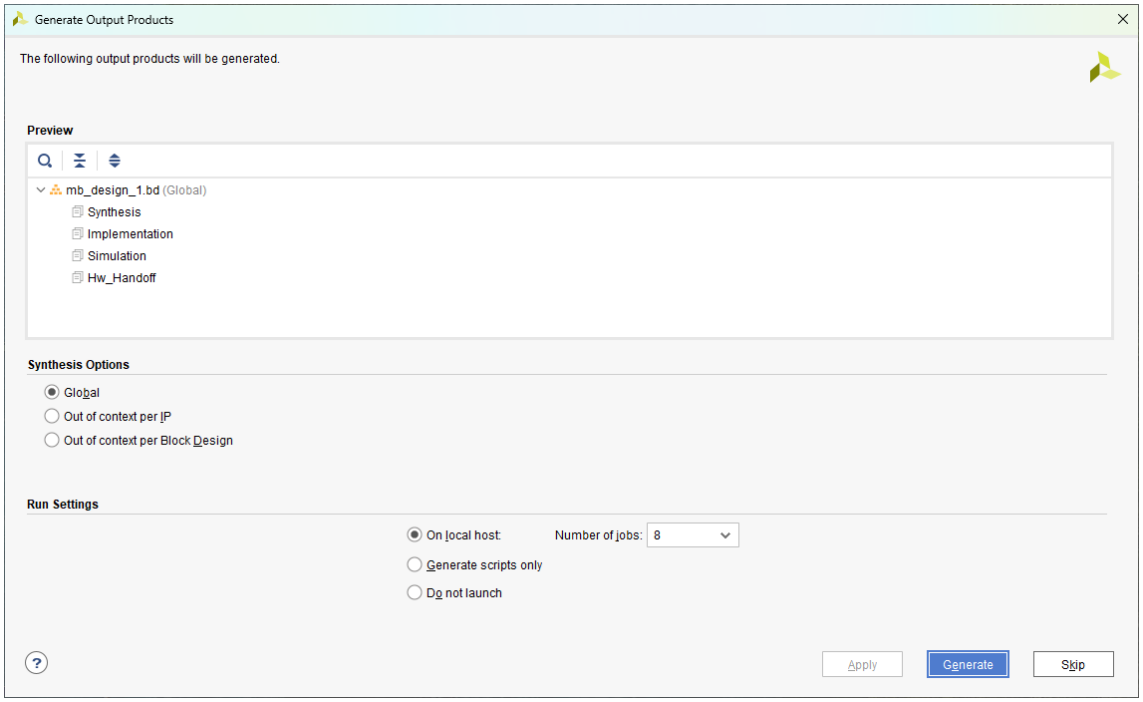
15. Back to the original **Vivado** window, click on **Report IP Status.**



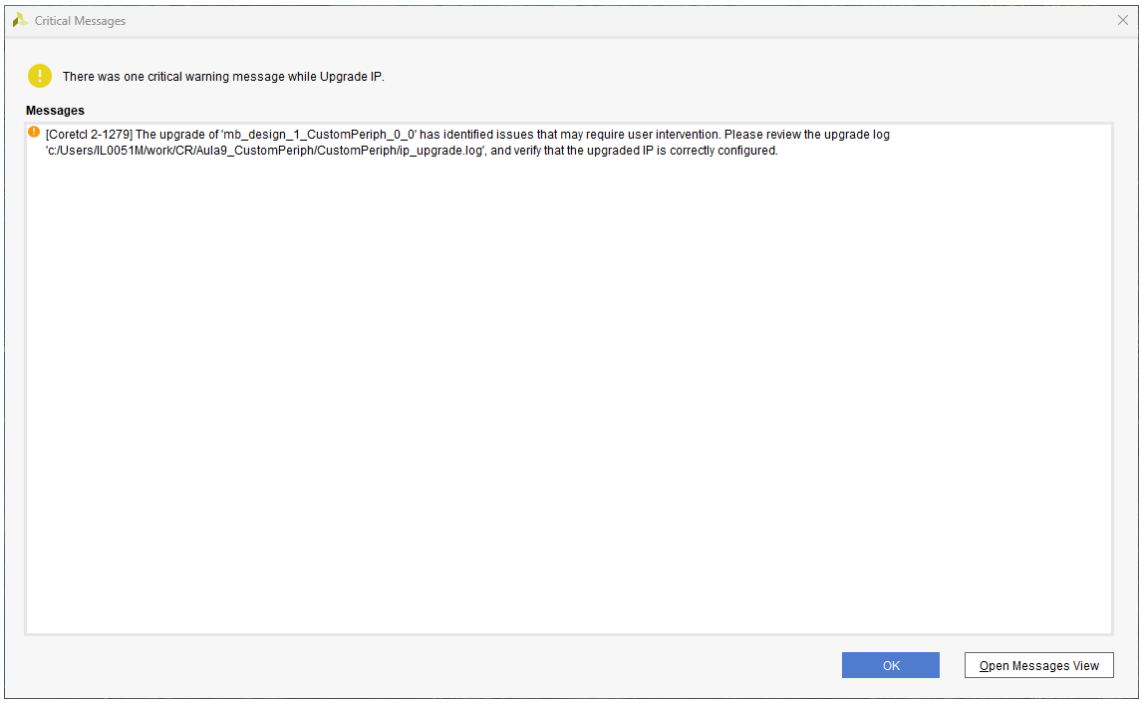
16. Click on **Upgrade Selected.**



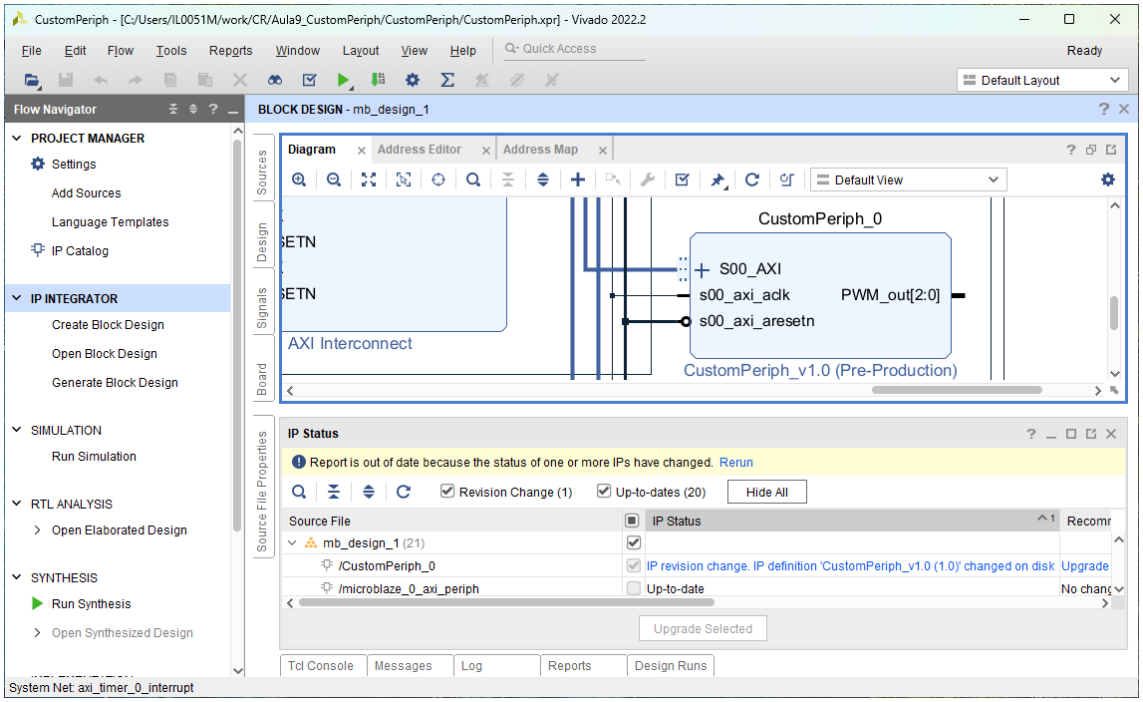
17. Close the pop-window (**X** on top right corner) concerning generation of Output Products.



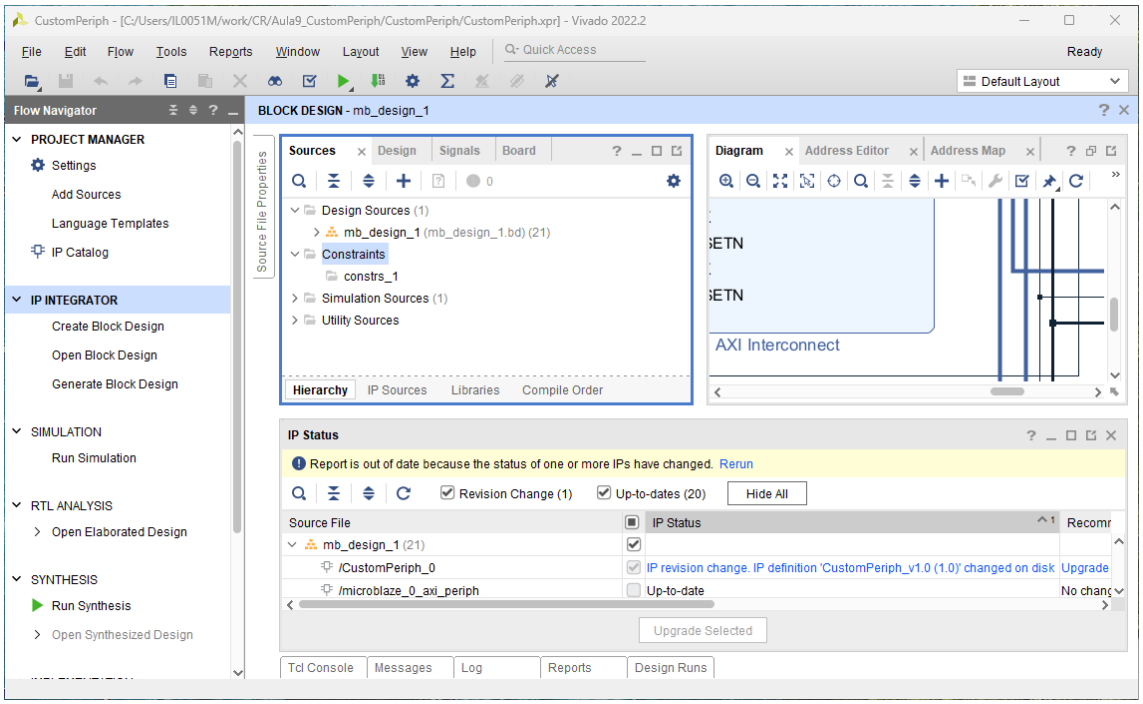
18. A warning message will show up. We will address it in the next steps. Click **OK**.



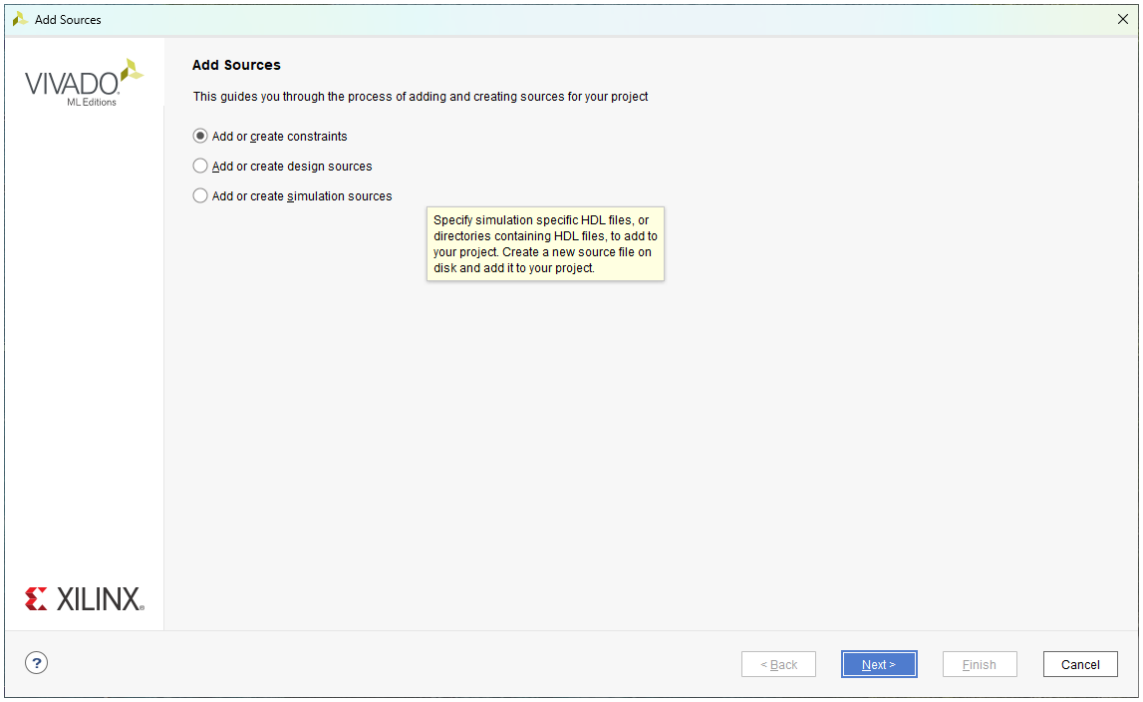
19. The reason is related to the fact that the **CustomPeriph** block does not have its **PWM_out** output connected anywhere.



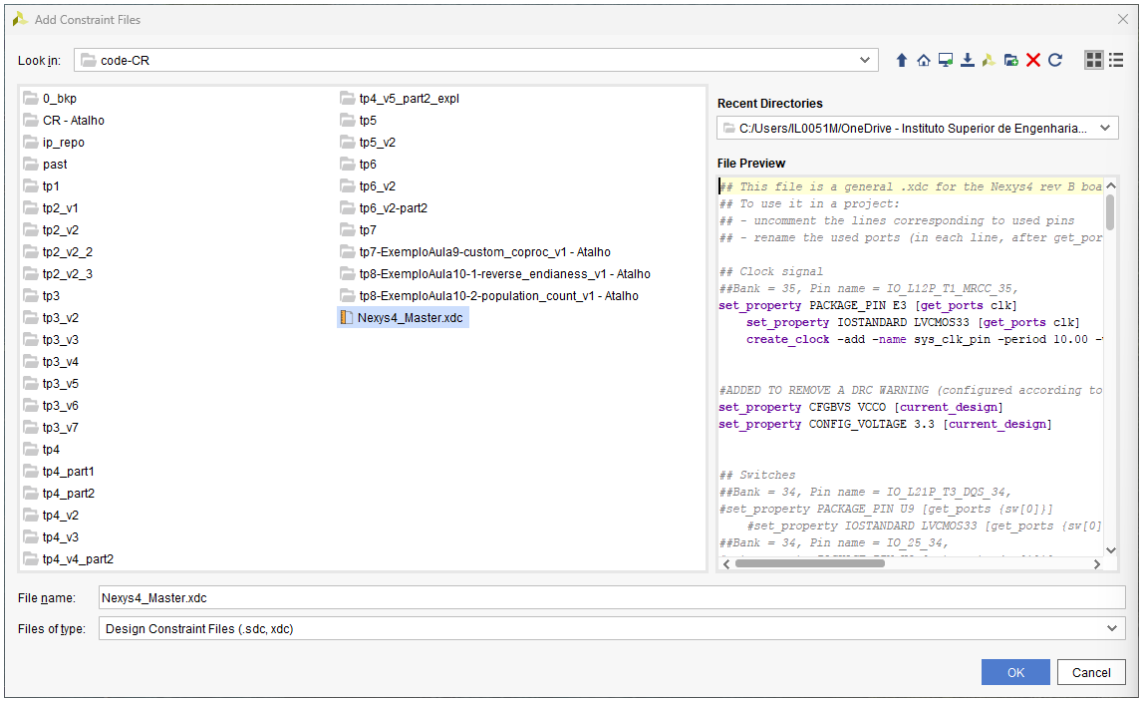
20. We will add an XDC file to address this issue. Open the **Sources** tab and click on **Add Sources** (‘**+**’ button).



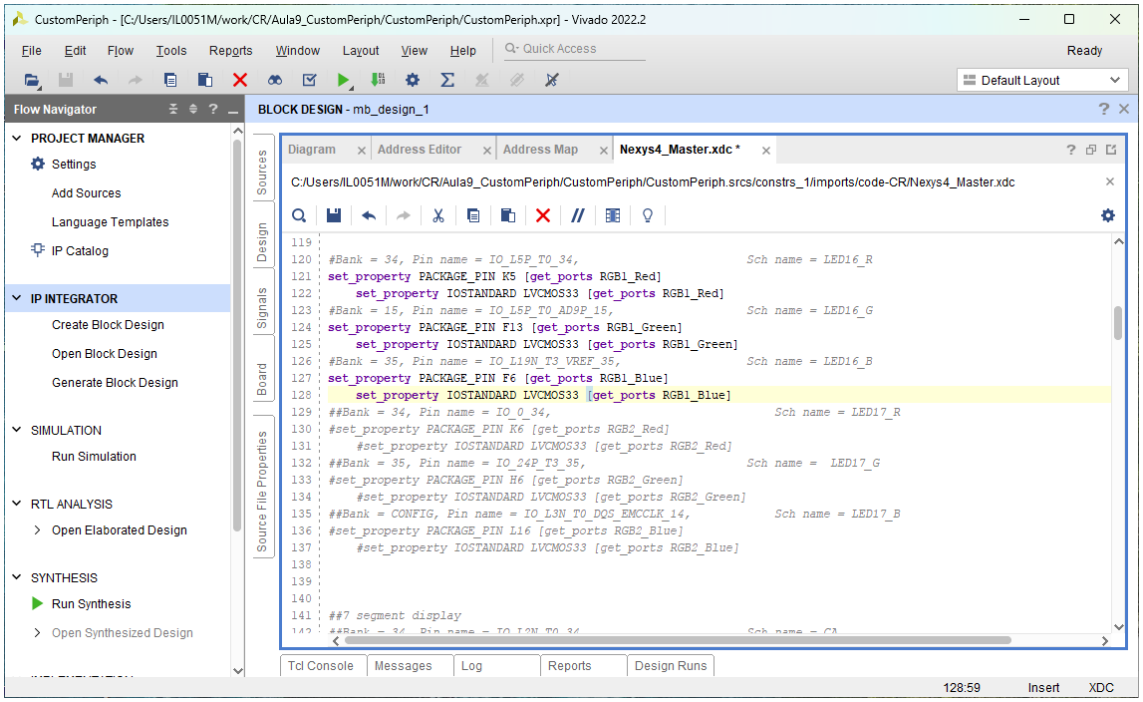
21. Click **Next**.



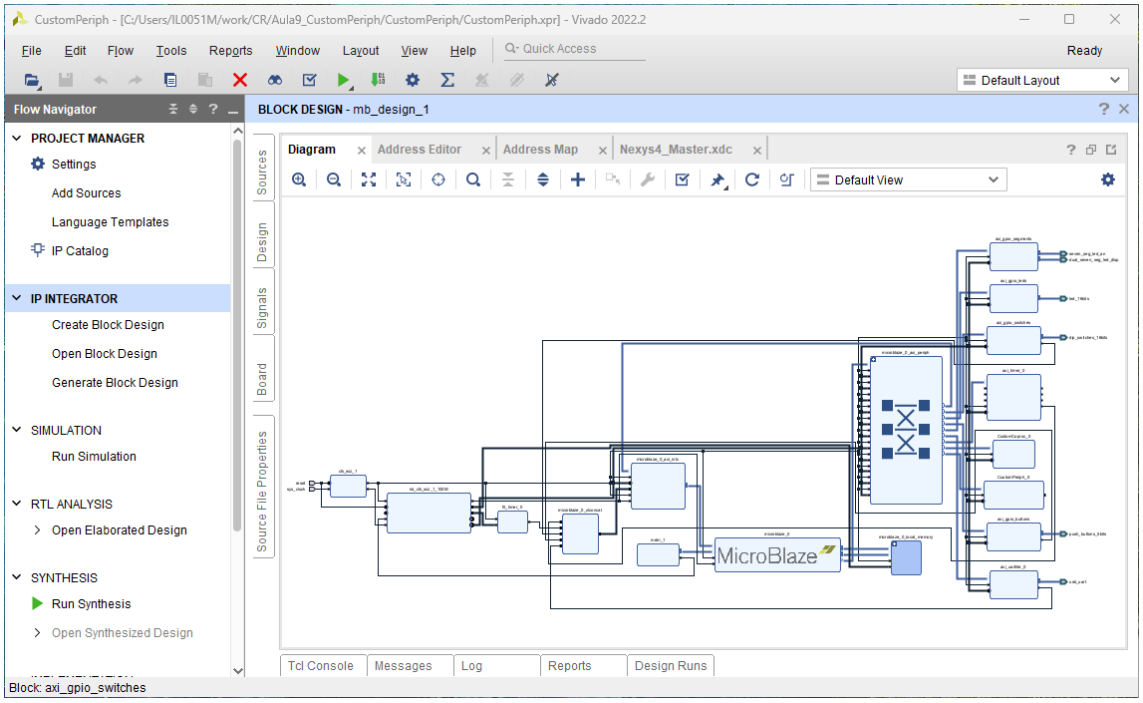
22. Add the XDC file that you used in the initial lab assignments. Click **OK**.



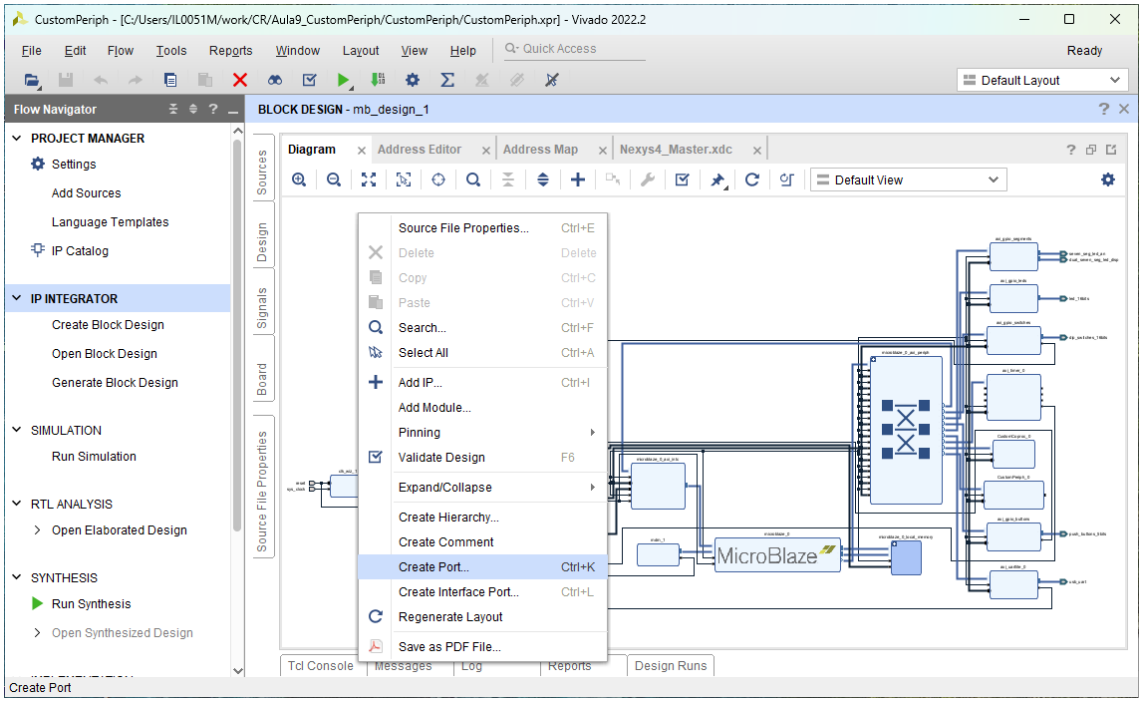
23. Uncomment the ports concerning the RGB LEDs.



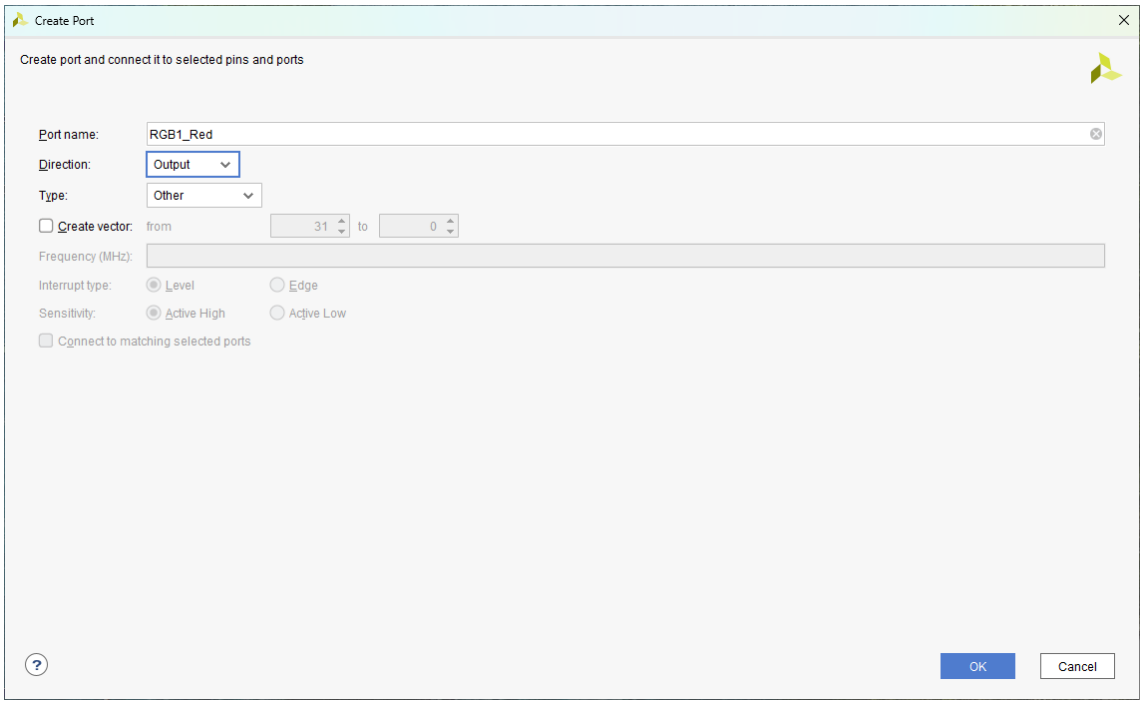
24. Return to the diagram view.



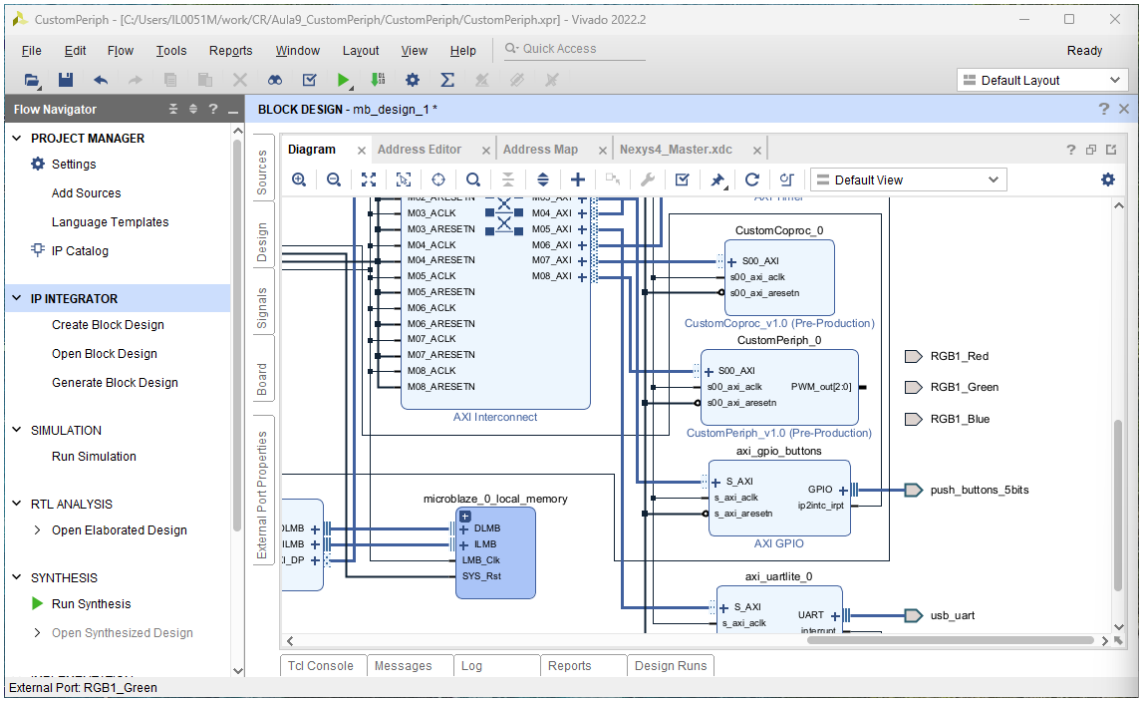
25. Right-click on the white open area of the diagram. Select **Create Port…** A pop-up window will show up.



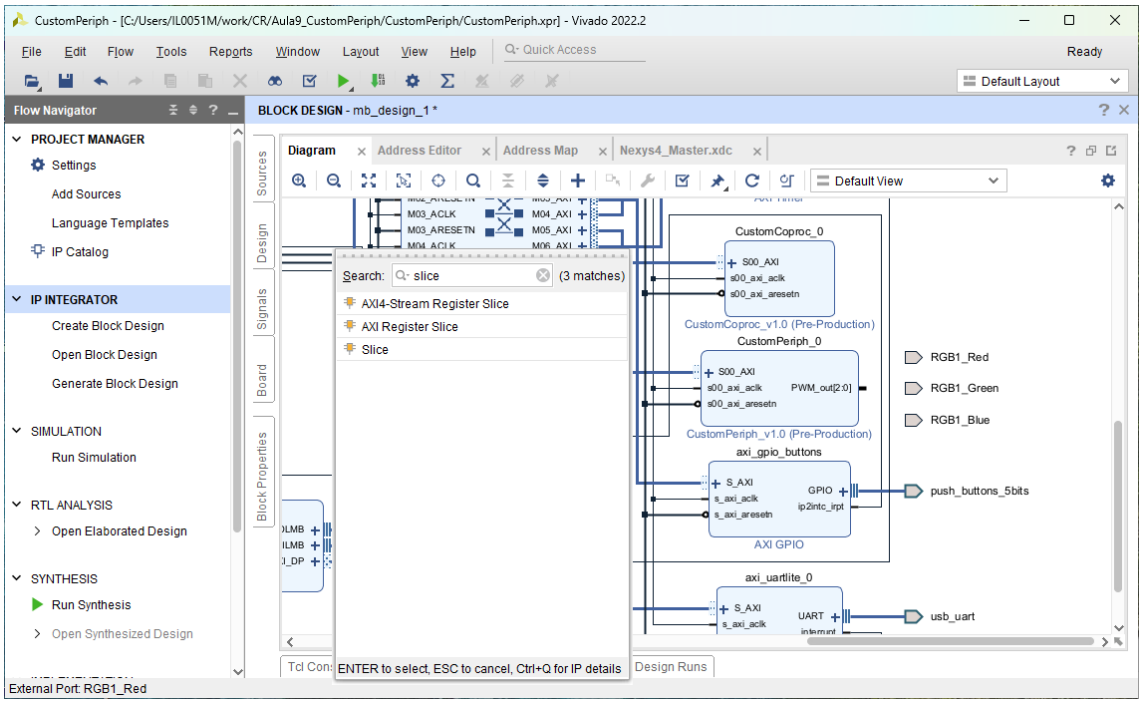
26. Name it **RGB1_Red** and assign it as **Output**. Name should match that in the XDC file. Do the same for the two remaining pins: **RGB1_Green and RGB1_Blue**.



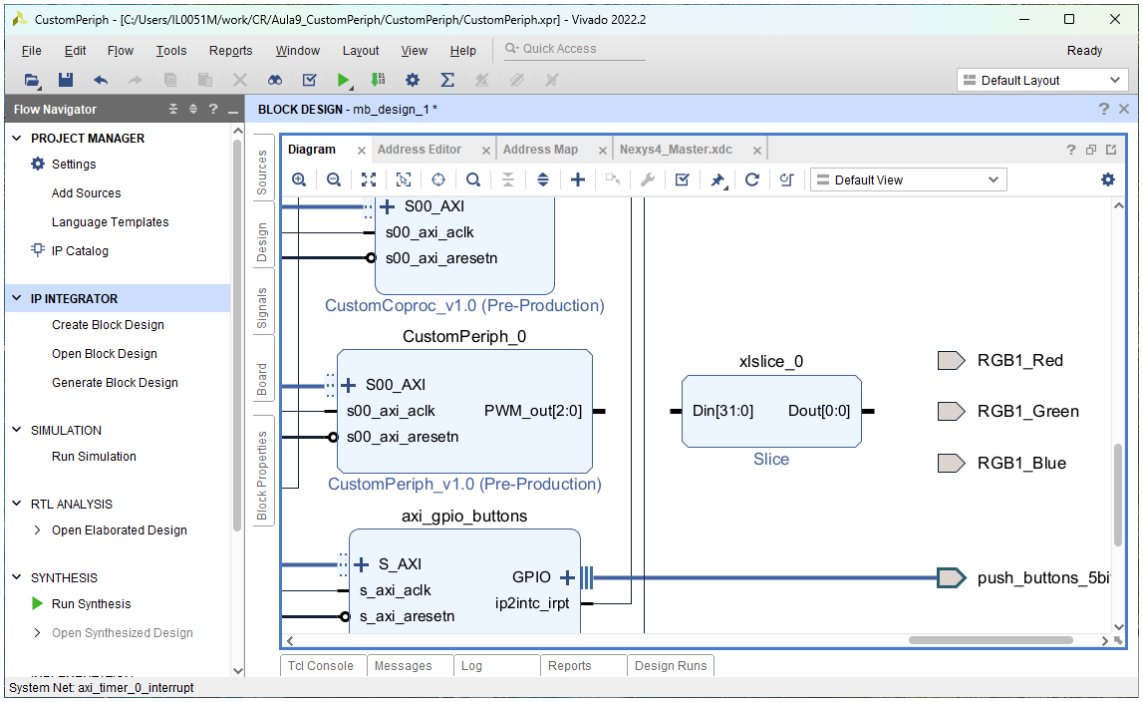
27. Move the pins to near the **CustomPeriph** block.



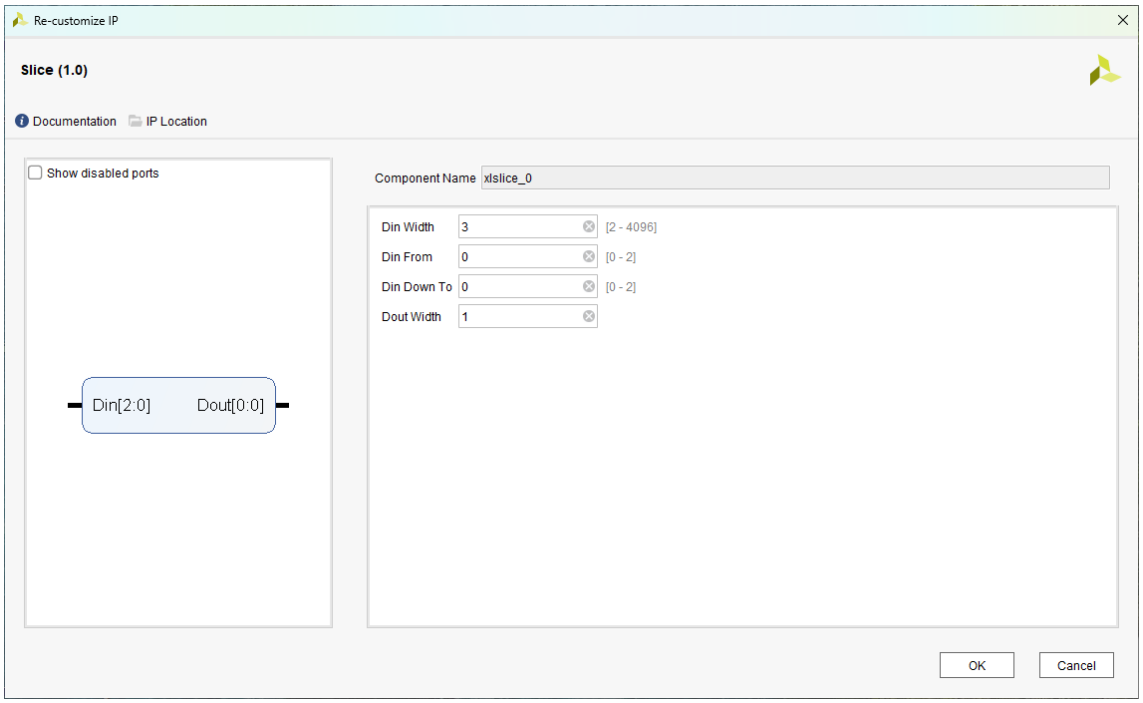
28. Click on the **Add IP** button (‘**+**’ sign button). Select the **Slice** block. This block takes a bus (i.e., an array of signals) and isolates individual signals.



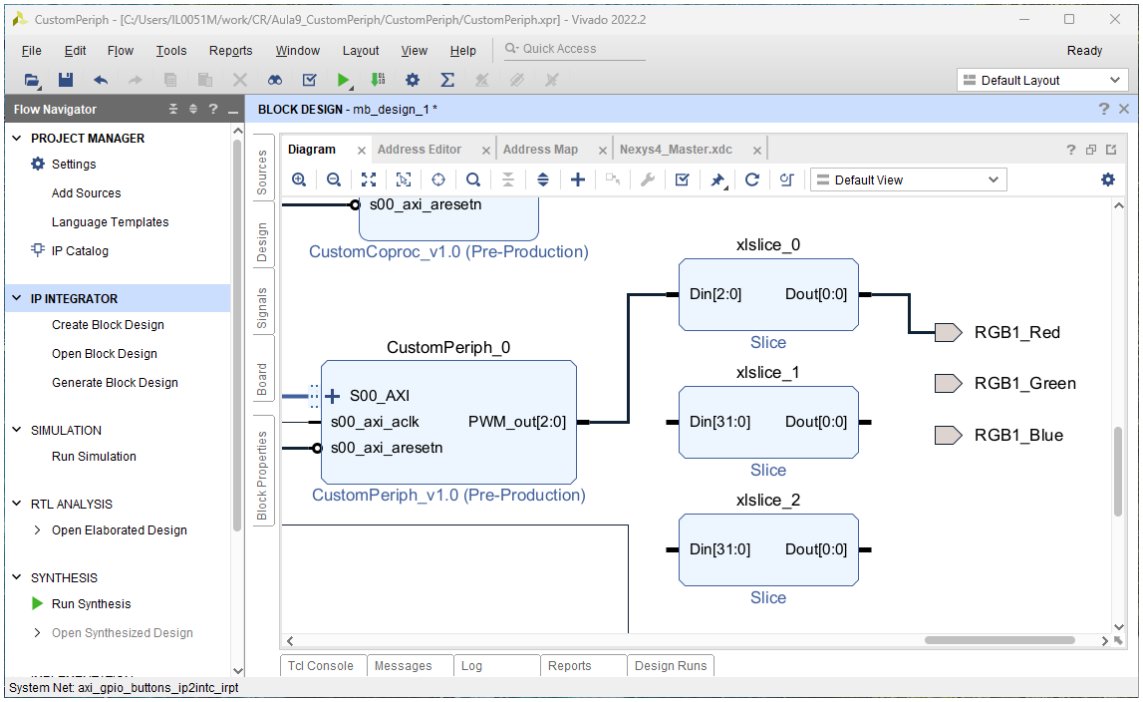
29. Add the **Slice** block between the **CustomPeriph** outputs and the **RGB** pins. Click on the Slice block to parameterize it.



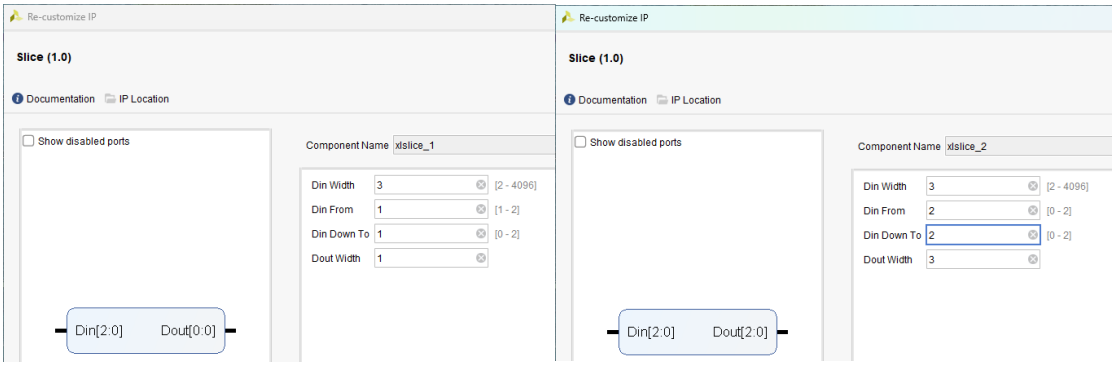
30. Field **Din Width** indicates the width of the output; set it to **3** bits.
    Fields **Din From** and **Din Down To** identify, respectively, the first and last index of the signals you wish to isolate. To isolate the LSB of the bus output by **CustomPeriph**, we set both fields to **0**.
    Field **Dout Width** indicates the width of the output; set it to **1**.



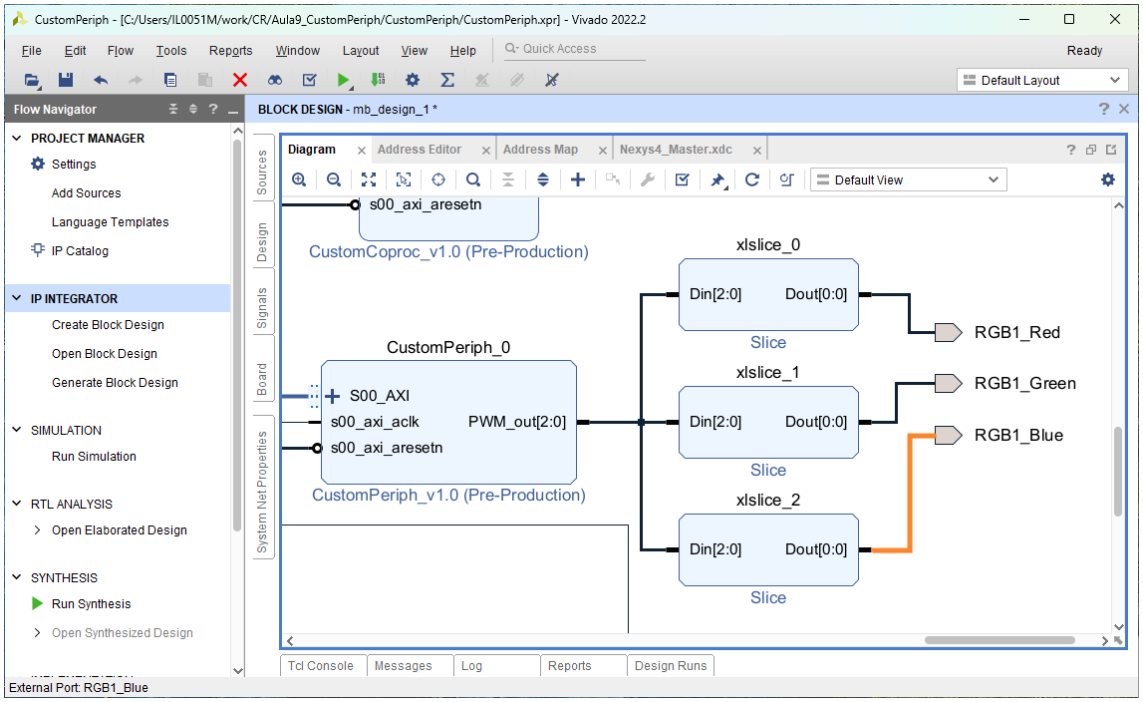
31. Add two more such blocks.



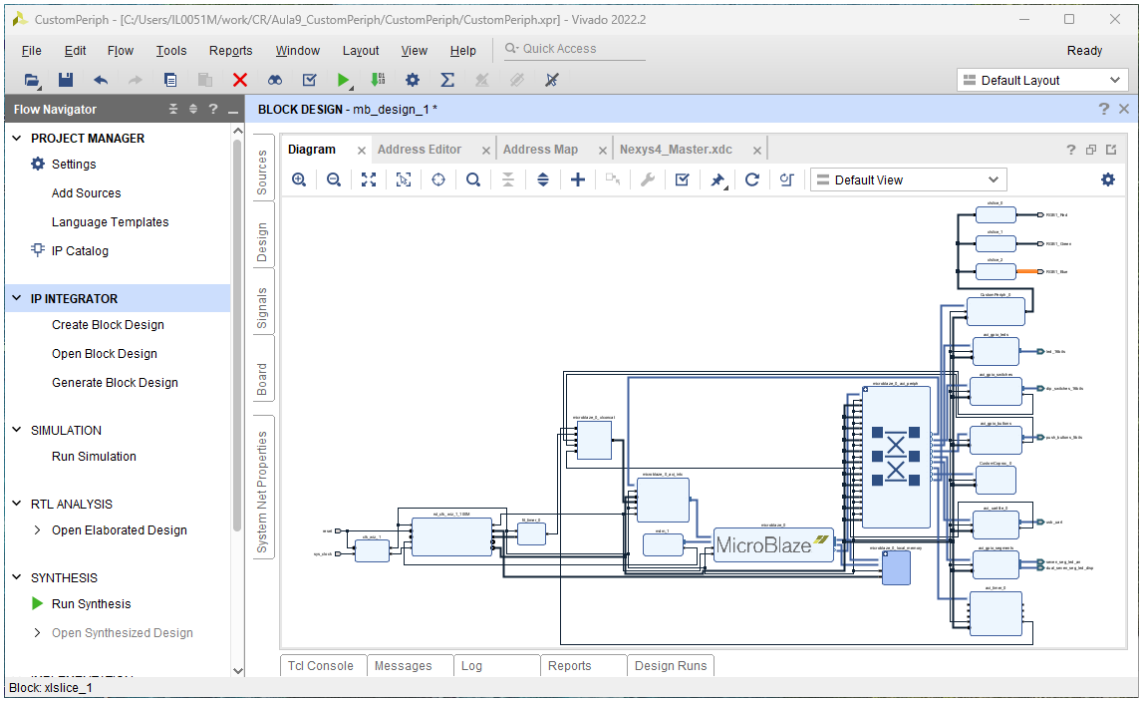
32. Parameterize them accordingly to isolate bit **1** and bit **2**.



33. Establish all connections.

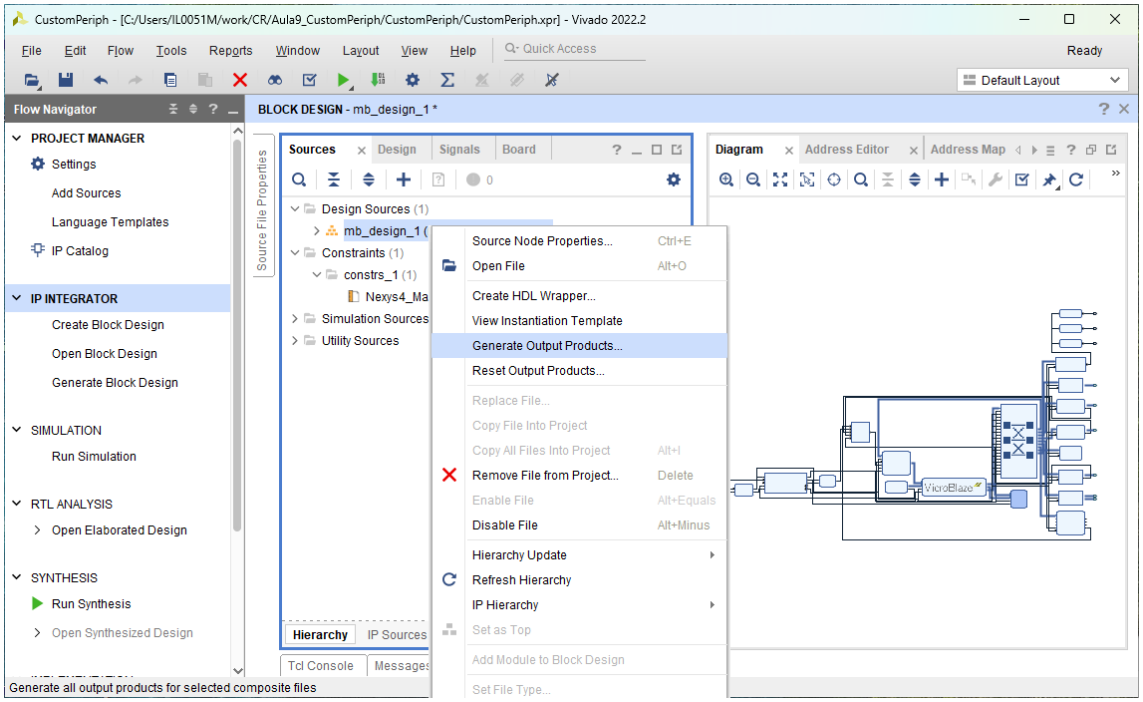


34. Click in **Regenerate Layout**.

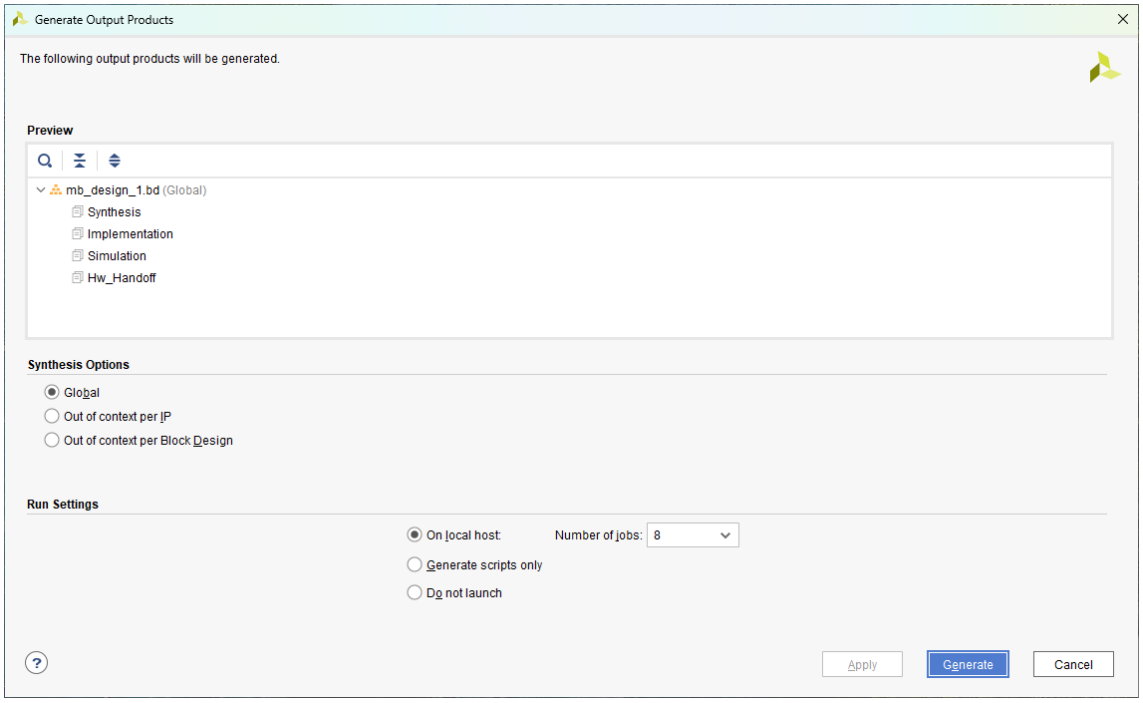


35. Confirm the status of the **CustomPeriph** module (step 16). Click **Re-run** if not up-to-date.

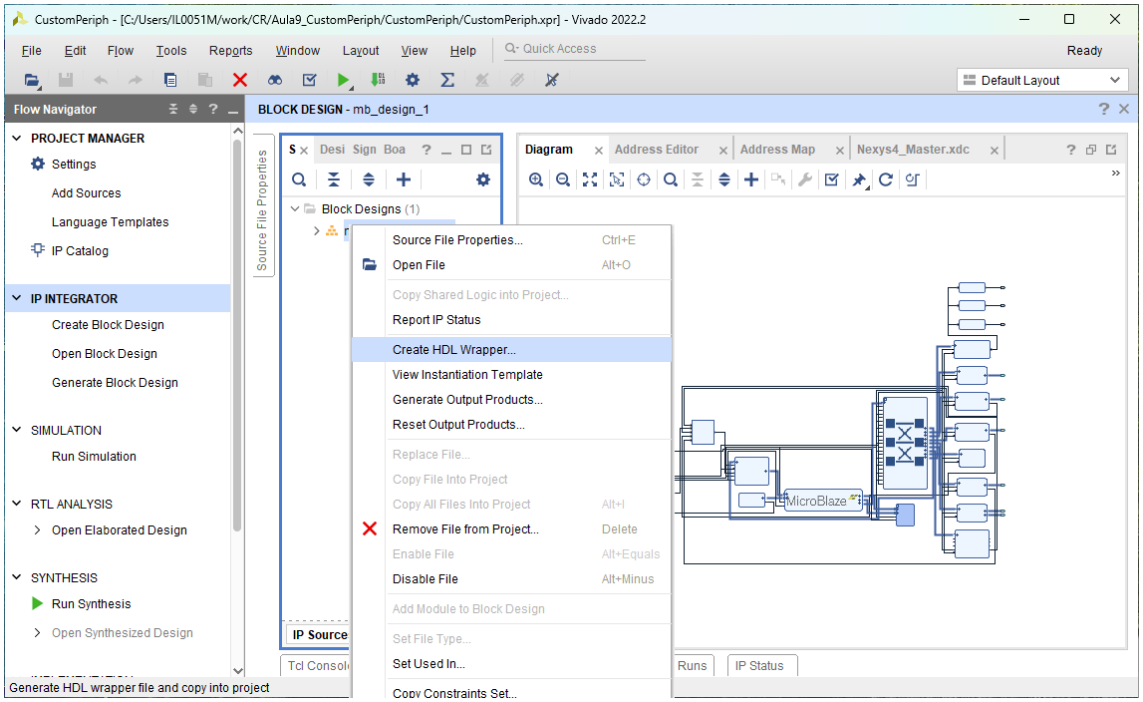
36. Right-click the wrapper file. Click in **Generate Output Products**.



37. Click on **Generate**.



38. Click in **Create HDL Wrapper**.



39. Click on **Generate Bitstream**
40. Click on **File** > **Export** > **Export Hardware**.

Congratulations!

Sources: AMD Xilinx documentation.