Reconfigurable Computing

COURSE PRESENTATION

2024/2025 ACADEMIC YEAR

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Reconfigurable Computing

Scientific area
- Architecture of computing systems
- Relevant course units
  - Introduction to Digital Systems
  - Digital Systems Laboratory
  - Computer Architecture I
  - Computer Architecture II
  - Advanced Computer Architecture
  - Operating Systems

Contact hours
- 3h (lecture + lab)

ECTS credits
- 6

The number of ECTS credits assigned to a course **does not indicate how many hours of classes you will have**. Instead, it **indicates the expected number of hours to study**.

1 ECTS = 25-30 hours of study. 6 ECTS = 150-180 hours of study.
The semester has ~ 15 weeks => you must study at least **10 hours per week**.

These hours include lectures, labs, book reading, exercise solving, exam study, etc.

Objectives

It is intended that students acquire skills in the design of **Systems-on-Chip (SoCs)** design, development of complex digital systems and hardware-software co-design.

Design of specialized or **reconfigurable** computational platforms for embedded systems based on **FPGAs** and programmable SoCs (PSoCs)

- specification, construction and specialization of the hardware platform and design and execution of software.

Expected outcomes

Upon completing this course unit, students will acquire the following skills:

- Modeling based on advanced use of hardware description languages and system programming languages.
- Development and prototyping of integrated systems based on high capacity programmable logic devices (FPGAs and PSoCs).
- Use of computer-aided design tools for modeling, simulation, synthesis, implementation, debugging, test, and optimization.

Topics

Construction of **heterogeneous multiprocessor platforms for SoCs**, containing processors, memory, communication infrastructures, standard peripherals and specialized modules, based on high-level tools and languages, hardware description languages and high capacity programmable logic devices (FPGAs and PSoCs).

Use of **computer-aided design (CAD) tools** for development and reuse of intellectual property (IP) cores, simulation, synthesis, implementation, debugging and testing.

Development, compilation, execution, debugging and profiling of embedded software, running in standalone mode or on the top of a kernel/operating system.

Analysis of the metrics resulting from the implementation of a system and the introduction of restrictions and optimizations, both at hardware and software levels, in order to improve the final quality of the design and/or the fulfillment of the specifications.

Evaluation

Final classification is obtained by two mutually exclusive alternatives:

- **Discrete evaluation** (default):
  - Theoretical evaluation T (test 1 <April 1> 25%, test 2 <May 27> 25%) – 50%
  - Practical evaluation P (group final project 30%, practical assignments 20%) – 50%
- **Final exam**:
  - Final exam (50%) <normal examination period>
  - Practical evaluation P (individual final project) – 50%

The evaluation method is **discrete** by default, but might be altered to **final** during the first two weeks of the semester (< 01.03.2025).

There is no minimum grade for individual components.

For approval, **the total weighted average must be ≥ 9.5**.

Practical assessment

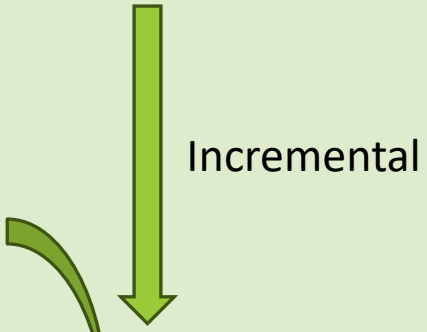
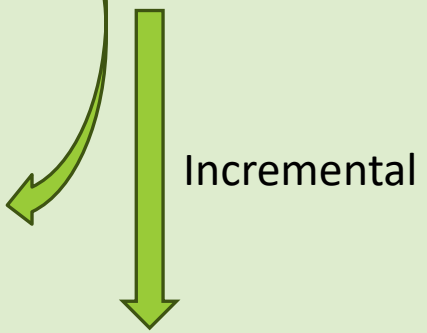
Group final project 30%

- One project for a group of two students
- Project specifications to be discussed in late April / early May
- Project presentation and defense will be organized during the last week of classes (or extra class)
- Objective: implementation of a system with specialized hardware that allows to accelerate/facilitate a certain operation / functionality

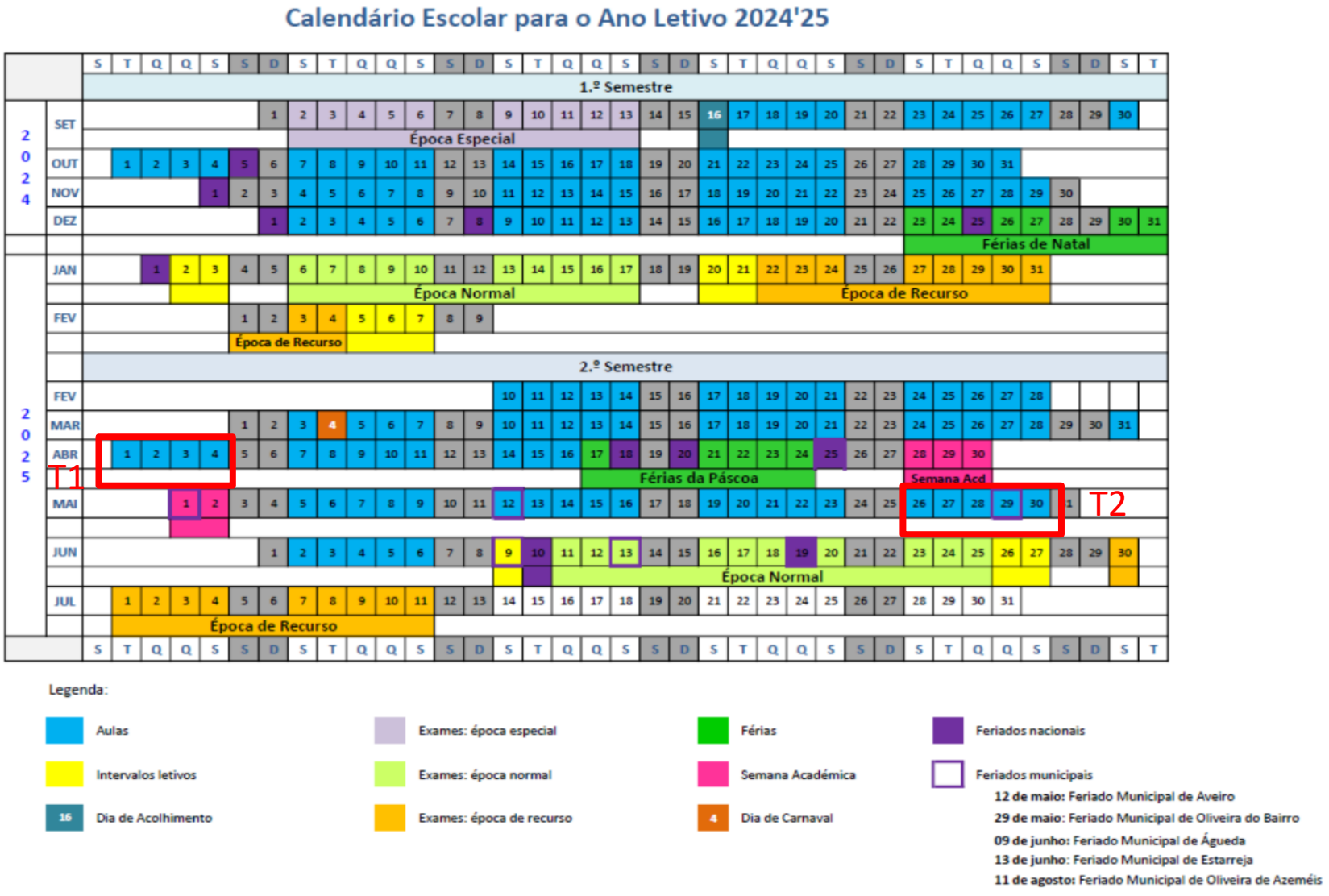
Practical assignments 20%

- One kit for every student
- The kits must be picked up at the university and returned back by the end of the semester
- The respective rules for loan and use of the development boards are explained at the course website
- **Some practical assignments have to be submitted** (3, 4 and 8)

Laboratory Classes

Topic	#		Notas
Digital circuit design (in VHDL)	Lab.1	Tutorial to programming Nexys 4. Typical workflow.	
	Lab.2	Digital circuit to control LEDs, Display	
	Lab.3	Dedicated module to control display	
	Lab.4	Contador minutos:segundos em display	
MicroBlaze – Programming in C and block	Lab.5	Processador embebido MicroBlaze	
	Lab.6	Controlo GPIOs pelo MicroBlaze	
	Lab.7	Configuração AXI-Slave	
	Lab.8	Co-processador hardware AXI-Stream	

Calendar


Calendário Escolar para o Ano Letivo 2024'25
1.º Semestre
Época Especial
Férias de Natal
Época Normal
Época de Recurso
Época de Recurso
2.º Semestre
Férias da Páscoa
Semana Acd
T1
T2
Época Normal
Época de Recurso
Legenda:
Aulas
Intervalos letivos
Dia de Acolhimento
Exames: época especial
Exames: época normal
Exames: época de recurso
Férias
Semana Académica
Dia de Carnaval
Feriados nacionais
Feriados municipais
12 de maio: Feriado Municipal de Aveiro
29 de maio: Feriado Municipal de Oliveira do Bairro
09 de junho: Feriado Municipal de Águeda
13 de junho: Feriado Municipal de Estarreja
11 de agosto: Feriado Municipal de Oliveira de Azeméis

Repeaters

Repeating students who have obtained a positive grade in the practical component of the course in 2024/2025 do not maintain their grade.

Working Students

Working students who have not been able to attend regular lab classes during the semester, will have their final exam(s) during the exam season.

The practical evaluation will only include the final project whose weight is 50% of the final grade.

The final project for these students must be individual.

It is possible to waive the status of worker-student by signing a declaration available on the course website.

Bibliography

P.P. Chu, *FPGA Prototyping by VHDL Examples: Xilinx MicroBlaze MCS SoC*, 2nd ed., John Wiley & Sons, 2017.

I. Skliarova, V. Sklyarov, *FPGA-Based Hardware Accelerators*, Springer, Switzerland, 2019.

V. Sklyarov, I. Skliarova, A. Barkalov, L. Titarenko, *Synthesis and Optimization of FPGA-Based Systems*, Springer, Switzerland, 2014.

A. Pedroni, *Circuit Design with VHDL*, MIT Press, 2020.

F. Wakerly, *Digital design: Principles and practices*, 5ª ed., Pearson, 2018.

B. C. Readler, *VHDL by Example - A Concise Introduction for FPGA Design*, Full ArcPress, 2014.

B. Mealy, F. Tappero, *Free Range VHDL*, www.freerangefactory.org, 2016.

L. Crockett, R. Elliot, M. Enderwitz, R. Stewart, *The Zynq Book: Embedded Processingwith the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC*, StrathclydeAcademic Media, 2014.

R. Jasinski, *Effective Coding with VHDL: Principles and Best Practice*, MIT Press, 2016.

Manuals

Course website: elearning.ua.pt

Support materials for classes

Lab guides

Course software

Assessment

Bibliography

Full reading of the teaching dossier is mandatory!

Final notes

Copying, in whole or in part, of any material delivered for evaluation is considered fraud.

The detection of this practice implies the attribution of the classification 0 (zero) to the respective evaluation element.

Let’s start!