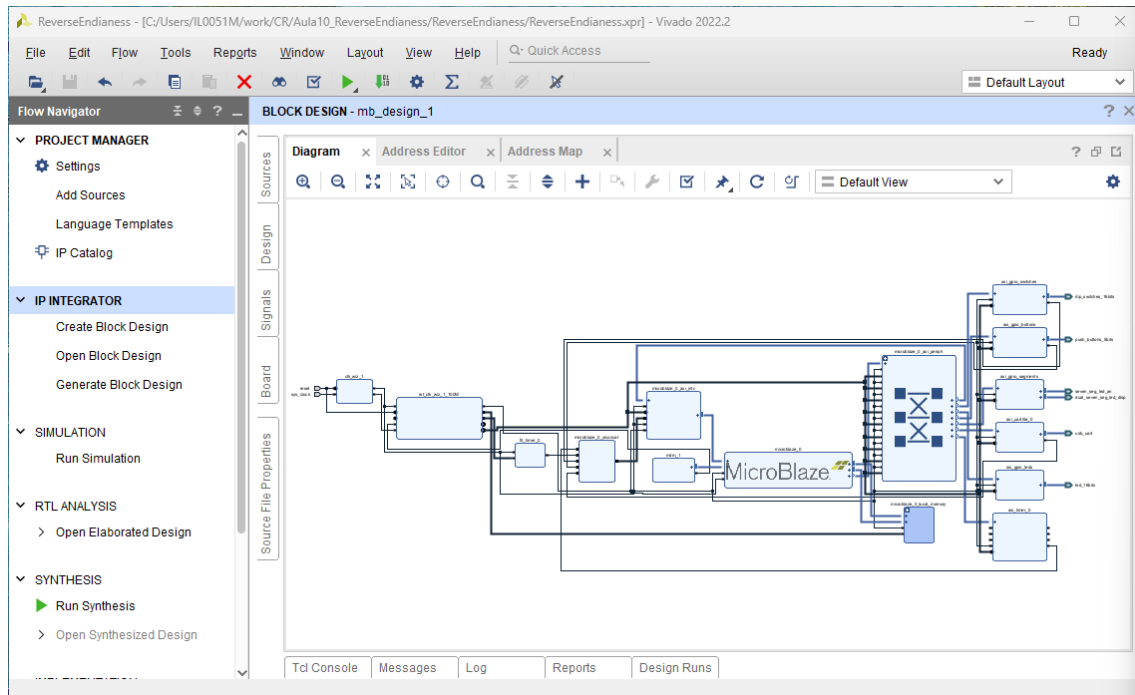


## Tutorial 6

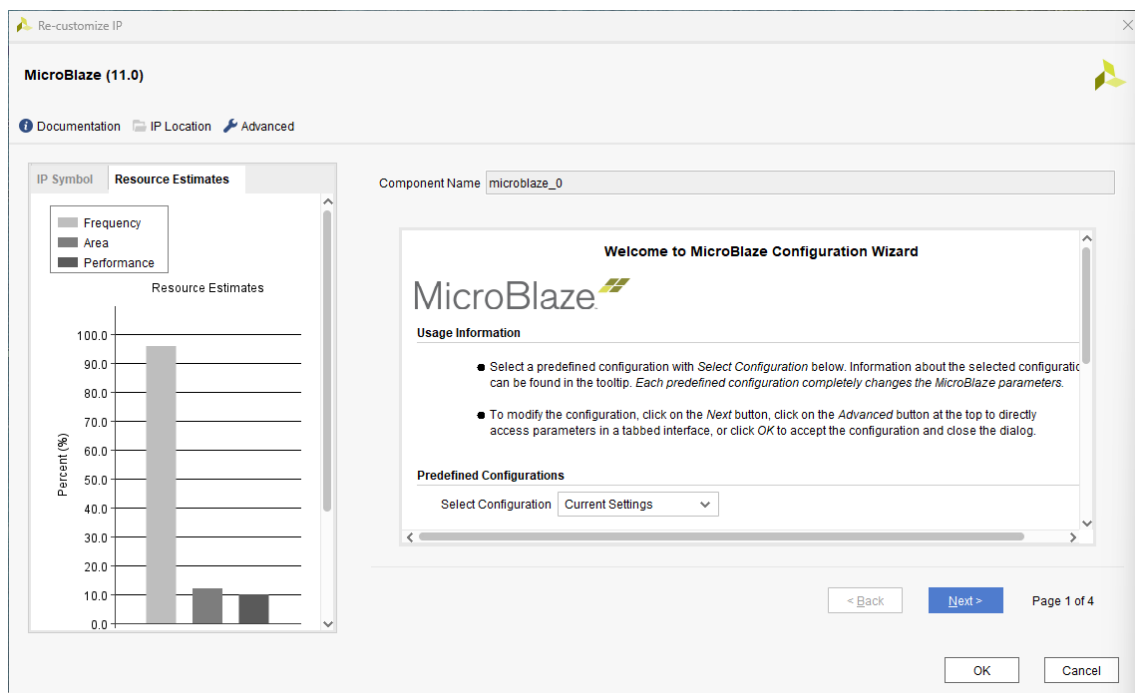
### Update MicroBlaze Platform with a Custom Coprocessor (Reverse Endianess) connected via AXI-Stream

Vivado version: 2022.2

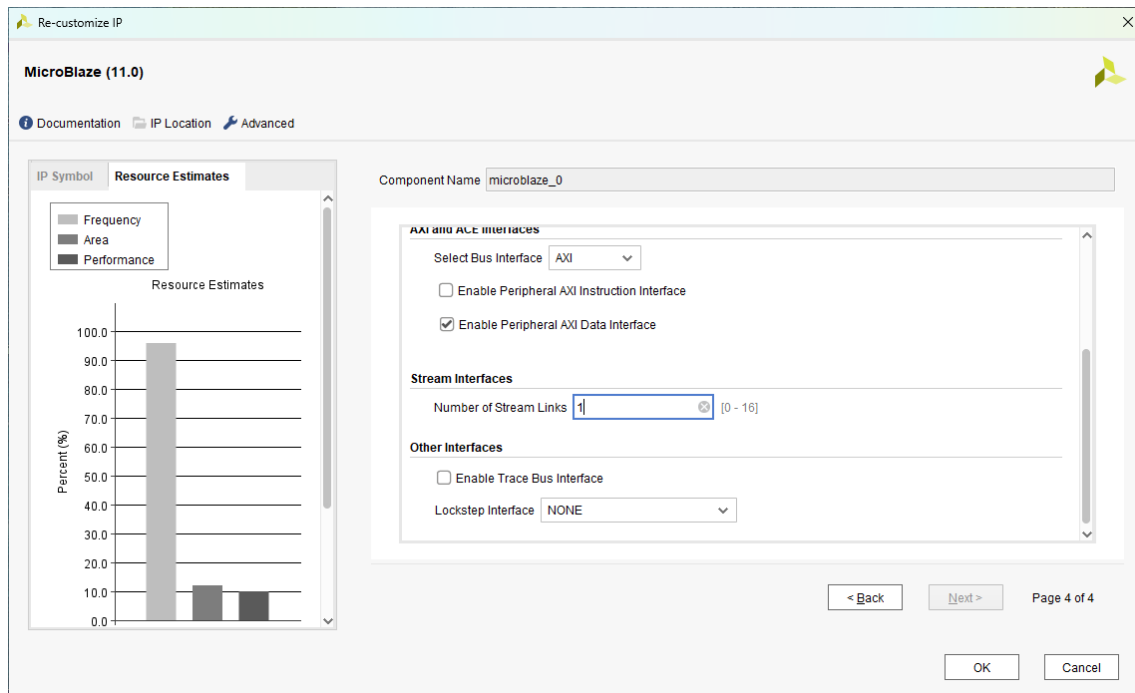
1. Double-click the **MicroBlaze** module.



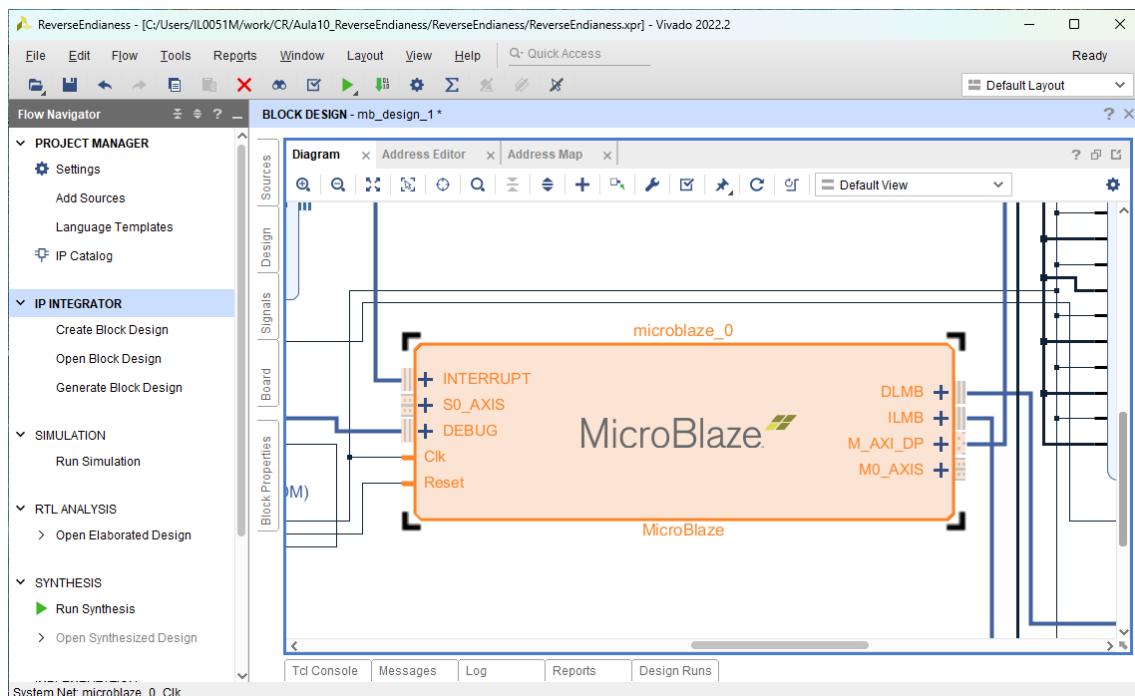
2. A configuration window pops-up. Click **Next** until page 4.



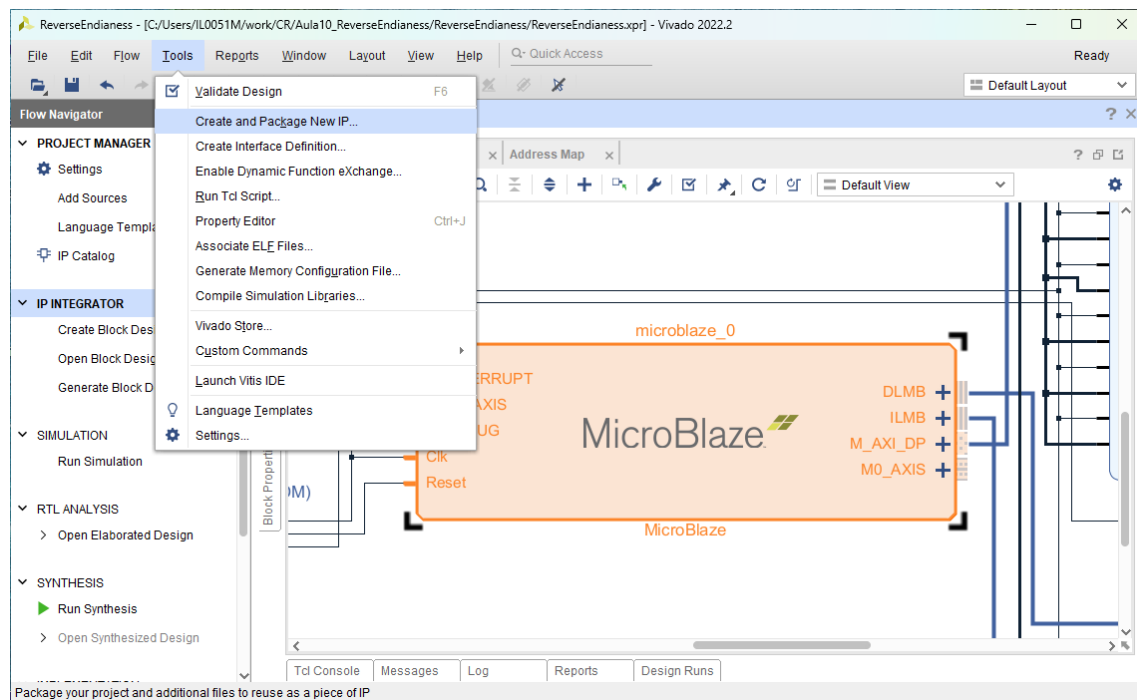
3. Navigate to the separator **Stream Interfaces**. Set **Number of Stream Links** to 1. Click **OK**.



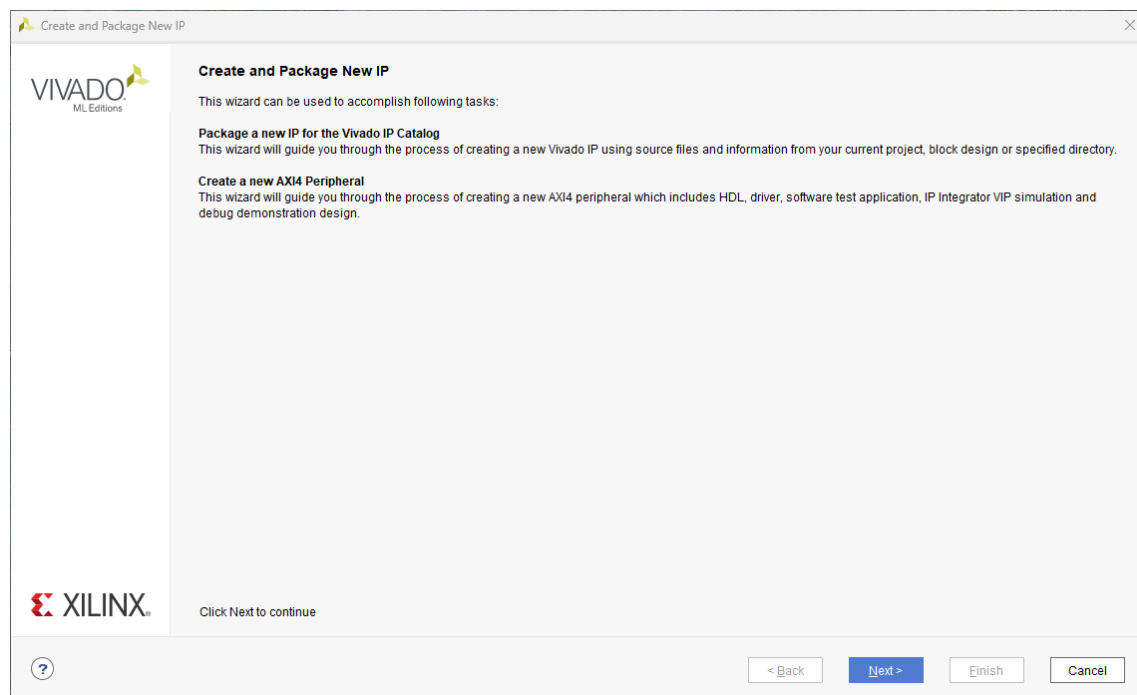
4. Note the new **AXI\_Stream** port (**S0\_AXIS**) in the MicroBlaze module.



## 5. Click on **Create and Package New IP**.



## 6. Click **Next** on the pop-up window.



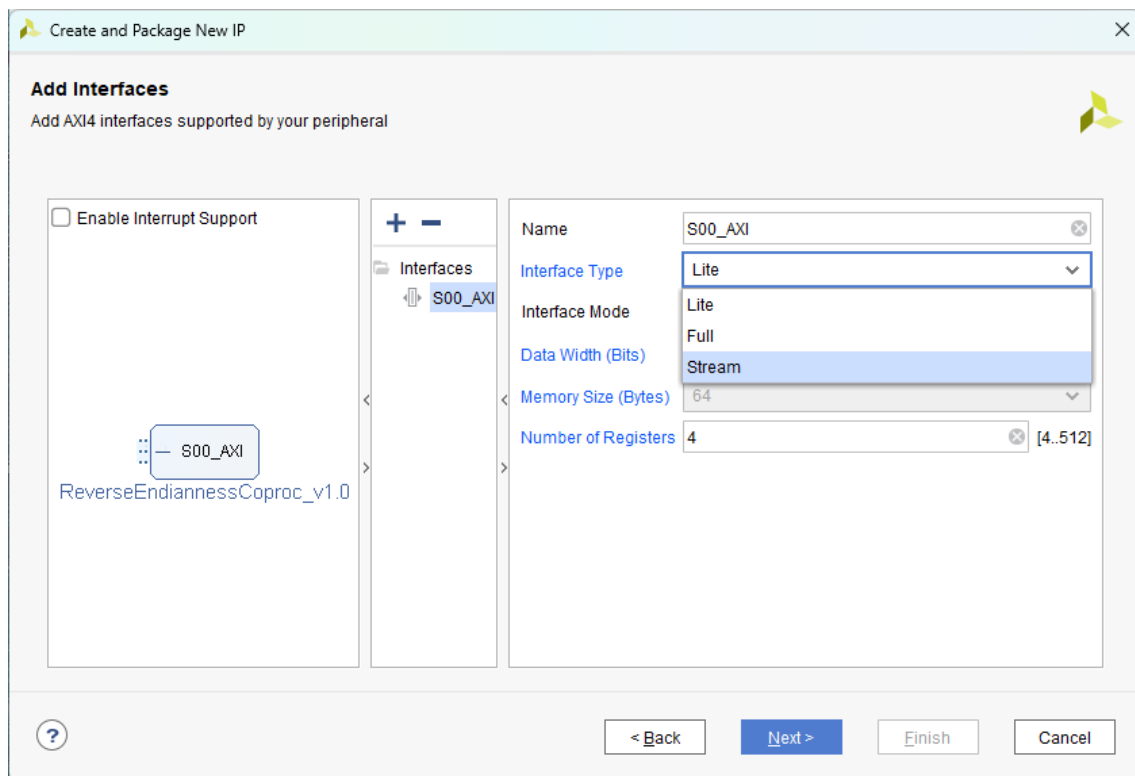
## 7. Select **Create a new AXI4 peripheral**.

The screenshot shows the 'Create and Package New IP' dialog box. The title bar says 'Create and Package New IP'. The main heading is 'Create Peripheral, Package IP or Package a Block Design'. Below it, it says 'Please select one of the following tasks.' There are two sections: 'Packaging Options' and 'Create AXI4 Peripheral'. In 'Packaging Options', there are three radio buttons: 'Package your current project' (selected), 'Package a block design from the current project' (with a dropdown menu showing 'mb\_design\_1'), and 'Package a specified directory'. In 'Create AXI4 Peripheral', there are two radio buttons: 'Create a new AXI4 peripheral' (selected) and 'Create an AXI4 IP, driver, software test application, IP Integrator AXI4 VIP simulation and debug demonstration design.' At the bottom, there are buttons: '< Back', 'Next >', 'Finish', and 'Cancel'.

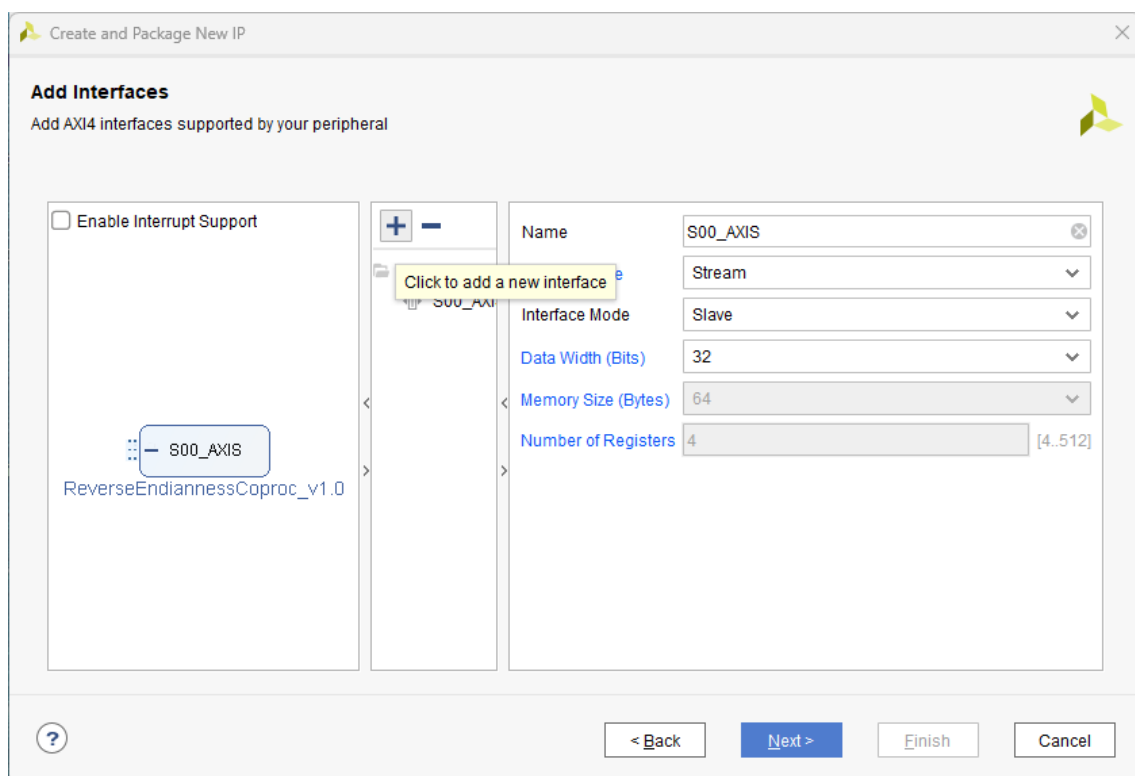
## 8. Name it at your discretion.

The screenshot shows the 'Create and Package New IP' dialog box, Step 2: Peripheral Details. The title bar says 'Create and Package New IP'. The main heading is 'Peripheral Details'. Below it, it says 'Specify name, version and description for the new peripheral'. There are five text input fields: 'Name' (ReverseEndiannessCoprocc), 'Version' (1.0), 'Display name' (ReverseEndiannessCoprocc\_v1.0), 'Description' (Reverse Endianness Coprocessor), and 'IP location' (C:/Users/IL0051M/work/CR/Aula10\_ReverseEndianness/ReverseEndianness/..ip\_repo). There is a checkbox 'Overwrite existing' which is unchecked. At the bottom, there are buttons: '< Back', 'Next >', 'Finish', and 'Cancel'.

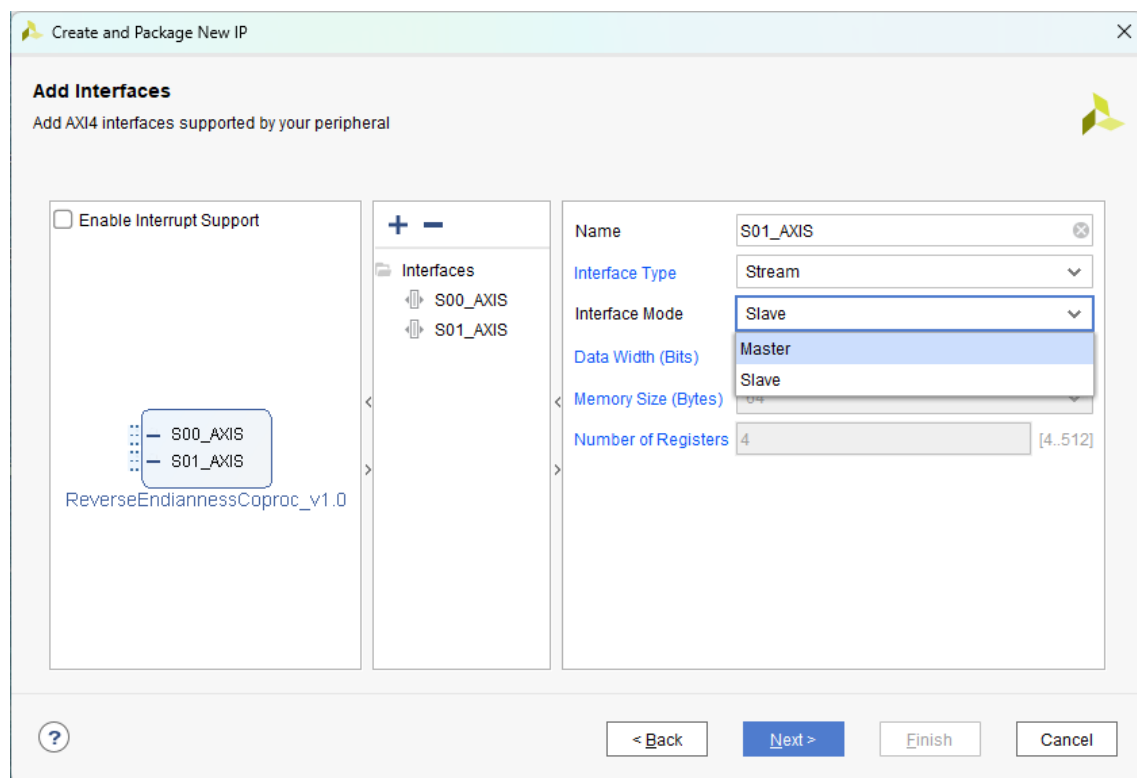
## 9. Set the **Interface Type** as **Stream**.



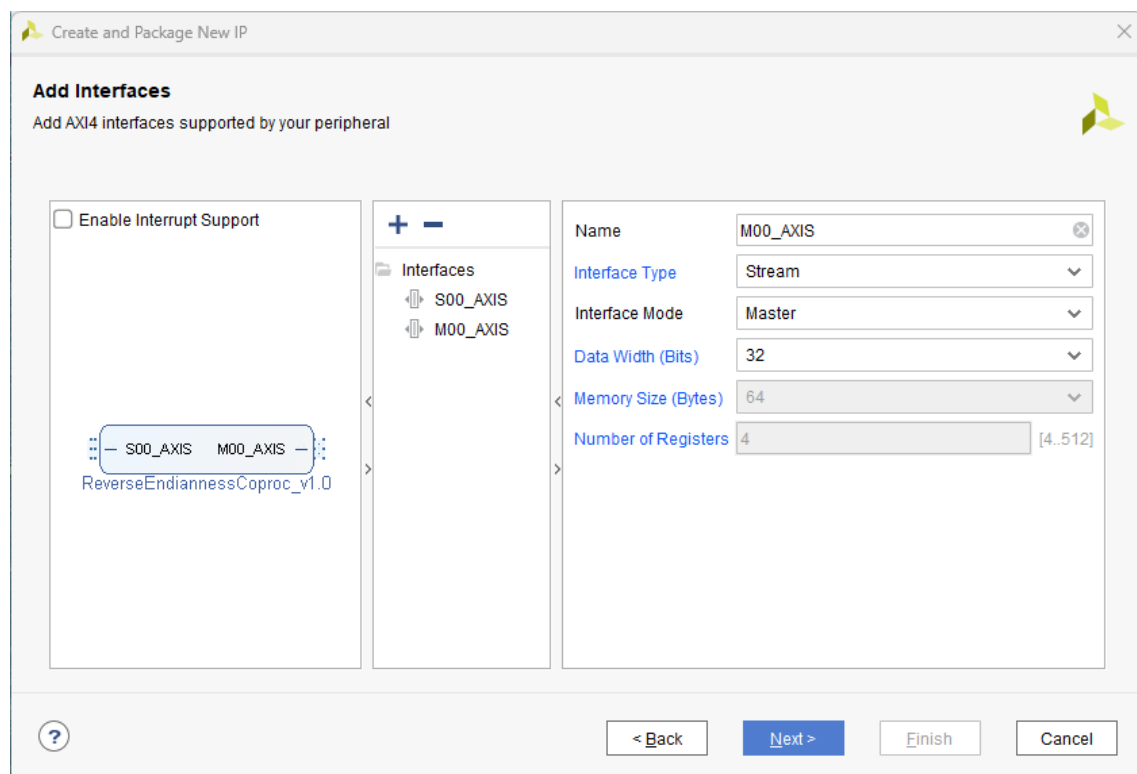
## 10. Click on + button to add a new interface.

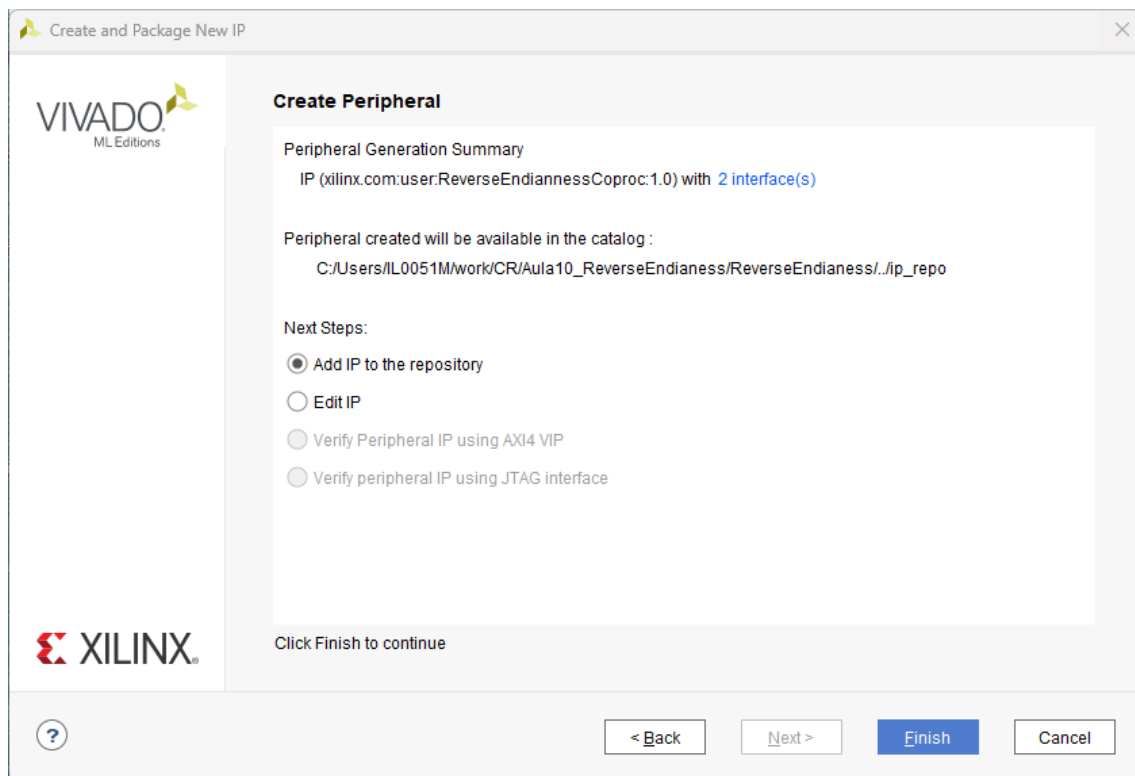


11. Set the new interface to be of type **Stream** and of mode **Master**.

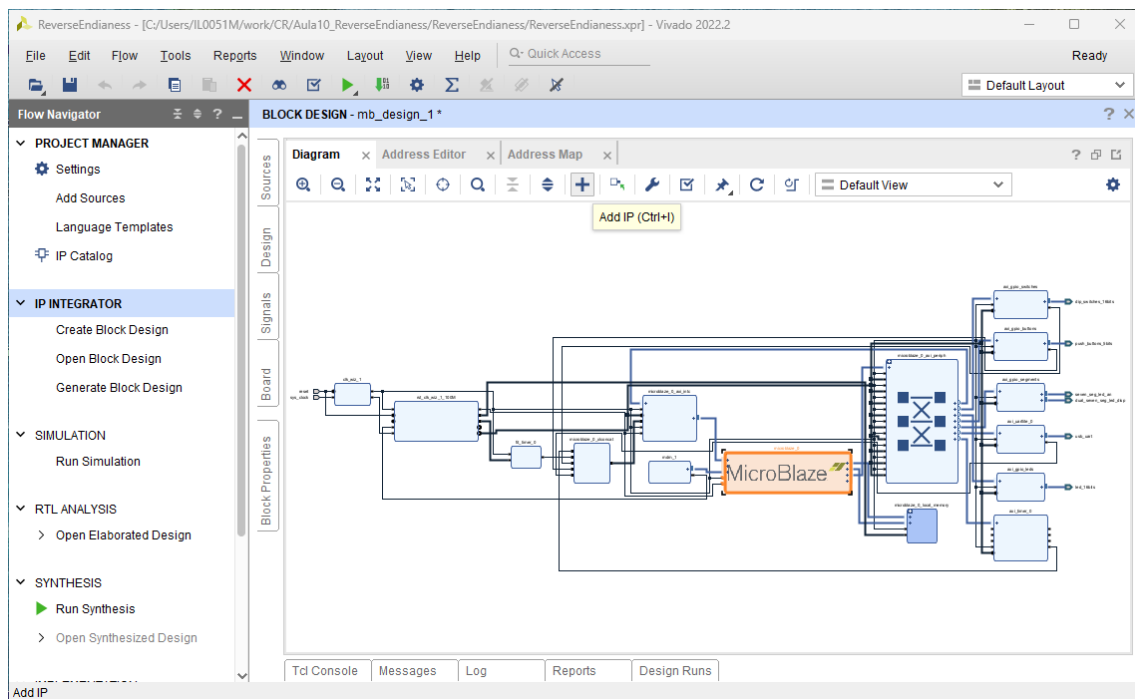


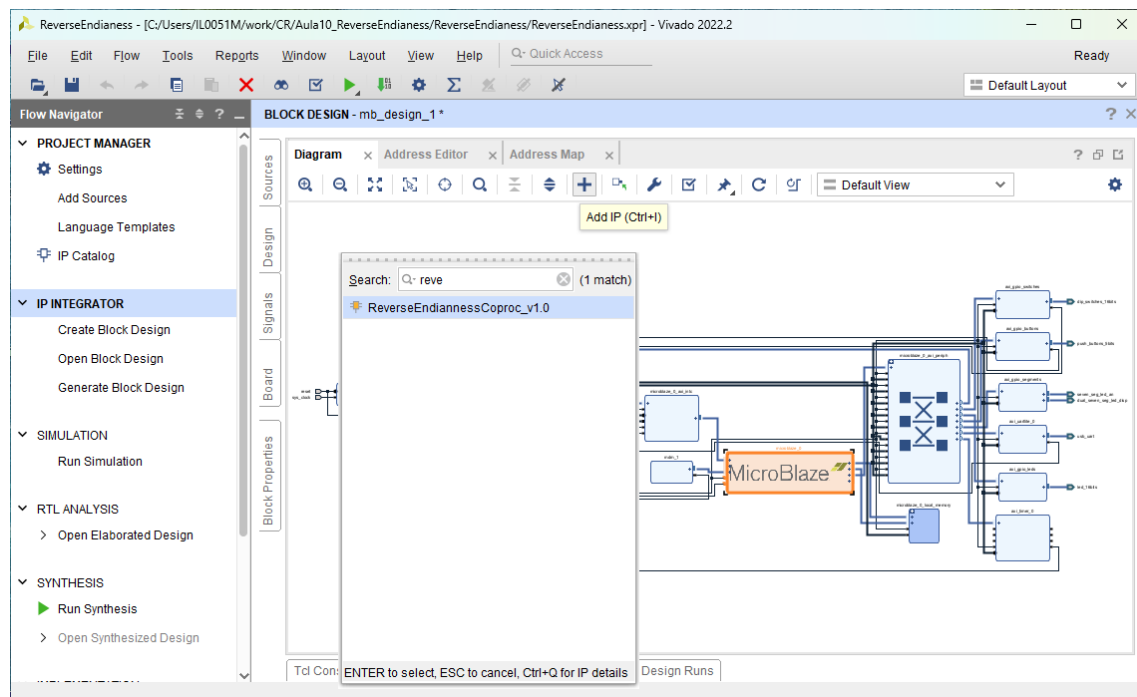
12. In the end, it should look like this. Click **Next**.



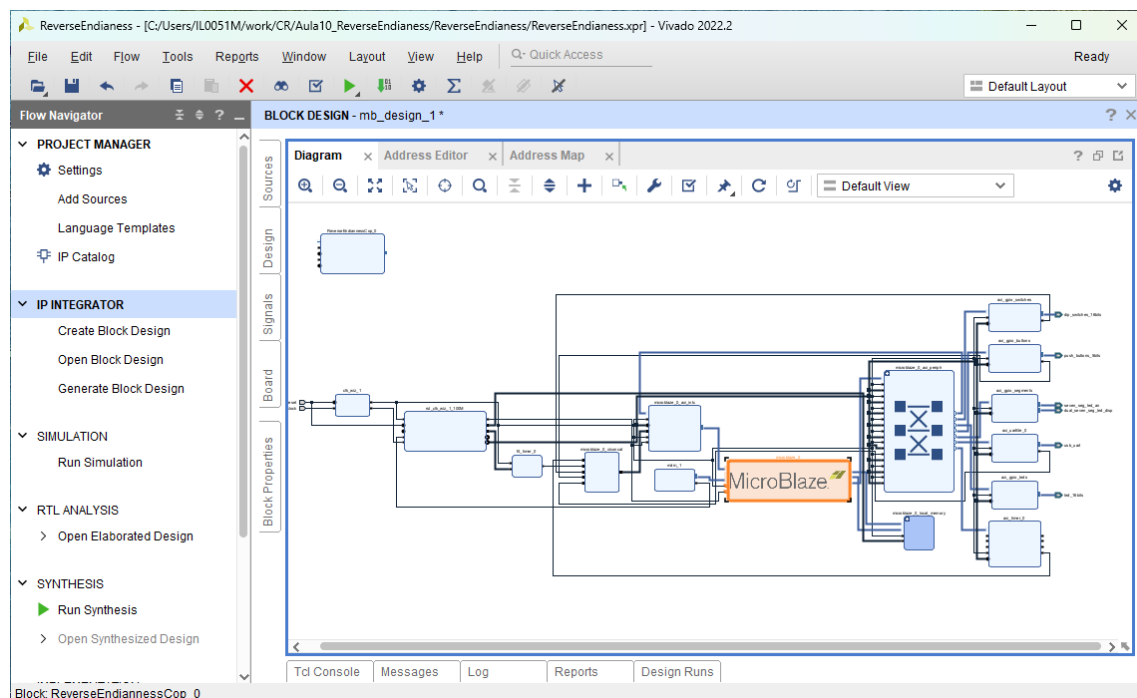
13. Click **Finish**.

## 14. Click on the + button (Add IP).



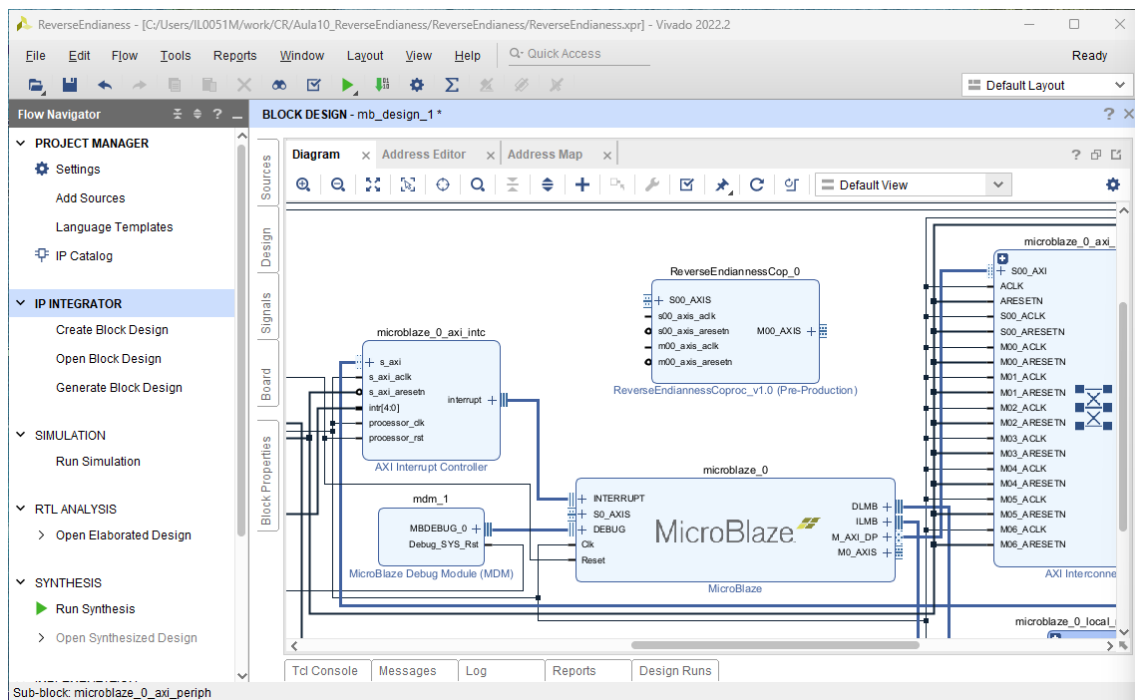
15. Search for the **ReverseEndianness** module.

## 16. It should appear in the diagram.

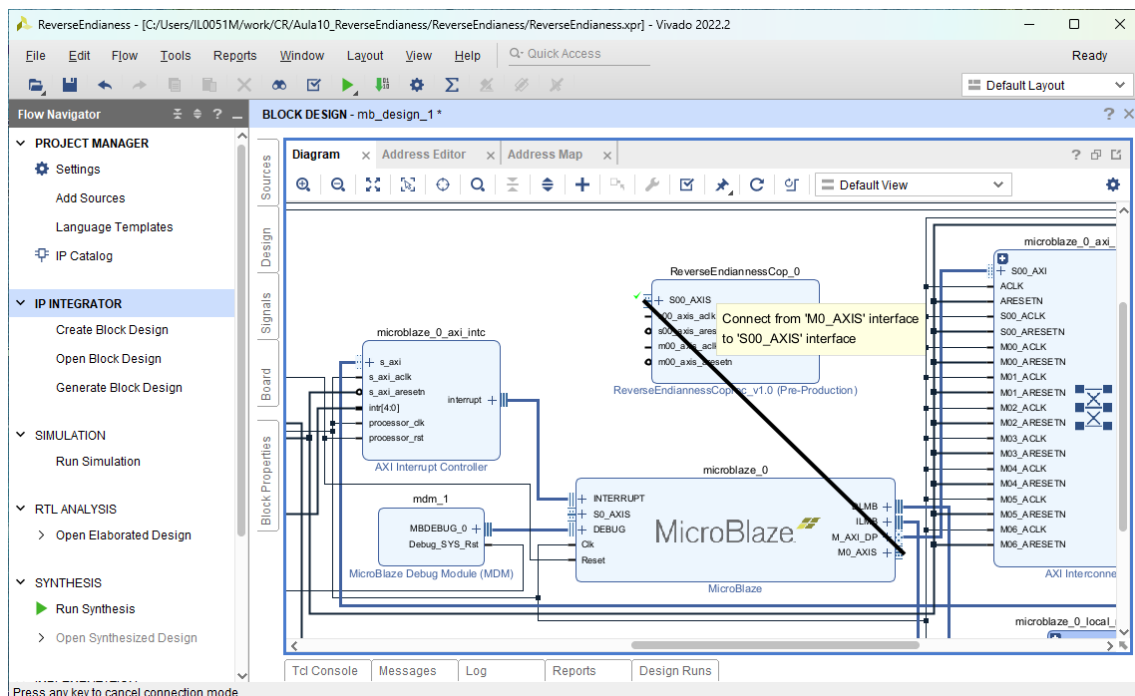




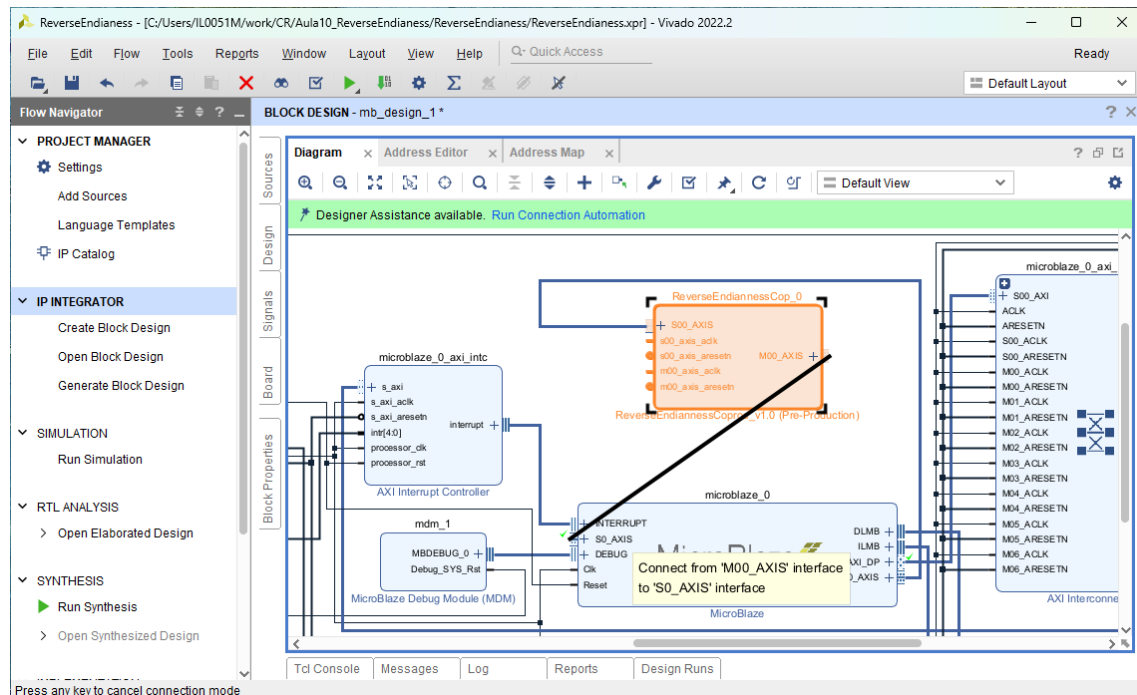
17. Place the **ReverseEndianness** module next to the **MicroBlaze**.



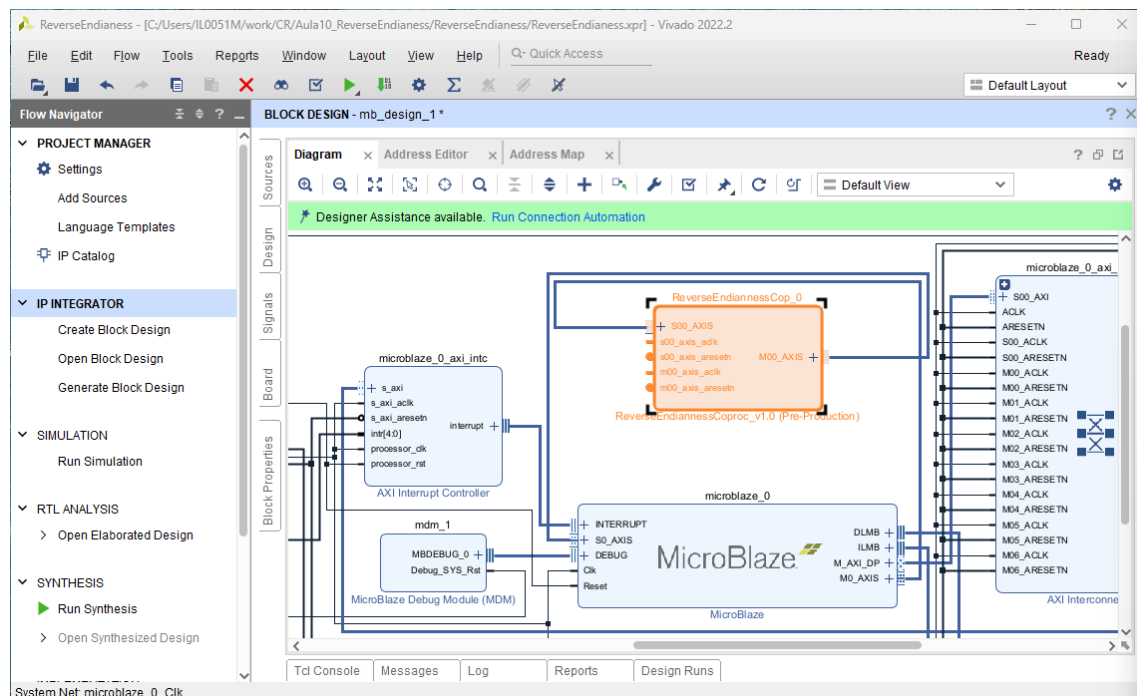
18. Connect from **M0\_AXIS** interface (in MicroBlaze) to the **S00\_AXIS** interface (in the module).



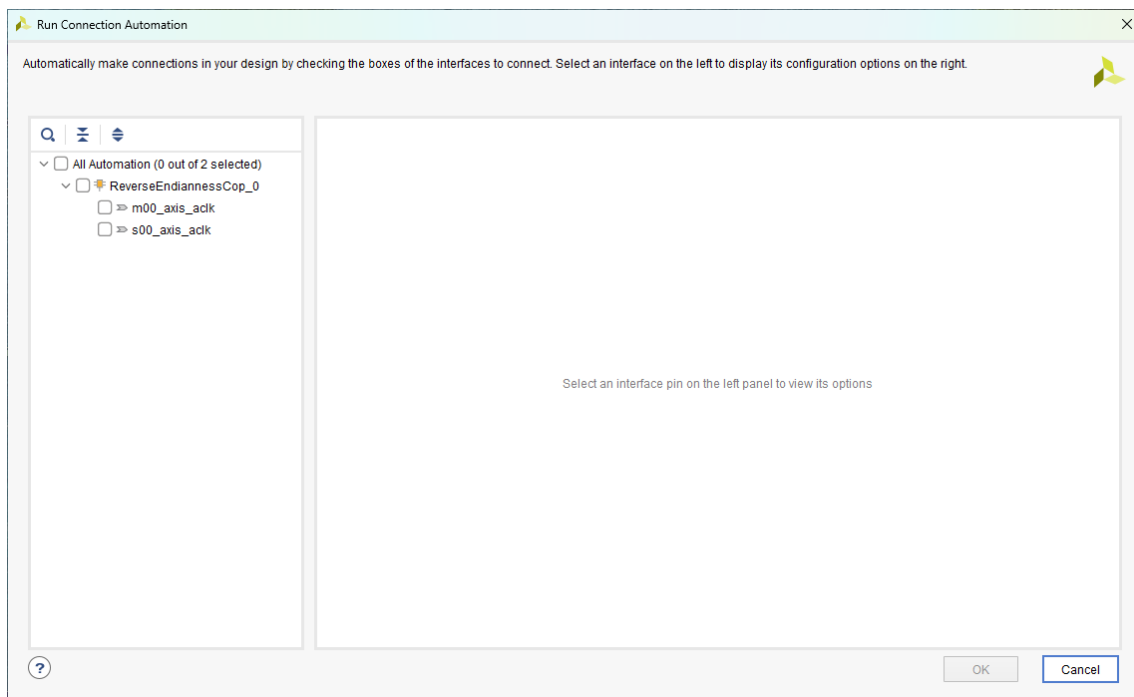
19. Connect from **S0\_AXIS** interface (in MicroBlaze) to **M00\_AXIS** interface (in the module).



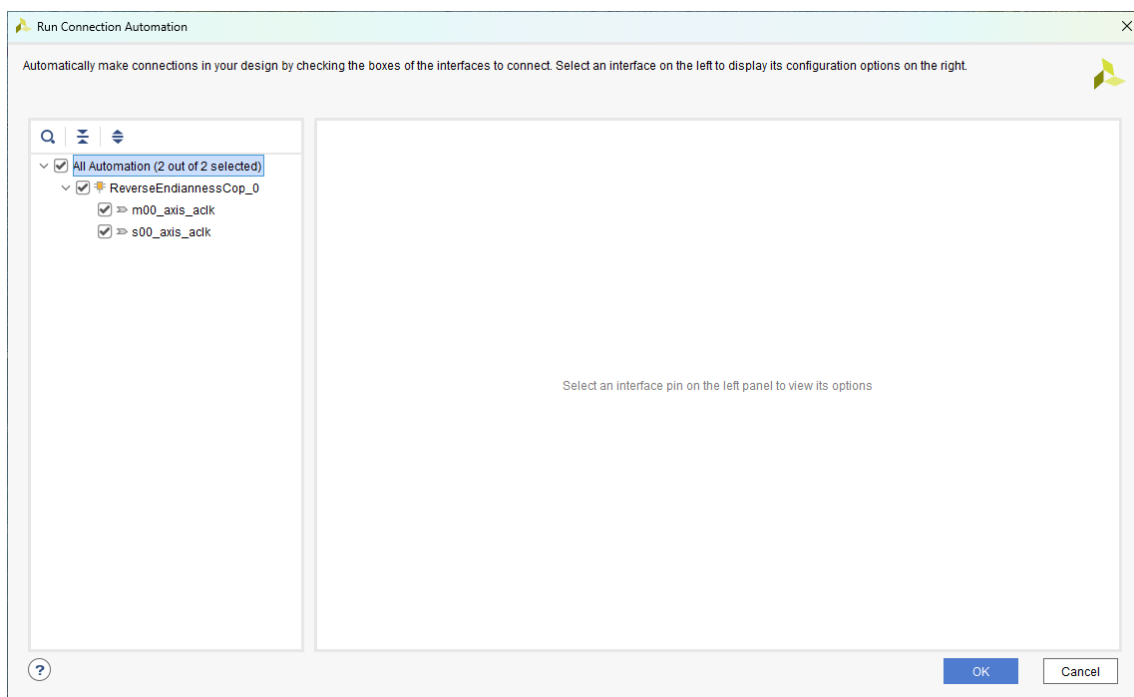
20. The result should look like the figure below. Click on **Run Connection Automation**.



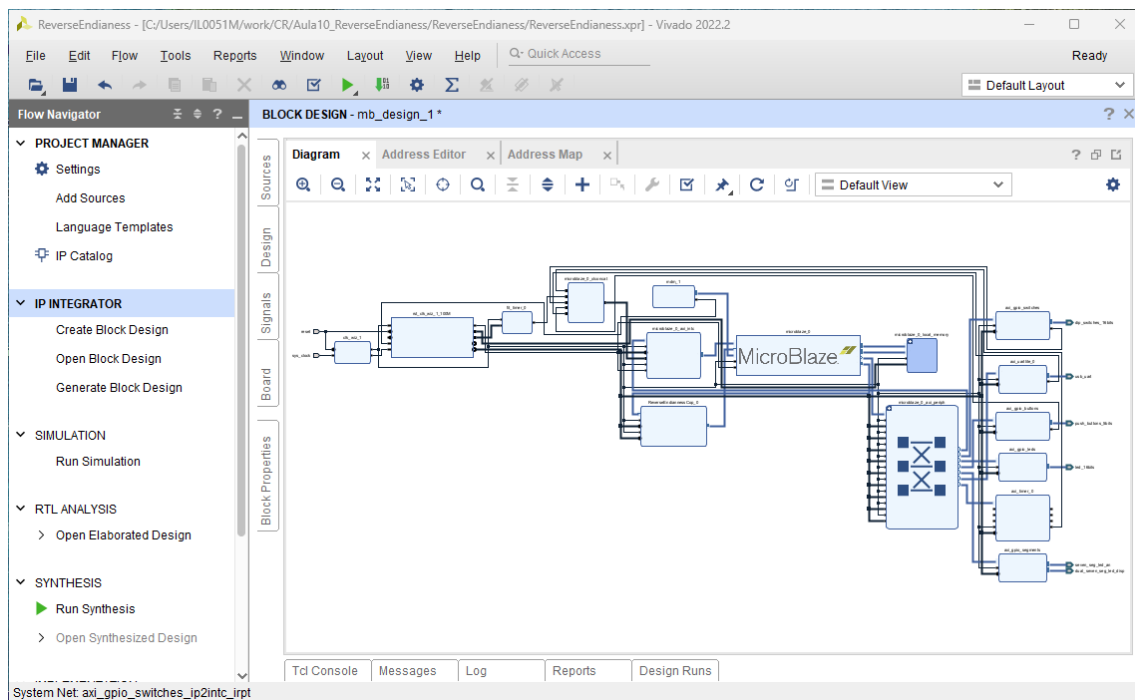
21. The following window opens.



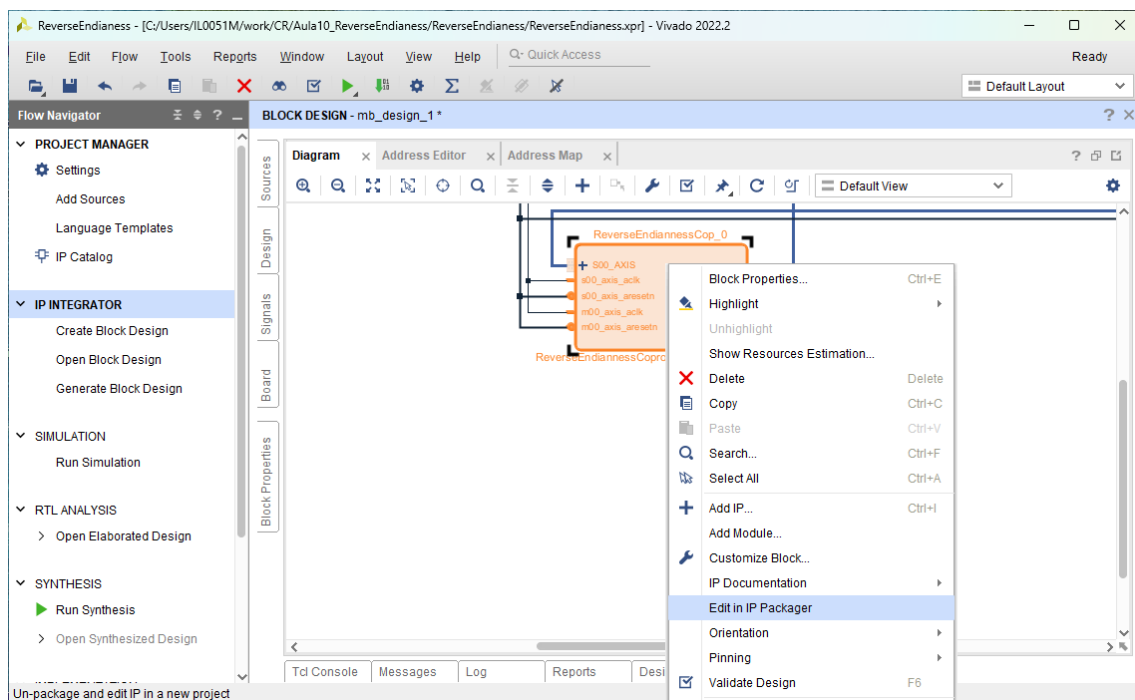
22. Tick all boxes.



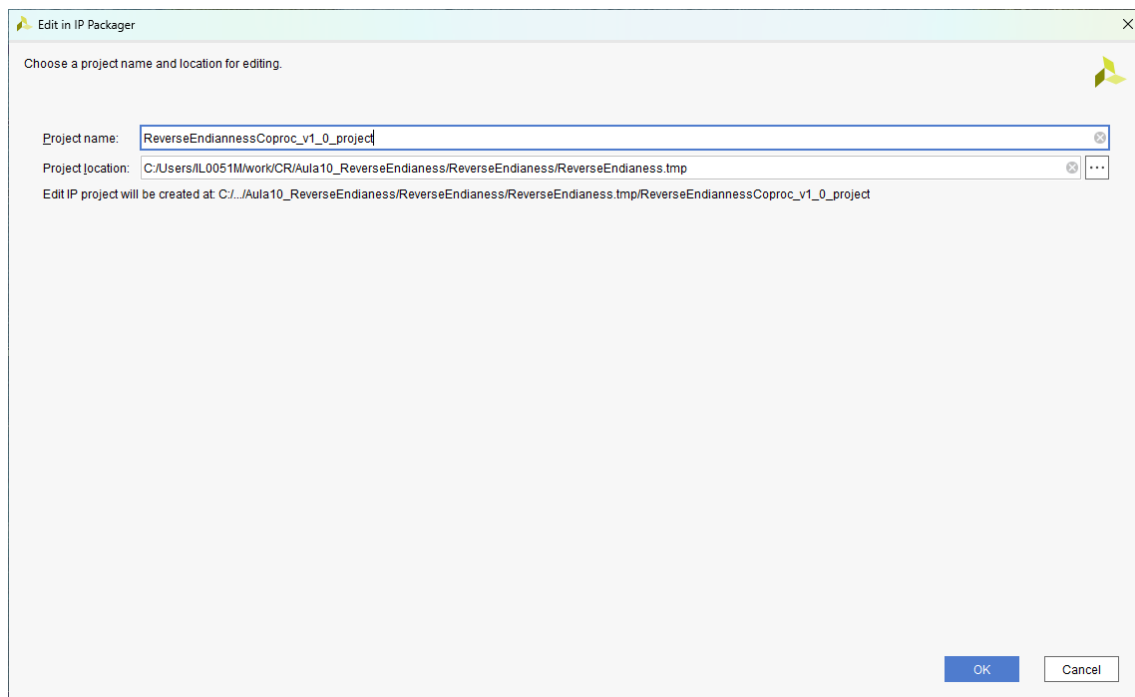
### 23. Click on **Regenerate Layout** (optional).



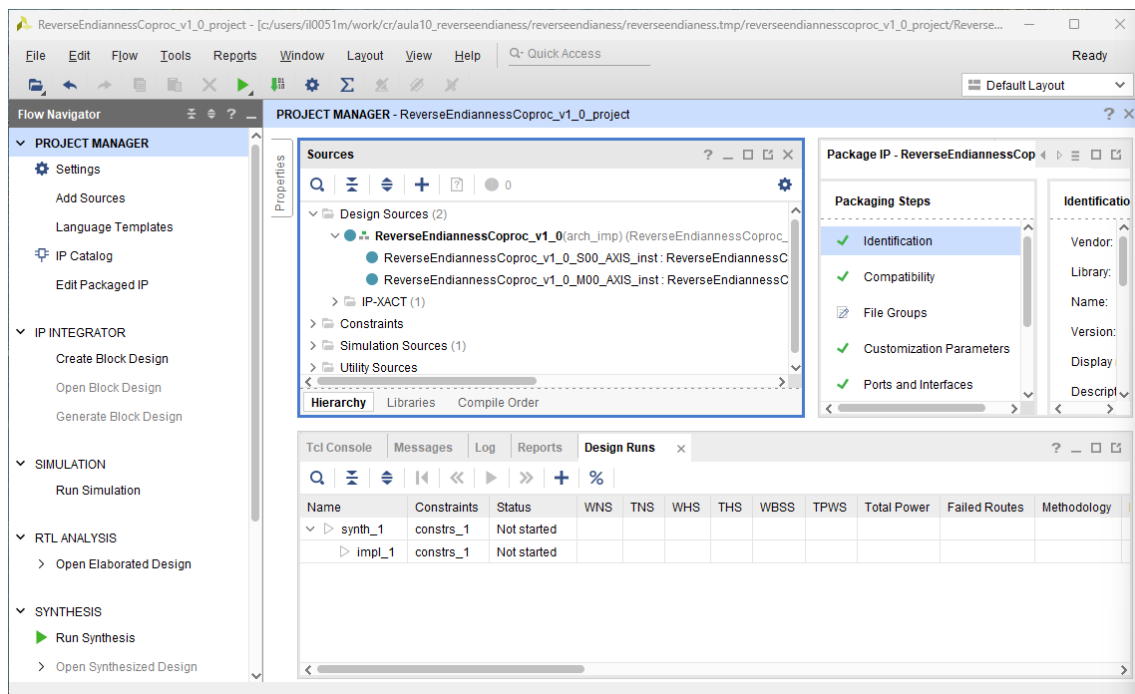
### 24. Right-click on the module. Click on **Edit in IP Packager...**



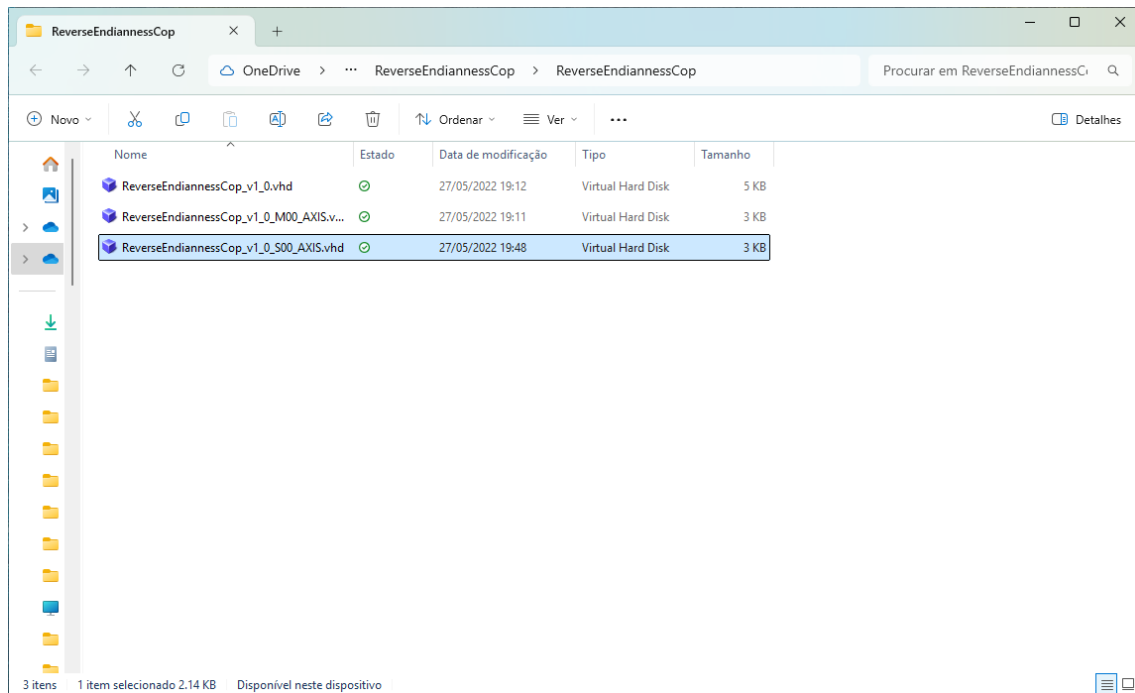
25. Click **OK**.



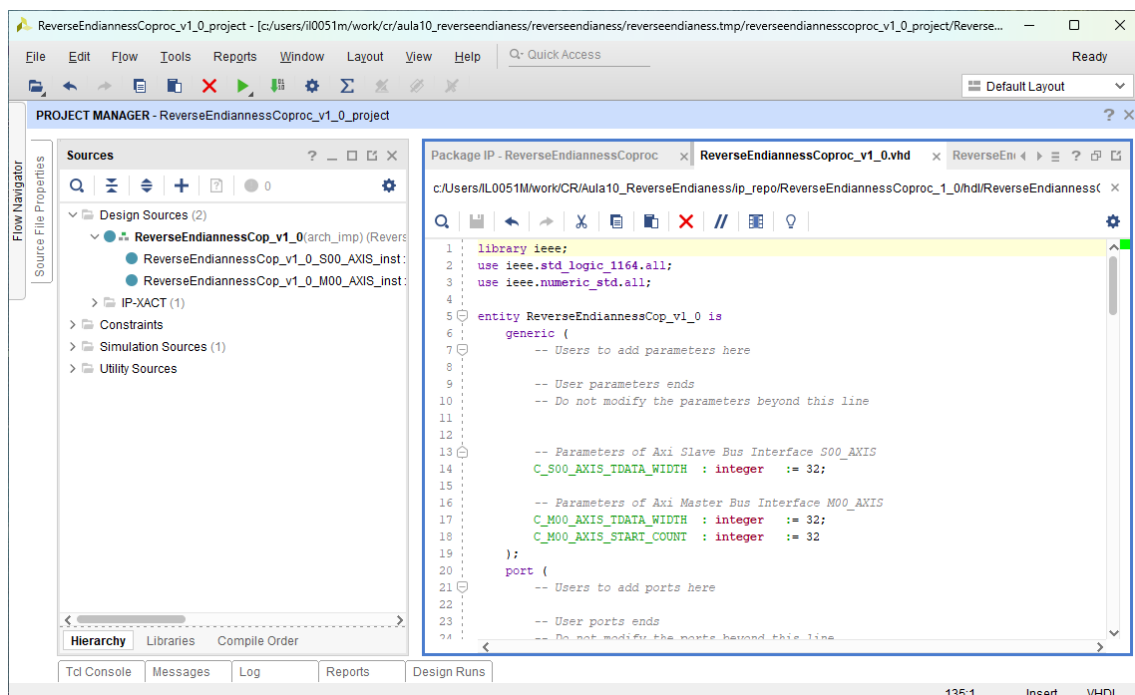
26. A new **Vivado** window opens. Notice that we now have 3 files (instead of just 2 on the AXI4-Lite bus).



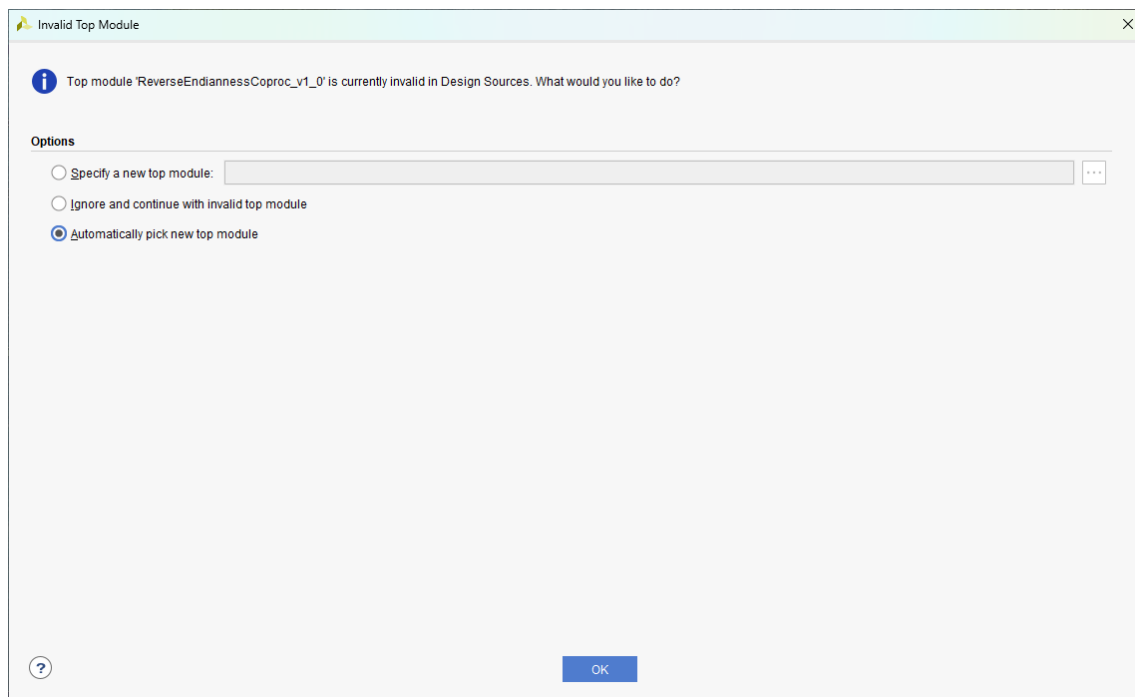
27. From the Moodle, fetch the file **ReverseEndiannessCop.rar**. Unzip it. Three files should be available.



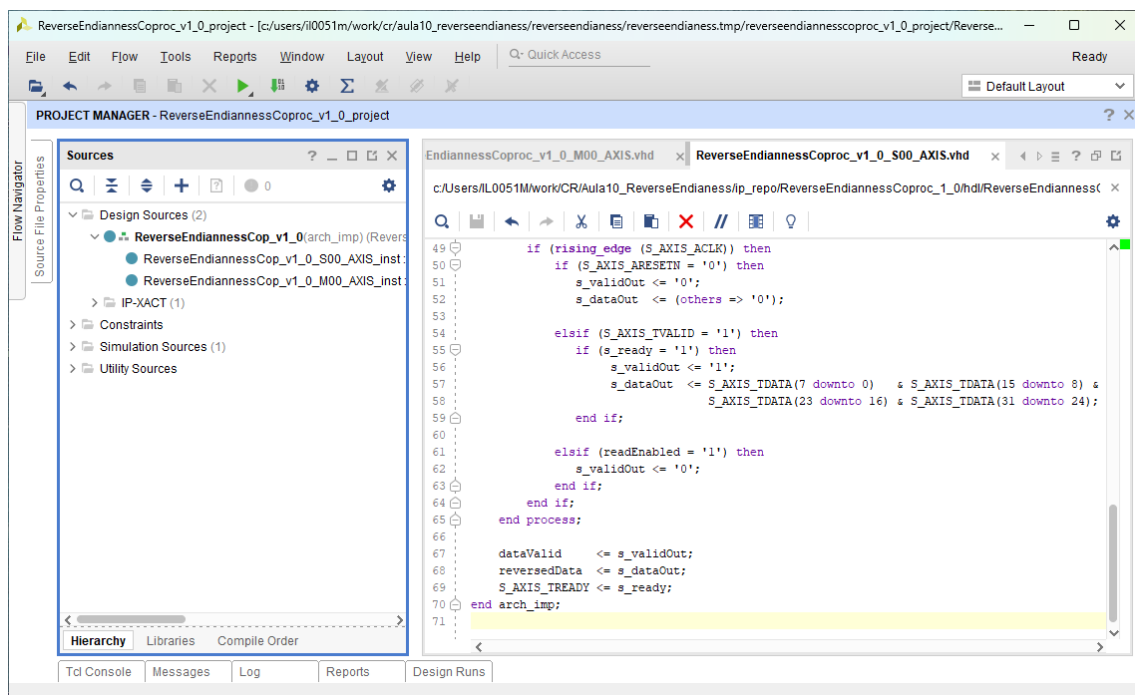
28. Replace the code of each of the three files.



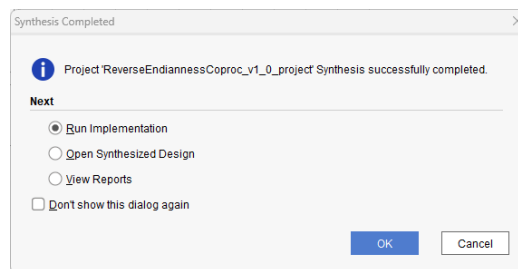
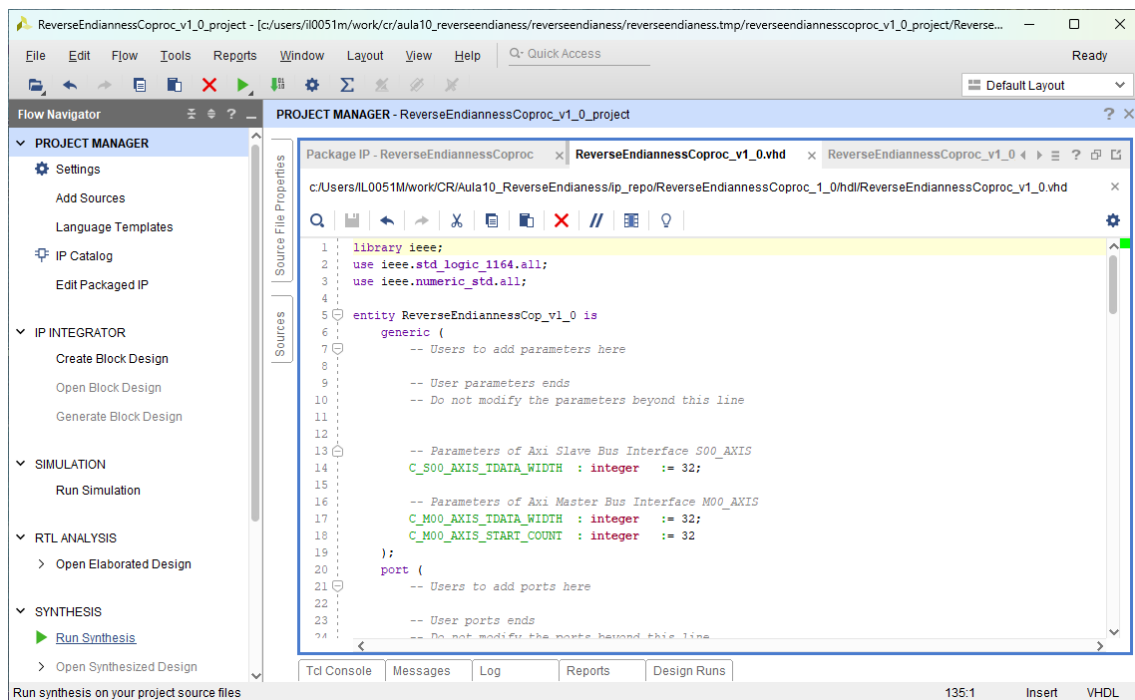
29. If this pop-up window shows up, click **OK**.



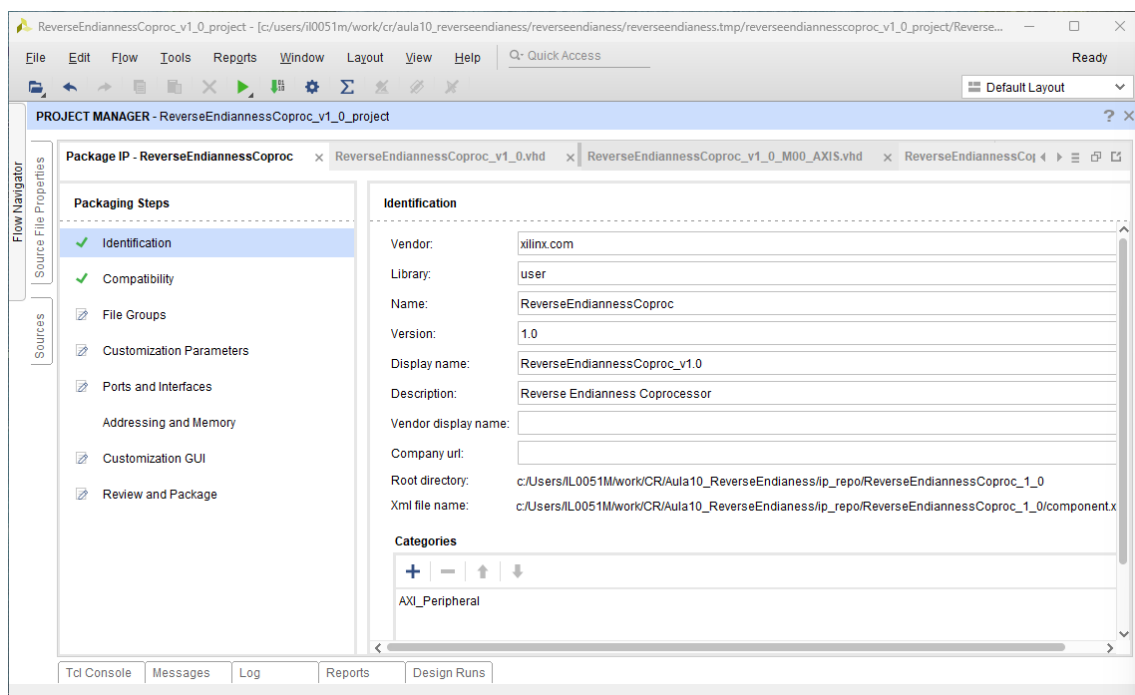
30. Confirm the hierarchical order of the files (in **Sources**).



31. Click on **Synthesis**. Close the pop-up window (click on the top right X).

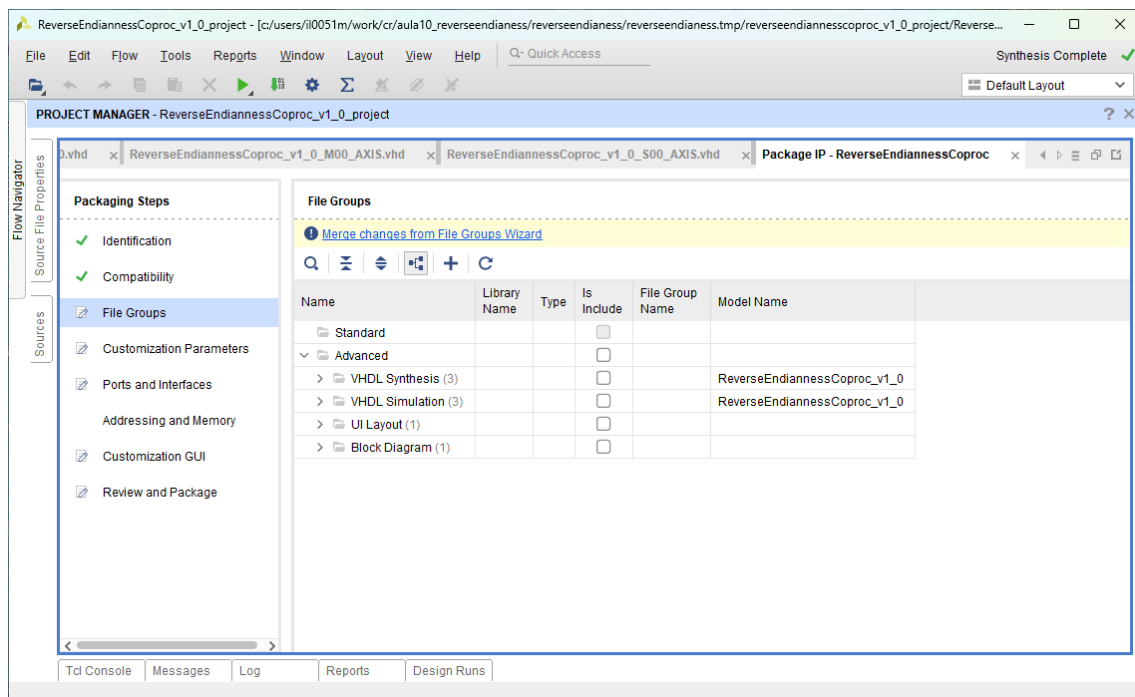


32. Open the **Package IP** tab.

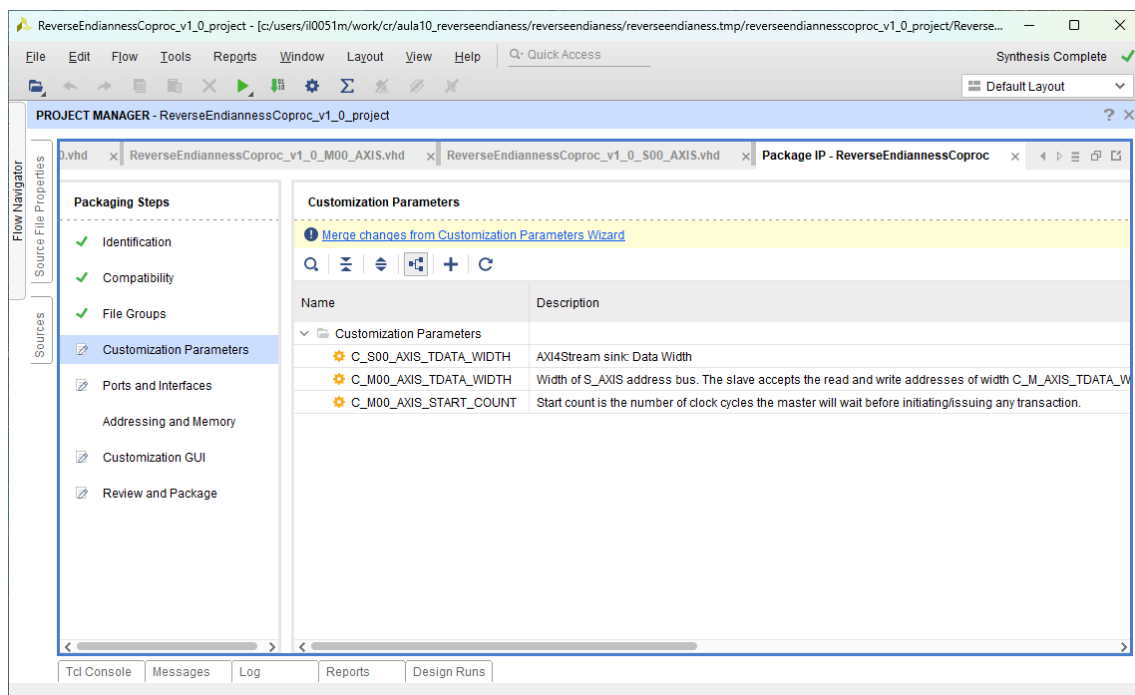


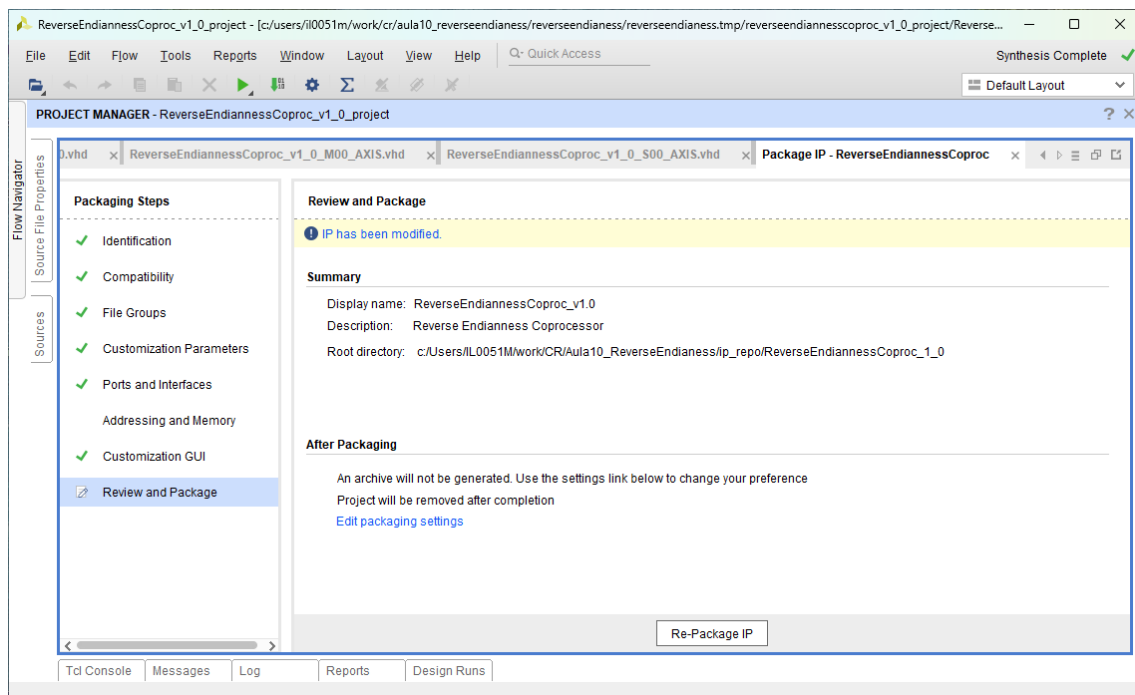
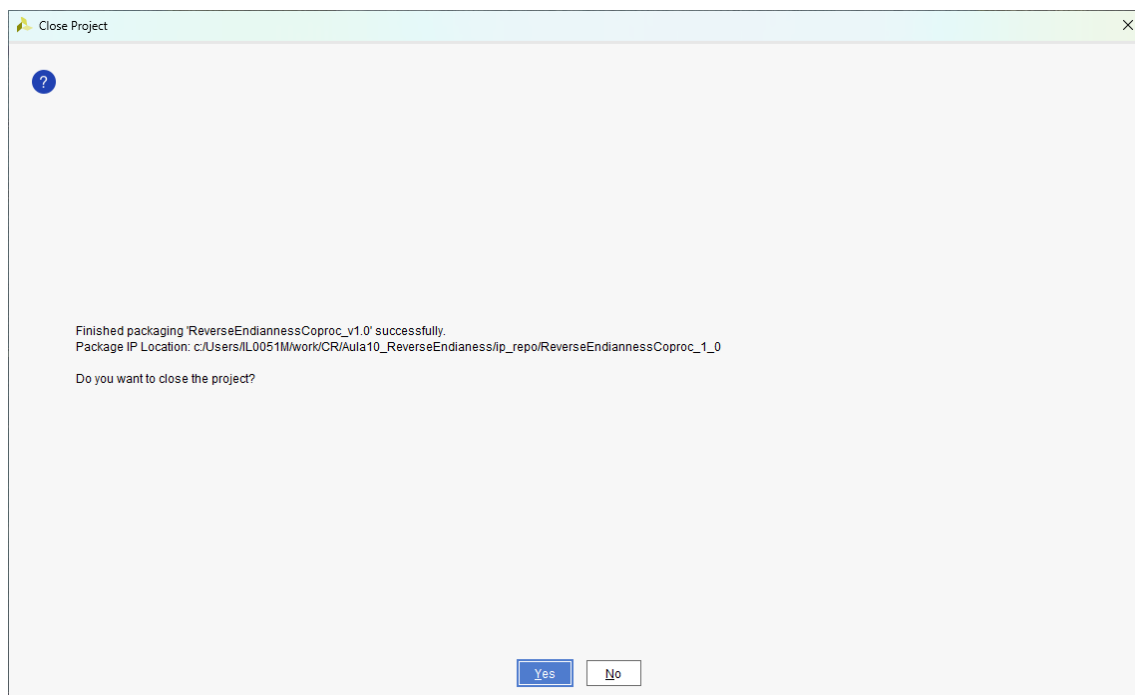


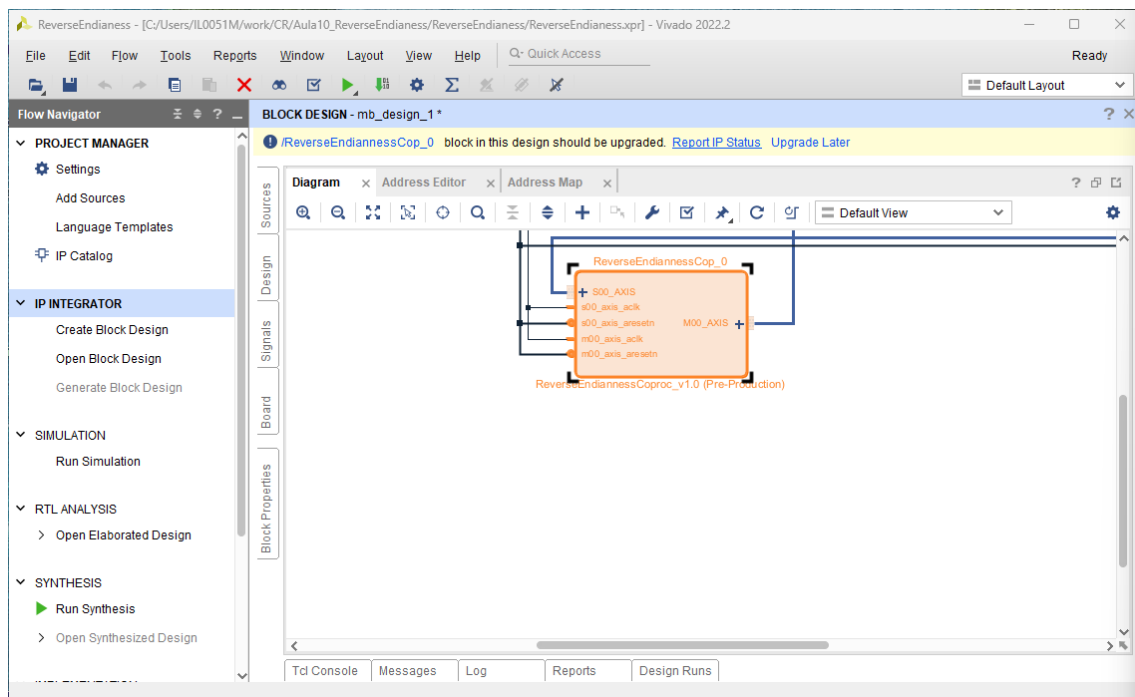
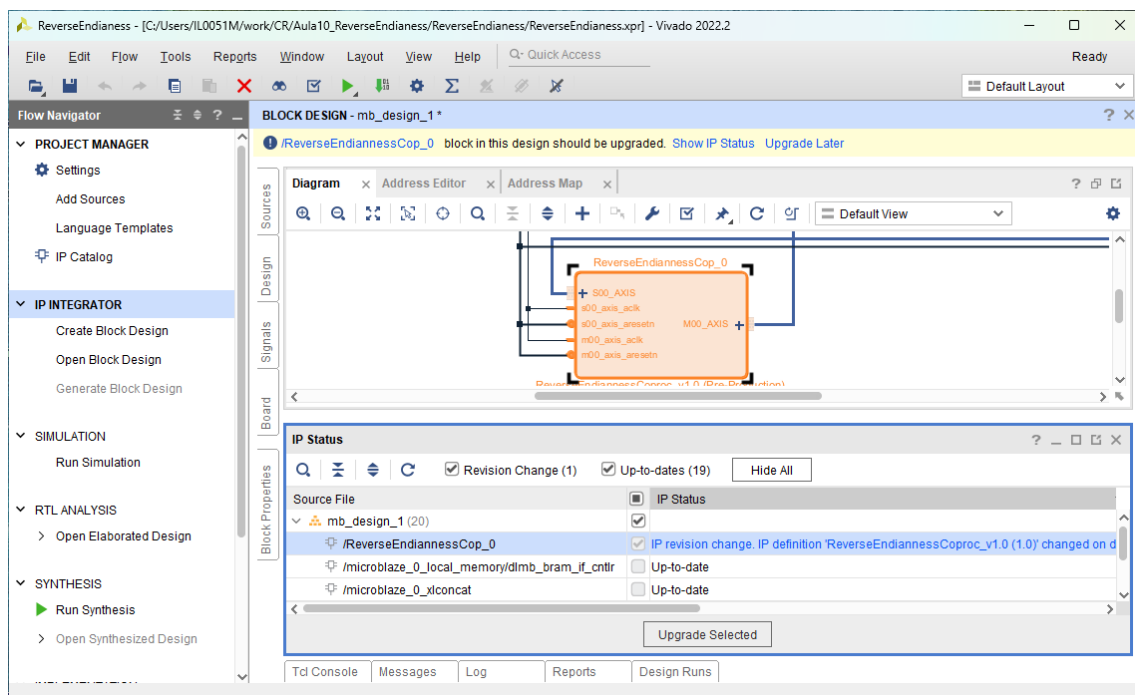
### 33. Select the **File Groups** tab. Click on **Merge Changes...**



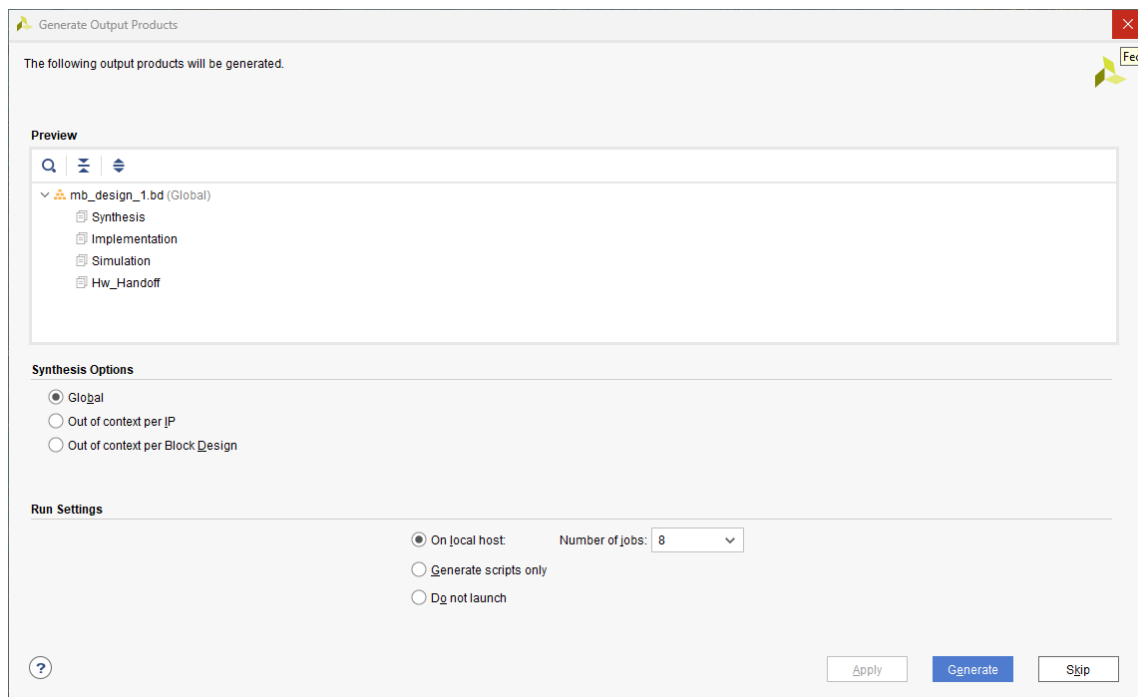
### 34. Select the **Customization Parameters** tab. Click on **Merge Changes...**



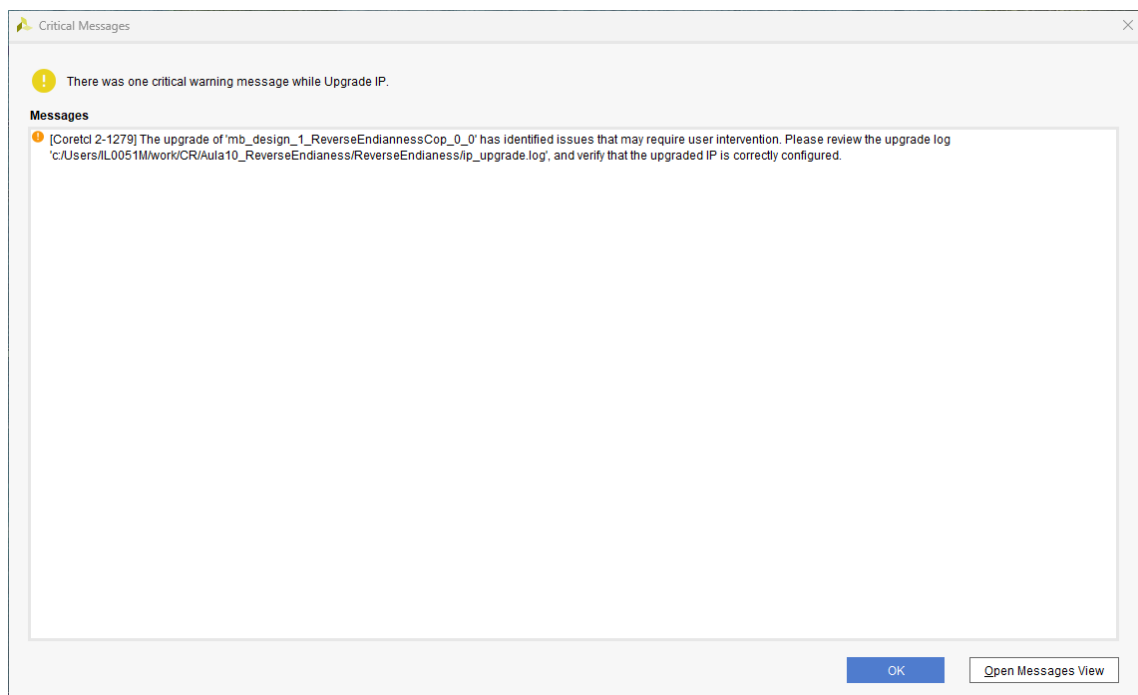
**35. Click on Re-Package IP.****36. Click OK.**

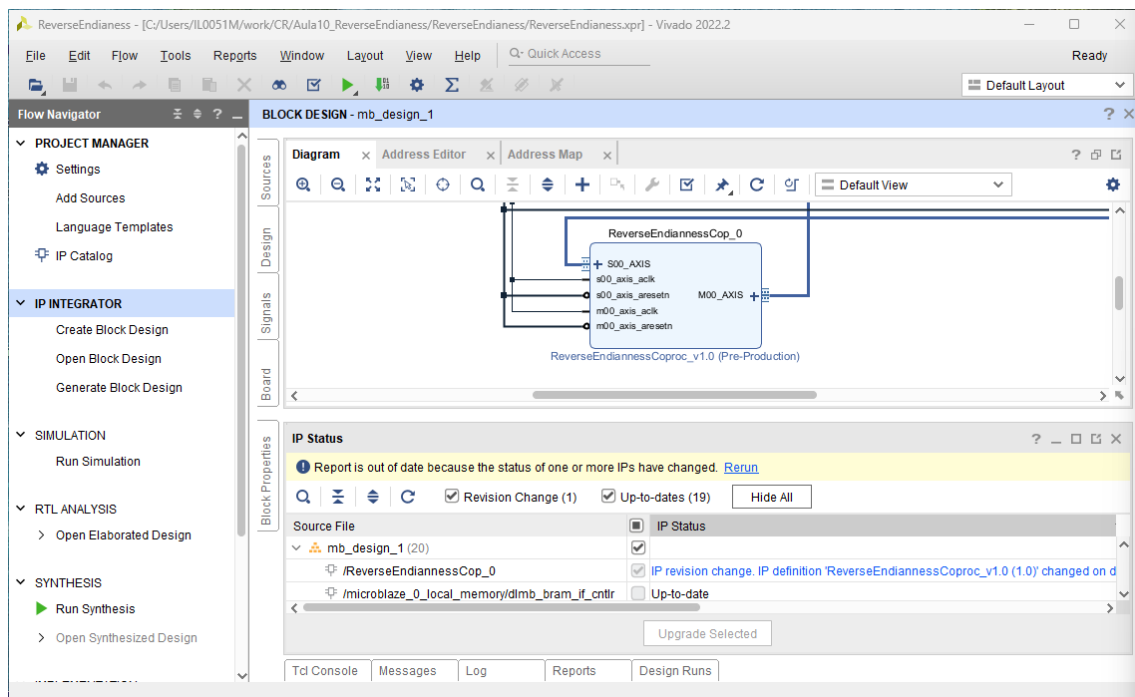
37. Click on **Report IP Status**.38. Click on **Upgrade Selected**.

39. Close the pop-up window (on the top right **X**).

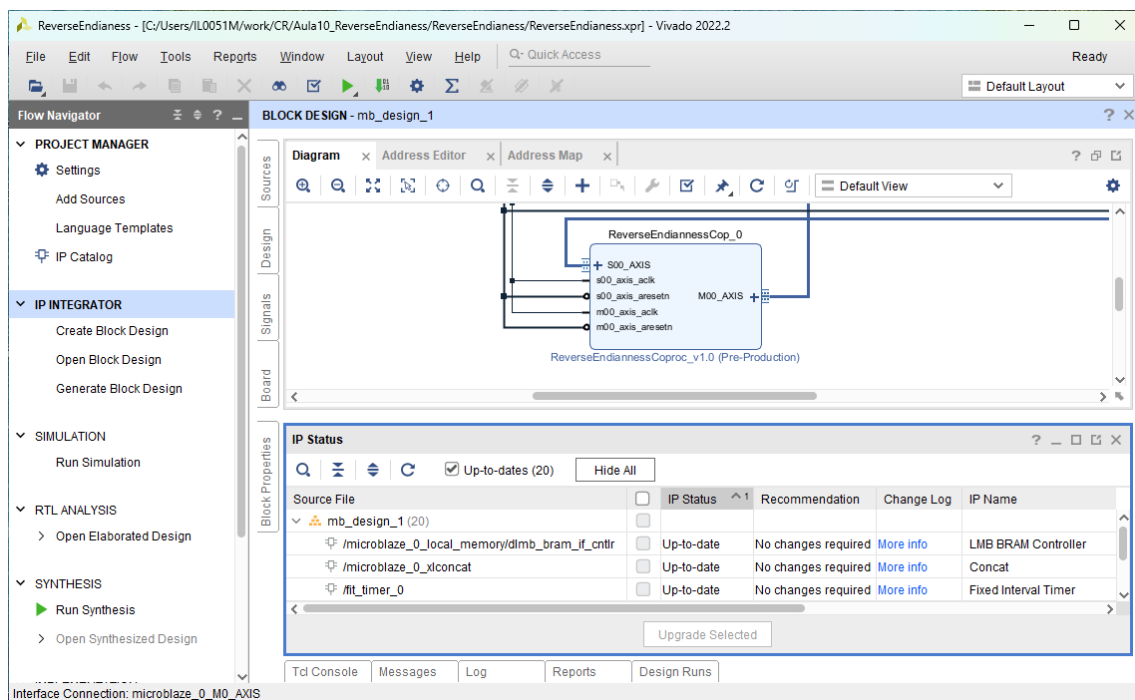


40. A warning window pops up. Click **OK**.

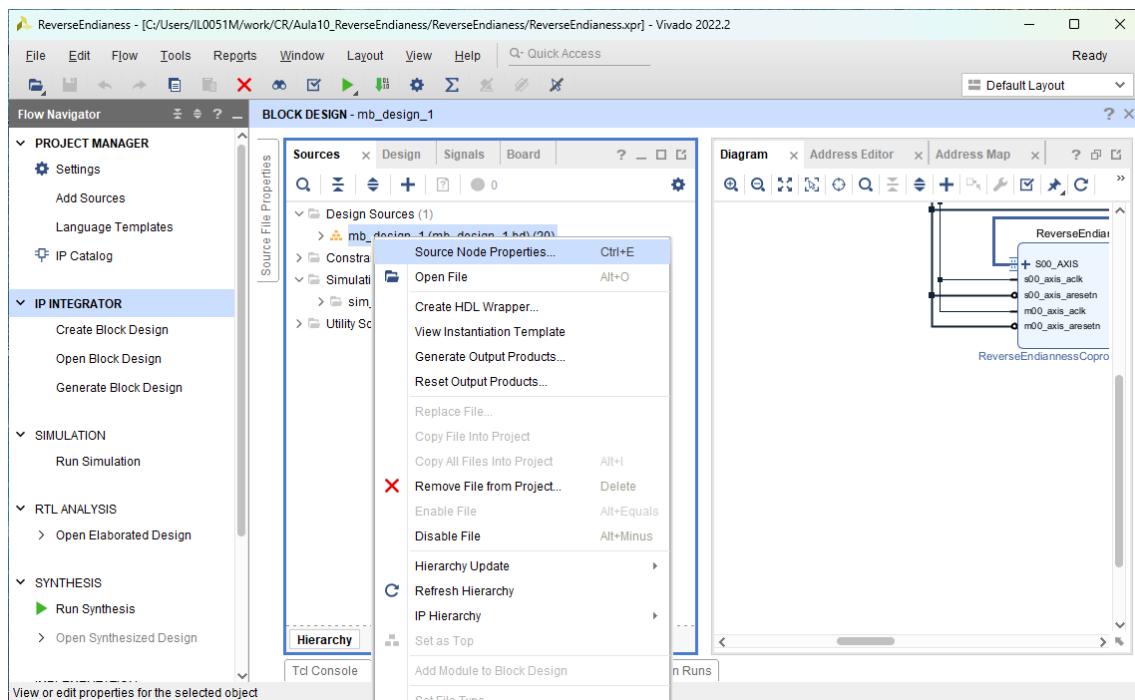


41. Click on **Re-run**.

## 42. Confirm the status of the new module.



43. Click on **Generate Output Products**, and after that, on **Create HDL Wrapper**.



44. Click on **Generate Bitstream**.

45. Click on **File > Export > Export Hardware**.

**Congratulations!**

Sources: AMD Xilinx documentation.