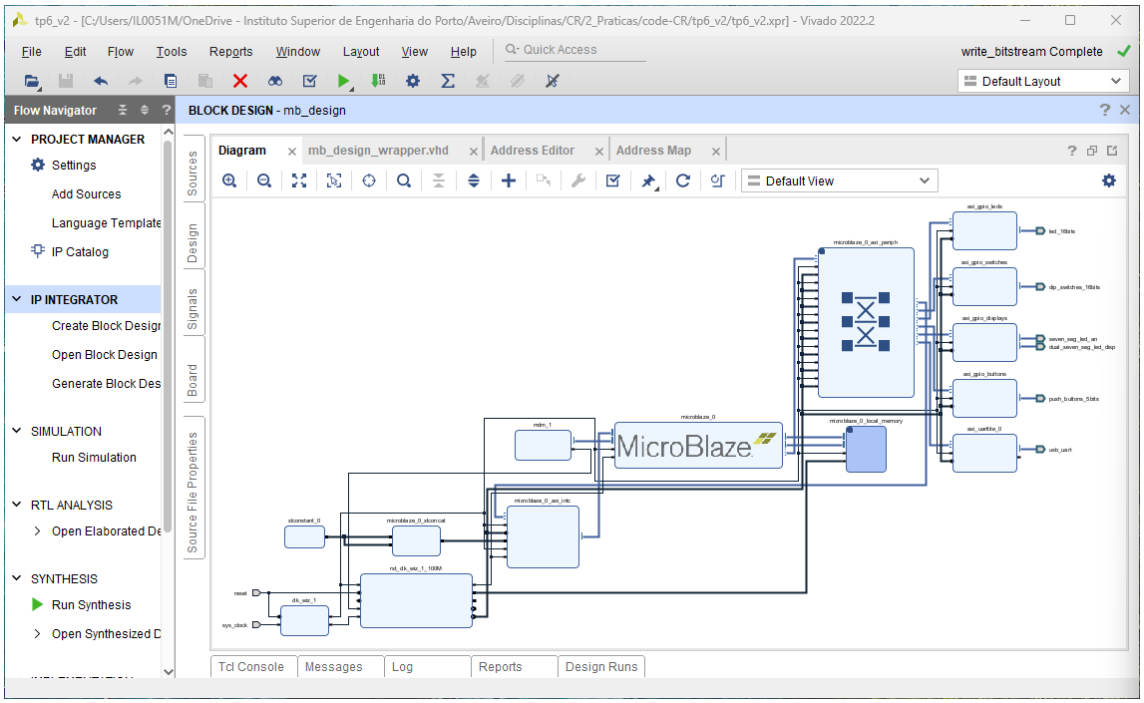
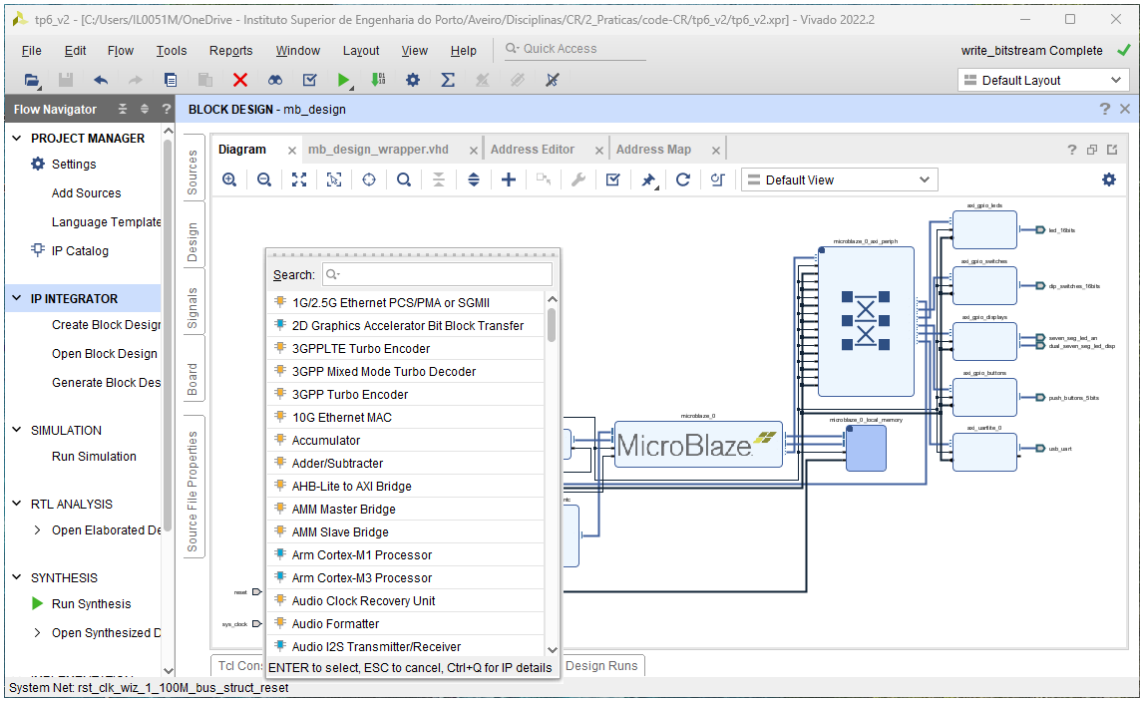
Instructions to update MicroBlaze Platform to handle Interrupts

1. Start **Vivado.**

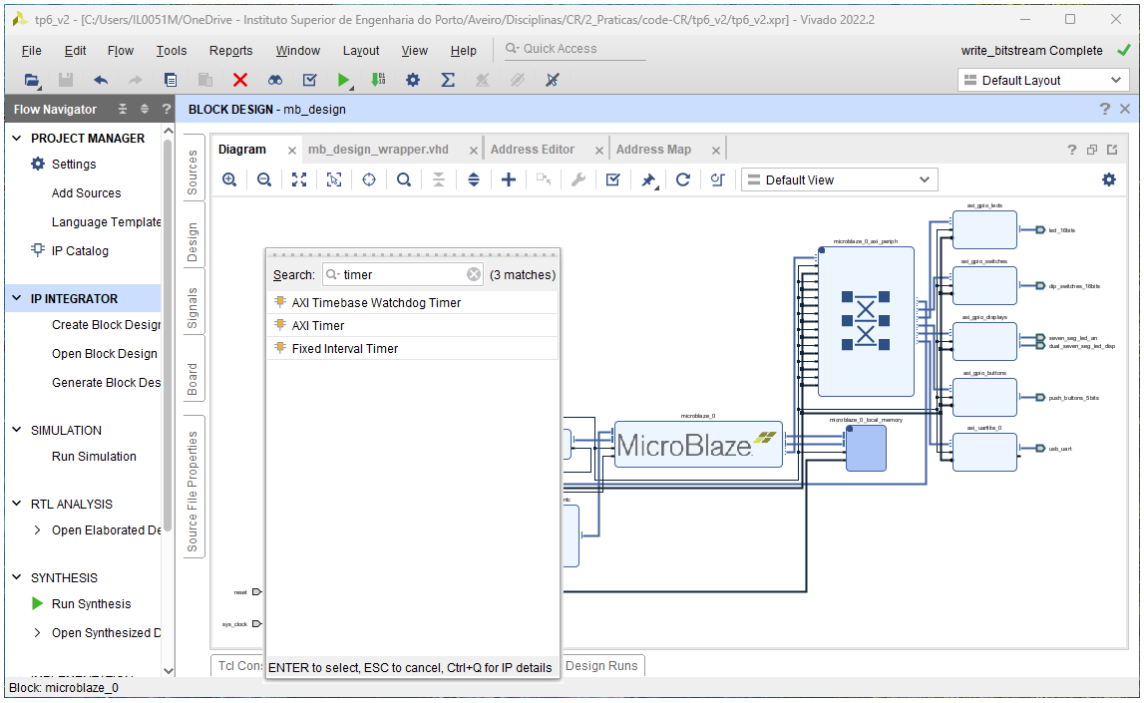
2. Load the Lab.5 project.



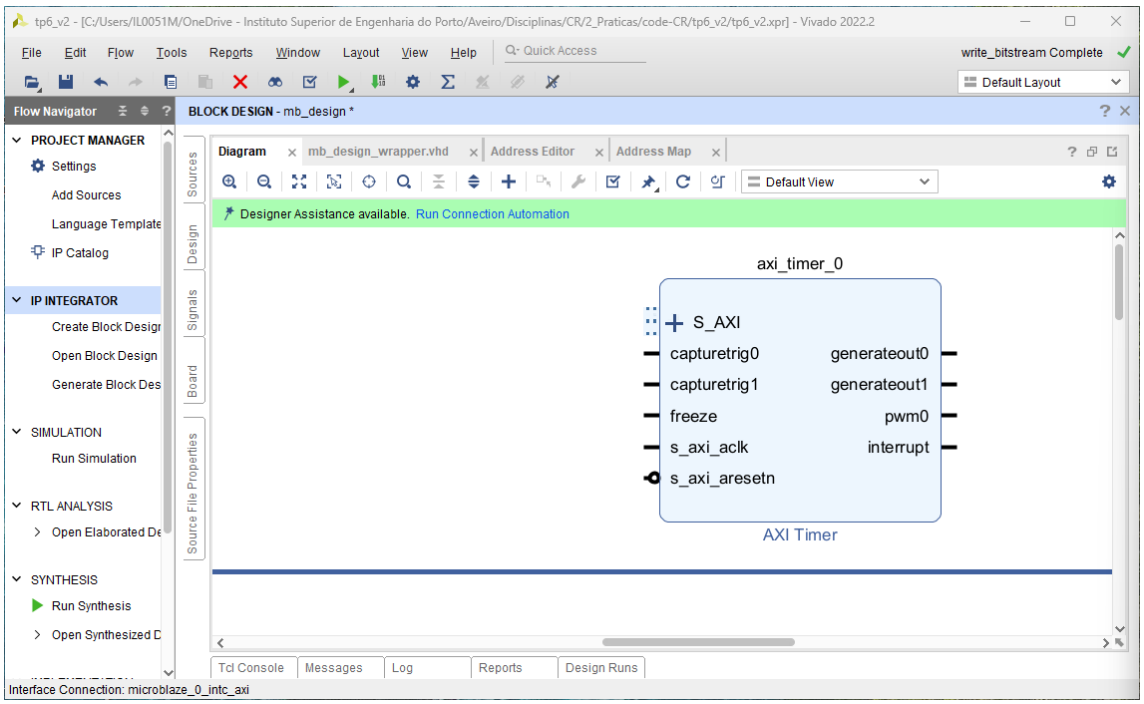
3. Click on the **+** sign to add a new block.



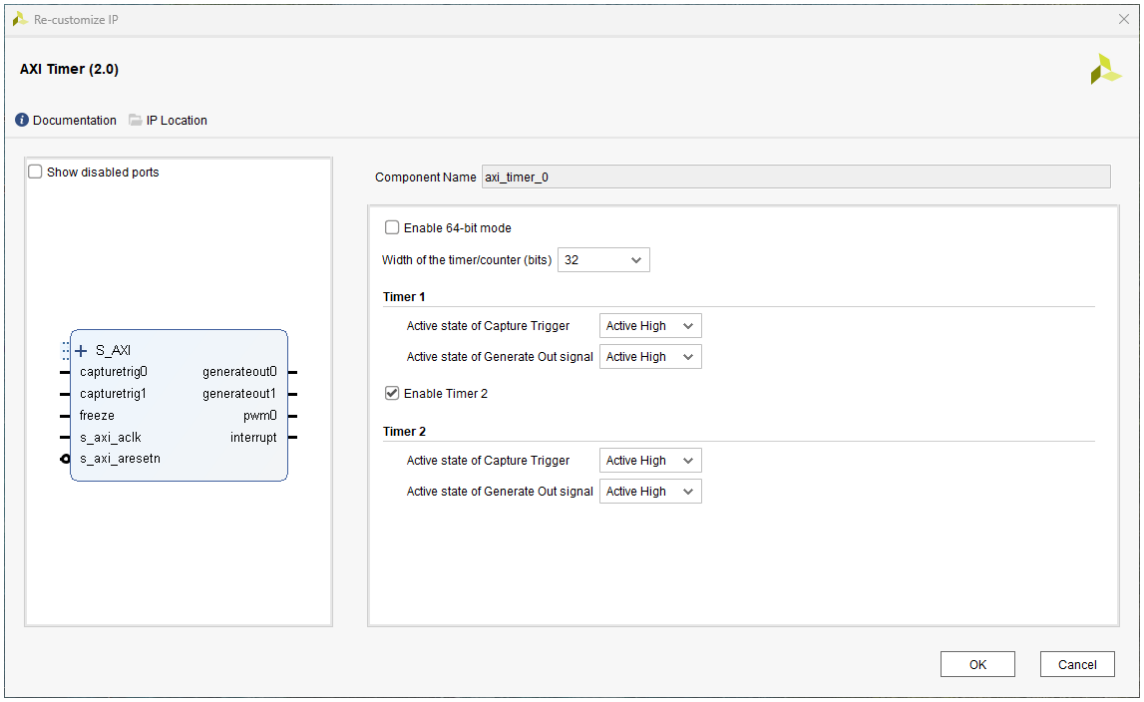
4. Select **AXI Timer** from the dropdown menu.



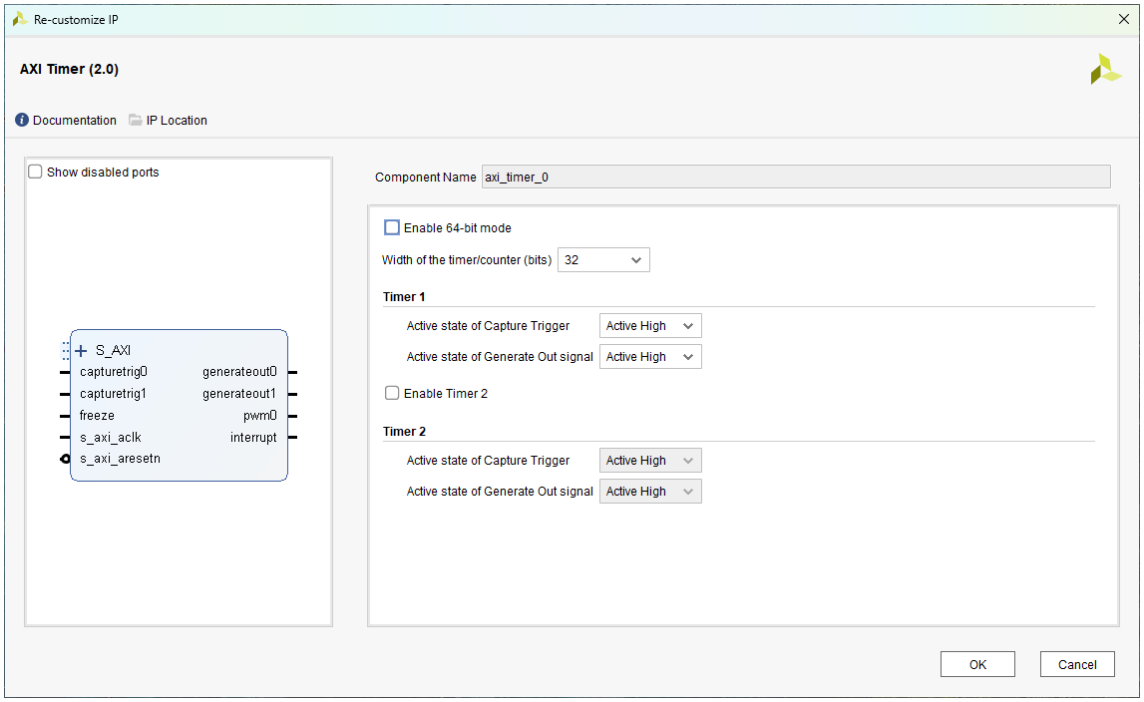
5. Right-click the new module.



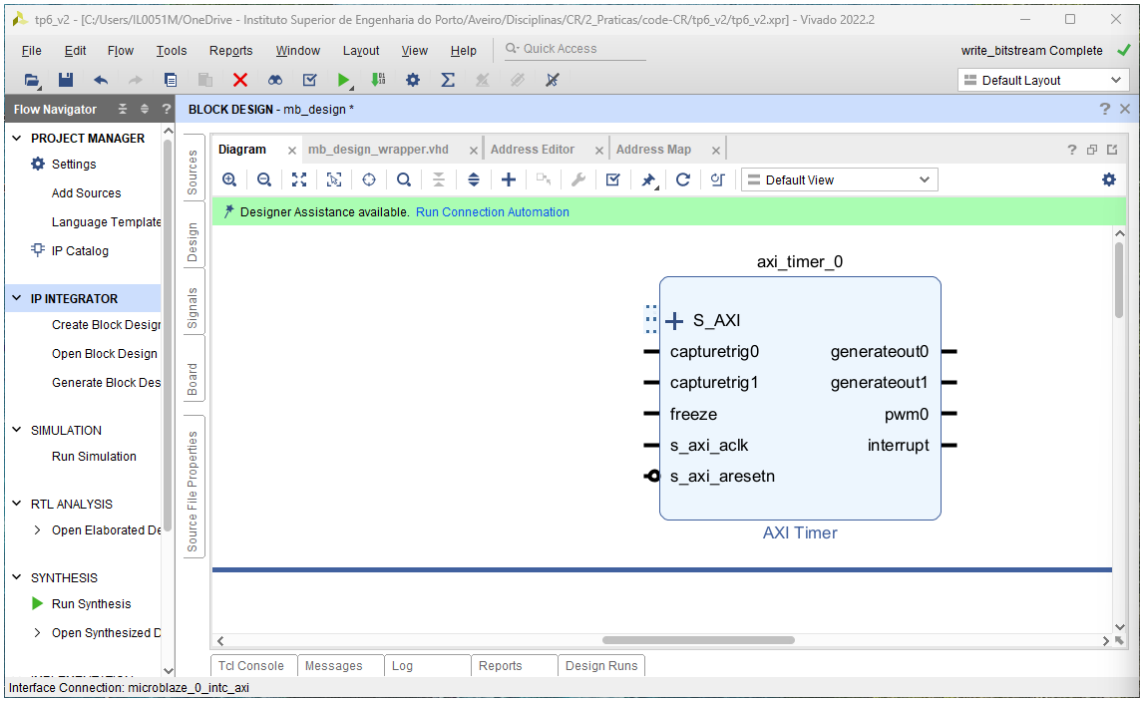
6. The following window shows up.



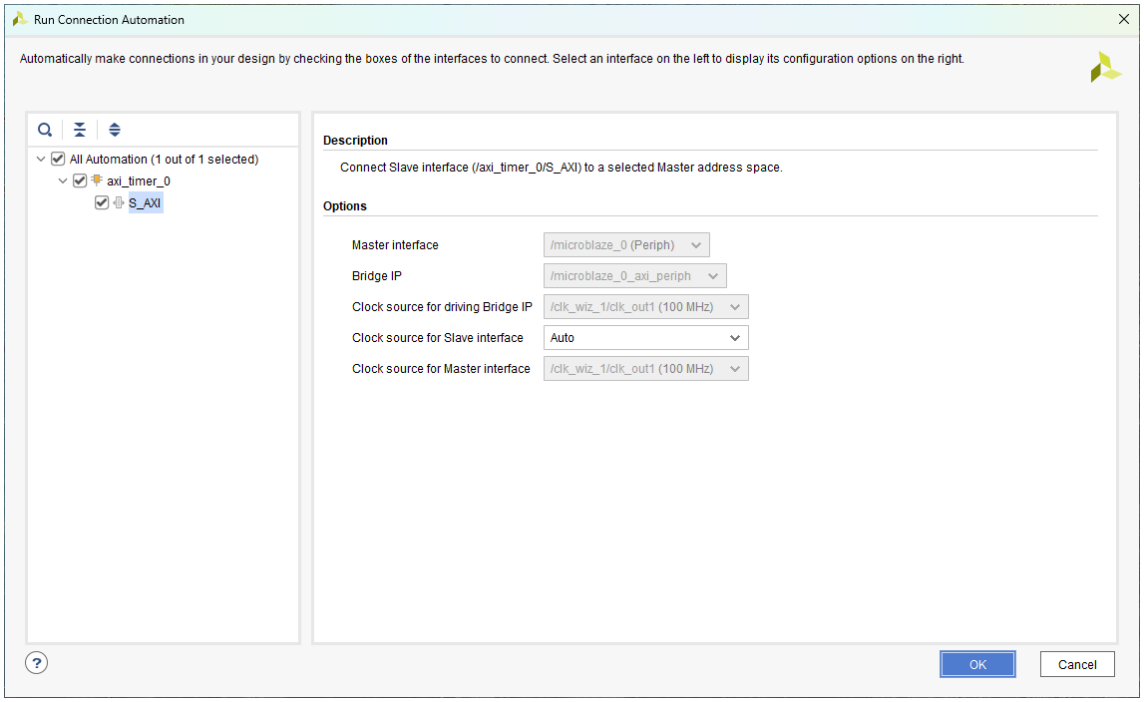
7. Tick off the box **Enable Timer 2**. Click OK to exit the window.



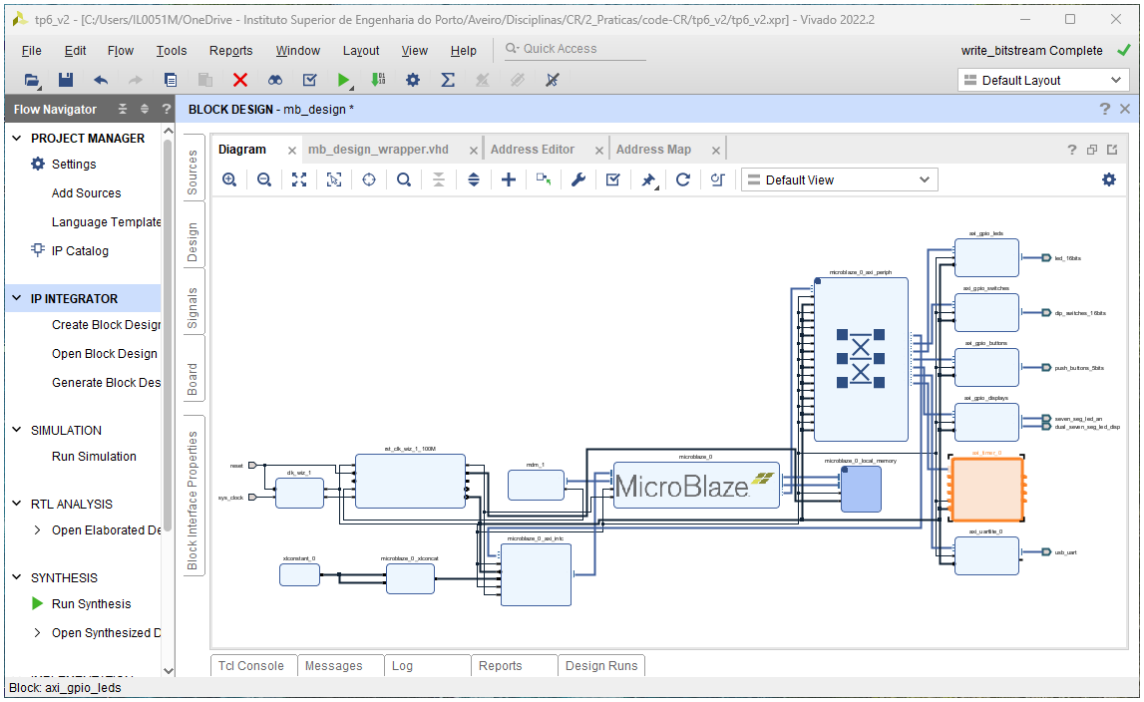
8. Click the **Run Connection Automation** button.



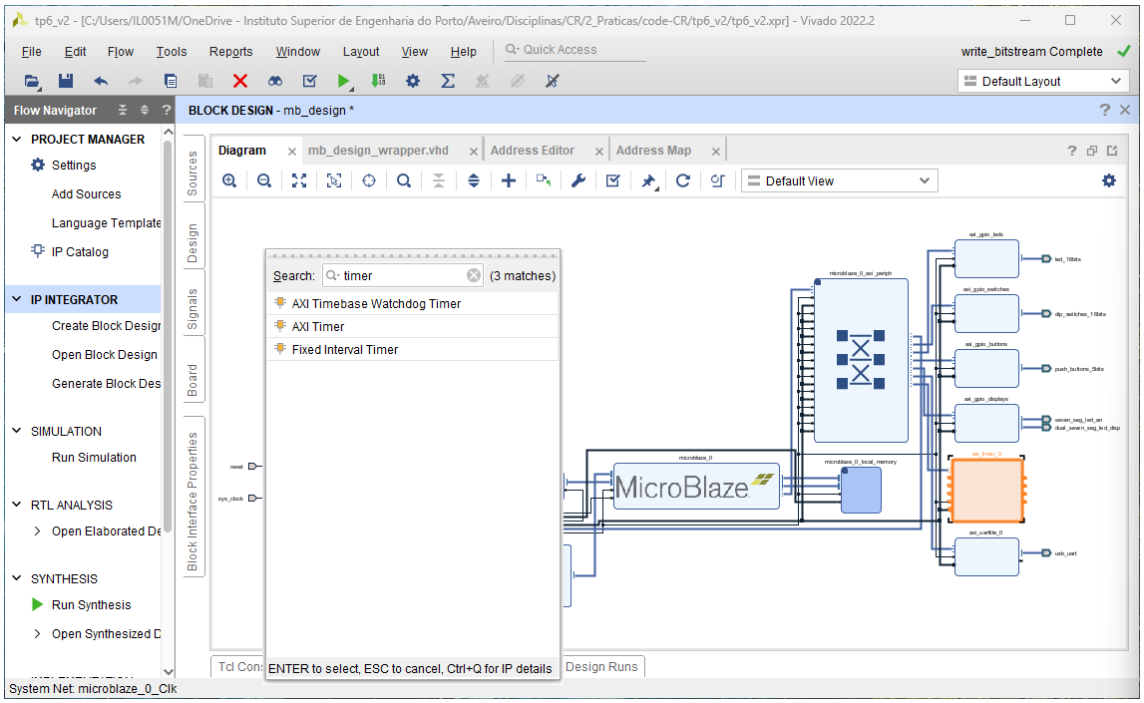
9. Click **OK**.



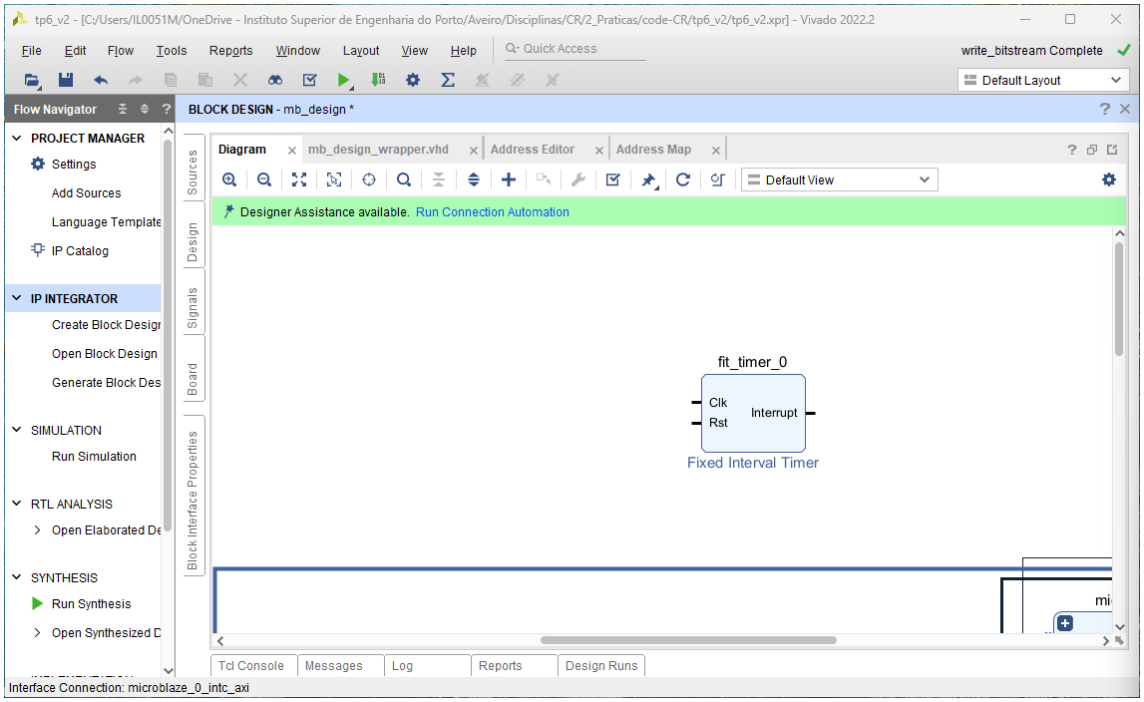
10. Click **Regenerate Layout** (optional).



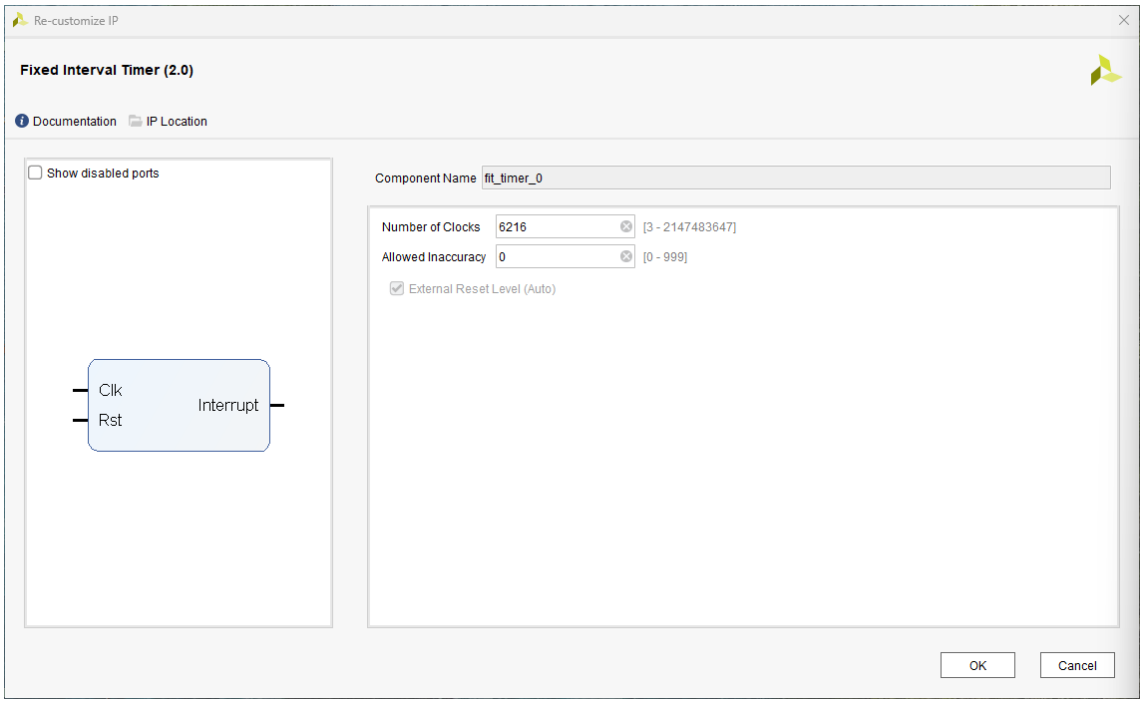
11. Click on the **+** sign to add a new block. Search for *timer*. Add a **Fixed Interval Timer** module.



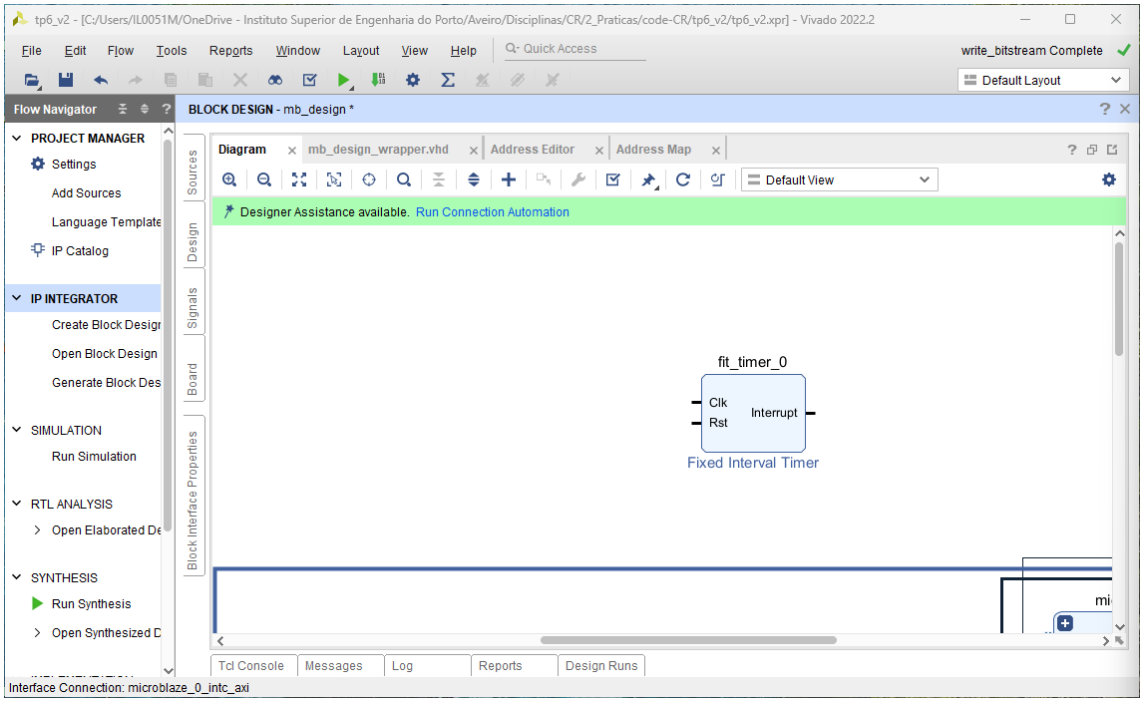
12. Right-click the new module.



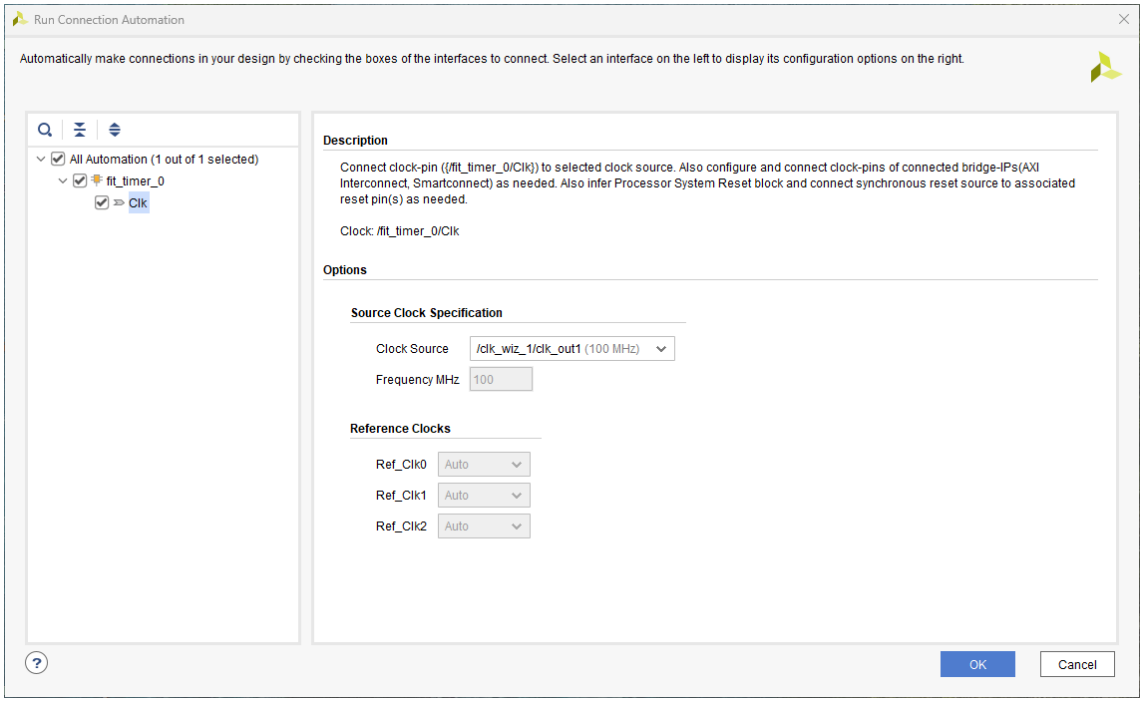
13. The number of clock cycles to wait before an interrupt is issued can be changed here. You can leave as is for now.



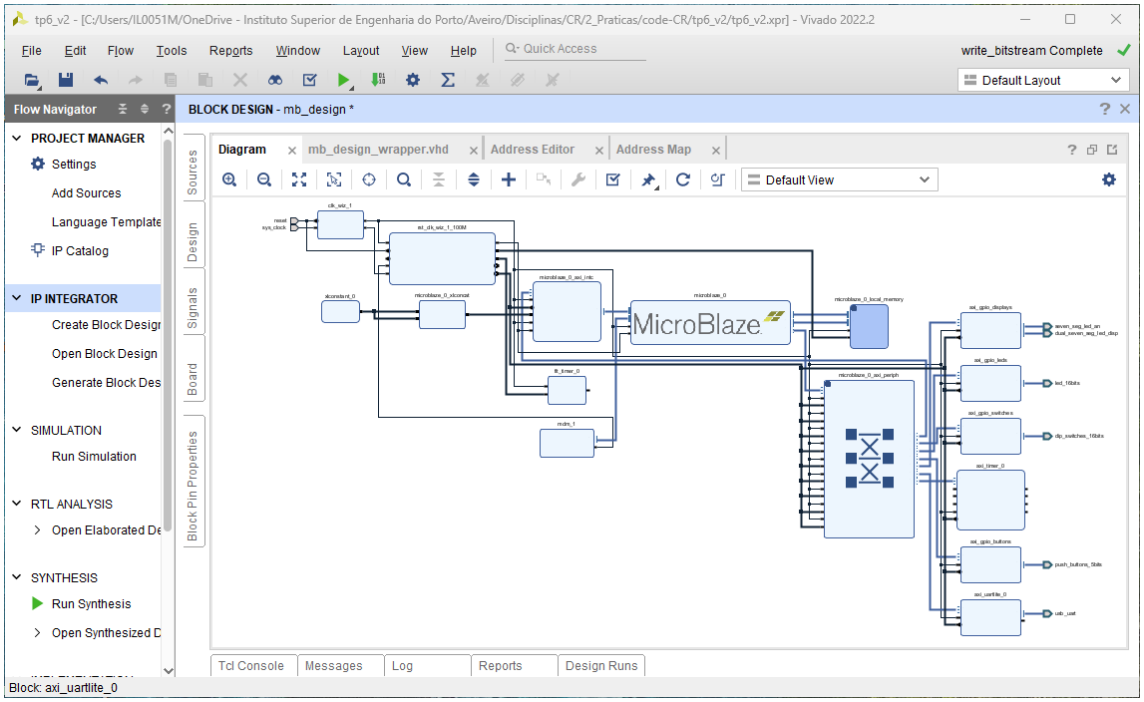
14. Click the **Run Connection Automation** button.



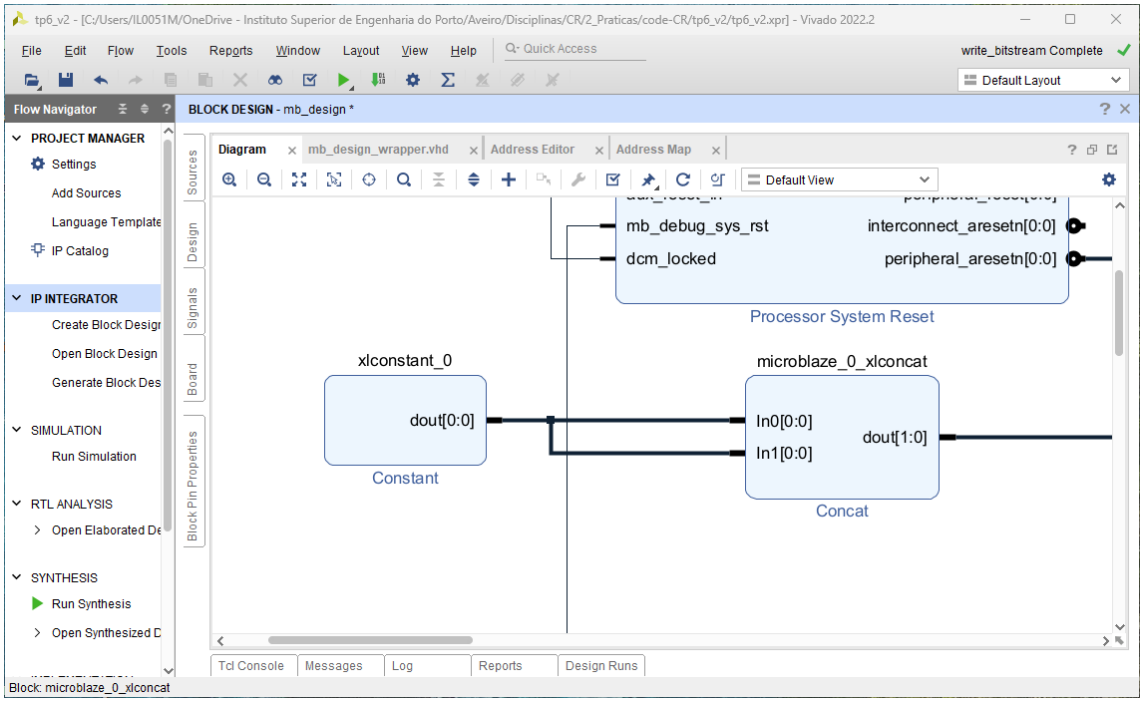
15. Click **OK**.



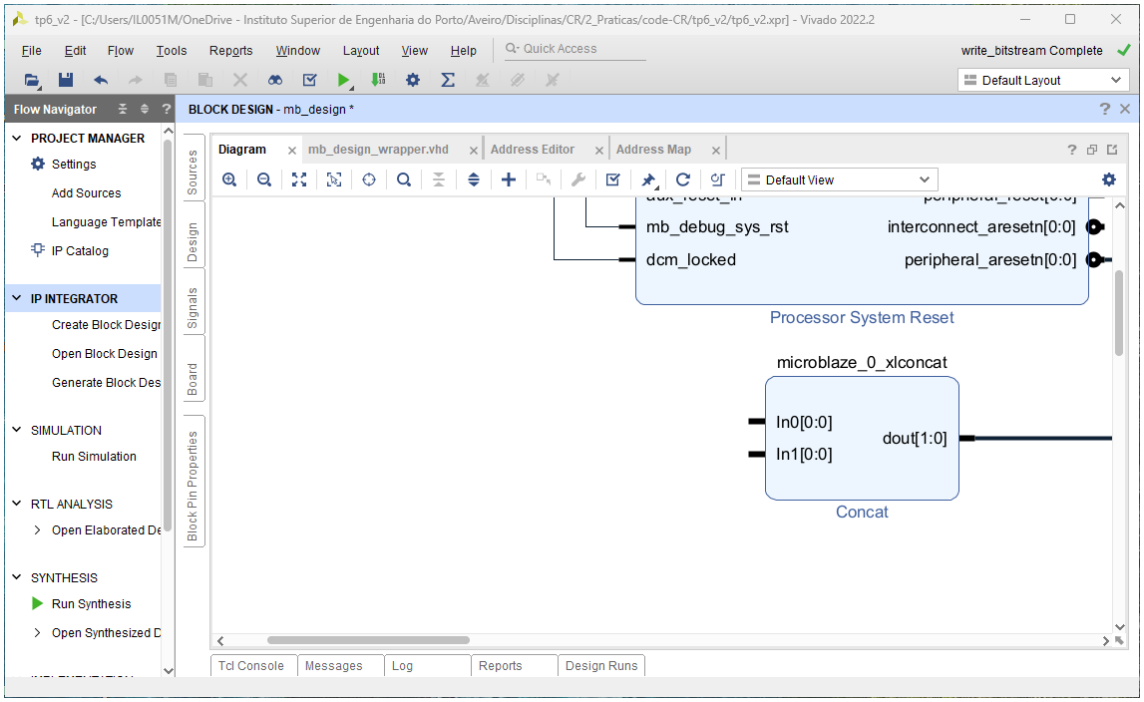
16. Click **Regenerate Layout** (optional).



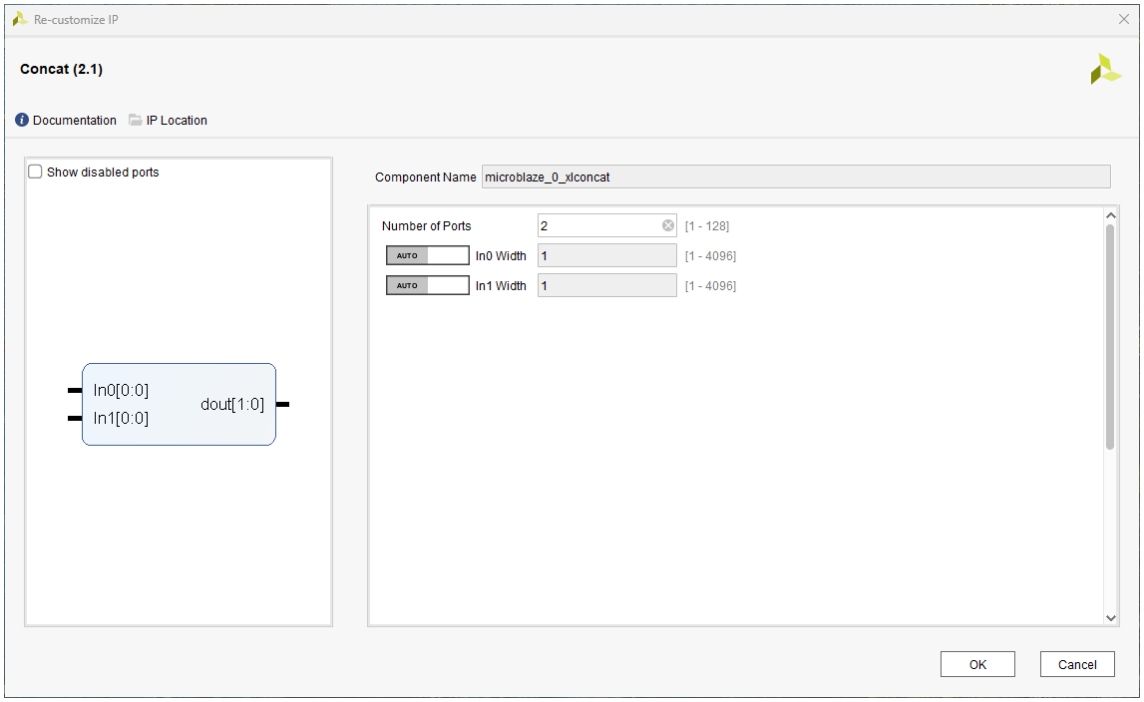
17. Navigate to the **xlconcat** and **xlconstant** modules



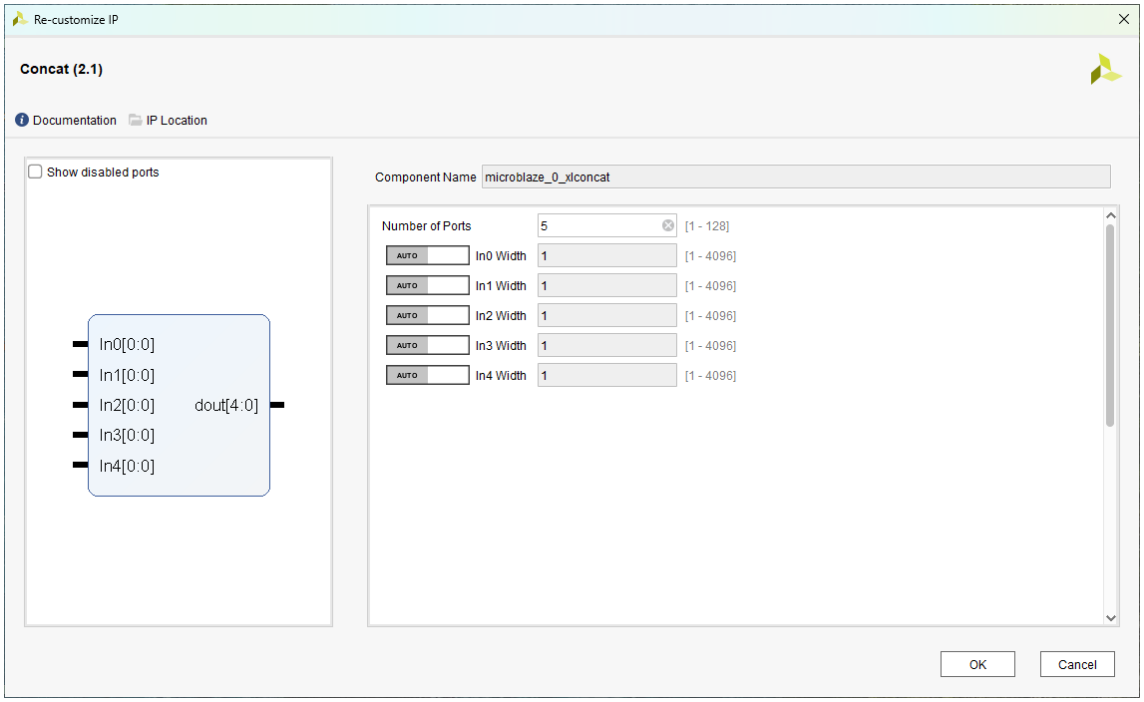
18. Delete the **xlconstant** module. Right-click the **xlconcat** module.



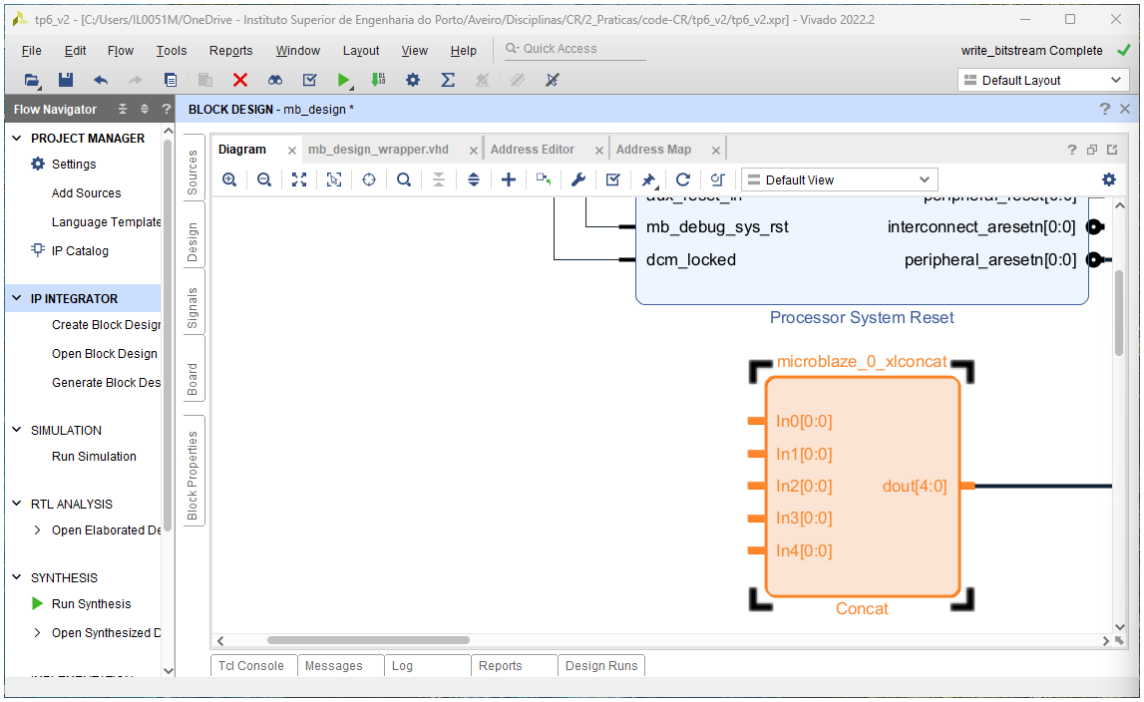
19. Right-click the **xlconcat** module.



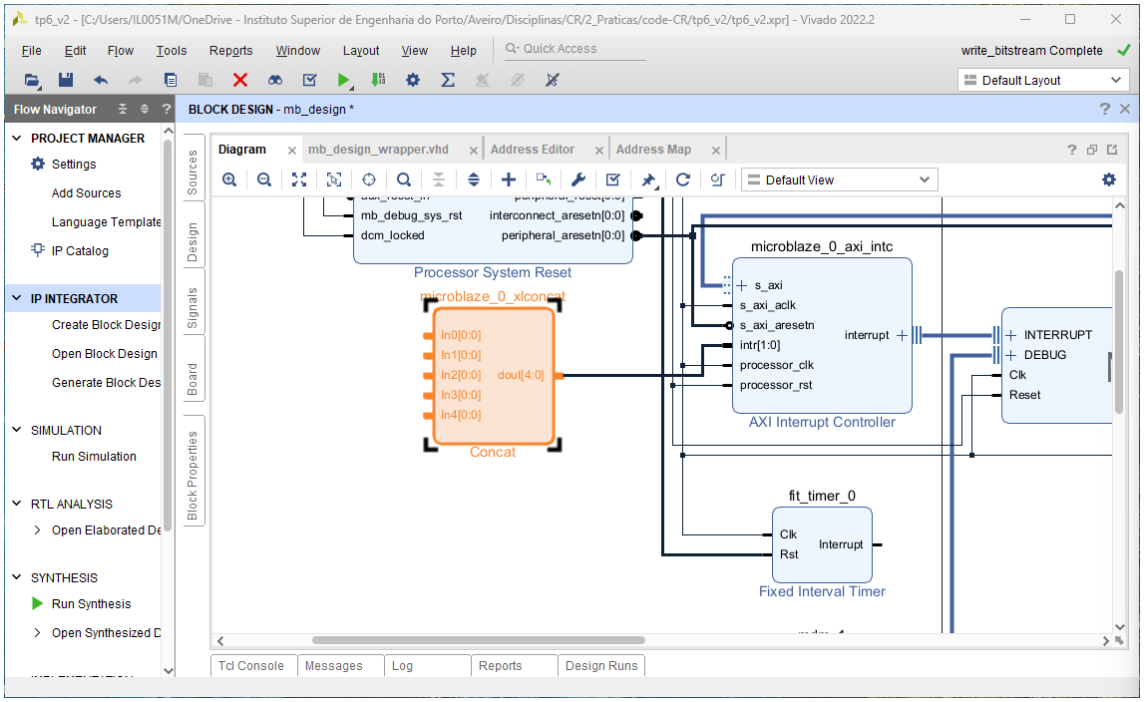
20. Change the value Number of Ports from 2 to 5. Click **OK**.



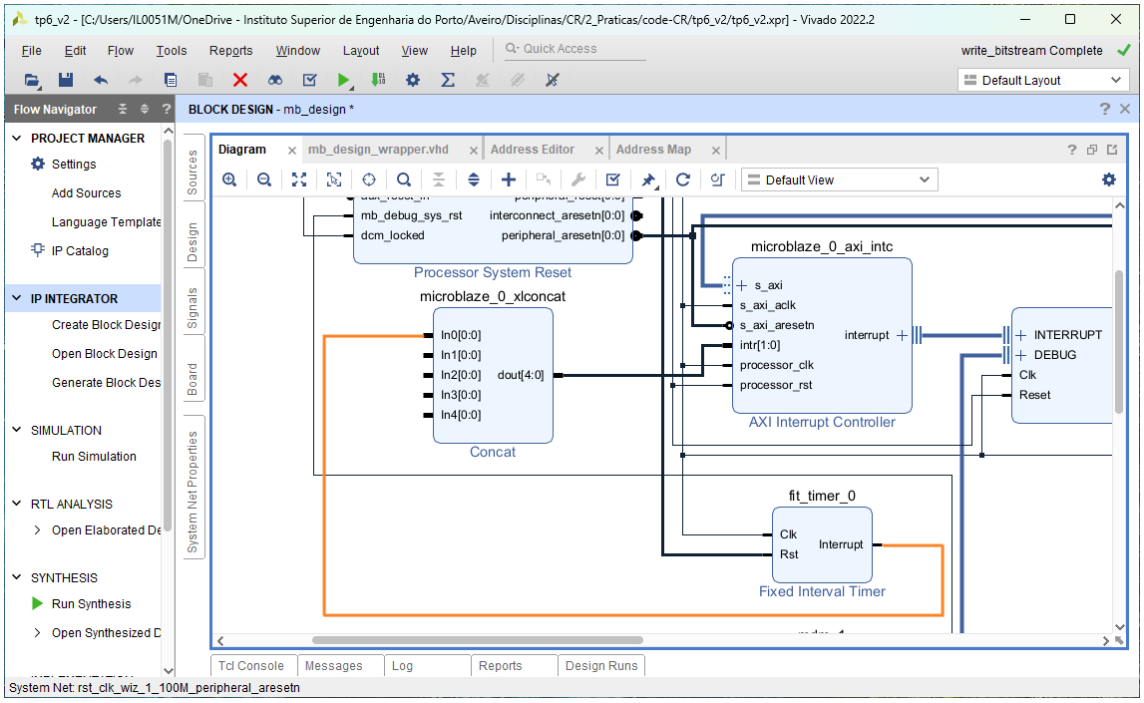
21. The module is updated as shown.



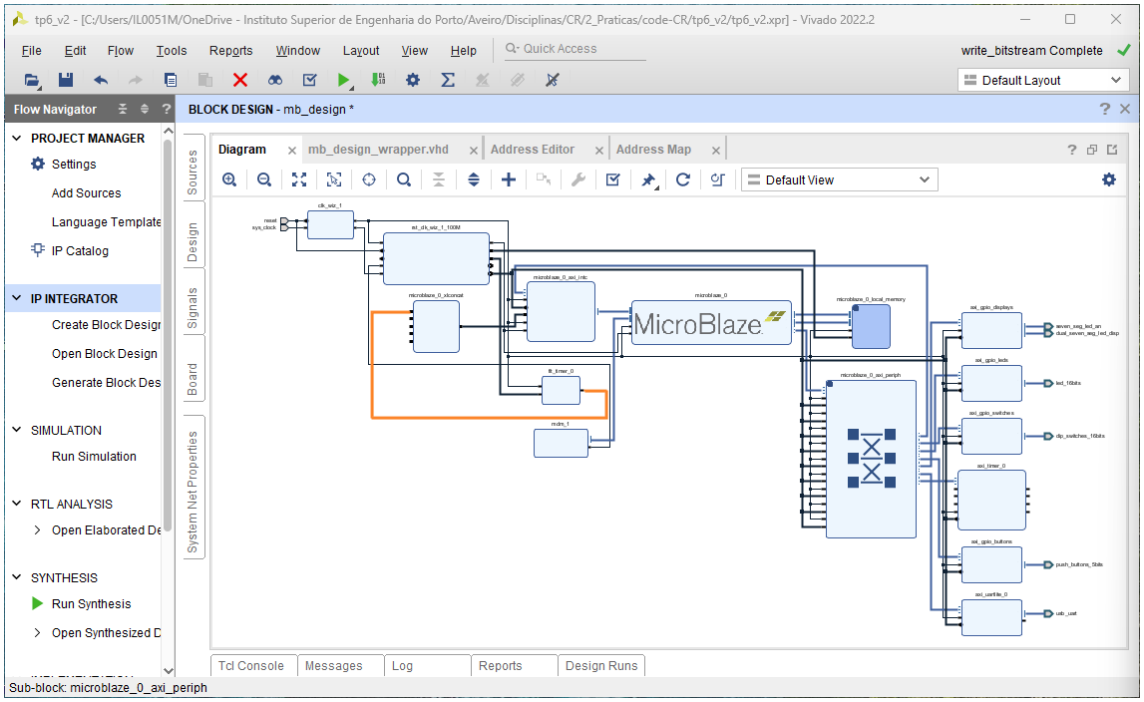
22. Zoom out to have the **xlconcat** and **fit_timer** modules in sight.



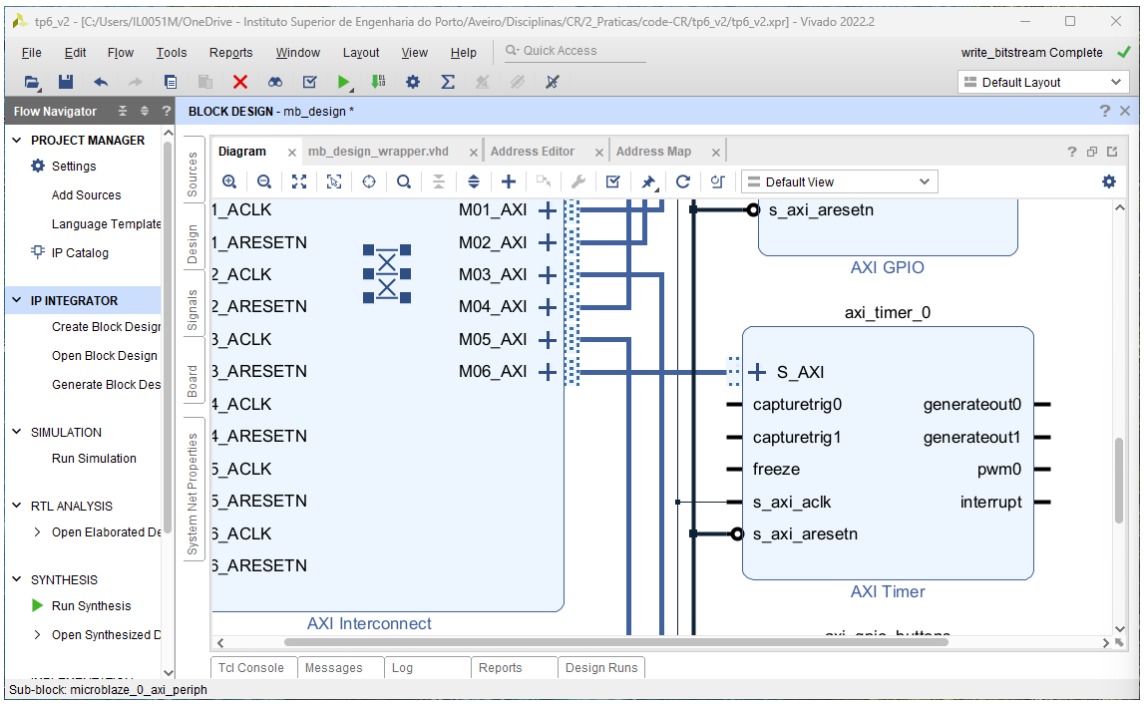
23. Connect the **interrupt** port of the **fit_timer** to port **In0** of the **xlconcat** module.



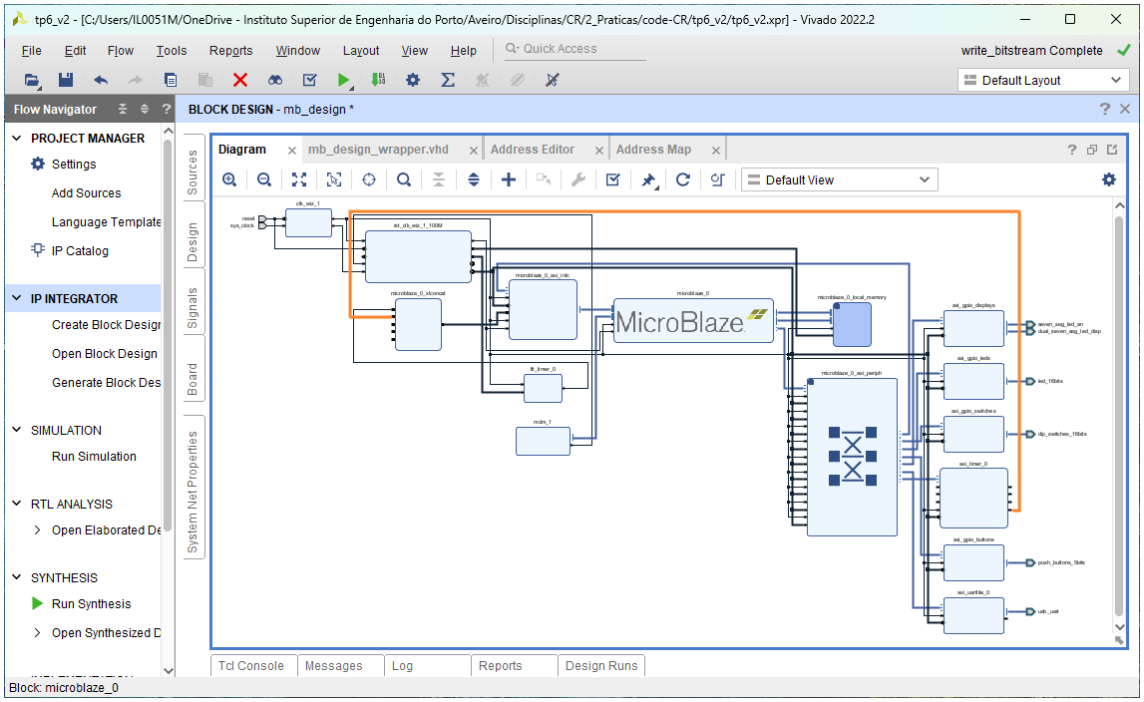
24. Zoom out completely.



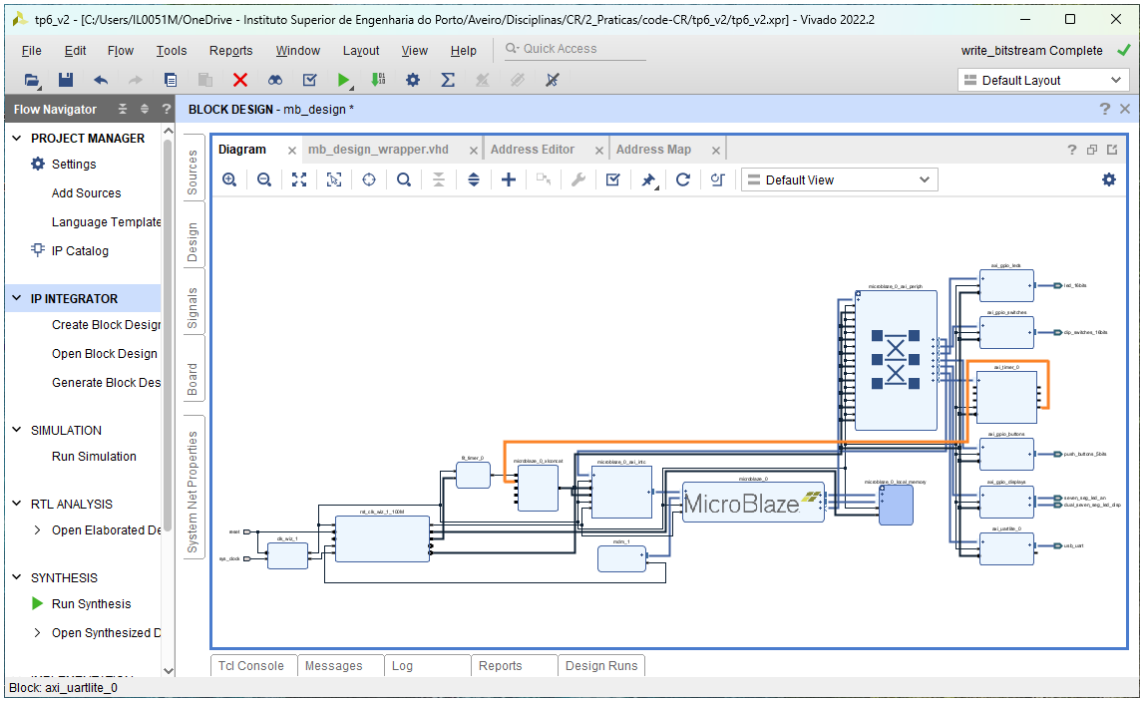
25. Identify the location of the **axi_timer** module. Zoom out completely again.



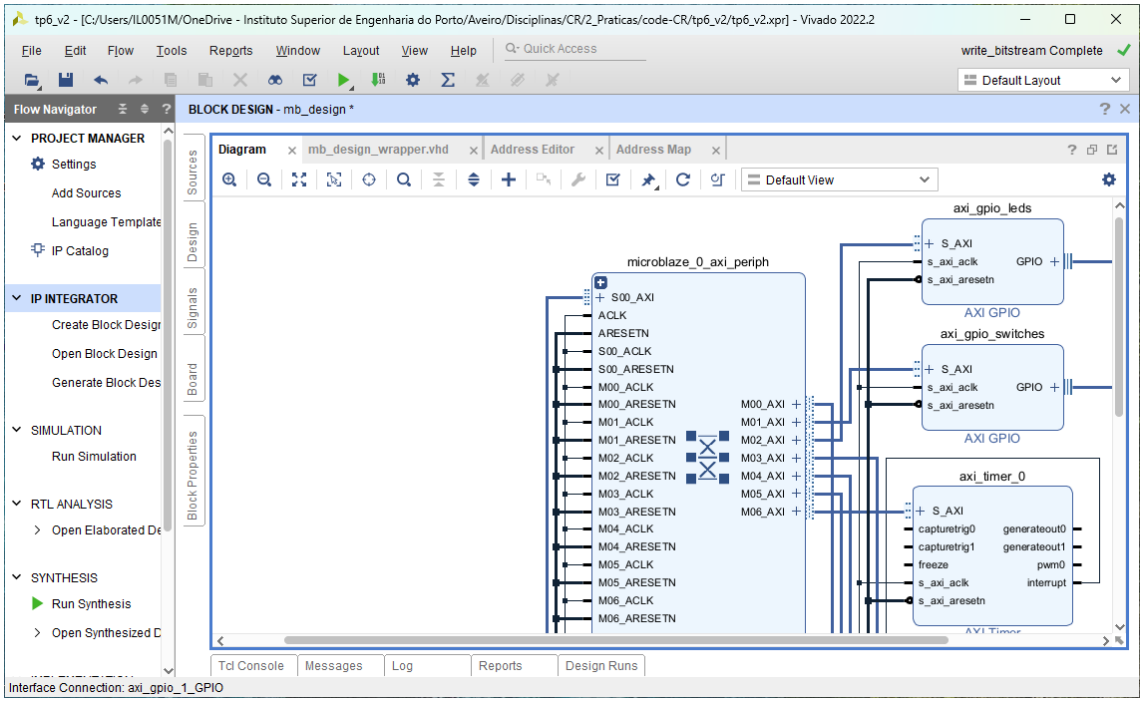
26. Connect the **interrupt** port of the **axi_timer** to port **In1** of the **xlconcat** module.



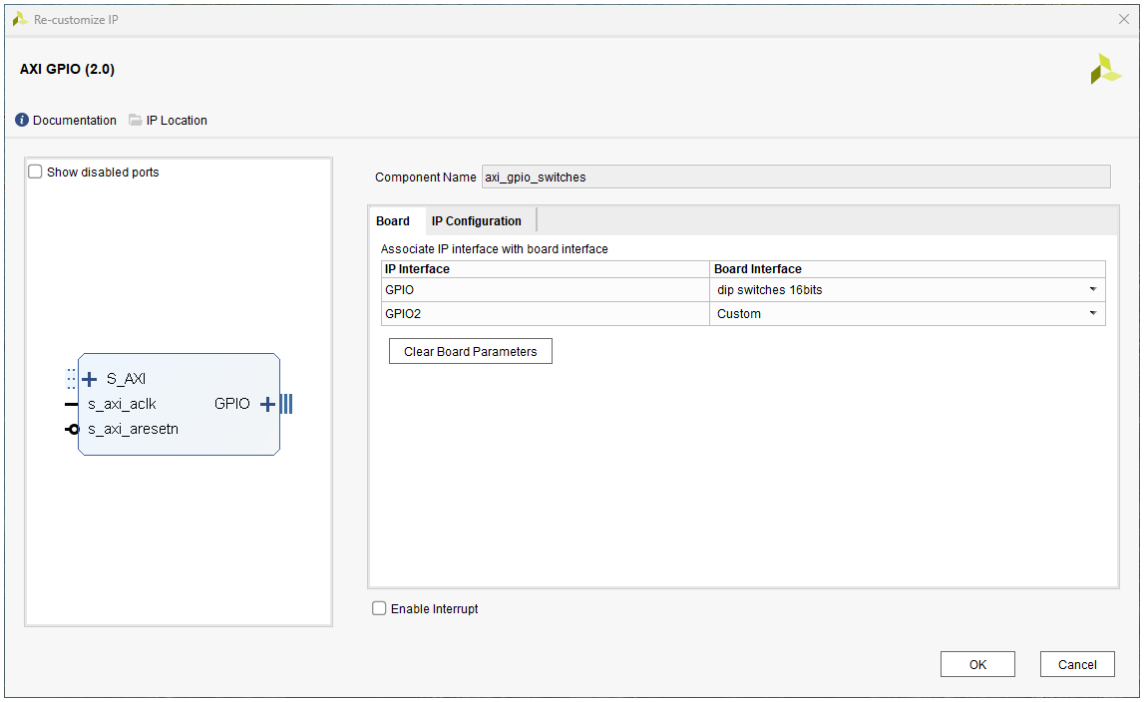
27. Click **Regenerate Layout** (optional).



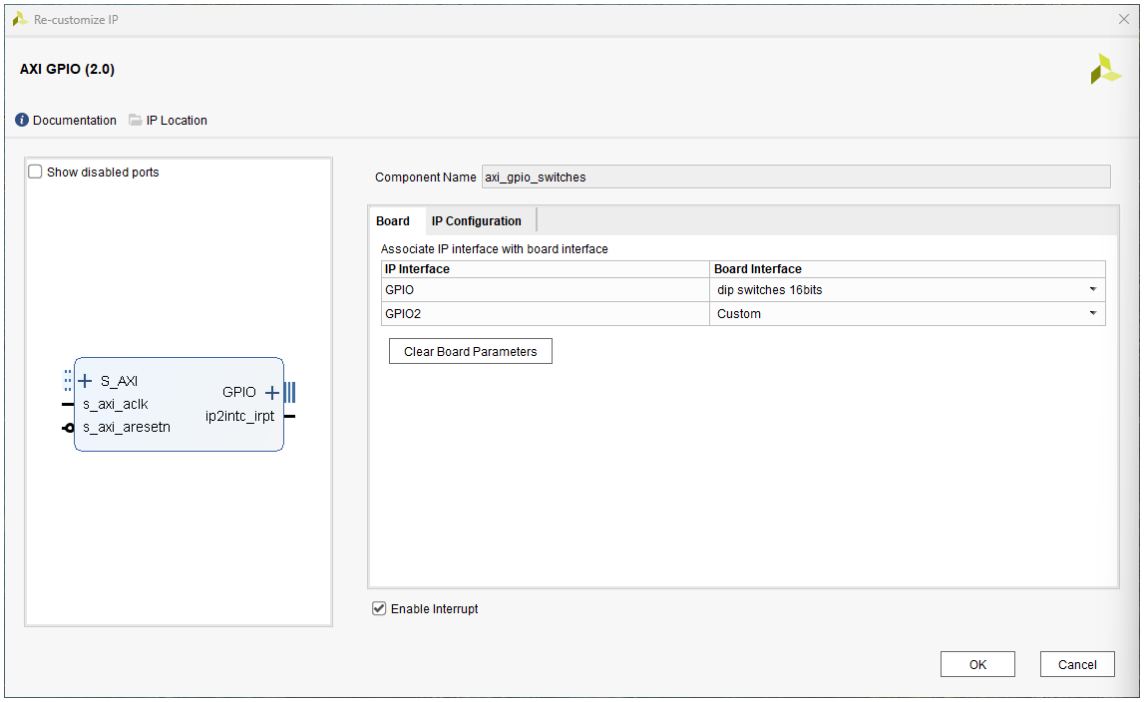
28. Right-click on the **axi_gpio_switches** module.



29. A window pops up.

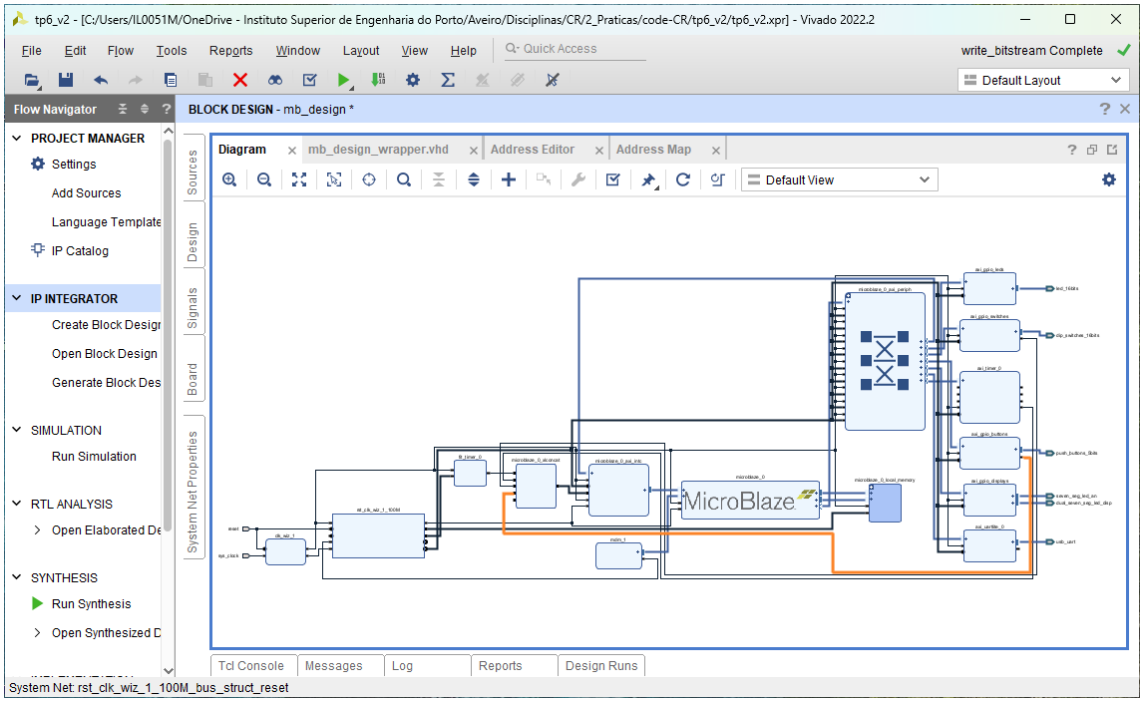


30. Tick the **Enable Interrupt** box. Click **OK**.

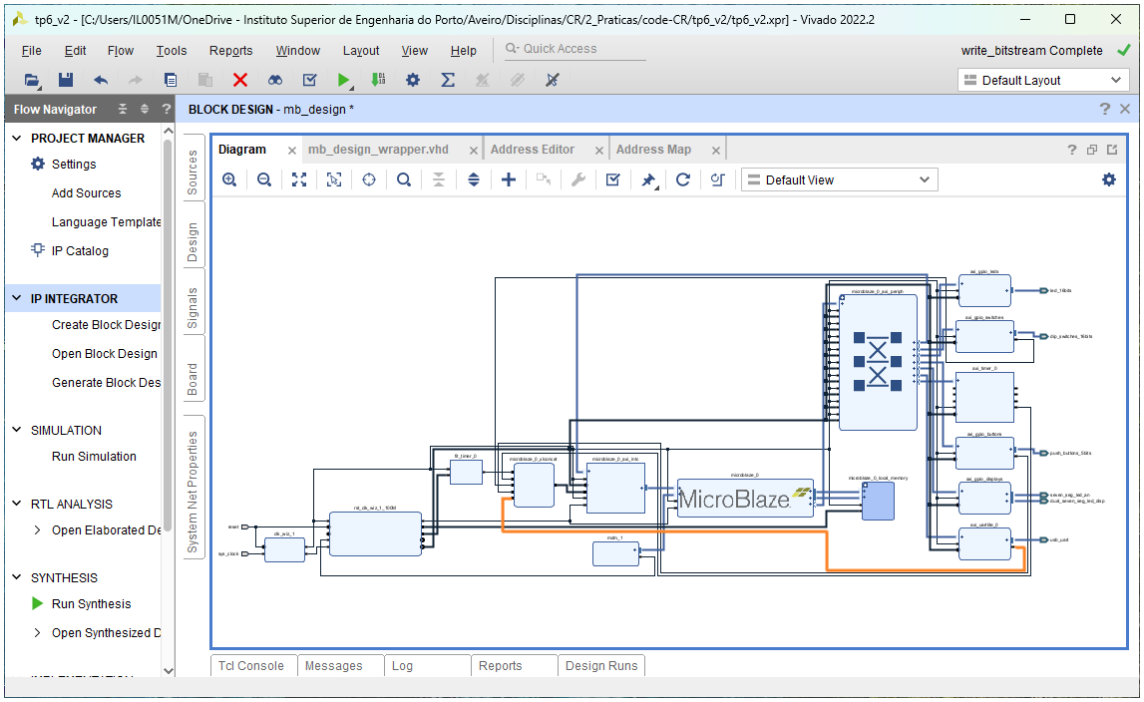


31. Repeat the process for the **axi_gpio_buttons** module.

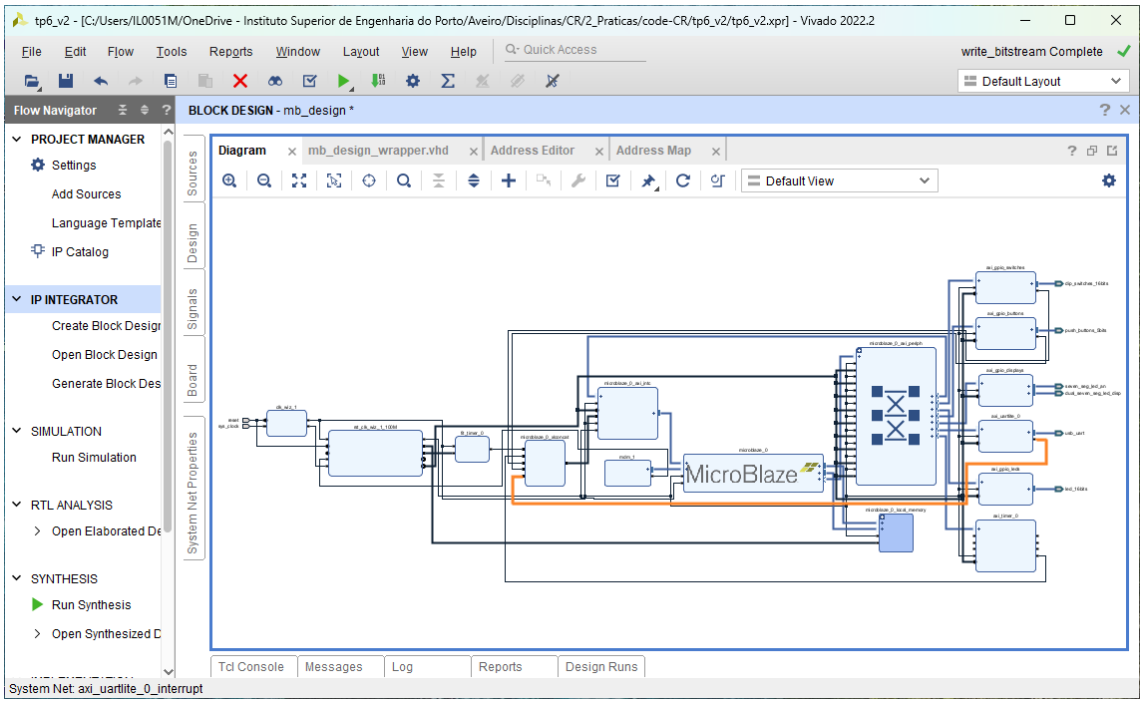
32. Connect the **interrupt** port of the **axi_gpio_switches** and **axi_gpio_buttons** to ports **In2 and In3** of the **xlconcat** module.



33. Connect the **interrupt** port of the **axi_uartlite** to ports **In4** of the **xlconcat** module.



34. Click **Regenerate Layout** (optional).



35. Click on **Validate Design.**

36. Generate Output Products (**'Global'** option should be selected)**.**

37. Create HDL Wrapper.

38. Generate Bitstream.

Congratulations!

Sources: AMD Xilinx documentation.