GLASGOW COLLEGE UESTC

Exam paper

Microelectronic Systems (UESTC1008)

Date: 24th June 2019
Time: 14:30-16:30pm

Attempt all PARTS. Total 100 marks

Use one answer sheet for each of the questions in this exam.
Show all work on the answer sheet.

Make sure that your University of Glasgow and UESTC Student Identification Numbers are on all answer sheets.

An electronic calculator may be used provided that it does not allow text storage or display, or graphical display.

All graphs should be clearly labelled and sufficiently large so that all elements are easy to read.

The numbers in square brackets in the right-hand margin indicate the marks allotted to the part of the question against which the mark is shown. These marks are for guidance only.

DATA/FORMULAE SHEET IS PROVIDED AT THE END OF PAPER

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Q1 (a) The below code will generate a waveform

```
1. #include "mbed.h"
2. PwmOut led(LED1);
3. int main() {
4.     led.period(4.0f);
5.     led.write(0.50f);
6.     while(1);
7. }
```

(i) What will be the duty cycle of this waveform? [2 marks]

(ii) Draw the shape of the waveform that will be output by the mbed by properly labelling the time period of the waveform? [3 marks]

(iii) Explain the purpose of each line in the code. [10 marks]

(b) Memory architectures:

(i) What are the two different type of memory architectures used in microcomputers [2 marks]

(ii) Sketch a diagram of each of the two memory architectures [5 marks]

(iii) Explain the difference between the two memory architectures [3 Marks]

Q2 (a) A green LED, which drops 2.1 V when current is flowing through it, is connected to the DigitalOut pin of a mbed microcontroller. The battery life of the system is to be increased by limiting the current flowing through the LED to 2mA using a series connected resistor. For an mbed with 3.6 V output voltage, what value of series resistor is required? [5 marks]

(b) Determine the truth table for the circuit configuration shown in Fig Q2b in which MA and MB are NMOS switches connected to input A and B respectively while ML is

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working as load transistor. The truth table should have inputs A & B and output Vo.

[10 marks]

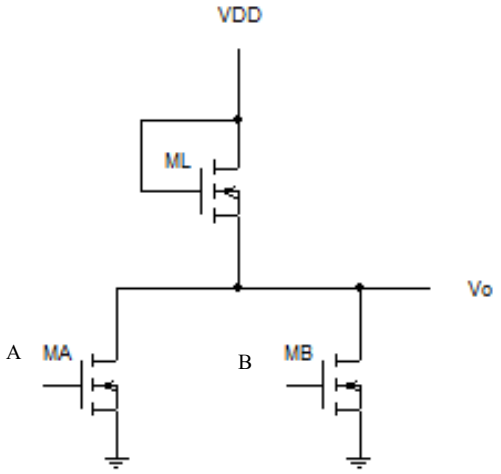

Fig Q2b

(c) A bit sequence 010111010011 is given at the input of a 3-bit Digital to Analog Converter (DAC) whose reference voltage Vr is 3.3 V.

(i) Calculate the analog output voltage Vo for input 111. [2 marks]

(ii) Assuming one DAC conversion takes 2µs. How long will it take to convert the whole bit sequence? [3 marks]

(iii) For a controller with 40 MHz clock speed, how many clock cycles would be required for the whole conversion? [5 marks]

Q3 (a) For the Boolean function

$$F = xy'z + x'y'z + w'xy + wx'y + wxy$$

(i) Draw the truth table of F. [5 marks]

(ii) Draw the logic diagram using the original Boolean expression. [5 marks]

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(b) Write a Boolean expression and construct the truth table for the logic diagram of Fig Q3b: [10 marks]

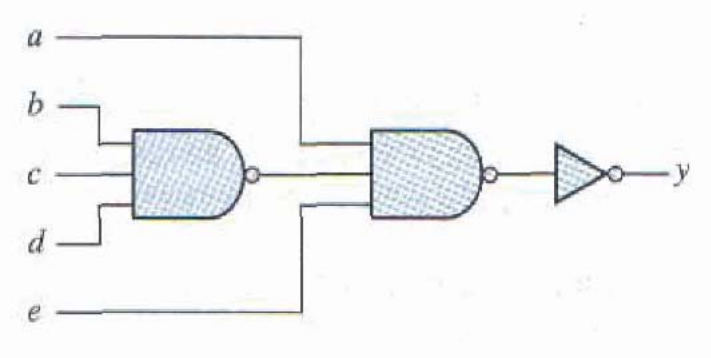

Fig Q3b

(c) Using block diagrams, sketch a 16x1 multiplexer which is created from two 8x1 and one 2x1 multiplexers. [5 marks]

Q4 (a) What is the difference between a sequential logic and a combinational logic circuit? [5 marks]

(b) Why are clocks used in latches? [5 marks]

(c) Redraw Fig Q4c2 below and add the outputs Q1, Q2 and Q3 from the circuit of Fig Q4c1 . Assume the circuit clock operates at the rising edge and that all Q outputs are initialized as 1. [15 marks]

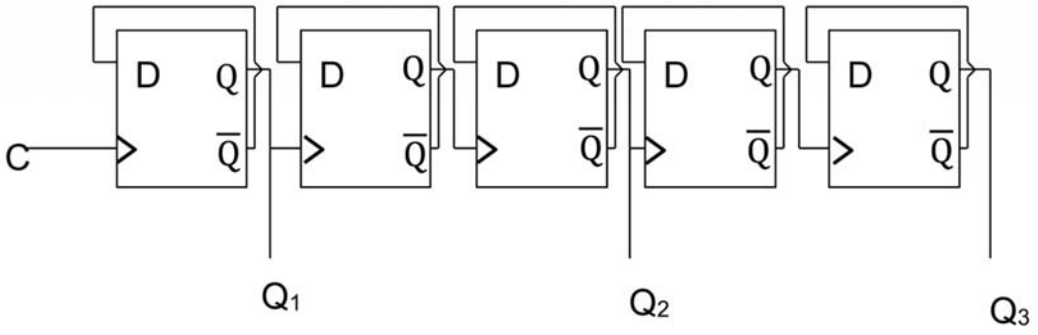

Fig Q4c1

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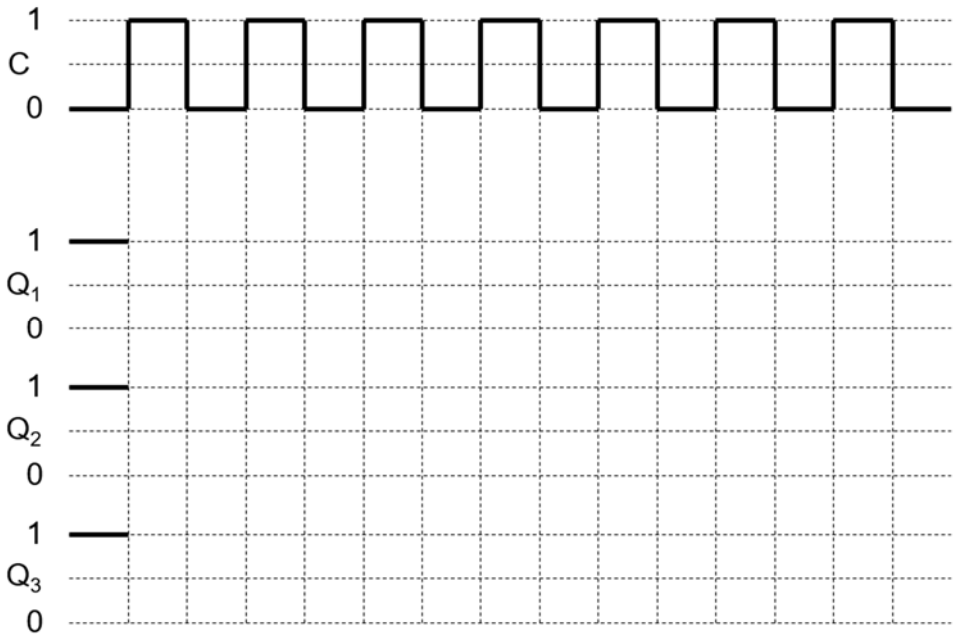

Fig Q4c2

End of question paper