GLASGOW COLLEGE UESTC

Final Exam paper

DIGITAL CIRCUIT DESIGN (UESTC3020)

Date: 2 January, 2020
Time: 09:30 – 11:30am

Attempt all PARTS. Total 100 marks

Use one answer sheet for each of the questions in this exam.
Show all work on the answer sheet.

Make sure that your University of Glasgow and UESTC Student Identification Numbers are on all answer sheets.

An electronic calculator may be used provided that it does not allow text storage or display, or graphical display.

All graphs should be clearly labelled and sufficiently large so that all elements are easy to read.

The numbers in square brackets in the right-hand margin indicate the marks allotted to the part of the question against which the mark is shown. These marks are for guidance only.

Continued overleaf

Q1 (a) Figure Q1a is an example of a VHDL structural architecture.

```
architecture MY_STRUCT of COMB_LOGIC is
signal C1, C2: STD_LOGIC;

component AND port(I0,I1:in STD_LOGIC; O:out STD_LOGIC);
end component;
component OR port(I0,I1:in STD_LOGIC; O:out STD_LOGIC);
end component;
component NOR port(I0:in STD_LOGIC; O:out STD_LOGIC);
end component;

begin
    U1: AND port map (A(1), A(0), C1);
    U2: OR port map (A(3), A(2), C2);
    U3: NOR port map (C1, C2, B);
end COMB_LOGIC;
```

Figure Q1a.

(i) Write down the VHDL entity associated with the architecture of Figure Q1a. [4]

(ii) Write down a behavioural VHDL architecture which performs the same function as the structural architecture of figure Q1a. [6]

(iii) Explain the main differences between behavioural architecture and structural architecture. [5]

(b) A simple Field Programmable Gate Array is built from a 'North-South-East-West' mesh connected array of Configurable Logic Blocks described in Figure Q1b. We wish to design a circuit which divides the clock frequency by two, and outputs this to the South of the most South-Westerly block of the design.

(i) Sketch the design of a ÷2 circuit using D-type flip-flop. [5]

(ii) How many Configurable Logic Blocks are required in total to carry out the logic functions and information routing functions of the ÷2 circuit? Give reasons for your answer. [5]

Continued overleaf

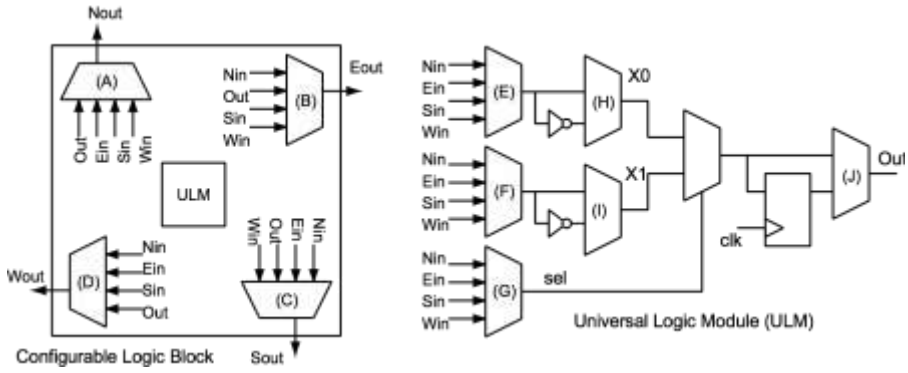

Figure Q1b.

Q2 (a) A student is required to design a DRAM chip with word size of 4 bits, with row and column address decoders limited to 6 input bits.

(i) What is the largest memory chip that the student can design under these restrictions? [4]

(ii) How many decoder NAND gates does the student's design save over one which uses a single large address decoder? [5]

(iii) What are the advantages and disadvantages of using DRAM compared to using SRAM? [6]

(b) Memory with read timing parameters described by Figure Q2b is used as part of a synchronous system, with input being fed directly from the outputs of registers with t_{pd} = 5 ns (rising clock edge to stable output) and outputs being fed to a register with setup and hold times of t_s = 3ns and t_h = 2ns respectively.

State the maximum clock frequency at which it can be driven. [7]

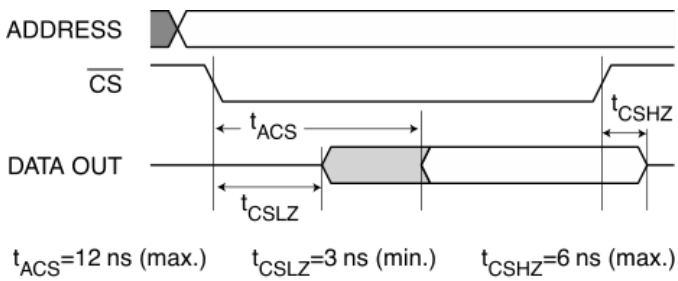

Figure Q2b.

Continued overleaf

(c) Describe the benefit of using VHDL in the design of large-scale digital systems. [3]

Q3 (a) Implement the following Boolean function F, together with the don't-care conditions d, using no more than two NOR gates: [9]

$F(A, B, C, D) = \sum(2, 4, 10, 12, 14)$
$d(A, B, C, D) = \sum(0, 1, 5, 8)$

Assume that both the normal and complement inputs are available.

(b) List the eight degenerate two-level forms and show that they reduce to a single operation.
Explain how the degenerate two-level forms can be used to extend the number of inputs to a gate. [16]

Q4 Design a sequential circuit with two D flip-flops A and B, and one input *x_in*

(a) When x_in = 0, the state of the circuit remains the same. When x_in = 1, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00, and repeats. [13]

(b) When x_in = 0, the state of the circuit remains the same. When x_in =1, the circuit goes through the state transitions from 00 to 11, to 01, to 10, back to 00, and repeats. [12]

End of question paper