GLASGOW COLLEGE UESTC

Exam

Digital Circuit Design (UESTC3020)

Date: Dec.23rd, 2021
Time: 9:30-11:30am

Attempt all PARTS. Total 100 marks

Use one answer sheet for each of the questions in this exam.
Show all work on the answer sheet.

Make sure that your University of Glasgow and UESTC Student Identification Numbers are on all answer sheets.

An electronic calculator may be used provided that it does not allow text storage or display, or graphical display.

All graphs should be clearly labelled and sufficiently large so that all elements are easy to read.

The numbers in square brackets in the right-hand margin indicate the marks allotted to the part of the question against which the mark is shown. These marks are for guidance only.

Continued overleaf

Q1 (a) In this question, you are tasked with designing a combinational circuit implementing an Excess-3 code.

Reminder on Excess-3: consider a 4-bit input, abcd, the 4-bit output, wxyz is calculated by adding 3 in binary (0011) to the input abcd.

(i) Calculate the truth table of the Excess-3 combinational circuit. [3]

(ii) Minimize each output function using k-maps. [6]

(iii) Implement the output functions using a PROM. [4]

(iv) Implement the output functions using 8-to-1 multiplexers. [6]

(b) Consider the VHDL code presented in figure Q1 and answer the following questions.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

library UNISIM;
use UNISIM.VComponents.all;

entity Question1 is
  Port ( x : in STD_LOGIC;
       A : inout STD_LOGIC :='1';
       B : in STD_LOGIC;
       CLK : in STD_LOGIC);
end Question1;

architecture Behavioral of Question1 is
signal C0, C1: std_logic;

component FD
  port (Q: out std_logic; D, C: in std_logic);
end component;
component AND2
  port (O: out std_logic; I0, I1: in std_logic);
end component;
component OR2
  port (O: out std_logic; I0, I1: in std_logic);
end component;

begin
  GAND0: AND2 port map (O => C0, I0 => A, I1 => x);
  GOR0: OR2 port map (O => C1, I0 => C0, I1 => B);
  DFF0: FD port map (Q => A, D => C1, C => CLK);
end Behavioral;
```

Figure Q1.

Continued overleaf

(i) Which VHDL description of the circuit is implemented in this code? Justify your answer. [2]

(ii) List the inputs and outputs of the circuit. [1]

(iii) From the architecture, draw the circuit that is simulated by this VHDL code. [3]

Continued overleaf

Q2 (a) (i) Simplify the following Boolean function *F*, together with the don't-care conditions *d*. [4]

$$\mathrm{F(A, B, C, D)} = \sum \mathrm{m(1,6,9,11,15)}$$

$$\mathrm{d(A, B, C, D)} = \sum \mathrm{m(4,7,12,14)}$$

(ii) Using the minimum Boolean expression found in (i), implement the circuit using 2-input NOR gates. Assume that you have access to the four variables both complemented and not complemented. [4]

The next two questions focus on writing a VHDL description of the NOR gates circuit.

(iv) Write the entity for the 2-input NOR circuit you have found in (ii) [3]

(v) Write the architecture description of the circuit using a data flow description. [5]

(b) Consider the Linear Feedback Shift Register presented in figure Q2.

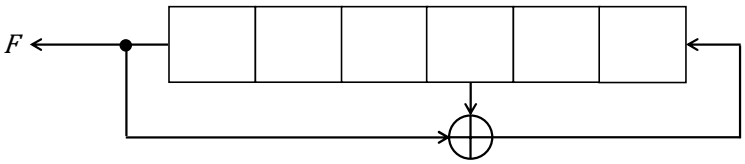

Figure Q2.

(i) Explain, in your own words, what a VHDL *process* is and how it works. [3]

(ii) Write a behavioural description of the circuit in fig Q2 using a process. The initial condition of the shift register is "001110". [6]

Continued overleaf

Q3 (a) In this question, you are tasked with designing a Moore finite state machine that implements a serial subtractor.

(i) Explain the differences between Mealy and Moore machines. [3]

(ii) Derive the states and state diagram of the Moore machine. [3]

(iii) Using the natural binary coding, derive the binary coded state table of the Moore machine. [2]

(iv) Implement the Moore machine using D-type flip-flops. [5]

(b) In this question, you are tasked with designing a synchronous counter that goes through the sequence 0 2 3 4 5 6 and then repeats.

(i) Derive the binary coded state table for a synchronous counter that goes through the sequence above. [2]

(ii) Discuss how to deal with the don't care states to make sure the counter will not enter one of these states or, at minimum, will not be entering a sequence that is not part of the specifications of the counter. [2]

(iii) Implement the counter using JK flip-flops. [8]

Continued overleaf

Q4 (a) Consider the stream cypher presented on figure Q4a. This cypher combines two LFSRs, LFSR1 and LFSR2. The pseudo-sequences from both LFSRs are combined using a XOR gate to generate the final sequence used to encode plain-text data.

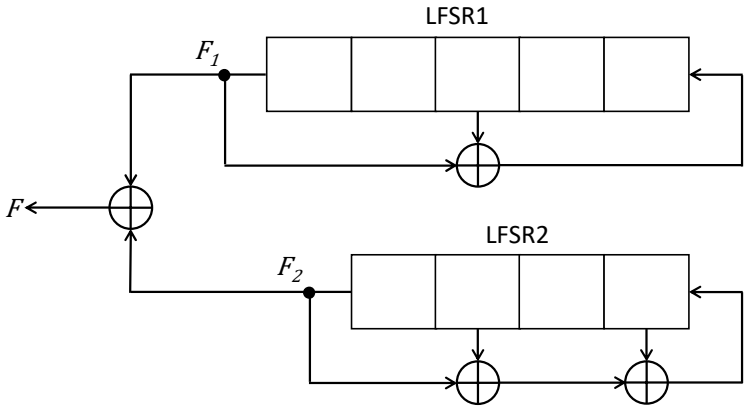

Figure Q4a.

(i) For each LFSR, find the expression of the characteristic polynomial. [2]

(ii) Calculate the output sequence for:

- F1 (output of LFSR1) [2]
- F2 (output of LFSR2) [2]
- F the output of the stream cypher [2]

(b) Explain how a DRAM binary cell works and its advantages compared to an SRAM cell. [5]

(c) Consider the function of six variables implementing a 3-bit half adder. Implement the least significant bit output using 4-input LUT (as available in Spartan 6 FPGA) [5]

(d) Consider the circuit on fig Q4d. The AND gates have a propagation delay of 8ns and the OR gate a propagation delay of 10ns.

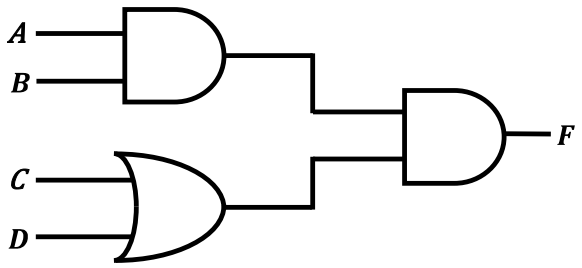

Figure Q4d.

Continued overleaf

At $t = 0ns$, the inputs are: $A = 0$, $B = 1$, $C = 0$, $D = 1$.

At $t = 5ns$, some of the inputs change and are now: $A = 1$, $B = 1$, $C = 0$, $D = 0$.

(i) Find the Boolean expression of the output and calculate the theoretical value of the output for values of inputs at t= 0s and after the change (gate propagation delays are neglected in this part). [2]

(ii) Draw the timing diagram of this circuit for time varying from 0 to 35ns considering the gate propagation delays. [3]

(iii) Explain what problem may appear in this circuit and propose a way to reduce the risk of this problem appearing. [2]

End of question paper