GLASGOW COLLEGE UESTC

Exam

Digital Circuit Design (UESTC3020)

Date: 29th Dec. 2020
Time: 09:30am - 11:30am

Attempt all PARTS. Total 100 marks

Use one answer sheet for each of the questions in this exam.
Show all work on the answer sheet.

Make sure that your University of Glasgow and UESTC Student Identification Numbers are on all answer sheets.

An electronic calculator may be used provided that it does not allow text storage or display, or graphical display.

All graphs should be clearly labelled and sufficiently large so that all elements are easy to read.

The numbers in square brackets in the right-hand margin indicate the marks allotted to the part of the question against which the mark is shown. These marks are for guidance only.

Continued overleaf

Q1 (a) Consider the Boolean function: $F_1(A, B, C, D) = \sum m(0,1,5,6,7,9,13)$

(i) Simplify *F* using a Karnaugh map. [3]

(ii) Implement *F* using only NOR gates. [4]

(iii) Implement *F* using a decoder and an OR gate. [3]

(iv) Implement F using an 8-to-1 multiplexer [4]

(v) Assuming the propagation delays for different gates and circuits are as follow: 5 ns for NOR and OR gates, 8ns for a decoder and 11ns for a 8-by-1 multiplexer, calculate the propagation delay for a change at input A to reach output F, when all other inputs are constant, for circuits designed in (ii), (iii) and (iv). [3]

(vi) If you are asked to implement the Boolean function from this question, which circuit would you choose between the three designed circuits, from (ii), from (iii) and from (iv)? Justify your answer. [4]

(b) In this question, we want to design a digital system that switches on the light and heating system automatically in an office. Three sensors are available: a temperature sensor, a presence sensor and a light sensor.

The temperature sensor output, noted T, is equal to a logic '1' if the temperature in the office is over a set temperature. The presence sensor, represented by a binary variable noted P, is '1' if someone is in the office. The light sensor, associated to a binary variable LS, is equal to '1' if the natural light level if above a given threshold.

The light in the office should be switched on if someone is in the office and the natural light is below the given threshold. The heating system is turned on if someone is in the office and the temperature is below the given set temperature.

(i) Find the Boolean expression to have the light on (you can use a binary variable L for the light with the following logic: L = 1 if the light is on). [2]

(ii) Find the Boolean expression to have the heating on (you can use a variable H with the following logic: H = 1 if the heating is on): [2]

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Q2 (a) Consider the sequential circuit presented on figure Q2

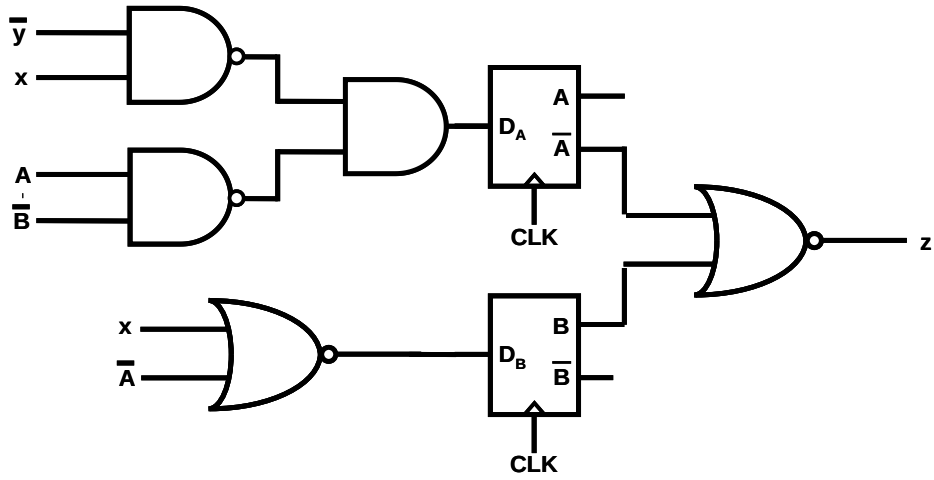


Figure Q2. Sequential circuit to analyse.

Answer the following questions:

(i) Find the Boolean expression for the next value of A and B and of the output. [4]

(ii) From (i), construct the state table. [4]

(b) In this question, you are tasked with designing a sequential circuit that detects the tag "10011". The circuit accepts one serial input, noted *x*, and has one output, noted *z*. The output is equal to '1', when the sequence '10011' has appeared at the input. Overlapping is not accepted.

Table Q2 presents an example of input sequence and output values (this table is only an illustration and does not illustrate all possible cases).

Table Q2. Example of a possible sequence for the system to be designed

x	0	1	0	0	1	1	0	0	1	1	0	1	1
z	0	0	0	0	0	1	0	0	0	0	0	0	0

In the first three subquestions, the proposed design is a Mealy machine.

(i) Define the states of the FSM and draw the state diagram. [4]

(ii) Deduce the binary coded state table. [4]

(iii) For an implementation using JK-type flip-flops, derive the Boolean expression of the flip-flop inputs and of the output function. [6]

Continued overleaf

(iv) Propose an alternative design (including a schematic) for a sequential circuit detecting the address ‘10011’ (not using an FSM). You must justify your answer. [3]

Continued overleaf

Q3 (a) In this question, you are tasked with designing a synchronous counter that goes through the sequence 0 1 3 5 4 7 2 6 and then repeats.

(i) Derive the state table for a synchronous counter that goes through the sequence above. [3]

(ii) Implement the counter using D flip-flops. [5]

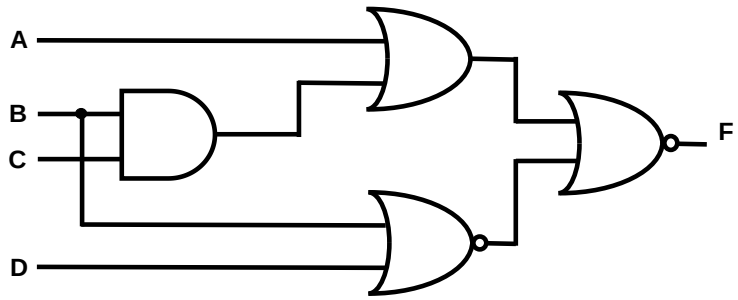
(b) This question relates to VHDL. Consider the combinational circuit represented by the Boolean function:

$$F(x, y, z) = x\bar{y} + \bar{x}z + yz$$

(i) Write the entity for this circuit. [3]

(ii) Propose a behavioral VHDL architecture for this circuit. [4]

(c) This question relates to VHDL. Consider the circuit on figure Q3c.



Write a structural VHDL code representing this circuit (you should provide both entity and architecture, but you can omit library definition at the start) [10]

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Q4 (a) Explain the differences between FPGA and ASIC and what are their respective advantages. [6]

(b) Stream cypher are a classic tool in cryptography. The principle is to XOR the plain text with a pseudorandom sequence in order to encrypt it.

To generate the pseudorandom sequence, a feedback polynomial is implemented using a LFSR.

Using a LFSR, propose an implementation for the feedback polynomial $x^{19} + x^{18} + x^{17} + x^{13} + 1$ [5]

(c) Describe the structure of an FPGA. You are expected to include drawings supporting your explanation and to explain the main blocks. [7]

(d) Implement the following four Boolean functions using a PROM:

$$F_1(x, y, z) = \sum m\,(1,2,4,6)$$
$$F_2(x, y, z) = \sum m(0,1,6,7)$$
$$F_3(x, y, z) = \sum m(2,6)$$
$$F_4(x, y, z) = \sum m(1,2,3,5,7)$$

[7]

End of question paper