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Kim et al.

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(54) **SEMICONDUCTOR PACKAGE INCLUDING REDISTRIBUTION PATTERN**

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CPC ***H01L 23/49822*** (2013.01); ***H01L 23/3128*** (2013.01); ***H01L 24/08*** (2013.01);
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CPC H01L 23/49822; H01L 23/3128; H01L 24/08; H01L 25/105; H01L 2224/08235; H01L 2225/1058
See application file for complete search history.

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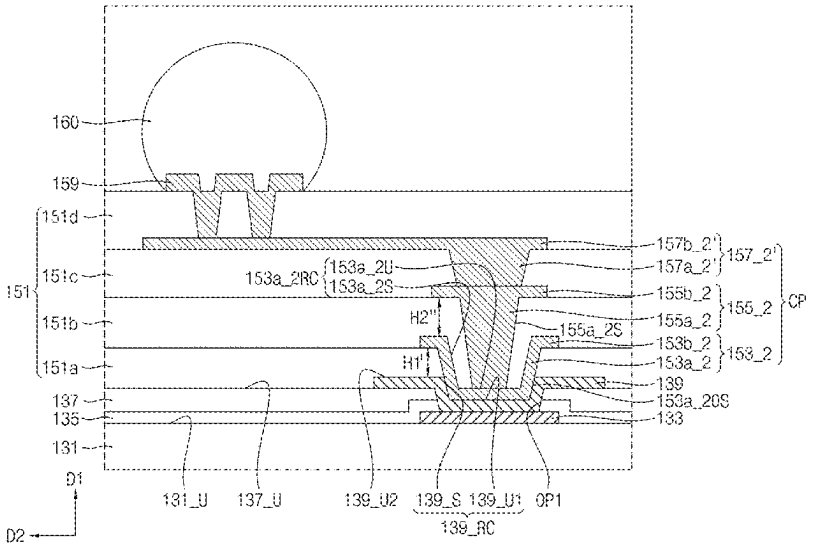
(57) **ABSTRACT**

A semiconductor package includes a semiconductor chip including a connecting pad, a mold layer covering the semiconductor chip, a lower redistribution layer on the semiconductor chip and the mold layer, and a connecting terminal on the lower redistribution layer. The lower redistribution layer includes a first lower insulating layer, a first conformal redistribution pattern extending through the first lower insulating layer, a second lower insulating layer on the first lower insulating layer and the first conformal redistribution pattern, and a first filled redistribution pattern disposed on the first conformal redistribution pattern and extending through the second lower insulating layer. A side surface of the first filled redistribution pattern is spaced apart from an inner side surface of the first conformal redistribution pattern. The second lower insulating layer is between the inner side surface of the first conformal redistribution pattern and the side surface of the first filled redistribution pattern.

20 Claims, 11 Drawing Sheets



(51) **Int. Cl.**
H01L 23/31 (2006.01)
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(52) **U.S. Cl.**
CPC .. ***H01L 25/105*** (2013.01); *H01L 2224/08235* (2013.01); *H01L 2225/1058* (2013.01)

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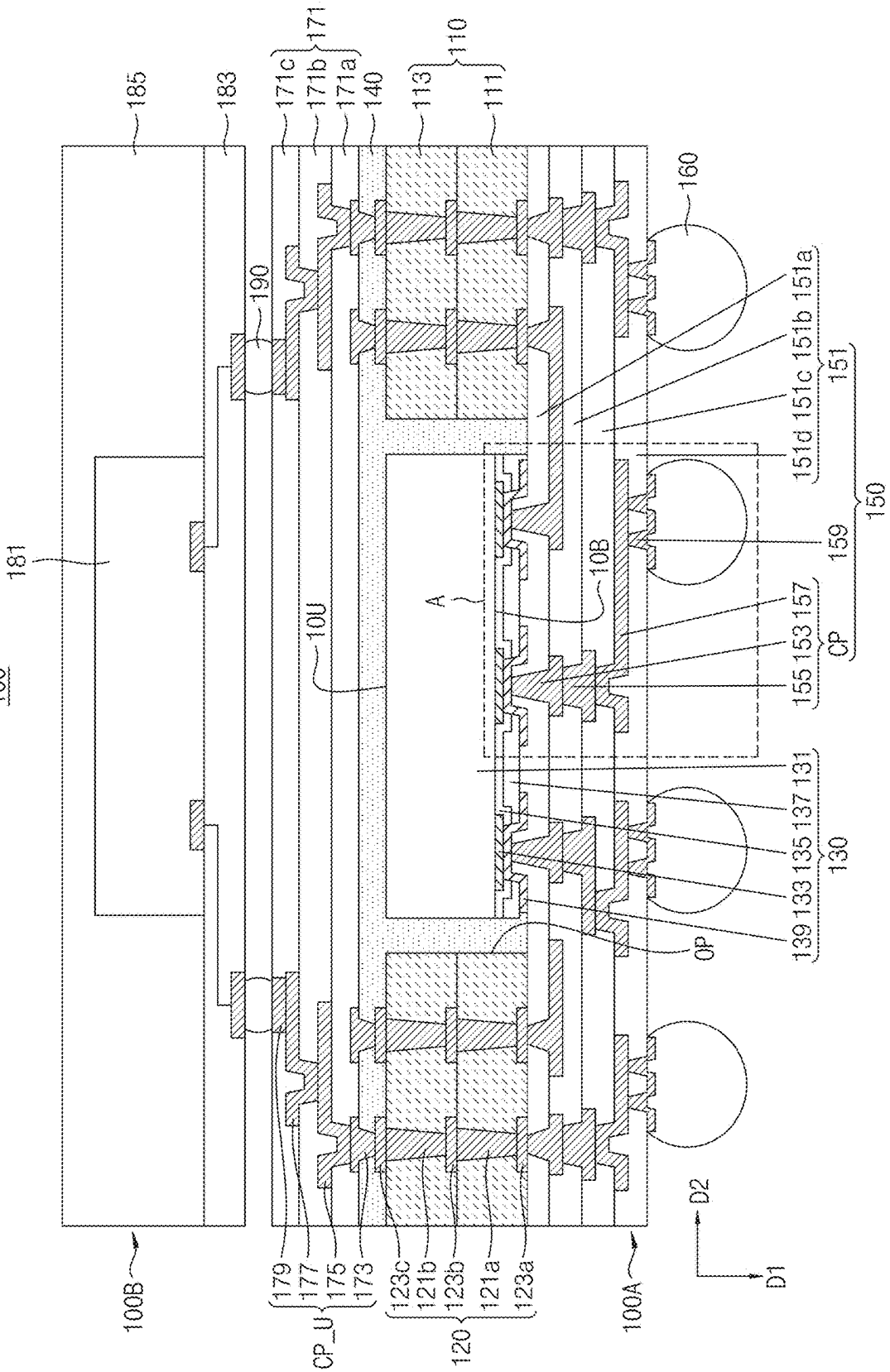
FIG. 1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181
185
183
171c
171b
171a
171
140
113
111
110
190
160
151a
151b
151c
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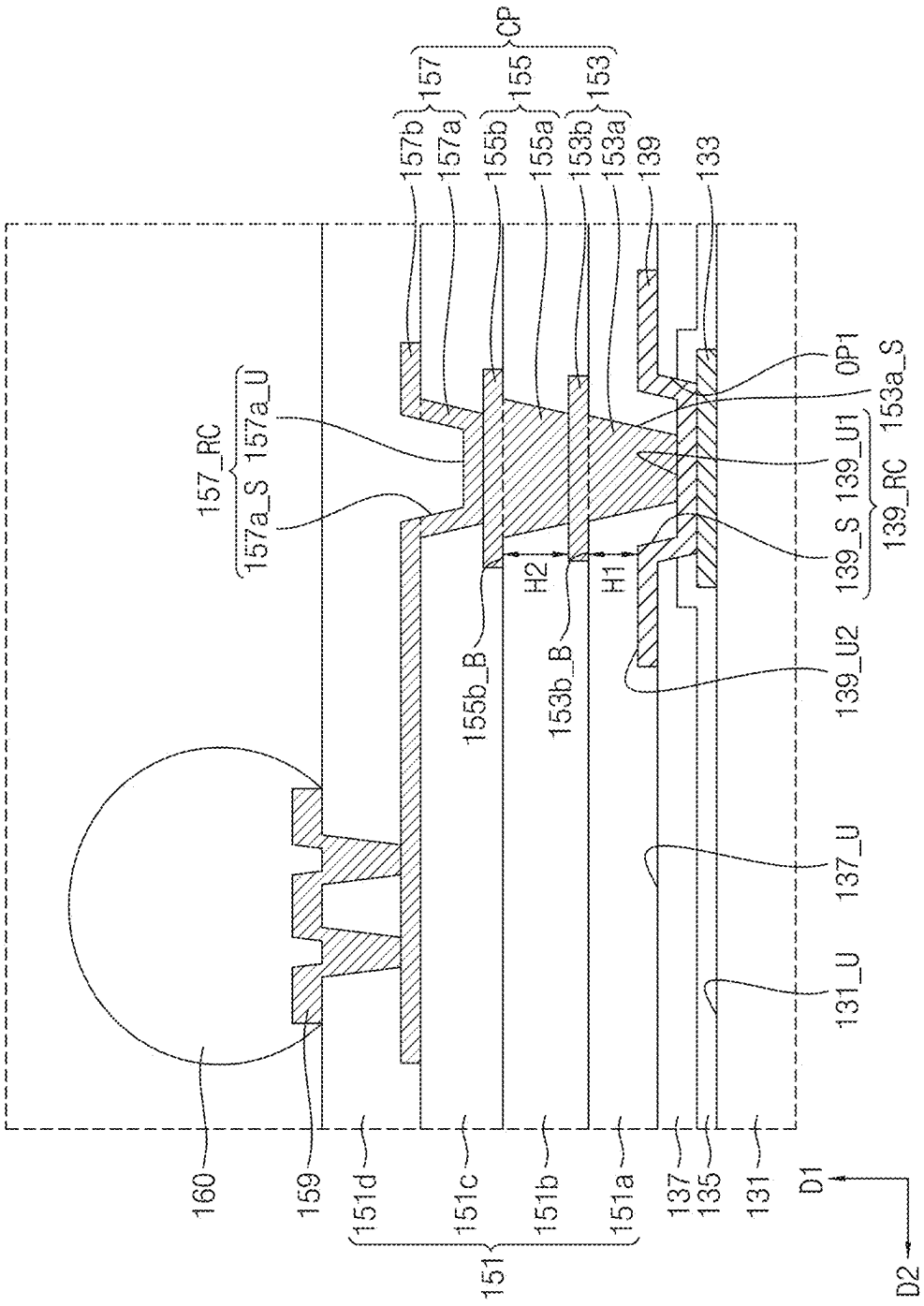
151
150
159
CP
157
153
155
131
137
135
133
139
130
OP
10U
A
10B
100B
100A
179
177
175
173
CP_U
123c
121b
123b
121a
123a
120
D2
D1

FIG. 2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157
155
153
157b
157a
155b
155a
153b
153a
139
133
157_RC
157a_S
157a_U
OP1
153a_S
139_U1
139_RC
139_S
H2
H1
155b_B
153b_B
139_U2
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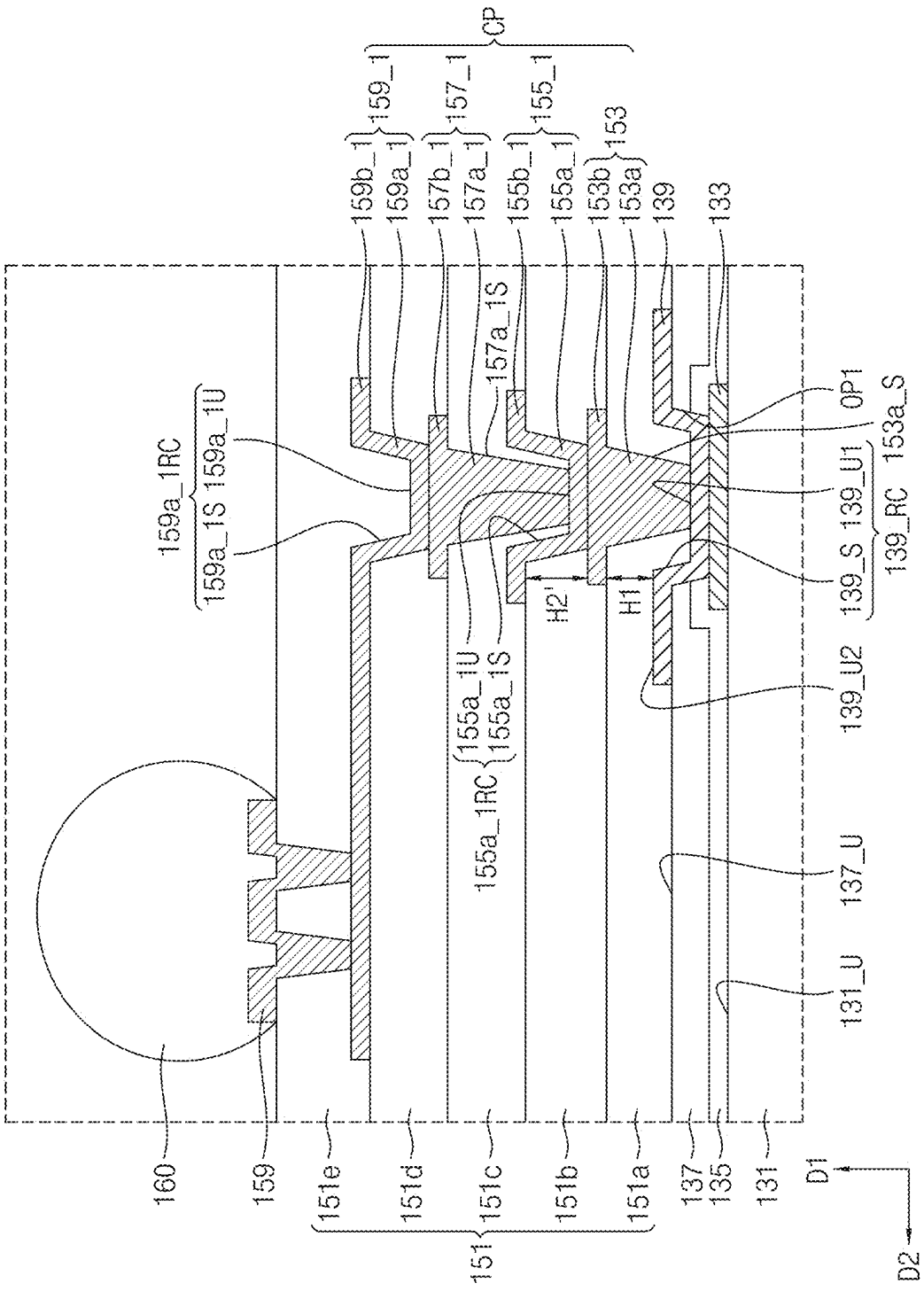
151d
151c
151b
151a
151
137
135
131
D1
D2

FIG. 3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159_1
157_1
155_1
153
159b_1
159a_1
157b_1
157a_1
155b_1
155a_1
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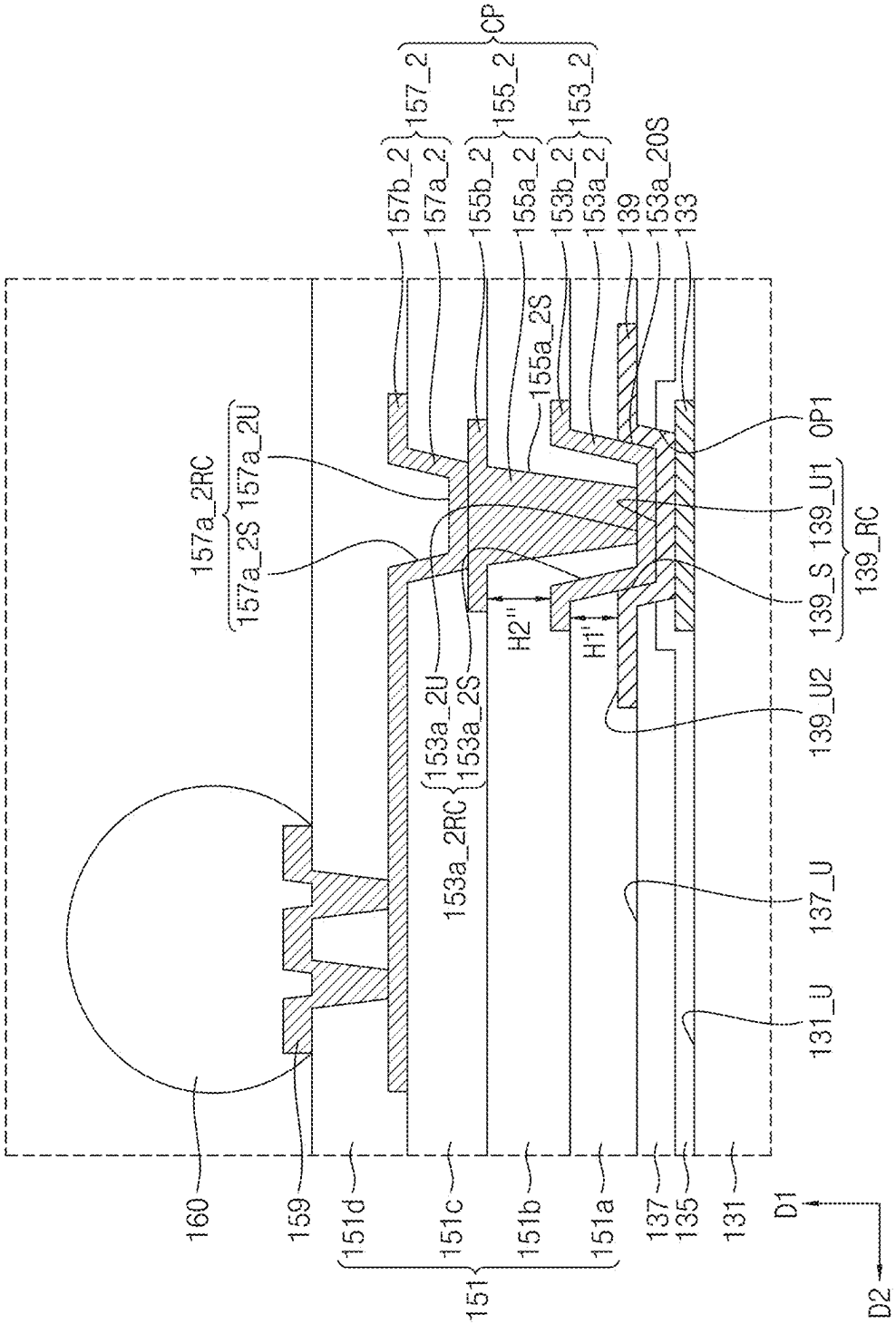
139
133
159a_1RC
159a_1S
159a_1U
157a_1S
0P1
153a_S
139_U1
139_RC
139_S
H2'
H1
155a_1U
155a_1S
155a_1RC
139_U2
137_U
131_U
160
159
151e
151d
151c
151b
151a
151
137
135
131
D1
D2

FIG. 4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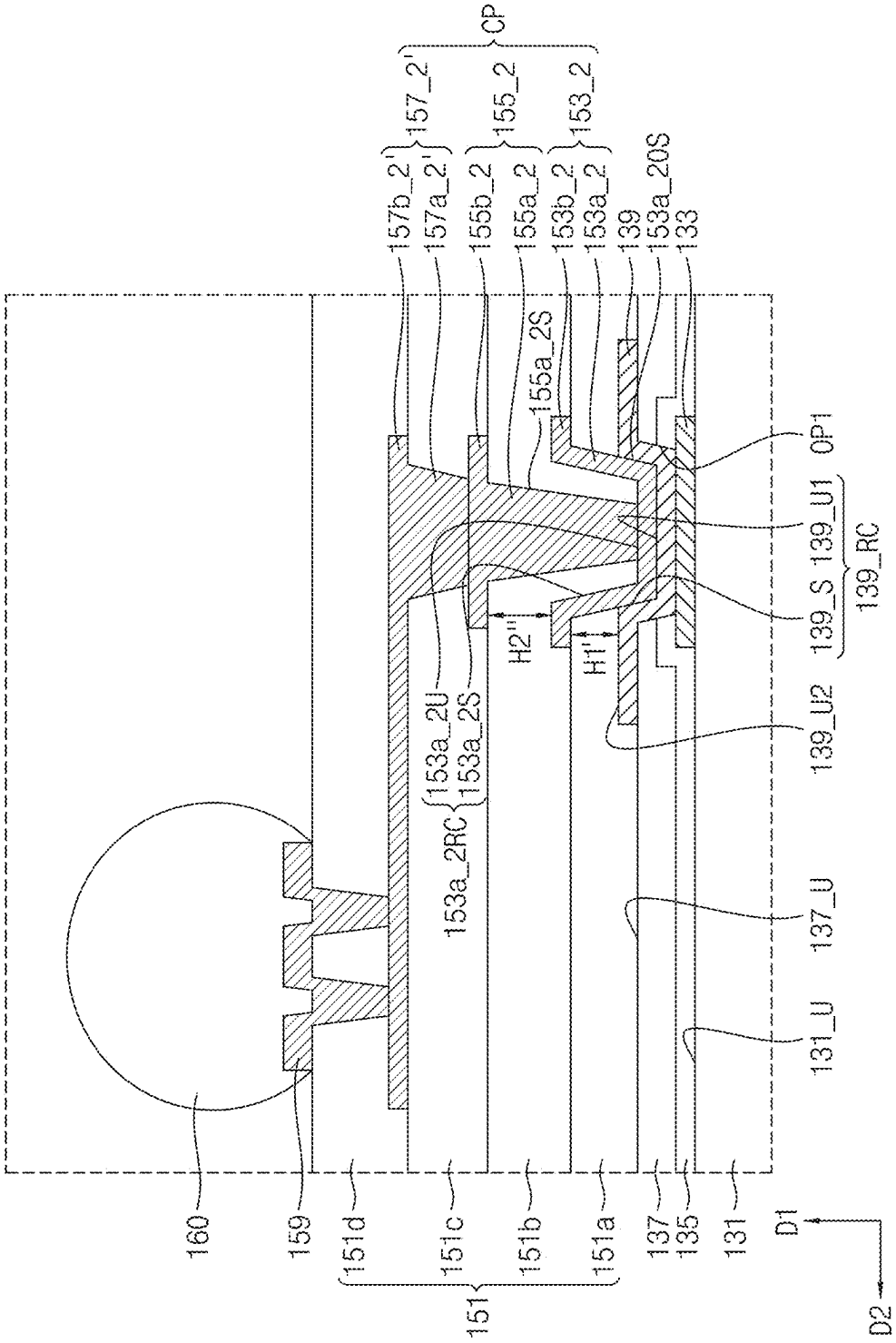
153a_2OS
133
OP1
139_U1
139_S
139_RC
139_U2
137_U
131_U
157a_2RC
157a_2S
157a_2U
153a_2U
153a_2S
153a_2RC
H2''
H1''
160
159
151d
151c
151b
151a
151
137
135
131
D1
D2

FIG. 5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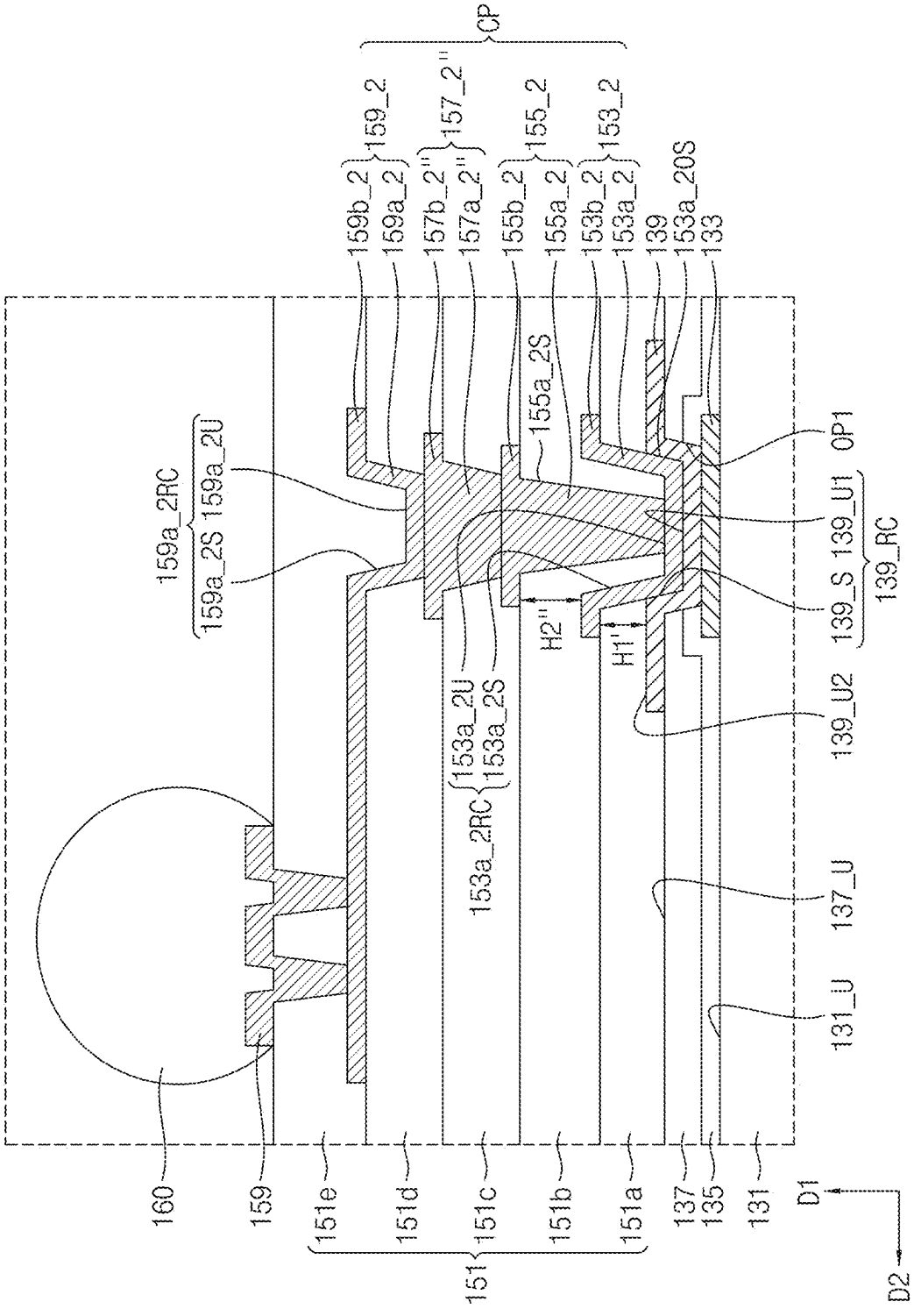
155a_2
153b_2
153a_2
139
153a_20S
133
155a_2S
0P1
139_U1
139_S
139_RC
H2'''
H1'''
153a_2U
153a_2S
153a_2RC
139_U2
137_U
131_U
160
159
151d
151c
151b
151a
151
137
135
131
D1
D2

FIG. 6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155_2
153_2
159b_2
159a_2
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155b_2
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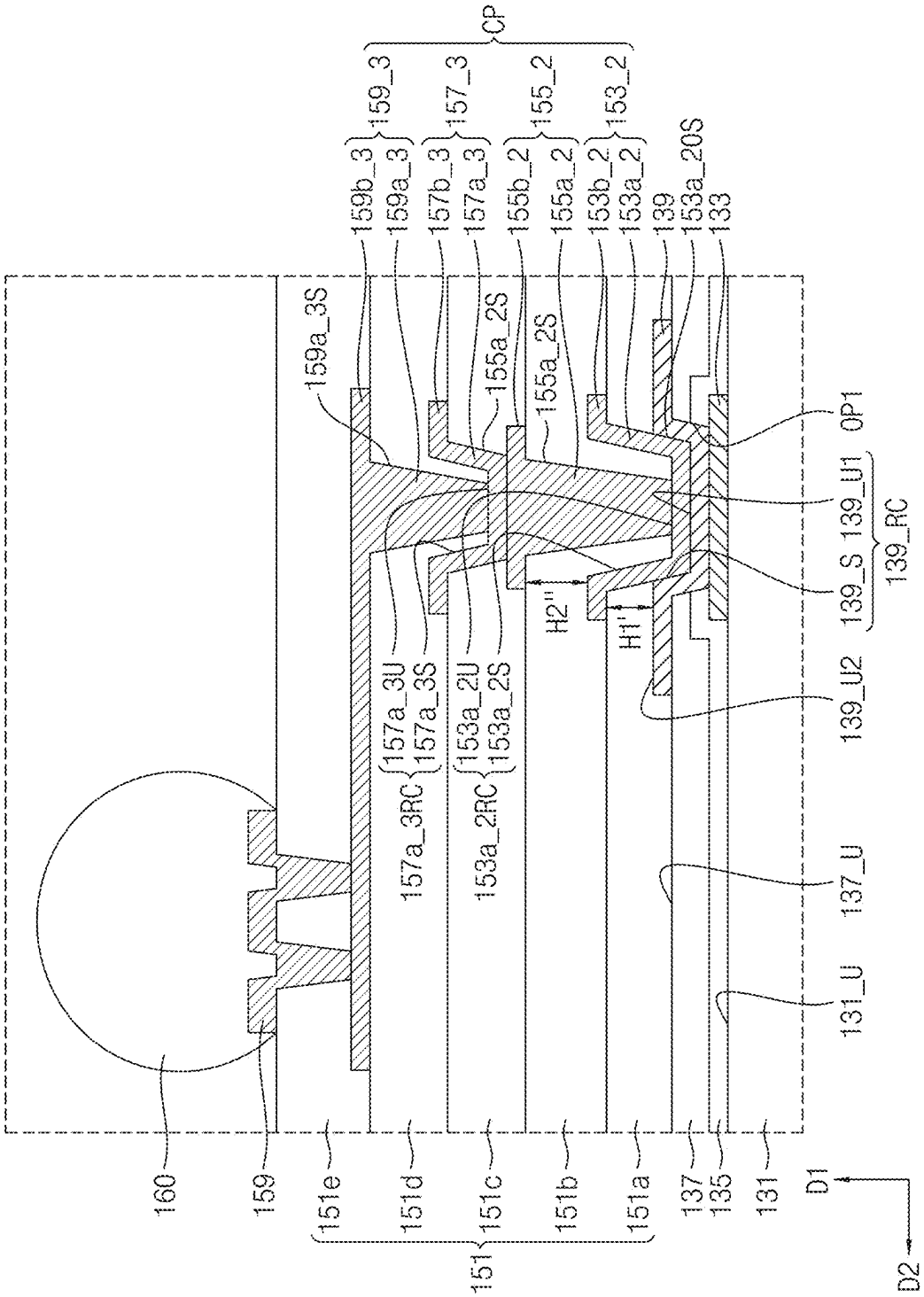
153a_2
139
153a_20S
133
159a_2RC
159a_2S
159a_2U
155a_2S
OP1
139_U1
139_S
139_RC
H2"
H1"
153a_2U
153a_2S
153a_2RC
139_U2
137_U
131_U
160
159
151e
151d
151c
151b
151a
151
137
135
131
D1
D2

FIG. 7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157_3
155_2
153_2
159b_3
159a_3
157b_3
157a_3
155b_2
155a_2
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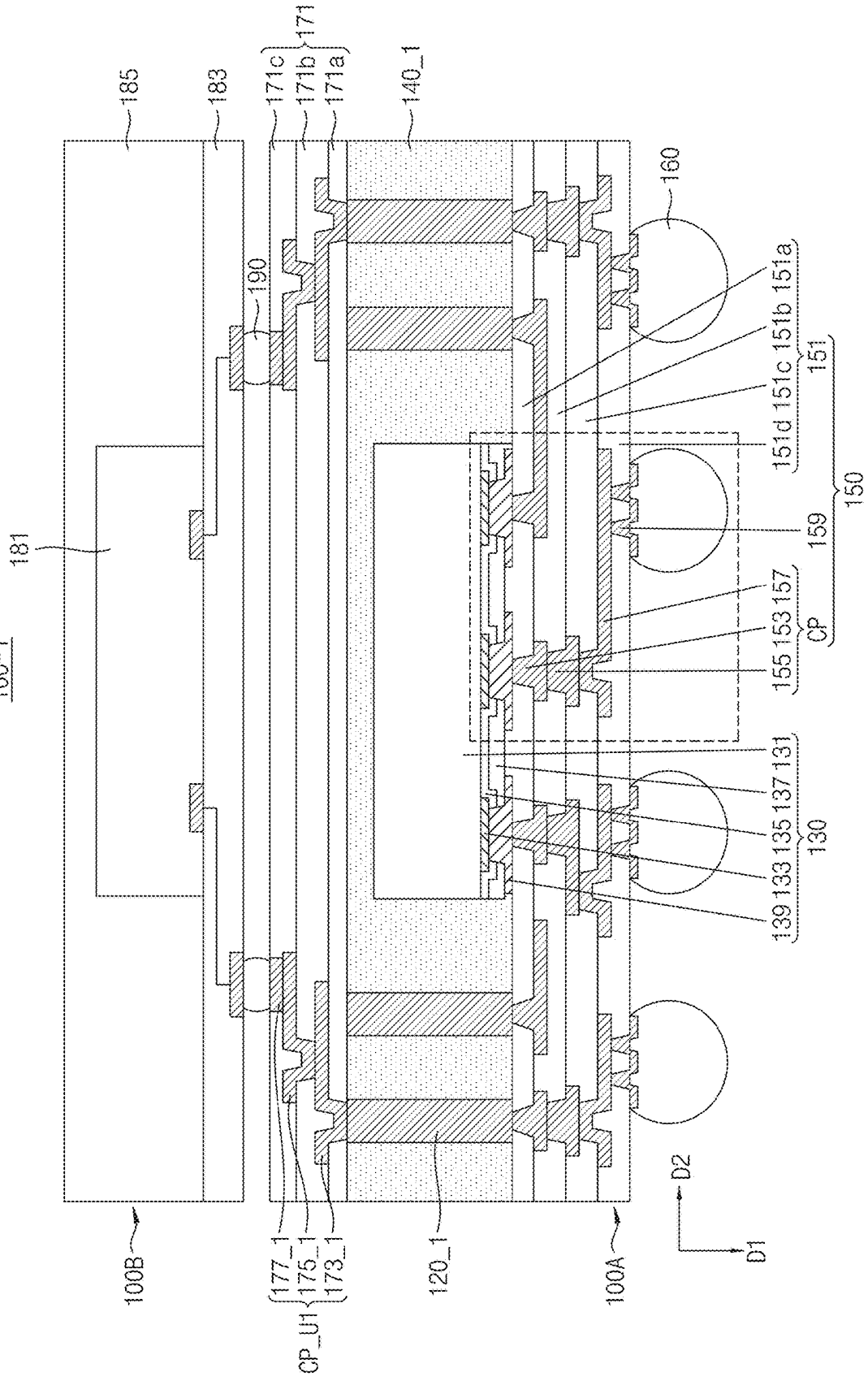
153a_2
139
153a_2OS
133
159a_3S
155a_2S
155a_2S
OP1
139_U1
139_RC
139_S
H2''
H1'
157a_3U
157a_3S
153a_2U
153a_2S
157a_3RC
153a_2RC
139_U2
137_U
131_U
160
159
151e
151d
151c
151b
151a
151
137
135
131
D1
D2

FIG. 8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185
183
171c
171b
171a
171
140_1
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151a
151b
151c
151d
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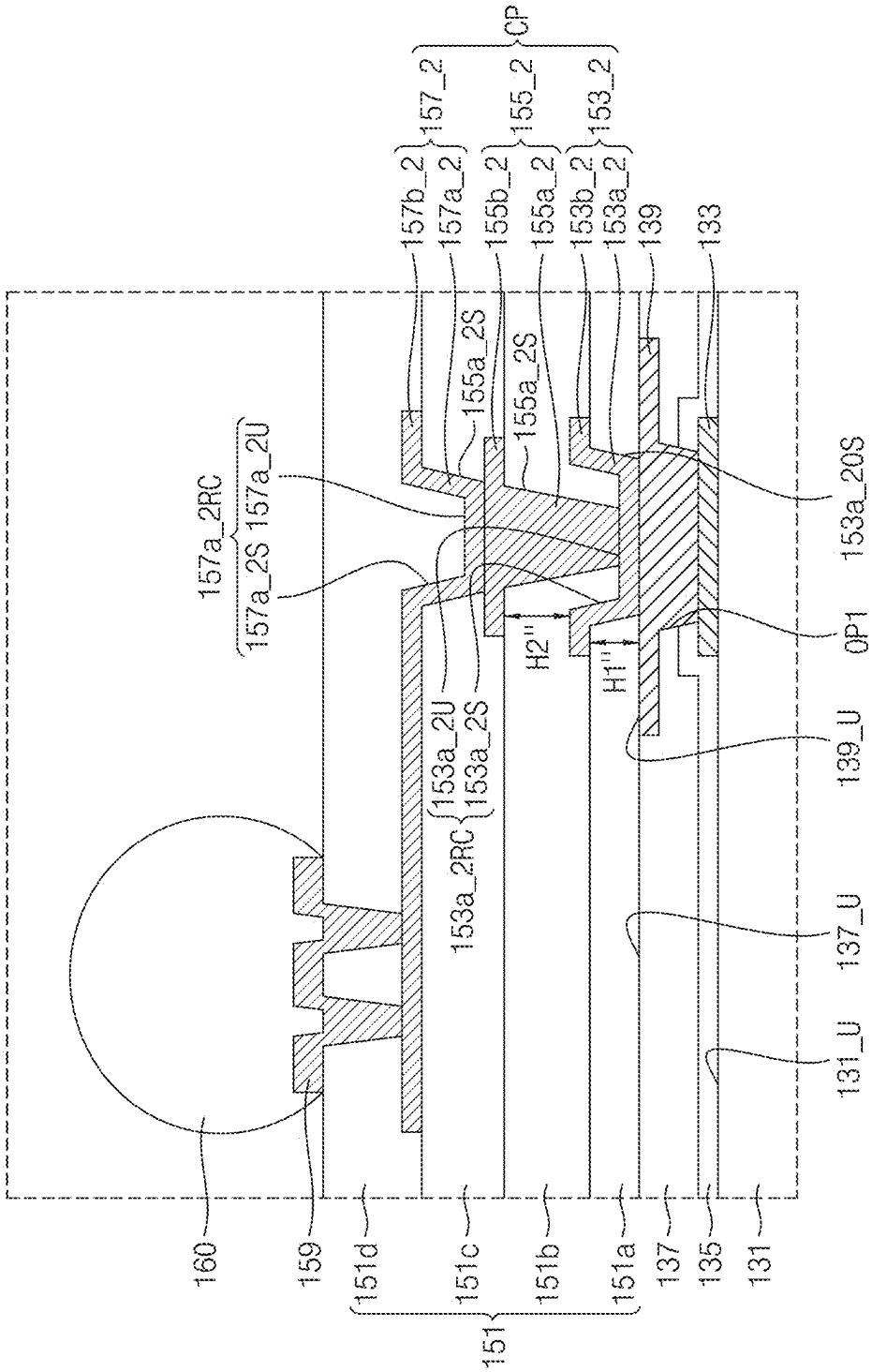
157
153
155
CP
131
137
135
133
139
130
100B
177_1
175_1
173_1
CP_U1
120_1
100A
D2
D1

FIG. 9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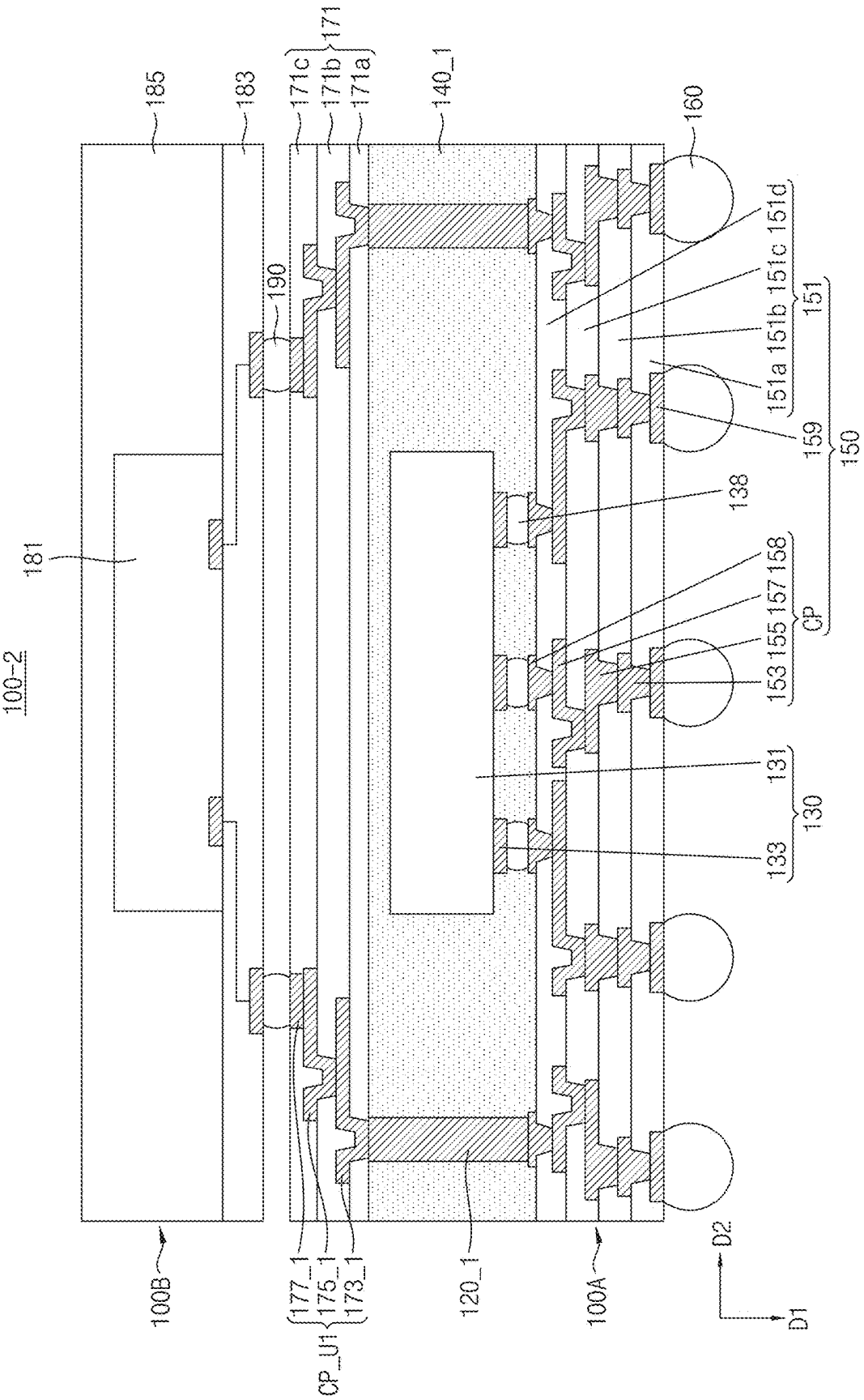
155_2
153_2
157b_2
157a_2
155b_2
155a_2
153b_2
153a_2
139
133
157a_2RC
157a_2S
157a_2U
155a_2S
155a_2S
153a_20S
H2''
H1''
0P1
153a_2U
153a_2S
153a_2RC
139_U
137_U
131_U
160
159
151d
151c
151b
151a
137
135
131
151

FIG. 10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185
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171c
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151d
151c
151b
151a
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138
158
157
155
153
CP
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133
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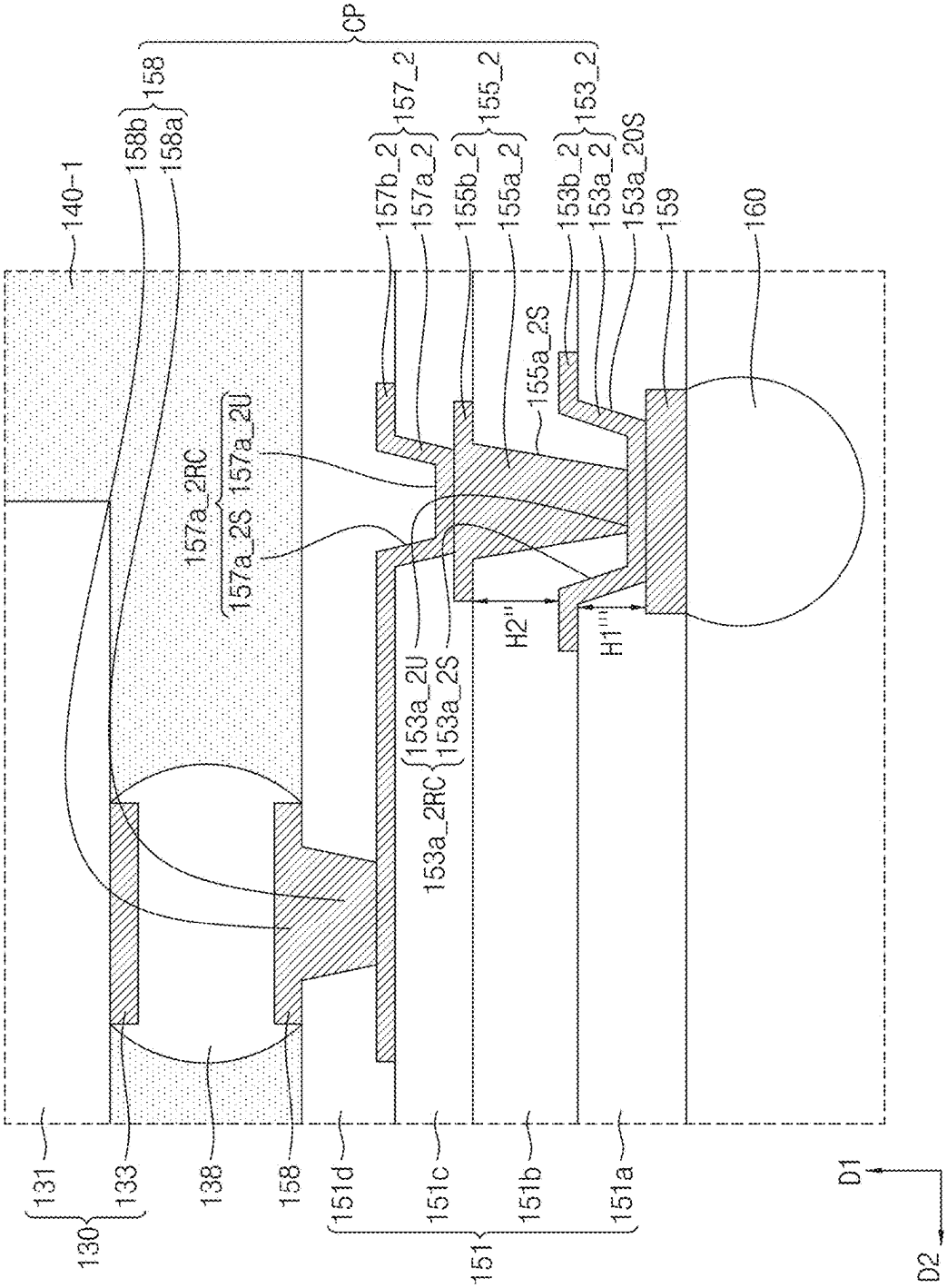
100B
177_1
175_1
173_1
CP_U1
120_1
100A
D2
D1

FIG. 11


CP
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158b
158a
140-1
157_2
157b_2
157a_2
155_2
155b_2
155a_2
153_2
153b_2
153a_2
153a_20S
159
160
155a_2S
157a_2RC
157a_2S
157a_2U
153a_2U
153a_2S
153a_2RC
H2''
H1''
131
133
130
138
158
151d
151c
151b
151a
151
D1
D2

SEMICONDUCTOR PACKAGE INCLUDING REDISTRIBUTION PATTERN

CROSS-REFERENCE TO THE RELATED APPLICATION

This application claims priority from Korean Patent Application No. 10-2021-0078640, filed on Jun. 17, 2021, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND

1. Field

The example embodiments of the disclosure relate to semiconductor packages including a redistribution pattern.

2. Description of the Related Art

In accordance with advances in electronics industries, development of a variety of technologies for achieving an enhancement in reliability and miniaturization of a semiconductor package is required. In order to meet such a requirement of an enhancement in reliability and miniaturization of a semiconductor package, active research on technology using a redistribution line is being conducted.

SUMMARY

The example embodiments of the disclosure provide semiconductor packages capable of eliminating a problem caused by a coefficient of thermal expansion difference between a semiconductor chip and a redistribution pattern in a semiconductor package using a redistribution line.

A semiconductor package according to an example embodiment of the disclosure may include a semiconductor chip including a connecting pad, a mold layer covering the semiconductor chip, a lower redistribution layer on the semiconductor chip and the mold layer, and a connecting terminal on the lower redistribution layer. The lower redistribution layer may include a first lower insulating layer, a first conformal redistribution pattern extending through the first lower insulating layer, a second lower insulating layer on the first lower insulating layer and the first conformal redistribution pattern, and a first filled redistribution pattern on the first conformal redistribution pattern, the first filled redistribution pattern extending through the second lower insulating layer. A side surface of the first filled redistribution pattern may be spaced apart from an inner side surface of the first conformal redistribution pattern. The second lower insulating layer may be between the inner side surface of the first conformal redistribution pattern and the side surface of the first filled redistribution pattern.

A semiconductor package according to an example embodiment of the disclosure may include a base layer including an opening, a conductive connector extending through the base layer, a semiconductor chip in the opening, a mold layer covering a top surface of each of the base layer and the semiconductor chip, and a lower redistribution layer on the base layer, the semiconductor chip and the mold layer. The semiconductor chip may include a die, a chip pad on the die, and a connecting pad on the chip pad. The connecting pad may include a first top surface, a second top surface, and an inner side surface interconnecting the first top surface and the second top surface. The lower redistribution layer may include a first lower insulating layer on the semiconductor chip, a first lower redistribution pattern extending through the first lower insulating layer, the first lower redistribution pattern including a first via contacting the first top surface of the connecting pad, and a first conductive pad on the first via, and a second lower redistribution pattern on the first lower redistribution pattern. A side surface of the first via may be spaced apart from the inner side surface of the connecting pad. The first lower insulating layer may be between the side surface of the first via and the inner side surface of the connecting pad.

A semiconductor package according to an example embodiment of the disclosure may include a semiconductor chip including a chip pad, a mold layer covering the semiconductor chip, a lower redistribution layer on a bottom surface of the mold layer, and a conductive connector connected to the lower redistribution layer and extending through the mold layer. The lower redistribution layer may include an under bump metal (UBM), a first lower insulating layer covering the UBM, a first conformal redistribution pattern on the UBM, the first conformal redistribution pattern extending through the first lower insulating layer, a second lower insulating layer on the first conformal redistribution pattern, and a first filled redistribution pattern on the first conformal redistribution pattern, the first filled redistribution pattern extending through the second lower insulating layer. A side surface of the first filled redistribution pattern may be spaced apart from an inner side surface of the first conformal redistribution pattern. The second lower insulating layer may be between the inner side surface of the first conformal redistribution pattern and the side surface of the first filled redistribution pattern.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a sectional view of a semiconductor package according to an example embodiment of the disclosure.

FIG. **2** is an enlarged view of a portion A of FIG. **1**.

FIG. **3** is an enlarged view showing a portion of a semiconductor package according to an example embodiment of the disclosure.

FIG. **4** is an enlarged view showing a portion of a semiconductor package according to an example embodiment of the disclosure.

FIG. **5** is an enlarged view showing a portion of a semiconductor package according to an example embodiment of the disclosure.

FIG. **6** is an enlarged view showing a portion of a semiconductor package according to an example embodiment of the disclosure.

FIG. **7** is an enlarged view showing a portion of a semiconductor package according to an example embodiment of the disclosure.

FIG. **8** is a sectional view of a semiconductor package according to an example embodiment of the disclosure.

FIG. **9** is an enlarged view showing a portion of a semiconductor package according to an example embodiment of the disclosure.

FIG. **10** is a sectional view of a semiconductor package according to an example embodiment of the disclosure.

FIG. **11** is an enlarged view of a portion of a semiconductor package according to an example embodiment of the disclosure.

DETAILED DESCRIPTION

When the terms "about" or "substantially" are used in this specification in connection with a numerical value, it is

intended that the associated numerical value includes a manufacturing or operational tolerance (e.g., ±10%) around the stated numerical value. Moreover, when the words "about" and "substantially" are used in connection with geometric shapes, it is intended that precision of the geometric shape is not required but that latitude for the shape is within the scope of the disclosure. Further, regardless of whether numerical values or shapes are modified as "about" or "substantially," it will be understood that these values and shapes should be construed as including a manufacturing or operational tolerance (e.g., ±10%) around the stated numerical values or shapes.

FIG. **1** is a sectional view of a semiconductor package according to an example embodiment of the disclosure.

Referring to FIG. **1**, a semiconductor package **100** may include a lower semiconductor package **100**A, and an upper semiconductor package **100**B on the lower semiconductor package **100**A. The upper semiconductor package **100**B may be disposed on the lower semiconductor package **100**A via connecting terminals **190**.

The lower semiconductor package **100**A may include a base layer **110**, a conductive connector **120**, a semiconductor chip **130**, a mold layer **140**, a lower redistribution layer **150**, connecting terminals **160**, and an upper redistribution layer **171**/CP_U.

The base layer **110** may be disposed outside the semiconductor chip **130**. The base layer **110** may have, at a central portion thereof, an opening OP extending through the base layer **110** in a first direction D**1**, and may be a plate having a quadrangular rim shape when viewed in a top view. The semiconductor chip **130** may be disposed in the opening OP. When viewed in a top view, the base layer **110** may surround a side surface of the semiconductor chip **130**. The size of the opening OP may be greater than the size of the semiconductor chip **130**. The semiconductor chip **130** and the base layer **110** may be spaced apart from each other in a second direction D**2**. The second direction D**2** may perpendicularly intersect the first direction D**1**.

The base layer **110** may have a multilayer structure. For example, the base layer **110** may include a first base layer **111** and a second base layer **113**. The first base layer **111** and the second base layer **113** may be sequentially stacked on a top surface of the lower redistribution layer **150** in a direction opposite to the first direction D**1**. The first base layer **111** may be disposed on the lower redistribution layer **150**, and the second base layer **113** may be disposed on the first base layer **111**. For example, the base layer **110** may include at least one of phenol resin, epoxy resin, and polyimide. For example, the base layer **110** may include at least one of flame retardant 4 (FR4), tetrafunctional epoxy, polyphenylene ether, bismaleimide triazine (BT), epoxy/polyphenylene oxide, Thermount, cyanate ester, polyimide, and liquid crystal polymer.

At least some of the conductive connector **120** may extend through the base layer **110**, and thus may electrically interconnect the lower redistribution layer **150** and the upper redistribution layer **171**/CP_U. The conductive connector **120** may include conductive vias **121***a* and **121***b*, and conductive pads **123***a*, **123***b* and **123***c*. The conductive vias **121***a* and **121***b* may include a first conductive via **121***a* and a second conductive via **121***b*. The conductive pads **123***a*, **123***b* and **123***c* may include a first conductive pad **123***a*, a second conductive pad **123***b*, and a third conductive pad **123***c*. The first conductive pad **123***a* may be disposed on a bottom surface of the first base layer **111**, the second conductive pad **123***b* may be disposed on a top surface of the first base layer **111**, and the first conductive via **121***a* may extend through the first base layer **111**, and thus may interconnect the first conductive pad **123***a* and the second conductive pad **123***b*. The third conductive pad **123***c* may be disposed on a top surface of the second base layer **113**, the second conductive via **121***b* may extend through the second base layer **113**, and thus may interconnect the second conductive pad **123***b* and the third conductive pad **123***c*.

The semiconductor chip **130** may be disposed in the opening OP of the base layer **110**. The semiconductor chip **130** may include a die **131**, chip pads **133**, a first passivation layer **135**, a second passivation layer **137**, and connecting pads **139**. The die **131** may include at least one of silicon, germanium, and gallium arsenide. Various circuits may be formed at the die **131**. The chip pads **133** may be disposed on a bottom surface **10**B of the die **131**. The chip pads **133** may include a conductive material. The first passivation layer **135** may cover a portion of the bottom surface **10**B of the die **131**, a portion of a bottom surface of each chip pad **133** and a side surface of each chip pad **133**. The first passivation layer **135** may expose a portion of the bottom surface of each chip pad **133**. For example, the first passivation layer **135** may include silicon oxide and/or silicon nitride. The second passivation layer **137** may cover the first passivation layer **135**. The first passivation layer **135** may be disposed between the second passivation layer **137** and the die **131** and between the second passivation layer **137** and the chip pads **133**. The second passivation layer **137** may expose the chip pads **133** through the first passivation layer **135** exposing the chip pads **133**. A plurality of openings OP**1** (cf. FIG. **2**) respectively exposing the chip pads **133** may be formed at the first passivation layer **135** and the second passivation layer **137**. For example, the second passivation layer **137** may include photosensitive polyimide (PSPI). The connecting pads **139** may be connected to the chip pads **133**, respectively. The connecting pads **139** may be connected to the chip pads **133** through the openings OP**1** (cf. FIG. **2**) of the first passivation layer **135** and the second passivation layer **137**, respectively. The connecting pads **139** may contact the first passivation layer **135** through the openings OP**1** (cf. FIG. **2**). The connecting pads **139** may cover a portion of a bottom surface of the second passivation layer **137**. The connecting pads **139** may include a conductive material.

The mold layer **140** may be disposed on the semiconductor chip **130** and the base layer **110**. The mold layer **140** may fill the opening OP of the base layer **110** while extending between the semiconductor chip **130** and the base layer **110**. The mold layer **140** may cover a side surface and a top surface **10**U of the semiconductor chip **130**, and may cover a top surface and an inner side surface of the base layer **110**. For example, the mold layer **140** may include an epoxy molding compound (EMC).

The lower redistribution layer **150** may be disposed on the base layer **110**, the semiconductor chip **130** and the mold layer **140**. The lower redistribution layer **150** may be disposed on the bottom surface **10**B of the die **131** of the semiconductor chip **130**. The lower redistribution layer **150** may include lower insulating layers **151**, lower redistribution patterns CP, and under bump metals (UBMs) **159**. The lower insulating layers **151** may include a first lower insulating layer **151***a*, a second lower insulating layer **151***b*, a third lower insulating layer **151***c*, and a fourth lower insulating layer **151***d*. The first to fourth lower insulating layers **151***a*, **151***b*, **151***c* and **151***d* may be sequentially stacked on a bottom surface of the base layer **110** and a bottom surface of the semiconductor chip **130** in the first direction D**1**. For example, the first to fourth lower insulating layers **151***a*, **151***b*, **151***c* and **151***d* may include a curable material. That

is, the lower insulating layers **151** may be a material cured by heat or light. For example, the curable material included in the first to fourth lower insulating layers **151***a*, **151***b*, **151***c* and **151***d* may include an inorganic material such as silicon oxide, silicon nitride or a silicon oxynitride and/or a polyamide series polymer material. For example, the curable material included in the lower insulating layers **151** may include at least one of photosensitive polyimide (PSPI), polybenzoxazole (PBO), a phenolic polymer, a benzocyclobutene (BCB) series polymer and an epoxy series polymer.

The lower redistribution patterns CP may be disposed in the lower insulating layers **151**. The lower redistribution patterns CP may include a first lower redistribution pattern **153**, a second lower redistribution pattern **155**, and a third lower redistribution pattern **157**. The first to third lower redistribution patterns **153**, **155** and **157** may be sequentially stacked in the first direction D**1**. The first lower redistribution pattern **153** may be directly connected to the connecting pad **139**. A portion of the first lower redistribution pattern **153** may extend through the first lower insulating layer **151***a*, and another portion of the lower redistribution pattern **153** may be disposed on a bottom surface of the first lower insulating layer **151***a*. The second lower redistribution pattern **155** may be connected to the first lower redistribution pattern **153**. A portion of the second lower redistribution pattern **155** may extend through the second lower insulating layer **151***b*, and another portion of the second lower redistribution pattern **155** may be disposed on a bottom surface of the second lower insulating layer **151***b*. The third lower redistribution pattern **157** may be connected to the second lower redistribution pattern **155**. A portion of the third lower redistribution pattern **157** may extend through the third lower insulating layer **151***c*, and another portion of the third lower redistribution pattern **157** may be disposed on a bottom surface of the third lower insulating layer **151***c*. The lower redistribution patterns CP may include a conductive material. For example, the lower redistribution patterns CP may include copper.

The UBMs **159** may be electrically connected to the lower redistribution patterns CP. The UBMs **159** may be directly connected to the third lower redistribution pattern **157**. A portion of each UBM **159** may be connected to a bottom surface of the third lower redistribution pattern **157** while extending through the fourth lower insulating layer **151***d*, and another portion of each UBM **159** may be disposed on a bottom surface of the fourth lower insulating layer **151***d*. The UBMs **159** may include a conductive material.

The connecting terminals **160** may be disposed on a bottom surface of the lower redistribution layer **150**. The connecting terminals **160** may be connected to the UBMs **159**, respectively. The connecting terminals **160** may be disposed on bottom surfaces of the UBMs **159**, respectively. The connecting terminals **160** may be electrically connected to the semiconductor chip **130** and/or the conductive connector **120** via the UBMs **159** and the lower redistribution patterns CP.

The upper redistribution layer **171**/CP_U may be disposed on the mold layer **140**. The upper redistribution layer **171**/CP_U may be disposed on the top surface **10**U of the semiconductor chip **130**. The upper redistribution layer **171**/CP_U may include upper insulating layers **171** and upper redistribution patterns CP_U. The upper insulating layers **171** may include a first upper insulating layer **171***a*, a second upper insulating layer **171***b*, and a third upper insulating layer **171***c*. The first to third upper insulating layers **171***a*, **171***b* and **171***c* may be sequentially stacked on the mold layer **140** in the direction opposite to the first direction D**1**. The upper insulating layers **171** may include the same material as the lower insulating layers **151**.

The upper redistribution patterns CP_U may be disposed in the upper insulating layers **171**. The upper redistribution patterns CP_U may include a first upper redistribution pattern **173**, a second upper redistribution pattern **175**, a third upper redistribution pattern **177**, and an upper pad **179**. The first upper redistribution pattern **173** may be connected to the third conductive pad **123***c* while extending through the mold layer **140**. The first upper insulating layer **171***a* may cover a portion of the first upper redistribution pattern **173**. The second upper redistribution pattern **175** may be connected to the first upper redistribution pattern **173** while extending through the first upper insulating layer **171***a*. The second upper insulating layer **171***b* may cover a portion of the second upper redistribution pattern **175**. The third upper redistribution pattern **177** may be disposed on the second upper redistribution pattern **175**. The upper pad **179** may be disposed on the third upper redistribution pattern **177**. The third upper insulating layer **171***c* may cover a portion of the third upper redistribution pattern **177** and a portion of the upper pad **179**. The third upper insulating layer **171***c* may expose a top surface of the upper pad **179**. The connecting terminal **190** may be disposed on the upper pad **179**.

The upper semiconductor package **100**B may include a semiconductor chip **181**, a redistribution layer **183**, and a mold layer **185**. In an example embodiment, the upper semiconductor package **100**B may include a configuration identical or similar to the configuration of the lower semiconductor package **100**A. For example, the redistribution layer **183** may have the same configuration as the lower redistribution layer **150**.

FIG. **2** is an enlarged view of a portion A of FIG. **1**. In FIG. **2**, the portion A of FIG. **1** is shown in an inverted state such that the connecting terminal **160** is disposed at a higher level than the lower redistribution layer **150**, for convenience of description. Accordingly, a constituent element referred to as a "top surface" in FIG. **1** may be referred to as a "bottom surface" in FIG. **2**, and a constituent element referred to as a "bottom surface" in FIG. **1** may be referred to as a "top surface" in FIG. **2**.

Referring to FIG. **2**, the connecting pad **139** may include a first top surface **139**_U**1**, a second top surface **139**_U**2**, and an inner side surface **139**_S. The second top surface **139**_U**2** may be disposed relatively farther from the die **131** of the semiconductor chip **130** than the first top surface **139**_U**1**. The first top surface **139**_U**1** may be disposed at a lower level than a top surface **137**_U of the second passivation layer **137** of the semiconductor chip **130** with reference to a top surface **131**_U of the die **131**, and the second top surface **139**_U**2** may be disposed at a higher level than the top surface **137**_U of the second passivation layer **137** of the semiconductor chip **130** with reference to the top surface **131**_U of the die **131**. The connecting pad **139** may have a step formed by the first top surface **139**_U**1** and the second top surface **139**_U**2**. The inner side surface **139**_S may interconnect the first top surface **139**_U**1** and the second top surface **139**_U**2**. The connecting pad **139** may include a recess **139**_RC defined by the first top surface **139**_U**1** and the inner side surface **139**_S.

The lower redistribution patterns CP may include a filled redistribution pattern and a conformal redistribution pattern. Each of the filled redistribution pattern and the conformal redistribution pattern may include a via extending through a lower insulating layer, and a conductive pattern on the via. The filled redistribution pattern may be formed by a fill

plating process, and may completely fill an opening of the lower insulating layer, through which the via of the filled redistribution pattern extends. The via of the filled redistribution pattern may have a pillar shape. For example, the via of the filled redistribution pattern may have a tapered pillar shape. The conformal redistribution pattern may be formed by a conformal plating process, and may be formed in a uniform thickness along a side wall of the opening of the lower insulating layer, through which the via of the conformal redistribution pattern extends. The conformal redistribution pattern may include a recess.

The first lower redistribution pattern **153** may be a filled redistribution pattern formed by a fill plating process. The first lower redistribution pattern **153** may be referred to as a "first filled redistribution pattern". The first lower redistribution pattern **153** may contact the first top surface **139**_U**1** of the connecting pad **139** while being spaced apart from the second top surface **139**_U**2** and the inner side surface **139**_S of the connecting pad **139**. The first lower pattern **153** may include a first via **153***a* and a first conductive pattern **153***b*. The first via **153***a* may be disposed on the connecting pad **139**. A portion of the first via **153***a* may be disposed in the recess **139**_RC of the connecting pad **139**. The first via **153***a* may extend through the first lower insulating layer **151***a*. A bottom surface of the first via **153***a* may contact the first top surface **139**_U**1** of the connecting pad **139**. The width of the bottom surface of the first via **153***a* may be smaller than the width of the first top surface **139**_U**1** of the connecting pad **139**. A side surface **153***a*_S of the first via **153***a* may be spaced apart from the inner side surface **139**_S of the connecting pad **139**. A portion of the first lower insulating layer **151***a* may be interposed between the side surface **153***a*_S of the first via **153***a* and the inner side surface **139**_S of the connecting pad **139**. The first lower insulating layer **151***a* may completely surround the side surface **153***a*_S of the first via **153***a*. The first lower insulating layer **151***a* may contact a portion of the first top surface **139**_U**1** of the connecting pad **139**, and may contact the inner side surface **139**_S of the connecting pad **139**. The first lower insulating layer **151***a* may fill the recess **139**_RC of the connecting pad **139**.

The first conductive pattern **153***b* may be disposed on the first via **153***a*. The first conductive pattern **153***b* may completely cover a top surface of the first via **153***a*. The width of the first conductive pattern **153***b* may be greater than the width of the top surface of the first via **153***a*. A portion of the first conductive pattern **153***b* may not vertically overlap with the first via **153***a*. A portion of the first conductive pattern **153***b* may vertically overlap with a portion of the second top surface **139**_U**2** of the connecting pad **139**. A minimum distance H**1** between a bottom surface **153***b*_B of the first conductive pattern **153***b* and the second top surface **139**_U**2** of the connecting pad **139** may be about 3 to 10 μm.

The second lower redistribution pattern **155** may be a filled redistribution pattern formed by a fill plating process. The second lower redistribution pattern **155** may be referred to as a "second filled redistribution pattern". The second lower redistribution pattern **155** may include a second via **155***a* and a second conductive pattern **155***b*. The second via **155***a* may be disposed on the first conductive pattern **153***b*. The second via **155***a* may extend through the second lower insulating layer **151***b*. A bottom surface of the second via **155***a* may contact a top surface of the first conductive pattern **153***b*. The second conductive pattern **155***b* may be disposed on the second via **155***a*. The second conductive pattern **155***b* may completely cover a top surface of the second via **155***a*. A minimum distance H**2** between a bottom surface **155***b*_B of the second conductive pattern **155***b* and the top surface of the first conductive pattern **153***b* may be equal to or greater than the minimum distance H**1** between a bottom surface **153**_B of the first conductive pattern **153***b* and the second top surface **139**_U**2** of the connecting pad **139**.

The third lower redistribution pattern **157** may be a conformal redistribution pattern formed by a conformal plating process. The third lower redistribution pattern **157** may be referred to as a "conformal redistribution pattern" or a "first conformal redistribution pattern". The third lower redistribution pattern **157** may have a uniform thickness. The third lower redistribution pattern **157** may include a third via **157***a* and a third conductive pattern **157***b*. The third via **157***a* may extend through the third lower insulating layer **151***c*. The third via **157***a* may have a U shape. The third via **157***a* may include a recess **157**_RC, and may include a top surface **157***a*_U and an inner side surface **157***a*_S which define the recess **157**_RC. The top surface **157***a*_U of the third via **157***a* may be disposed at a lower level than a top surface of the third lower insulating layer **151***c* with reference to the top surface **131**_U of the die **131** of the semiconductor chip **130**. The inner side surface **157***a*_S of the third via **157***a* may interconnect the top surface **157***a*_U of the third via **157***a* and the third conductive pattern **157***b*. The third conductive pattern **157***b* may be connected to an upper end of the third via **157***a*. The third conductive pattern **157***b* may extend in the second direction D**2**, and an extension portion of the third conductive pattern **157***b* may not overlap with the connecting pad **139**. The fourth lower insulating layer **151***d* may cover the top surface **157***a*_U and the inner side surface **139**_S of the third via **157***a*. The fourth lower insulating layer **151***d* may fill the recess **157**_RC of the third via **157***a*. The fourth lower insulating layer **151***d* may cover the third conductive pattern **157***b*.

The UBM **159** may be connected to the third conductive pattern **157***b* while extending through the fourth lower insulating layer **151***d*. The UBM **159** may be disposed on the portion of the third conductive pattern **157***b* extending in the second direction D**2**. The UBM **159** may not vertically overlap with the connecting pad **139**. The UBM **159** may not vertically overlap with the first lower redistribution pattern **153**, the second lower redistribution pattern **155**, and the third via **157***a* of the third lower redistribution pattern **157**.

Although the lower redistribution patterns CP are shown in FIG. **2** as including two filled redistribution patterns **153** and **155**, the example embodiments of the disclosure are not limited thereto, and the lower redistribution patterns CP may include three or more filled redistribution patterns under the conformal redistribution pattern **157**. In an example embodiment, the lower redistribution patterns CP may further include a fourth lower redistribution pattern, which is a filled redistribution pattern, on the third lower redistribution pattern **157**.

FIG. **3** is an enlarged view showing a portion of a semiconductor package according to an example embodiment of the disclosure.

Referring to FIG. **3**, lower redistribution patterns CP may include a first lower redistribution pattern **153**, a second lower redistribution pattern **155_1**, a third lower redistribution pattern **157_1**, and a fourth lower redistribution pattern **159_1**. Lower insulating layers **151** may include a first lower insulating layer **151***a*, a second lower insulating layer **151***b*, a third lower insulating layer **151***c*, a fourth lower insulating layer **151***d*, and a fifth lower insulating layer **151***e*. The first lower redistribution pattern **153** may be a filled redistribu-

tion pattern, and may have the same characteristics as the first lower redistribution pattern **153** described with reference to FIG. **2**.

The second lower redistribution pattern **155_1** may be disposed on the first lower redistribution pattern **153**. The second lower redistribution pattern **155_1** may be a conformal redistribution pattern formed by a conformal plating process. The second lower redistribution pattern **155_1** may be referred to as a "first conformal redistribution pattern". The second lower redistribution pattern **155_1** may have a uniform thickness. The second lower redistribution pattern **155_1** may include a second via **155***a*_1 and a second conductive pattern **155***b*_1. The second via **155***a*_1 may extend through the second lower insulating layer **151***b*. The second via **155***a*_1 may have a U shape. The second via **155***a*_1 may include a recess **155***a*_1RC, and may include a top surface **155***a*_1U and an inner side surface **155***a*_1S which define the recess **155***a*_1RC. The top surface **155***a*_1U of the second via **155***a*_1 may be disposed at a lower level than a top surface of the second lower insulating layer **151***b* with reference to a top surface **131**_U of a die **131** of a semiconductor chip **130**. The inner side surface **155***a*_1S of the second via **155***a*_1 may interconnect the top surface **155***a*_1U of the second via **155***a*_1 and the second conductive via **155***b*_1. The second conductive pattern **155***b*_1 may be connected to an upper end of the second via **155***a*_1. The third lower insulating layer **151***c* may contact a portion of the top surface **155***a*_1U of the second via **155***a*_1 and the inner side surface **155***a*_1S of the second via **155***a*_1. The third lower insulating layer **151***c* may fill the recess **155***a*_1RC of the second via **155***a*_1. The third lower insulating layer **151***c* may cover the second conductive pattern **155***b*_1.

The third lower redistribution pattern **157_1** may be disposed on the second lower redistribution pattern **155_1**. The third lower redistribution pattern **157_1** may be a filled redistribution pattern formed by a fill plating process. The third lower redistribution pattern **157_1** may be referred to as a "second filled redistribution pattern". A side surface of the third lower redistribution pattern **157_1** may be spaced apart from the inner side surface **155***a*_1S of the second lower redistribution pattern **155_1**. The third lower insulating layer **151***c* may be interposed between the side surface of the third lower redistribution pattern **157_1** and the inner side surface **155_1**S of the second lower redistribution pattern **155_1**. The third lower redistribution pattern **157_1** may include a third via **157***a*_1 and a third conductive pattern **157***b*_1. The third via **157***a*_1 may extend through the third lower insulating layer **151***c*. A portion of the third via **157***a*_1 may be disposed in the recess **155***a*_1RC of the second via **155***a*_1. A side surface **157***a*_1S of the third via **157***a*_1 may be spaced apart from the inner side surface **155***a*_1S of the second via **155***a*_1. A portion of the top surface **155***a*_1U of the second via **155***a*_1 may be exposed by the third via **157***a*_1. The third insulating layer **151***c* may fill the recess **155***a*_1RC of the second via **155***a*_1. The third lower insulating layer **151***c* may contact the inner side surface **155***a*_1S of the second via **155***a*_1. The third lower insulating layer **151***c* may contact a portion of the top surface **155***a*_1U of the second via **155***a*_1 exposed by the third via **157***a*_1. The third lower insulating layer **151***c* may completely surround the side surface **157***a*_1S of the third via **157***a*_1. The third lower insulating layer **151***c* may be disposed between the side surface **157***a*_1S of the third via **157***a*_1 and the inner side surface **155***a*_1S of the second via **155***a*_1. The third conductive pattern **157***b*_1 may be disposed on the third via **157***a*_1.

The fourth lower redistribution pattern **159_1** may be disposed on the third lower redistribution pattern **157_1**. The fourth lower redistribution pattern **159_1** may be a conformal redistribution pattern formed by a conformal plating process. The fourth lower redistribution pattern **159_1** may be referred to as a "second conformal redistribution pattern". The fourth lower redistribution pattern **159_1** may include a fourth via **159***a*_1 and a fourth conductive pattern **159***b*_1. The fourth via **159***a*_1 may extend through the fourth lower insulating layer **151***d*. The fourth via **159***a*_1 may have a U shape. The fourth via **159***a*_1 may include a recess **159***a*_1RC, and may include a top surface **159***a*_1U and an inner side surface **159***a*_1S which define the recess **159***a*_1RC. The top surface **159***a*_1U of the fourth via **159***a*_1 may be disposed at a lower level than a top surface of the fourth lower insulating layer **151***d* with reference to the top surface **131**_U of the die **131** of the semiconductor chip **130**. The inner side surface **159***a*_1S of the fourth via **159***a*_1 may interconnect the top surface **159***a*_1U of the fourth via **159***a*_1 and the fourth conductive pattern **159***b*_1. The fourth conductive pattern **159***b*_1 may be connected to an upper end of the fourth via **159***a*_1. The fifth insulating layer **151***e* may be disposed on the fourth lower redistribution pattern **159_1**. The fifth lower insulating layer **151***e* may contact the top surface **159***a*_1U and the inner side surface **159***a*_1S of the fourth via **159***a*_1. The fifth lower insulating layer **151***e* may fill the recess **159***a*_1RC of the fourth via **159***a*_1. A UBM **159** may be connected to the fourth lower redistribution pattern **159_1** while extending through the fifth lower insulating layer **151***e*.

In an example embodiment, the fourth lower redistribution pattern **159_1** may be a filled redistribution pattern formed by a fill plating process, differently from the shown case. In an example embodiment, the fourth lower redistribution pattern **159_1** may be omitted, differently from the shown case. In this case, the third conductive pattern **157***b*_1 may be directly connected to the UBM **159**.

FIG. **4** is an enlarged view showing a portion of a semiconductor package according to an example embodiment of the disclosure.

Referring to FIG. **4**, lower redistribution patterns CP may include a first lower redistribution pattern **153_2**, a second lower redistribution pattern **155_2**, and a third lower redistribution pattern **157_2**. Lower insulating layers **151** may include a first lower insulating layer **151***a*, a second lower insulating layer **151***b*, a third lower insulating layer **151***c*, and a fourth lower insulating layer **151***d*.

The first lower redistribution pattern **153_2** may be a conformal redistribution pattern formed by a conformal plating process. The first lower redistribution pattern **153_2** may be referred to as a "first conformal redistribution pattern". The first lower redistribution pattern **153_2** may have a uniform thickness. The first lower redistribution pattern **153_2** may include a first via **153***a*_2 and a first conductive pattern **153***b*_2. The first via **153***a*_2 may extend through the first lower insulating layer **151***a*. The first via **153***a*_2 may have a U shape. A bottom surface of the first via **153***a*_2 may cover a first top surface **139**_U1 of a connecting pad **139**. The width of the bottom surface of the first via **153***a*_2 may correspond to the width of a first top surface **139**_U1 of the connecting pad **139**. A portion of an outer side surface **153***a*_2OS of the first via **153***a*_2 may contact an inner side surface **139**_S of the connecting pad **139**. A portion of the outer side surface **153***a*_2OS of the first via **153***a*_2 may contact the first lower insulating layer **151***a*. The first via **153***a*_2 may include a recess **153***a*_2RC, and may include a top surface **153***a*_2U and an inner side surface

153*a*_2S which define the recess 153*a*_2RC. The top surface 153*a*_2U of the first via 153*a*_2 may be disposed at a lower level than a second top surface 139_U2 of the connecting pad 139 with reference to a top surface 131_U of a die 131 of a semiconductor chip 130. The inner side surface 153*a*_2S of the first via 153*a*_2 may interconnect the top surface 153*a*_2U of the first via 153*a*_2 and the first conductive pattern 153*b*_2. The first conductive pattern 153*b*_2 may be connected to an upper end of the first via 153*a*_2. The second lower insulating layer 151*b* may contact a portion of the top surface 153*a*_2U of the first via 153*a*_2 and the inner side surface 153*a*_2S of the first via 153*a*_2. The second lower insulating layer 151*b* may fill the recess 153*a*_2RC of the first via 153*a*_2. The second lower insulating layer 151*b* may cover the first conductive pattern 153*b*_2.

The second lower redistribution pattern 155_2 may be disposed on the first lower redistribution pattern 153_2. The second lower redistribution pattern 155_2 may be a filled redistribution pattern formed by a fill plating process. The second lower redistribution pattern 155_2 may be referred to as a "first filled redistribution pattern". A side surface of the second lower redistribution pattern 155_2 may be spaced apart from the inner side surface 153*a*_2S of the first lower redistribution pattern 153_2. The second lower insulating layer 151*b* may be interposed between the side surface of the second lower redistribution pattern 155_2 and the inner side surface 153*a*_2S of the first lower redistribution pattern 153_2. The second lower redistribution pattern 155_2 may include a second via 155*a*_2 and a second conductive pattern 155*b*_2. The second via 155*a*_2 may extend through the second lower insulating layer 151*b*. A portion of the second via 155*a*_2 may be disposed in the recess 153*a*_2RC of the first via 153*a*_2. A side surface 155*a*_2S of the second via 155*a*_2 may be spaced apart from the inner side surface 153*a*_2S of the first via 153*a*_2. A bottom surface of the second via 155*a*_2 may contact a portion of the top surface 153*a*_2U of the first via 153*a*_2. A portion of the top surface 153*a*_2U of the first via 153*a*_2 may be exposed by the second via 155*a*_2. The second lower insulating layer 151*b* may fill the recess 153*a*_2RC of the first via 153*a*_2. The second lower insulating layer 151*b* may contact the inner side surface 153*a*_2S of the first via 153*a*_2. The second lower insulating layer 151*b* may contact a portion of the top surface 153*a*_2U of the first via 153*a*_2 exposed by the second via 155*a*_2. The second lower insulating layer 151*b* may completely surround the side surface 155*a*_2S of the second via 155*a*_2. The second lower insulating layer 151*b* may be interposed between the side surface 155*a*_2S of the second via 155*a*_2 and the inner side surface 153*a*_2S of the first via 153*a*_2. The second conductive pattern 155*b*_2 may be disposed on the second via 155*a*_2. A portion of the second conductive pattern 155*b*_2 may vertically overlap with a portion of the first conductive pattern 153*b*_2. A minimum distance H2" between the first conductive pattern 153*b*_2 and the second conductive pattern 155*b*_2 may be equal to or greater than a minimum distance H1' between the second top surface 139_U2 of the connecting pad 139 and the first conductive pattern 153*b*_2. For example, the minimum distance H1' between the second top surface 139_U2 of the connecting pad 139 and the first conductive pattern 153*b*_2 may be about 3 to 10 μm.

The third lower redistribution pattern 157_2 may be disposed on the second lower redistribution pattern 155_2. The third lower redistribution pattern 157_2 may be a conformal redistribution pattern formed by a conformal plating process. The third lower redistribution pattern 157_2 may be referred to as a "second conformal redistribution pattern". The third lower redistribution pattern 157_2 may have a uniform thickness. The third lower redistribution pattern 157_2 may include a third via 157*a*_2 and a third conductive pattern 157*b*_2. The third via 157*a*_2 may extend through the third lower insulating layer 151*c*. The third via 157*a*_2 may have a U shape. The third via 157*a*_2 may include a recess 157*a*_2RC, and may include a top surface 157*a*_2U and an inner side surface 157*a*_2S which define the recess 157*a*_2RC. The top surface 157*a*_2U of the third via 157*a*_2 may be disposed at a lower level than a top surface of the third lower insulating layer 151*c* with reference to the top surface 131_U of the die 131 of the semiconductor chip 130. The inner side surface 157*a*_2S of the third via 157*a*_2 may interconnect the top surface 157*a*_2U of the third via 157*a*_2 and the third conductive via 157*b*_2. The third conductive pattern 157*b*_2 may be connected to an upper end of the third via 157*a*_2. The fourth lower insulating layer 151*d* may be disposed on the third lower redistribution pattern 157_2. The fourth lower insulating layer 151*d* may fill the recess 157*a*_2RC of the third via 157*a*_2. The fourth lower insulating layer 151*d* may contact the top surface 157*a*_2U and the inner side surface 157*a*_2S of the third via 157*a*_2. The fourth lower insulating layer 151*d* may cover the second conductive pattern 157*b*_2.

FIG. 5 is an enlarged view showing a portion of a semiconductor package according to an example embodiment of the disclosure.

Referring to FIG. 5, lower redistribution patterns CP are different from the lower redistribution patterns CP of FIG. 4 in that a third lower redistribution pattern 157_2' is a filled redistribution pattern other than a conformal redistribution pattern. The lower redistribution patterns CP of FIG. 5 may have the same characteristics as the lower redistribution patterns CP described with reference to FIG. 4, except that the third lower redistribution pattern 157_2' is a filled redistribution pattern. The third lower redistribution pattern 157_2' may be referred to as a "second filled redistribution pattern".

FIG. 6 is an enlarged view showing a portion of a semiconductor package according to an example embodiment of the disclosure.

Referring to FIG. 6, lower redistribution patterns CP may further include a fourth lower redistribution pattern 159_2, as compared to the lower redistribution patterns CP of FIG. 5, and lower insulating layers 151 may further include a fifth lower insulating layer 151*e*, as compared to the lower insulating layers 151 of FIG. 5. A third lower redistribution pattern 157_2" may be spaced apart from a UBM 159. The third lower redistribution pattern 157_2" may include a third via 157*a*_2" and a third conductive pattern 157*b*_2", and the third conductive pattern 157*b*_2" may not lengthily extend in a second direction D2, differently from a third conductive pattern 157*a*_2' of FIG. 5.

A fourth lower redistribution pattern 159_2 may be disposed on the third lower redistribution pattern 157_2". The fourth lower redistribution pattern 159_2 may be a conformal redistribution pattern formed by a conformal plating process. The fourth lower redistribution pattern 159_2 may be referred to as a "second conformal redistribution pattern". The fourth lower redistribution pattern 159_2 may have a uniform thickness. The fourth lower redistribution pattern 159_2 may include a fourth via 159*a*_2 and a fourth conductive pattern 159*b*_2. The fourth via 159*a*_2 may extend through a fourth lower insulating layer 151*d*. The fourth via 159*a*_2 may have a U shape. The fourth via 159*a*_2 may

include a recess **159***a*_2RC, and may include a top surface **159***a*_2U and an inner side surface **159***a*_2S which define the recess **159***a*_2RC. The top surface **159***a*_2U of the fourth via **159***a*_2 may be disposed at a lower level than a top surface of the fourth lower insulating layer **151***d* with reference to a top surface **131**_U of a die **131** of a semiconductor chip **130**. The inner side surface **159***a*_2S of the fourth via **159***a*_2 may interconnect the top surface **159***a*_2U of the fourth via **159***a*_2 and the fourth conductive pattern **159***b*_2. The fourth conductive pattern **159***b*_2 may be connected to an upper end of the fourth via **159***a*_2. The fourth conductive pattern **159***b*_2 may extend in the second direction D2, and an extension portion of the fourth conductive pattern **159***b*_2 may not overlap with a connecting pad **139**. The fifth lower insulating layer **151***e* may cover the top surface **159***a*_2U and the inner side surface **159***a*_2S of the fourth via **159***a*_2. The fifth lower insulating layer **151***e* may fill the recess **159***a*_2RC of the fourth via **159***a*_2. The fifth lower insulating layer **151***e* may cover the fourth conductive pattern **159***b*_2.

A UBM **159** may be connected to the fourth conductive pattern **159***b*_2 while extending through the fifth lower insulating layer **151***e*. The UBM **159** may be disposed on the portion of the fourth conductive pattern **159***b*_2 extending in the second direction D2.

In an example embodiment, the fourth lower redistribution pattern **159**_2 may be a filled-plated pattern formed by a fill plating method, differently from the case shown in FIG. **6**. In this case, the fourth lower redistribution pattern **159**_2 may be referred to as a "third filled redistribution pattern".

FIG. **7** is an enlarged view showing a portion of a semiconductor package according to an example embodiment of the disclosure.

Referring to FIG. **7**, lower redistribution patterns CP may further include a fourth lower redistribution pattern **159**_3, as compared to the lower redistribution patterns CP of FIG. **4**, and lower insulating layers **151** may further include a fifth lower insulating layer **151***e*, as compared to the lower insulating layers **151** of FIG. **4**.

A third lower redistribution pattern **157**_3 may be disposed on a second lower redistribution pattern **155**_2. The third lower redistribution pattern **157**_3 may be a conformal redistribution pattern formed by a conformal plating process. The third lower redistribution pattern **157**_3 may be referred to as a "second conformal redistribution pattern". The third lower redistribution pattern **157**_3 may have a uniform thickness. The third lower redistribution pattern **157**_3 may include a third via **157***a*_3 and a third conductive pattern **157***b*_3. The third via **157***a*_3 may extend through a third lower insulating layer **151***c*. The third via **157***a*_3 may have a U shape. The third via **157***a*_3 may include a recess **157***a*_3RC, and may include a top surface **157***a*_3U and an inner side surface **157***a*_3S which define the recess **157***a*_3RC. The top surface **157***a*_3U of the third via **157***a*_3 may be disposed at a lower level than a top surface of the third lower insulating layer **151***c* with reference to a top surface **131**_U of a die **131** of a semiconductor chip **130**. The inner side surface **157***a*_3S of the third via **157***a*_3 may interconnect the top surface **157***a*_3U of the third via **157***a*_3 and the third conductive pattern **157***b*_3. A fourth lower insulating layer **151***d* may contact a portion of the top surface **157***a*_3U of the third via **157***a*_3 and the inner side surface **157***a*_3S of the third via **157***a*_3.

The fourth lower redistribution pattern **159**_3 may be disposed on the third lower redistribution pattern **157**_3. The fourth lower redistribution pattern **159**_3 may be a filled redistribution pattern formed by a fill plating process. The fourth lower redistribution pattern **159**_3 may be referred to as a "second filled redistribution pattern". The fourth lower redistribution pattern **159**_3 may include a fourth via **159***a*_3 and a fourth conductive pattern **159***b*_3. The fourth via **159***a*_3 may extend through the fourth lower insulating layer **151***d*, and a portion of the fourth via **159***a*_3 may be disposed in the recess **157***a*_3RC of the third via **157***a*_3. A side surface **159***a*_3S of the fourth via **159***a*_3 may be spaced apart from the inner side surface **157***a*_3S of the third via **157***a*_3. A portion of the top surface **157***a*_3U of the third via **157***a*_3 may be exposed by the fourth via **159***a*_3. The fourth lower insulating layer **151***d* may fill the recess **157***a*_3RC of the third via **157***a*_3. The fourth lower insulating layer **151***d* may be interposed between the inner side surface **157***a*_3S of the third via **157***a*_3 and the side surface **159***a*_3S of the fourth via **159***a*_3. The fourth lower insulating layer **151***d* may contact the inner side surface **157***a*_3S of the third via **157***a*_3. The fourth lower insulating layer **151***d* may contact a portion of the top surface **157***a*_3U of the third via **157***a*_3 exposed by the fourth via **159***a*_3. The fourth lower insulating layer **151***d* may completely surround the side surface **159***a*_3S of the fourth via **159***a*_3. The fourth conductive pattern **159***b*_3 may be disposed on the fourth via **159***a*_3. The fourth conductive pattern **159***b*_3 may extend in a second direction D2, and an extension portion of the fourth conductive pattern **159***b*_3 may not vertically overlap with a connecting pad **139**. The fifth lower insulating layer **151***e* may cover the fourth conductive pattern **159***b*_3 of the fourth lower redistribution pattern **159**_3. A UBM **159** may be disposed on the extension portion of the fourth conductive pattern **159***b*_3 while extending through the fifth lower insulating layer **151***e*.

FIG. **8** is a sectional view of a semiconductor package according to an example embodiment of the disclosure.

Referring to FIG. **8**, a semiconductor package **100-1** may include a lower semiconductor package **100**A and an upper semiconductor package **100**B. The lower semiconductor package **100**A may include a semiconductor chip **130**, a mold layer **140**_1, a conductive connector **120**_1, a lower redistribution layer **150**, connecting terminals **160**, and an upper redistribution layer **171**/CP_U1. The lower semiconductor package **100**A of FIG. **8** is different form the lower semiconductor package **100**A of FIG. **1** in that the lower semiconductor package **100**A includes the mold layer **140**_1 and the conductive connector **120**_1, which extends through the mold layer **140**_1, in place of the base layer **110** and the conductive connector **120**_1, respectively, in the base layer **110**.

The semiconductor chip **130** may be disposed on the lower redistribution layer **150**. The mold layer **140**_1 may cover a side surface and a top surface of the semiconductor chip **130**. The mold layer **140**_1 may cover a portion of a top surface of the lower redistribution layer **150**. The conductive connector **120**_1 may extend through the mold layer **140**_1. The conductive connector **120**_1 may electrically interconnect the lower redistribution layer **150** and the upper redistribution layer **171**/CP_U1.

The semiconductor chip **130** may have the same characteristics as the semiconductor chip **130** described with reference to FIG. **1**, except that the semiconductor chip **130** includes a connecting pad **139** having a flat bottom surface. The lower redistribution layer **150** may include lower redistribution patterns CP, lower insulating layers **151**, and UBMs **159**, and the lower redistribution patterns CP may have characteristics identical or similar to those of the lower redistribution patterns CP described with reference to FIGS.

1 to 7, except that the lower redistribution patterns CP are connected to the connecting pad **139** having the flat bottom surface.

The upper redistribution layer **171**/CP_U1 may be disposed on the mold layer **140_1**. The upper redistribution layer **171**/CP_U1 may include upper insulating layers **171** and upper redistribution patterns CP_U1, and the upper redistribution patterns CP_U1 may include a first upper redistribution pattern **173_1**, a second upper redistribution pattern **175_1**, and an upper pad **177_1** which are sequentially stacked. The upper insulating layers **171** may include a first upper insulating layer **171***a*, a second upper insulating layer **171***b*, and a third upper insulating layer **171***c* which are sequentially stacked. The first upper redistribution pattern **173_1** may be connected to the conductive connector **120_1** while extending through the first upper insulating layer **171***a*. The second upper redistribution pattern **175_1** may be connected to the first upper redistribution pattern **173_1** while extending through the second upper insulating layer **171***b*. The upper pad **177_1** may be disposed on the second upper redistribution pattern **175_1** in the third upper insulating layer **171***c*.

FIG. **9** is an enlarged view showing a portion of a semiconductor package according to an example embodiment of the disclosure.

Referring to FIG. **9**, a connecting pad **139** of a semiconductor chip **130** may include a flat top surface **139**_U. For example, the top surface **139**_U of the connecting pad **139** may be coplanar with a top surface **137**_U of a second passivation layer **137**.

Lower redistribution patterns CP may be disposed on the connecting pad **139**. The lower redistribution patterns CP may include a first lower redistribution pattern **153_2**, a second lower redistribution pattern **155_2**, and a third lower redistribution pattern **157_2**. The first lower redistribution pattern **153_2** of FIG. **9** may be disposed on the top surface **139**_U of the connecting pad **139**. The first lower redistribution pattern **153_2** may be a conformal redistribution pattern formed by a conformal plating process. The first lower redistribution pattern **153_2** may include a first via **153***a*_2 and a first conductive pattern **153***b*_2. An outer side surface **153***a*_2OS of the first via **153***a*_2 may be completely covered by a first lower insulating layer **151***a*. A minimum distance H1" between the top surface **139**_U of the connecting pad **139** and the first conductive pattern **153***b*_2 may be about 3 to 10 μm. The first lower redistribution pattern **153_2** may have the same characteristics as the first lower redistribution pattern **153_2** described with reference to FIG. **4**, except that the first lower redistribution pattern **153_2** is disposed on the flat top surface **139**_U of the connecting pad **139**, and the outer side surface **153***a*_2OS of the first via **153***a*_2 is completely surrounded by the first lower insulating layer **151***a*. The second lower redistribution pattern **155_2** and the third lower redistribution pattern **157_2** may also have the same characteristics as the second lower redistribution pattern **155_2** and the third lower redistribution pattern **157_2** described with reference to FIG. **4**.

FIG. **10** is a sectional view of a semiconductor package according to an example embodiment of the disclosure.

Referring to FIG. **10**, a semiconductor package **100-2** may include a lower semiconductor package **100**A and an upper semiconductor package **100**B. The lower semiconductor package **100**A may include a semiconductor chip **130**, a mold layer **140_1**, conductive connectors **120_1**, a lower redistribution layer **150**, connecting terminals **138** and **160**, and an upper redistribution layer **171**/CP_U1.

The semiconductor chip **130** may include a die **131** and chip pads **133**. The chip pads **133** may be disposed on a bottom surface of the die **131**. The mold layer **140_1** may cover the semiconductor chip **130**. The mold layer **140_1** may cover a top surface of the lower redistribution layer **150**. The conductive connectors **120_1** may extend through the mold layer **140_1**, and thus may interconnect the lower redistribution layer **150** and the upper redistribution layer **171**/CP_U1.

The lower redistribution layer **150** may be connected to the semiconductor chip **130** via the connecting terminals **138**. The connecting terminals **138** may be disposed between the chip pads **133** of the semiconductor chip **130** and the lower redistribution layer **150**. The lower redistribution layer **150** may include lower insulating layers **151**, lower redistribution patterns CP, and UBMs **159**. The lower insulating layers **151** may include a first lower insulating layer **151***a*, a second lower insulating layer **151***b*, a third lower insulating layer **151***c*, and a fourth lower insulating layer **151***d*. The first to fourth lower insulating layers **151***a*, **151***b*, **151***c* and **151***d* may be sequentially stacked under the semiconductor chip **130** in a direction opposite to a first direction D1. Accordingly, the fourth lower insulating layer **151***d*, which is an uppermost layer, may contact the mold layer **140_1**. The lower redistribution patterns CP may include a first lower redistribution pattern **153**, a second lower redistribution pattern **155**, a third lower redistribution pattern **157**, and a fourth lower redistribution pattern **158**. The first to fourth lower redistribution patterns **153**, **155**, **157** and **158** may be sequentially stacked in the direction opposite to the first direction D1. A portion of the first lower redistribution pattern **153** may extend through the first lower insulating layer **151***a*. A portion of the first lower redistribution pattern **153** may be disposed on the first lower insulating layer **151***a*. A portion of the second redistribution pattern **155** may be connected to the first lower redistribution pattern **153** while extending through the second lower insulating layer **151***b*. A portion of the second lower redistribution pattern **155** may be disposed on the second lower insulating layer **151***b*. A portion of the third lower redistribution pattern **157** may be connected to the second lower redistribution pattern **155** while extending through the third lower insulating layer **151***c*. A portion of the third lower redistribution pattern **157** may be disposed on the third lower insulating layer **151***c*. A portion of the fourth lower redistribution pattern **158** may be connected to the third lower redistribution pattern **157** while extending through the fourth lower insulating layer **151***d*. A portion of the fourth lower redistribution pattern **158** may be disposed on the fourth lower insulating layer **151***d*. The fourth lower redistribution pattern **158** may be connected to the connecting terminal **138**, and thus may be electrically connected to the semiconductor chip **130** via the connecting terminal **138**. The fourth lower redistribution pattern **158** may contact the mold layer **140_1**. The UBMs **159** may be disposed in the first lower insulating layer **151***a*. The UBMs **159** may be connected to the first lower redistribution pattern **153**. The first lower redistribution pattern **153** may be connected to top surfaces of the UBMs **159**. Bottom surfaces of the UBMs **159** may be exposed by the first lower insulating layer **151***a*. Connecting terminals **160** may be disposed on the bottom surfaces of the UBMs **159**.

One or two of the first to fourth lower redistribution patterns **153**, **155**, **157** and **158** may be a conformal redistribution pattern formed by a conformal plating process, and the remaining three or two of the first to fourth lower redistribution patterns **153**, **155**, **157** and **158** may be a filled

redistribution pattern formed by a fill plating process. The lower redistribution patterns CP of FIG. **10** may include the first to third lower redistribution patterns **153**, **155** and **157**, and may not include the fourth lower redistribution pattern **158**. In this case, the lower insulating layers **151** may include the first to third insulating layers **151***a*, **151***b* and **151***c*, and may not include the fourth lower insulating layer **151***d*. The lower redistribution patterns CP of FIG. **10** may have the characteristics of the lower redistribution patterns CP described with reference to FIGS. **2** to **7**. The lower redistribution patterns CP of FIG. **10** may be different from the lower redistribution patterns CP of FIGS. **2** to **7** only in that the first lower redistribution pattern **1532** contacts the UBMs **159** other than the connecting pad **139**, the third lower redistribution pattern **157** or the fourth lower redistribution pattern **158** contacts the connecting terminals **138** other than the UBMs **159**.

FIG. **11** is an enlarged view of a portion of a semiconductor package according to an example embodiment of the disclosure.

Referring to FIG. **11**, a UBM **159** may be disposed in a first lower insulating layer **151***a*. A bottom surface of the UBM **159** may be coplanar with a bottom surface of the first lower insulating layer **151***a*. A connecting terminal **160** may be disposed on the bottom surface of the UBM **159**.

Lower redistribution patterns CP may include a first lower redistribution pattern **153_2**, a second lower redistribution pattern **155_2**, a third lower redistribution pattern **157_2**, and a fourth lower redistribution pattern **158**. The first lower redistribution pattern **153_2** may be disposed on the UBM **159** disposed in the first lower insulating layer **151***a*. The first lower redistribution pattern **153_2** may be a conformal redistribution pattern formed by a conformal plating process. The first lower redistribution pattern **153_2** may include a first via **153***a*_2 and a first conductive pattern **153***b*_2. An outer side surface **153***a*_2OS of the first via **153***a*_2 may completely contact the first lower insulating layer **151***a*. A minimum distance H1''' between the UBM **159** and the first conductive pattern **153***b*_2 may be about 3 to 10 μm. The first lower redistribution pattern **153_2** may have the same characteristics as the first lower redistribution pattern **153_2** described with reference to FIG. **4**, except that the first lower redistribution pattern **153_2** is disposed on the UBM **159** such that the outer side surface **153***a*_2OS of the first via **153***a*_2 is completely surrounded by the first lower insulating layer **151***a*. Further, the second lower redistribution pattern **155_2** and the third lower redistribution pattern **157_2** may have the same characteristics as the second lower redistribution pattern **155_2** and the third lower redistribution pattern **157_2** described with reference to FIG. **4**. The fourth lower redistribution pattern **158** may be disposed on the third lower redistribution pattern **157_2**, and may be a filled redistribution pattern or a conformal redistribution pattern. The fourth lower redistribution pattern **158** may include a fourth via **158***a* and a fourth conductive pattern **158***b*. The fourth via **158***a* may be connected to the third lower redistribution pattern **157_2** while extending through the fourth lower insulating layer **151***d*. The fourth conductive pattern **158***b* may be disposed on the fourth via **158***a*, and may be connected to the connecting terminal **160**.

In accordance with the example embodiments of the disclosure, a redistribution layer having a stack via structure, in which a plurality of vias is vertically stacked, may include a filled redistribution pattern and a conformal redistribution pattern, and thus may alleviate stress caused by a coefficient of thermal expansion difference between a semiconductor chip and the stack via structure. Accordingly, a semiconductor package having enhanced reliability may be provided.

While the above example embodiments of the disclosure have been described with reference to the accompanying drawings, it should be understood by those skilled in the art that various modifications may be made without departing from the scope of the disclosure and without changing essential features thereof. Therefore, the above-described example embodiments should be considered in a descriptive sense only and not for purposes of limitation.

What is claimed is:

1. A semiconductor package comprising:

a semiconductor chip comprising a connecting pad;

a mold layer covering the semiconductor chip;

a lower redistribution layer on the semiconductor chip and the mold layer; and

a connecting terminal on the lower redistribution layer,

wherein the lower redistribution layer comprises

a first lower insulating layer,

a first conformal redistribution pattern extending through the first lower insulating layer, the first conformal redistribution pattern including a top horizontal portion, a bottom horizontal portion, and a connecting portion interconnecting the top horizontal portion and the bottom horizontal portion,

a second lower insulating layer on the first lower insulating layer and the first conformal redistribution pattern, and

a first filled redistribution pattern on the first conformal redistribution pattern, the first filled redistribution pattern extending through the second lower insulating layer, the first filled redistribution pattern including a via and a conductive pattern, the via being a filled pattern extending through the second lower insulating layer, an entirety of a top surface of the via being in contact with the conductive pattern, the conductive pattern extending horizontally on the second lower insulating layer,

wherein a side surface of the first filled redistribution pattern is spaced apart from an inner side surface of the connecting portion of the first conformal redistribution pattern, and

wherein the second lower insulating layer is between the inner side surface of the first conformal redistribution pattern and the side surface of the first filled redistribution pattern.

2. The semiconductor package according to claim **1**, wherein:

the first conformal redistribution pattern comprises a first via and a first conductive pattern;

the first via comprises a top surface and a side surface that define a recess; and

the second lower insulating layer contacts the top surface of the first via and filling the recess of the first via.

3. The semiconductor package according to claim **2**, wherein the second lower insulating layer completely covers the side surface of the first via.

4. The semiconductor package according to claim **2**, wherein:

the first filled redistribution pattern comprises a second via and a second conductive pattern; and

a side surface of the second via is spaced apart from the side surface of the first via.

5. The semiconductor package according to claim **4**, wherein the second lower insulating layer completely surrounds the side surface of the second via.

6. The semiconductor package according to claim 2, wherein:

the connecting pad comprises a first top surface, a second top surface, and a side surface interconnecting the first top surface and the second top surface; and

the first conformal redistribution pattern completely covers the first top surface and the side surface of the connecting pad.

7. The semiconductor package according to claim 6, wherein a minimum distance between the second top surface of the connecting pad and a bottom surface of the first conductive pattern is about 3 to 10 μm.

8. The semiconductor package according to claim 1, further comprising:

a third lower insulating layer on the second lower insulating layer; and

a second conformal redistribution pattern being on the first filled redistribution pattern and extending through the third lower insulating layer.

9. The semiconductor package according to claim 1, further comprising:

a third lower insulating layer on the second lower insulating layer;

a second filled redistribution pattern being on the first filled redistribution pattern and extending through the third lower insulating layer; and

a second conformal redistribution pattern being on the second filled redistribution pattern.

10. The semiconductor package according to claim 8, further comprising:

a fourth lower insulating layer being on the second conformal redistribution pattern and filling a recess of the second conformal redistribution pattern.

11. The semiconductor package according to claim 10, further comprising:

a second filled redistribution pattern being on the second conformal redistribution pattern and extending through the fourth lower insulating layer.

12. The semiconductor package according to claim 11, wherein:

the second conformal redistribution pattern comprises a first via and a first conductive pattern;

the first via comprises a top surface and a side surface that define a recess; and

the fourth lower insulating layer contacts the top surface of the first via and fills the recess of the first via.

13. The semiconductor package according to claim 12, wherein:

the second filled redistribution pattern comprises a second via and a second conductive pattern; and

a side surface of the second via is spaced apart from the side surface of the first via.

14. The semiconductor package according to claim 13, wherein the fourth lower insulating layer is between the side surface of the first via and the side surface of the second via.

15. The semiconductor package according to claim 13, wherein the fourth lower insulating layer completely surrounds the side surface of the second via.

16. A semiconductor package comprising:

a base layer comprising an opening;

a conductive connector extending through the base layer;

a semiconductor chip in the opening;

a mold layer covering a top surface of each of the base layer and the semiconductor chip; and

a lower redistribution layer on the base layer, the semiconductor chip and the mold layer,

wherein the semiconductor chip comprises a die, a chip pad on the die, and a connecting pad on the chip pad, the connecting pad comprising a first horizontal top surface, a second horizontal top surface, and an inner side surface interconnecting the first horizontal top surface and the second horizontal top surface,

wherein the lower redistribution layer comprises

a first lower insulating layer on the semiconductor chip,

a first lower redistribution pattern extending through the first lower insulating layer, the first lower redistribution pattern comprising a first via and a first conductive pattern, the first via extending through the first lower insulating layer and being in contact with the first horizontal top surface of the connecting pad, and the first conductive pattern being on the first via and extending horizontally on the first lower insulating layer, and

a second lower redistribution pattern on the first lower redistribution pattern,

wherein a side surface of the first via is spaced apart from the inner side surface of the connecting pad, and

wherein the first lower insulating layer is between the side surface of the first via and the inner side surface of the connecting pad.

17. The semiconductor package according to claim 16, wherein the first lower insulating layer contacts a portion of the first horizontal top surface of the connecting pad and the inner side surface of the connecting pad.

18. The semiconductor package according to claim 16, wherein the first lower insulating layer completely surrounds the side surface of the first via.

19. The semiconductor package according to claim 16, wherein the second lower redistribution pattern is a conformal redistribution pattern or a filled redistribution pattern.

20. A semiconductor package comprising:

a semiconductor chip comprising a chip pad;

a mold layer covering the semiconductor chip;

a lower redistribution layer on a bottom surface of the mold layer; and

a conductive connector connected to the lower redistribution layer and extending through the mold layer,

wherein the lower redistribution layer comprises,

an under bump metal (UBM),

a first lower insulating layer covering the UBM,

a first conformal redistribution pattern on the UBM, the first conformal redistribution pattern extending through the first lower insulating layer, the first conformal redistribution pattern including a top horizontal portion, a bottom horizontal portion, and a connecting portion interconnecting the top horizontal portion and the bottom horizontal portion,

a second lower insulating layer on the first conformal redistribution pattern; and

a first filled redistribution pattern on the first conformal redistribution pattern, the first filled redistribution pattern extending through the second lower insulating layer, the first filled redistribution pattern including a via and a conductive pattern, the via being a filled pattern extending through the second lower insulating layer, an entirety of a top surface of the via being in contact with the conductive pattern, the conductive pattern extending horizontally on the second lower insulating layer,

wherein a side surface of the first filled redistribution pattern is spaced apart from an inner side surface of the connecting portion of the first conformal redistribution pattern, and

wherein the second lower insulating layer is between the inner side surface of the first conformal redistribution pattern and the side surface of the first filled redistribution pattern.

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