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(54) **WIRE BOND WIRES FOR INTERFERENCE SHIELDING**

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H01L 23/00 (2006.01)
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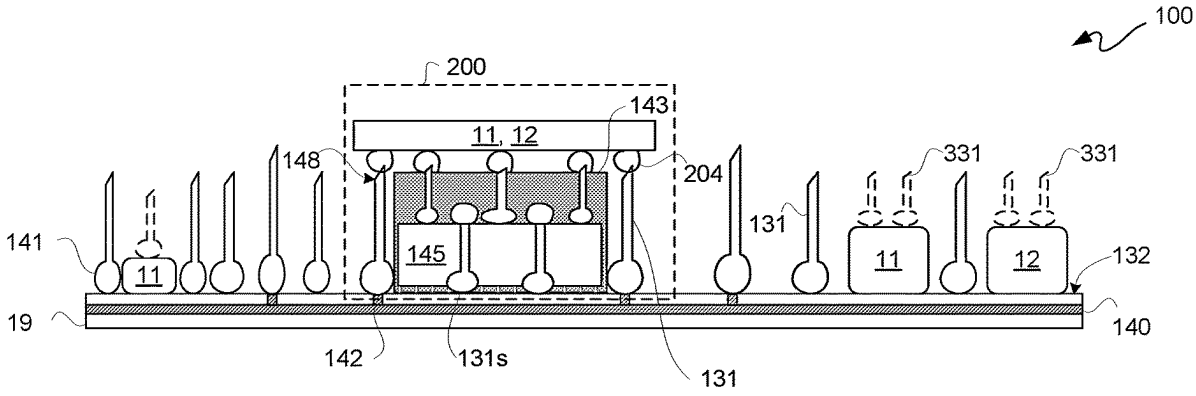
(Continued)

(57) **ABSTRACT**

Apparatuses relating generally to a microelectronic package having protection from interference are disclosed. In an apparatus thereof, a substrate has an upper surface and a lower surface opposite the upper surface and has a ground plane. A first microelectronic device is coupled to the upper surface of the substrate. Wire bond wires are coupled to the ground plane for conducting the interference thereto and extending away from the upper surface of the substrate. A first portion of the wire bond wires is positioned to provide a shielding region for the first microelectronic device with respect to the interference. A second portion of the wire bond wires is not positioned to provide the shielding region. A second microelectronic device is coupled to the substrate and located outside of the shielding region. A conductive surface is over the first portion of the wire bond wires for covering the shielding region.



Related U.S. Application Data

continuation of application No. 17/893,725, filed on Aug. 23, 2022, now Pat. No. 11,810,867, which is a continuation of application No. 16/715,524, filed on Dec. 16, 2019, now Pat. No. 11,462,483, which is a continuation of application No. 16/127,110, filed on Sep. 10, 2018, now Pat. No. 10,559,537, which is a continuation of application No. 15/804,122, filed on Nov. 6, 2017, now Pat. No. 10,115,678, which is a continuation of application No. 15/344,990, filed on Nov. 7, 2016, now Pat. No. 9,812,402, which is a continuation of application No. 14/880,967, filed on Oct. 12, 2015, now Pat. No. 9,490,222.

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H01L 25/065	(2023.01)
H01L 25/10	(2006.01)

(52) **U.S. Cl.**

CPC *H01L 2924/20751* (2013.01); *H01L 2924/20754* (2013.01); *H01L 2924/3025* (2013.01)

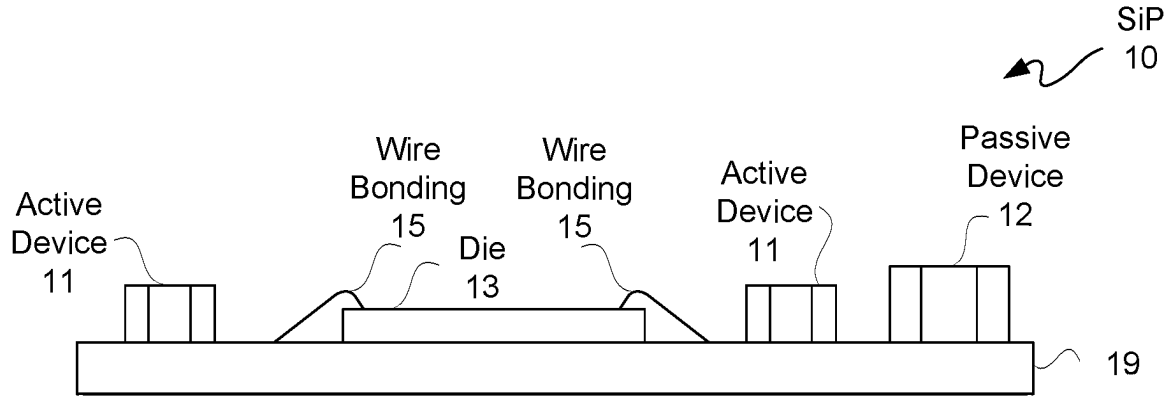

FIG. 1A
(Prior Art)

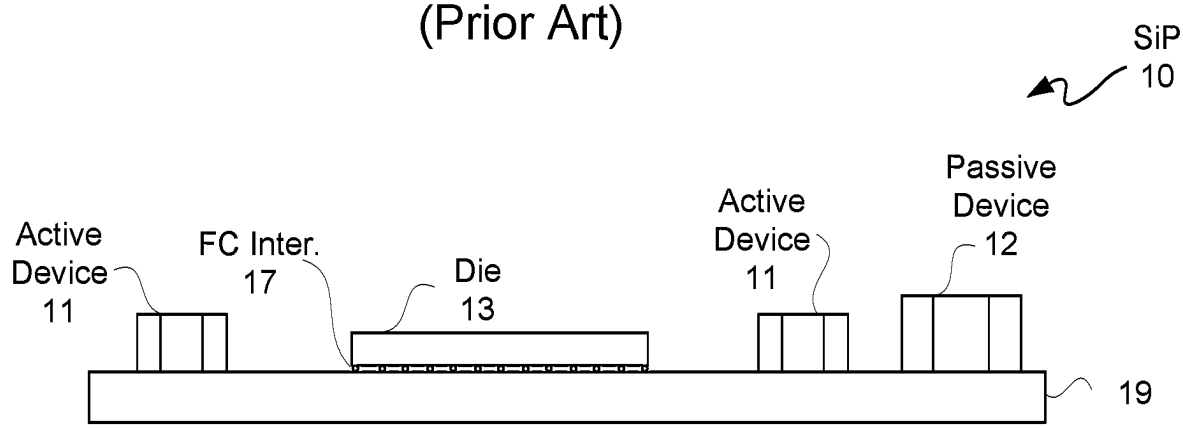

FIG. 1B
(Prior Art)

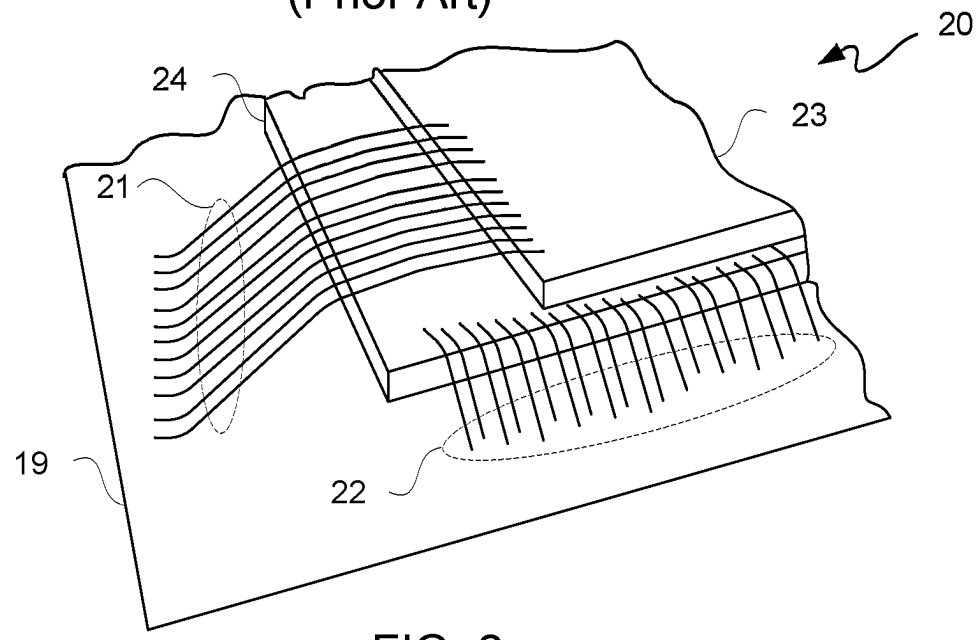

FIG. 2
(Prior Art)

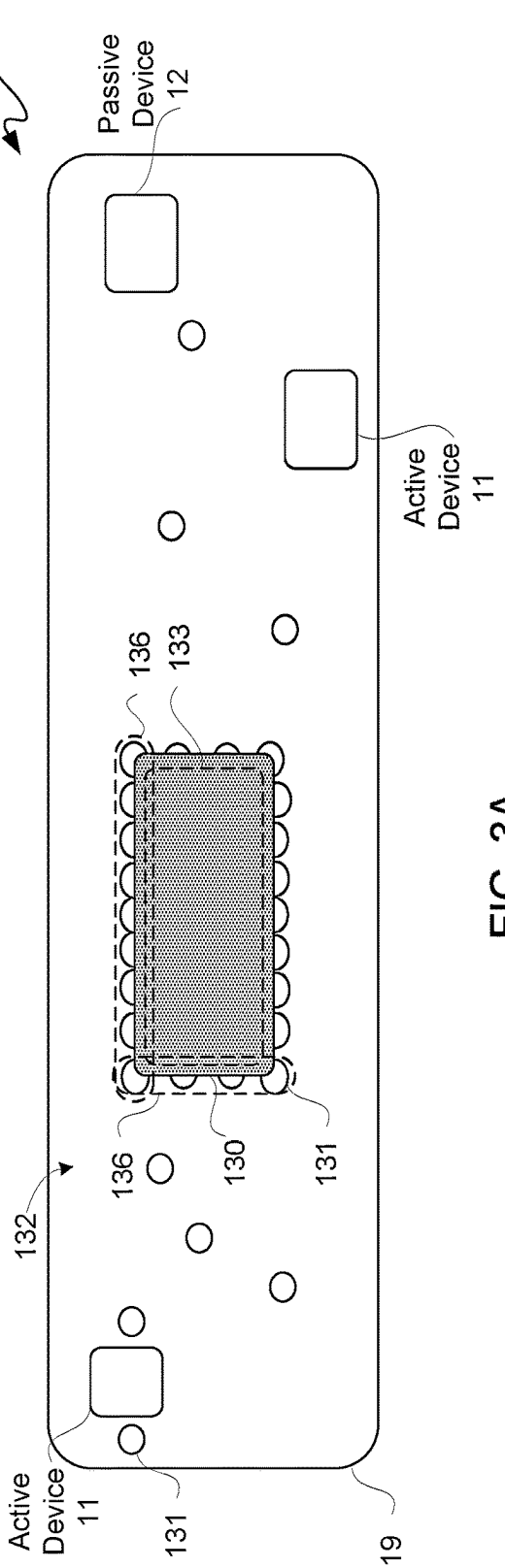
100
Passive Device 12
Active Device 11
136
133
132
136
130
131
Active Device 11
131
19

FIG. 3A

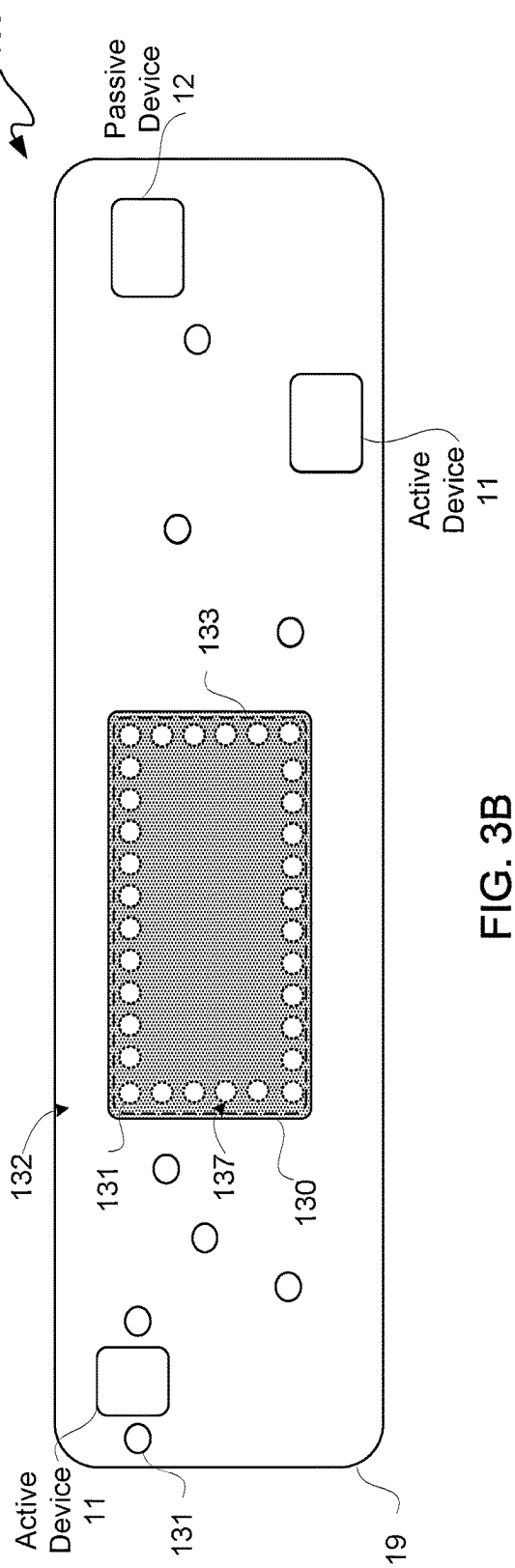
100
Passive Device 12
Active Device 11
133
132
131
137
130
Active Device 11
131
19

FIG. 3B

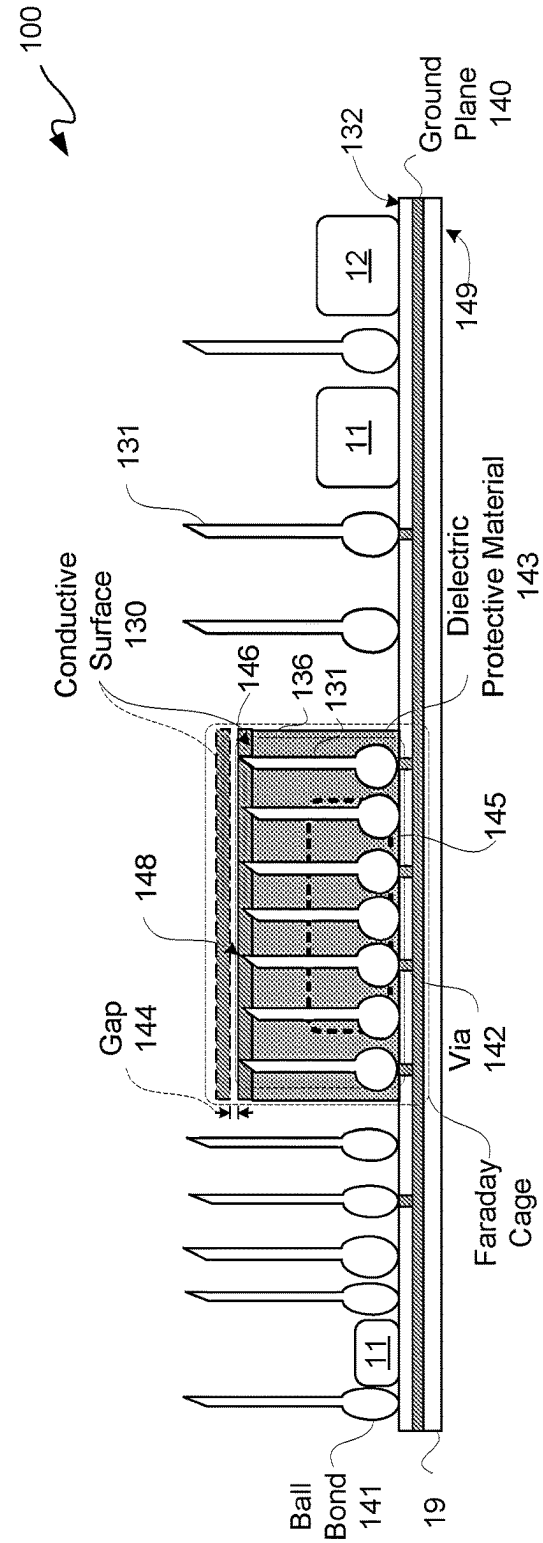
100
Ground Plane 140
132
12
149
131
11
Conductive Surface 130
146
136
131
Dielectric Protective Material 143
148
145
Gap 144
Via 142
Faraday Cage 153
11
Ball Bond 141
19

FIG. 4

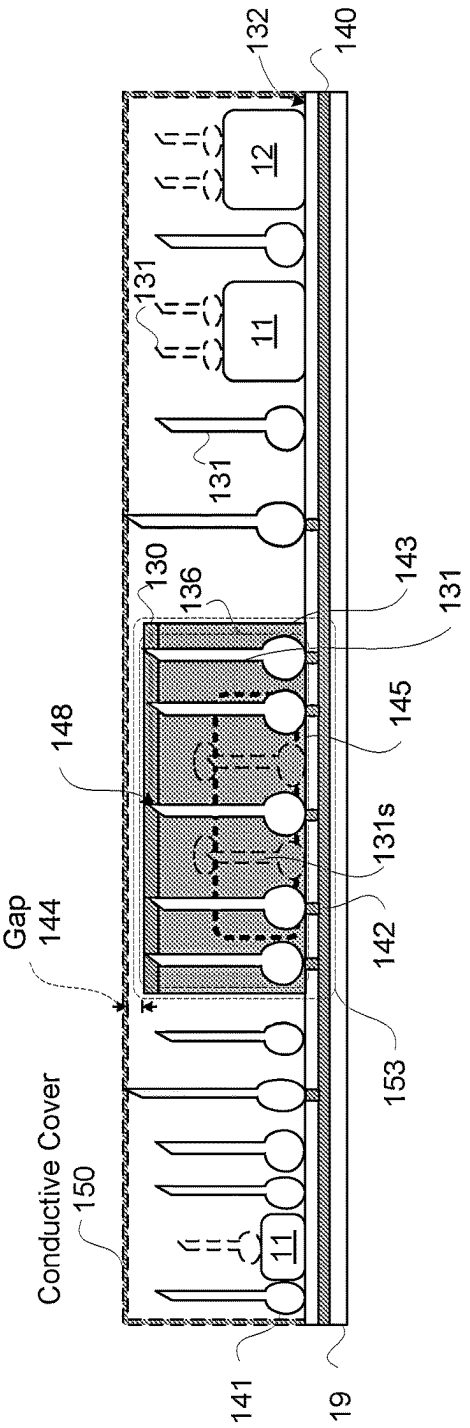
132
140
12
131
11
131
130
136
143
131
148
145
131s
Gap 144
142
153
Conductive Cover 150
11
141
19

FIG. 5

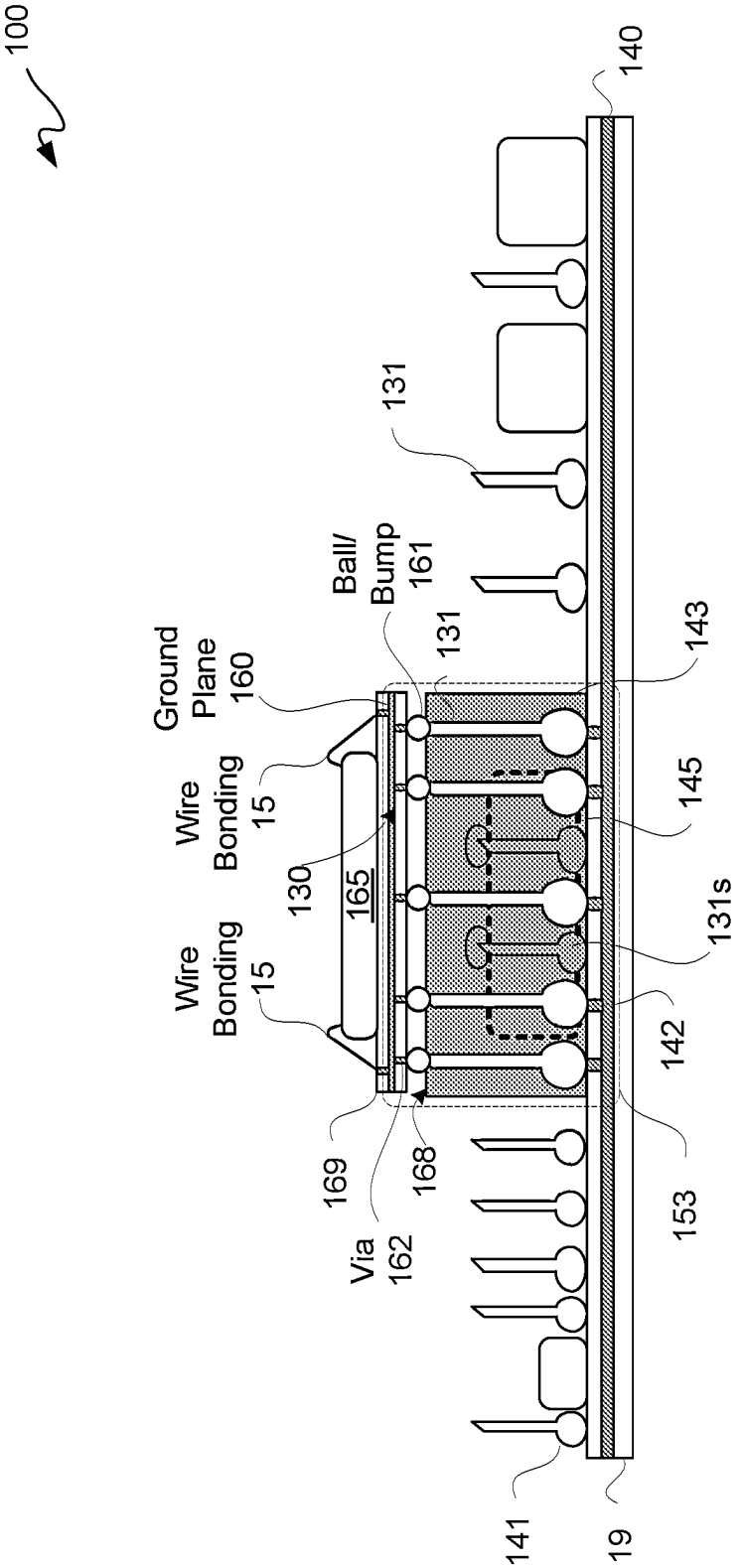
100
140
131
Ball/
Bump
161
131
143
Ground
Plane
160
Wire
Bonding
15
145
130
165
131s
Wire
Bonding
15
142
169
168
153
Via
162
141
19

FIG. 6

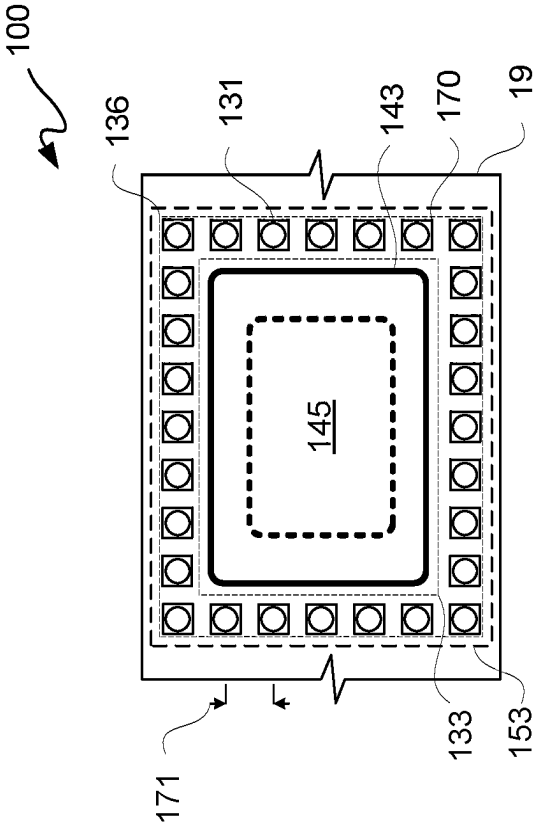
100
136
131
143
170
19
145
171
133
153

FIG. 7

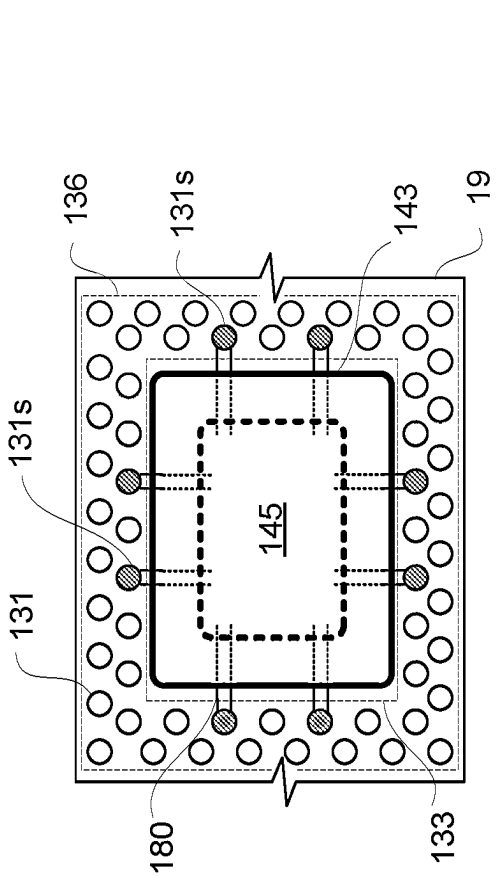
100
136
131s
143
19
131s
145
131
180
133

FIG. 8

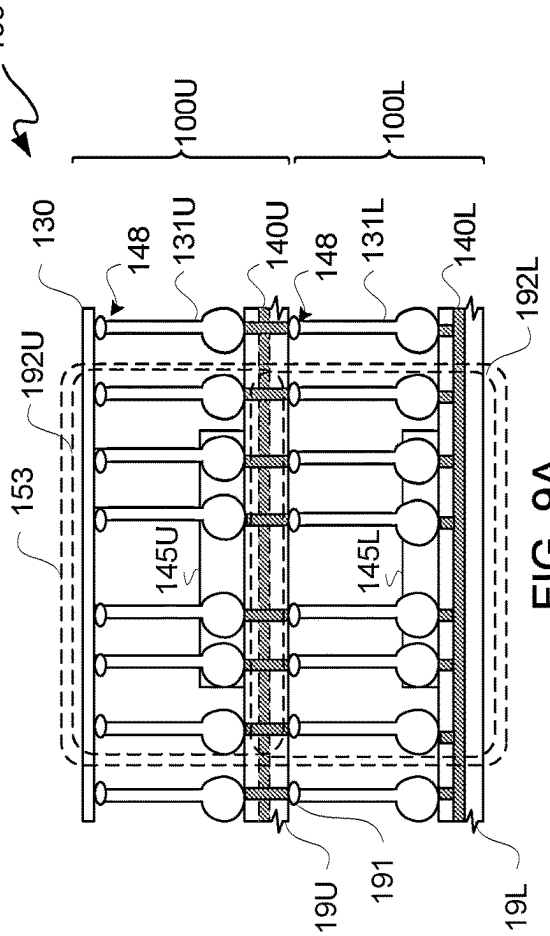
190
100U
100L
130
148
131U
140U
148
131L
140L
192L
192U
153
145U
145L
19U
191
19L

FIG. 9A

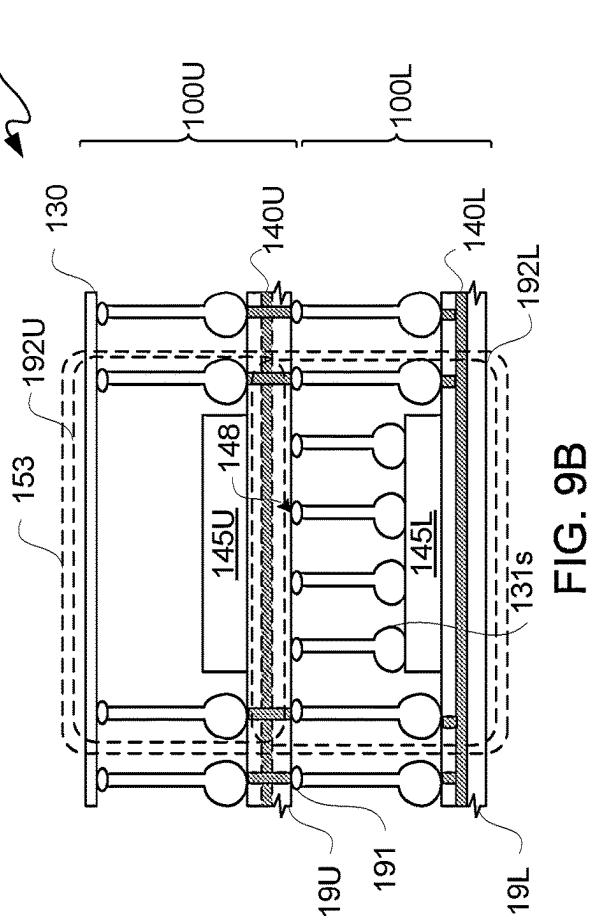
190
100U
100L
130
140U
140L
192L
192U
153
148
145U
145L
131s
19U
191
19L

FIG. 9B

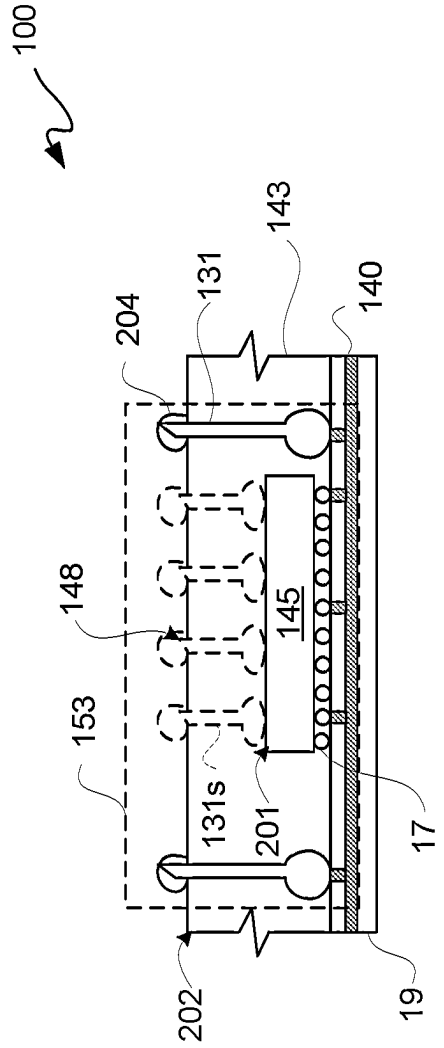

FIG. 10

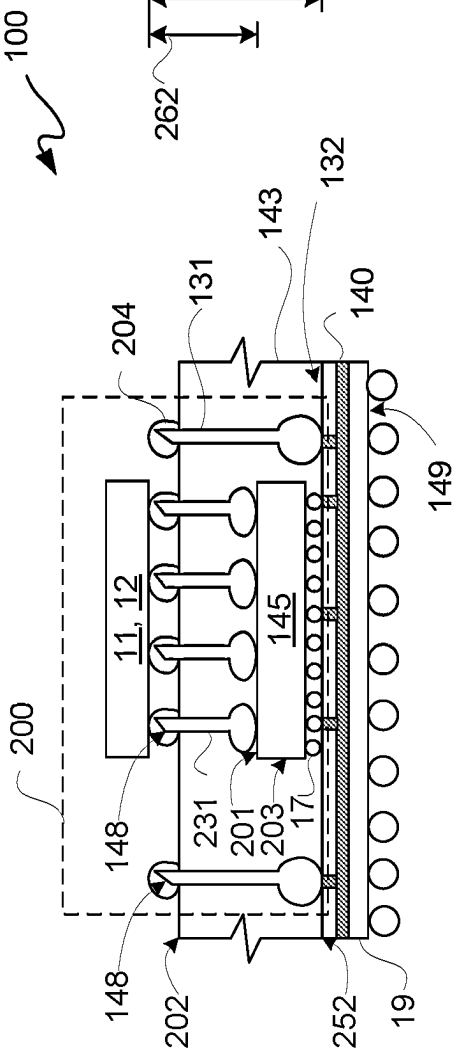

FIG. 11A

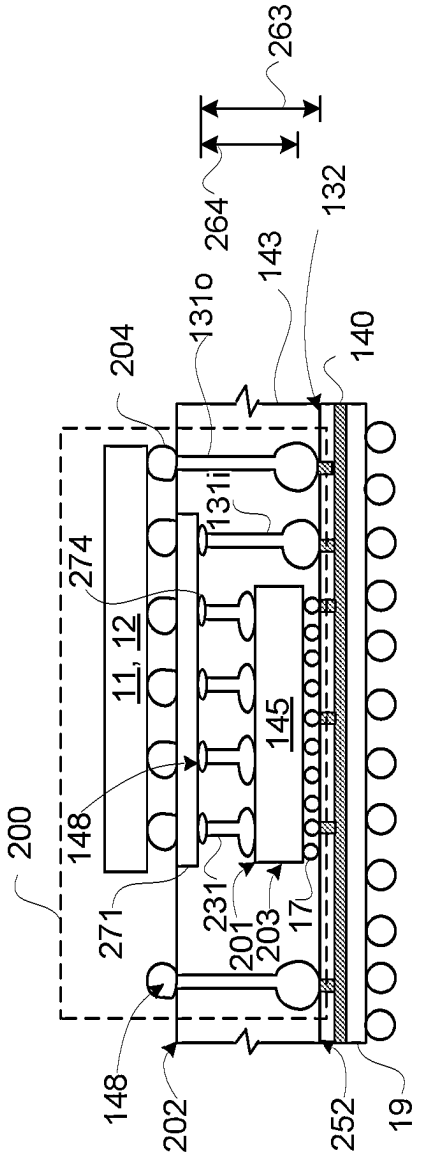

FIG. 11B

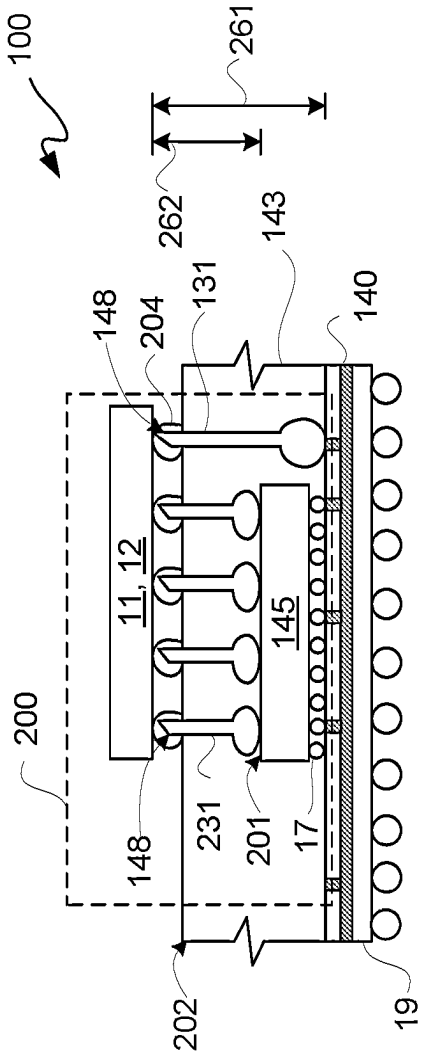

FIG. 12A

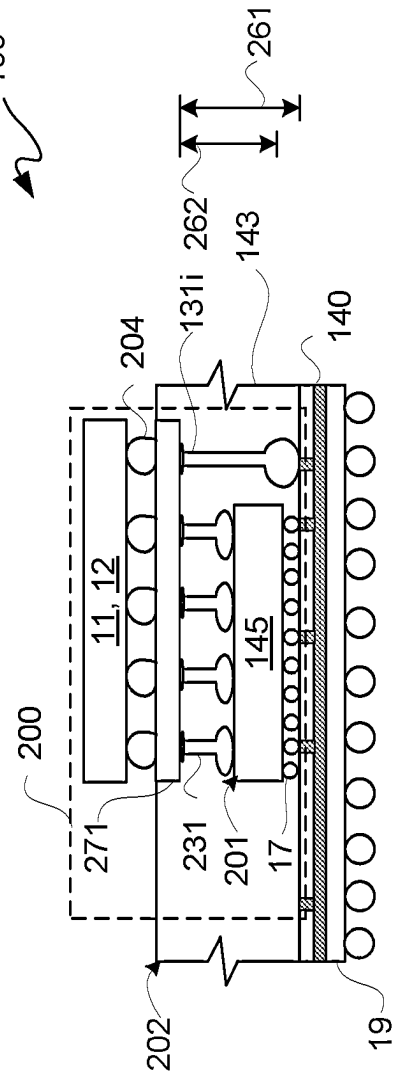

FIG. 12B

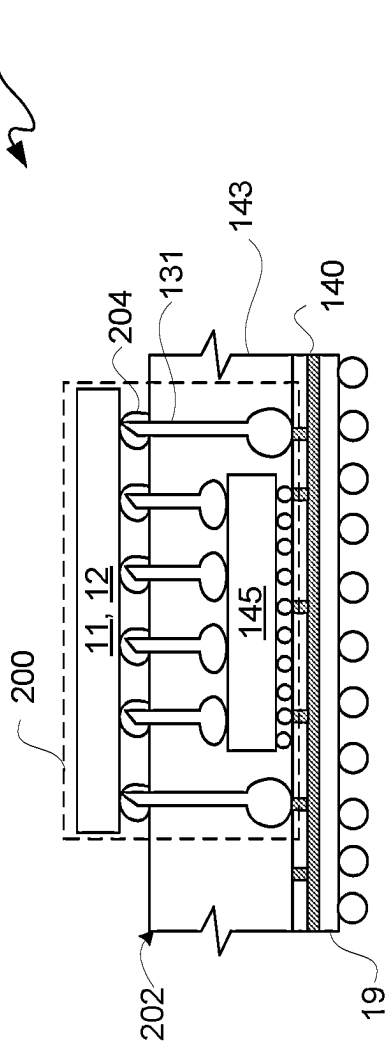

FIG. 12C

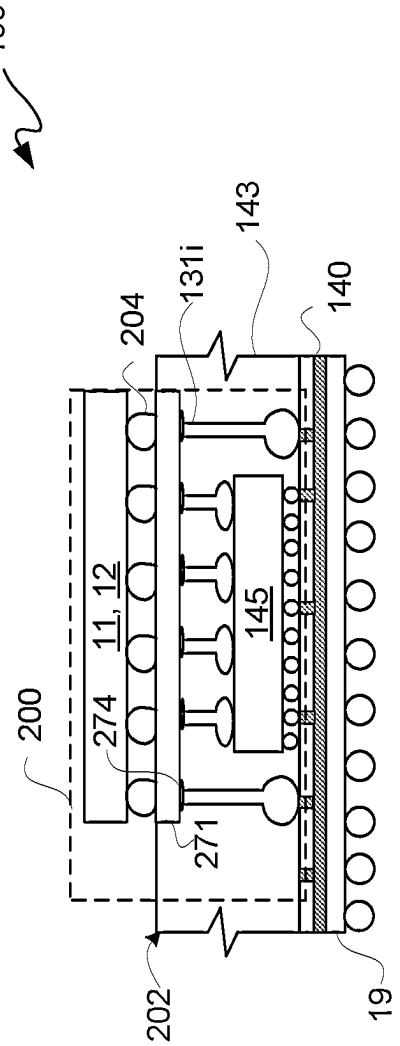

FIG. 12D

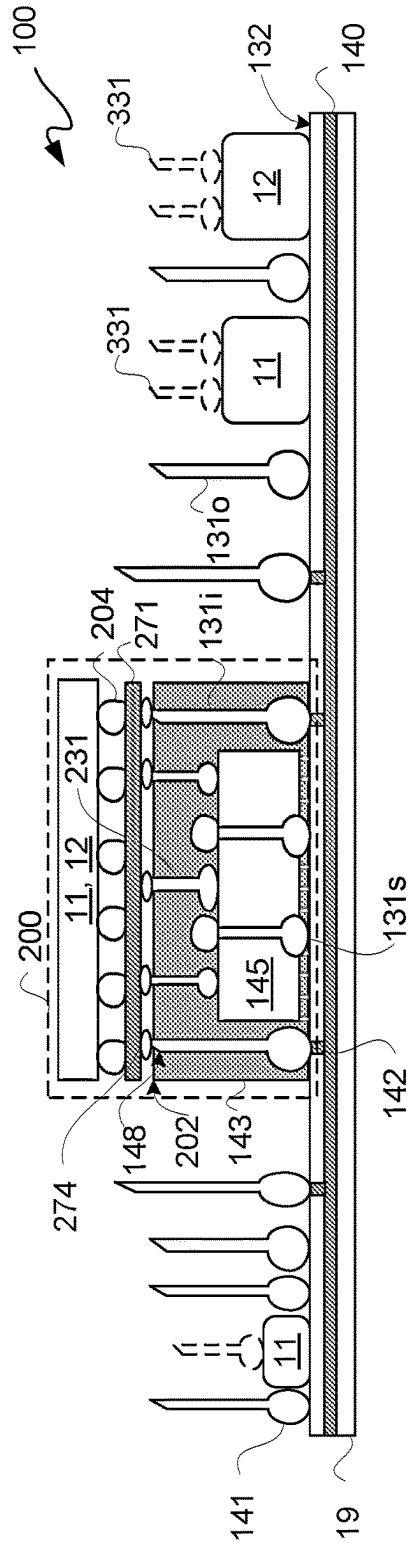

FIG. 13A

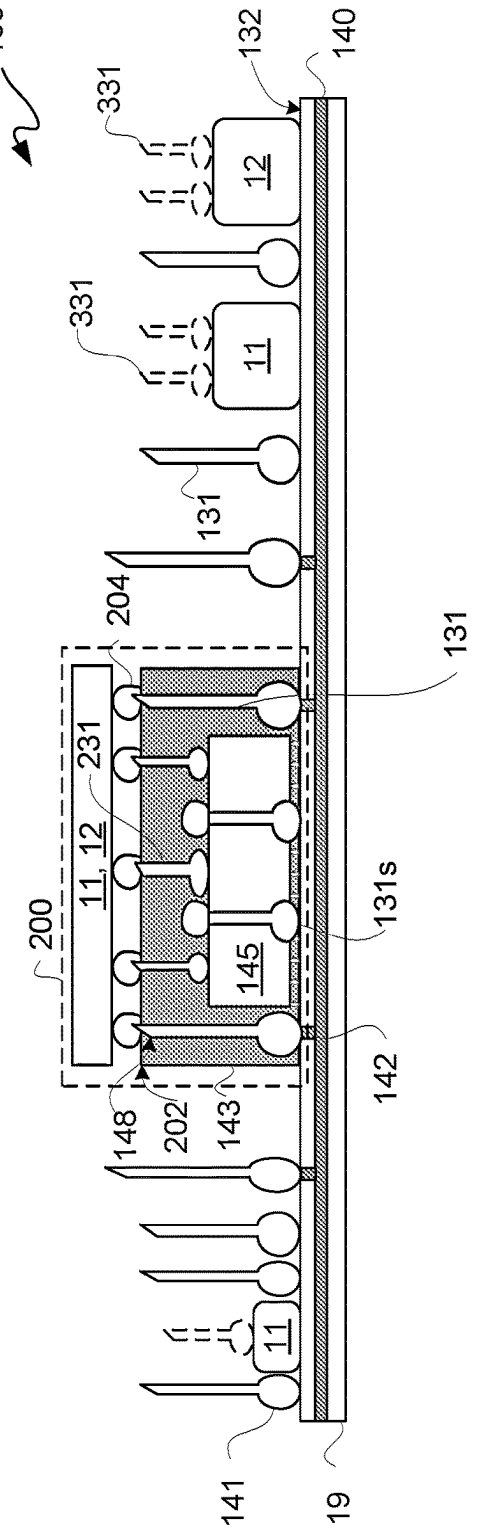

FIG. 13B

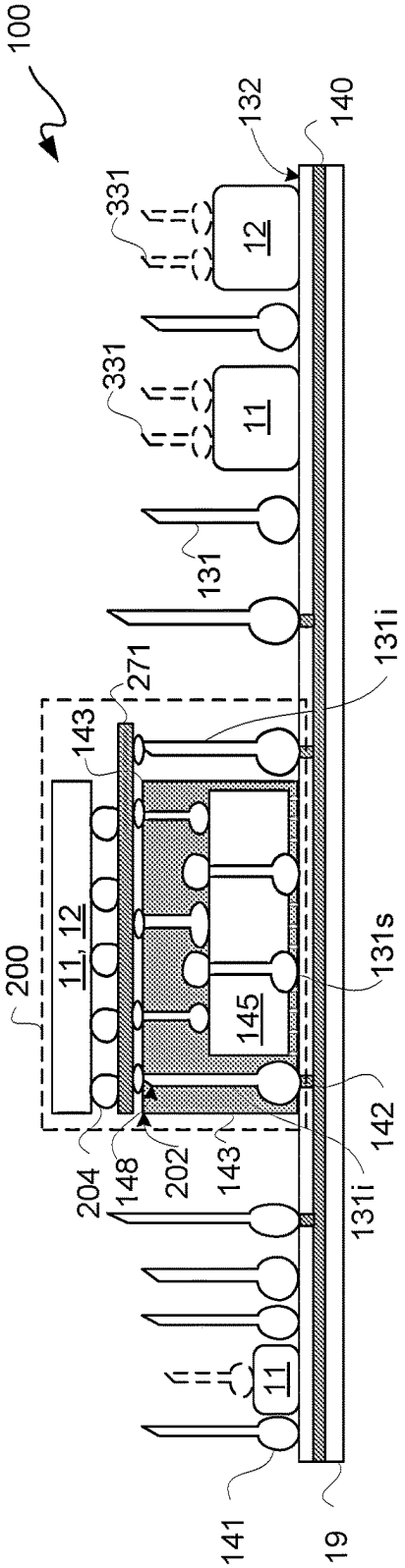

FIG. 13C

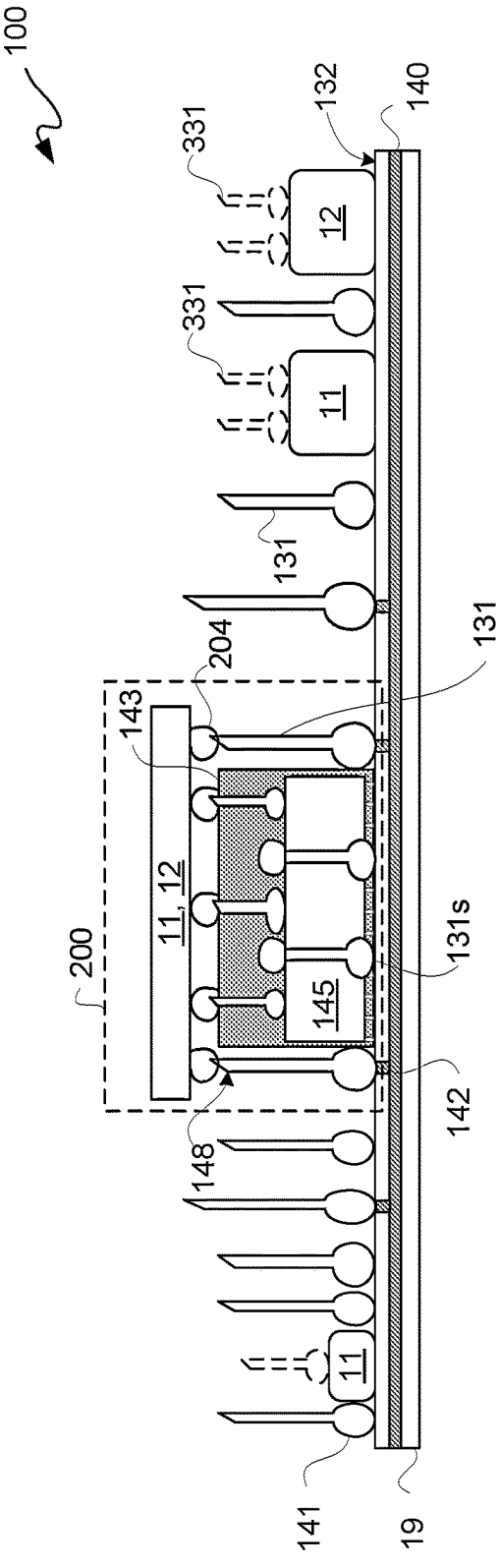

FIG. 13D

WIRE BOND WIRES FOR INTERFERENCE SHIELDING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of and hereby claims priority to U.S. patent application Ser. No. 16/127,110, filed Sep. 10, 2018, which is a continuation of U.S. Pat. No. 10,115,678, which is a continuation of U.S. Pat. No. 9,812,402, which is a continuation of U.S. Pat. No. 9,490,222, filed on Oct. 12, 2015, the entirety of each of which is hereby incorporated by reference herein for all purposes.

FIELD

[0002] The following description relates generally to wire bond wires for vertical interconnection and/or interference shielding.

BACKGROUND

[0003] Microelectronic assemblies generally include one or more ICs, such as for example one or more packaged dies ("chips") or one or more dies. One or more of such ICs may be mounted on a circuit platform, such as a wafer such as in wafer-level-packaging ("WLP"), printed board ("PB"), a printed wiring board ("PWB"), a printed circuit board ("PCB"), a printed wiring assembly ("PWA"), a printed circuit assembly ("PCA"), a package substrate, an interposer, or a chip carrier. Additionally, one IC may be mounted on another IC. An interposer may be a passive or an active IC, where the latter includes one or more active devices, such as transistors for example, and the former does not include any active device but may include one or more passive devices, such as capacitors, inductors, and/or resistors. Furthermore, an interposer may be formed like a PWB, namely without any circuit elements, such as without any passive or active devices. Additionally, an interposer may include at least one through-substrate-via

[0004] An IC may include conductive elements, such as pathways, traces, tracks, vias, contacts, pads such as contact pads and bond pads, plugs, nodes, or terminals for example, that may be used for making electrical interconnections with a circuit platform. These arrangements may facilitate electrical connections used to provide functionality of ICs. An IC may be coupled to a circuit platform by bonding, such as bonding traces or terminals, for example, of such circuit platform to bond pads or exposed ends of pins or posts or the like of an IC; or an IC may be coupled to a circuit platform by soldering. Additionally, a redistribution layer ("RDL") may be part of an IC to facilitate a flip-chip configuration, die stacking, or more convenient or accessible position of bond pads for example.

[0005] Some passive or active microelectronic devices may be shielded from electric-magnetic interference ("EMI") and/or radio frequency interference ("RFI"). However, conventional shielding may be complicated to fabricate, too heavy for some mobile applications, and/or too large for some low-profile applications. Moreover, some shielding may not be suitable for a stacked die or stacked package, generally referred to as three-dimensional ("3D") ICs or "3D ICs."

[0006] Accordingly, it would be desirable and useful to provide interference shielding that provides an improvement over conventional interference shielding.

BRIEF SUMMARY

[0007] An apparatus relates generally to a microelectronic package having protection from interference. In such an apparatus, a substrate has an upper surface and a lower surface opposite the upper surface and has a ground plane. A first microelectronic device is coupled to the upper surface of the substrate. Wire bond wires are coupled to the ground plane for conducting the interference thereto and extending away from the upper surface of the substrate. A first portion of the wire bond wires is positioned to provide a shielding region for the first microelectronic device with respect to the interference. A second portion of the wire bond wires is not positioned to provide the shielding region. A second microelectronic device is coupled to the substrate and located outside of the shielding region. A conductive surface is over the first portion of the wire bond wires for covering the shielding region.

[0008] An apparatus relates generally to another microelectronic package having protection from interference. In such an apparatus, a substrate has an upper surface and a lower surface opposite the upper surface and has a ground plane. A microelectronic device is coupled to the upper surface of the substrate. Wire bond wires are bonded to and extend away from the upper surface of the substrate. A first portion of the wire bond wires have a first height and are positioned proximate to and around the first microelectronic device for providing a shielding region for the first microelectronic device with respect to the interference. The first portion of the wire bond wires are coupled to the ground plane for conducting the interference thereto. A second portion of the wire bond wires have a second height, which is less than the first height, and are positioned proximate to and around the first microelectronic device. The second portion of the wire bond wires include signal wires for electrically coupling the microelectronic device with the substrate. A conductive surface is over the wire bond wires for covering the shielding region. Upper ends of the first portion of the wire bond wires are mechanically coupled to the conductive surface.

[0009] An apparatus relates generally to yet another microelectronic package having protection from interference. In such an apparatus, a substrate has an upper surface and a lower surface opposite the upper surface and has a ground plane. A first microelectronic device is coupled to the upper surface of the substrate. Lower ends of wire bond wires are coupled to the ground plane for conducting the interference thereto. A first portion of the wire bond wires is positioned to provide a shielding region for the first microelectronic device with respect to the interference. A second portion of the wire bond wires is not positioned to provide the shielding region. A second microelectronic device is coupled to the substrate and located outside of the shielding region. A conductive surface has the first portion of the wire bond wires coupled thereto. The conductive surface covers the shielding region and defines the shielding region with the first portion of the wire bond wires extending away from the conductive surface.

BRIEF DESCRIPTION OF THE DRAWING(S)

[0010] Accompanying drawing(s) show exemplary embodiment(s) in accordance with one or more aspects of exemplary apparatus(es) or method(s). However, the accom-

panying drawings should not be taken to limit the scope of the claims, but are for explanation and understanding only.

[0011] FIG. **1**A is a block diagram of a side view depicting an exemplary conventional system-in-package ("SiP") without electric-magnetic interference ("EMI") shielding.

[0012] FIG. **1**B is a block diagram of a side view depicting another exemplary conventional SiP without EMI shielding.

[0013] FIG. **2** is a corner top-down perspective view depicting an exemplary portion of a conventional EMI shielding.

[0014] FIGS. **3**A and **3**B are top views of block diagrams depicting respective exemplary SiPs with EMI shielding.

[0015] FIG. **4** is a block diagram of a cross-sectional side view depicting an exemplary SiP with EMI shielding.

[0016] FIG. **5** is a block diagram of a cross-sectional side view depicting an exemplary SiP with a conductive cover and with signal wire bond wires in an EMI shielding region under the conductive cover.

[0017] FIG. **6** is a block diagram of a cross-sectional side view depicting an exemplary SiP with EMI shielding using an upper substrate.

[0018] FIG. **7** is a block diagram of a top-down view depicting an exemplary portion of an SiP prior to addition of an upper conductive surface of a Faraday cage.

[0019] FIG. **8** is a block diagram of a top-down view depicting an exemplary portion of another SiP prior to addition of an upper conductive surface of a Faraday cage.

[0020] FIG. **9**A is a block diagram of a cross-sectional side view depicting an exemplary portion of a package-on-package ("POP") device with EMI shielding.

[0021] FIG. **9**B is a block diagram of a cross-sectional side view depicting an exemplary portion of another POP device with EMI shielding.

[0022] FIG. **10** is a block diagram of a cross-sectional side view depicting an exemplary portion of another SiP with EMI shielding.

[0023] FIG. **11**A is a block diagram of a cross-sectional side view depicting an exemplary portion of an SiP without wire bond wire EMI shielding.

[0024] FIG. **11**B is a block diagram of a cross-sectional side view depicting an exemplary portion of another SiP without wire bond wire EMI shielding.

[0025] FIGS. **12**A through **12**D are respective block diagrams of cross-sectional side views depicting exemplary portions of respective SiPs without wire bond wire EMI shielding.

[0026] FIGS. **13**A through **13**D are respective block diagrams of cross-sectional side views depicting exemplary portions of respective SiPs without wire bond wire EMI shielding and with vertically integrated microelectronic packages.

DETAILED DESCRIPTION

[0027] In the following description, numerous specific details are set forth to provide a more thorough description of the specific examples described herein. It should be apparent, however, to one skilled in the art, that one or more other examples or variations of these examples may be practiced without all the specific details given below. In other instances, well known features have not been described in detail so as not to obscure the description of the examples herein. For ease of illustration, the same number labels are used in different diagrams to refer to the same items; however, in alternative examples the items may be different.

[0028] Exemplary apparatus(es) and/or method(s) are described herein. It should be understood that the word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any example or feature described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other examples or features.

[0029] Interference may be electric-magnetic interference ("EMI") and/or radio frequency interference ("RFI"). The following description of interference shielding may be used for either or both of these types of interference. However, for purposes of clarity by way of example and not limitation, generally only shielding from EMI is described below in additional detail.

[0030] FIG. **1**A is a block diagram of a side view depicting an exemplary conventional system-in-package ("SiP") **10** without EMI shielding. In SiP **10**, there may be coupled to a package substrate **19** one or more active microelectronic devices **11**, passive microelectronic devices **12**, and/or IC dies **13**. In this example, IC die **13**, which may be a passive or active die, may be subject to EMI. IC die **13** may be wire bonded to package substrate **19** with wire bonds **15** for carrying input/output among other signals, a power supply voltage and ground reference.

[0031] Package substrate **19** may be formed of thin layers called laminates or laminate substrates. Laminates may be organic or inorganic. Examples of materials for "rigid" package substrates include an epoxy-based laminate such as FR4 or FR5, a resin-based laminate such as bismaleimide-triazine ("BT"), a ceramic substrate (e.g. a low temperature co-fired ceramic (LTCC)), a glass substrate, or other form of rigid package substrate. Moreover, a package substrate **19** herein may be a PCB or other circuit board. Other known details regarding conventional SiP **10** are not described for purposes of clarity.

[0032] FIG. **1**B is a block diagram of a side view depicting another exemplary conventional SiP **10** without EMI shielding. SiP **10** of FIG. **1**B is the same as SiP **10** of FIG. **1**A, except rather than wire bonds **15**, flip-chip ("FC") interconnects, such as microbumps, **17** are used. Even though microbump interconnects **17** are illustratively depicted, other types of die-surface mount interconnects may be used. Moreover, microbump interconnects **17** may be used in addition to wire bonds **15**, though not illustratively depicted in FIG. **1**B.

[0033] FIG. **2** is a corner top-down perspective view depicting an exemplary portion of a conventional EMI shielding **20**. In conventional EMI shielding **20**, a top electrically conductive plate **23** may be disposed over a bottom conductive plate **24**, where such bottom conductive plate **24** has a larger surface area than such top conductive plate **23**.

[0034] Conductive plates **23** and **24** may be respectively coupled to a package substrate **19** with rows of wire bonds **21** and **22**. Thus, two sides of top plate **23** may be wire bonded with corresponding rows of wire bonds **21**, and likewise two sides of bottom plate **24** may be wire bonded with corresponding rows of wire bonds **22**. Non-electrically conductive spacers (not shown) may be used to insulate wire bonds **21** from bottom conductive plate **24**. A microelectronic device (not shown) to be EMI shielded may be sandwiched between top and bottom conductive plates **23**

and **24**. This type of EMI shielding with wire bonding may be too bulky for many applications. Furthermore, there may be gaps on opposite sides with respect to wire bonds providing side EMI shielding.

Interference Shielding

[0035] FIGS. **3**A and **3**B are top views of block diagrams depicting respective exemplary SiPs **100** with EMI shielding. Each of SiPs **100** may include a package substrate **19** having coupled to an upper surface **132** thereof one or more active microelectronic devices **11**, one or more passive microelectronic devices **12**, and wire bond wires **131**, where upper ends of such wire bond wires **131** may be coupled to an upper surface **132**. Upper surface **132** may be a conductive surface. Wire bond wires **131** may include wire diameters equal to or less than approximately 0.0508 millimeters (2 mils).

[0036] A portion of wire bond wires **131** may be positioned to define a shielding region **133**. Along those lines, rows and columns of a BVA arrangement **136** of wire bond wires **131** may be used to encircle or otherwise surround a shielding region **133**. Upper ends of at least a subset of such wire bond wires **131** surrounding a shielding region **133** may be used to support conductive surface **130**, and such conductive surface **130** may be over such shielding region **133** for covering thereof.

[0037] Conductive surface **130** may be a rigid or flexible surface which is electrically conductive. In an implementation, conductive surface **130** may be flexible, such as a flexible conductive coating on a surface of a flexible sheet. In another implementation, a rigid plate may provide a conductive surface. A rigid plate may be made of a conductive material. However, a conductive coating may be sprayed or painted on a rigid plate or flexible sheet. In the example of FIG. **3**B, conductive surface **130** may have holes **137** for allowing upper portions of at least some of wire bond wires **131** defining a shielding region **133** to extend through upper surface **130**, as described below in additional detail.

[0038] FIG. **4** is a block diagram of a cross-sectional side view depicting an exemplary SiP **100** with EMI shielding. SiP **100** may include a package substrate **19** having coupled to an upper surface **132** thereof one or more active microelectronic devices **11**, one or more passive microelectronic devices **12**, and wire bond wires **131**, where upper ends of such wire bond wires **131** may be coupled to a conductive surface **130**. Even though an SiP **100** is described, another type of microelectronic package having protection from EMI may be used.

[0039] Package substrate **19** has an upper surface **132** and a lower surface **149** opposite the upper surface. Package substrate **19** may have located between surfaces **132** and **149** a ground plane **140** and vias **142** interconnected to such ground plane for electrical conductivity.

[0040] Wire bond wires **131** may be coupled to ground plane **140** with vias **142**. Some wire bond wires **131** may be mechanically coupled to upper surface **132** with ball bonds **141** for electrical conductivity; however, in other implementations, other types of bonding may be used. Moreover, not all wire bond wires **131** need be coupled to ground plane **140**. Some wire bond wires **131** may be used for carrying supply voltages or signals within SiP **100**. Some wire bond wires **131** may be used for coupling to other devices within SiP **100**. However, generally much of the following description is directed at wire bond wires **131** associated with a Faraday cage **153**. Along those lines, wire bond wires **131** may be coupled to one or more ground planes for electrically conducting interference thereto.

[0041] An active or passive microelectronic device **145** may be coupled to upper surface **132** of package substrate **19**. Microelectronic device **145** may include an active integrated circuit die and/or a passive component. A passive component may be a capacitor, an inductor, or a resistor, or any combination thereof.

[0042] Microelectronic device **145** may be coupled to package substrate **19** with ball or bump interconnects and/or wire bond wires, as previously described. Moreover, microelectronic device **145** may be coupled to upper surface **132** with an adhesive or an underfill layer (not shown).

[0043] Microelectronic device **145** may be disposed in a dielectric protective material **143**, such as with an encapsulant or a molding material, for at least covering an upper surface and sidewalls of microelectronic device **145**. Wire bond wires **131** may be disposed around sidewalls of microelectronic device **145**.

[0044] Conductive surface **130** may be located upon or coupled to a top or upper surface **146** of dielectric protective material **143**. However, in another implementation a top surface of dielectric protective material **143** may be at a higher level than tips **148** of wire bond wires **131**, as described below in additional detail. Conductive surface **130** may be positioned over wire bond wires **131** associated with Faraday cage **153**. Upper ends or tips **148** of such wire bond wires **131** may be mechanically coupled to conductive surface **130**. This coupling may be with a heated press bonding or other form of mechanical coupling.

[0045] Faraday cage **153** may be a combination of a portion of ground plane **140** interconnected to wire bond wires **131**, such as with vias **142**, supporting a conductive surface **130**. In another implementation, there may be a gap **144** between conductive surface **130** and tips **148** of some of wire bond wires **131**. Along those lines, a bottom of conductive surface **130**, such as of a conductive plate for example, may be attached to or rest upon a top surface of dielectric protective material **143**, and height of dielectric protective material **143** may be greater than height of wire bond wires **131**.

[0046] Thus, a conductive surface **130** may be positioned over a portion of wire bond wires **131** with upper ends or tips **148** thereof spaced apart from conductive surface **130**. However, a configuration with a gap **144** may provide a less effective Faraday cage **153**, and so for purposes of clarity by way of example and not limitation, it shall be assume that there is no gap.

[0047] Wire bond wires **131** coupled to ground plane **140** projecting or extending upwardly away from upper surface **132** of package substrate **19** may be arrayed. Along those lines, even though single rows and columns of a Bond Via Array™ or BVA™ arrangement **136** of wire bond wires **131** may be present in an implementation, multiple rows and/or multiple columns of wire bond wires **131** of a BVA™ arrangement **136**, may be present along one or more sides of a shielding region **133**.

[0048] To recapitulate, some of wire bond wires **131**, such as in BVA arrangement **136** defining a shielding region **133**, may be positioned to provide such a shielding region **133** for microelectronic device **145** from or with respect to EMI. Another portion of wire bond wires **131** located outside of

shielding region **133** may not be used for EMI shielding. Moreover, one or more other active or passive microelectronic devices **11** and/or **12** may be coupled to substrate **19** and be located outside of shielding region **133** and not part of, or position for such shielding region.

[0049] FIG. **5** is a block diagram of a cross-sectional side view depicting an exemplary SiP **100** with a conductive cover **150** and with signal wire bond wires **131***s* in an EMI shielding region under conductive cover **150**. SiP **100** of FIG. **5** is the same as SiP **100** of FIG. **4**, but with the following differences.

[0050] In this example, a portion of wire bond wires **131** have a height that is greater than a height of another portion of wire bond wires **131**. Both sets of wire bond wires **131** may be positioned proximate to and around microelectronic device **145**. However, the portion of wire bond wires **131** that are taller may be for providing a shielding region **133** for microelectronic device **145** with respect to EMI. Whereas, the other portion of wire bond wires **131** that are shorter ("wire bond wires **131***s*") may be signal wires coupling microelectronic device **145** to conductors of package substrate **19**. Such shorter wire bond wires **131***s* may be within a Faraday cage **153**. Heights of taller wire bond wires **131** may be limited to low-profile package applications.

[0051] Conductive cover **150** may be coupled to upper surface **132** of package substrate **19**. Conductive cover **150** may cover components of SiP **100** coupled to upper surface **132** including microelectronic device **145**, microelectronic devices **11**, **12** and wire bond wires **131**. Wire bond wires **131** not part of BVA arrangement **136** may interconnect conductive cover **150** and ground plane **140**. This coupling may be used to reduce internal noise. However, Faraday cage **153** may be located under cover **150** for internal EMI shielding. Optionally, conductive surface **130** may be omitted in favor of using conductive cover as an upper conductive surface of Faraday cage **153**, with or without a gap **144** between tips **148** and an underside of conductive cover **150**.

[0052] Some wire bond wires **131** within BVA arrangement **136** may be signal wires, namely wire bond wires **131***s*. Wire bond wires **131***s* may not be coupled to ground plane **140**, but may be coupled to traces (not shown) of package substrate **19**. Tips of wire bond wires **131***s* may be bonded or soldered to microelectronic device **145** prior to use of dielectric protective material **143**. In another implementation, dielectric protective material **143** may be omitted with respect to microelectronic device **145**.

[0053] Wire bond wires **131***s* may be bonded to upper surfaces of one or more of passive microelectronic devices **12** or active microelectronic devices **11**. These wire bond wires **131***s* may be for interconnection within SiP **100**.

[0054] FIG. **6** is a block diagram of a cross-sectional side view depicting an exemplary SiP **100** with EMI shielding using an upper substrate **169**. SiP **100** of FIG. **6** is the same as SiP **100** of FIG. **5**, but without a conductive cover **150** and with the following differences.

[0055] Upper substrate **169** in addition to vias **162** may include a ground plane **160**. Tips or upper ends **148** of wire bond wires **131** may be interconnected to vias **162** along a bottom surface of upper substrate **169** with interconnects **161**, such as with micro balls or microbumps for example, for coupling to ground plane **160**. Interconnects **161** may be disposed on an upper surface **168** of dielectric protective material **143**. Ground plane **160** may provide an upper conductive surface **130** of Faraday cage **153**.

[0056] Another microelectronic device **165**, whether active or passive, may be coupled to a top surface of upper substrate **169**. Microelectronic device **165** may be coupled with wire bond wires **15** to vias or traces of substrate **169**. However, micro balls or microbumps may be used in another implementation. Microelectronic device **165** may be coupled outside of Faraday cage **153**.

[0057] FIG. **7** is a block diagram of a top-down view depicting an exemplary portion of an SiP **100** prior to addition of an upper conductive surface **130** of a Faraday cage **153**. Bond pads **170** may be positioned proximate to and around microelectronic device **145** for coupling wire bond wires **131** respectively thereto for providing shielding region **133** of Faraday cage **153**. Shielding region **133** may be defined within a BVA arrangement **136**.

[0058] Bond pads **170** may be spaced apart from one another around sides of dielectric protective material **143**. Microelectronic device **145** in dielectric protective material **143** may be located in a central portion of shielding region **133**. A pad-to-pad pitch **171** of bond pads **170** may be equal to or less than approximately 250 microns. Pitch **171** of bond pads **170** may be selected for frequencies associated with interference, such as EMI and/or RFI, to shield microelectronic device **145** from EMI and/or RFI. Moreover, microelectronic device **145** may be an interference radiator, and thus such shielding may be to protect other components of SiP **100** from interference generated by microelectronic device **145**.

[0059] Even though single rows and columns of bond pads **170** are illustratively depicted, in another implementation there may be more than one or two rows and/or columns. Moreover, rows and/or columns of bond pads **170** may be interleaved with respect to one another to provide denser shielding. Effectively, wire bond wires **131** may be used to provide a low pass filter Faraday cage for reducing EMI with respect to operation of microelectronic device **145**. Along those lines, placement of bond pads **170**, and thus wire bond wires **131** may, though need not be, uniform. Wire bond wires **131** may be placed and/or adjusted for density tailored to shield a particular range of frequencies to or from microelectronic device **145**.

[0060] FIG. **8** is a block diagram of a top-down view depicting an exemplary portion of another SiP **100** prior to addition of an upper conductive surface **130** of a Faraday cage **153**. In this example, two rows and two columns of a BVA arrangement **136** of wire bond wires **131** are used to define a shielding region **133**. In this example, spacing between rows and columns is interleaved to provide a denser pattern of wire bond wires **131**.

[0061] In this example, some of wire bond wires **131** of BVA arrangement **136** are for carrying signals, namely wire bond wires **131***s*. Along those lines, interconnects **180** may be formed for extending from microelectronic device **145** outside of dielectric protective material **143** for interconnection with signal wire bond wires **131***s*.

[0062] FIG. **9**A is a block diagram of a cross-sectional side view depicting an exemplary portion of a package-on-package ("POP") device **190** with EMI shielding. PoP device **190** may include an upper SiP **100**U stacked on top of a lower SiP **100**L. PoP device **190** may include one or more other microelectronic devices outside of a shielding region as well as other details, such as previously described with reference to FIGS. **3**A through **8** for example. Accord-

ingly, previously described details for SiPs **100** are not described hereinbelow for purposes of clarity and not limitation.

[0063] A lower package substrate **19**L of a lower SiP **100**L may include a lower ground plane **140**L having lower wire bond wires **131**L extending upwardly from an upper surface of lower package substrate **19**L. Such lower wire bond wires **131**L and ground plane **140**L may be interconnected to one another, such as with vias and ball bonds as previously described, for forming a lower portion of a Faraday cage **153**. Tips **148** of lower wire bond wires **131**L may be bonded or coupled with interconnects **191** to pads and vias therefor along an underneath side of upper package substrate **19**U.

[0064] Optionally, upper package substrate **19**U may include an upper ground plane **140**U for forming a Faraday cage **153** as a stack of two Faraday cages, namely an upper Faraday cage **192**U and a lower Faraday cage **192**L. Each of Faraday cages **192**U and **192**L may include respective packaged microelectronic devices **145**U and **145**L respectively coupled to upper surfaces of package substrates **19**U and **19**L.

[0065] Upper ground plane **140**U of upper substrate **19**U may be located over a lower microelectronic device **145**L, so tips or upper ends **148** of lower wire bond wires **131**L may be interconnected to pads or contacts with interconnects **191** along an underside surface of upper package substrate **19**U for electrical coupling to upper ground plane **140**U. Upper wire bond wires **131**U and optional ground plane **140**U may be interconnected to one another, such as with vias and ball bonds as previously described, for forming an upper portion of a Faraday cage **153**. Tips **148** of upper wire bond wires **131**U may be bonded or coupled to conductive surface **130** for completing such upper Faraday cage **192**U.

[0066] In another implementation, vias of upper substrate package **19**U may interconnect lower wire bond wires **131**L with upper wire bond wires **131**U without being connected to an upper ground plane **140**U to form a "two-story" or bi-level Faraday cage **153** for two microelectronic devices **145**U, **145**L. Even though only two levels are illustratively depicted, more than two levels may be used in other implementations.

[0067] FIG. **9**B is a block diagram of a cross-sectional side view depicting an exemplary portion of another POP device **190** with EMI shielding. PoP device **190** may include one or more other microelectronic devices outside of a shielding region as well as other details, such as previously described with reference to FIGS. **3**A through **9**A for example. Accordingly, previously described details for SiPs **100** are not described hereinbelow for purposes of clarity and not limitation.

[0068] PoP device **190** of FIG. **9**B may be the same as POP device **190** of FIG. **9**A, except with the following differences. PoP device **190** of FIG. **9**B may include signal wire bond wires **131***s*. Signal wire bond wires **131***s* may be located within Faraday cage **153**, including within Faraday cage **192**U.

[0069] Signal wire bond wires **131***s* in this configuration may extend upwardly from an upper surface of a lower microelectronic device **145**L. Tips or upper ends **148** of wire bond wires **131***s* extending from an upper surface of lower microelectronic device **145**L may be interconnected to an underneath side of upper package substrate **19**U, such as with interconnects **191**. Vias and/or traces (not shown) may electrically couple upper and low microelectronic devices **145** with signal wire bond wires **131***s*. Moreover, lower substrate package **19**L may include vias and/or traces (not shown) for interconnection with lower microelectronic device **145**.

[0070] FIG. **10** is a block diagram of a cross-sectional side view depicting an exemplary portion of another SiP **100** with EMI shielding. SiP **100** may include one or more other microelectronic devices outside of a shielding region as well as other details, such as previously described with reference to FIGS. **3**A through **9**B for example. Accordingly, previously described details for SiPs **100** are not described hereinbelow for purposes of clarity and not limitation.

[0071] In this example, wire bond wires **131** and a microelectronic device **145**, such as an IC die, are protected by a dielectric protective material **143**. Microelectronic device **145** may be interconnected with microbump interconnects **17** to an upper surface of package substrate **19** prior to depositing or injecting dielectric protective material **143**. Likewise, wire bond wires **131** may be ball bonded to an upper surface of package substrate **19** prior to depositing or injecting dielectric protective material **143**.

[0072] Optionally, signal wire bond wires **131***s* may be ball bonded to an upper surface **201** of microelectronic device **145** prior to depositing or injecting dielectric protective material **143**. Signal wire bond wires **131***s* thus may be within a shielding region **133** of a Faraday cage **153**.

[0073] Tips or upper ends **148** of wire bond wires **131**, as well as optional signal wire bond wires **131***s*, may extend above an upper surface **202** of dielectric protective material **143**. Solder balls or other interconnect eutectic masses **204** may be deposited onto tips **148** for subsequent interconnection, such as describe elsewhere herein.

Vertical Integration without Interference Shielding

[0074] FIG. **11**A is a block diagram of a cross-sectional side view depicting an exemplary portion of an SiP **100** without wire bond wire EMI shielding. FIG. **11**B is a block diagram of a cross-sectional side view depicting an exemplary portion of aSiP **100** which may or may not include EMI shielding. With simultaneous reference to FIGS. **11**A and **11**B, SiPs **100** respectively illustratively depicted in those figures are further described. Each of SiPs **100** may include one or more other microelectronic devices as well as other details, such as previously described. Accordingly, previously described details for SiP **100** are not described hereinbelow for purposes of clarity and not limitation.

[0075] Each of SiPs **100** includes a vertically integrated microelectronic package **200**. Each of microelectronic packages **200** includes a substrate **19** having an upper surface **132** and a lower surface **149** opposite the upper surface. Package substrate **19** may have located between surfaces **132** and **149** a ground plane **140** and vias **142** interconnected to such ground plane for electrical conductivity, however, this is not a requirement.

[0076] A microelectronic device **145** may be coupled to upper surface **132** of substrate **19**, where microelectronic device is an active or passive microelectronic device. Along those lines, in an SiP **100** there may be one or more of either or both passive or active microelectronic devices coupled to upper surface **132**. The active or passive devices may be implemented on a semiconductor chip or may be implemented as discreet components, such as standalone capacitors, resistors, inductors, antenna, sensors, etc. If implemented in or on a semiconductor material, the component may be connected in a face up or face down configuration

and may also have one or more through semiconductor vias (TSVs) coupling opposing sides of the component. According to this implementation upper surfaces of such active or passive microelectronic devices, which may in the past have gone unused for vertical integration, now include bonding wire bond wires attached to such upper surfaces of such microelectronic devices for connection to other passive or active components.

[0077] More particularly, wire bond wires **131** may be coupled to and extend away from the upper surface **132** of substrate **19**, and wire bond wires **231** may be coupled to and extend away from an upper surface **201** of microelectronic device **145**. Wire bond wires **131** and **231** may be mechanically coupled to upper surfaces **132** and **201**, respectively, with ball bonds **141** for electrical conductivity. However, in other implementations, other types of bonding may be used. Wire bond wires **231** are shorter in length than wire bond wires **131**.

[0078] With reference to FIG. **11**A, wire bond wires **131** may have an overall finished length **261**, and wire bond wires **231** may have an overall finished length **262**. However, finished heights of wire bond wires **131** and **231** may be approximately the same for having upper ends **148** extend above an upper surface **202** of molding layer **143**.

[0079] Upper ends **148** may be coterminous for being generally coplanar. Solder balls or other interconnect eutectic masses **204** may be deposited on upper surface **202** respectively over upper ends **148** for forming interconnects with pads (not shown) on a front face underside of an active or passive microelectronic device **11** or **12**.

[0080] According to one implementation, microelectronic device **145** may be coupled to upper surface **132** of package substrate **19**. Microelectronic device **145** may include conductive traces and may include only passive components. If implemented as a passive component, microelectronic device **145** may represent a capacitor, an inductor, or a resistor, or any combination thereof. If implemented as an active component, microelectronic device **145** may represent, e.g., a die with transistors, but additionally or alternatively may include other active or passive devices on or in the active component.

[0081] Microelectronic device **145** may be coupled to package substrate **19** with ball or bump interconnects and/or wire bond wires, as previously described. Moreover, microelectronic device **145** may be coupled to upper surface **132** with an adhesive or an underfill layer (not shown).

[0082] In the implementation shown, microelectronic device **145**, as well as microelectronic device **11** or **12**, have orientations facing downwardly, namely face-down orientations, toward upper surface **132** of substrate **19**. However, in another implementation, microelectronic device **11** or **12** may additionally or alternatively have circuitry on a front side face facing upwardly away from an upper surface **132** of substrate **19**.

[0083] A microelectronic device **11** or **12** may be coupled above uppermost surface **202** of molding layer **143**. In an implementation, a microelectronic device **11** or **12** may be coupled to upper ends **148** of wire bond wires **131** and **231** with eutectic masses **204** or other mechanical interconnects. Microelectronic device **11** or **12** may be located above microelectronic device **145** and may completely overlap microelectronic device **145**, at least partially overlap such microelectronic device **145**, or may not overlap microelectronic device **145** at all.

[0084] Molding layer **143** may have an uppermost surface **202** and a lowermost surface **252** opposite the uppermost surface. Molding layer **143** may be disposed for surrounding portions of lengths **261** and **262** for both wire bond wires **131** and **231**. Upper ends **148** may not be covered with molding layer **143**, such as by use of a mold assist film for an injection molding for example. In another implementation, molding layer **143** may temporarily completely cover lengths **261** and **262** followed by an etch back to reveal upper ends **148**.

[0085] In an implementation of a vertically integrated microelectronic package **200**, microelectronic device **145** may be disposed in molding layer **143**. Along those lines, in an implementation, microelectronic device **145** may be completely located between uppermost surface **202** and lowermost surface **252** of molding layer **143**. Wire bond wires **131** may be disposed around sidewalls **203** of microelectronic device **145** though not for interference shielding in this example implementation.

[0086] Wire bond wires **131** may be coupled to ground plane **140** for projecting or extending upwardly away from upper surface **132** of package substrate **19** and may be arrayed. Along those lines, even though single rows and columns of a BVA™ arrangement of wire bond wires **131** and/or **231** may be present in an implementation, multiple rows and/or multiple columns of such wire bond wires may be in a BVA™ arrangement.

[0087] In an implementation of vertically integrated microelectronic package **200**, microelectronic device **12**, implemented as a passive microelectronic device, may be used. However, in another implementation of vertically integrated microelectronic package **200**, microelectronic device **11** may be implemented as an active microelectronic device.

[0088] With reference to FIG. **11**B, inner wire bond wires **131***i* may have an overall finished length **263**, and wire bond wires **231** may have an overall finished length **264**. Outer wire bond wires **1310** may have an overall finished height **261**, as previously described with reference to FIG. **11**A. Finished heights of wire bond wires **131***i* and **231** may be approximately the same after forming for having upper ends **148** generally even with one another.

[0089] Upper ends **148** of wire bond wires **131***i* and **231** may be coterminous for being generally coplanar. Solder balls or other interconnect eutectic masses **274** may couple a lower surface of an active or passive microelectronic device **271** respectively to upper ends **148** of wire bond wires **131***i* and **231** for forming interconnects with pads (not shown) on a front face underside of an active or passive microelectronic device **271**. A molding material may be injected to form molding material layer **143** with microelectronic device **271** in place, and thus a lower surface of microelectronic device **271** may be in contact with molding material of molding layer **143**. For molding, a mold assist film may be used to allow tips **148** of outer wire bond wires **1310** to extend above upper surface **202** of molding layer **143**, as well as pads or other interconnects (not shown) of microelectronic device **271**. In another implementation, molding layer **143** may temporarily completely cover lengths **261** followed by an etch back to reveal upper ends **148** thereof.

[0090] Microelectronic device **271** may be coupled to and located above microelectronic device **145** and may at least partially overlap microelectronic device **145**. Along those

lines, microelectronic device **271** may laterally extend outside a perimeter of microelectronic device **271** for interconnection of inner wire bond wires **131***i* between upper surface **132** of substrate **19** and a lower surface of microelectronic device **271** facing such upper surface **132**. Wire bond wires **131***i*, as well as wire bond wires **1310**, may be disposed around sidewalls **203** of microelectronic device **145** though not for interference shielding in this example implementation.

[0091] Again, a passive microelectronic device **145** may be coupled to upper surface **132** of package substrate **19**. Microelectronic device **145** may include conductive traces and may include only passive components. A passive component may be a capacitor, an inductor, or a resistor, or any combination thereof. Microelectronic device **145** may be coupled to package substrate **19** with ball or bump interconnects and/or wire bond wires, as previously described. Moreover, microelectronic device **145** may be coupled to upper surface **132** with an adhesive or an underfill layer (not shown). If the microelectronic device is a discreet passive component, the wire **231** may be formed on a solder portion, such as a solder pad or on a copper, nickel, gold, or alloy pad.

[0092] Molding layer **143** may have an uppermost surface **202** and a lowermost surface **252** opposite the uppermost surface. Molding layer **143** may be disposed for surrounding portions of lengths **261** of wire bond wires **1310** and for surrounding lengths **263** and **264** for both wire bond wires **131***i* and **231**.

[0093] In an implementation of vertically integrated microelectronic package **200**, microelectronic device **145** may be disposed in molding layer **143** and completely located between uppermost surface **202** and lowermost surface **252** of molding layer **143**. Microelectronic device **271** may be disposed in molding layer **143** and at least partially located between uppermost surface **202** and lowermost surface **252** of molding layer **143**. Microelectronic device **11** or **12** may be coupled above uppermost surface **202** of molding layer **143**.

[0094] For a passive microelectronic device **271**, microelectronic device **271** may include conductive traces and may include only passive components. Microelectronic device **271** may include an RDL. A passive component may be a capacitor, an inductor, or a resistor, or any combination thereof. In this implementation, microelectronic devices **145** and **271**, as well as microelectronic devices **11** or **12**, have orientations facing downwardly, namely face-down orientations, toward upper surface **132** of substrate **19**. However, in another implementation, microelectronic device **11** or **12** and/or microelectronic device **271** may have a front side face facing upwardly away from an upper surface **132** of substrate **19**.

[0095] In an implementation of vertically integrated microelectronic package **200**, microelectronic device **12**, which is a passive microelectronic device, may be used. However, in another implementation of vertically integrated microelectronic package **200**, microelectronic device **11**, which is an active microelectronic device, may be used. A microelectronic device **11** or **12** may be coupled above uppermost surface **202** of molding layer **143** for interconnection with microelectronic device **271**. In an implementation, a microelectronic device **11** or **12** may be coupled to an upper surface of microelectronic device **271** with eutectic masses **204** or other mechanical interconnects for electrical conductivity.

[0096] Microelectronic device **11** or **12** may be located above microelectronic device **271** and at least partially overlap such microelectronic device **271**. Along those lines, a microelectronic device **11** or **12** may be coupled above uppermost surface **202** of molding layer **143** for interconnection with upper ends **148** of outer wire bond wires **1310**, as well as interconnection with an upper surface of microelectronic device **271**.

[0097] Wire bond wires **131***i* and **1310** may be coupled to ground plane **140** for projecting or extending upwardly away from upper surface **132** of package substrate **19** and may be arrayed. Along those lines, even though single rows and columns of a BVA™ arrangement of wire bond wires **131***i*, **1310**, and/or **231** may be present in an implementation, multiple rows and/or multiple columns of such wire bond wires may be in a BVA™ arrangement.

[0098] FIG. **12**A is a block diagram of a cross-sectional side view depicting an exemplary portion of another SiP **100** without wire bond wire EMI shielding. SiP **100** of FIG. **12**A may be the same as in FIG. **11**A, except for the following details. In this implementation of a vertically integrated microelectronic package **200**, microelectronic device **12** is cantilevered for laterally extending over and above a wire bond wire **131**. Along those lines, upper ends **148** of wire bond wires **131** may be interconnected with eutectic masses **204** to a lower surface of a microelectronic device **11** or **12**.

[0099] FIG. **12**B is a block diagram of a cross-sectional side view depicting an exemplary portion of another SiP **100** without wire bond wire EMI shielding. SiP **100** of FIG. **12**B may be the same as in FIG. **11**B, except for the following details. In this implementation of a vertically integrated microelectronic package **200**, microelectronic device **12** is not cantilevered for laterally extending over and above a wire bond wire **1310**. Along those lines, a microelectronic device **11** or **12** and microelectronic device **271** may have approximately equal surface areas for lower and upper surfaces respectively thereof.

[0100] FIG. **12**C is a block diagram of a cross-sectional side view depicting an exemplary portion of another SiP **100** without wire bond wire EMI shielding. SiP **100** of FIG. **12**C may be the same as in FIG. **12**A, except for the following details. In this implementation of a vertically integrated microelectronic package **200**, microelectronic device **12** is cantilevered for laterally extending over and above wire bond wires **131** on both a right and a left side of microelectronic device **145**. Along those lines, upper ends **148** of wire bond wires **131** may be interconnected with eutectic masses **204** to a lower surface of a microelectronic device **11** or **12**. Accordingly, it should be appreciated that wire bond wires **131** disposed around a microelectronic device and interconnected to a microelectronic device **11** or **12** may be used for fan-out.

[0101] FIG. **12**D is a block diagram of a cross-sectional side view depicting an exemplary portion of another SiP **100** without wire bond wire EMI shielding. SiP **100** of FIG. **12**D may be the same as in FIG. **12**B, except for the following details. In this implementation of a vertically integrated microelectronic package **200**, microelectronic device **12** is not cantilevered for laterally extending over and above a wire bond wire **1310**. Along those lines, a microelectronic device **11** or **12** and microelectronic device **271** may have

approximately equal surface areas for lower and upper surfaces respectively thereof. Along those lines, upper ends **148** of wire bond wires **131***i* may be interconnected with eutectic masses **274** to a lower surface of a microelectronic device **271**. Accordingly, it should be appreciated that wire bond wires **131***i* disposed around a microelectronic device **145** and interconnected to a microelectronic device **271** may be used for fan-out.

[0102] FIG. **13**A is a block diagram of a cross-sectional side view depicting an exemplary SiP **100** without EMI shielding and with a vertically integrated microelectronic package **200**. In this implementation, a vertically integrated microelectronic package **200** may be a stand-alone package coupled to substrate **19** as in FIG. **12**D of an SiP **100**. As components of SiP **100** have been previously described, such as with reference to FIG. **4** for example, such description is not repeated.

[0103] In this implementation, eutectic masses **274** are formed on an upper surface **202** of molding layer **143**. Eutectic masses **274** interconnect upper ends **148** of wire bond wires **131***i* and **231**, which may be encapsulated in molding layer **143** except for lower and upper ends thereof, to a lower surface of microelectronic device **271**. In this example, a lower surface of microelectronic device **271** is not in contact with an upper surface **202** of molding layer **143**.

[0104] Moreover, in this example implementation, signal wire bond wires **131***s* may be encapsulated in molding material of molding layer **143**, except for lower surfaces of such signal wire bond wires **131***s*. Signal wire bond wires **131***s* may be shorter than inner wire bond wires **131***i* and may be as previously described for interconnection with a microelectronic device **145**. Along those lines, microelectronic device **271** may be coupled to upper ends **148** of a taller portion of wire bond wires **131** coupled to upper surface **132**, such as wire bond wires **131***i*. Microelectronic device **271** may further be coupled to upper ends **148** of wire bond wires **231**. Another portion of wire bond wires **131** coupled to upper surface **132**, such as signal wire bond wires **131***s*, may have upper ends **148** thereof coupled to an upper surface of microelectronic device **145**, such as previously described.

[0105] Optionally, wire bond wires **331** may be coupled to one or more upper surfaces of active microelectronic devices **11** and/or passive microelectronic devices **12** directly coupled to an upper surface **132** of substrate **19**.

[0106] Other details regarding SiP **100** of FIG. **13**A have been previously described, and thus are not repeated for purposes of clarity and not limitation.

[0107] FIG. **13**B is a block diagram of a cross-sectional side view depicting an exemplary SiP **100** without EMI shielding and with a vertically integrated microelectronic package **200**. In this implementation, a vertically integrated microelectronic package **200** may be a stand-alone package coupled to substrate **19** as in FIG. **13**A of an SiP **100**. As components of SiP **100** have been previously described, such as with reference to FIG. **4** for example, such description is not repeated.

[0108] SiP **100** of FIG. **13**B is similar to SiP **100** of FIG. **13**A, except for the following differences. In SiP **100** of FIG. **13**B, vertically integrated microelectronic package **200** omits microelectronic device **271**. Thus, a microelectronic device **11** and/or **12** may be directly coupled to an upper surface **202** of molding layer **143** with eutectic masses **204**, such as previously described.

[0109] FIG. **13**C is a block diagram of a cross-sectional side view depicting an exemplary SiP **100** without EMI shielding and with a vertically integrated microelectronic package **200**. In this implementation, a vertically integrated microelectronic package **200** may be a stand-alone package coupled to substrate **19** as in FIG. **13**A of an SiP **100**. As components of SiP **100** have been previously described, such as with reference to FIG. **4** for example, such description is not repeated.

[0110] SiP **100** of FIG. **13**C is similar to SiP **100** of FIG. **13**A, except for the following differences. In SiP **100** of FIG. **13**C, vertically integrated microelectronic package **200** has some wire bond wires **131***i* encapsulated in molding material of molding layer **143** as previously described and has some wire bond wires **131***i* not encapsulated in molding material of molding layer **143**.

[0111] FIG. **13**D is a block diagram of a cross-sectional side view depicting an exemplary SiP **100** without EMI shielding and with a vertically integrated microelectronic package **200**. In this implementation, a vertically integrated microelectronic package **200** may be a stand-alone package coupled to substrate **19** as in FIG. **13**B of an SiP **100**. As components of SiP **100** have been previously described, such as with reference to FIG. **4** for example, such description is not repeated.

[0112] SiP **100** of FIG. **13**D is similar to SiP **100** of FIG. **13**B, except for the following differences. In SiP **100** of FIG. **13**D, vertically integrated microelectronic package **200** does not have wire bond wires **131** encapsulated in molding material of molding layer **143**.

[0113] These are some of a variety of implementations of a vertically integrated microelectronic package **200** for an SiP **100**. However, these or other implementations may be provided in accordance with the description herein.

[0114] Along those lines, while the foregoing describes exemplary embodiment(s) in accordance with one or more aspects of the invention, other and further embodiment(s) in accordance with the one or more aspects of the invention may be devised without departing from the scope thereof, which is determined by the claim(s) that follow and equivalents thereof. Claim(s) listing steps do not imply any order of the steps. Trademarks are the property of their respective owners.

1-20. (canceled)

21. An apparatus, comprising:

a substrate comprising a first side and a second side opposite the first side;

a first microelectronic device coupled to the first side of the substrate;

a second microelectronic device coupled to the first side of the substrate;

an EMI shield comprising a plurality of wire bond wires having first ends coupled to the first side of the substrate and second ends extending away therefrom, wherein the second microelectronic device is separated from the first microelectronic device by at least a portion of the EMI shield; and

a conductive layer, wherein:

the conductive layer extends along a top portion of the apparatus; and

the conductive layer extends along at least a portion of one or more sides of the apparatus.

22. The apparatus according to claim **21**, wherein the conductive layer is part of a top portion of the EMI shield.

23. The apparatus according to claim **21**, wherein a portion of the conductive layer is coupled to the substrate.

24. The apparatus according to claim **21**, wherein a portion of the conductive layer extends from the top portion of the apparatus to the first side of the substrate.

25. The apparatus according to claim **21**, wherein:

a first wire bond wire of the plurality of wire bond wires has a first height;

the portion of the one or more sides of the apparatus has a second height; and

the first height is substantially the same as the second height.

26. The apparatus according to claim **21**, further comprising additional wire bond wires connected to the conductive layer.

27. The apparatus according to claim **21**, further comprising a second EMI shield comprising additional wire bond wires having first ends coupled to the first side of the substrate.

28. The apparatus according to claim **21**, wherein at least a portion of the plurality of wire bond wires substantially shield the first microelectronic device from interference at one or more frequencies generated by the second microelectronic device.

29. The apparatus according to claim **21**, wherein at least a portion of the plurality of wire bond wires substantially shield the second microelectronic device from interference at one or more frequencies generated by the first microelectronic device.

30. The apparatus according to claim **21**, wherein:

the first microelectronic device is an active device; and

the second microelectronic device is a passive device.

31. The apparatus according to claim **21**, wherein at least a portion of the plurality of wire bond wires are uniformly spaced apart from one another.

32. The apparatus according to claim **21**, wherein at least a portion of the plurality of wire bond wires are not uniformly spaced apart from one another.

33. An apparatus, comprising:

a substrate comprising a first side and a second side opposite the first side;

a first microelectronic device coupled to the first side of the substrate;

a second microelectronic device coupled to the first side of the substrate;

a plurality of wire bond wires having first ends coupled to the first side of the substrate and second ends extending away therefrom, wherein the second microelectronic device is separated from the first microelectronic device by at least two wire bonds of the plurality of wire bond wires; and

a conductive layer, wherein:

the conductive layer extends along a top portion of the apparatus; and

the conductive layer is grounded.

34. The apparatus according to claim **33**, further comprising an EMI shield comprising a portion of the plurality of wire bond wires, wherein the conductive layer is part of a top portion of the EMI shield.

35. The apparatus according to claim **33**, wherein a portion of the conductive layer is coupled to the substrate.

36. The apparatus according to claim **33**, wherein a portion of the conductive layer extends from the top portion of the apparatus to the first side of the substrate.

37. The apparatus according to claim **33**, wherein:

a first wire bond wire of the plurality of wire bond wires has a first height;

one or more sides of the apparatus has a second height; and

the first height is substantially the same as the second height.

38. The apparatus according to claim **33**, further comprising an EMI shield comprising additional wire bond wires having first ends coupled to the first side of the substrate.

39. The apparatus according to claim **33**, wherein at least a portion of the plurality of wire bond wires substantially shield the first microelectronic device from interference at one or more frequencies generated by the second microelectronic device.

40. The apparatus according to claim **33**, wherein at least a portion of the plurality of wire bond wires substantially shield the second microelectronic device from interference at one or more frequencies generated by the first microelectronic device.

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