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SEMICONDUCTOR PACKAGE AND METHOD OF FABRICATING THE SAME

Abstract

Disclosed are semiconductor packages and methods of fabricating the same. The semiconductor package comprises a first redistribution substrate and a first semiconductor device on the first redistribution substrate. The first redistribution substrate includes a first dielectric layer that includes a first hole, an under-bump that includes a first bump part in the first hole and a second bump part that protrudes from the first bump part onto the first dielectric layer, an external connection terminal on a bottom surface of the first dielectric layer and connected to the under-bump through the first hole, a wetting layer between the external connection terminal and the under-bump, and a first barrier/seed layer between the under-bump and the first dielectric layer and between the under-bump and the wetting layer.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION [0001] This U.S. nonprovisional application is a continuation of U.S. patent application Ser. No. 17/405,603 filed on Aug. 18, 2021, which claims priority under 35 U.S.C § 119 to Korean Patent Application No. 10-2020-0115240 filed on Sep. 9, 2020 in the Korean Intellectual Property Office, the disclosure of each of which is hereby incorporated by reference in its entirety.

BACKGROUND

[0002] The present inventive concepts relate to a semiconductor package and a method of fabricating the same.

[0003] A semiconductor package is provided to implement an integrated circuit chip to qualify for use in electronic products. A semiconductor package is typically configured such that a semiconductor chip is mounted on a printed circuit board (PCB) and bonding wires or bumps are used to electrically connect the semiconductor chip to the printed circuit board. With the development of electronic industry, many studies have been conducted to improve reliability and/or durability of semiconductor packages.

SUMMARY

[0004] Some example embodiments of the present inventive concepts provide a semiconductor package with increased reliability.

[0005] Some example embodiments of the present inventive concepts provide a method of fabricating a semiconductor package, which method is capable of increasing a yield.

[0006] An object of the present inventive concepts is not limited to the mentioned above, and other objects which have not been mentioned above will be clearly understood to those skilled in the art from the following description.

[0007] According to some example embodiments of the present inventive concepts, a semiconductor package may comprise: a first redistribution substrate; and a first semiconductor device on the first redistribution substrate. The first redistribution substrate may include: a first dielectric layer that includes a first hole; an under-bump that includes a first bump part in the first hole and a second bump part that protrudes from the first bump part onto the first dielectric layer; an external connection terminal on a bottom surface of the first dielectric layer and connected to the under-bump through the first hole; a wetting layer between the external connection terminal and the under-bump; and a first barrier/seed layer between the under-bump and the first dielectric layer and between the under-bump and the wetting layer.

[0008] According to some example embodiments of the present inventive concepts, a semiconductor package may comprise: a first redistribution substrate; and a first semiconductor device on the first redistribution substrate. The first redistribution substrate may include: a first dielectric layer that includes a first hole; an under-bump that includes a first bump part in the first

hole and a second bump part that protrudes from the first bump part onto the first dielectric layer; and an external connection terminal on a bottom surface of the first dielectric layer and connected to the under-bump through the first hole. An inner sidewall of the first hole may make a first angle with the bottom surface of the first dielectric layer. The first angle may range from about 45° to about 90°.

[0009] According to some example embodiments of the present inventive concepts, a semiconductor package may comprise: a first redistribution substrate; a first semiconductor device on the first redistribution substrate; and a mold layer that covers the first semiconductor device and the first redistribution substrate. The first redistribution substrate may include: a first dielectric layer that includes a first hole; an under-bump that includes a first bump part in the first hole and a second bump part that protrudes from the first bump part onto the first dielectric layer; an external connection terminal on a bottom surface of the first dielectric layer and connected to the under-bump through the first hole; a wetting layer between the external connection terminal and the under-bump; a first barrier/seed layer between the under-bump and the first dielectric layer and between the under-bump and the wetting layer; a second dielectric layer that covers the under-bump and the first dielectric layer; and a first redistribution pattern that penetrates the second dielectric layer and is connected to the under-bump. The external connection terminals may include: a first terminal part in the first hole; and a second terminal part that protrudes outwardly from the bottom surface of the first dielectric layer. A sidewall of the first terminal part may make a first angle with a top surface of the second terminal part. The first angle may range from about 45° to about 90°.

[0010] According to some example embodiments of the present inventive concepts, a method of fabricating a semiconductor package may comprise: forming a redistribution substrate; mounting a semiconductor device on the redistribution substrate; and bonding an external connection terminal to the redistribution substrate. The step of forming the redistribution substrate may include: sequentially stacking a release layer and an etch stop layer on a carrier substrate; coating a first dielectric layer on the etch stop layer; exposing and developing the first dielectric layer to form a first hole that exposes the etch stop layer; sequentially stacking a sacrificial pattern and a wetting layer in the first hole, the wetting layer exposing an upper portion of an inner sidewall of the first hole; forming a first barrier/seed layer and an under-bump on the wetting layer; and removing the carrier substrate, the release layer, the etch stop layer, and the sacrificial pattern to expose the wetting layer and a bottom surface of the first dielectric layer. The external connection terminal may be bonded to the wetting layer.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. **1** illustrates a cross-sectional view showing a semiconductor package according to some example embodiments of the present inventive concepts.

[0012] FIG. **2** illustrates an enlarged view showing section P**1** of FIG. **1** according to some example embodiments of the present inventive concepts.

[0013] FIGS. **3**A to **3**C illustrate enlarged views showing section P**2** of FIG. **2** according to some example embodiments of the present inventive concepts.

[0014] FIG. **4** illustrates a plan view showing an under-bump according to some example embodiments of the present inventive concepts.

[0015] FIGS. **5**A to **5**I illustrate enlarged partial cross-sectional views showing a method of fabricating the semiconductor package of FIG. **1** according to some example embodiments of the present inventive concepts.

[0016] FIG. **6** illustrates a cross-sectional view showing a semiconductor package according to

some example embodiments of the present inventive concepts.
[0017] FIG. **7** illustrates a cross-sectional view showing a semiconductor package according to some example embodiments of the present inventive concepts.
[0018] FIG. **8** illustrates a cross-sectional view showing a semiconductor package according to some example embodiments of the present inventive concepts.
[0019] FIG. **9** illustrates a cross-sectional view showing a semiconductor package according to some example embodiments of the present inventive concepts.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0020] Some example embodiments of the present inventive concepts will now be described in detail with reference to the accompanying drawings to aid in clearly explaining the present inventive concepts.
[0021] FIG. **1** illustrates a cross-sectional view showing a semiconductor package according to some example embodiments of the present inventive concepts. FIG. **2** illustrates an enlarged view showing section P**1** of FIG. **1** according to some example embodiments of the present inventive concepts. FIGS. **3**A to **3**C illustrate enlarged views showing section P**2** of FIG. **2** according to some example embodiments of the present inventive concepts. FIG. **4** illustrates a plan view showing an under-bump according to some example embodiments of the present inventive concepts.
[0022] Referring to FIGS. **1** and **2**, a semiconductor package **1000** according to the present example embodiments may include a first redistribution substrate RD**1** and a first semiconductor device CH**1** mounted on the first redistribution substrate RD**1**. The first semiconductor device CH**1** and the first redistribution substrate RD**1** may be covered with a first mold layer MD**1**. In this description, the term "redistribution substrate" may be called "redistribution layer" or "wiring structure."
[0023] The first redistribution substrate RD**1** may include first, second, third, and fourth dielectric layers IL**1**, IL**2**, IL**3**, and IL**4** that are sequentially stacked. The first, second, third, and fourth dielectric layers IL**1**, IL**2**, IL**3**, and IL**4** may each include a photo-imageable dielectric (PID) layer.
[0024] Referring to FIGS. **1**, **2**, and **3**A, the first dielectric layer IL**1** may include a plurality of first holes H**1**. The first hole H**1** may have an inclined inner sidewall SS. The inner sidewall SS of the first hole H**1** may make a first angle θ**1** with a bottom surface IL**1**B of the first dielectric layer IL**1**. The first angle θ**1** may be, for example, an acute angle. The first angle θ**1** may range, for example, from about 45° to about 90°. The inner sidewall SS of the first hole H**1** may make a second angle θ**2** with a top surface IL**1**U of the first dielectric layer IL**1**. The second angle θ**2** may be, for example, an obtuse angle. The second angle θ**2** may range, for example, from about 90° to about 135°.
[0025] Referring to FIG. **3**A, under-bumps UBM may be correspondingly disposed in the first holes H**1**. The under-bumps UBM may each have a T-shaped cross-section. The under-bumps UBM may each include a first bump part PT**1** that is inserted into the first hole H**1** and a second bump part PT**2** that protrudes onto the first dielectric layer IL**1**. The first and second bump parts PT**1** and PT**2** may be integrally connected into a single piece. The first bump part PT**1** may have an inclined first sidewall SW**1**. The first sidewall SW**1** of the first bump part PT**1** and a bottom surface PT**2**B of the second bump part PT**2** may make therebetween an angle the same as the second angle θ**2**. The first sidewall SW**1** of the first bump part PT**1** and a bottom surface PT**1**B of the first bump part PT**1** may make therebetween an angle the same as the second angle θ**2**.
[0026] Referring still to FIG. **3**A, the bottom surface PT**2**B of the second bump part PT**2** may make a third angle θ**3** with a second sidewall SW**2** of the second bump part PT**2**. The third angle θ**3** may be greater than the first angle θ**1** and less than the second angle θ**2**. For example, the third angle θ**3** may be about 90° or right angle. As shown in FIG. **3**A, the second sidewall SW**2** of the second bump part PT**2** may be almost perpendicular to the top surface IL**1**U of the first dielectric layer IL**1**.
[0027] In example embodiments of the present inventive concepts, as shown in FIG. **3**C, the first to

third angles θ**1** to **03** may each be about 90°.
[0028] Referring to FIG. **3**B, the first bump part PT**1** may have a first width W**1** in one direction. The first width W**1** may increase as approaching the top surface IL**1**U from the bottom surface IL**1**B of the first dielectric layer IL**1**. The second bump part PT**2** may have a second width W**2** in the one direction. The second width W**2** may be greater than the first width W**1**. The second bump part PT**2** may cover the top surface IL**1**U of the first dielectric layer IL**1**. The under-bump UBM may include copper or nickel.
[0029] When viewed in plan as shown in FIG. **4**, the first bump part PT**1** may have a circular shape at the bottom surface PT**1**B thereof. When viewed in plan, the first sidewall SW**1** of the first bump part PT**1** and the bottom surface PT**2**B of the second bump part PT**2** may each have an annular shape that surrounds the bottom surface PT**1**B of the first bump part PT**1**.
[0030] A first barrier/seed layer SL**1** may be interposed between the under-bump UBM and the first dielectric layer IL**1**. The first barrier/seed layer SL**1** may include a barrier layer and a seed layer that are sequentially stacked. The barrier layer may include one or more of a titanium layer, a tantalum layer, a titanium nitride layer, and a tantalum nitride layer. The seed layer may include the same material as that of the under-bump UBM. The first barrier/seed layer SL**1** may be in contact with the first sidewall SW**1** and the bottom surface PT**1**B of the first bump part PT**1** and with the bottom surface PT**2**B of the second bump part PT**2**.
[0031] The first barrier/seed layer SL**1** (or the barrier layer thereof) may serve to reduce or prevent a constituent metal of the under-bump UBM from diffusing into the first dielectric layer IL**1**. Therefore, the first barrier/seed layer SL**1** may reduce or prevent a constituent metal of the under-bump UBM from reacting with a constituent material of the first dielectric layer IL**1**. Accordingly, a void may be reduced or prevented from forming between the under-bump UBM and the first dielectric layer IL**1**, and thus the under-bump UBM may be reduced or prevented from cracking and/or delamination from the first dielectric layer IL**1**.
[0032] External connection terminals **100** may be bonded to the bottom surface IL**1**B of the first dielectric layer IL**1**. The external connection terminal **100** may have a circular shape when viewed in plan. The external connection terminals **100** may be correspondingly connected through the first holes H**1** to the under-bumps UBM. The external connection terminals **100** may each include a first terminal part **100***a* that is inserted into the first hole H**1** and a second terminal part **100***b* that protrudes outwardly from the bottom surface IL**1**B of the first dielectric layer IL**1**. The first and second terminal parts **100***a* and **100***b* may be integrally connected into a single piece. The external connection terminals **100** may include one or more of tin, lead, and silver. The external connection terminals **100** may be formed of SnAg, for example.
[0033] Referring back to FIG. **3**A, the under-bump UBM may have a first thickness T**1** at the second bump part PT**2** thereof. The under-bump UBM may have a second thickness T**2** at the first bump part PT**1** thereof. The external connection terminal **100** may have a third thickness T**3** at the first terminal part **100***a* thereof. The second thickness T**2** may be about 0.8 times to about 1.2 times the third thickness T**3**. The first thickness T**1** may be the same as, greater than, or less than the second thickness T**2**.
[0034] Referring again to FIG. **3**A, a sidewall **100**S**1** of the first terminal part **100***a* and a top surface **100**S**2** of the second terminal part **100***b* may make therebetween an angle the same as the first angle θ**1**. Referring back to FIG. **3**B, the first terminal part **100***a* may have a third width W**3** in the one direction. The third width W**3** may increase as approaching the top surface IL**1**U from the bottom surface IL**1**B of the first dielectric layer IL**1**. The second terminal part **100***b* may have a fourth width W**4** in the one direction. The fourth width W**4** may be greater than the third width W**3**. The fourth width W**4** may be the same as or less than the second width W**2**.
[0035] The first hole H**1** may have therein a wetting layer **5** interposed between the first barrier/seed layer SL**1** and the external connection terminal **100**. The wetting layer **5** may include, for example, gold. The wetting layer **5** may reduce or prevent oxidation of the under-bump UBM

and/or the first barrier/seed layer SL**1**, may have improved wettability to the external connection terminal **100**, may reduce or prevent contact failure between the under-bump UBM and the external connection terminal **100**, and may reduce or prevent delamination of the external connection terminal **100**.

[0036] The first barrier/seed layer SL**1**, the wetting layer **5**, and the external connection terminal **100** may all be in contact with the inner sidewall SS of the first hole H**1**. The first barrier/seed layer SL**1**, the wetting layer **5**, and the first terminal part **100***a* of the external connection terminal **100** may have their sidewalls that are aligned with each other. For example, the first barrier/seed layer SL**1**, the wetting layer **5**, and the first terminal part **100***a* of the external connection terminal **100** may have their sidewalls that are disposed on a single straight line.

[0037] The first barrier/seed layer SL**1** (or the barrier layer thereof) may serve to reduce or prevent a constituent metal of the under-bump UBM from diffusing into the wetting layer **5** and the external connection terminal **100**. Therefore, the first barrier/seed layer SL**1** may reduce or prevent a constituent metal of the under-bump UBM from reacting with a constituent material of the wetting layer **5** and a constituent material of the external connection terminal **100**. Accordingly, a void may be reduced or prevented from forming between the under-bump UBM and the external connection terminal **100**, and thus it may be possible to reduce or prevent contact failure and/or cracking between the under-bump UBM and the external connection terminal **100** and delamination of the external connection terminal **100**.

[0038] Furthermore, as shown in FIG. **3**A, an acute angle, or the first angle θ**1**, may be made between the sidewall **100**S**1** of the first terminal part **100***a* and the top surface **100**S**2** of the second terminal part **100***b*, and thus the external connection terminal **100** may be difficult to escape from the first hole H**1**. Accordingly, the external connection terminal **100** may be reduced or prevented from delamination.

[0039] Moreover, according to some example embodiments of the present inventive concepts, the first dielectric layer IL**1** may partially cover and partially expose the under-bump UBM to thereby constitute a solder mask defined (SMD) structure, and accordingly, stress may be reduced between the under-bump UBM and the first dielectric layer IL**1** and delamination of the under-bump UBM may be reduced or prevented. As a result, the semiconductor package **1000** may increase in reliability.

[0040] Referring also to FIG. **3**A, the second dielectric layer IL**2** may cover the under-bumps UBM and the first dielectric layer IL**1**. The under-bumps UBM may directly contact the second dielectric layer IL**2**. The first barrier/seed layer SL**1** may not be interposed between the second dielectric layer IL**2** and the under-bump UBM. Therefore, a constituent metal of the under-bump UBM may partially diffuse into the second dielectric layer IL**2**, and thus the constituent metal of the under-bump UBM and oxygen inside the second dielectric layer IL**2** may react with each other to form a metal oxide layer CO of FIG. **3**B. The metal oxide layer CO may be positioned between the under-bump UBM and the second dielectric layer IL**2**. In addition, because the constituent metal of the under-bump UBM partially diffuses into the second dielectric layer IL**2**, as shown in FIG. **3**B, void regions VD may be formed on a surface of the under-bump UBM.

[0041] Referring back to FIGS. **1** and **2**, a first redistribution pattern RP**1** may be interposed between the second dielectric layer IL**2** and the third dielectric layer IL**3**. A second barrier/seed layer SL**2** may be interposed between the first redistribution pattern RP**1** and the second dielectric layer IL**2** and between the first redistribution pattern RP**1** and the under-bump UBM.

[0042] A second redistribution pattern RP**2** may be interposed between the third dielectric layer IL**3** and the fourth dielectric layer IL**4**. A third barrier/seed layer SL**3** may be interposed between the second redistribution pattern RP**2** and the third dielectric layer IL**3** and between the second redistribution pattern RP**2** and the first redistribution pattern RP**1**.

[0043] A substrate conductive pattern **10** may be disposed on the fourth dielectric layer IL**4**. A portion of the substrate conductive pattern **10** may penetrate the fourth dielectric layer IL**4** and may

be connected to the second redistribution pattern RP**2**. A fourth barrier/seed layer SL**4** may be interposed between the substrate conductive pattern **10** and the fourth dielectric layer IL**4** and between the substrate conductive pattern **10** and the second redistribution pattern RP**2**.

[0044] The first redistribution pattern RP**1**, the second redistribution pattern RP**2**, and the substrate conductive pattern **10** may include, for example, one or more of copper, nickel, aluminum, and gold. The second to fourth barrier/seed layers SL**2** to SL**4** may have the same material and structure as those of the first barrier/seed layer SL**1**.

[0045] Each of the first and second redistribution patterns RP**1** and RP**2** may include a via part VP and a line part LP that is positioned on the via part VP and has a linear shape. The via part VP and the line part LP may be integrally connected into a single piece. The via part VP may have a width that decreases in a downward direction. For example, the via part VP of the first redistribution pattern RP**1** may have a fifth width W**5** in the one direction as shown in FIG. **3**B. The fifth width W**5** may increase in an upward direction. The fifth width W**5** may be less than the first to fourth widths W**1** to W**4**.

[0046] The first semiconductor device CH**1** may be a single semiconductor die or chip, or a semiconductor package that includes a plurality of semiconductor dies of the same type or different types. The first semiconductor device CH**1** may be one selected from an image sensor chip such as CMOS image sensor (CIS), a microelectromechanical system (MEMS) device chip, an application specific integrated circuit (ASIC) chip, and a memory device chip such as Flash memory, DRAM, SRAM, EEPROM, PRAM, MRAM, ReRAM, HBM (high bandwidth memory), and HMC (hybrid memory cubic).

[0047] The first semiconductor device CH**1** may be flip-chip bonded through first internal connection members **110** to the first redistribution substrate RD**1**. The first internal connection members **110** may electrically connect the substrate conductive patterns **10** to chip pads **105** of the first semiconductor device CH**1**. The first internal connection members **110** may include one or more of solder balls, conductive bumps, and conductive pillars. The first internal connection members **110** may include one or more of tin, lead, silver, copper, nickel, and gold.

[0048] The first mold layer MD**1** may cover a sidewall of the first semiconductor device CH**1**, a top surface of the first semiconductor device CH**1**, and a top surface of the first redistribution substrate RD**1**. The first mold layer MD**1** may include a dielectric resin, such as epoxy molding compound (EMC). The first mold layer MD**1** may further include fillers, and the fillers may be dispersed in the dielectric resin.

[0049] A first under-fill layer UF**1** may be interposed between the first semiconductor device CH**1** and the first redistribution substrate RD**1**. The first under-fill layer UF**1** may include a thermo-curable resin or a photo-curable resin. In addition, the first under-fill layer UF**1** may further include organic fillers or inorganic fillers.

[0050] FIGS. **5**A to **5**I illustrate enlarged partial cross-sectional views showing a method of fabricating the semiconductor package of FIG. **1** according to some example embodiments of the present inventive concepts.

[0051] Referring to FIG. **5**A, a carrier substrate CB may be prepared. The carrier substrate CB may be, for example, a transparent glass substrate. A release layer RL may be formed on the carrier substrate CB. The release layer RL may include an epoxy resin. The release layer RL may exhibit, for example, photodegradability or thermodegradability. An etch stop layer EL may be formed on the release layer RL. The etch stop layer EL may include a conductive material having an etch selectivity with respect to the release layer RL. For example, the etch stop layer EL may include metal, such as titanium. A first dielectric layer IL**1** may be formed on the etch stop layer EL. The first dielectric layer IL**1** may be formed by coating, exposure, and development processes. The exposure and development processes may cause the first dielectric layer IL**1** to form including first holes H**1** that expose the etch stop layer EL.

[0052] Additionally, the first dielectric layer IL**1** may be cured. Therefore, the first dielectric layer

IL**1** may contract. In some example embodiments, the first dielectric layer IL**1** may have a bottom surface IL**1**B that is in contact with the etch stop layer EL and is fixed by the etch stop layer EL, and thus the first dielectric layer IL**1** may be difficult to contract a lower portion thereof. In contrast, the first dielectric layer IL**1** may have a top surface IL**1**U that is not fixed by the etch stop layer EL, and thus the first dielectric layer IL**1** may be easy to contract an upper portion thereof. The first holes H**1** may thus have their inclined inner sidewalls SS. For example, the inner sidewalls SS of the first holes H**1** may make a first angle θ**1** with the bottom surface IL**1**B of the first dielectric layer IL**1**. The inner sidewalls SS of the first holes H**1** may make a second angle θ**2** with the top surface IL**1**U of the first dielectric layer IL**1**. The first angle θ**1** may be less than the second angle θ**2**.

[0053] Referring to FIG. **5**B, a sacrificial pattern SP and a wetting layer **5** may be sequentially formed in the first hole H**1**. The sacrificial pattern SP and the wetting layer **5** may each be formed by electroplating. The sacrificial pattern SP and the wetting layer **5** may not completely fill the first hole H**1** and may expose an upper portion of the inner sidewall SS of the first hole H**1**. The sacrificial pattern SP may include a conductive material having an etch selectivity with respect to both the etch stop layer EL and the wetting layer **5**. The sacrificial pattern SP may include metal different from those of the etch stop layer EL and the wetting layer **5**. For example, the sacrificial pattern SP may include nickel. The wetting layer **5** may include gold (Au).

[0054] Referring to FIG. **5**C, a first barrier/seed layer SL**1** may be conformally formed on the wetting layer **5** and the first dielectric layer IL**1**. The first barrier/seed layer SL**1** may be formed by sequentially stacking a barrier layer and a seed layer. A first mask pattern PR**1** may be formed on the first barrier/seed layer SL**1**. The first mask pattern PR**1** may include a first opening OP**1** that overlaps the first hole H**1**. The first opening OP**1** may expose the first barrier/seed layer SL**1**. The first mask pattern PR**1** may be, for example, a photoresist pattern. An electroplating process may be performed to form an under-bump UBM on the first barrier/seed layer SL**1**. The under-bump UBM may fill the first hole H**1** and may fill at least a portion of the first opening OP**1**. The under-bump UBM may expose a top surface of the first mask pattern PR**1**.

[0055] Referring to FIGS. **5**C and **5**D, the first mask pattern PR**1** may be removed to expose a top surface of the first barrier/seed layer SL**1** and a lateral surface of the under-bump UBM. When the first mask pattern PR**1** is a photoresist pattern, an ashing process may be employed to remove the first mask pattern PR**1**. The first barrier/seed layer SL**1** exposed on a side of the under-bump UBM may be removed to expose the top surface IL**1**U of the first dielectric layer IL**1**.

[0056] Referring also to FIG. **5**E, a second dielectric layer IL**2** may be formed on the under-bump UBM and the first dielectric layer IL**1**. The second dielectric layer IL**2** may be formed by coating, exposure, development, and curing processes. The second dielectric layer IL**2** may be formed to include a second hole H**2** that exposes a top surface of the under-bump UBM. A second barrier/seed layer SL**2** may be conformally formed on the second dielectric layer IL**2**. A second mask pattern PR**2** may be formed on the second barrier/seed layer SL**2**. The second mask pattern PR**2** may be, for example, a photoresist pattern. The second mask pattern PR**2** may be formed to include a second opening OP**2** that overlaps the second hole H**2** and exposes a portion of the second barrier/seed layer SL**2**. An electroplating process may be performed to form a first redistribution pattern RP**1** in the second hole H**2** and the second opening OP**2**. The first redistribution pattern RP**1** may be formed to include a via part VP that fills the second hole H**2** and a line part LP that lies in the second opening OP**2**.

[0057] Referring to FIGS. **5**E and **5**F, the second mask pattern PR**2** and its underlying second barrier/seed layer SL**2** may be removed to expose a top surface of the second dielectric layer IL**2**.

[0058] Referring to FIG. **5**G, a third dielectric layer IL**3** may be formed to expose the first redistribution pattern RP**1** and the second dielectric layer IL**2**. A third barrier/seed layer SL**3** and a second redistribution pattern RP**2** may be formed by using the same method as that discussed with reference to FIGS. **5**E and **5**F. A fourth dielectric layer IL**4** may be formed to cover the second

redistribution pattern RP**2** and the third dielectric layer IL**3**. A fourth barrier/seed layer SL**4** and a substrate conductive pattern **10** may be formed by using the same method as that discussed with reference to FIGS. **5**E and **5**F. Accordingly, a first redistribution substrate RD**1** may be formed.
[0059] Referring to FIGS. **1**, **5**G, and **5**H, a first internal connection member **110** may be used to mount a first semiconductor device CH**1** on the first redistribution substrate RD**1**. A first under-fill layer UF**1** may be formed between the first semiconductor device CH**1** and the first redistribution substrate RD**1**. A first mold layer MD**1** may be formed to cover the first redistribution substrate RD**1** and the first semiconductor device CH**1**.
[0060] Referring to FIGS. **5**H and **5**I, the carrier substrate CB may be separated from the etch stop layer EL. When the release layer RL is a photo-degradable layer, an ultraviolet ray UV may be irradiated through the carrier substrate CB to the release layer RL so as to separate the carrier substrate CB. Alternatively, when the release layer RL is a thermo-degradable layer, high-temperature heat may be applied through the carrier substrate CB to the release layer RL so as to separate the carrier substrate CB. Alternatively, a lateral surface of the release layer RL may be provided with a mechanical force to physically separate the carrier substrate CB from the etch stop layer EL. After the separation of the carrier substrate CB, at least a portion of the release layer RL may remain on the etch stop layer EL. A first etching process may be performed in which the release layer RL may be removed to expose a surface of the etch stop layer EL. In some example embodiments, the etch stop layer EL may reduce or prevent the wetting layer **5** from receiving a first etchant used for the first etching process. A second etching process may be performed in which the etch stop layer EL may be removed to expose a bottom surface of the first dielectric layer IL**1** and a bottom surface of the sacrificial pattern SP. The sacrificial pattern SP may reduce or prevent the wetting layer **5** from receiving a second etchant used for the second etching process. A third etching process may be performed in which the sacrificial pattern SP may be removed to expose a surface of the wetting layer **5** and a lower inner sidewall of the first hole H**1**. Subsequently, referring back to FIG. **2**, an external connection terminal **100** may be bonded to the wetting layer **5** exposed through the first hole H**1**. A singulation process may be performed to separate semiconductor packages from each other. Accordingly, a semiconductor package **1000** may be eventually fabricated as shown in FIGS. **1** and **2**.
[0061] In a method of fabricating a semiconductor package according to some example embodiments of the present inventive concepts, the etch stop layer EL and the sacrificial pattern SP may be used such that the wetting layer **5**, the first barrier/seed layer SL**1**, and the under-bump UBM may be formed without failure thereof. As a result, a yield may increase.
[0062] Moreover, the semiconductor package fabrication method may include an operation of forming the wetting layer **5**, and thus it may be possible to reduce or prevent oxidation of the under-bump UBM and/or the first barrier/seed layer SL**1**. Therefore, contact failure may be reduced or prevented between the under-bump UBM and the external connection terminal **100**. In addition, when the wetting layer **5** is absent, a problem may occur in which the external connection terminal **100** is not bonded to the under-bump UBM or the first barrier/seed layer SL**1**. The present inventive concepts may include an operation of forming the wetting layer **5**, and accordingly may reduce or prevent process failure and may increase a yield.
[0063] FIG. **6** illustrates a cross-sectional view showing a semiconductor package according to some example embodiments of the present inventive concepts.
[0064] Referring to FIG. **6**, a semiconductor package **1001** according to the present example embodiments may be configured such that a first semiconductor device CH**1** and a second semiconductor device CH**2** may be mounted side by side on the first redistribution substrate RD**1**. The first semiconductor device CH**1** may be spaced apart from the second semiconductor device CH**2**. The first under-fill layer UF**1** may be interposed between the first semiconductor device CH**1** and the first redistribution substrate RD**1**. A second under-fill layer UF**2** may be interposed between the second semiconductor device CH**2** and the first redistribution substrate RD**1**. The first

and second semiconductor devices CH**1** and CH**2** may be of the same type or of different types. The first mold layer MD**1** may cover the first semiconductor device CH**1** and the second semiconductor device CH**2**. In the present example embodiments, two semiconductor devices CH**1** and CH**2** are mounted side by side, but the number of the semiconductor devices CH**1** and CH**2** may be three or more. Other configurations may be identical or similar to those discussed with reference to FIGS. **1** to **4**.

[0065] FIG. **7** illustrates a cross-sectional view showing a semiconductor package according to some example embodiments of the present inventive concepts.

[0066] Referring to FIG. **7**, a semiconductor package **1002** according to the present example embodiments may include a first redistribution substrate RD**1** including a first substrate conductive pattern **10***a* and a second substrate conductive pattern **10***b*. The first substrate conductive pattern **10***a* may be connected to the first internal connection member **110**. The semiconductor package **1002** may further include a second redistribution substrate RD**2** disposed on the first mold layer MD**1** and a mold via MV that penetrates the first mold layer MD**1** and connects the first redistribution substrate RD**1** to the second redistribution substrate RD**2**. The mold via MV may contact the second substrate conductive pattern **10***b*. The mold via MV may include a conductive material, such as copper. The mold via MV may directly contact the first mold layer MD**1**.

[0067] The second redistribution substrate RD**2** may include fifth, sixth, and seventh dielectric layers IL**5**, IL**6**, and IL**7** that are sequentially stacked. The fifth to seventh dielectric layers IL**5** to IL**7** may each include a photo-imageable dielectric (PID) layer. A third redistribution pattern RP**3** may be interposed between the fifth dielectric layer IL**5** and the sixth dielectric layer IL**6**. A fifth barrier/seed layer SL**5** may be interposed between the third redistribution pattern RP**3** and the fifth dielectric layer IL**5**. The third redistribution pattern RP**3** may be connected to the mold via MV. A fourth redistribution pattern RP**4** may be interposed between the sixth dielectric layer IL**6** and the seventh dielectric layer IL**7**. A sixth barrier/seed layer SL**6** may be interposed between the fourth redistribution pattern RP**4** and the sixth dielectric layer IL**6**. The third and fourth redistribution patterns RP**3** and RP**4** may each include a via part VP and a line part LP. A third substrate conductive pattern **20** may be disposed on the seventh dielectric layer IL**7**. A seventh barrier/seed layer SL**7** may be interposed between the third substrate conductive pattern **20** and the seventh dielectric layer IL**7**. The third redistribution pattern RP**3**, the fourth redistribution pattern RP**4**, and the third substrate conductive pattern **20** may each include, for example, one or more of copper, nickel, aluminum, and gold. The fifth to seventh barrier/seed layers SL**5** to SL**7** may each have the same material and structure as those of the first barrier/seed layer SL**1**. Other configurations may be identical or similar to those discussed with reference to FIGS. **1** to **4**.

[0068] FIG. **8** illustrates a cross-sectional view showing a semiconductor package according to some example embodiments of the present inventive concepts.

[0069] Referring to FIG. **8**, a semiconductor package **1003** according to the present example embodiments may include a first sub-semiconductor package PK**1** and a second sub-semiconductor package PK**2** stacked on the first sub-semiconductor package PK**1**. The first sub-semiconductor package PK**1** may have a structure the same as or similar to that of the semiconductor package **1002** of FIG. **7**. The second sub-semiconductor package PK**2** may include a first package substrate SB**1**, a second semiconductor device CH**2** mounted on the first package substrate SB**1**, and a second mold layer MD**2** that covers the second semiconductor device CH**2** and the first package substrate SB**1**. The second semiconductor device CH**2** may be electrically connected to the first package substrate SB**1** through, for example, a wire **360**. The second semiconductor device CH**2** may be a single semiconductor die or chip, or a semiconductor package that includes a plurality of semiconductor dies of the same type or different types. The second semiconductor device CH**2** may be one selected from an image sensor chip such as CMOS image sensor (CIS), a microelectromechanical system (MEMS) device chip, an application specific integrated circuit (ASIC) chip, and a memory device chip such as Flash memory, DRAM, SRAM, EEPROM,

PRAM, MRAM, ReRAM, HBM (high bandwidth memory), and HMC (hybrid memory cubic).
[0070] The second mold layer MD**2** may include the same material as that of the first mold layer MD**1**. The wire **360** may include copper or gold. The first package substrate SB**1** may be, for example, bi-layered or multi-layered printed circuit board. The first package substrate SB**1** may include an upper conductive pattern **380** disposed on a top surface thereof and a lower conductive pattern **382** disposed on a bottom surface thereof. The first package substrate SB**1** may have therein an internal wiring line (not shown) to connect the upper conductive pattern **380** to the lower conductive pattern **382**. The upper and lower conductive patterns **380** and **382** may include, for example, one or more of gold, copper, aluminum, and nickel.
[0071] The first sub-semiconductor package PK**1** may be connected through a second internal connection member **120** to the second sub-semiconductor package PK**2**. The second internal connection member **120** may connect the lower conductive pattern **382** to the third substrate conductive pattern **20**. The second internal connection member **120** may include one or more of solder balls, conductive bumps, and conductive pillars. The second internal connection member **120** may include one or more of tin, lead, silver, copper, nickel, and gold. Other configurations may be identical or similar to those discussed with reference to FIG. **7**.
[0072] FIG. **9** illustrates a cross-sectional view showing a semiconductor package according to some example embodiments of the present inventive concepts.
[0073] Referring to FIG. **9**, a semiconductor package **1004** according to the present example embodiments may include a first sub-semiconductor package PK**1** including a first redistribution substrate RD**1**, a connection substrate **900** and a first semiconductor device CH**1** that are mounted on the first redistribution substrate RD**1**, a first mold layer MD**1** that covers the connection substrate **900** and the first semiconductor device CH**1**, and a second redistribution substrate RD**2** on the first mold layer MD**1**.
[0074] A first under-fill layer UF**1** may be interposed between the first semiconductor device CH**1** and the first redistribution substrate RD**1**. The connection substrate **900** may include a cavity region CV at a center thereof. The first semiconductor device CH**1** may be disposed in the cavity region CV. The connection substrate **900** may include a plurality of base layers **910** and a conductive structure **920**. The base layers **910** may include a dielectric material. For example, the base layers **910** may include a carbon-based material, a ceramic, or a polymer. The conductive structure **920** may include a connection pad **921**, a first connection via **922**, a connection line **923**, and a second connection via **924**.
[0075] The connection substrate **900** may be connected through a third internal connection member **130** to the first redistribution substrate RD**1**. A second under-fill layer UF**2** may be interposed between the connection substrate **900** and the first redistribution substrate RD**1**. The first mold layer MD**1** may fill a space between the first semiconductor device CH**1** and an inner sidewall of the cavity region CV of the connection substrate **900**. The second under-fill layer UF**2** may include the same material as that of the first under-fill layer UF**1**.
[0076] A subsidiary via **30** may penetrate the first mold layer MD**1** and may connect the second connection via **924** of the connection substrate **900** to the third redistribution pattern RP**3** of the second redistribution substrate RD**2**. A third under-fill layer UF**3** may fill a space between the first sub-semiconductor package PK**1** and the second sub-semiconductor package PK**2**. The third under-fill layer UF**3** may include the same material as that of the first under-fill layer UF**1**. Other configurations may be identical or similar to those discussed with reference to FIG. **8**.
[0077] A semiconductor package according to the present inventive concepts may be configured such that an under-bump and a first dielectric layer may have therebetween a first barrier/seed layer to reduce or prevent the under-bump from being delaminated from the first dielectric layer. Moreover, the first barrier/seed layer may be interposed between the under-bump and an external connection terminal, and may thus reduce or prevent delamination of the external connection terminal.

[0078] Furthermore, the under-bump and the external connection terminal may have therebetween a wetting layer to reduce or prevent contact failure between the under-bump and the external connection terminal and delamination of the external connection terminal.
[0079] In addition, an acute angle, or a first angle, may be made between a sidewall of a first terminal part of the external connection terminal and a top surface of a second terminal part of the external connection terminal, and thus the external connection terminal may be difficult to escape from a first hole. Accordingly, the external connection terminal may be reduced or prevented from delamination.
[0080] A method of fabricating a semiconductor package according to the present inventive concepts, an etch stop layer and a sacrificial pattern may be used such that a wetting layer, a first barrier/seed layer, and an under-bump may be formed without failure thereof. As a result, a yield may increase.
[0081] Although the present inventive concepts have been described in connection with some example embodiments of the present inventive concepts illustrated in the accompanying drawings, it will be understood to those skilled in the art that various changes and modifications may be made without departing from the technical spirit and essential feature of the present inventive concepts. The above disclosed example embodiments should thus be considered illustrative and not restrictive. The example embodiments of FIGS. **1** to **9** may be combined with each other.

Claims

1. A method of fabricating a semiconductor package, the method comprising: forming a redistribution substrate; mounting a semiconductor device on the redistribution substrate; and bonding an external connection terminal to the redistribution substrate, wherein the forming the redistribution substrate includes sequentially stacking a release layer and an etch stop layer on a carrier substrate, coating a first dielectric layer on the etch stop layer, exposing and developing the first dielectric layer so that the first dielectric layer defines a first hole therein that exposes the etch stop layer, sequentially stacking a sacrificial pattern and a wetting layer in the first hole, the wetting layer exposing an upper portion of an inner sidewall of the first hole, forming a first barrier/seed layer and an under-bump on the wetting layer, and removing the carrier substrate, the release layer, the etch stop layer, and the sacrificial pattern to expose a bottom surface of the wetting layer and a bottom surface of the first dielectric layer, wherein the external connection terminal is bonded to the wetting layer.
2. The method of claim 1, wherein, before the sequentially stacking the sacrificial pattern and the wetting layer in the first hole, the forming the redistribution substrate further includes curing the first dielectric layer to incline the inner sidewall of the first hole.
3. The method of claim 1, wherein the forming the first barrier/seed layer and the under-bump on the wetting layer includes: conformally forming the first barrier/seed layer on the first dielectric layer and the wetting layer; forming on the first barrier/seed layer a mask pattern, the mask pattern defining an opening that overlaps the first hole; forming the under-bump in the opening and the first hole; removing the mask pattern to expose the under-bump and the first barrier/seed layer that is adjacent the under-bump; and removing the first barrier/seed layer that is adjacent the under-bump to expose a top surface of the first dielectric layer.
4. The method of claim 3, wherein a width of the opening is greater than a width of the first hole in a direction parallel to the top surface of the first dielectric layer, wherein the under-bump includes a first bump portion in the first hole and a second bump portion in the opening.
5. The method of claim 1, wherein, before separating the carrier substrate from the release layer during the removing the carrier substrate, the release layer, the etch stop layer and the sacrificial pattern, the forming the redistribution substrate further includes: forming a second dielectric layer that covers the first dielectric layer; and forming a redistribution pattern that penetrates the second

dielectric layer and is connected to the under-bump.
6. The method of claim 5, wherein the under-bump is in direct contact with the second dielectric layer, and wherein the first barrier/seed layer is not interposed between the second dielectric layer and the under-bump.
7. The method of claim 6, wherein the forming the second dielectric layer includes forming a metal oxide layer between the second dielectric layer and the under-bump.
8. The method of claim 7, wherein the forming the metal oxide layer includes forming the metal oxide layer as defining a void region between the metal oxide layer and the under-bump.
9. The method of claim 1, wherein the sacrificial pattern includes a conductive material having an etch selectivity with respect to both the etch stop layer and the wetting layer.
10. A method of fabricating a semiconductor package, the method comprising: forming a redistribution substrate; and bonding an external connection terminal to the redistribution substrate, wherein the forming the redistribution substrate includes forming an etch stop layer on a carrier substrate, coating a first dielectric layer on the etch stop layer, exposing and developing the first dielectric layer so that the first dielectric layer defines a first hole penetrating the first dielectric layer, sequentially stacking a sacrificial pattern and a wetting layer in the first hole, the wetting layer exposing an upper portion of an inner sidewall of the first hole, forming a first barrier/seed layer and an under-bump on the wetting layer, and exposing a bottom surface of the wetting layer and a bottom surface of the first dielectric layer, wherein the forming the first barrier/seed layer and the under-bump includes forming the first barrier/seed layer conformally covering a top surface of the first dielectric layer, an exposed upper portion of an inner sidewall of the first hole and a top surface of the wetting layer, and forming the under-bump on the first barrier/seed layer.
11. The method of claim 10, wherein the forming the etch stop layer on the carrier substrate includes: forming a release layer on the carrier substrate; and stacking the etch stop layer on the release layer.
12. The method of claim 11, wherein the exposing the bottom surface of the wetting layer and the bottom surface of the first dielectric layer includes: removing the carrier substrate and the release layer; and removing the etch stop layer and the sacrificial pattern.
13. The method of claim 10, wherein, before the sequentially stacking the sacrificial pattern and the wetting layer in the first hole, the forming the redistribution substrate further includes curing the first dielectric layer to incline the inner sidewall of the first hole, and wherein the inner sidewall of the first hole and a bottom surface of the first dielectric layer form an acute angle.
14. The method of claim 10, wherein the forming the first barrier/seed layer and the under-bump on the wetting layer includes: conformally forming the first barrier/seed layer on the first dielectric layer and the wetting layer; forming on the first barrier/seed layer a mask pattern, the mask pattern defining an opening therein that overlaps the first hole; forming the under-bump in the opening and the first hole; removing the mask pattern to expose the under-bump and the first barrier/seed layer that is adjacent the under-bump; and removing the first barrier/seed layer that is adjacent the under-bump to expose the top surface of the first dielectric layer, wherein a width of the opening is greater than a width of the first hole in a direction parallel to the top surface of the first dielectric layer, and wherein the under-bump includes a first bump portion in the first hole and a second bump portion in the opening.
15. The method of claim 11, wherein the forming the redistribution substrate further comprises separating the carrier substrate from the release layer, and wherein before the separating the carrier substrate from the release layer, the forming the redistribution substrate further includes: forming a second dielectric layer that covers the first dielectric layer and the under-bump; and forming a metal oxide layer between the second dielectric layer and the under-bump, the forming the metal oxide layer comprises forming the metal oxide layer as defining a void region between the metal oxide layer and the under-bump.
16. A method of fabricating a semiconductor package, the method comprising: forming a

redistribution substrate; and bonding an external connection terminal to the redistribution substrate, wherein the forming the redistribution substrate includes forming an etch stop layer on a carrier substrate, coating a first dielectric layer on the etch stop layer, exposing and developing the first dielectric layer so that the first dielectric layer defines a first hole penetrating the first dielectric layer, sequentially stacking a sacrificial pattern and a wetting layer in the first hole, the wetting layer exposing an upper portion of an inner sidewall of the first hole, forming a first barrier/seed layer and an under-bump on the wetting layer, forming a second dielectric layer that covers the first dielectric layer and the under-bump, forming a metal oxide layer between the second dielectric layer and the under-bump, and exposing a bottom surface of the wetting layer and a bottom surface of the first dielectric layer.

17. The method of claim 16, wherein the forming the first barrier/seed layer and the under-bump on the wetting layer includes: conformally forming the first barrier/seed layer on the first dielectric layer and the wetting layer; forming on the first barrier/seed layer a mask pattern, the mask pattern defining an opening therein that overlaps the first hole; forming the under-bump in the opening and the first hole; and removing the mask pattern to expose the under-bump and the first barrier/seed layer that is adjacent the under-bump; and removing the first barrier/seed layer that is adjacent the under-bump to expose a top surface of the first dielectric layer.

18. The method of claim 16, wherein, before the sequentially stacking the sacrificial pattern and the wetting layer in the first hole, the forming the redistribution substrate further includes: curing the first dielectric layer to incline the inner sidewall of the first hole, wherein the inner sidewall of the first hole and the bottom surface of the first dielectric layer form an acute angle.

19. The method of claim 16, wherein the forming the metal oxide layer further includes forming the metal oxide as defining a void region between the metal oxide layer and the under-bump.

20. The method of claim 16, wherein the forming the etch stop layer on the carrier substrate includes: forming a release layer on the carrier substrate; and stacking the etch stop layer on the release layer.