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(12) **United States Patent**
Nishioka

(10) **Patent No.:** **US 12,389,702 B2**
(45) **Date of Patent:** **Aug. 12, 2025**

(54) **SOLID-STATE IMAGING ELEMENT**

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(72) Inventor: **Yuta Nishioka**, Kanagawa (JP)

(73) Assignee: **SONY SEMICONDUCTOR SOLUTIONS CORPORATION**, Kanagawa (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 452 days.

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(22) PCT Filed: **Mar. 6, 2020**

(86) PCT No.: **PCT/JP2020/009837**
§ 371 (c)(1),
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(30) **Foreign Application Priority Data**
Mar. 13, 2019 (JP) 2019-045759

(51) **Int. Cl.**
H04N 5/3745 (2011.01)
H04N 25/771 (2023.01)
H10F 39/00 (2025.01)

(52) **U.S. Cl.**
CPC ***H10F 39/811*** (2025.01); ***H04N 25/771*** (2023.01); ***H10F 39/8057*** (2025.01); ***H10F 39/809*** (2025.01)

(58) **Field of Classification Search**
CPC H01L 27/14636; H01L 27/14623; H01L 27/14634; H10F 39/811; H10F 39/8057; H10F 39/809; H04N 25/771
See application file for complete search history.

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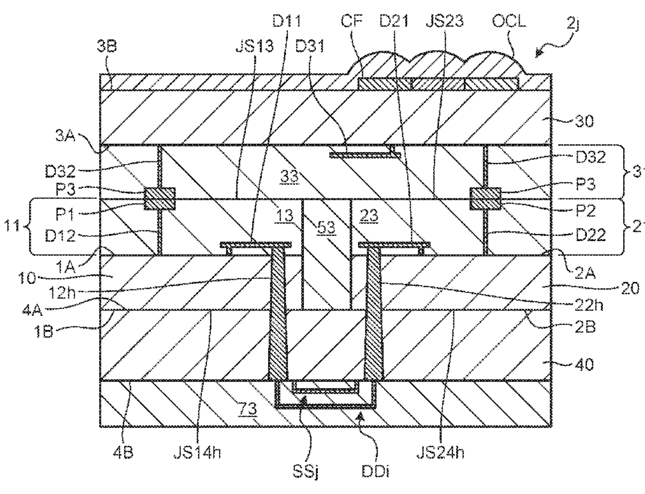
Primary Examiner — Jarrett J Stark
(74) *Attorney, Agent, or Firm* — CHIP LAW GROUP

(57) **ABSTRACT**

A solid-state imaging element includes a first semiconductor substrate having a first semiconductor circuit on a first surface of the substrate, a second semiconductor substrate having a second semiconductor circuit on a second surface of the substrate, and a pixel substrate having a pixel circuit on one surface of the substrate, in which the first semiconductor substrate, the second semiconductor substrate, and the pixel substrate are joined to each other such that the first surface of the first semiconductor substrate and the second surface of the second semiconductor substrate face the one surface of the pixel substrate, and the first semiconductor circuit and the second semiconductor circuit are connected

(Continued)



to each other on the first surface side and the second surface side, opposite to the side facing the pixel substrate.

13 Claims, 24 Drawing Sheets

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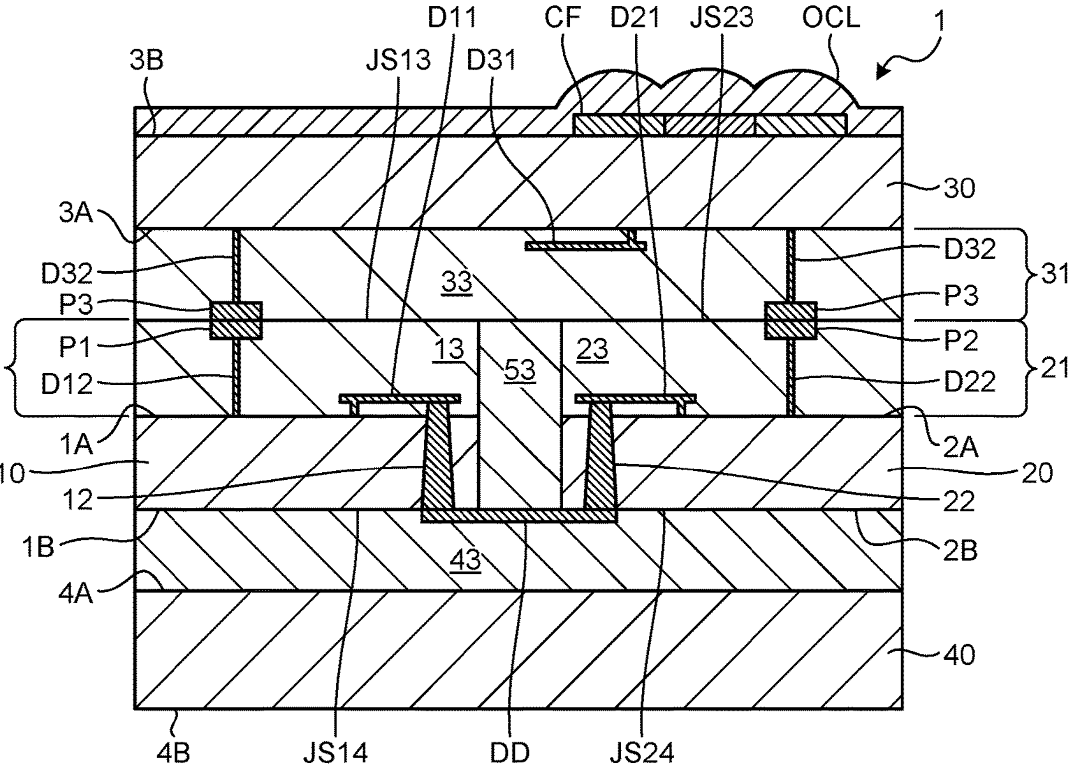
FIG. 1A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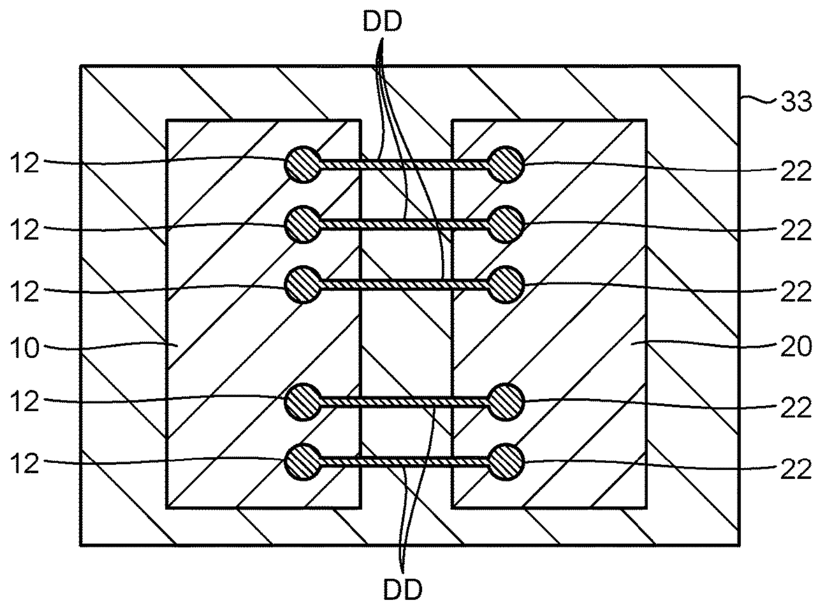
CF
D21
JS23
OCL
1
3B
JS13
D31
30
3A
D32
33
D32
31
P3
P3
11
P1
13
53
23
P2
21
D12
D22
1A
2A
10
20
12
22
1B
43
2B
4A
40
4B
JS14
DD
JS24

FIG. 1B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12
22
DD

FIG. 2A

FIG. 2B

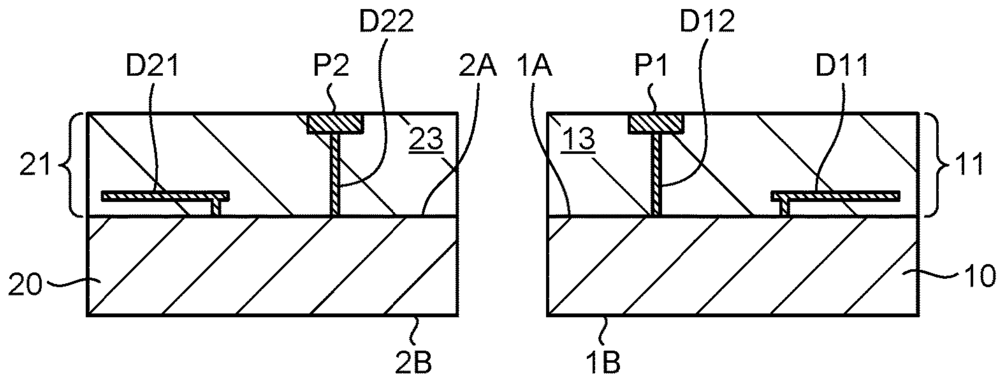


FIG. 2C

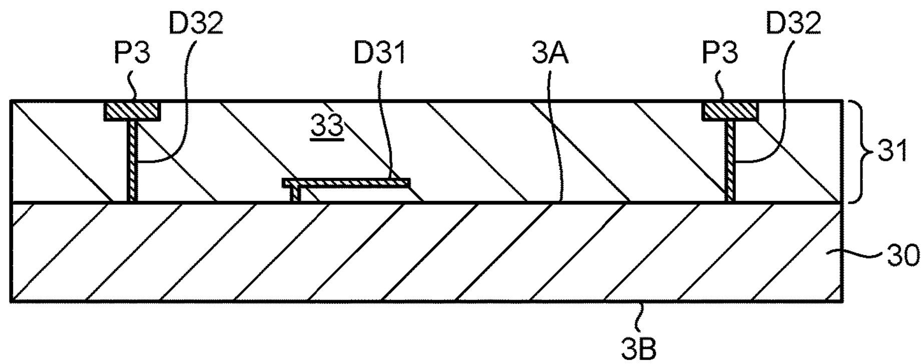


FIG. 2D

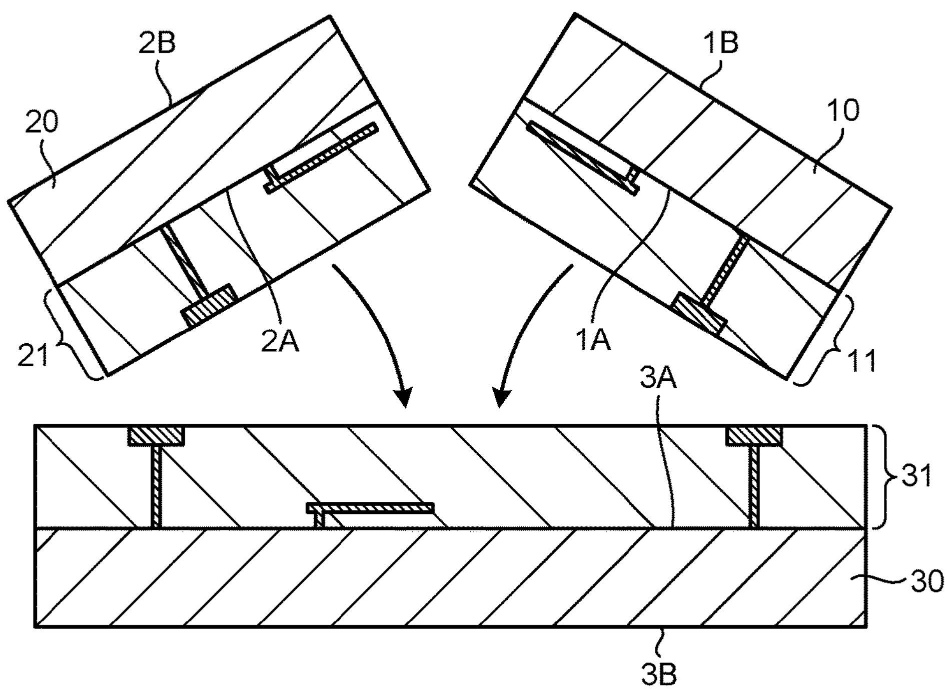


FIG. 3A

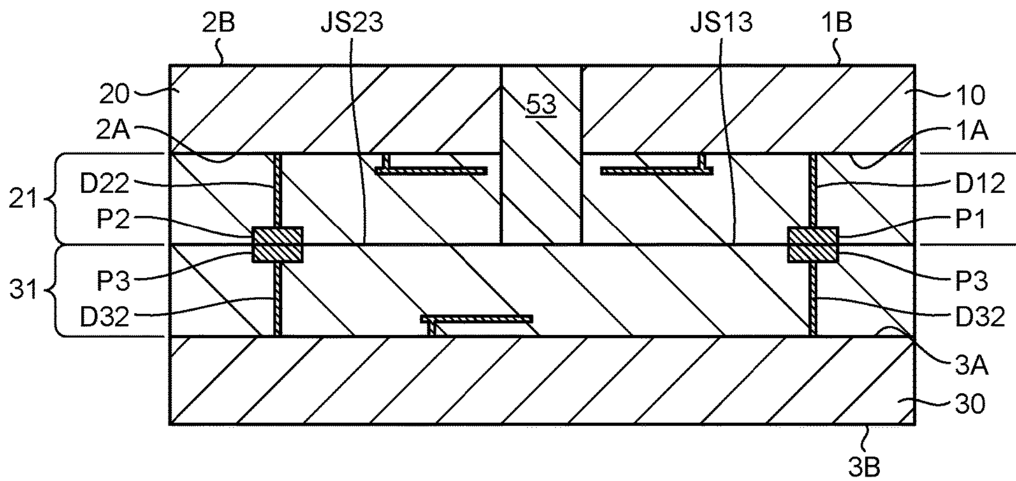


FIG. 3B

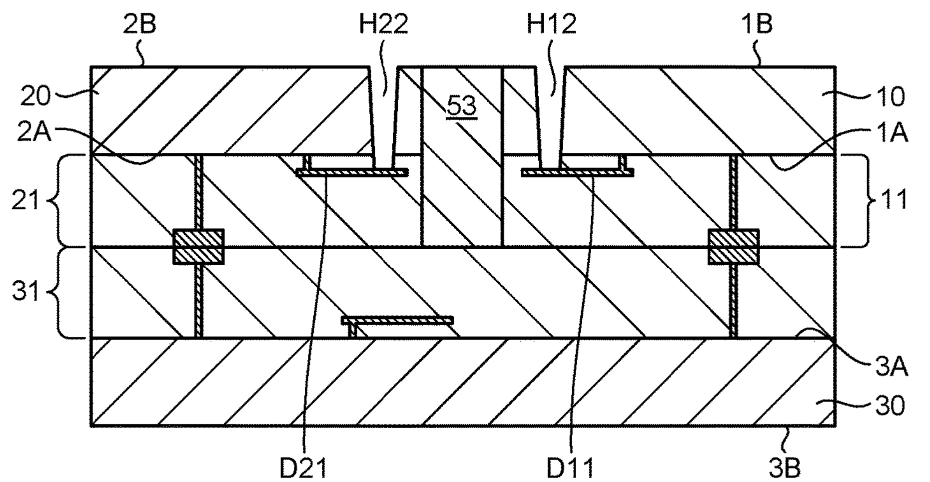


FIG. 3C

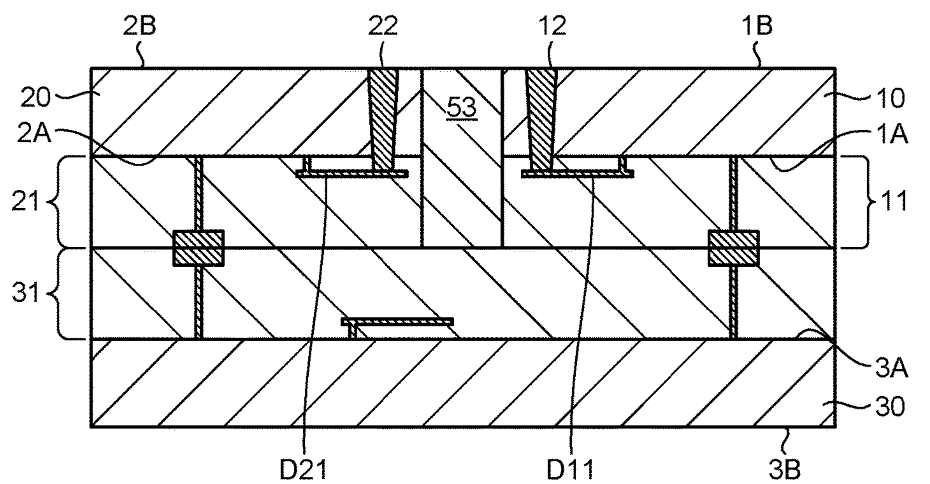


FIG. 4A

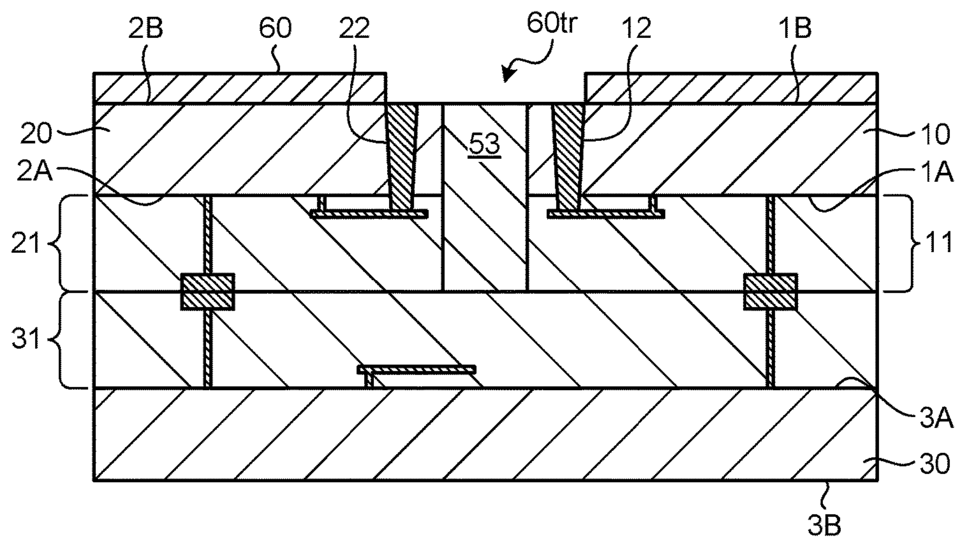


FIG. 4B

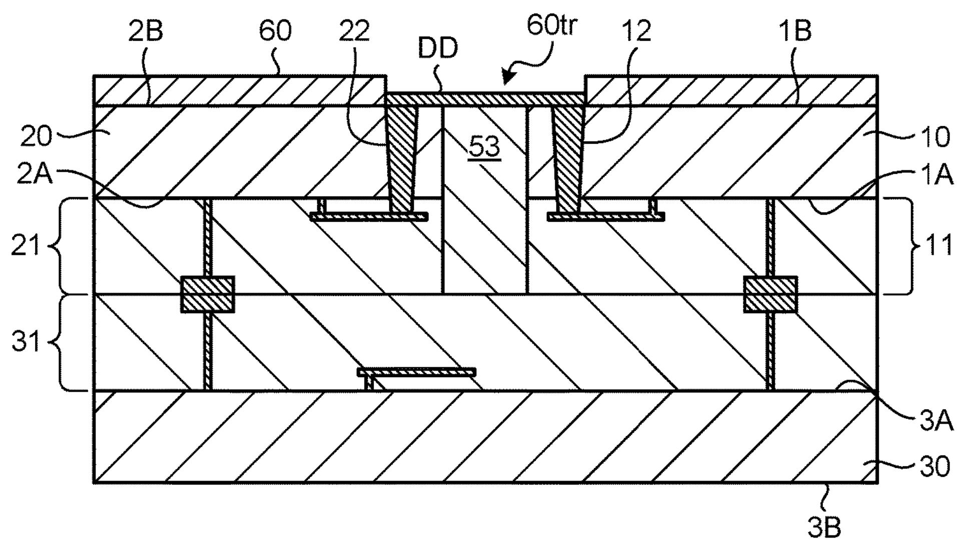


FIG. 4C

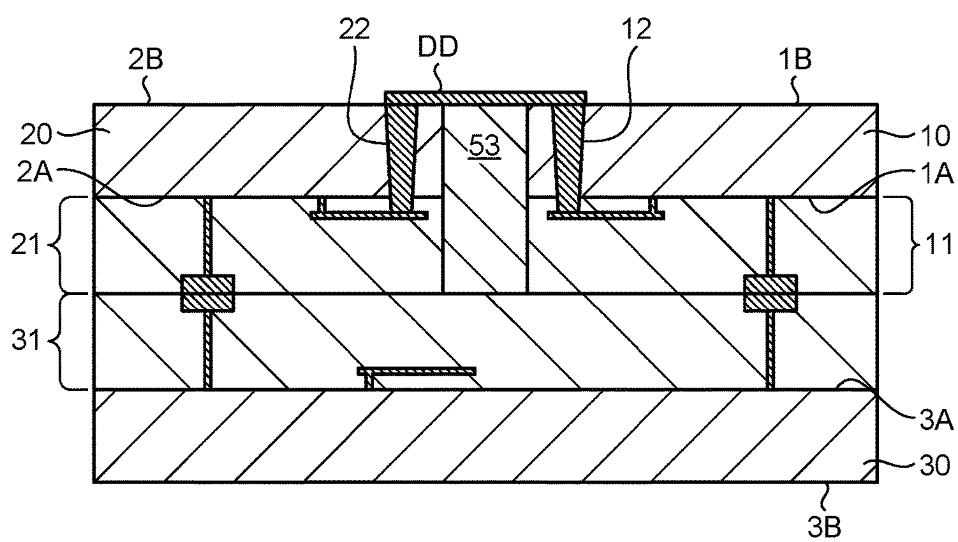
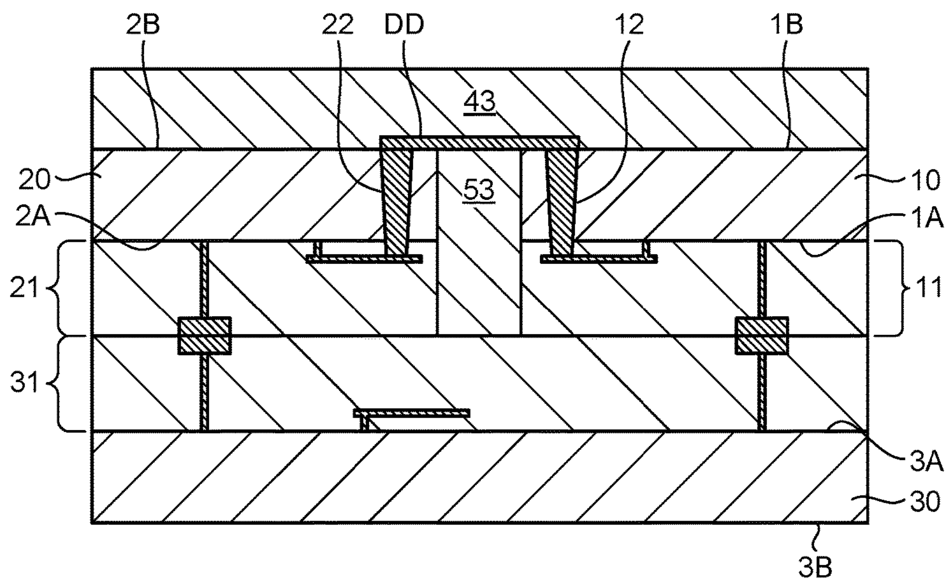


FIG. 5A


2B
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DD
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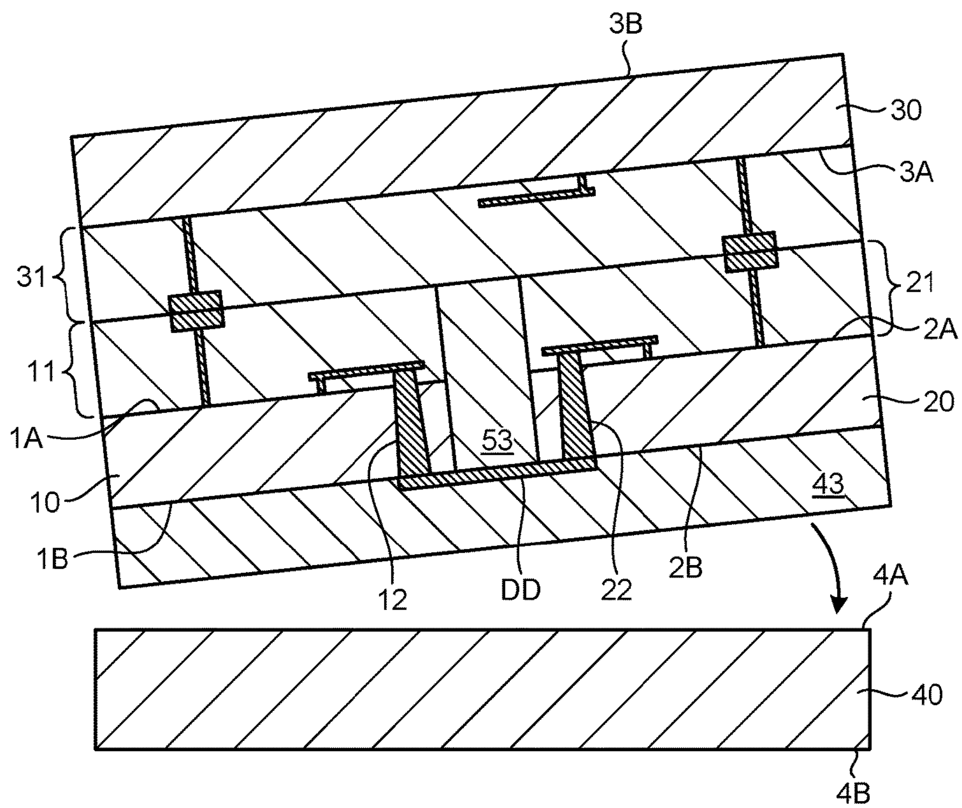
53
10
2A
1A
21
11
31
3A
30
3B

FIG. 5B


3B
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3A
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2A
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1A
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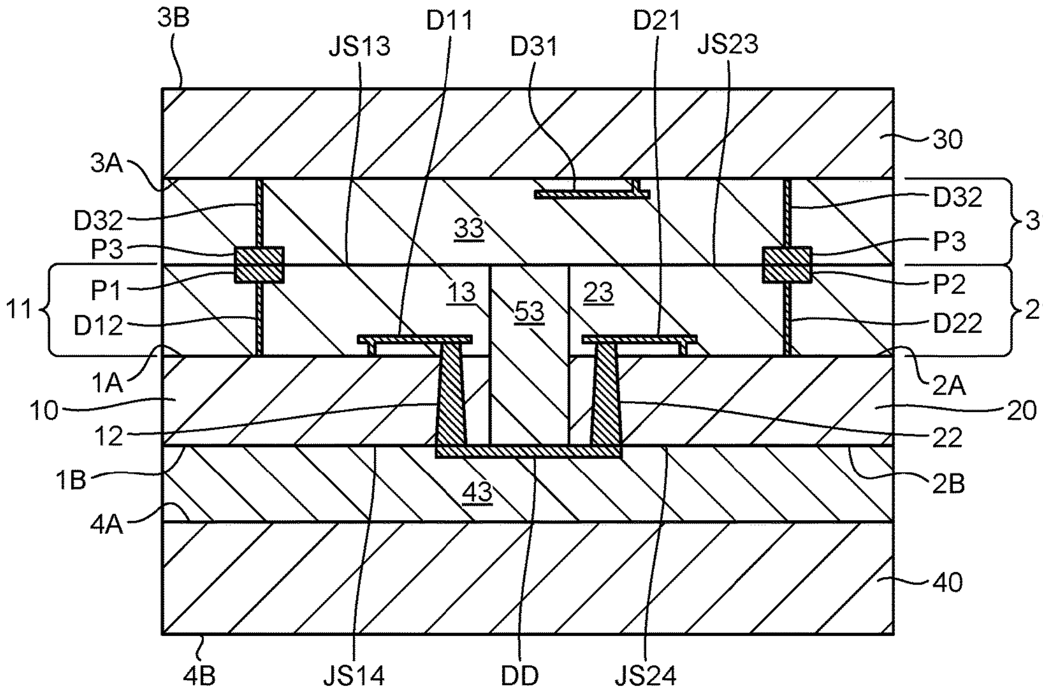
43
10
1B
12
DD
22
2B
4A
40
4B

FIG. 6A



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JS13
D11
D31
D21
JS23
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3A
D32
P3
P1
11
D12
1A
10
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1B
4A
33
13
53
23
43
D32
31
P3
P2
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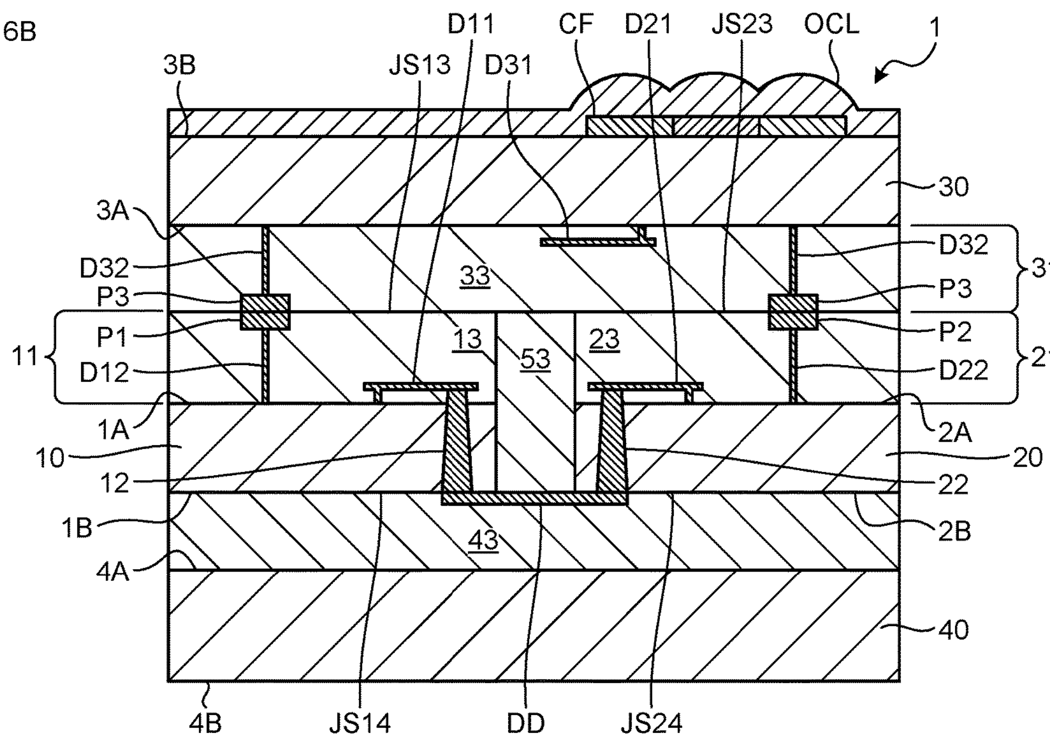
D22
2A
20
22
2B
40
4B
JS14
DD
JS24

FIG. 6B



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3B
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3A
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P3
P1
11
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10
12
1B
4A
33
13
53
23
43
D32
31
P3
P2
21
D22
2A
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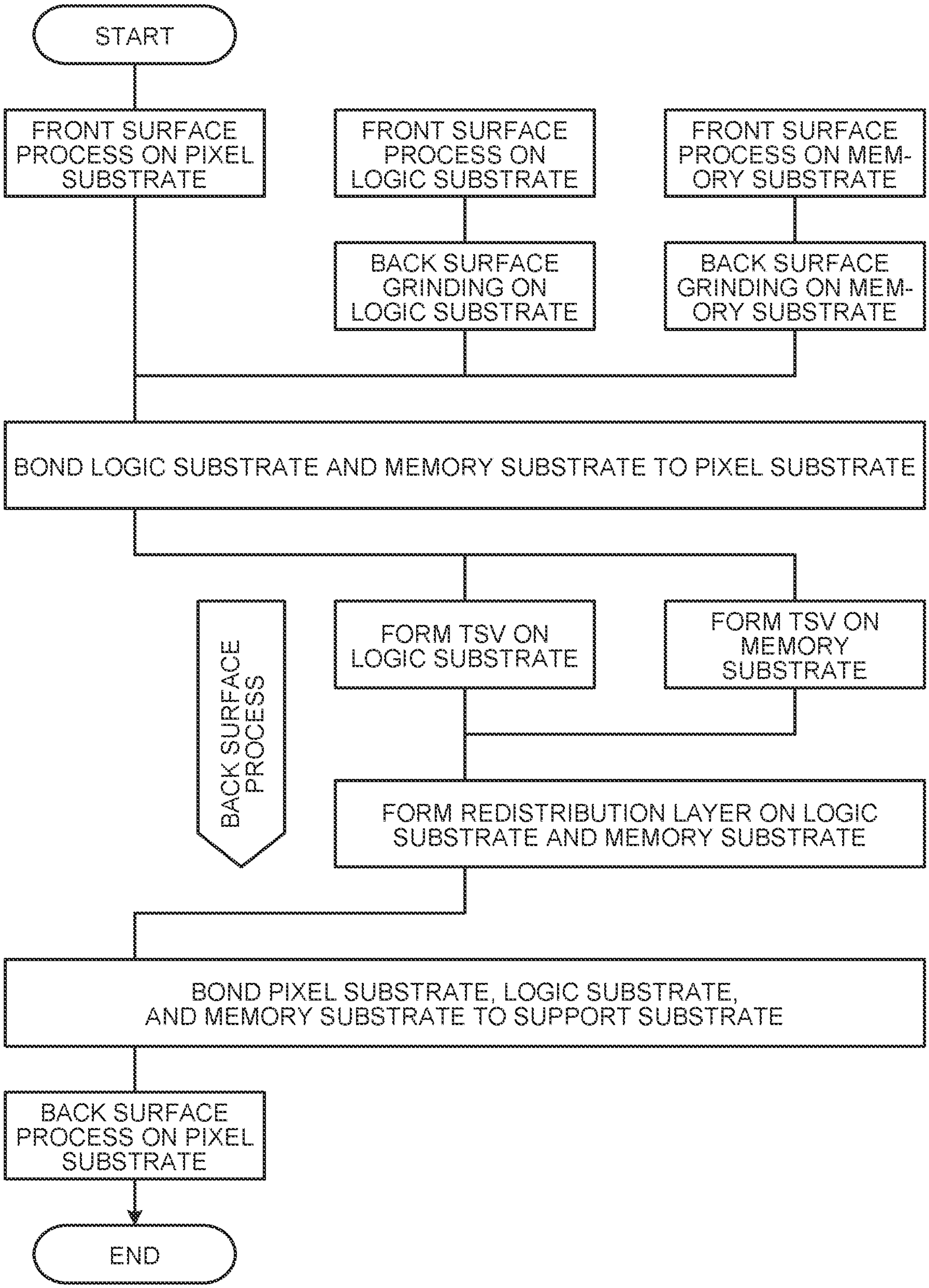
22
2B
40
4B
JS14
DD
JS24

FIG.7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FRONT SURFACE PROCESS ON PIXEL SUBSTRATE
FRONT SURFACE PROCESS ON LOGIC SUBSTRATE
FRONT SURFACE PROCESS ON MEM-ORY SUBSTRATE
BACK SURFACE GRINDING ON LOGIC SUBSTRATE
BACK SURFACE GRINDING ON MEM-ORY SUBSTRATE
BOND LOGIC SUBSTRATE AND MEMORY SUBSTRATE TO PIXEL SUBSTRATE
BACK SURFACE PROCESS
FORM TSV ON LOGIC SUBSTRATE
FORM TSV ON MEMORY SUBSTRATE
FORM REDISTRIBUTION LAYER ON LOGIC SUBSTRATE AND MEMORY SUBSTRATE
BOND PIXEL SUBSTRATE, LOGIC SUBSTRATE, AND MEMORY SUBSTRATE TO SUPPORT SUBSTRATE
BACK SURFACE PROCESS ON PIXEL SUBSTRATE
END

FIG.8

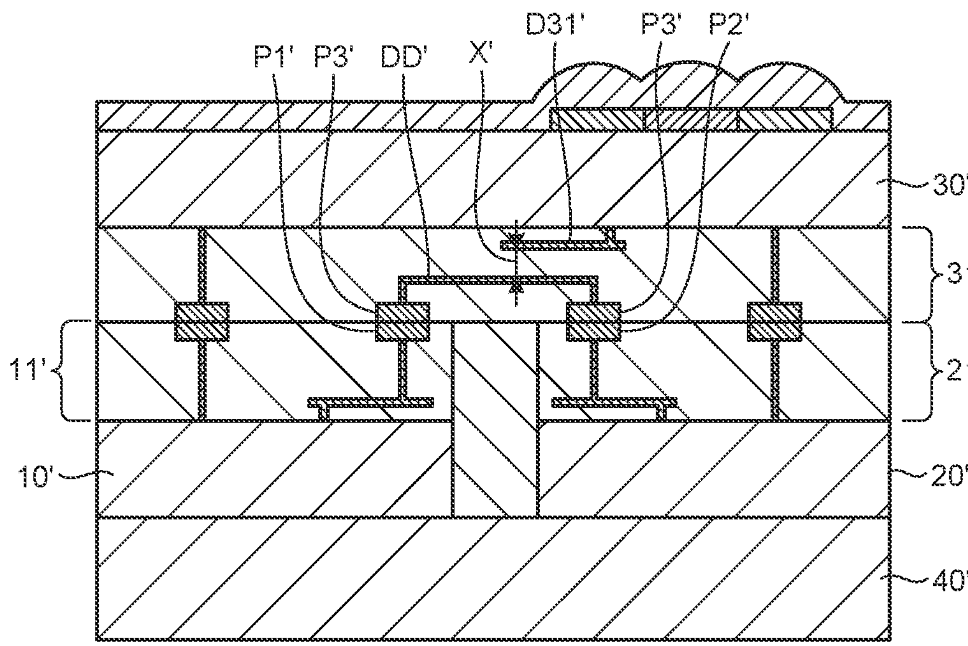


FIG. 9A

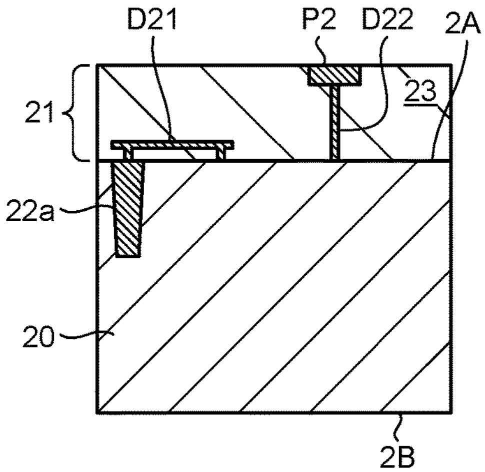


FIG. 9B

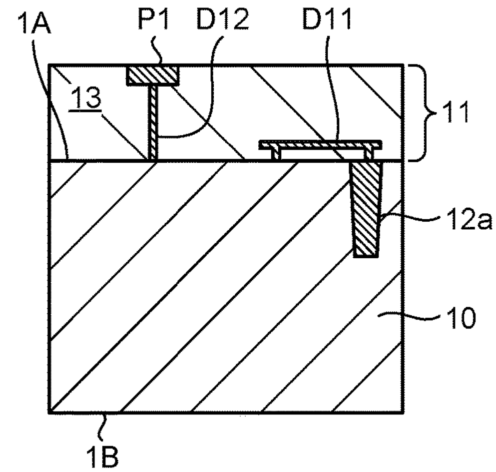


FIG. 9C

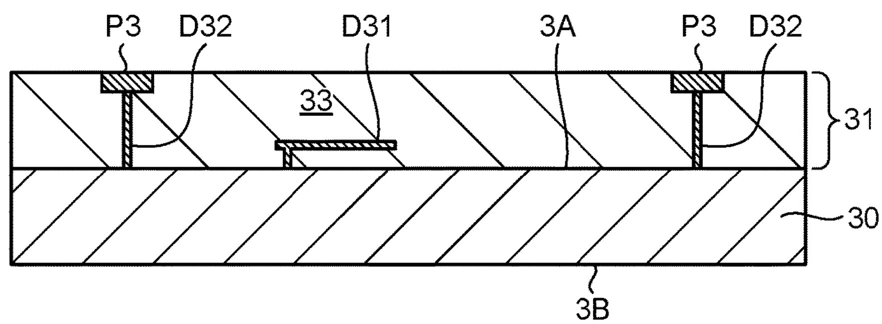


FIG. 9D

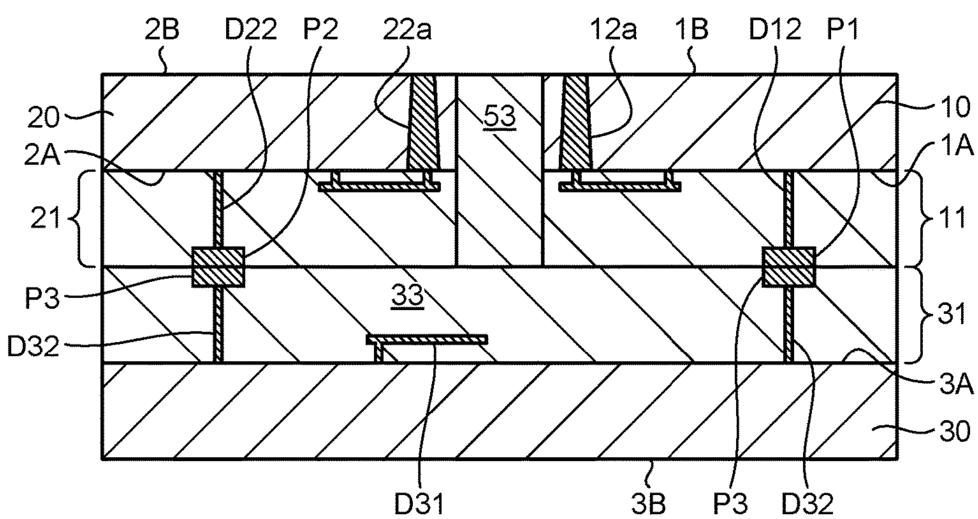


FIG. 10A

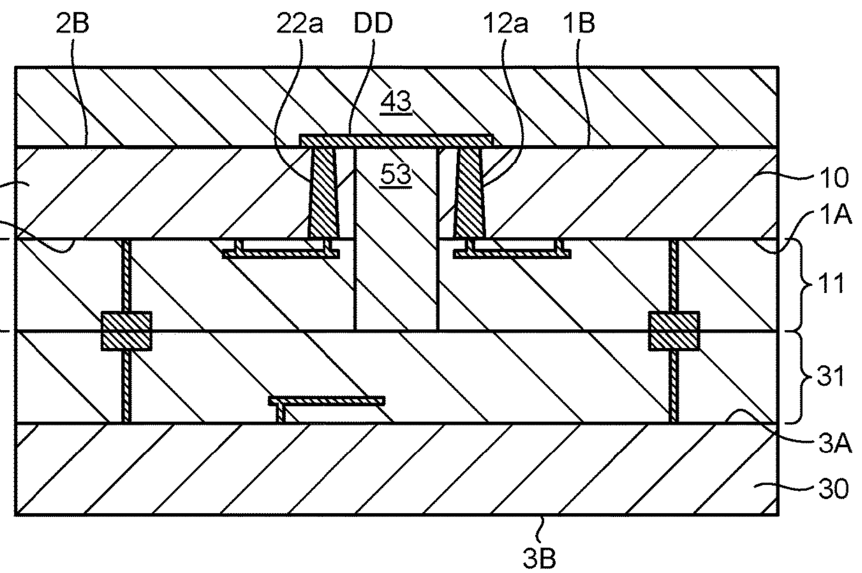


FIG. 10B

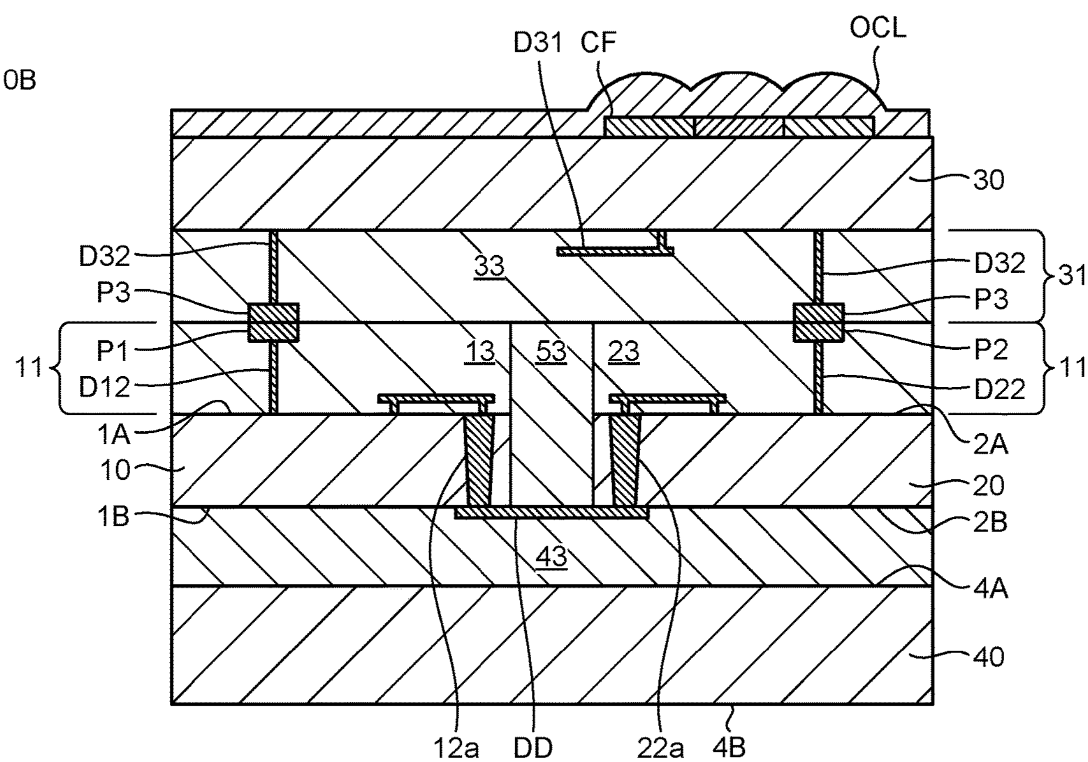
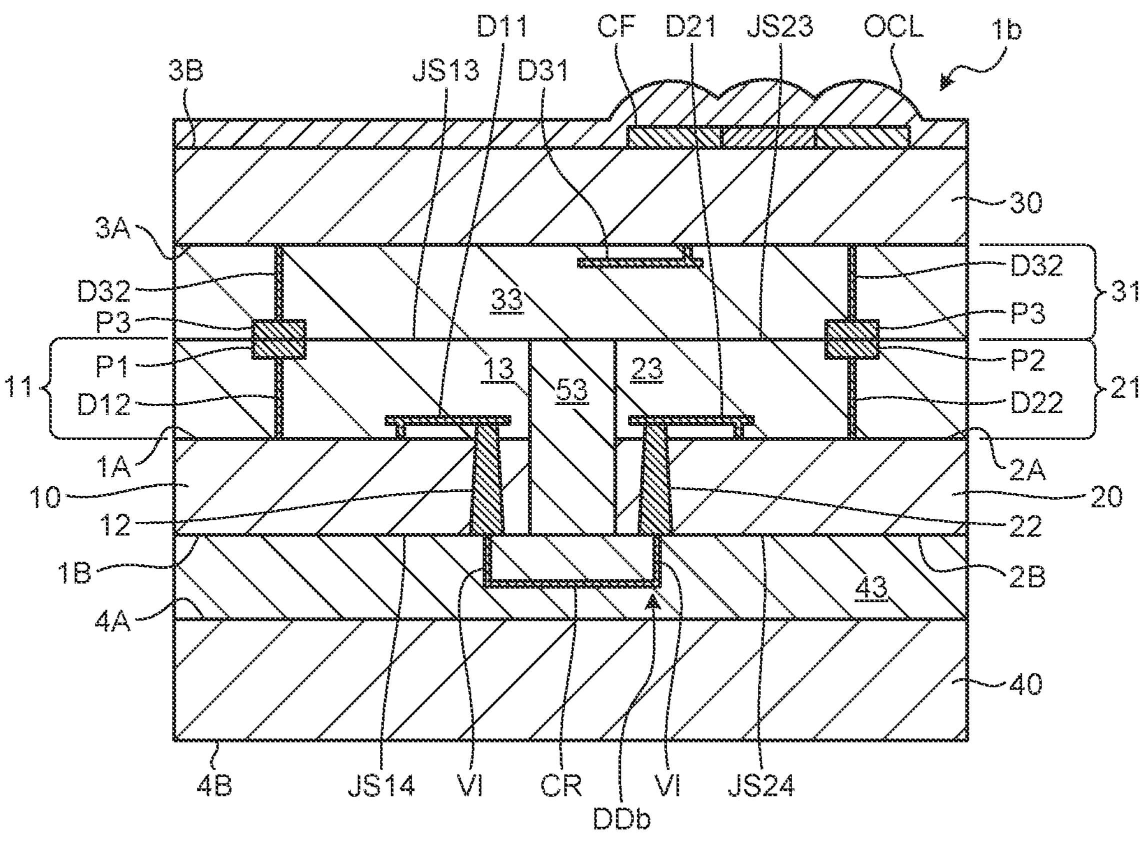


FIG.11



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P2
11
53
21
D12
D22
1A
2A
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1B
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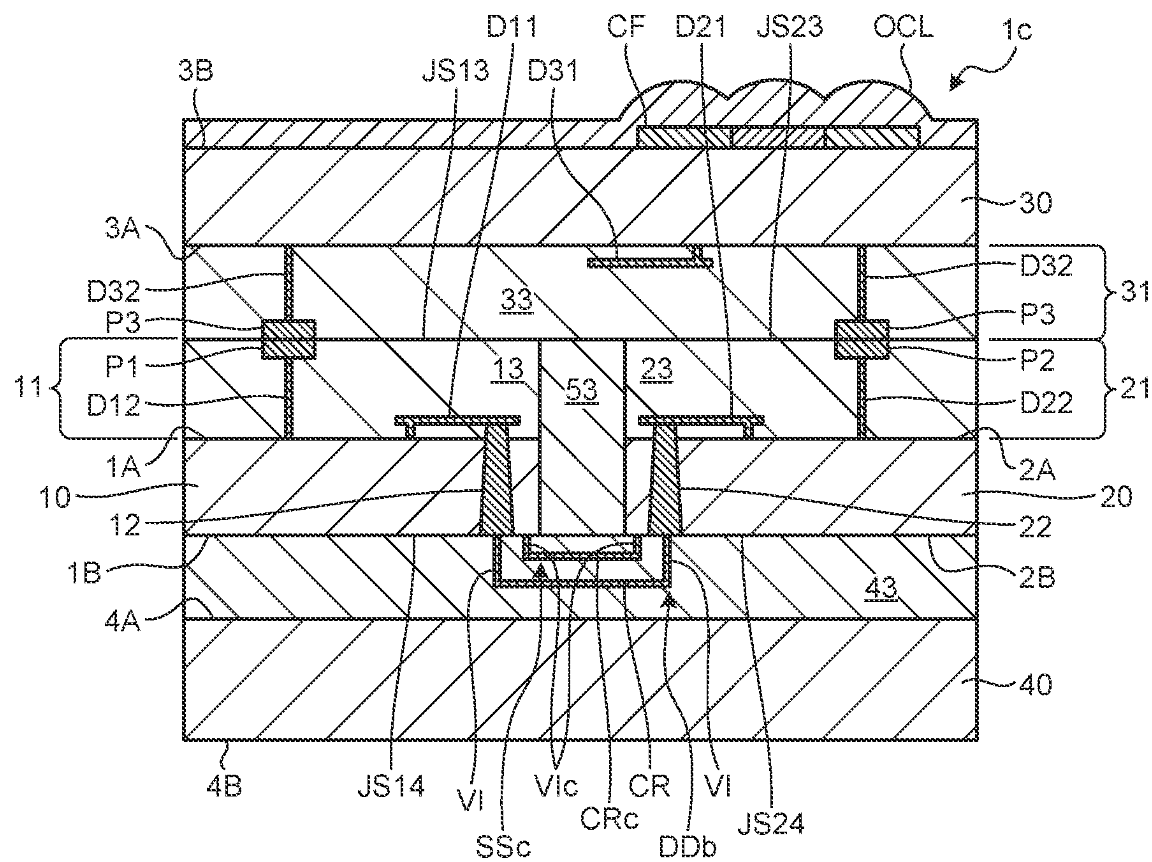
VI
CR
VI
JS24
DDb

FIG.12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D32
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P3
P3
11
P1
13
53
23
P2
21
D12
D22
1A
2A
10
20
12
22
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VIc
CR
VI
JS24
CRc
SSc
DDb

FIG. 13A

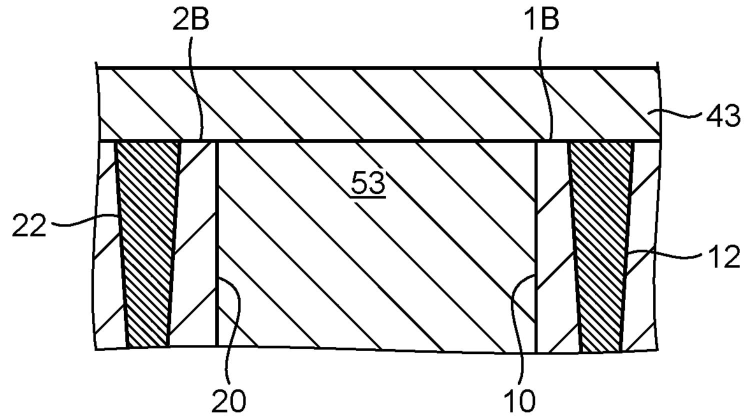


FIG. 13B

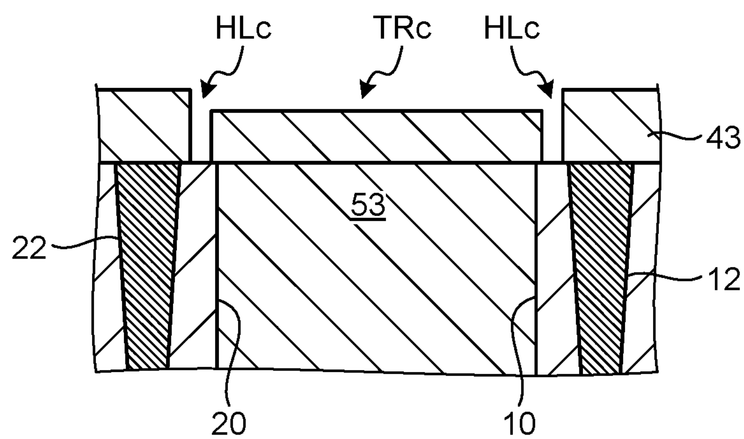


FIG. 13C

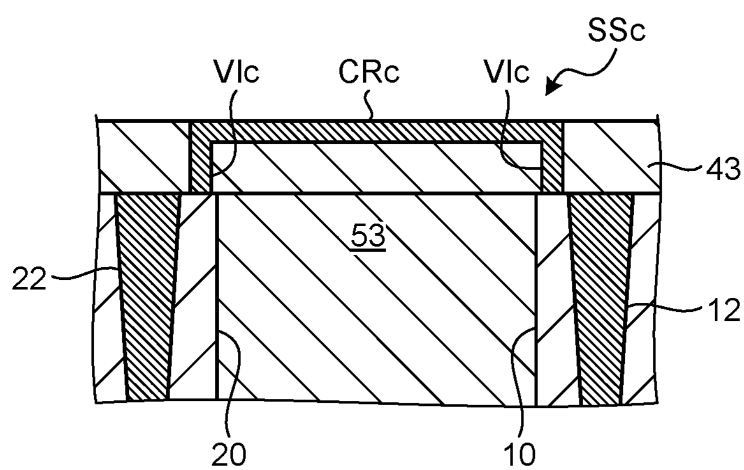


FIG. 14A

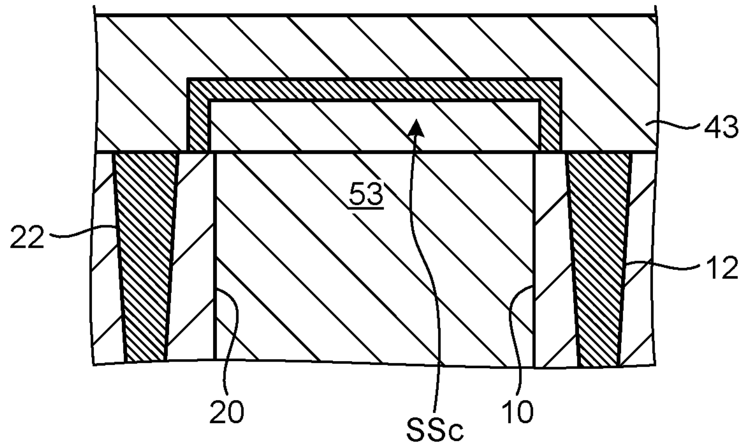


FIG. 14B

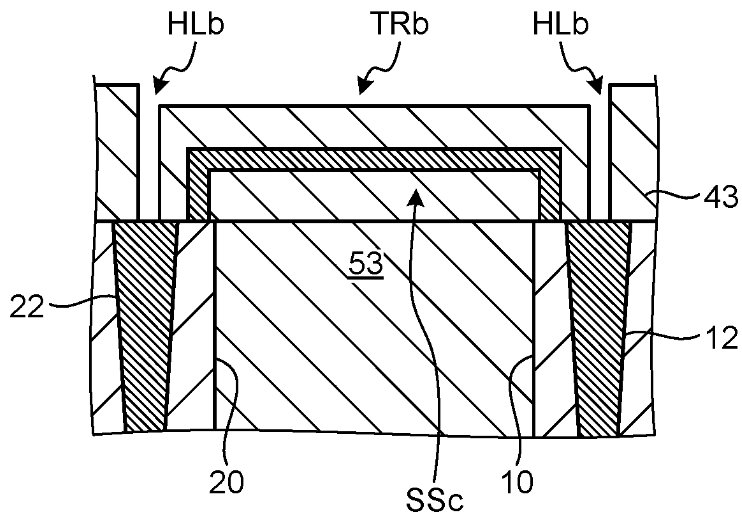


FIG. 14C

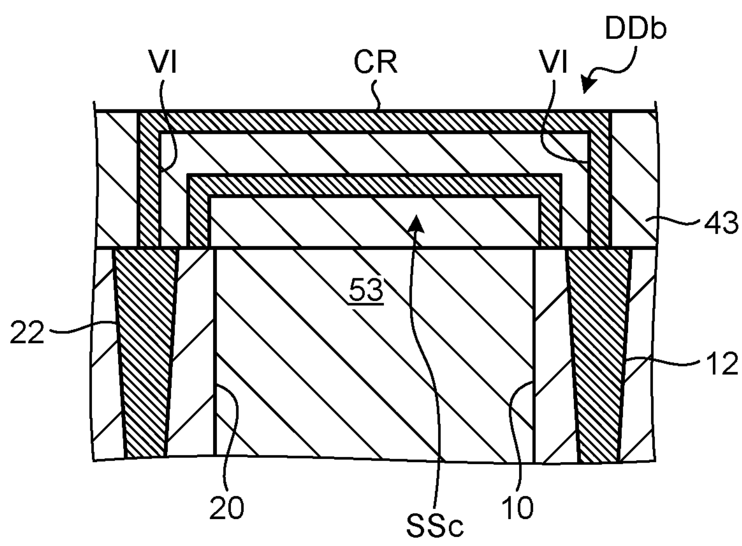
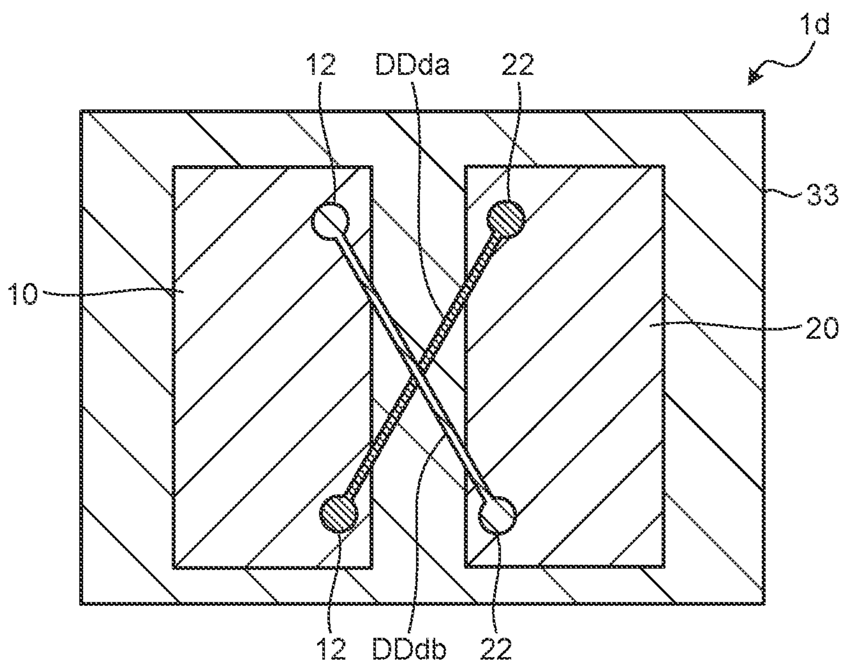


FIG.15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DDdb
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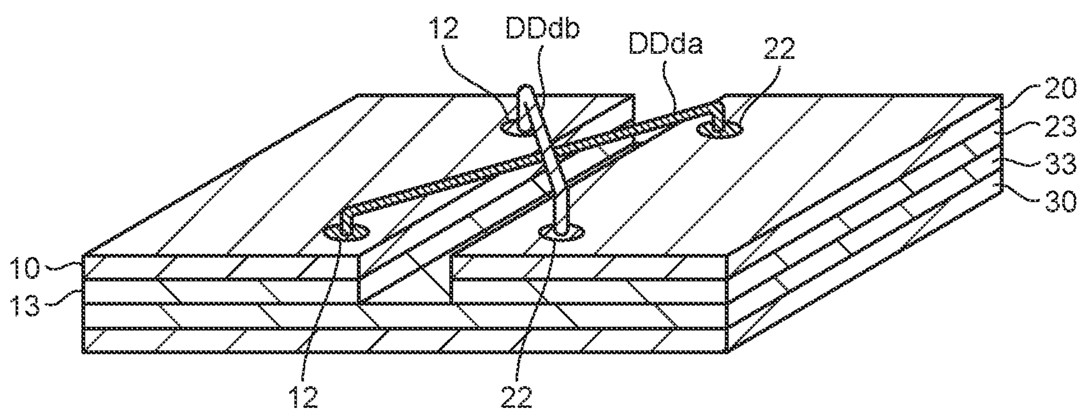
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DDdb
DDda
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23
33
30
10
13
12
22

FIG. 16A

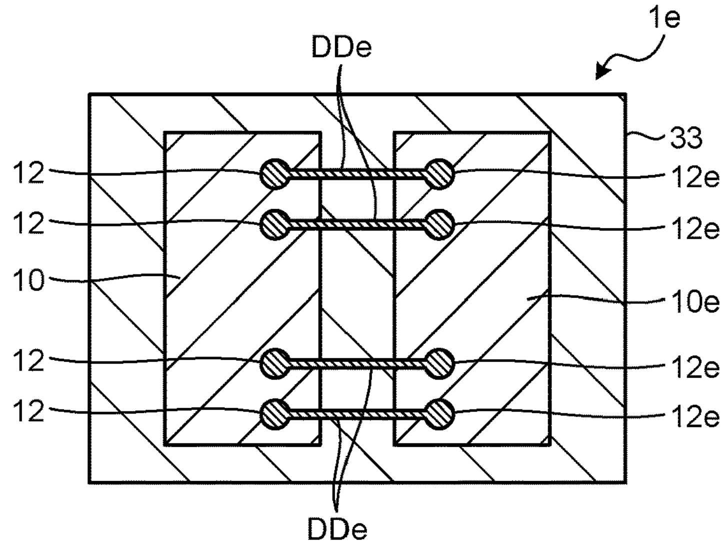


FIG. 16B

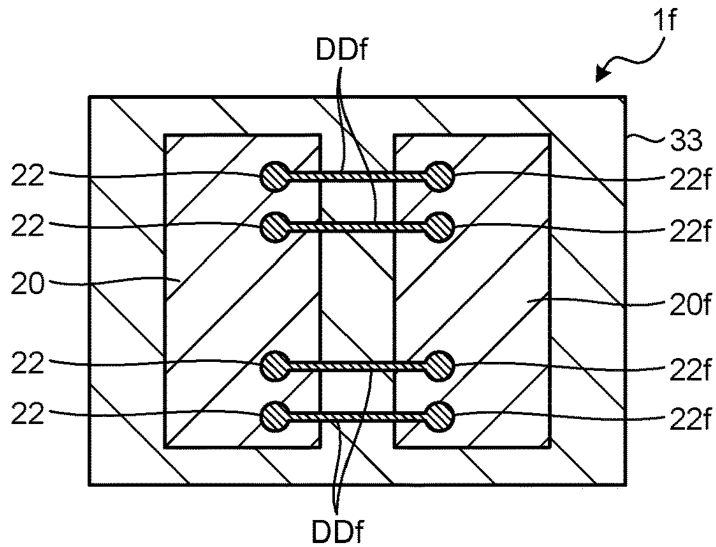


FIG. 16C

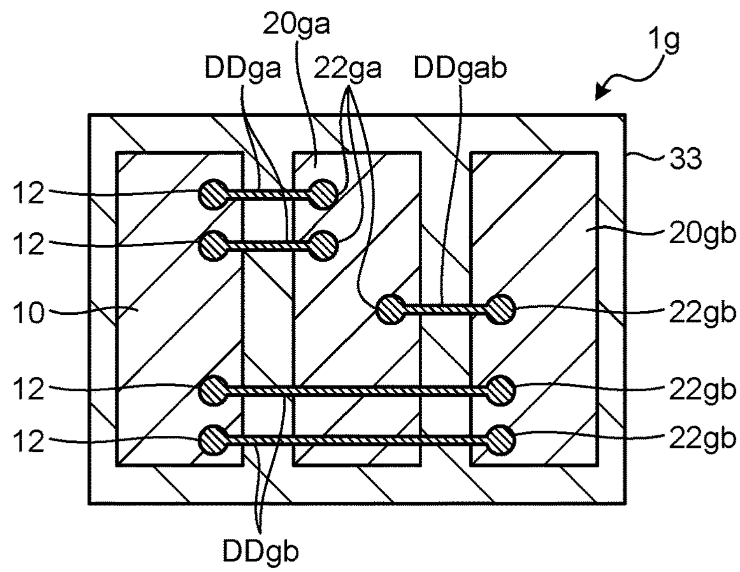
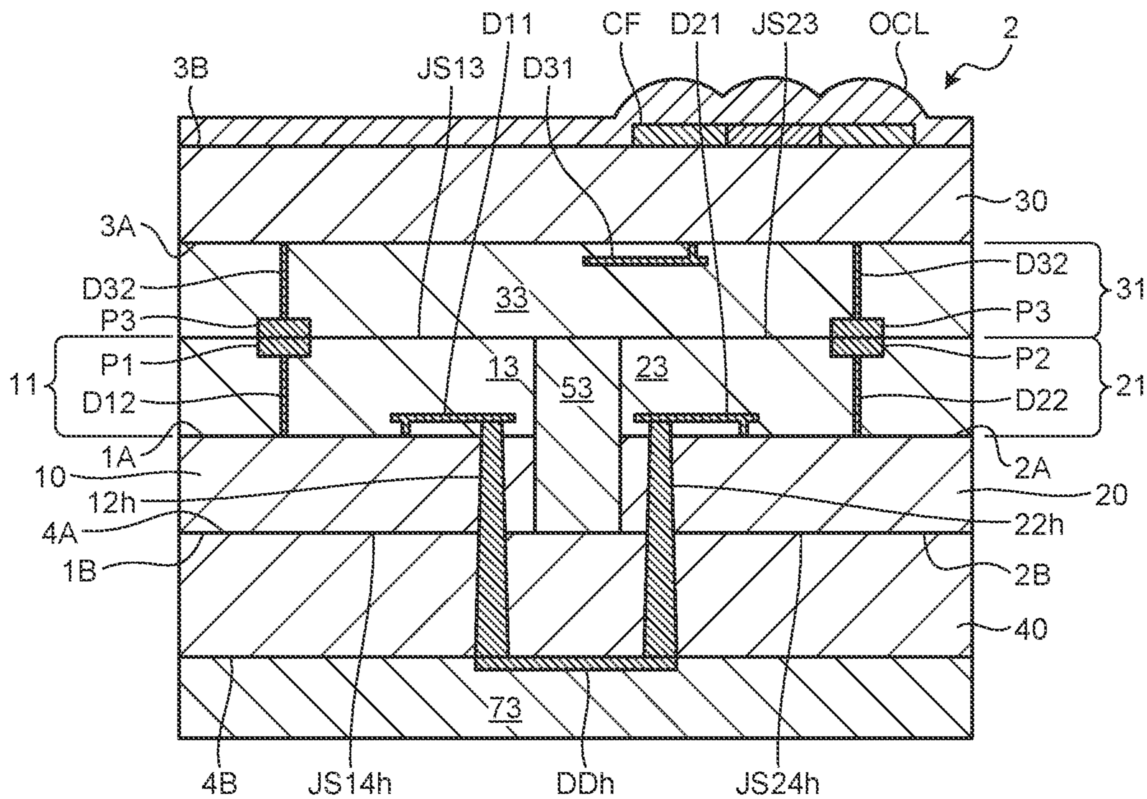


FIG.17



2
3B
JS13
D11
D31
CF
D21
JS23
OCL
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3A
D32
P3
33
D32
31
P3
P1
13
53
23
P2
11
D12
D22
21
1A
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22h
4A
1B
2B
40
73
4B
JS14h
DDh
JS24h

FIG. 18A

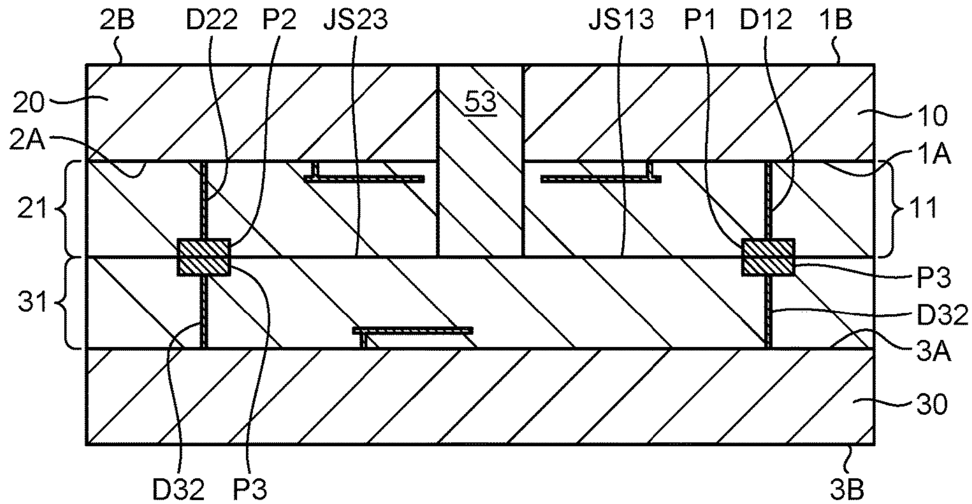


FIG. 18B

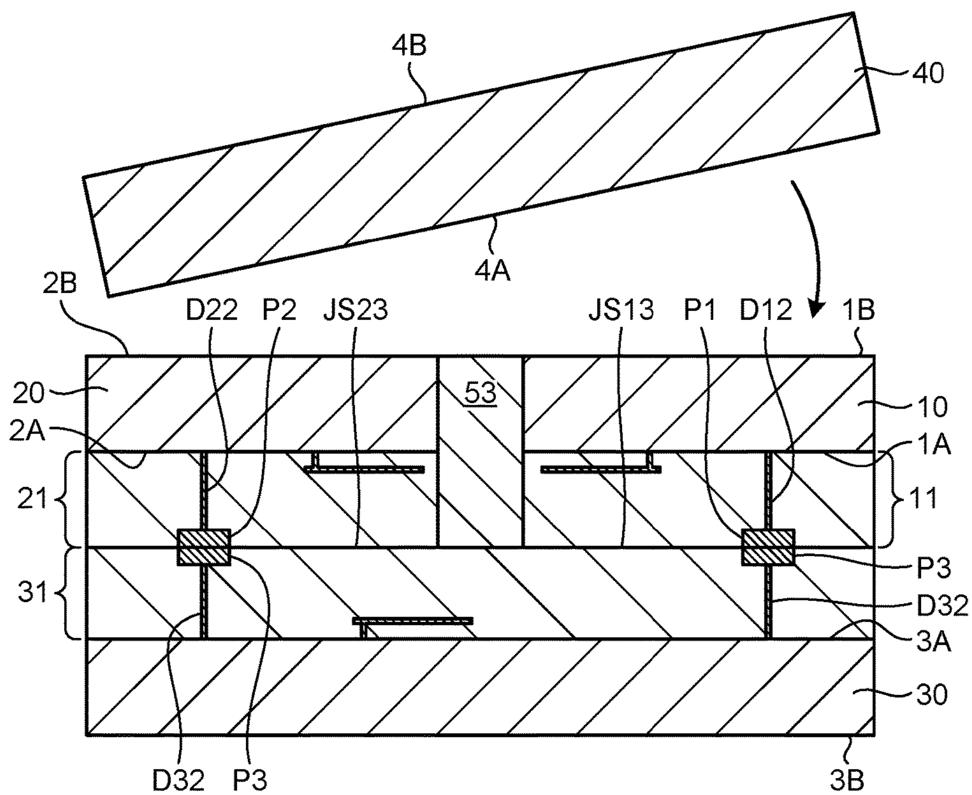


FIG. 19A

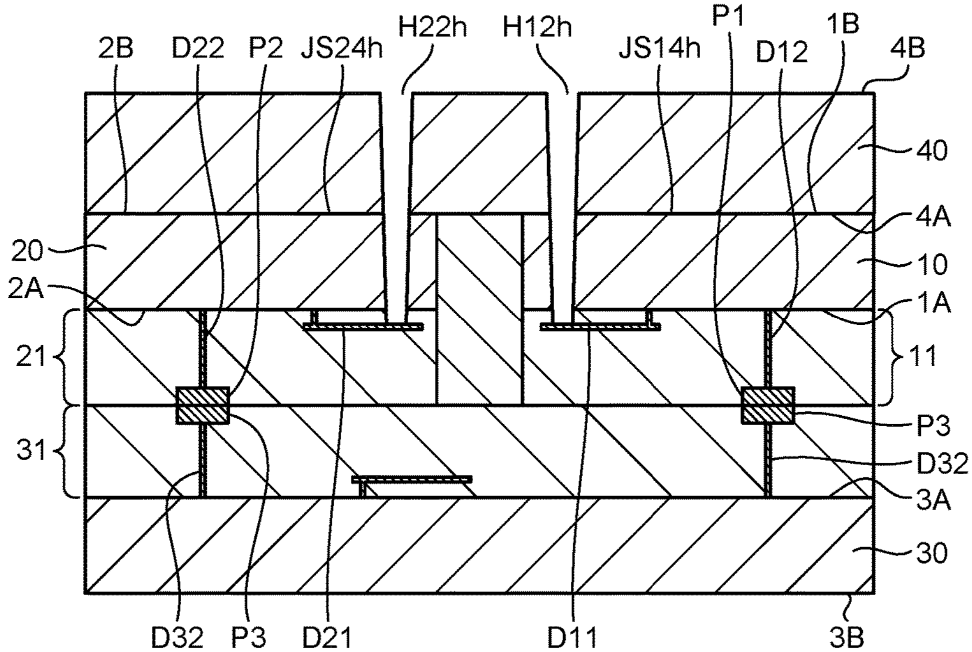


FIG. 19B

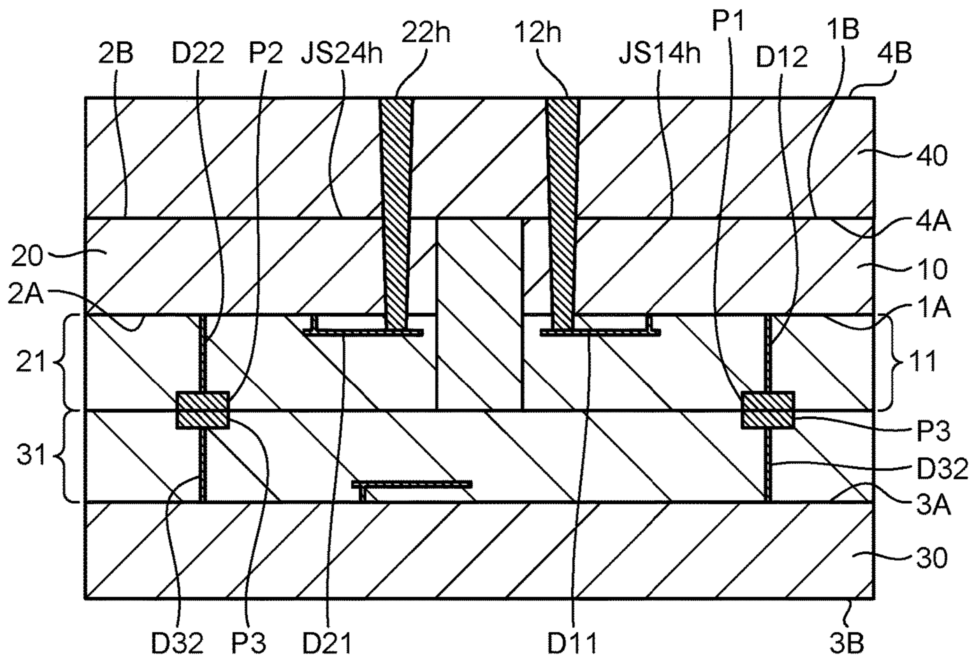


FIG. 20A

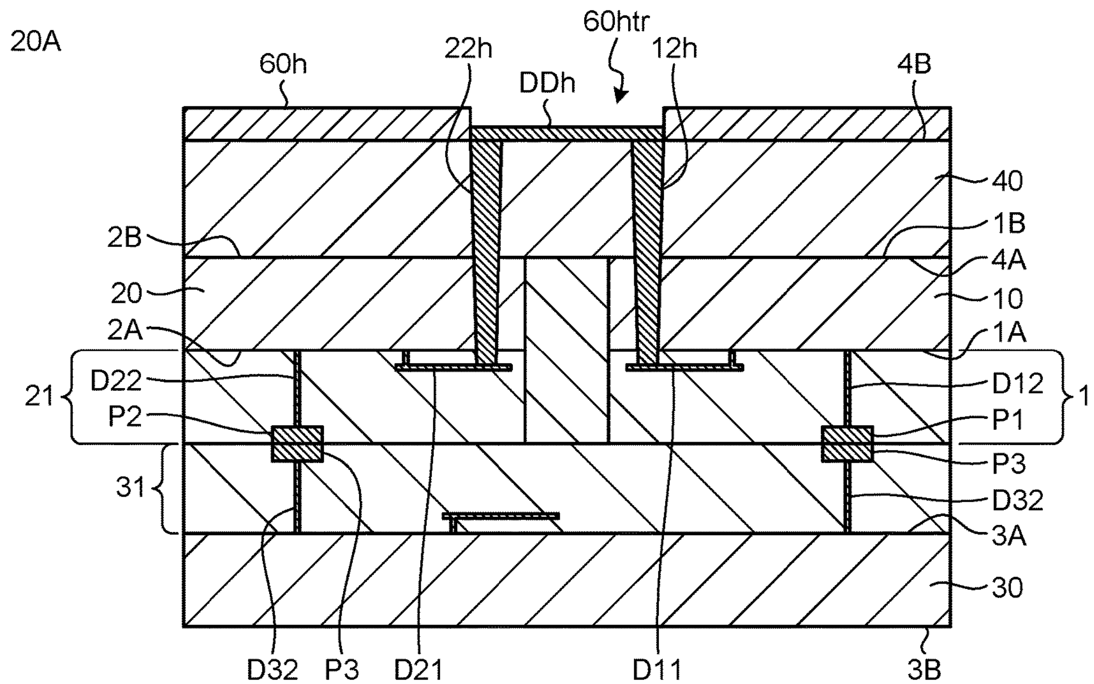


FIG. 20B

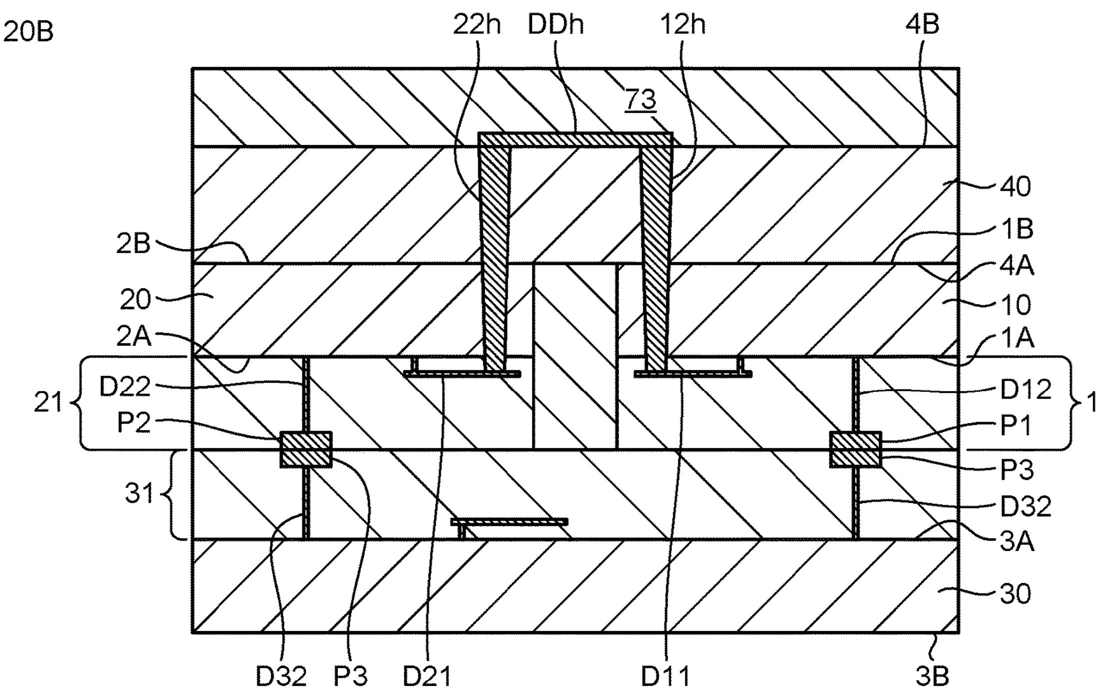


FIG. 21A

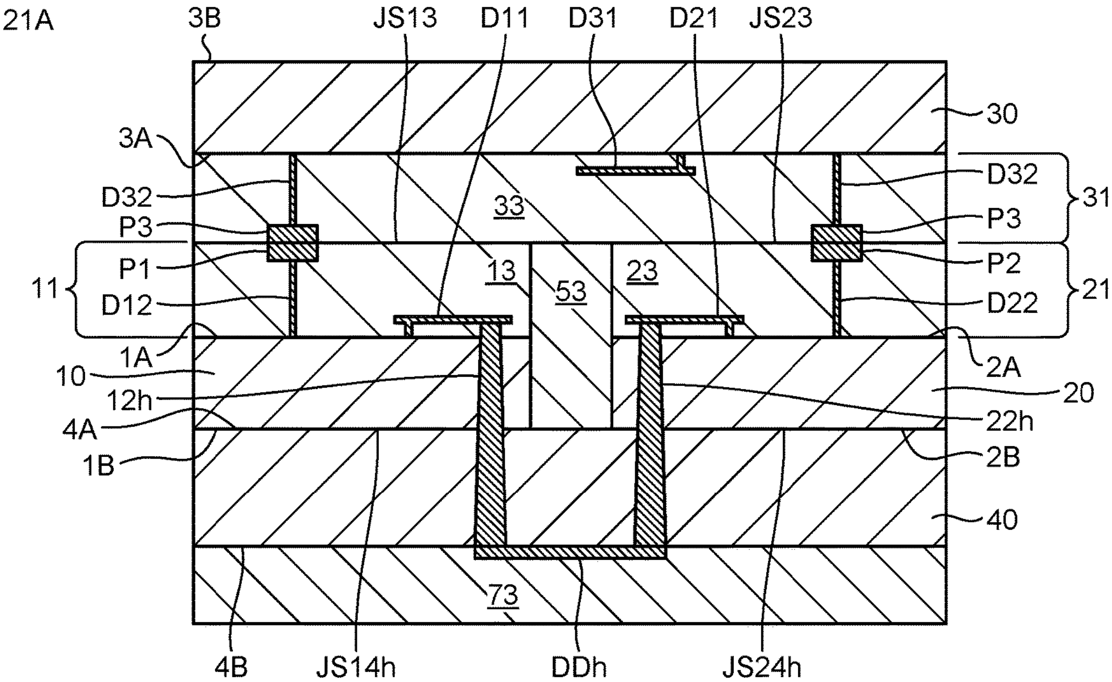


FIG. 21B

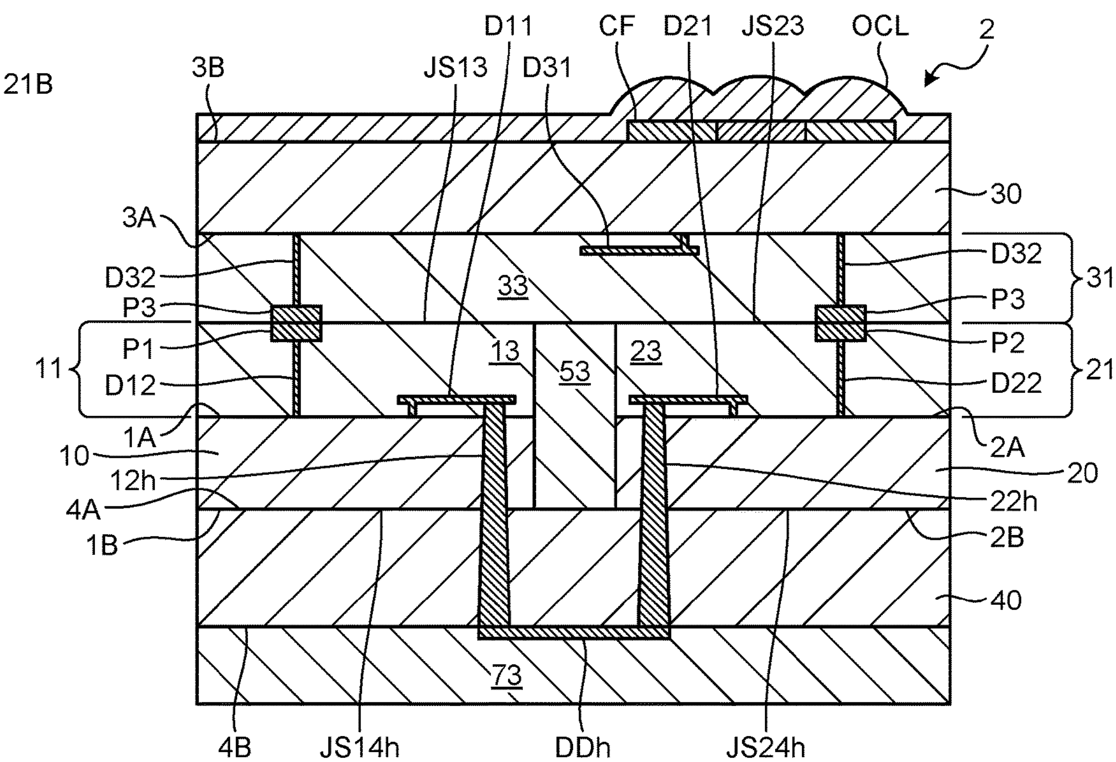


FIG.22

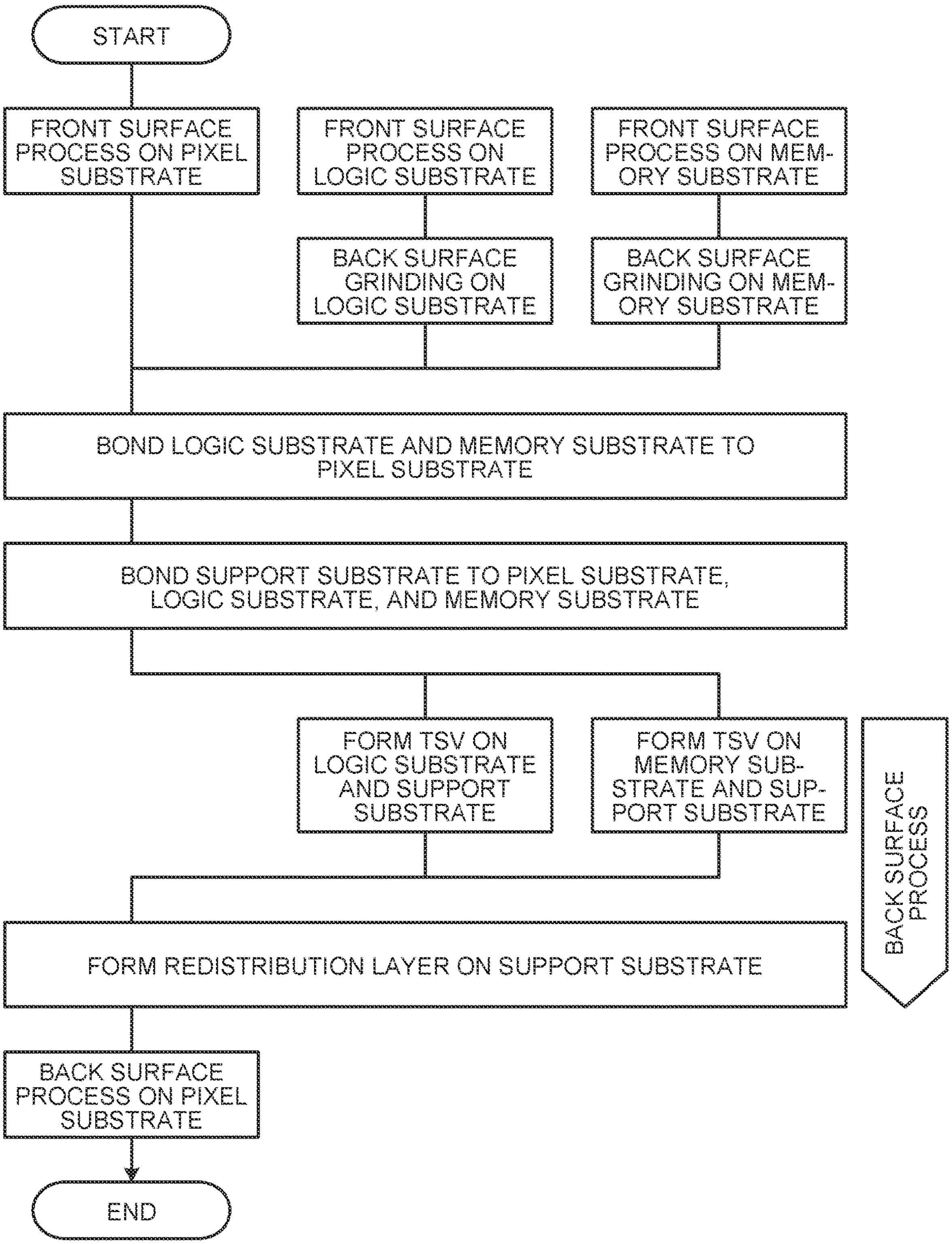
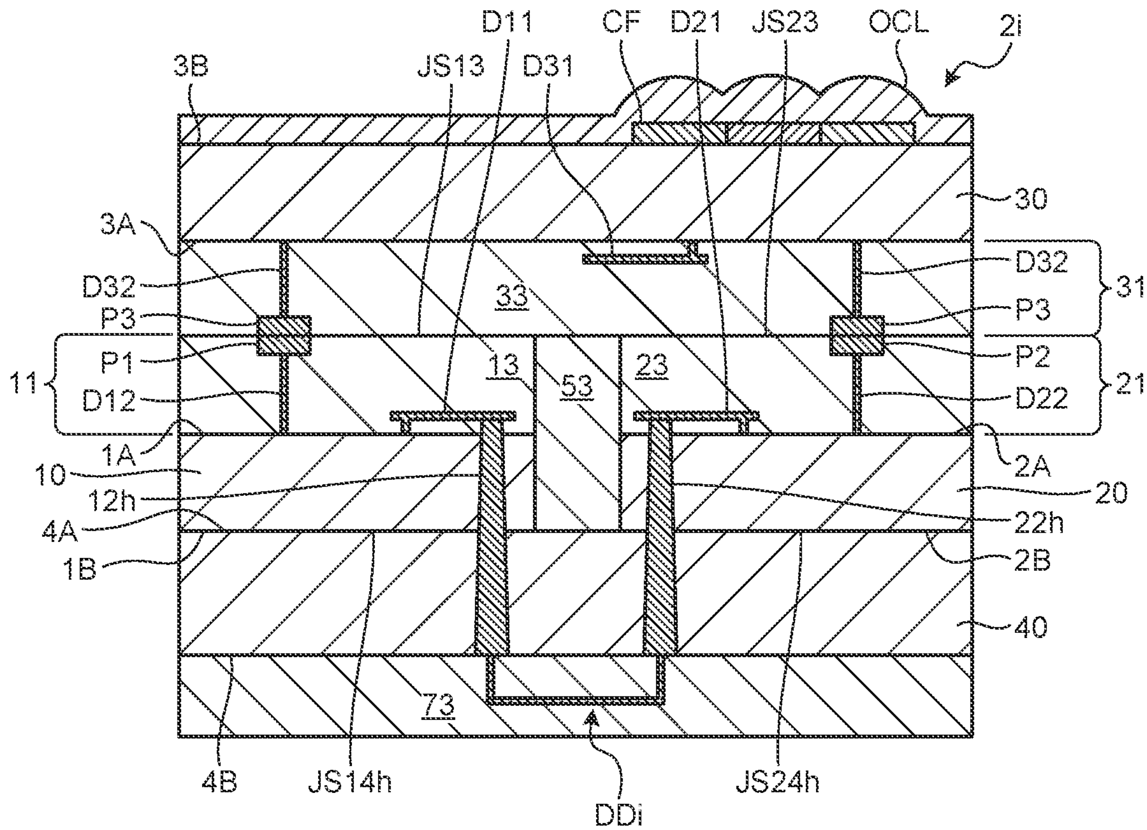

START
FRONT SURFACE PROCESS ON PIXEL SUBSTRATE
FRONT SURFACE PROCESS ON LOGIC SUBSTRATE
FRONT SURFACE PROCESS ON MEMORY SUBSTRATE
BACK SURFACE GRINDING ON LOGIC SUBSTRATE
BACK SURFACE GRINDING ON MEMORY SUBSTRATE
BOND LOGIC SUBSTRATE AND MEMORY SUBSTRATE TO PIXEL SUBSTRATE
BOND SUPPORT SUBSTRATE TO PIXEL SUBSTRATE, LOGIC SUBSTRATE, AND MEMORY SUBSTRATE
FORM TSV ON LOGIC SUBSTRATE AND SUPPORT SUBSTRATE
FORM TSV ON MEMORY SUBSTRATE AND SUPPORT SUBSTRATE
BACK SURFACE PROCESS
FORM REDISTRIBUTION LAYER ON SUPPORT SUBSTRATE
BACK SURFACE PROCESS ON PIXEL SUBSTRATE
END

FIG.23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P2
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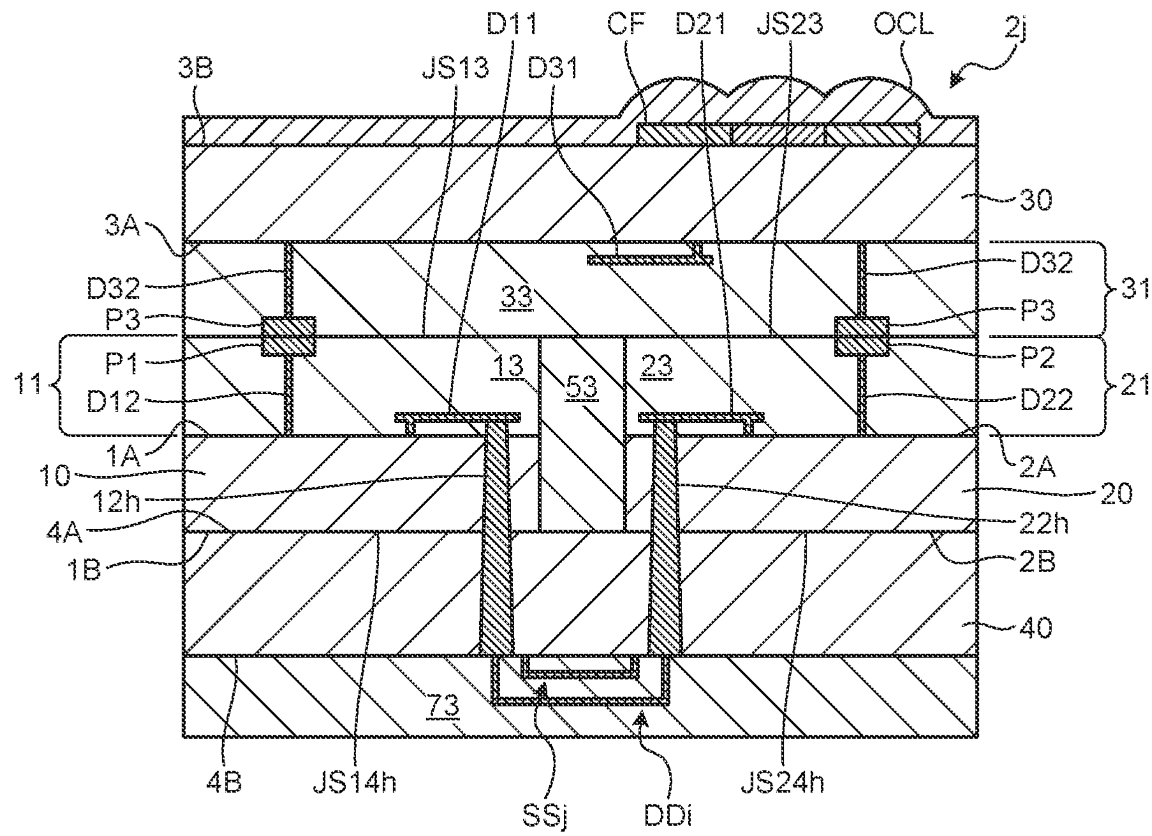
D12
D22
1A
2A
10
20
12h
22h
4A
1B
2B
40
73
4B
JS14h
JS24h
DDi

FIG.24


D11
CF
D21
JS23
OCL
2j
3B
JS13
D31
30
3A
D32
33
D32
31
P3
P3
P1
13
23
P2
11
D12
53
D22
21
1A
2A
10
20
12h
22h
4A
1B
2B
40
73
4B
JS14h
JS24h
SSj
DDi

SOLID-STATE IMAGING ELEMENT

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a U.S. National Phase of International Patent Application No. PCT/JP2020/009837 filed on Mar. 6, 2020, which claims priority benefit of Japanese Patent Application No. JP 2019-045759 filed in the Japan Patent Office on Mar. 13, 2019. Each of the above-referenced applications is hereby incorporated herein by reference in its entirety.

FIELD

The present disclosure relates to a solid-state imaging element.

BACKGROUND

There is a three-dimensional mounting technique of stacking a plurality of semiconductor substrates. For example, there is a known configuration of a solid-state imaging element in which a pixel substrate on which a pixel circuit is formed and a semiconductor substrate on which a semiconductor circuit such as a logic circuit is formed are stacked (refer to Patent Literature 1).

CITATION LIST

Patent Literature

Patent Literature 1: JP 2010-245506 A

SUMMARY

Technical Problem

When stacking a plurality of semiconductor substrates on a pixel substrate in the structure disclosed in Patent Literature 1, there is a concern of occurrence of a problem such as crosstalk due to a layout in which the wiring line connecting the semiconductor substrates is close to the wiring line in a pixel circuit.

Therefore, the present disclosure proposes a solid-state imaging element capable of suppressing crosstalk across wiring lines and reducing noise in a pixel substrate.

Solution to Problem

A solid-state imaging element according to the present disclosure includes: a first semiconductor substrate having a first semiconductor circuit on a first surface of the substrate; a second semiconductor substrate having a second semiconductor circuit on a second surface of the substrate; and a pixel substrate having a pixel circuit on one surface of the substrate, wherein the first semiconductor substrate, the second semiconductor substrate, and the pixel substrate are joined to each other such that the first surface of the first semiconductor substrate and the second surface of the second semiconductor substrate face the one surface of the pixel substrate, and the first semiconductor circuit and the second semiconductor circuit are connected to each other on the first surface side and the second surface side, opposite to the side facing the pixel substrate.

BRIEF DESCRIPTION OF DRAWINGS

FIGS. **1**A and **1**B are schematic diagrams illustrating a part of a solid-state imaging element according to a first embodiment of the present disclosure.

FIGS. **2**A, **2**B, **2**C, and **2**D are flowcharts illustrating an example of a manufacturing process procedure of the solid-state imaging element according to the first embodiment of the present disclosure.

FIGS. **3**A, **3**B, and **3**C are flowcharts illustrating the example of the manufacturing process procedure of the solid-state imaging element according to the first embodiment of the present disclosure.

FIGS. **4**A, **4**B, and **4**C are flowcharts illustrating the example of the manufacturing process procedure of the solid-state imaging element according to the first embodiment of the present disclosure.

FIGS. **5**A and **5**B are flowcharts illustrating the example of the manufacturing process procedure of the solid-state imaging element according to the first embodiment of the present disclosure.

FIGS. **6**A and **6**B are flowcharts illustrating the example of the manufacturing process procedure of the solid-state imaging element according to the first embodiment of the present disclosure.

FIG. **7** is a flowchart illustrating an overall image of the manufacturing process of the solid-state imaging element according to the first embodiment of the present disclosure.

FIG. **8** is a schematic diagram illustrating a part of a solid-state imaging element according to a comparative example of the present disclosure.

FIGS. **9**A, **9**B, **9**C, and **9**D are flowcharts illustrating an example of a manufacturing process procedure of a solid-state imaging element according to a first modification of the first embodiment of the present disclosure.

FIGS. **10**A and **10**B are flowcharts illustrating the example of the manufacturing process procedure of the solid-state imaging element according to the first modification of the first embodiment of the present disclosure.

FIG. **11** is a schematic diagram illustrating a part of a solid-state imaging element according to a second modification of the first embodiment of the present disclosure.

FIG. **12** is a schematic diagram illustrating a part of a solid-state imaging element according to a third modification of the first embodiment of the present disclosure.

FIGS. **13**A, **13**B, and **13**C are flowcharts illustrating an example of a manufacturing process procedure of the solid-state imaging element according to the third modification of the first embodiment of the present disclosure.

FIGS. **14**A, **14**B, and **14**C are flowcharts illustrating the example of the manufacturing process procedure of the solid-state imaging element according to the third modification of the first embodiment of the present disclosure.

FIG. **15** is a schematic diagram illustrating a part of a solid-state imaging element according to a fourth modification of the first embodiment of the present disclosure.

FIGS. **16**A, **16**B, and **16**C are schematic diagrams illustrating a part of a solid-state imaging element according to a fifth modification of the first embodiment of the present disclosure.

FIG. **17** is a schematic diagram illustrating a part of a solid-state imaging element according to a second embodiment of the present disclosure.

FIGS. **18**A and **18**B are flowcharts illustrating an example of a manufacturing process procedure of the solid-state imaging element according to the second embodiment of the present disclosure.

FIGS. **19**A and **19**B are flowcharts illustrating the example of the manufacturing process procedure of the solid-state imaging element according to the second embodiment of the present disclosure.

FIGS. **20**A and **20**B are flowcharts illustrating the example of the manufacturing process procedure of the solid-state imaging element according to the second embodiment of the present disclosure.

FIGS. **21**A and **21**B are flowcharts illustrating the example of the manufacturing process procedure of the solid-state imaging element according to the second embodiment of the present disclosure.

FIG. **22** is a flowchart illustrating an overall image of the manufacturing process of the solid-state imaging element according to the second embodiment of the present disclosure.

FIG. **23** is a schematic diagram illustrating a part of a solid-state imaging element according to a first modification of the second embodiment of the present disclosure.

FIG. **24** is a schematic diagram illustrating a part of a solid-state imaging element according to a second modification of the second embodiment of the present disclosure.

DESCRIPTION OF EMBODIMENTS

Embodiments of the present disclosure will be described below in detail with reference to the drawings. In each of the following embodiments, the same parts are denoted by the same reference symbols, and a repetitive description thereof will be omitted.

First Embodiment

A solid-state imaging element of a first embodiment will be described with reference to FIGS. **1**A, **1**B, **2**A, **2**B, **2**C, **2**D, **3**A, **3**B, **3**C, **4**A, **4**B, **4**C, **5**A, **5**B, **6**A, **6**B. **7**. **8**, **9**A, **9**B, **9**C, **9**D, **10**A, **10**B, **11**, **12**, **13**A, **13**B, **13**C, **14**A, **14**B, **14**C, **15**, **16**A, **16**B, and **16**C.

Configuration Example of Solid-State Imaging Element

FIGS. **1**A and **1**B are schematic diagrams illustrating a part of a solid-state imaging element **1** according to the first embodiment of the present disclosure. FIG. **1**A is a cross-sectional view illustrating a part of the solid-state imaging element **1** according to the first embodiment; FIG. **1**B is a plan view illustrating the part of the solid-state imaging element **1** according to the first embodiment as viewed from a support substrate **40** side. Note that FIG. **1**B omits illustration of the support substrate **40**.

As illustrated in FIGS. **1**A and **1**B, the solid-state imaging element **1** includes a logic substrate **10** as a first semiconductor substrate, a memory substrate **20** as a second semiconductor substrate, and a pixel substrate **30**. A surface **1**A as a first surface of the logic substrate **10** and a surface **2**A as a second surface of the memory substrate **20** are arranged to face a surface **3**A as one surface of the pixel substrate **30**. The logic substrate **10**, the memory substrate **20**, and the pixel substrate **30** are joined at joining surfaces JS**13** and JS**23** on their facing surface sides. The logic substrate **10** and the memory substrate **20** are further joined to the support substrate **40**, on the side opposite to the side facing the pixel substrate **30**. Examples of the logic substrate **10**, the memory substrate **20**, the pixel substrate **30**, and the support substrate **40** include silicon substrates, or the like.

The pixel substrate **30** includes a pixel circuit **31** including members such as wiring lines D**31** and D**32**, and pixel transistors (not illustrated), on the surface **3**A facing the logic substrate **10** and the memory substrate **20**. The pixel circuit **31** is stacked in an insulating layer **33** on the pixel substrate **30**. Examples of the wiring lines D**31** and D**32** include Cu wiring lines, or the like. The pixel substrate **30** includes a photoelectric conversion element (not illustrated) in the substrate. The pixel substrate **30** includes a color filter CF and an on-chip lens OCL on a surface **3**B opposite to the surface **3**A. The on-chip lens OCL collects emitted light, and then, the collected light is guided to the photoelectric conversion element through the color filter CF. Using photoelectric conversion, the photoelectric conversion element converts the received light into an electric signal corresponding to the amount of received light. The pixel circuit **31** reads out an electric signal from the photoelectric conversion element and outputs the electric signal to the logic substrate **10** side.

The logic substrate **10** includes a logic circuit **11** as a first semiconductor circuit including wiring lines D**11** and D**12**, a logic element (not illustrated), and the like, on the surface **1**A facing a pixel substrate **30**. The logic circuit **11** is stacked in the insulating layer **13** on the logic substrate **10**. Examples of the wiring lines D**11** and D**12** include Cu wiring lines, or the like. The logic circuit **11** processes the electric signal output from the pixel substrate **30**. The logic circuit **11** is electrically connected to the pixel circuit **31** through an electrode pad P**3** connected to the wiring line D**32** included in the pixel circuit **31** and through an electrode pad P**1** connected to the wiring line D**12** included in the logic circuit **11**. Examples of the material of the electrode pads P**1** and P**3** include Cu.

The memory substrate **20** includes a memory circuit **21** as a second semiconductor circuit including wiring lines D**21** and D**22**, a storage element (not illustrated), and the like, on the surface **2**A facing the pixel substrate **30**. The memory circuit **21** is stacked in an insulating layer **23** on the memory substrate **20**. Examples of the wiring lines D**21** and D**22** include Cu wiring lines, or the like. The memory circuit **21** holds various data necessary for the solid-state imaging element **1** to function. The memory circuit **21** is electrically connected to the pixel circuit **31** through the electrode pad P**3** connected to the wiring line D**32** included in the pixel circuit **31** and through an electrode pad P**2** connected to the wiring line D**22** included in the memory circuit **21**. Examples of the material of the electrode pad P**2** include Cu.

The logic circuit **11** and the memory circuit **21** are connected to each other on the side of surfaces **1**B and **2**B, opposite to the side facing the pixel substrate **30**.

More specifically, the logic substrate **10** and the memory substrate **20** are connected to each other through a via **12** as a first via penetrating the logic substrate **10**, a via **22** as a second via penetrating the memory substrate **20**, and a wiring line DD in a wiring layer connecting the vias **12** and **22** to each other. Examples of the material of the vias **12** and **22** and the wiring line DD include Cu. The vias **12** and **22** are Through Silicon Vias (TSVs) penetrating through the logic substrate **10** and the memory substrate **20**, respectively. The vias **12** and **22** have, for example, reverse tapered shapes in which the diameter increases from the surfaces **1**A and **2**A side to the surfaces **1**B and **2**B side. As described below, a wiring layer in which the wiring line DD is disposed is a redistribution layer (RDL) formed by a plating technique, for example. The wiring line DD is arranged on the surface **1**B of the logic substrate **10**, the surface **2**B of the memory substrate **20**, and an insulating layer **53** filling the space between the logic substrate **10** and the memory substrate **20**.

As illustrated in FIG. **1**B, the logic substrate **10** and the memory substrate **20** may be connected to each other by a plurality of wiring lines DD. The plurality of wiring lines DD may be arranged in parallel to each other, for example.

The support substrate **40** has: a surface **4**A facing the surface **1**B of the logic substrate **10** and the surface **2**B of the memory substrate **20**; and a surface **4**B on a side opposite to the surface **4**A. The support substrate **40** is joined to the logic substrate **10** and the memory substrate **20** through an insulating layer **43** at joining surfaces JS**14** and JS**24**.

Example of Process of Manufacturing Solid-State Imaging Element

Next, an example of a process of manufacturing the solid-state imaging element **1** according to the first embodiment will be described with reference to FIGS. **2**A, **2**B, **20**, **2**D, **3**A, **3**B, **3**C, **4**A, **4**B, **4**C, **5**A, **5**B, **6**A, **6**B, and **7**. FIGS. **2**A, **2**B, **2**C, **2**D, **3**A, **3**B, **3**C, **4**A, **4**B, **4**C, **5**A, **5**B, **6**A, and **6**B are flowcharts illustrating an example of a manufacturing process procedure of the solid-state imaging element **1** according to the first embodiment of the present disclosure.

As illustrated in FIG. **2**A, the memory substrate **20**, in which the memory circuit **21** is stacked in the insulating layer **23**, is formed. After the formation of the wiring lines D**21** and D**22**, the electrode pad P**2**, and the like, the memory substrate **20** is ground to be thinned.

As illustrated in FIG. **2**B, the logic substrate **10**, in which the logic circuit **11** is stacked in the insulating layer **13**, is formed. After the formation of the wiring lines D**11** and D**12**, the electrode pad P**1**, and the like, the logic substrate **10** is ground to be thinned.

As illustrated in FIG. **2**C, the pixel substrate **30**, in which the pixel circuit **31** is stacked in the insulating layer **33**, is formed. The pixel substrate **30** is provided with the wiring lines D**31** and D**32**, the electrode pad P**3**, and the like. The pixel substrate **30** may also be ground to be thinned.

The order of formation of the logic substrate **10**, the memory substrate **20**, and the pixel substrate **30** is not limited.

As illustrated in FIG. **2**D, the logic substrate **10** and the memory substrate **20** are bonded to the pixel substrate **30** such that the surface **1**A of the logic substrate **10** and the surface **2**A of the memory substrate **20** face the surface **3**A of the pixel substrate **30**.

As illustrated in FIG. **3**A, using the procedure described above, the logic substrate **10** is joined to the pixel substrate **30** at the joining surface JS**13** through the electrode pads P**1** and P**3**. In addition, the memory substrate **20** is joined to the pixel substrate **30** at the joining surface JS**23** through the electrode pads P**2** and P**3**. The electrode pads P**1** and P**3** are joined to each other and the electrode pads P**2** and P**3** are joined to each other using Cu—Cu joining, for example.

Using a chemical vapor deposition (CVD) process, for example, the insulating layer **53** filling the space between the logic substrate **10** and the memory substrate **20** is formed, and then, the insulating layer **53** is planarized by a chemical mechanical polishing (CMP) process, for example.

As illustrated in FIG. **3**B, a through hole H**12** is formed to penetrate the logic substrate **10** from the surface **1**B side to reach the wiring line D**11**. In addition, a through hole H**22** is formed to penetrate the memory substrate **20** from the surface **2**B side to reach the wiring line D**21**. These through holes **12** and **22** tend to have a tapered shape in which the diameter decreases from the surfaces **1**B and **2**B side to the surfaces **1**A and **2**A side.

As illustrated in FIG. **3**C, the through hole H**12** is filled with a conductive material such as Cu to form the via **12** that penetrates the logic substrate **10** to be connected to the wiring line D**11**, for example. In addition, the through hole H**22** is filled with a conductive material such as Cu to form the via **22** that penetrates the memory substrate **20** to be connected to the wiring line D**21**, for example. For example, by having a tapered shape in which the diameter decreases from the surfaces **1**B and **2**B side to the surfaces **1**A and **2**A side, the vias **12** and **22** can be determined to have been formed from the surfaces **1**B and **2**B side.

As illustrated in FIG. **4**A, a resin **60** is formed on the surface **1**B of the logic substrate **10** and the surface **2**B of the memory substrate **20**. The resin **60** has a trench pattern **60**tr in a region including the via **12** of the logic substrate **10** and the via **22** of the memory substrate **20**.

As illustrated in FIG. **4**B, the trench pattern **60**tr in the resin **60** is filled with a conductive material such as Cu by a plating method, for example, so as to form the wiring line DD.

As illustrated in FIG. **4**C, the resin **60** is peeled off. This forms the wiring line DD in the redistribution layer. For formation of the redistribution layer, an insulating layer having a trench pattern, or the like, can be used instead of the resin **60** having the trench pattern ***60**tr*.

As illustrated in FIG. **5**A, the insulating layer **43** is formed on the surface **1**B of the logic substrate **10** and the surface **2**B of the memory substrate **20** so as to cover the wiring line DD.

As illustrated in FIG. **5**B, the logic substrate **10** and the memory substrate **20** are bonded to the support substrate **40** such that the surface **1**B of the logic substrate **10** and the surface **2**B of the memory substrate **20** face the surface **4**A of the support substrate **40**.

As illustrated in FIG. **6**A, using the procedure described above, the logic substrate **10** is joined to the support substrate **40** at the joining surface JS**14** through the insulating layer **43**. In addition, the memory substrate **20** is joined to the support substrate **40** at a joining surface JS**24** through the insulating layer **43**.

As illustrated in FIG. **6**B, the color filter CF and the on-chip lens OCL are formed on the surface **3**B of the pixel substrate **30**.

FIG. **7** illustrates an overall flow of the process of manufacturing the solid-state imaging element **1** according to the first embodiment. FIG. **7** is a flowchart illustrating an overall image of a manufacturing process of the solid-state imaging element **1** according to the first embodiment of the present disclosure.

As illustrated in FIG. **7**, the pixel circuit **31**, the logic circuit **11**, and the memory circuit **21** are formed by the front surface process on the pixel substrate **30**, the logic substrate **10**, and the memory substrate **20**, respectively. Thereafter, the back surfaces of the logic substrate **10** and the memory substrate **20**, namely, the surfaces **1**B and **2**B, are ground.

Next, the logic substrate **10** and the memory substrate **20** are bonded to the pixel substrate **30**.

Next, using a back surface process of the logic substrate **10** and the memory substrate **20**, the vias **12** and **22** as TSVs are formed in the logic substrate **10** and the memory substrate **20**, respectively, and further, the wiring line DD in the redistribution layer connecting these vias **12** and **22** is formed.

Next, the logic substrate **10** and the memory substrate **20**, which have been joined to the pixel substrate **30**, are bonded to the support substrate **40**.

Next, the color filter CF and the on-chip lens OCL are formed on the pixel substrate **30** by the back surface process of the pixel substrate **30**.

The above-described procedure completes the process of manufacturing the solid-state imaging element **1** according to the first embodiment.

Comparative Example

Next, problems of a solid-state imaging element of a comparative example will be described with reference to FIG. **8**. As illustrated in FIG. **8**, the solid-state imaging element of the comparative example has a configuration in which a logic substrate **10'** having a logic circuit **11'** and a memory substrate **20'** having a memory circuit **21'** are joined to a pixel substrate **30'** having a pixel circuit **31'**. These substrates **10'**, **20'**, and **30'** are further supported by a support substrate **40'**. The logic circuit **11'** and the memory circuit **21'** are electrically connected to each other through electrode pads P**1'** and P**3'**, a wiring line DD', and electrode pads P**3'** and P**2'**, on the joining surface side with the pixel substrate **30'**. The wiring line DD' is formed on the pixel substrate **30'** side.

Unfortunately, however, such a connection method has a problem of proximity in which a distance X' between the wiring line DD' and a wiring line D**31'** of the pixel substrate **30'** is too short, leading to a concern of occurrence of crosstalk. Such crosstalk would cause occurrence of noise in the pixel circuit **31'**, leading to degradation of the characteristics of the solid-state imaging element. Another problem is that the wiring line DD' is formed in the region of the logic circuit **11'**, causing a restriction on the layout in the wiring design. In a case where a shield is applied to the wiring line DD' in order to suppress crosstalk, the restriction regarding the layout would be more severe.

In contrast, according to the solid-state imaging element **1** of the first embodiment, the logic circuit **11** and the memory circuit **21** are connected to each other on the side of the surfaces **1**B and **2**B, opposite to the side facing the pixel substrate **30**. With this configuration, the wiring line DD connecting the logic circuit **11** and the memory circuit **21** to each other and the wiring line D**31** and the like of the pixel substrate **30** are separated from each other by a distance which is the thickness of the logic substrate **10** and the memory substrate **20**, or more. This makes it possible to suppress the crosstalk between the wiring line DD and the wiring line D**31**, leading to achievement of noise reduction in the pixel circuit **31**.

According to the solid-state imaging element **1** of the first embodiment, the wiring line DD is arranged on the surface **1**B side of the logic substrate **10** and the surface **2**B side of the memory substrate **20**. This eliminates the necessity to connect the logic circuit **11** and the memory circuit **21** to each other using the region of the logic circuit **11**, increasing the degree of freedom of layout in the wiring design.

According to the solid-state imaging element **1** of the first embodiment, the wiring layer including the wiring line DD connecting the logic circuit **11** and the memory circuit **21** to each other is a redistribution layer formed by a plating technique, for example. This makes it possible to form the wiring line DD by a simple and inexpensive method.

First Modification

Next, a solid-state imaging element according to a first modification of the first embodiment will be described with reference to FIGS. **9**A, **9**B, **90**, **9**D, **10**A, and **10**B. The solid-state imaging element of the first modification is different from that of the first embodiment in a part of the manufacturing process procedure.

As illustrated in FIG. **9**A, the memory substrate **20**, in which the memory circuit **21** is stacked in the insulating layer **23**, is formed. The memory substrate **20** is not ground at this stage. The memory substrate **20** is provided with a via **22***a* reaching halfway through a thick substrate. The via **22***a* is formed from the surface **2**A side of the memory substrate **20** (front surface process), and the wiring line D**21** is thereafter formed so as to be connected to the upper surface of the via **22***a*.

As illustrated in FIG. **9**B, the logic substrate **10**, in which the logic circuit **11** is stacked in the insulating layer **13**, is formed. The logic substrate **10** is not ground at this stage. The logic substrate **10** is provided with a via **12***a* reaching halfway through the thick substrate. The via **12***a* is formed from the surface **1**A side of the logic substrate **10** (front surface process), and the wiring line D**11** is thereafter formed so as to be connected to the upper surface of the via **12***a*.

As illustrated in FIG. **9**C, the pixel substrate **30**, in which the pixel circuit **31** is stacked in the insulating layer **33**, is formed. Formation of the logic substrate **10**, the memory substrate **20**, and the pixel substrate **30** may be performed in any order.

As illustrated in FIG. **9**D, the logic substrate **10** and the memory substrate **20** are bonded to the pixel substrate **30** such that the surface **1**A of the logic substrate **10** and the surface **2**A of the memory substrate **20** face the surface **3**A of the pixel substrate **30**.

The insulating layer **53** filling a space between the logic substrate **10** and the memory substrate **20** is formed by the CVD process, for example, and the insulating layer **53** is planarized by the CMP process, for example.

The logic substrate **10**, the memory substrate **20**, and the insulating layer **50** therebetween are ground, so as to thin the logic substrate **10** and the memory substrate **20** until the end portions of the vias **12***a* and **22***a* on the surfaces **1**B and **2**B sides are exposed.

Thereafter, the solid-state imaging element of the first modification is manufactured in a procedure similar to that in the above-described first embodiment.

That is, as illustrated in FIG. **10**A, the wiring line DD connected to the end portions of the vias **12***a* and **22***a* on the surfaces **1**B and **2**B sides is formed by using a redistribution technique, for example. Furthermore, as illustrated in FIG. **10**B, the logic substrate **10** and the memory substrate **20**, to which the pixel substrate **30** has been joined, are to be joined to the support substrate **40**, so as to form the color filter CF and the on-chip lens OCL on the pixel substrate **30**.

The above-described procedure completes the process of manufacturing the solid-state imaging element according to the first modification. In the solid-state imaging element of the first modification, the via **12***a*, which is the first via formed from the surface **1**A side, has a tapered shape in which the diameter decreases from the surface **1**A side to the surface **1**B side, for example. Furthermore, the via **22***a*, which is the second via formed from the surface **2**A side, has a tapered shape in which the diameter decreases from the surface **2**A side to the surface **2**B side, for example.

Second Modification

Next, a solid-state imaging element **1***b* according to a second modification of the first embodiment will be described with reference to FIG. **11**. The solid-state imaging element **1***b* of the second modification is different from the case of the first embodiment in that the wiring layer in which a wiring line DDb is arranged is not a redistribution layer.

As illustrated in FIG. **11**, the solid-state imaging element **1***b* includes the wiring line DDb stacked in the insulating layer **43**. More specifically, the wiring line DDb has two via portions VI and one bridge portion CR. One end of one via portion VI is connected to an end portion of the via **12** of the logic substrate **10** on the surface **1**B side, while the other end is connected to one end of the bridge portion CR. One end of the other via portion VI is connected to an end portion on the surface **2**B side of the via **22** of the memory substrate **20**, and the other end is connected to the other end of the bridge portion CR. The wiring line DDb having such a structure is formed by a damascene process using a photolithography technique and a dry etching technique, for example.

According to the solid-state imaging element **1***b* of the second modification, the wiring line DDb is formed by a photolithography technique and a dry etching technique. This makes it possible to form a finer wiring line DDb with high accuracy, leading to achievement of high integration of the wiring line DDb.

Third Modification

Next, a solid-state imaging element **1c** according to a third modification of the first embodiment will be described with reference to FIGS. **12**, **13**A, **13**B, **13**C **14**A, **14**B, and **14**C. In addition to the wiring line DDb, the solid-state imaging element **1c** of the third modification further includes a shield SSc to which a method of forming the wiring line DDb is applied.

As illustrated in FIG. **12**, the shield SSc disposed in a shield layer as a conductive layer is arranged between the joining surfaces JS**13** and JS**23**, which join the pixel substrate **30** with the logic substrate **10** and the memory substrate **20**, and the wiring line DDb. Similarly to the wiring line DDb, the shield SSc is also stacked in the insulating layer **43**. More specifically, the shield SSc includes two via portions VIc and one bridge portion CRc. One end of one via portion VIc is connected to the surface **1**B of the logic substrate **10**, while the other end is connected to one end of the bridge portion CRc. One end of the other via portion VIc is connected to the surface **2**B of the memory substrate **20**, while the other end is connected to the other end of the bridge portion CRc. Similarly to the wiring line DDb, the shield SSc having such a structure is formed by the damascene process using a photolithography technique and a dry etching technique, for example.

The wiring line DDb and the shield SSc can be formed using, for example, the dual damascene process illustrated in FIGS. **13**A, **13**B, **13**C, **14**A, **14**B, and **14**C. The flow illustrated from FIGS. **13**A, **13**B, **13**C, **14**A, **14**B, and **14**C are replacements for the flow of FIGS. **4**A, **4**B, and **4**C of the first embodiment described above. FIGS. **13**A, **13**B, **13**C, **14**A, **14**B, and **14**C are enlarged illustrations of the vicinity of the end portion of the via **12** of the logic substrate **10** on the surface **1**B side and the end portion of the via **22** of the memory substrate **20** on the surface **2**B side.

As illustrated in FIG. **13**A, the insulating layer **43** is formed on the surface **1**B of the logic substrate **10**, on the insulating layer **53**, and on the surface **2**B of the memory substrate **20**. At this time, the insulating layer **43** is formed to be thinner than the final thickness.

As illustrated in FIG. **13**B, for example, a photolithography technique and a dry etching technique are used to form holes HLc, each of which penetrating the insulating layer **43** to reach the surface **1**B of the logic substrate **10** and the surface **2**B of the memory substrate **20**, individually, and to form a trench TRc having each end portion connected to each of the holes HLc.

As illustrated in FIG. **13**C, the inside of the hole HLc and the inside of the trench TRc are filled with a conductive material such as Cu by the CVD process, for example, and an excessive conductive material is removed by the CMP process or the like to form the shield SSc having the via portions Vlc and the bridge portion CRc.

As illustrated in FIG. **14**A, the insulating layer **43** is further formed so as to cover the shield SSc.

As illustrated in FIG. **14**B, a photolithography technique and a dry etching technique are used, for example, to form holes HLb, each of which penetrating the insulating layer **43** to reach the via **12** of the logic substrate **10** and the via **22** of the memory substrate **20**, individually, and to form a trench TRb having each end portion connected to each of the holes HLb.

As illustrated in FIG. **14**C, the inside of the hole HLb and the inside of the trench TRb are filled with a conductive material such as Cu by the CVD process, for example, and an excessive conductive material is removed by the CMP process or the like to form the wiring line DDb having the via portions VI and the bridge portion CR.

The above-described procedure completes the formation of the wiring line DDb and the shield SSc. In the above example, the dual damascene process of collectively forming the via portions and the bridge portion is used, but a single damascene process of separately forming the via portions and the bridge portion may be used.

According to the solid-state imaging element **1***c* of the third modification, the shield SSc is disposed on the pixel substrate **30** side of the wiring line DDb. With this configuration, the wiring line DDb is shielded against the wiring line D**31** and the like of the pixel substrate **30**, making it possible to further suppress the crosstalk between the wiring line DDb and the wiring line D**31**, leading to achievement of the reduction of the noise in the pixel circuit **31**.

Fourth Modification

Next, a solid-state imaging element **1***d* of a fourth modification of the first embodiment will be described with reference to FIG. **15**. The solid-state imaging element **1***d* of the fourth modification is different from the case of the first embodiment described above in that two wiring lines DDda and DDdb intersect each other.

As illustrated in the plan view of FIG. **15**(*a*), the wiring lines DDda and DDdb connecting the logic substrate **10** and the memory substrate **20** to each other intersect each other.

As illustrated in the perspective view of FIG. **15**(*b*), such a configuration can be obtained by arranging one of the wiring lines, namely, the wiring line DDdb, to be positioned higher than the other wiring line, namely the wiring line DDda, so as to allow the two wiring lines DDda and DDdb to three-dimensionally intersect each other.

These wiring lines DDda and DDdb can be easily formed by the photolithography technique and the dry etching technique as described in the above second and third modifications, for example. The wiring layer including the one of the wiring lines, namely, the wiring line DDda, may be a redistribution layer using the plating technique as described in the first embodiment. Alternatively, vias may be further formed on the vias **12** and **22** so as to form both wiring layers including the wiring lines DDda and DDdb are to be implemented as redistribution layers using a plating technique.

Fifth Modification

Although the above-described first embodiment and the like have a configuration in which one logic substrate **10** and one memory substrate **20** are joined to the pixel substrate **30**, the present invention is not limited to this configuration. Hereinafter, some examples of joining various different substrates to the pixel substrate **30** will be described with reference to FIGS. **16**A, **16**B, and **16**C as a solid-state imaging element of a fifth modification of the first embodiment.

As illustrated in FIG. **16**A, a solid-state imaging element **1***e* has a configuration in which two logic substrates **10** and **10**e are bonded to a pixel substrate **30**. The logic circuits included in the two logic substrates **10** and **10***e* are electrically connected to each other by a via **12** of the logic substrate **10**, a via **10***e* of the logic substrate **12***e*, and a wiring line DDe joining these vias **12** and **12***e* to each other.

As illustrated in FIG. **16**B, a solid-state imaging element **1***f* has a configuration in which two memory substrates **20** and **20***f* are bonded to a pixel substrate **30**. The memory circuits included in the two memory substrates **20** and **20***f* are electrically connected to each other by a via **22** of the memory substrate **20**, a via **20***f* of the memory substrate **22***f*, and a wiring line DDf joining these vias **22** and **22***f* to each other.

As illustrated in FIG. **16**C, a solid-state imaging element **1***g* has a configuration in which one logic substrate **10** and two memory substrates **20***ga* and **20***gb* are bonded to a pixel substrate **30**. The logic circuit of the logic substrate **10** and the memory circuit of the memory substrate **20***ga* are electrically connected to each other by a via **12** of the logic substrate **10**, a via **22***ga* of the memory substrate **20***ga*, and a wiring line DDga joining these vias **12** and **22***ga* to each other. The logic circuit of the logic substrate **10** and the memory circuit of the memory substrate **20***gb* are electrically connected to each other by a via **12** of the logic substrate **10**, a via **22***gb* of the memory substrate **20***gb*, and a wiring line DDgb joining these vias **12** and **22***gb* to each other. The memory circuits included in the memory substrate **20***ga* and the memory substrate **20***gb* are electrically connected to each other by the via **22***ga* of the memory substrate **20***ga*, the via **22***gb* of the memory substrate **20***gb*, and a wiring line DDgab joining these vias **22***ga* and **22***gb* to each other.

In addition to the above, the solid-state imaging element of the fifth modification can have a configuration in which various substrates of arbitrary numbers are bonded with the pixel substrate **30**. The solid-state imaging element of the fifth modification may include a shield layer in addition to the wiring layer.

Second Embodiment

Next, a solid-state imaging element **2** of a second embodiment will be described with reference to FIGS. **17**, **18**A, **18**B, **19**A, **19**B, **20**A, **20**B, **21**A, **21**B, **22**, **23**, and **24**. The solid-state imaging element **2** of the second embodiment is different from the case of the first embodiment described above in that a wiring line DDh is provided on the surface **4**B side of the support substrate **40**.

Configuration Example of Solid-State Imaging Element

FIG. **17** is a schematic diagram illustrating a part of the solid-state imaging element **2** according to the second embodiment of the present disclosure. As illustrated in FIG. **17**, the solid-state imaging element **2** includes the support substrate **40** directly joined both to the logic substrate **10** and to the memory substrate **20**. That is, the surface 1B of the logic substrate **20** and the surface **2**B of the memory substrate **20** are bonded to the surface **4**A of the support substrate **40** at joining surfaces JS**14***h* and JS**24***h*, respectively.

The logic circuit **11** and the memory circuit **21** are electrically connected to each other through a via **12***h* as a first via penetrating the support substrate **40** and the logic substrate **10**, a via **22***h* as a second via penetrating the support substrate **40** and the memory substrate **20**, and the wiring line DDh joining these vias **12***h* and **22***h* to each other.

The wiring line DDh is disposed on the surface **4**B of the support substrate **40**, which is the surface on the side opposite to the side on which the logic substrate **10** and the memory substrate **20** are disposed. On the surface **4**B of the support substrate **40**, an insulating layer **73** is disposed to cover the wiring line DDh.

Example of Process of Manufacturing Solid-State Imaging Element

Next, an example of a process of manufacturing the solid-state imaging element **2** according to the second embodiment will be described with reference to FIGS. **18**A, **18**B, **19**A, **19**B, **20**A, **20**B, **21**A, **21**B, and **22**. FIGS. **18**A, **18**B, **19**A, **19**B, **20**A, **20**B, **21**A, and **21**B are flowcharts illustrating an example of a manufacturing process procedure of the solid-state imaging element **2** according to the second embodiment of the present disclosure.

As illustrated in FIG. **18**A, the pixel substrate **30** in which the logic substrate **10** and the memory substrate **20** are bonded to each other is formed. The process up to this point is similar to the process up to FIG. **3**A of the first embodiment described above.

As illustrated in FIG. **18**B, the surface **4**A of the support substrate **40** is bonded to the surface 1B of the logic substrate **10** and the surface 2B of the memory substrate **20**, which have been bonded to the pixel substrate **30**.

As illustrated in FIG. **19**A, a through hole H**12***h* which penetrates the support substrate **40** and the logic substrate **10** from the surface 4B side of the support substrate **40** and reaches, for example, a wiring line DD**11** is formed. In addition, a through hole H**22***h* which penetrates the support substrate **40** and the memory substrate **20** from the surface 4B side of the support substrate **40** and reaches, for example, a wiring line DD**21** is formed.

As illustrated in FIG. **19**B, the through hole H**12***h* is filled with a conductive material such as Cu to form the via **12***h* that penetrates the support substrate **40** and the logic substrate **10** to be connected, for example, to the wiring line D**11**. In addition, the through hole H**22***h* is filled with a conductive material such as Cu to form the via **22***h* which penetrates the support substrate **40** and the memory substrate **20** to be connected, for example, to the wiring line D**21**.

The vias **12***h* and **22***h* formed from the surface **4**B side of the support substrate **40** each have a tapered shape in which the diameter decreases from the surface **4**B side of the support substrate **40** to the surface **1**A side of the logic substrate **10** and the surface **2**A side of the memory substrate **20**, for example.

As illustrated in FIG. **20**A, a resin **60***h* having a trench pattern **60***htr* is formed in a region including the vias **12***h* and **22***h* on the surface **4**B of the support substrate **40**. Subsequently, the trench pattern **60***htr* is filled with a conductive material such as Cu by a plating method, for example, to form the wiring line DDh.

As illustrated in FIG. **20**B, after the resin **60***h* is peeled off, the insulating layer **73** is formed on the surface **4**B of the support substrate **40** so as to cover the wiring line DDh.

As illustrated in FIG. **21**A, the stacked substrates, namely, the support substrate **40**, logic substrate **10**, memory substrate **20**, and pixel substrate **30**, are inverted, to be arranged such that the support substrate **40** faces downward and the pixel substrate **30** faces upward.

As illustrated in FIG. **21**B, the color filter CF and the on-chip lens OCL are formed on the surface **3**B of the pixel substrate **30**.

FIG. **22** illustrates an overall flow of manufacturing process of the solid-state imaging element **2** of the second embodiment. FIG. **22** is a flowchart illustrating an overall image of a manufacturing process of the solid-state imaging element **2** according to the second embodiment of the present disclosure.

As illustrated in FIG. **22**, the process is similar to that of the first embodiment described above up to the point where the logic substrate **10** and the memory substrate **20** are bonded to the pixel substrate **30**.

Next, the support substrate **40** is joined to the logic substrate **10** and the memory substrate **20**, which have been bonded to the pixel substrate **30**.

Next, using a back surface process of the support substrate **40**, the vias **12***h* and **22***h* as TSVs are formed in the support substrate **40**, the logic substrate **10** and the memory substrate **20**, respectively, and further, the wiring line DDh in the redistribution layer connecting these vias **12***h* and **22***h* is formed on the support substrate **40**.

Next, the color filter CF and the on-chip lens OCL are formed on the pixel substrate **30** by the back surface process of the pixel substrate **30**.

The above-described procedure completes the process of manufacturing the solid-state imaging element **2** according to the second embodiment.

According to the solid-state imaging element **1** of the first embodiment, the logic circuit **11** and the memory circuit **21** are connected to each other on the surface **4**B side of the support substrate **40**. With this configuration, the wiring line DDh connecting the logic circuit **11** and the memory circuit **21** to each other and the wiring line D**31** and the like of the pixel substrate **30** are separated by a distance which is a sum of the thickness of the logic substrate **10**, the memory substrate **20**, and the thickness of the support substrate **40**, or more. This makes it possible to further suppress the crosstalk between the wiring line

DD and the wiring line D**31**, leading to enhanced noise reduction in the pixel circuit **31**.

First Modification

Next, a solid-state imaging element **2***i* according to a first modification of the second embodiment will be described with reference to FIG. **23**. The solid-state imaging element **2***i* of the first modification includes a wiring line DDi formed by a photolithography technique and a dry etching technique.

FIG. **23** is a schematic diagram illustrating a part of the solid-state imaging element **2***i* according to the first modification of the second embodiment of the present disclosure. As illustrated in FIG. **23**, the solid-state imaging element **2***i* includes the wiring line DDi having two via portions and one bridge portion, similarly to the second modification of the first embodiment described above. The wiring line DDi is stacked in the insulating layer **73**. The wiring line DDi is formed by a photolithography technique and a dry etching technique, for example.

According to the solid-state imaging element **2***i* of the first modification, the finer wiring line DDi can be accurately formed by the photolithography technique and the dry etching technique, for example, leading to achievement of high integration of the wiring line DDi.

Second Modification

Next, a solid-state imaging element **2***j* according to a second modification of the second embodiment will be described with reference to FIG. **24**. In addition to the wiring line DDi, the solid-state imaging element **2***j* of the second modification further includes a shield SSj which is disposed in a shield layer as a conductive layer and to which a method of forming the wiring line DDi is applied.

FIG. **24** is a schematic diagram illustrating a part of a solid-state imaging element **2***j* according to the second modification of the second embodiment of the present disclosure. As illustrated in FIG. **24**, the solid-state imaging element **2***j* includes the shield SSj disposed in a shield layer having two via portions and one bridge portion, similarly to the third modification of the first embodiment described above. The shield SSj is also stacked in the insulating layer **73**. Similarly to the wiring line DDi, the shield SSj is formed by the photolithography technique and the dry etching technique.

According to the solid-state imaging element **2***j* of the second modification, the crosstalk between the wiring line DDb and the wiring line D**31** can be further suppressed by the shield SSc arranged on the pixel substrate **30** side of the wiring line DDi, leading to enhanced noise reduction in the pixel circuit **31**.

Third Modification

Even with a configuration having the wiring layer on the support substrate **40** as in the solid-state imaging element of the second embodiment and the like, it is possible to form a configuration in which various substrates of an arbitrary number, such as a plurality of logic substrates and a plurality of memory substrates, are bonded to the pixel substrate **30**, as described as the configuration of the fifth modification of the first embodiment.

The solid-state imaging element of the third modification may include a shield layer in addition to the wiring layer on the support substrate **40**.

The effects described in the present specification are merely examples, and thus, there may be other effects, not limited to the exemplified effects.

Other Embodiments

Note that the present technology can also have the following configurations.

(1)

A solid-state imaging element comprising:

a first semiconductor substrate having a first semiconductor circuit on a first surface of the substrate;

a second semiconductor substrate having a second semiconductor circuit on a second surface of the substrate; and

a pixel substrate having a pixel circuit on one surface of the substrate,

wherein the first semiconductor substrate, the second semiconductor substrate, and the pixel substrate are joined to each other such that

the first surface of the first semiconductor substrate and the second surface of the second semiconductor substrate face the one surface of the pixel substrate, and

the first semiconductor circuit and the second semiconductor circuit are connected to each other on the first surface side and the second surface side, opposite to the side facing the pixel substrate.

(2)

The solid-state imaging element according to (1),

wherein the first semiconductor circuit and the second semiconductor circuit are connected to each other through

a first via penetrating the first semiconductor substrate, a second via penetrating the second semiconductor substrate, and a wiring line connecting the first via and the second via to each other.

(3)

The solid-state imaging element according to (2),

wherein a shield is disposed between a joining surface which joins the first semiconductor substrate and the second semiconductor substrate to the pixel substrate, and the wiring line.

(4)

The solid-state imaging element according to (2) or (3) ,

wherein the wiring line is disposed on the first semiconductor substrate and the second semiconductor substrate.

(5)

The solid-state imaging element according to (2) or (3), further comprising

a support substrate joined to a side of the first semiconductor substrate and the second semiconductor substrate, opposite to the side facing the pixel substrate,

wherein the first via and the second via each penetrate the support substrate, and

the wiring line is disposed on the support substrate on a side opposite to the first semiconductor substrate and the second semiconductor substrate.

(6)

The solid-state imaging element according to any one of (2) to (5),

wherein a wiring layer in which the wiring line is disposed is a redistribution layer formed by a plating technique.

(7)

The solid-state imaging element according to any one of (2) to (5),

wherein a wiring layer in which the wiring line is disposed is a wiring layer formed by a photolithography technique and a dry etching technique.

(8)

The solid-state imaging element according to any one of (1) to (7),

wherein the first semiconductor substrate is a logic substrate including a logic circuit as the first semiconductor circuit, and

the second semiconductor substrate is a memory substrate including a memory circuit as the second semiconductor circuit.

(9)

The solid-state imaging element according to any one of (1) to (7),

wherein the first semiconductor substrate is a first logic substrate including a first logic circuit as the first semiconductor circuit, and

the second semiconductor substrate is a second logic substrate including a second logic circuit as the second semiconductor circuit.

(10)

The solid-state imaging element according to any one of (1) to (7),

wherein the first semiconductor substrate is a first memory substrate including a first memory circuit as the first semiconductor circuit, and

the second semiconductor substrate is a second memory substrate including a second memory circuit as the second semiconductor circuit.

(11)

The solid-state imaging element according to any one of (1) to (7), further comprising

a third semiconductor substrate having a third semiconductor circuit on a third surface of the substrate,

wherein the third semiconductor substrate and the pixel substrate are joined to each other such that the third surface of the third semiconductor substrate and the one surface of the pixel substrate face each other,

the first semiconductor circuit and the third semiconductor circuit are connected to each other on the first surface side and the third surface side, opposite to the side facing the pixel substrate, and

the second semiconductor circuit and the third semiconductor circuit are connected to each other on the second surface side and the third surface side, opposite to the side facing the pixel substrate.

(12)

The solid-state imaging element according to (11), further comprising:

a first wiring line that connects the first semiconductor circuit and the third semiconductor circuit to each other; and

a second wiring line that connects the second semiconductor circuit and the third semiconductor circuit to each other,

wherein the first wiring line is disposed on the first semiconductor substrate and the third semiconductor substrate, and

the second wiring line is disposed on the second semiconductor substrate and the third semiconductor substrate.

(13)

The solid-state imaging element according to (11) or (12),

wherein the first semiconductor substrate is a logic substrate including a logic circuit as the first semiconductor circuit,

the second semiconductor substrate is a first memory substrate including a first memory circuit as the second semiconductor circuit, and the third semiconductor substrate is a second memory substrate including a second memory circuit as the third semiconductor circuit.

(14)

The solid-state imaging element according to (5), further comprising:

a third semiconductor substrate having a third semiconductor circuit on a third surface of the substrate;

a first wiring line that connects the first semiconductor circuit and the third semiconductor circuit to each other on the first surface side and the third surface side, opposite to the side facing the pixel substrate; and

a second wiring line that connects the second semiconductor circuit and the third semiconductor circuit to each other on the second surface side and the third surface side, opposite to the side facing the pixel substrate,

wherein the third surface of the third semiconductor substrate and the one surface of the pixel substrate are joined to each other so as to face each other, and

the first wiring line and the second wiring line are disposed on the support substrate on a side opposite to the third semiconductor substrate.

REFERENCE SIGNS LIST

1, **1***b*, **1***c*, **2**, **2***i*, **2***j* SOLID-STATE IMAGING ELEMENT
10 LOGIC SUBSTRATE
11 LOGIC CIRCUIT
12, **12***a*, **12***h* VIA
20 MEMORY SUBSTRATE
21 MEMORY CIRCUIT
22, **22***a*, **22***h* VIA
30 PIXEL SUBSTRATE
31 PIXEL CIRCUIT
DD, DDb, DD, DDh, DDi WIRING LINE
SSc, SSj SHIELD

The invention claimed is:

1. A solid-state imaging element, comprising:

a first semiconductor substrate that includes a first semiconductor circuit, wherein the first semiconductor circuit is on a first surface of the first semiconductor substrate;

a second semiconductor substrate that includes a second semiconductor circuit, wherein the second semiconductor circuit is on a first surface of the second semiconductor substrate;

a pixel substrate that includes a pixel circuit, wherein the pixel circuit is on a surface of the pixel substrate;

a joining surface at which the first semiconductor substrate and the second semiconductor substrate are joined to the pixel substrate, wherein

each of the first surface of the first semiconductor substrate and the first surface of the second semiconductor substrate faces the surface of the pixel substrate,

the first semiconductor circuit is connected to the second semiconductor circuit on a second surface of the first semiconductor substrate and a second surface of the second semiconductor substrate,

the second surface of the first semiconductor substrate is opposite to the first surface of the first semiconductor substrate, and

the second surface of the second semiconductor substrate is opposite to the first surface of the second semiconductor substrate;

a wiring line; and

a shield between the joining surface and the wiring line, wherein

the shield includes a first via and a second via,

an end of the first via is connected to the second surface of the first semiconductor substrate, and

an end of the second via is connected to the second surface of the second semiconductor substrate.

2. The solid-state imaging element according to claim **1**, further comprising:

a third via that penetrates the first semiconductor substrate; and

a fourth via that penetrates the second semiconductor substrate, wherein

the wiring line is configured to connect the third via to the fourth via, and

the first semiconductor circuit is connected to the second semiconductor circuit through the third via, the fourth via, and the wiring line.

3. The solid-state imaging element according to claim **2**, wherein the wiring line is on the first semiconductor substrate and the second semiconductor substrate.

4. The solid-state imaging element according to claim **2**, further comprising a support substrate joined to the second surface of the first semiconductor substrate and the second surface of the second semiconductor substrate, wherein

each of the third via and the fourth via penetrates the support substrate, and

the wiring line is on the support substrate.

5. The solid-state imaging element according to claim **2**, further comprising a wiring layer that includes the wiring line, wherein

the wiring layer corresponds to a redistribution layer, and

fabrication of the wiring layer is based on a plating technique.

6. The solid-state imaging element according to claim **2**, further comprising a wiring layer that includes the wiring line, wherein fabrication of the wiring layer is based on a photolithography technique and a dry etching technique.

7. The solid-state imaging element according to claim **1**, wherein

the first semiconductor substrate is a logic substrate,

the first semiconductor circuit is a logic circuit,

the second semiconductor substrate is a memory substrate, and

the second semiconductor circuit is including a memory circuit.

8. The solid-state imaging element according to claim **1**, wherein

the first semiconductor substrate is a first logic substrate,

the first semiconductor circuit is a first logic circuit,

the second semiconductor substrate is a second logic substrate, and

the second semiconductor circuit is a second logic circuit.

9. The solid-state imaging element according to claim **1**, wherein

the first semiconductor substrate is a first memory substrate,

the first semiconductor circuit is a first memory circuit,

the second semiconductor substrate is a second memory substrate, and

the second semiconductor circuit is a second memory circuit.

10. The solid-state imaging element according to claim **1**, further comprising a first memory substrate that includes a first memory circuit, wherein

the first memory substrate is joined to the pixel substrate,

the first semiconductor circuit is connected to the first memory circuit, and

the second semiconductor circuit is connected to the first memory circuit.

11. The solid-state imaging element according to claim **1**, further comprising:

a first wiring line configured to connect the first semiconductor circuit with the pixel circuit; and

a second wiring line configured to connect the second semiconductor circuit with the pixel circuit, wherein

the first wiring line is on the first semiconductor substrate, and

the second wiring line is on the second semiconductor substrate.

12. The solid-state imaging element according to claim **10**, wherein

the first semiconductor substrate is a logic substrate,

the first semiconductor circuit is a logic circuit,

the second semiconductor substrate is a second memory substrate, and

the second semiconductor circuit is second memory circuit.

13. The solid-state imaging element according to claim **4**, further comprising:

a first wiring line configured to connect the first semiconductor circuit with the pixel circuit; and

a second wiring line configured to connect the second semiconductor circuit with the pixel circuit, wherein

the first wiring line is on the first surface of the first semiconductor substrate, and

the second wiring line is on the first surface of the second semiconductor substrate.

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