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SiC SEMICONDUCTOR DEVICE WITH CURRENT SENSING CAPABILITY

Abstract

A SiC semiconductor device is provided that is capable of improving the detection accuracy of the current value of a principal current detected by a current sensing portion by restraining heat from escaping from the current sensing portion to a wiring member joined to a sensing-side surface electrode. The semiconductor device includes a SiC semiconductor substrate, a source portion including a principal-current-side unit cell, a current sensing portion including a sensing-side unit cell, a source-side surface electrode disposed above the source portion, and a sensing-side surface electrode that is disposed above the current sensing portion and that has a sensing-side pad to which a sensing-side wire is joined, and, in the semiconductor device, the sensing-side unit cell is disposed so as to avoid being positioned directly under the sensing-side pad.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS [0001] This application is a continuation of U.S. application Ser. No. 18/311,780, filed May 3, 2023, which is a continuation of U.S. application Ser. No. 17/456,785, filed Nov. 29, 2021 (now U.S. Pat. No. 11,674,983), which is a continuation of U.S. application Ser. No. 16/891,957, filed Jun. 3, 2020 (now U.S. Pat. No. 11,215,647), which is a continuation of U.S. application Ser. No. 16/061,967, filed Jun. 13, 2018 (now U.S. Pat. No. 10,705,123), which is a continuation of PCT/J P2016/086445, filed Dec. 7, 2016, which claims priority to Japanese application no. 2015-247727, filed Dec. 18, 2015. The entire contents of all prior applications are hereby incorporated by reference.

TECHNICAL FIELD

[0002] The present invention relates to a SiC semiconductor device that has a current sensing portion.

BACKGROUND ART

[0003] A semiconductor device that includes a current sensing portion to detect a current value of a principal current of a device is heretofore known, and semiconductor devices of, for example, Patent Documents 1 and 2 have been proposed.

PRIOR ART DOCUMENTS

Patent Documents

[0004] Patent Document 1: Japanese Patent Application Publication No. 8-46193 [0005] Patent

Document 2: Japanese Patent Application Publication No. 11-74370

SUMMARY OF INVENTION

Technical Problem

[0006] Generally, a current sensing portion is formed smaller in area than a source portion through which a principal current flows. An area ratio between the current sensing portion and the source portion defines a sensing ratio when the principal current is detected. Additionally, the current value of the principal current is calculated by multiplying the value of an electric current that has actually flowed through the current sensing portion by the sensing ratio.

[0007] If conditions other than the area condition are completely identical with each other, the current value of the principal current might be able to be accurately detected only by considering the sensing ratio. However, in practice, differences exist with respect to a condition under which

the current sensing portion and the source portion are placed, and the differences affect detection accuracy.

[0008] For example, a pad of the source portion is comparatively large, and the occupation area of a bonding wire with respect to the pad is small, and, on the other hand, a pad of the current sensing portion is comparatively small, and therefore the occupation area of the bonding wire with respect to the pad becomes large. This causes a difference in the amount of heat escaping through the bonding wire, and therefore there is a possibility that an error produced in on-resistance between the source portion and the current sensing portion will become large. This error in on-resistance affects the detection accuracy of the current value of the principal current.

[0009] An object of the present invention is to provide a SiC semiconductor device that is capable of improving the detection accuracy of the current value of a principal current detected by a current sensing portion by restraining heat from escaping from the current sensing portion to a wiring member joined to a sensing-side surface electrode.

Solution to Problem

[0010] A semiconductor device according to a preferred embodiment of the present invention includes a semiconductor layer made of SiC, a source portion that is formed at the semiconductor layer and that includes a first unit cell on a principal current side, a current sensing portion that is formed at the semiconductor layer and that includes a second unit cell on a current detection side, a source-side surface electrode disposed above the source portion, and a sensing-side surface electrode disposed so that at least one part of the sensing-side surface electrode includes a region positioned above the current sensing portion, and, in the semiconductor device, the second unit cell is disposed at a position below the sensing-side surface electrode and so as to avoid being positioned directly under a joint part of a wiring member.

[0011] According to this arrangement, the second unit cell on the current detection side is disposed so as to avoid being positioned directly under the joint part of the wiring member. This makes it possible to maintain a fixed distance between the second unit cell and the wiring member, and hence makes it possible to restrain heat generated at the second unit cell from escaping while being preferentially transmitted to the wiring member. Therefore, it is possible to lessen an error generated in on-resistance between the first unit cell of the source portion and the second unit cell of the current sensing portion. Additionally, the second unit cell is not placed directly under the joint part of the wiring member, and therefore it is possible to prevent a shock caused when the wiring member is joined to the sensing-side surface electrode from running directly to the second unit cell, and it is also possible to restrain the second unit cell from being broken. As a result thereof, it is possible to improve the detection accuracy of the current value of a principal current detected by the current sensing portion.

[0012] The use of the semiconductor layer made of SiC makes it possible to achieve an arrangement in which the second unit cell is disposed so as to avoid being positioned directly under the joint part of the wiring member as mentioned above. In other words, in a Si semiconductor device, the amount of flowing current per unit area is small, and therefore a cell area for a somewhat large sensing portion is required to set an appropriate sensing ratio (about 1000 to 2000) having high detection accuracy with respect to a source portion having a large area through which high current flows, and therefore it is difficult to form it so as to avoid being positioned directly thereunder. On the other hand, in the SiC semiconductor device, the amount of flowing current per unit area is large, and therefore it is possible to secure an appropriate sensing ratio even if the sensing portion is small in cell area with respect to the source portion, and therefore it is possible to form it so as to avoid being positioned directly thereunder.

[0013] The semiconductor device may include an interlayer insulating film disposed between the current sensing portion and the sensing-side surface electrode and a gate insulating film formed at a lower position than the interlayer insulating film, and, in the semiconductor device, the interlayer insulating film may be formed thicker than the gate insulating film.

[0014] According to this arrangement, it is possible to lessen a shock running to the second unit cell when the wiring member is joined to the sensing-side surface electrode. As a result, it is possible to secure the reliability of the detection accuracy of the current value of a principal current.

[0015] In the semiconductor device, the current sensing portion may be formed in a region surrounded by the source portion.

[0016] According to this arrangement, it is possible to bring the amount of heat generation of the current sensing portion close to that of the source portion, and therefore it is possible to lessen an error in on-resistance generated because of a difference in the amount of heat generation.

[0017] The semiconductor device may include a passivation film that selectively covers a portion positioned directly over the second unit cell of the sensing-side surface electrode and that has an opening by which a part of the sensing-side surface electrode is exposed as a sensing-side pad.

[0018] According to this arrangement, the portion positioned directly over the second unit cell and the sensing-side pad are clearly distinguished from each other when viewed from outside the semiconductor device, and therefore it is possible to prevent the wiring member from being erroneously joined to the portion positioned directly over the second unit cell. Therefore, it is possible to reliably maintain a fixed distance between the second unit cell and the wiring member.

[0019] In the semiconductor device, the first unit cell and the second unit cell may have mutually same cell structures, respectively.

[0020] According to this arrangement, it is possible to estimate a sensing ratio when the current value of the principal current is calculated from a cell ratio between the first unit cell and the second unit cell, and therefore it is possible to easily perform current detection.

[0021] In the semiconductor device, the current sensing portion may be formed at only one place in an in-plane direction of the semiconductor layer.

[0022] According to this arrangement, it is possible to achieve the space-saving of a surface part of the semiconductor layer.

[0023] In the semiconductor device, the interlayer insulating film may have a thickness of 1 μm or more.

[0024] According to this arrangement, it is possible to give sufficient shock resistance (for example, wire bonding resistance) to the interlayer insulating film.

[0025] The semiconductor device may include a gate-side surface electrode that is disposed on the semiconductor layer and that has a gate-side joint region to which a wiring member is joined, and, in the semiconductor device, the interlayer insulating film may also be disposed at a place directly under the gate-side joint region.

[0026] According to this arrangement, it is possible to form in the same process step an interlayer insulating film with which the source portion is covered and an interlayer insulating film with which the gate portion is covered, and therefore it is possible to shorten a manufacturing process.

[0027] In the semiconductor device, the interlayer insulating film may include a SiO_2 film, and the SiO_2 film may contain P (phosphorus) or B (boron).

[0028] The SiO_2 film is easily produced, and, if the SiO_2 film contains P (phosphorus) or B (boron), it is also possible to perform a reflow process after the film is produced. It is possible to easily flatten the interlayer insulating film (SiO_2 film) by the reflow process, and therefore it is possible to easily join the wiring member, which possibly affects the heat dissipation capability of the current sensing portion, according to a design plan.

[0029] In the semiconductor device, the sensing-side surface electrode may include an electrode having a layered structure in which Ti, TiN, and AlCu are stacked together in this order from the bottom.

[0030] According to this arrangement, the use of AlCu for the topmost surface of the sensing-side surface electrode makes it possible to give sufficient shock resistance (for example, wire bonding resistance) to the electrode.

[0031] The semiconductor device may include a gate-side surface electrode disposed on the semiconductor layer and a passivation film that has an opening by which a part of the sensing-side surface electrode is exposed as a sensing-side pad and an opening by which a part of the gate-side surface electrode is exposed as a gate-side pad, and in the semiconductor device, the sensing-side pad and the gate-side pad may be each formed so as to have a shape long in a same direction. [0032] According to this arrangement, it is possible to extend and join the wiring members from the same direction to the sensing-side pad and to the gate-side pad, respectively, and therefore it is possible to easily lay the wiring members when a package is assembled.

Description

BRIEF DESCRIPTION OF DRAWINGS

[0033] FIG. 1 is a schematic plan view of a semiconductor device according to a preferred embodiment of the present invention.

[0034] FIG. 2 is an enlarged view of a region surrounded by broken line II of FIG. 1.

[0035] FIG. 3 is an enlarged view of a region surrounded by broken line III of FIG. 2.

[0036] FIG. 4 is a cross-sectional view in a cutting plane along line IV-IV of FIG. 3.

[0037] FIG. 5 is an enlarged view around a gate-side pad of FIG. 1.

[0038] FIG. 6 is a cross-sectional view in a cutting plane along line VI-VI of FIG. 5.

[0039] FIG. 7 is a cross-sectional view in a cutting plane along line VII-VII of FIG. 5.

[0040] FIG. 8 is a cross-sectional view in a cutting plane along line VIII-VIII of FIG. 5.

[0041] FIG. 9 is a circuit diagram to describe current detection in the semiconductor device.

[0042] FIG. 10 is a flowchart showing a manufacturing process of the semiconductor device.

[0043] FIG. 11 is a view showing a modification of a gate structure of the semiconductor device.

[0044] FIG. 12 is a view showing a modification of a sensing-side pad of the semiconductor device.

DESCRIPTION OF EMBODIMENTS

[0045] Preferred embodiments of the present invention will be hereinafter described in detail with reference to the accompanying drawings.

[0046] FIG. 1 is a schematic plan view of a semiconductor device 1 according to a preferred embodiment of the present invention.

[0047] The semiconductor device 1 includes a semiconductor substrate 2 that is an example of a semiconductor layer of the present invention and that is formed in a quadrangular shape in a plan view. The semiconductor substrate 2 has four sides 3A, 3B, 3C, and 3D in a plan view.

[0048] A plurality of surface electrode films 4 are formed on the semiconductor substrate 2 so as to be separated from each other. The surface electrode films 4 include a source-side surface electrode 5, a sensing-side surface electrode 6, and a gate-side surface electrode 7. The source-side surface electrode 5 is formed in most regions on the semiconductor substrate 2 (the hatched region of FIG. 1 and regions of source-side pads 14A, 14B, and 14B described later), and removal regions 8 and 9 for which a part of the source-side surface electrode 5 has been removed are formation regions of the sensing-side surface electrode 6 and the gate-side surface electrode 7, respectively. Both of the removal regions 8 and 9 are defined by being surrounded by the source-side surface electrode 5.

[0049] A passivation film 10 that wholly covers the plurality of surface electrode films 4 with the single film 10 is formed on the semiconductor substrate 2. The passivation film 10 has a plurality of pad openings 11, 12, and 13. The source-side surface electrode 5, the sensing-side surface electrode 6, and the gate-side surface electrode 7 are exposed from the pad openings 11, 12, and 13 as source-side pads 14A and 14B, as a sensing-side pad 15, and as a gate-side pad 16, respectively.

[0050] The plurality of source-side pads 14A and 14B are disposed so as to be separated from each other. In FIG. 1, the three source-side pads 14A, 14B, and 14B are provided on the semiconductor

substrate 2. The source-side pad 14A that is one of the three source-side pads is disposed closer to a side 3A of the semiconductor substrate 2 in a central part in a direction along the side 3A, and the remaining source-side pads 14B and 14B are disposed on both sides of the source-side pad 14A, respectively. The source-side pads 14B and 14B disposed on both sides respectively have extension portions 17 and 17 that extend toward a side 3C opposite to the side 3A with respect to the source-side pad 14A disposed between the source-side pads 14B and 14B. The extension portions 17 face each other with an interval therebetween, and define a region 18 in which the gate-side pad 16 is disposed at a part adjacent to the source-side pad 14A disposed between the source-side pads 14B and 14B. Although the plurality of source-side pads 14A and 14B are separated from each other in appearance, these source-side pads 14A and 14B are connected to each other through the hatched region of FIG. 1 below the passivation film 10 so that the source-side pads 14A and 14B are united together and serve as the source-side surface electrode 5.

[0051] The sensing-side pad 15 is disposed only at one corner portion of the quadrangular semiconductor substrate 2. This makes it possible to achieve space-saving on the semiconductor substrate 2. The sensing-side pad 15 is formed in a shape that is long along the two sides 3B and 3D of the semiconductor substrate 2, and is surrounded by one of the two source-side pads 14B and 14B. In the sensing-side pad 15, a part of its periphery may be surrounded by the source-side pad 14B as shown in FIG. 1, or, alternatively, all of its periphery may be surrounded by the source-side pad 14B (not shown).

[0052] The gate-side pad 16 is disposed in the region 18 between the source-side pads 14B and 14B that face each other. The gate-side pad 16 is formed in a shape that is long along the sides 3B and 3D of the semiconductor substrate 2 in the same way as the sensing-side pad 15.

[0053] The gate-side surface electrode 7 additionally includes a gate finger 19 that extends from the gate-side pad 16. The gate finger 19 is covered with the passivation film 10. The gate finger 19 includes a central portion 20 that extends in a direction from the side 3C of the semiconductor substrate 2 toward the side 3A opposite to the side 3C so as to pass through the center of the source-side surface electrode 5 and a peripheral portion 21 that extends along a peripheral edge of the semiconductor substrate 2 (i.e., along the sides 3B, 3C, and 3D in FIG. 1) and that surrounds the source-side surface electrode 5.

[0054] A source-side wire 22, a sensing-side wire 23, and a gate-side wire 24 are connected to the source-side pads 14A and 14B, to the sensing-side pad 15, and to the gate-side pad 16, respectively. For example, aluminum wires are used as the wires 22 to 24. The aluminum wire is normally joined by not ball bonding but slender wedge bonding. Therefore, if the sensing-side pad 15 and the gate-side pad 16 are each formed in a shape long in the same direction as in FIG. 1, it is possible to extend and join the wires 23 and 24 from the same direction to the sensing-side pad 15 and to the gate-side pad 16, respectively. As a result, it is possible to easily lay the wires when a package is assembled.

[0055] With respect to the diameter of each of the wires 22 to 24, the diameter of the source-side wire 22 may be, for example, 300 μm to 500 μm , and the diameter of the sensing-side wire 23 and that of the gate-side wire 24 may be, for example, 100 μm to 200 μm .

[0056] A bonding wire is not necessarily required to be used as a wiring member by which the source-side pads 14A and 14B, the sensing-side pad 15, and the gate-side pad 16 are connected to the outside, and another wiring member, such as a bonding plate or a bonding ribbon, may be used as the wiring member.

[0057] FIG. 2 is an enlarged view of a region surrounded by broken line II of FIG. 1.

[0058] In appearance, the sensing-side surface electrode 6 is exposed as the sensing-side pad 15 formed in a substantially rectangular shape in a plan view in a state in which a part (in FIG. 2, one corner portion) of the sensing-side surface electrode 6 is covered with the passivation film 10 although the sensing-side surface electrode 6 is formed in a rectangular shape in a plan view as shown in FIG. 2. Preferably, the length L1 of a long side and the length L2 of a short side of the

sensing-side pad **15** are 1.2 mm or less and 0.6 mm or less, respectively. This makes it possible to confine the size of the sensing-side pad **15** to 0.72 mm.^{sup.2} or less, and hence makes it possible to restrain an increase in on-resistance of a sensing-side unit cell **40** (described later). Additionally, the sensing-side pad **15** is made slender by increasing the length **L1** of the long side about twice as long as the length **L2** of the short side, thus making it possible to easily join a bonding wire (sensing-side wire **23**) by means of wedge bonding.

[0059] The region **25** covered with the passivation film **10** is formed in a rectangular shape in a plan view, and one short side and one long side of the region **25** form an extension portion of the short side and an extension portion of the long side of the sensing-side pad **15**, respectively. The region **25** covered therewith is not necessarily required to be formed in a rectangular shape in a plan view, and may be formed in another shape (for example, square, circular, or triangular). Of course, likewise, its position is not necessarily required to be placed at a corner portion of the sensing-side surface electrode **6**, and it may be placed, for example, between both ends of a side of the sensing-side surface electrode **6**.

[0060] A current sensing portion **26** that serves as an aggregation of many sensing-side unit cells **40** (described later) is formed at a place directly under the covered region **25**. On the other hand, the current sensing portion **26** is not formed at a place directly under the sensing-side pad **15**. In other words, in the present preferred embodiment, the entirety of the current sensing portion **26** is formed so as to avoid being positioned directly under the sensing-side pad **15**.

[0061] On the other hand, a source portion **27** that serves as an aggregation of many principal-current-side unit cells **34** (described later) is formed around the sensing-side surface electrode **6**. The source portion **27** is formed at a place directly under the source-side surface electrode **5**, and is formed so as to surround the sensing-side surface electrode **6** in a plan view. The source portion **27** may be formed at a place directly under the entirety of the source-side surface electrode **5** shown in FIG. **1** (not shown).

[0062] FIG. **3** is an enlarged view of a region surrounded by broken line III of FIG. **2**. FIG. **4** is a cross-sectional view in a cutting plane along line IV-IV of FIG. **3**. FIG. **5** is an enlarged view around the gate-side pad **16** of FIG. **1**. FIG. **6** is a cross-sectional view in a cutting plane along line VI-VI of FIG. **5**. FIG. **7** is a cross-sectional view in a cutting plane along line VII-VII of FIG. **5**. FIG. **8** is a cross-sectional view in a cutting plane along line VIII-VIII of FIG. **5**. In FIG. **4**, repeated parts in the lateral direction of FIG. **3** are partially excluded.

[0063] As shown in FIG. **4** and in FIG. **6** to FIG. **8**, the semiconductor substrate **2** may be a SiC epitaxial substrate that includes a base substrate **28** and an epitaxial layer **29** on the base substrate **28**. In the present preferred embodiment, the semiconductor substrate **2** includes a base substrate **28** made of n⁺ type SiC (whose concentration is, for example, 1×10^{17} cm.^{sup.-3} to 1×10^{19} cm.^{sup.-3}) and an epitaxial layer **29** made of n type SiC (whose concentration is, for example, 1×10^{14} cm.^{sup.-3} to 1×10^{17} cm.^{sup.-3}).

[0064] A p.^{sup.-} type well **30** (whose concentration is, for example, 1×10^{14} cm.^{sup.-3} to 1×10^{19} cm.^{sup.-3}) is formed at a surface part of the n' type epitaxial layer **29**. The p.^{sup.-} type well **30** includes a principal-current-side p.^{sup.-} type body well **31**, a sensing-side p.^{sup.-} type body well **32**, and a gate-side p.^{sup.-} type well **33**. As shown in FIG. **4**, the principal-current-side p.^{sup.-} type body well **31** and the sensing-side p.^{sup.-} type body well **32** are formed so as to be separated from each other. As shown in FIG. **6**, the gate-side p.^{sup.-} type well **33** is connected to the principal-current-side p.^{sup.-} type body well **31**.

[0065] The principal-current-side p.^{sup.-} type body well **31** includes a cell forming portion **35** that forms a principal-current-side unit cell **34** that is an example of a first unit cell of the present invention and a field forming portion **36** that has a comparatively wide region. In other words, each cell forming portion **35** defines the principal-current-side unit cell **34** that is a minimum unit through which a principal current flows.

[0066] As shown in FIG. **3** and FIG. **5**, many cell forming portions **35** are arranged in a matrix

manner, thus making up the source portion **27**.

[0067] The field forming portion **36** is formed so as to surround the many cell forming portions **35**, and connects adjoining cell forming portions **35** together while straddling between the adjoining cell forming portions **35** at an outer peripheral part of the source portion **27**.

[0068] The principal-current-side p.sup.- type body well **31** additionally includes a connection portion **37** formed at an intersection of lattice regions partitioned by the matrix-shaped cell forming portions **35**. This connection portion **37** connects the adjoining cell forming portions **35** together inside the source portion **27**.

[0069] As thus described, the cell forming portions **35** are electrically connected together at the outer peripheral part and the inner part of the source portion **27** by means of the field forming portion **36** and the connection portion **37**. Consequently, the many cell forming portions **35** are held at mutually equal electric potentials.

[0070] An n+ type source region **38** is formed in an inner region of the cell forming portion **35**, and a p+ type body contact region **39** (whose concentration is, for example, $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$) is formed in an inner region of the n+ type source region **38** (whose concentration is, for example, $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$).

[0071] The sensing-side p-type body well **32** includes a cell forming portion **41** that forms the sensing-side unit cell **40** that is an example of a second unit cell of the present invention and a field forming portion **42** that has a comparatively wide region. In other words, each cell forming portion **41** defines the sensing-side unit cell **40** that is a minimum unit through which a principal current flows.

[0072] As shown in FIG. 3, many cell forming portions **41** are arranged in a matrix manner at places each of which is positioned so as to avoid being positioned directly under the sensing-side pad **15**, thus making up the current sensing portion **26**. The cell forming portion **41** has the same cell structure (size and pitch) as the principal-current-side cell forming portion **35**.

[0073] The field forming portion **42** is formed so as to surround the many cell forming portions **41**, and connects adjoining cell forming portions **41** together while straddling between the adjoining cell forming portions **41** at an outer peripheral part of the current sensing portion **26**.

[0074] The sensing-side p-type body well **32** additionally includes a connection portion **43** formed at an intersection of lattice regions partitioned by the matrix-shaped cell forming portions **41**. This connection portion **43** connects the adjoining cell forming portions **41** together inside the current sensing portion **26**.

[0075] As thus described, the cell forming portions **41** are electrically connected together at the outer peripheral part and the inner part of the current sensing portion **26** by means of the field forming portion **42** and the connection portion **43**. Consequently, the many cell forming portions **41** are held at mutually equal electric potentials.

[0076] An n.sup.+ type source region **44** (whose concentration is, for example, $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$) is formed in an inner region of the cell forming portion **41**, and a p+ type body contact region **45** (whose concentration is, for example, $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$) is formed in an inner region of the n+ type source region **44**.

[0077] The field forming portion **42** is formed so as to extend from an outer peripheral part of the cell forming portion **41** to the place positioned directly under the sensing-side pad **15**. In the present preferred embodiment, the field forming portion **42** spreads over the entirety of the place directly under the sensing-side pad **15**. In other words, in FIG. 2, it is formed over the entirety of a place positioned directly under the sensing-side surface electrode **6** having a substantially rectangular shape in a plan view excluding the covered region **25**.

[0078] Additionally, a p+ type region **46** (whose concentration is, for example, $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$) is formed at a surface part of the field forming portion **42** at the place positioned directly under the sensing-side pad **15**. The p.sup.+ type region **46** is connected directly to the sensing-side surface electrode **6**. The formation of the p+ type region **46** makes it

possible to stably keep the electric potential of the place positioned directly under the sensing-side pad **15** at a constant electric potential.

[0079] As shown in FIG. **6**, the gate-side p.sup.- type well **33** is formed at a place positioned directly under the gate-side pad **16**. A p+ type region **47** (whose concentration is, for example, $1 \times 10^{17} \text{ cm}^{-3}$ to $1 \times 10^{21} \text{ cm}^{-3}$) is formed at a surface part of the gate-side p.sup.- type well **33**.

[0080] A gate insulating film **48** is formed on the semiconductor substrate **2**, and a gate electrode **49** is formed on the gate insulating film **48**. The gate insulating film **48** is made of, for example, silicon oxide (SiO_2), and the gate electrode **49** is made of, for example, polysilicon.

[0081] The gate electrode **49** includes a functional portion **52** that is formed along lattice regions partitioned by the matrix-shaped unit cells **34** and **40** and that straddles between adjoining unit cells **34** and **40** in the current sensing portion **26** and the source portion **27**. Consequently, the gate electrode **49** faces channel regions **50** and **51** of the unit cells **34** and **40**, respectively, with the gate insulating film **48** therebetween. The channel regions **50** and **51** are outer regions of the n+ type source regions **38** and **44** in the cell forming portions **35** and **41** of the p.sup.- type body wells **31** and **32**, respectively.

[0082] As shown in FIG. **4**, the gate electrode **49** additionally includes a connection portion **53** in addition to the functional portion **52** facing the channel regions **50** and **51** of the unit cells **34** and **40**, respectively. The connection portion **53** straddles between the current sensing portion **26** and the source portion **27** across the removal region **8** that is below the surface electrode film **4** and that is between the source-side surface electrode **5** and the sensing-side surface electrode **6**. This connection portion **53** secures an electric connection between the functional portion **52** of the current sensing portion **26** and the functional portion **52** of the source portion **27**. In other words, the gate electrode **49** serves as an electrode shared between the current sensing portion **26** and the source portion **27**.

[0083] On the other hand, as shown in FIG. **7** and FIG. **8**, the gate electrode **49** is connected to the gate-side surface electrode **7** in the gate finger **19** of the semiconductor device **1**. In other words, the gate electrode **49** is formed so as to extend from the source portion **27** toward a lower part of the gate finger **19**, and has a contact portion **62** at a place directly under the gate finger **19**. Consequently, a gate voltage applied onto the gate-side pad **16** is also applied to the gate electrode **49** of the current sensing portion **26** through the contact portion **62** (FIG. **7**) and through the connection portion **53** (FIG. **4**).

[0084] Although the gate insulating film **48** is disposed below the gate electrode **49** in order to secure insulation between the gate electrode **49** and the semiconductor substrate **2**, the gate insulating film **48** is also formed at a place directly under the sensing-side pad **15** and at a place directly under the gate-side pad **16** in the present preferred embodiment. As shown in FIG. **4** and FIG. **7**, the gate insulating film **48** is made of an extension portion that is continuous with the gate insulating film **48** positioned directly under the functional portion **52** of the gate electrode **49**.

[0085] An interlayer insulating film **54** is formed on the semiconductor substrate **2** so as to cover the gate electrode **49**. The interlayer insulating film **54** is made of, for example, silicon oxide (SiO_2), and, preferably, contains P (phosphorus) or B (boron). In other words, the interlayer insulating film **54** may be BPSG (Boron Phosphorus Silicon Glass) or may be PSG (Phosphorus Silicon Glass). A SiO_2 film is easily produced, and, if this SiO_2 film contains P (phosphorus) or B (boron), it is also possible to perform a reflow process after the film is produced. The reflow process makes it possible to easily flatten the interlayer insulating film **54** (SiO_2 film), and hence makes it possible to easily join the sensing-side wire **23**, which possibly affects the heat dissipation capability of the current sensing portion **26**, according to a design plan.

[0086] The interlayer insulating film **54** integrally includes a first part **55** with which the gate electrode **49** is covered in the current sensing portion **26** and in the source portion **27**, a second part **56** disposed at a place directly under the sensing-side pad **15**, and a third part **57** disposed at a place

directly under the gate-side pad **16**. It is possible to give sufficient shock resistance (for example, wire bonding resistance) to the interlayer insulating film **54** by thickening the interlayer insulating film **54** positioned directly under the sensing-side pad **15** and the interlayer insulating film **54** positioned directly under the gate-side pad **16**.

[0087] The surface electrode film **4** (the source-side surface electrode **5**, the sensing-side surface electrode **6**, and the gate-side surface electrode **7**) is formed on the interlayer insulating film **54**. The source-side surface electrode **5** passes through the interlayer insulating film **54** and through the gate insulating film **48**, and is connected to the n⁺ type source region **38** and to the p⁺ type body contact region **39**. The sensing-side surface electrode **6** passes through the interlayer insulating film **54** and through the gate insulating film **48**, and is connected to the n⁺ type source region **44** and to the p⁺ type body contact region **45**. The gate-side surface electrode **7** (the gate finger **19**) passes through the interlayer insulating film **54**, and is connected to the gate electrode **49**.

[0088] The surface electrode film **4** may be an electrode film having a layered structure in which, for example, Ti, TiN, and AlCu are stacked together in this order from the bottom (i.e., from the semiconductor-substrate-2 side). The use of AlCu for the topmost surface of the surface electrode film **4** makes it possible to give more sufficient shock resistance (for example, wire bonding resistance) to the electrode film **4** than the use of Al.

[0089] The passivation film **10** is formed on the surface electrode film **4**. The passivation film **10** may be made of, for example, silicon nitride (SiN). The pad openings **11** to **13** are formed in the passivation film **10** as described above.

[0090] A drain electrode **58** is formed on a rear surface of the semiconductor substrate **2**. The drain electrode **58** may be an electrode film having a layered structure in which Ti, Ni, Au, and Ag are stacked together in this order from the semiconductor-substrate-2 side. The drain electrode **58** serves as an electrode shared between the current sensing portion **26** and the source portion **27**.

[0091] Next, as an example, a method for detecting an electric current in the semiconductor device **1** will be described with reference to FIG. **9**. FIG. **9** is a circuit diagram to describe current detection in the semiconductor device **1**.

[0092] As shown in FIG. **9**, the semiconductor device **1** has the principal-current-side source portion **27** and the current-detection-side current sensing portion **26** both of which are included in one chip. A detection resistor **59** is connected to a source S of the current sensing portion **26**. The detection resistor **59** may be built into a module together with the semiconductor device **1** when the semiconductor device **1** is built into the module or it may be built into the inside of the semiconductor device **1**, for example. A gate G and a drain D are shared between the current sensing portion **26** and the source portion **27** as described above.

[0093] A voltage larger than a threshold value is applied to the gate G in a state in which a voltage is applied between the source S and the drain D, and, as a result, an electric current flows between the source S and the drain D, and the semiconductor device **1** reaches an ON state. Consequently, a detection current $I_{\text{sub.SENSE}}$ flows through the current sensing portion **26**. On the other hand, a principal current $I_{\text{sub.MAIN}}$ flows through the source portion **27**.

[0094] Whether the principal current $I_{\text{sub.MAIN}}$ is a short-circuit current is determined by monitoring whether the voltage $V_{\text{sub.SENSE}}$ of the detection resistor **59** has exceeded a predetermined threshold value. The resistance $R_{\text{sub.SENSE}}$ of the detection resistor **59** is fixed, and therefore the voltage $V_{\text{sub.SENSE}}$ becomes higher in proportion to an increase in the detection current $I_{\text{sub.SENSE}}$. Therefore, the fact that the voltage $V_{\text{sub.SENSE}}$ has exceeded the threshold value denotes that an excessive detection current $I_{\text{sub.SENSE}}$ is flowing, and hence indicates that the current value $I_{\text{sub.MAIN}}$ of the principal current calculated based on a sensing ratio between the current sensing portion **26** and the source portion **27** is also in an excessive state.

[0095] In the aforementioned detection method, if the principal current $I_{\text{sub.MAIN}}$ that has actually flowed and the principal current $I_{\text{sub.MAIN}}$ that is calculated by multiplying the detection current $I_{\text{sub.SENSE}}$ by the sensing ratio are equal to each other, it is possible to accurately

perform the short-circuit detection, and it is possible to shut off the gate voltage at an appropriate timing.

[0096] However, as shown in FIG. 1, the source-side pads **14A** and **14B** are comparatively large, and the occupation area of the source-side wire **22** with respect to the pads **14A** and **14B** is a small, and, on the other hand, the sensing-side pad **15** is comparatively small, and therefore the occupation area of the sensing-side wire **23** with respect to the sensing-side pad **15** becomes large. This causes a difference in the amount of heat escaping through the wires **22** and **23**, and therefore there is a possibility that an error produced in on-resistance between the source portion **27** and the current sensing portion **26** will become larger. As a result, there is a case in which an excessive detection current $I_{\text{sub.SENSE}}$ flows to the current-detection side although the principal current $I_{\text{sub.MAIN}}$ is not a short-circuit current in actuality. In this case, short-circuit detection is strictly based on the voltage $V_{\text{sub.SENSE}}$ of the current-detection-side detection resistor **59**, and therefore there is a fear that it will be determined that it is a short circuit even when there is no need, and the gate voltage will be shut off.

[0097] Therefore, according to the semiconductor device **1**, the current sensing portion **26** is disposed so as to avoid being positioned directly under the sensing-side pad **15** as shown in FIG. 2. This makes it possible to maintain a fixed distance between the current sensing portion **26** and the sensing-side wire **23** when the sensing-side wire **23** (FIG. 1) is joined to the sensing-side pad **15**, and hence makes it possible to restrain heat generated at the current sensing portion **26** from escaping while being preferentially transmitted to the sensing-side wire **23**. Therefore, it is possible to lessen an error generated in on-resistance between the principal-current-side unit cell **34** of the source portion **27** and the sensing-side unit cell **40** of the current sensing portion **26**. Additionally, the current sensing portion **26** is not positioned directly under the sensing-side pad **15**, and therefore it is possible to prevent a shock caused when the sensing-side wire **23** is joined to the sensing-side pad **15** from running directly to the current sensing portion **26**, and it is also possible to restrain the current sensing portion **26** from being broken. As a result thereof, it is possible to improve the detection accuracy of the current value of a principal current detected by the current sensing portion **26**.

[0098] The use of the semiconductor substrate **2** made of SiC makes it possible to achieve an arrangement in which the current sensing portion **26** is disposed so as to avoid being positioned directly under the sensing-side pad **15** as mentioned above. In other words, in a Si semiconductor device, the amount of flowing current per unit area is small, and therefore a cell area for a somewhat large sensing portion is required to set an appropriate sensing ratio (about 1000 to 2000) having high detection accuracy with respect to a source portion having a large area through which a high current flows, and therefore it is difficult to form it so as to avoid being positioned directly thereunder. On the other hand, in the SiC semiconductor device, the amount of flowing current per unit area is large, and therefore it is possible to secure an appropriate sensing ratio even if the sensing portion is small in cell area with respect to the source portion, and therefore it is possible to form it so as to avoid being positioned directly thereunder.

[0099] Additionally, in the present preferred embodiment, the current sensing portion **26** is surrounded by the source portion **27** as shown in FIG. 3, and therefore it is possible to bring the amount of heat generation of the current sensing portion **26** close to that of the source portion **27**. Therefore, it is possible to lessen an error in on-resistance generated because of a difference in the amount of heat generation.

[0100] Additionally, in the present preferred embodiment, the entirety of the current sensing portion **26** is covered with the covered region **25** by the passivation film **10** as shown in FIG. 2, and a portion positioned directly over the current sensing portion **26** and the sensing-side pad **15** are clearly distinguished from each other when viewed from outside the semiconductor device **1**. Therefore, it is possible to prevent the sensing-side wire **23** from being erroneously joined to the portion positioned directly over the current sensing portion **26**. It is possible to reliably maintain a

fixed distance between the current sensing portion **26** and the sensing-side wire **23**.

[0101] Additionally, in the present preferred embodiment, the interlayer insulating film **54** has the second part **56** that is comparatively thick (for example, 1 μm or more) at a place directly under the sensing-side pad **15** as shown in FIG. **4** and FIG. **5**. This makes it possible to lessen a shock running to the current sensing portion **26** when the sensing-side wire **23** is joined to the sensing-side pad **15**. As a result, it is possible to secure the reliability of the detection accuracy of the current value of a principal current.

[0102] Next, a method for manufacturing the semiconductor device **1** will be described with reference to FIG. **10**.

[0103] For example, first, the n.sup.- type epitaxial layer **29** is formed on the n.sup.+ type base substrate **28** by means of epitaxial growth, so that the semiconductor substrate **2** is formed (step **S1**).

[0104] Thereafter, p.sup.- type impurity ions are selectively implanted into a surface part of the semiconductor substrate **2**, and, as a result, the p.sup.- type well **30** is formed (step **S2**).

[0105] Thereafter, n type impurity ions are selectively implanted into each of the cell forming portions **35** and **41**, and, as a result, the n.sup.+ type source regions **38** and **44** are formed (step **S3**).

[0106] Thereafter, p.sup.- type impurity ions are selectively implanted into the p-type well **30**, and, as a result, the p.sup.+ type body contact regions **39**, **45** and the p.sup.+ type regions **46**, **47** are formed (step **S4**).

[0107] Thereafter, the gate insulating film **48** is formed on the surface of the semiconductor substrate **2** by means of, for example, thermal oxidation (step **S5**).

[0108] Thereafter, polysilicon is deposited on the semiconductor substrate **2** according to, for example, a CV D method, and the gate electrode **49** is formed thereon by means of patterning (step **S6**).

[0109] Thereafter, the interlayer insulating film **54** is formed on the semiconductor substrate **2** according to, for example, the CVD method (step **S7**).

[0110] Thereafter, a contact hole that passes through the interlayer insulating film **54** and through the gate insulating film **48** is formed, and then the surface electrode film **4** is formed according to, for example, a sputtering method (step **S8** and step **S9**).

[0111] Thereafter, the passivation film **10** with which the surface electrode film **4** is covered is formed, and then the pad openings **11**, **12**, and **13** are formed by means of patterning (step **S10** and step **S11**).

[0112] Through these steps, the aforementioned semiconductor device **1** is obtained.

[0113] Although the present invention has been described as above, the present invention can be embodied in other modes.

[0114] For example, the gate structure of the semiconductor device **1** may be a trench gate structure shown in FIG. **11** without being limited to the planar gate structure shown in FIG. **4**. In the trench gate structure, a gate trench **60** is formed in the semiconductor substrate **2**, and a gate electrode **49** is embedded in its inside. In this case, the gate electrode **49** is not convex on the semiconductor substrate **2**, and therefore the first part **55** and the second part **56** of the interlayer insulating film **54** may be equal to each other in thickness.

[0115] Additionally, the current sensing portion **26** is not necessarily required to have the arrangement of FIG. **2** in which its entirety is covered with the passivation film **10**, and only one part of the current sensing portion **26** may be covered with the passivation film **10** as shown in FIG. **12**. In this case, the current sensing portion **26** partially overlaps with a portion positioned directly under the sensing-side pad **15**, and yet it is recommended to virtually set a joint region **61** of the sensing-side wire **23** in the sensing-side pad **15** at a position exclusive of the position of the current sensing portion **26**. In other words, the sensing-side joint region of the present invention is not necessarily required to coincide with the sensing-side pad **15**.

[0116] Besides, various design changes can be made within the scope of the subject matter

described in the claims.

[0117] The present application corresponds to Japanese Patent Application No. 2015-247727 filed with the Japan Patent Office on Dec. 18, 2015, and the entire disclosure of the application is incorporated herein by reference.

REFERENCE SIGNS LIST

[0118] **1** Semiconductor device [0119] **2** Semiconductor substrate [0120] **4** Surface electrode film [0121] **5** Source-side surface electrode [0122] **6** Sensing-side surface electrode [0123] **7** Gate-side surface electrode [0124] **10** Passivation film [0125] **12** Pad opening [0126] **15** Sensing-side pad [0127] **23** Sensing-side wire [0128] **26** Current sensing portion [0129] **27** Source portion [0130] **34** Principal-current-side unit cell [0131] **40** Sensing-side unit cell [0132] **54** Interlayer insulating film [0133] **55** First part [0134] **56** Second part [0135] **57** Third part [0136] **61** Joint region

Claims

1.-21. (canceled)

22. A semiconductor device comprising: a semiconductor chip having a first surface and a second surface; a first element portion that is formed at a side of the first surface of the semiconductor chip and that includes a first unit cell on a principal current side; a current sensing portion that is formed at the side of the first surface of the semiconductor chip and that includes a second unit cell on a current detection side; a first element-side surface electrode disposed above the first element portion; a sensing-side surface electrode disposed so that at least one part of the sensing-side surface electrode includes a region positioned above the current sensing portion, the sensing-side surface electrode having a substantially rectangular shape; a first element-side wiring member joined to the first element-side surface electrode; a sensing-side wiring member joined to the sensing-side surface electrode, the sensing-side wiring member being thinner than the first element-side wiring member; and a passivation film that selectively covers a portion positioned directly over the second unit cell of the sensing-side surface electrode and that has a first opening by which a part of the sensing-side surface electrode is exposed as a sensing-side pad, wherein the second unit cell is disposed at a position below the sensing-side surface electrode and so as to avoid being positioned directly under a joint part of the sensing-side wiring member, and both of the sensing-side surface electrode and the gate-side surface electrode are placed along an edge of the semiconductor chip.

23. The semiconductor device according to claim 22, wherein the current sensing portion is smaller than the sensing-side pad.

24. The semiconductor device according to claim 23, wherein the sensing-side wiring member is shorter than the first element-side wiring member.

25. The semiconductor device according to claim 24, wherein the sensing-side wiring member and the first element-side wiring member extend in different directions from each other from the semiconductor chip.

26. The semiconductor device according to claim 25, further comprising: an interlayer insulating film disposed between the current sensing portion and the sensing-side surface electrode; and a surface insulating film formed at a lower position than the interlayer insulating film, wherein the interlayer insulating film is formed thicker than the surface insulating film.

27. The semiconductor device according to claim 26, wherein the current sensing portion is formed in a region surrounded by the first element portion.

28. The semiconductor device according to claim 27, wherein the first unit cell and the second unit cell have mutually same cell structures, respectively.

29. The semiconductor device according to claim 28, wherein the current sensing portion is formed at only one place in an in-plane direction of the semiconductor chip.

30. The semiconductor device according to claim 29, wherein the interlayer insulating film has a

thickness of 1 μm or more.

31. The semiconductor device according to claim 30, wherein the first element portion and the current sensing portion are switching elements having control terminals, respectively, and the semiconductor device further comprises a control terminal-side surface electrode that is disposed on the semiconductor chip and that has a control terminal-side joint region to which a wiring member is joined, wherein the interlayer insulating film is also disposed at a place directly under the control terminal-side joint region.

32. The semiconductor device according to claim 31, wherein the interlayer insulating film includes a SiO_2 film.

33. The semiconductor device according to claim 32, wherein the SiO_2 film contains P (phosphorus).

34. The semiconductor device according to claim 33, wherein the SiO_2 film contains B (boron).

35. The semiconductor device according to claim 34, wherein the sensing-side surface electrode includes an electrode having a layered structure in which Ti, TiN, and AlCu are stacked together in this order from a bottom of the layered structure to a top of the layered structure.

36. The semiconductor device according to claim 35, wherein the first element portion and the current sensing portion are switching elements having control terminals, respectively, at least one of the first element portion and the current sensing portion includes a control terminal-side surface electrode that is disposed on the semiconductor chip, the passivation film has a second opening by which a part of the control terminal-side surface electrode is exposed as a control terminal-side pad, and wherein the sensing-side pad and the control terminal-side pad are each formed so as to have a shape long in a same direction.

37. The semiconductor device according to claim 36, the sensing-side pad has a first length of a long side of 1.2 mm or less and a second length of a short side of 0.6 mm or less.

38. The semiconductor device according to claim 37, wherein the sensing-side surface electrode is formed in a quadrangular shape in a plan view such that a part of the sensing-side surface electrode is a covered region which is covered with the passivation film, a recess is formed by denting a part of at least one side of the sensing-side surface electrode such that the covering region is formed in the recess in plan view, and the current sensing portion is formed directly under the covered region.

39. The semiconductor device according to claim 38, wherein the sensing-side wiring member has a diameter from 100 μm to 200 μm .

40. The semiconductor device according to claim 39, wherein the first element-side wiring member is a first wire, and the sensing-side wiring member is a second wire.
