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Inventor(s)

Buehler; David Paul et al.

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### SYSTEMS AND METHODS FOR POWER MODULE FOR INVERTER FOR ELECTRIC VEHICLE

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#### Abstract

A power module includes: a first substrate having an outer surface and an inner surface, the first substrate extending from a first longitudinal end toward a second longitudinal end; a semiconductor die coupled to the inner surface of the first substrate; and a second substrate having an outer surface and an inner surface, the semiconductor die being coupled to the inner surface of the second substrate, the second substrate extending from a first longitudinal end toward a second longitudinal end, wherein the first longitudinal end of the first substrate is longitudinally offset from the first longitudinal end of the second substrate.

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**Inventors:** Buehler; David Paul (Noblesville, IN), Gertiser; Kevin M. (Carmel, IN), Ihms; David W. (Kokomo, IN), Gose; Mark Wendell (Kokomo, IN)

**Applicant:** BorgWarner US Technologies LLC (Wilmington, DE)

**Family ID:** 1000008561425

**Assignee:** BorgWarner US Technologies LLC (Wilmington, DE)

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**Background/Summary**

CROSS-REFERENCE TO RELATED APPLICATION(S) [0001] This application claims the benefit of priority to U.S. patent application Ser. No. 18/175,270, filed Feb. 27, 2023, which claims priority to U.S. Provisional Patent Application No. 63/377,486, filed Sep. 28, 2022, U.S. Provisional Patent Application No. 63/377,501, filed Sep. 28, 2022, U.S. Provisional Patent Application No. 63/377,512, filed Sep. 28, 2022, and U.S. Provisional Patent Application No. 63/378,601, filed Oct. 6, 2022, the entireties of which are incorporated by reference herein.

## TECHNICAL FIELD

[0002] Various embodiments of the present disclosure relate generally to a power module for an inverter for an electric vehicle, and more specifically, to a power module including an electrically conductive spacer or flexible circuit.

## BACKGROUND

[0003] Inverters, such as those used to drive a motor in an electric vehicle, for example, are responsible for converting High Voltage Direct Current (HVDC) into Alternating Current (AC) to drive the motor. In an inverter, a power module may include devices that generate a large amount of heat. The layout and design of the power module affects the operation of the devices and the thermal characteristics of the power module. Incorrect operation of the devices or overheating of the power module may compromise the operation of the inverter.

[0004] The present disclosure is directed to overcoming one or more of these above-referenced challenges.

## SUMMARY OF THE DISCLOSURE

[0005] In some aspects, the techniques described herein relate to a power module, including: a first substrate having an outer surface and an inner surface; a semiconductor die coupled to the inner surface of the first substrate; a second substrate having an outer surface and an inner surface, the semiconductor die being coupled to the inner surface of the second substrate; and a first electrically conductive spacer coupled to inner surface of the first substrate and to the inner surface of the second substrate.

[0006] In some aspects, the techniques described herein relate to a power module, wherein the first substrate further includes a middle section between the inner surface and the outer surface, wherein the middle section includes a ceramic, and the outer surface and the inner surface of the first substrate includes a metal.

[0007] In some aspects, the techniques described herein relate to a power module, further including a first lead coupled to the inner surface of the second substrate.

[0008] In some aspects, the techniques described herein relate to a power module, wherein the first electrically conductive spacer is coupled to a first part of the inner surface of the second substrate, and the semiconductor die is coupled to a second part of the inner surface of the second substrate, wherein the first part and the second part are not directly coupled to one another.

[0009] In some aspects, the techniques described herein relate to a power module, further including a second electrically conductive spacer coupled to the inner surface of the second substrate and to the inner surface of the first substrate.

[0010] In some aspects, the techniques described herein relate to a power module, wherein the first electrically conductive spacer and the second electrically conductive spacer are coplanar.

[0011] In some aspects, the techniques described herein relate to a power module, wherein the ceramic includes silicon nitride.

[0012] In some aspects, the techniques described herein relate to a power module, wherein the second substrate further includes a middle layer between the inner surface and the outer surface, wherein the middle layer includes a ceramic, and the outer surface and the inner surface of the second substrate includes a metal.

[0013] In some aspects, the techniques described herein relate to a power module, wherein the source connection of the semiconductor die is coplanar with the connection.

[0014] In some aspects, the techniques described herein relate to a power module, wherein the semiconductor die includes a drain, wherein the drain is coupled to the inner surface of the first substrate.

[0015] In some aspects, the techniques described herein relate to a power module, wherein the semiconductor die includes a source, wherein the source is coupled to the inner surface of the second substrate.

[0016] In some aspects, the techniques described herein relate to an inverter including the power module.

[0017] In some aspects, the techniques described herein relate to a vehicle including the inverter.

[0018] In some aspects, the techniques described herein relate to a system including: an inverter configured to convert DC power from a battery to AC power to drive a motor, wherein the inverter includes: a power module for an inverter for an electric vehicle, the power module including: a first substrate; a second substrate; and an electrically conductive spacer connecting the first substrate to the second substrate.

[0019] In some aspects, the techniques described herein relate to a system, further including: the battery configured to supply the DC power to the inverter; and the motor configured to receive the AC power from the inverter to drive the motor.

[0020] In some aspects, the techniques described herein relate to a system including: a power module for an inverter, the power module including: a lower substrate including an upper conductive layer; an upper substrate including a lower conductive layer; and one or more electrically conductive spacers between the lower substrate and the upper substrate, the one or more electrically conductive spacers configured to maintain a distance between the lower substrate and the upper substrate and provide an electrically conductive path from the lower conductive layer to the upper conductive layer.

[0021] In some aspects, the techniques described herein relate to a system, wherein: the lower conductive layer includes a first lower conductive region, a second lower conductive region, and a third lower conductive region, and the upper conductive layer includes a first upper conductive region and a second upper conductive region.

[0022] In some aspects, the techniques described herein relate to a system, wherein: the one or more electrically conductive spacers includes a first electrically conductive spacer and a second electrically conductive spacer, the first electrically conductive spacer connects the first lower conductive region to the first upper conductive region, and the second electrically conductive spacer connects the second lower conductive region to the second upper conductive region.

[0023] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: a first power switch configured to selectively electrically connect the first upper conductive region to the second lower conductive region, and a second power switch configured to selectively electrically connect the third lower conductive region to the second upper conductive region.

[0024] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: a first interconnect on the first lower conductive region, a second interconnect on the third lower conductive region, and a third interconnect on the third lower conductive region.

[0025] In some aspects, the techniques described herein relate to a system, wherein: the first power switch is configured to selectively electrically connect the first interconnect to the third interconnect through the first lower conductive region, the first electrically conductive spacer, the first upper conductive region, the first power switch, and the second lower conductive region, and the second power switch is configured to selectively electrically connect the second interconnect to the third interconnect through the third lower conductive region, the second power switch, the second upper conductive region, the second electrically conductive spacer, and the second lower conductive region.

[0026] In some aspects, the techniques described herein relate to a power module, including: a first substrate; a second substrate; a semiconductor die disposed between the first substrate and the second substrate, the semiconductor die having a drain coupled to the first substrate, and a source coupled to the second substrate; a first electrically conductive spacer disposed between the first substrate and the second substrate, wherein a connection between the first electrically conductive spacer and the first substrate is coplanar with a connection between the drain of the semiconductor die and the first substrate.

[0027] In some aspects, the techniques described herein relate to a power module, wherein a connection between the first electrically conductive spacer and the second substrate is coplanar with a connection between the source of the semiconductor die and the second substrate.

[0028] In some aspects, the techniques described herein relate to a power module, including: a first substrate having an outer surface and an inner surface; a semiconductor die coupled to the inner surface of the first substrate; a second substrate having an outer surface and an inner surface, the semiconductor die being coupled to the inner surface of the second substrate; and a flex circuit coupled to the semiconductor die.

[0029] In some aspects, the techniques described herein relate to a power module, wherein the flex circuit is coupled to the inner surface of the second substrate.

[0030] In some aspects, the techniques described herein relate to a power module, wherein the flex circuit includes an insulating material and an electrically conductive material, wherein the inner surface of the second substrate is electrically insulated from the electrically conductive material of the flex circuit.

[0031] In some aspects, the techniques described herein relate to a power module, wherein the electrically conductive material of the flex circuit is coupled to the semiconductor die.

[0032] In some aspects, the techniques described herein relate to a power module, wherein the semiconductor die includes a gate, wherein the electrically conductive material of the flex circuit is coupled to the gate of the semiconductor die.

[0033] In some aspects, the techniques described herein relate to a power module, wherein the semiconductor die is coupled to the second substrate, through the flex circuit.

[0034] In some aspects, the techniques described herein relate to a power module, wherein the semiconductor die includes a source connection, wherein the source connection is coupled to the second substrate, through the flex circuit.

[0035] In some aspects, the techniques described herein relate to a power module, wherein the semiconductor die includes a gate, wherein electrical connections to the gate are contained only within the flex circuit.

[0036] In some aspects, the techniques described herein relate to a power module, wherein the semiconductor die includes a gate, wherein electrical connections to the gate, within the power module, are contained solely within the flex circuit.

[0037] In some aspects, the techniques described herein relate to a power module, wherein the semiconductor die includes a gate, wherein electrical connections to the gate, within the power module, do not extend through any part of the second substrate.

[0038] In some aspects, the techniques described herein relate to a power module, wherein the first substrate further includes a middle section between the inner surface and the outer surface, wherein the middle section includes a ceramic and the outer surface and the inner surface of the first substrate include a metal.

[0039] In some aspects, the techniques described herein relate to a power module, wherein the ceramic include silicon nitride.

[0040] In some aspects, the techniques described herein relate to a power module, further include a first lead coupled to the inner surface of the second substrate.

[0041] In some aspects, the techniques described herein relate to a power module, wherein the second substrate further includes a middle surface between the inner surface and the outer surface,

wherein the inner surface includes a ceramic and the outer surface and the inner surface of the second substrate include a metal.

[0042] In some aspects, the techniques described herein relate to a power module, wherein the semiconductor die includes a drain, wherein the drain is coupled to the inner surface of the first substrate.

[0043] In some aspects, the techniques described herein relate to a power module, wherein the semiconductor die includes a source, wherein the source is coupled to the inner surface of the second substrate.

[0044] In some aspects, the techniques described herein relate to an inverter, including the power module.

[0045] In some aspects, the techniques described herein relate to a vehicle, including the inverter.

[0046] In some aspects, the techniques described herein relate to a power module, including: a semiconductor die having a source connection, a drain connection, and a gate; a substrate coupled to the source connection; and a flex circuit coupled to gate, wherein electrical connections to the gate, within the power module, are contained solely within the flex circuit.

[0047] In some aspects, the techniques described herein relate to a power module, including: a semiconductor die having a source connection, a drain connection, and a gate; a substrate coupled to the source connection; and a flex circuit coupled to gate, wherein electrical connections to the gate, within the power module, do not extend through any part of the substrate.

[0048] In some aspects, the techniques described herein relate to a system including: an inverter configured to convert DC power from a battery to AC power to drive a motor, wherein the inverter includes: a power module including: a first substrate including a first conductive layer; a second substrate including a second conductive layer; a power switch between the first substrate and the second substrate; and a flex layer between the first substrate and the second substrate, the flex layer electrically connected to the power switch.

[0049] In some aspects, the techniques described herein relate to a system, wherein the first conductive layer and the second conductive layer are configured to route high voltage power through the power switch, and the flex layer is configured to route a control signal to the power switch.

[0050] In some aspects, the techniques described herein relate to a system, wherein the flex layer includes a base polyimide material, an internal conductive layer, and a coverlet.

[0051] In some aspects, the techniques described herein relate to a system, wherein the base polyimide material of the flex layer is laminated to the first conductive layer.

[0052] In some aspects, the techniques described herein relate to a system, wherein: the power switch includes a power switch gate connection, and the base polyimide material and the internal conductive layer are routed between the first conductive layer and the power switch gate connection so that the internal conductive layer is electrically connected to the power switch gate connection and the internal conductive layer is electrically insulated from the first conductive layer by the base polyimide material.

[0053] In some aspects, the techniques described herein relate to a system, wherein the flex layer is configured to insulate a perimeter of the power switch from the first conductive layer.

[0054] In some aspects, the techniques described herein relate to a system, wherein the flex layer is configured to prevent disruption of current flowing in the first conductive layer.

[0055] In some aspects, the techniques described herein relate to a system, further including: the battery configured to supply the DC power to the inverter; and the motor configured to receive the AC power from the inverter to drive the motor.

[0056] In some aspects, the techniques described herein relate to a system including: a power module for an inverter, the power module including: a first substrate including a first conductive layer; a second substrate including a second conductive layer; a power switch between the first substrate and the second substrate; and a flex layer between the first substrate and the second

substrate, the flex layer electrically connected to the power switch.

[0057] In some aspects, the techniques described herein relate to a system, wherein: the power switch includes a power switch gate connection, and the power module further includes: a point-of-use controller between the first substrate and the second substrate, the point-of-use controller configured to provide a signal via the flex layer to the power switch gate connection to control the power switch.

[0058] In some aspects, the techniques described herein relate to a system, wherein: the power switch further includes a control connection, and the point-of-use controller is electrically connected to the control connection via the flex layer.

[0059] In some aspects, the techniques described herein relate to a system, wherein: the power switch further includes: a first power connection connected to one or more of the first conductive layer or the second conductive layer, and a second power connection connected to one or more of the first conductive layer or the second conductive layer.

[0060] In some aspects, the techniques described herein relate to a system, wherein: the first power connection is configured to be connected to a power supply, and the second power connection is configured to be connected to a load.

[0061] In some aspects, the techniques described herein relate to a system, wherein: the power switch is configured to control a flow of current between the first conductive layer and the second conductive layer to control a flow of current between the power supply and the load, and the flex layer is configured to route a control signal to the power switch.

[0062] In some aspects, the techniques described herein relate to a system including: a power module for an inverter, the power module including: a lower substrate including a lower conductive layer; an upper substrate including an upper conductive layer; a power switch between the lower conductive layer and the upper conductive layer, the power switch including a power switch gate connection; and a flex layer between the lower conductive layer and the upper conductive layer, the flex layer electrically connected to the power switch gate connection.

[0063] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: a gate control pin, wherein the flex layer electrically connects the gate control pin to the power switch gate connection.

[0064] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: a gate control pin, and a point-of-use controller, wherein the flex layer electrically connects the gate control pin to the point-of-use controller, and electrically connects the point-of-use controller to the power switch gate connection.

[0065] In some aspects, the techniques described herein relate to a system, wherein the flex layer includes an insulating layer and a conductive layer.

[0066] In some aspects, the techniques described herein relate to a system, wherein the insulating layer is connected to the lower conductive layer.

[0067] In some aspects, the techniques described herein relate to a system, wherein the power switch includes a die, and wherein the die includes: an upper surface connected to the upper conductive layer, and a lower surface connected to the lower conductive layer through an opening in the flex layer.

[0068] In some aspects, the techniques described herein relate to a power module, including: a first substrate having an outer surface and an inner surface, the first substrate extending from a first longitudinal end toward a second longitudinal end; a semiconductor die coupled to the inner surface of the first substrate; and a second substrate having an outer surface and an inner surface, the semiconductor die being coupled to the inner surface of the second substrate, the second substrate extending from a first longitudinal end toward a second longitudinal end, wherein the first longitudinal end of the first substrate is longitudinally offset from the first longitudinal end of the second substrate.

[0069] In some aspects, the techniques described herein relate to a power module, wherein the

second longitudinal end of the first substrate is offset from the second longitudinal end of the second substrate.

[0070] In some aspects, the techniques described herein relate to a power module, wherein a length of the first substrate is approximately equal to a length of the second substrate.

[0071] In some aspects, the techniques described herein relate to a power module, wherein a length of the first substrate is greater than a length of the second substrate.

[0072] In some aspects, the techniques described herein relate to a power module, further including a first lead frame coupled to the inner surface of the first substrate.

[0073] In some aspects, the techniques described herein relate to a power module, further including a second lead frame coupled to the inner surface of the first substrate.

[0074] In some aspects, the techniques described herein relate to a power module, further including a second lead frame coupled to the inner surface of the second substrate.

[0075] In some aspects, the techniques described herein relate to a power module, wherein the first lead frame has a thickness greater than 500 microns.

[0076] In some aspects, the techniques described herein relate to a power module, wherein the first lead frame has a thickness greater than 700 microns.

[0077] In some aspects, the techniques described herein relate to a power module, wherein the first lead frame has a thickness greater than a space between the inner surface of the first substrate and the inner surface of the second substrate.

[0078] In some aspects, the techniques described herein relate to a power module, further including an overmold coupled to the first substrate, the second substrate, and the semiconductor die.

[0079] In some aspects, the techniques described herein relate to an inverter including the power module.

[0080] In some aspects, the techniques described herein relate to a vehicle including the inverter.

[0081] In some aspects, the techniques described herein relate to a power module, including: a first substrate having an outer surface and an inner surface, the first substrate extending from a first longitudinal end toward a second longitudinal end; a semiconductor die coupled to the inner surface of the first substrate; a second substrate having an outer surface and an inner surface, the semiconductor die being coupled to the inner surface of the second substrate, the second substrate extending from a first longitudinal end toward a second longitudinal end; and a lead frame coupled to the inner surface of the first substrate, wherein a thickness of the lead frame is greater than a distance from the inner surface of the first substrate to the inner surface of the second substrate.

[0082] In some aspects, the techniques described herein relate to a system including: an inverter configured to convert DC power from a battery to AC power to drive a motor, wherein the inverter includes: a power module including: a lower substrate including a lower conductive layer extending in a lower plane; and an upper substrate including an upper conductive layer extending in an upper plane separated from the lower plane, wherein an end of the upper substrate is offset in the upper plane from a corresponding end of the lower substrate so that a normal vector from the upper plane at the end of the upper substrate does not intersect the lower substrate.

[0083] In some aspects, the techniques described herein relate to a system, further including: a first lead frame connected to the lower conductive layer, wherein at least a portion of the first lead frame is in the upper plane; and a second lead frame connected to the upper conductive layer, wherein at least a portion of the second lead frame is in the lower plane.

[0084] In some aspects, the techniques described herein relate to a system, wherein one or more of the first lead frame or the second lead frame has a thickness greater than 500 microns.

[0085] In some aspects, the techniques described herein relate to a system, wherein a distance between an inner surface of the upper substrate and an inner surface of the lower substrate is less than 500 microns.

[0086] In some aspects, the techniques described herein relate to a system, wherein a length of the lower substrate is approximately equal to a length of the upper substrate.



[0087] In some aspects, the techniques described herein relate to a system, further including: the battery configured to supply the DC power to the inverter; and the motor configured to receive the AC power from the inverter to drive the motor.

[0088] In some aspects, the techniques described herein relate to a system including: a power module for an inverter, the power module including: a first substrate including a first conductive layer extending in a first plane; and a second substrate including a second conductive layer extending in a second plane separated from the first plane, wherein an end of the first substrate is offset in the first plane from a corresponding end of the second substrate so that a normal vector from the first plane at the end of the first substrate does not intersect the second substrate.

[0089] In some aspects, the techniques described herein relate to a system including: a power module for an inverter, the power module including: a lower substrate including a lower conductive layer extending in a lower plane; an upper substrate including an upper conductive layer extending in an upper plane separated from the lower plane; a first lead frame connected to the lower conductive layer, wherein at least a portion of the first lead frame is in the upper plane; and a second lead frame connected to the upper conductive layer, wherein at least a portion of the second lead frame is in the lower plane.

[0090] In some aspects, the techniques described herein relate to a system including: an inverter configured to convert DC power from a battery to AC power to drive a motor, wherein the inverter includes: a first power module, the first power module including: a first substrate including a first conductive layer; a second substrate including a second conductive layer; a power switch between the first conductive layer and the second conductive layer, the power switch including a gate connection, wherein the power switch is configured to selectively electrically connect the first conductive layer to the second conductive layer based on a signal to the gate connection; and a point-of-use controller between the first conductive layer and the second conductive layer, the point-of-use controller configured to provide the signal to the gate connection to control the power switch.

[0091] In some aspects, the techniques described herein relate to a system, wherein the first power module further includes: a first lead frame connection; and a second lead frame connection, wherein the point-of-use controller is on the first substrate between the first lead frame connection and the second lead frame connection.

[0092] In some aspects, the techniques described herein relate to a system, wherein the first power module further includes: an electrically conductive spacer between the first substrate and the second substrate, wherein the first lead frame connection is connected to the first power switch via the electrically conductive spacer.

[0093] In some aspects, the techniques described herein relate to a system, wherein the first power module further includes: a flex layer between the first substrate and the second substrate, wherein the point-of-use controller is connected to the gate connection via the flex layer.

[0094] In some aspects, the techniques described herein relate to a system, wherein the first power module further includes: a control connection, wherein the first point-of-use controller is connected to the control connection via the flex layer.

[0095] In some aspects, the techniques described herein relate to a system, wherein the power switch includes one or more silicon carbide dies.

[0096] In some aspects, the techniques described herein relate to a system, wherein the inverter further includes: a second power module; and a third power module.

[0097] In some aspects, the techniques described herein relate to a system, further including: the battery configured to supply the DC power to the inverter; and the motor configured to receive the AC power from the inverter to drive the motor.

[0098] In some aspects, the techniques described herein relate to a system including: a power module for an inverter, the power module including: a first substrate including a first conductive region and a second conductive region; a second substrate including a third conductive region and a

fourth conductive region; a first power switch between the first substrate and the second substrate, the first power switch including a first gate connection, wherein the first power switch is configured to selectively electrically connect the first conductive region to the third conductive region based on a first signal to the first gate connection; and a first point-of-use controller between the first substrate and the second substrate, the first point-of-use controller configured to provide the first signal to the first gate connection to control the first power switch.

[0099] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: a second power switch between the first substrate and the second substrate, the second power switch including a second gate connection, wherein the second power switch is configured to selectively electrically connect the second conductive region to the fourth conductive region based on a second signal to the second gate connection.

[0100] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: a second point-of-use controller between the first substrate and the second substrate, the second point-of-use controller configured to provide the second signal to the second gate connection to control the second power switch.

[0101] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: a first lead frame connection; and a second lead frame connection, wherein the first point-of-use controller is on the first substrate between the first lead frame connection and the second lead frame connection.

[0102] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: an electrically conductive spacer between the first substrate and the second substrate, wherein the first lead frame connection is connected to the first power switch via the electrically conductive spacer.

[0103] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: a flex layer between the first substrate and the second substrate, wherein the first point-of-use controller is connected to the first gate connection via the flex layer.

[0104] In some aspects, the techniques described herein relate to a system including: a power module for an inverter, the power module including: a lower substrate including a lower conductive layer, the lower conductive layer including a first lower conductive region and a second lower conductive region; an upper substrate including an upper conductive layer, the upper conductive layer including a first upper conductive region and a second upper conductive region; a first power switch between the first lower conductive region and the first upper conductive region, the first power switch including a first gate connection, wherein the first power switch is configured to selectively electrically connect the first lower conductive region to the first upper conductive region based on a first signal to the first gate connection; a first point-of-use controller between the lower conductive layer and the upper conductive layer, the first point-of-use controller configured to provide the first signal to the first gate connection to control the first power switch; a second power switch between the second lower conductive region and the second upper conductive region, the second power switch including a second gate connection, wherein the second power switch is configured to selectively electrically connect the second lower conductive region to the second upper conductive region based on a second signal to the second gate connection; and a second point-of-use controller between the lower conductive layer and the upper conductive layer, the second point-of-use controller configured to provide the second signal to the second gate connection to control the second power switch.

[0105] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: a first lead frame connection; and a second lead frame connection, wherein the first point-of-use controller is on the lower substrate between the first lead frame connection and the second lead frame connection.

[0106] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: a third lead frame connection, wherein the second point-of-use controller

is on the lower substrate between the third lead frame connection and the second lead frame connection.

[0107] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: an electrically conductive spacer between the lower substrate and the upper substrate, wherein the first lead frame connection is connected to the first power switch via the electrically conductive spacer.

[0108] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: a flex layer between the lower conductive layer and the upper conductive layer, wherein the first point-of-use controller is connected to the first gate connection via the flex layer.

[0109] In some aspects, the techniques described herein relate to a system, wherein the power module further includes: a control connection, wherein the first point-of-use controller is connected to the control connection via the flex layer.

[0110] In some aspects, the techniques described herein relate to a power module, including: a first substrate having an outer surface and an inner surface, the first substrate extending from a first longitudinal end toward a second longitudinal end; a power switch including a semiconductor die, the power switch being coupled to the inner surface of the first substrate; a second substrate having an outer surface and an inner surface, the power switch being coupled to the inner surface of the second substrate, the second substrate extending from a first longitudinal end toward a second longitudinal end, wherein the first longitudinal end of the first substrate is longitudinally offset from the first longitudinal end of the second substrate; a first electrically conductive spacer coupled to the inner surface of the first substrate and to the inner surface of the second substrate; and a flex circuit coupled to the power switch.

[0111] In some aspects, the techniques described herein relate to a power module, wherein the first substrate further includes a middle layer between the inner surface and the outer surface, wherein the middle layer includes a ceramic, and the outer surface and the inner surface of the first substrate include a metal.

[0112] In some aspects, the techniques described herein relate to a power module, wherein the electrically conductive spacer is coupled to a first part of the inner surface of the second substrate, and the power switch is coupled to a second part of the inner surface of the second substrate, wherein the first part and the second part are not directly coupled to one another.

[0113] In some aspects, the techniques described herein relate to a power module, further including a second electrically conductive spacer coupled to the inner surface of the second substrate and to the inner surface of the first substrate.

[0114] In some aspects, the techniques described herein relate to a power module, wherein the semiconductor die includes silicon carbide.

[0115] In some aspects, the techniques described herein relate to a power module, wherein the second substrate further includes a middle layer between the inner surface and the outer surface, wherein the middle layer includes a ceramic, and the outer surface and the inner surface of the second substrate include a metal.

[0116] In some aspects, the techniques described herein relate to a power module, wherein a source connection of the power switch is coplanar with the connection.

[0117] In some aspects, the techniques described herein relate to a power module, wherein the power switch includes a drain, wherein the drain is coupled to the inner surface of the first substrate.

[0118] In some aspects, the techniques described herein relate to a power module, wherein the power switch includes a source, wherein the source is coupled to the inner surface of the second substrate.

[0119] In some aspects, the techniques described herein relate to a power module, wherein the flex circuit includes an insulating material and an electrically-conductive material, wherein the inner

surface of the second substrate is electrically insulated from the electrically conductive material of the flex circuit.

[0120] In some aspects, the techniques described herein relate to a power module, wherein the power switch includes a gate, wherein electrical connections to the gate are contained only within the flex circuit.

[0121] In some aspects, the techniques described herein relate to a power module, wherein the power switch includes a gate, wherein electrical connections to the gate, within the power module, are contained solely within the flex circuit.

[0122] In some aspects, the techniques described herein relate to a power module, wherein the power switch includes a gate, wherein electrical connections to the gate, within the power module, do not extend through any part of the second substrate.

[0123] In some aspects, the techniques described herein relate to a power module, further including: a first connection; a second connection, wherein the power switch includes a first gate terminal, the power switch configured to control a first flow of current between the first connection and the second connection based on a first signal to the first gate terminal; and a first point-of-use controller configured to provide the first signal to the first gate terminal to control the first power switch.

[0124] In some aspects, the techniques described herein relate to an inverter including the power module.

[0125] In some aspects, the techniques described herein relate to a vehicle including the inverter.

[0126] In some aspects, the techniques described herein relate to a power module, including: a first substrate having an outer surface and an inner surface, the first substrate extending from a first longitudinal end toward a second longitudinal end; a power switch including a semiconductor die coupled to the inner surface of the first substrate, wherein the semiconductor die includes silicon carbide; a second substrate having an outer surface and an inner surface, the semiconductor die being coupled to the inner surface of the second substrate, the second substrate extending from a first longitudinal end toward a second longitudinal end, wherein the first longitudinal end of the first substrate is longitudinally offset from the first longitudinal end of the second substrate; a first electrically conductive spacer coupled to inner surface of the first substrate and to the inner surface of the second substrate; a flex circuit coupled to the semiconductor die; a first connection; a second connection, wherein the power switch includes a first gate terminal, the first power switch configured to control a first flow of current between the first connection and the second connection based on a first signal to the first gate terminal; and a first point-of-use controller configured to provide the first signal to the first gate terminal to control the first power switch.

[0127] In some aspects, the techniques described herein relate to an inverter, including the power module.

[0128] In some aspects, the techniques described herein relate to a vehicle, including the inverter.

[0129] In some aspects, the techniques described herein relate to a power module, including: a first substrate having an outer surface and an inner surface, the first substrate extending from a first longitudinal end toward a second longitudinal end; a power switch including a semiconductor die coupled to the inner surface of the first substrate, wherein the semiconductor die includes silicon carbide; a second substrate having an outer surface and an inner surface, the semiconductor die being coupled to the inner surface of the second substrate, the second substrate extending from a first longitudinal end toward a second longitudinal end, wherein the first longitudinal end of the first substrate is longitudinally offset from the first longitudinal end of the second substrate; a first electrically conductive spacer coupled to inner surface of the first substrate and to the inner surface of the second substrate; a flex circuit coupled to the semiconductor die; a first connection; a second connection, wherein the power switch includes a first gate terminal, the first power switch configured to control a first flow of current between the first connection and the second connection based on a first signal to the first gate terminal, wherein electrical connections to the first gate

terminal, within the power module, do not extend through any part of the second substrate; and a first point-of-use controller configured to provide the first signal to the first gate terminal to control the first power switch.

[0130] Additional objects and advantages of the disclosed embodiments will be set forth in part in the description that follows, and in part will be apparent from the description, or may be learned by practice of the disclosed embodiments. The objects and advantages of the disclosed embodiments will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims.

[0131] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the disclosed embodiments, as claimed.

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## **Description**

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0132] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate various exemplary embodiments and together with the description, serve to explain the principles of the disclosed embodiments.

[0133] FIG. 1 depicts an exemplary system infrastructure for a vehicle including a combined inverter and converter, according to one or more embodiments.

[0134] FIG. 2 depicts an exemplary system infrastructure for the combined inverter and converter of FIG. 1 with a point-of-use switch controller, according to one or more embodiments.

[0135] FIG. 3 depicts an exemplary system infrastructure for the controller of FIG. 2, according to one or more embodiments.

[0136] FIG. 4 depicts an exemplary system infrastructure for the point-of-use switch controller of FIG. 2, according to one or more embodiments.

[0137] FIG. 5 depicts an exemplary system infrastructure for the upper power module of FIG. 4, according to one or more embodiments.

[0138] FIG. 6 depicts an exemplary electrical schematic for a power module including electrically conductive spacers, according to one or more embodiments.

[0139] FIG. 7 depicts an exemplary architecture for a power module including electrically conductive spacers, according to one or more embodiments.

[0140] FIG. 8 depicts a cross-section view of an exemplary architecture for a power module including electrically conductive spacers, according to one or more embodiments.

[0141] FIG. 9 depicts a single-sided cooling heat flow in a cross-section view of an exemplary architecture for a power module including electrically conductive spacers, according to one or more embodiments, in cross-section view.

[0142] FIG. 10 depicts an assembly of a power module with devices on two substrates and an assembly of an exemplary power module with devices on a single substrate, according to one or more embodiments.

[0143] FIG. 11 depicts an assembly of an exemplary power module including a substrate layer and a flex layer, according to one or more embodiments.

[0144] FIG. 12 depicts a cross-section view of an exemplary architecture for a power module including a surface mount component, according to one or more embodiments.

[0145] FIG. 13 depicts a cross-section view of an exemplary architecture for a power module including a shifted substrate, according to one or more embodiments.

[0146] FIG. 14 depicts an assembly of an exemplary power module including a shifted substrate, according to one or more embodiments.

[0147] FIG. 15 depicts a cross-section view of an exemplary architecture for a sintered power

module including a shifted substrate, according to one or more embodiments.

[0148] FIGS. **16A** and **16B** depict an assembly of an exemplary sintered power module including a shifted substrate, according to one or more embodiments.

[0149] FIG. **17** depicts a cross-section view of an exemplary architecture for a power module including a point-of-use switch controller, according to one or more embodiments.

[0150] FIG. **18** depicts an assembly of an exemplary power module including a point-of-use switch controller, according to one or more embodiments.

#### DETAILED DESCRIPTION OF EMBODIMENTS

[0151] Both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the features, as claimed. As used herein, the terms “comprises,” “comprising,” “has,” “having,” “includes,” “including,” or other variations thereof, are intended to cover a non-exclusive inclusion such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements, but may include other elements not expressly listed or inherent to such a process, method, article, or apparatus. In this disclosure, unless stated otherwise, relative terms, such as, for example, “about,” “substantially,” and “approximately” are used to indicate a possible variation of  $\pm 10\%$  in the stated value. In this disclosure, unless stated otherwise, any numeric value may include a possible variation of  $\pm 10\%$  in the stated value.

[0152] The terminology used below may be interpreted in its broadest reasonable manner, even though it is being used in conjunction with a detailed description of certain specific examples of the present disclosure. Indeed, certain terms may even be emphasized below; however, any terminology intended to be interpreted in any restricted manner will be overtly and specifically defined as such in this Detailed Description section. For example, in the context of the disclosure, the switching devices may be described as switches or devices, but may refer to any device for controlling the flow of power in an electrical circuit. For example, switches may be metal-oxide-semiconductor field-effect transistors (MOSFETs), bipolar junction transistors (BJTs), insulated-gate bipolar transistors (IGBTs), or relays, for example, or any combination thereof, but are not limited thereto.

[0153] Various embodiments of the present disclosure relate generally to systems and methods for an adaptive driver for an inverter for an electric vehicle, and, more particularly, to systems and methods for an adaptive driver for a power device switch for an inverter for an electric vehicle.

[0154] Inverters, such as those used to drive a motor in an electric vehicle, for example, are responsible for converting High Voltage Direct Current (HVDC) into Alternating Current (AC) to drive the motor. A three phase inverter may include a bridge with six power device switches (for example, power transistors such as IGBT or MOSFET) that are controlled by Pulse Width Modulation (PWM) signals generated by a controller. An inverter may include three half-H bridge switches to control the phase voltage, upper and lower gate drivers to control the switches, a PWM controller, and glue logic between the PWM controller and the gate drivers. The PWM controller may generate signals to define the intended states of the system. The gate drivers may send the signals from the PWM controller to the half-H bridge switches. The half-H bridge switches may drive the phase voltage. The inverter may include an isolation barrier between low voltage and high voltage planes. Signals may pass from the PWM controller to the half-H bridge switches by passing across the isolation barrier, which may employ optical, transformer-based, or capacitance-based isolation. PWM signals may be distorted when passing through the glue logic, which may include resistive, capacitive, or other types of filtering. PWM signals may be distorted when passing through the gate driver, due to the galvanic isolation barrier and other delays within the gate driver. PWM signals may be distorted when the signals processed by the half-H switch via the gate driver output.

[0155] Gate drivers may tolerate common-mode transients that occur during field-effect transistor (FET) switching and when one side of the floating high voltage terminal is shorted to ground or

subject to an electro-static discharge. These voltage transients may result in fast edges which may create bursts of common-mode current through the galvanic isolation. A gate driver may need to demonstrate common-mode transient immunity (CMTI) in order to be effective and safe.

[0156] Gate drivers may have a high-voltage domain in common to the voltage plane of an associated FET. Further, high-voltage planes may be supplied by a flyback converter that may be isolated through a transformer from the low-voltage plane. The high-voltage domain supply may be used to power circuits which source and sink gate current to drive the FET and which may detect FET faults so the faults can be acted upon and/or communicated to the low-voltage domain. Gate drivers may include a galvanic channel dedicated to FET commands, and one or more bidirectional or unidirectional galvanic channels dedicated to FET communications.

[0157] High current switching transients may create strong electro-magnetic (EM) fields that may couple into nearby metal traces. The magnitude and frequency of coupled currents may depend upon the layout of the FET packaging solution and the direction and length of metal traces between the FET and the control integrated circuit (IC). For example, typical values for coupled currents may be up to 1 A at AC frequencies up to 100 MHz. Typically, within a circuit, the gate driver IC may be placed far enough away from the FET that high EM fields do not couple directly into the internal metal traces within the gate driver IC. The gate driver is placed a distance from EM fields such that induced currents within the circuitry are below levels that will cause malfunction of the gate driver, or a metal shield is placed between the gate driver and the source of EM fields to protect the gate driver circuitry. The output terminals of the gate driver that connect to the FET are exposed to the EM fields at the point where the output terminals are no longer covered by a shield. The gate driver switches large currents (such as 5 A to 15 A, for example) through these exposed terminals. The switched large currents are generally greater in magnitude than the EM-induced currents. The gate driver is able to overdrive the induced currents to maintain control of the FETs. The high side of the gate drivers and the FET may share a common ground and a gate control signal trace, both of which may be susceptible to coupled currents.

[0158] Gate drivers may turn on low-resistance switches to source and sink gate currents. Series resistors may sometimes be added to limit gate current. Switched gate currents may be larger than coupled currents in order to maintain control of their respective FETs.

[0159] Gate drivers may be able to sense FET operating voltages or currents in order to provide feedback and react to faults. Over-current faults may typically be detected by sensing the FET drain to source voltage and comparing the sensed voltage to a reference value. Sensed voltages may be heavily filtered to reject coupled currents. Filtering may slow down the response to fault conditions, resulting in delays in response. For example, the rate of current increase due to a low resistance short circuit may reach damaging levels prior to being detected by the heavily filtered drain to source voltage detection strategy. The resulting short circuit may damage the FET or the vehicle, prior to being detected and shut off.

[0160] According to one or more embodiments, a FET driver circuit may provide rapid over-current detection by either shunt current sensing or by diverting a fraction of the load current through a parallel FET that may have a current sensing circuit. Utilizing either strategy may require a “point-of-use IC” where sensing circuitry is in close proximity to the FET. Even if a point-of-use IC and a remote controller are resistant to EM fields, communication between the point-of-use IC and remote controller remains susceptible to induced currents. Point-of-use ICs have been implemented in low EM field applications, such as smart FETs for automotive applications. However, point-of-use ICs have not been used in high EM field applications. A high EM field may be a field (i) that induces a current within an IC that is in excess of an operating current of the IC and leads to malfunction, or (ii) that induces a differential voltage within an IC which is in excess of the operating differential voltage and leads to malfunction. A high EM field may be a field that is greater than approximately 10 A or approximately 100V, for example.

[0161] Half-bridge topology selection for power modules may operate with lower loop inductance,

less ringing, and voltage overshoot than other topologies. Using silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs), results in reduced the switching times relative to, for example, some silicon insulated gate bipolar transistors (Si IGBT), and the reduced inductance of a half bridge module may be pursued to take advantage of that capability.

[0162] Half bridge circuits may be used in power electronics to apply pulse width modulated voltage in controlling the current applied to inductive loads such as motors. In such a circuit, the source and its related circuits may most naturally be on the opposing substrates for the two switches in the half bridge. That is, in a half bridge circuit, the source of the upper switch and drain of the lower switch may share a common connection with the load, and the source and drain may be on opposite sides of a bare die that are used in power applications. For high voltage, dual side cooled applications, the source and the drain may be cooled at their interconnects, through an insulating substrate, with the drain being on one substrate and the source being on the other.

[0163] Each power device in the bridge may have circuits referenced to the source connection. However, having the sources on opposing substrates in a dual side cooled package may cause difficulties for assembly. For example, bottom-up assembly for dual side cooled modules may be compromised, as each substrate and its source referenced circuit must be assembled separately and then brought together. In addition, the die associated with the lowers would be inverted from those of the uppers, but the source and drain interconnects may have different voltage standoff requirements, causing differences at the interconnect, which could cause issues with co-planarity during assembly.

[0164] Such difficulties during assembly may lead to lower yields and higher costs. In addition, some devices may face issues of efficiency related to paths for heat and current.

[0165] FIG. 1 depicts an exemplary system infrastructure for a vehicle including a combined inverter and converter, according to one or more embodiments. In the context of this disclosure, the combined inverter and converter may be referred to as an inverter. As shown in FIG. 1, electric vehicle **100** may include an inverter **110**, a motor **190**, and a battery **195**. The inverter **110** may include components to receive electrical power from an external source and output electrical power to charge battery **195** of electric vehicle **100**. The inverter **110** may convert DC power from battery **195** in electric vehicle **100** to AC power, to drive motor **190** of the electric vehicle **100**, for example, but the embodiments are not limited thereto. The inverter **110** may be bidirectional, and may convert DC power to AC power, or convert AC power to DC power, such as during regenerative braking, for example. Inverter **110** may be a three-phase inverter, a single-phase inverter, or a multi-phase inverter.

[0166] FIG. 2 depicts an exemplary system infrastructure for the inverter **110** of FIG. 1 with a point-of-use switch controller, according to one or more embodiments. Electric vehicle **100** may include inverter **110**, motor **190**, and battery **195**. Inverter **110** may include an inverter controller **300** (shown in FIG. 3) to control the inverter **110**. Inverter **110** may include a low voltage upper phase controller **120** separated from a high voltage upper phase controller **130** by a galvanic isolator **150**, and an upper phase power module **140**. Upper phase power module **140** may include a point-of-use upper phase controller **142** and upper phase switches **144**. Inverter **110** may include a low voltage lower phase controller **125** separated from a high voltage lower phase controller **135** by galvanic isolator **150**, and a lower phase power module **145**. Lower phase power module **145** may include a point-of-use lower phase controller **146** and lower phase switches **148**. Upper phase switches **144** and lower phase switches **148** may be connected to motor **190** and battery **195**.

Galvanic isolator **150** may be one or more of optical, transformer-based, or capacitance-based isolation. Galvanic isolator **150** may be one or more capacitors with a value from approximately 20 fF to approximately 100 fF, with a breakdown voltage from approximately 6 kV to approximately 12 kV, for example. Galvanic isolator **150** may include a pair of capacitors, where one capacitor of the pair carries a complementary data signal from the other capacitor of the pair to create a differential signal for common-mode noise rejection. Galvanic isolator **150** may include more than



one capacitor in series. Galvanic isolator **150** may include one capacitor located on a first IC, or may include a first capacitor located on a first IC and a second capacitor located on a second IC that communicates with the first IC.

[0167] Inverter **110** may include a low voltage area, where voltages are generally less than 5V, for example, and a high voltage area, where voltages may exceed 500V, for example. The low voltage area may be separated from the high voltage area by galvanic isolator **150**. Inverter controller **300** may be in the low voltage area of inverter **110**, and may send signals to and receive signals from low voltage upper phase controller **120**. Low voltage upper phase controller **120** may be in the low voltage area of inverter **110**, and may send signals to and receive signals from high voltage upper phase controller **130**. Low voltage upper phase controller **120** may send signals to and receive signals from low voltage lower phase controller **125**. High voltage upper phase controller **130** may be in the high voltage area of inverter **110**. Accordingly, signals between low voltage upper phase controller **120** and high voltage upper phase controller **130** pass through galvanic isolator **150**. High voltage upper phase controller **130** may send signals to and receive signals from point-of-use upper phase controller **142** in upper phase power module **140**. Point-of-use upper phase controller **142** may send signals to and receive signals from upper phase switches **144**. Upper phase switches **144** may be connected to motor **190** and battery **195**. Upper phase switches **144** and lower phase switches **148** may be used to transfer energy from motor **190** to battery **195**, from battery **195** to motor **190**, from an external source to battery **195**, or from battery **195** to an external source, for example. The lower phase system of inverter **110** may be similar to the upper phase system as described above.

[0168] FIG. **3** depicts an exemplary system infrastructure for inverter controller **300** of FIG. **2**, according to one or more embodiments. Inverter controller **300** may include one or more controllers.

[0169] The inverter controller **300** may include a set of instructions that can be executed to cause the inverter controller **300** to perform any one or more of the methods or computer based functions disclosed herein. The inverter controller **300** may operate as a standalone device or may be connected, e.g., using a network, to other computer systems or peripheral devices.

[0170] In a networked deployment, the inverter controller **300** may operate in the capacity of a server or as a client in a server-client user network environment, or as a peer computer system in a peer-to-peer (or distributed) network environment. The inverter controller **300** can also be implemented as or incorporated into various devices, such as a DC to DC converter, an AC to DC converter, a charger, a DC to AC converter for controlling a motor and providing AC power, a personal computer (PC), a mobile device, a laptop computer, a desktop computer, a communications device, a control system, a web appliance, a network router, switch or bridge, or any other machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. In a particular implementation, the inverter controller **300** can be implemented using electronic devices that provide voice, video, or data communication. Further, while the inverter controller **300** is illustrated as a single system, the term “system” shall also be taken to include any collection of systems or sub-systems that individually or jointly execute a set, or multiple sets, of instructions to perform one or more computer functions.

[0171] As shown in FIG. **3**, the inverter controller **300** may include a processor **302**, e.g., a central processing unit (CPU), a graphics processing unit (GPU), or both. The processor **302** may be a component in a variety of systems. For example, the processor **302** may be part of a standard inverter. The processor **302** may be one or more general processors, digital signal processors, application specific integrated circuits, field programmable gate arrays, servers, networks, digital circuits, analog circuits, combinations thereof, or other now known or later developed devices for analyzing and processing data. The processor **302** may implement a software program, such as code generated manually (i.e., programmed) or automatically.

[0172] The inverter controller **300** may include a memory **304** that can communicate via a bus **308**.

The memory **304** may be a main memory, a static memory, or a dynamic memory. The memory **304** may include, but is not limited to computer readable storage media such as various types of volatile and non-volatile storage media, including but not limited to random access memory, read-only memory, programmable read-only memory, electrically programmable read-only memory, electrically erasable read-only memory, flash memory, magnetic tape or disk, optical media and the like. In one implementation, the memory **304** includes a cache or random-access memory for the processor **302**. In alternative implementations, the memory **304** is separate from the processor **302**, such as a cache memory of a processor, the system memory, or other memory. The memory **304** may be an external storage device or database for storing data. Examples include a hard drive, compact disc (“CD”), digital video disc (“DVD”), memory card, memory stick, floppy disc, universal serial bus (“USB”) memory device, or any other device operative to store data. The memory **304** is operable to store instructions executable by the processor **302**. The functions, acts or tasks illustrated in the figures or described herein may be performed by the processor **302** executing the instructions stored in the memory **304**. The functions, acts or tasks are independent of the particular type of instructions set, storage media, processor or processing strategy and may be performed by software, hardware, integrated circuits, firm-ware, micro-code and the like, operating alone or in combination. Likewise, processing strategies may include multiprocessing, multitasking, parallel processing and the like.

[0173] As shown, the inverter controller **300** may further include and/or interface to a display **310**, such as a liquid crystal display (LCD), an organic light emitting diode (OLED), a flat panel display, a solid-state display, a cathode ray tube (CRT), a projector, a printer or other now known or later developed display device for outputting determined information. The display **310** may act as an interface for the user to see the functioning of the processor **302**, or specifically as an interface with the software stored in the memory **304** or in the drive unit **306**, such as for programming, for example.

[0174] Additionally or alternatively, the inverter controller **300** may include an input device **312** configured to allow a user to interact with any of the components of inverter controller **300**, such as for calibrating or testing, for example. The input device **312** may be a number pad, a keyboard, or a cursor control device, such as a mouse, or a joystick, touch screen display, remote control, or any other device operative to interact with the inverter controller **300**.

[0175] The inverter controller **300** may also or alternatively include drive unit **306** implemented as a disk or optical drive, flash memory, or any medium that is capable of storing, encoding, or carrying a set of instructions for execution by the inverter controller **300**. The drive unit **306** may include a computer-readable medium **322** in which one or more sets of instructions **324**, e.g. software, can be embedded. Further, the instructions **324** may embody one or more of the methods or logic as described herein. The instructions **324** may reside completely or partially within the memory **304** and/or within the processor **302** during execution by the inverter controller **300**. The memory **304** and the processor **302** also may include computer-readable media as discussed above.

[0176] In some systems, a computer-readable medium **322** includes instructions **324** or receives and executes instructions **324** responsive to a propagated signal so that a device connected to a network **370** can communicate voice, video, audio, images, or any other data over the network **370**. Further, the instructions **324** may be transmitted or received over the network **370** via a communication port or interface **320**, and/or using a bus **308**. The communication port or interface **320** may be a part of the processor **302** or may be a separate component. The communication port or interface **320** may be created in software or may be a physical connection in hardware. The communication port or interface **320** may be configured to connect with a network **370**, external media, the display **310**, or any other components in inverter controller **300**, or combinations thereof. The connection with the network **370** may be a physical connection, such as a wired Ethernet connection or may be established wirelessly as discussed below. Likewise, the additional connections with other components of the inverter controller **300** may be physical connections or

may be established wirelessly. The network **370** may alternatively be directly connected to a bus **308**.

[0177] While the computer-readable medium **322** is shown to be a single medium, the term “computer-readable medium” may include a single medium or multiple media, such as a centralized or distributed database, and/or associated caches and servers that store one or more sets of instructions. The term “computer-readable medium” may also include any medium that is capable of storing, encoding, or carrying a set of instructions for execution by a processor or that cause a computer system to perform any one or more of the methods or operations disclosed herein. The computer-readable medium **322** may be non-transitory, and may be tangible.

[0178] The computer-readable medium **322** can include a solid-state memory such as a memory card or other package that houses one or more non-volatile read-only memories. The computer-readable medium **322** can be a random-access memory or other volatile re-writable memory. Additionally or alternatively, the computer-readable medium **322** can include a magneto-optical or optical medium, such as a disk or tapes or other storage device to capture carrier wave signals such as a signal communicated over a transmission medium. A digital file attachment to an e-mail or other self-contained information archive or set of archives may be considered a distribution medium that is a tangible storage medium. Accordingly, the disclosure is considered to include any one or more of a computer-readable medium or a distribution medium and other equivalents and successor media, in which data or instructions may be stored.

[0179] In an alternative implementation, dedicated hardware implementations, such as application specific integrated circuits, programmable logic arrays and other hardware devices, can be constructed to implement one or more of the methods described herein. Applications that may include the apparatus and systems of various implementations can broadly include a variety of electronic and computer systems. One or more implementations described herein may implement functions using two or more specific interconnected hardware modules or devices with related control and data signals that can be communicated between and through the modules, or as portions of an application-specific integrated circuit. Accordingly, the present system encompasses software, firmware, and hardware implementations.

[0180] The inverter controller **300** may be connected to a network **370**. The network **370** may define one or more networks including wired or wireless networks. The wireless network may be a cellular telephone network, an 802.11, 802.16, 802.20, or WiMAX network, for example. Further, such networks may include a public network, such as the Internet, a private network, such as an intranet, or combinations thereof, and may utilize a variety of networking protocols now available or later developed including, but not limited to TCP/IP based networking protocols. The network **370** may include wide area networks (WAN), such as the Internet, local area networks (LAN), campus area networks, metropolitan area networks, a direct connection such as through a Controller Area Network (CAN), FlexRay™, Universal Serial Bus (USB) port, or any other networks that may allow for data communication. The network **370** may be configured to couple one computing device to another computing device to enable communication of data between the devices. The network **370** may generally be enabled to employ any form of machine-readable media for communicating information from one device to another. The network **370** may include communication methods by which information may travel between computing devices. The network **370** may be divided into sub-networks. The sub-networks may allow access to all of the other components connected thereto or the sub-networks may restrict access between the components. The network **370** may be regarded as a public or private network connection and may include, for example, a virtual private network or an encryption or other security mechanism employed over the public Internet, or the like.

[0181] In accordance with various implementations of the present disclosure, the methods described herein may be implemented by software programs executable by a computer system. Further, in an exemplary, non-limited implementation, implementations can include distributed

processing, component or object distributed processing, and parallel processing. Alternatively, virtual computer system processing can be constructed to implement one or more of the methods or functionality as described herein.

[0182] Although the present specification describes components and functions that may be implemented in particular implementations with reference to particular standards and protocols, the disclosure is not limited to such standards and protocols. For example, standards for Internet and other packet switched network transmission (e.g., TCP/IP, UDP/IP, HTML, HTTP) represent examples of the state of the art. Such standards are periodically superseded by faster or more efficient equivalents having essentially the same functions. Accordingly, replacement standards and protocols having the same or similar functions as those disclosed herein are considered equivalents thereof.

[0183] It will be understood that the operations of methods discussed are performed in one embodiment by an appropriate processor (or processors) of a processing (i.e., computer) system executing instructions (computer-readable code) stored in storage. It will also be understood that the disclosure is not limited to any particular implementation or programming technique and that the disclosure may be implemented using any appropriate techniques for implementing the functionality described herein. The disclosure is not limited to any particular programming language or operating system.

[0184] FIG. 4 depicts an exemplary system infrastructure for the point-of-use switch controller of FIG. 2, according to one or more embodiments. For a three-phase inverter, each of the upper phase and the lower phase may include three phases correlating with phases A, B, and C. For example, upper phase power module **140** may include upper phase power module **140A** for upper phase A, upper phase power module **140B** for upper phase B, and upper phase power module **140C** for upper phase C. Upper phase power module **140A** may include point-of-use upper phase A controller **142A** and upper phase A switches **144A**. Upper phase power module **140B** may include point-of-use upper phase B controller **142B** and upper phase B switches **144B**. Upper phase power module **140C** may include point-of-use upper phase C controller **142C** and upper phase C switches **144C**. Each of the upper phase A switches **144A**, upper phase B switches **144B**, and upper phase C switches **144C** may be connected to motor **190** and battery **195**. FIG. 4 depicts details of the upper phase power module **140**. Although not shown, the lower phase power module **145** may include a similar structure as the upper phase power module **140** for lower phases A, B, and C.

[0185] FIG. 5 depicts an exemplary system infrastructure for the upper power module of FIG. 4, according to one or more embodiments. For example, FIG. 5 provides additional details of upper phase power module **140A**. Although not shown, upper phase power module **140B**, upper phase power module **140C**, and respective lower phase power modules of lower phase power module **145** may include a similar structure as the upper phase power module **140A** shown in FIG. 5. Moreover, the terms upper, lower, north, and south used in the disclosure are merely for reference, do not limit the elements to a particular orientation, and are generally interchangeable throughout. For example, the upper phase power module **140** could be referred to a lower phase power module, a north phase power module, a south phase power module, a first phase power module, or a second phase power module.

[0186] Upper phase power module **140A** may include point-of-use upper phase A controller **142A** and upper phase A switches **144A**. Upper phase A switches **144A** may include one or more groups of switches. As shown in FIG. 5, upper phase A switches **144A** may include upper phase A north switches **144A-N** and upper phase A south switches **144A-S**. Point-of-use upper phase A controller **142A** may include one or more memories, controllers, or sensors. For example, point-of-use upper phase A controller **142A** may include a communication manager **405**, a functional safety controller **410**, a testing interface and controller **415**, a north thermal sensor **420A**, a south thermal sensor **420B**, a self-test controller **425**, a command manager **430**, a waveform adjuster **435**, a memory **440**, north switches control and diagnostics controller **450N**, and south switches control and

diagnostics controller **450S**. Point-of-use upper phase A controller **142A** may include more or less components than those shown in FIG. 5. For example, point-of-use upper phase A controller **142A** may include more or less than two switch control and diagnostics controllers, and may include more than two thermal sensors.

[0187] Communication manager **405** may control inter-controller communications to and from point-of-use upper phase A controller **142A** and/or may control intra-controller communications between components of point-of-use upper phase A controller **142A**. Functional safety controller **410** may control safety functions of point-of-use upper phase A controller **142A**. Testing interface and controller **415** may control testing functions of point-of-use upper phase A controller **142A**, such as end-of-line testing in manufacturing, for example. North thermal sensor **420A** may sense a temperature at a first location in point-of-use upper phase A controller **142A**, and south thermal sensor **420B** may sense a temperature at a second location in point-of-use upper phase A controller **142A**. Self-test controller **425** may control a self-test function of point-of-use upper phase A controller **142A**, such as during an initialization of the point-of-use upper phase A controller **142A** following a power on event of inverter **110**, for example. Command manager **430** may control commands received from communication manager **405** issued to the north switches control and diagnostics controller **450N** and south switches control and diagnostics controller **450S**. Waveform adjuster **435** may control a waveform timing and shape of commands received from communication manager **405** issued to the north switches control and diagnostics controller **450N** and south switches control and diagnostics controller **450S**. Memory **440** may include one or more volatile and non-volatile storage media for operation of point-of-use upper phase A controller **142A**. North switches control and diagnostics controller **450N** may send one or more signals to north switches **144A-N** to control an operation of north switches **144A-N**, and may receive one or more signals from north switches **144A-N** that provide information about north switches **144A-N**. South switches control and diagnostics controller **450S** may send one or more signals to south switches **144A-S** to control an operation of south switches **144A-S**, and may receive one or more signals from south switches **144A-S** that provide information about south switches **144A-S**. As stated above, the terms north and south are merely used for reference, and north switches control and diagnostics controller **450N** may send one or more signals to south switches **144A-S**, and south switches control and diagnostics controller **450S** may send one or more signals to north switches **144A-N**.

[0188] FIG. 6 depicts an exemplary electrical schematic for a power module including electrically conductive spacers, according to one or more embodiments. FIG. 7 depicts an exemplary architecture for a power module including electrically conductive spacers, according to one or more embodiments.

[0189] As discussed above, application of half-bridge topology for power modules may present difficulties during assembly, and possibly leading to lower yields and higher costs. In addition, some devices may face issues of efficiency related to paths for heat and current. Power modules according to one or more embodiments may overcome these challenges through use of electrically conductive spacers. The spacers may be formed of copper, for example, or another electrically and/or thermally conductive material. The spacers may provide a connection between a first substrate and a second substrate. A spacer may be 2 mm by 2 mm, for example, and may have a thickness similar to that of a die, such as 180  $\mu\text{m}$ , for example. The spacers may be surface mount components and placed along with SiC MOSFETs using a same process. The spacers may replace wires and clips that some systems may use, and die interconnects may allow the gate, drain, and source to be connected to the same substrate.

[0190] Electrically conductive spacers may be employed in a half-bridge topology for a power module, which may provide for reduced loop inductance in the device. Reduced loop inductance may, in turn, provide less ringing and less voltage overshoot. An application of the device may then speed up the switching time, reduce the power, and may offer more current throughput at a given

price and performance point.

[0191] Electrically conductive spacers may provide a path for current flow from a first substrate to a second substrate, thus allowing source referenced circuits to be assembled to one (e.g., exactly one, only one, or no more than one) substrate. The electrically conductive spacers may be compatible with methods used to make connections to both sides of a die, such as by sinter or solder interconnect, for example. The electrically conductive spacers may thus allow current to flow between the two substrates, as shown in FIG. 6.

[0192] The power flow in a cooled power module **600** according to one or more embodiments is shown in FIG. 6 and FIG. 7 in schematic and planar view, respectively. As shown in the figures, the interconnects **610**, **620**, and **630** may be on a lower or first substrate providing a source plane. Current may, thus, flow along path **660** from the interconnect **610** from the lower (source) substrate to an upper or second substrate providing a drain plane, through electrically conductive spacers **640** and to drains of a first group of parallel SiC MOSFETs (e.g. upper phase switches **144**). The drains of the first group of parallel SiC MOSFETs may be attached to the drain plane on a first side (the left side in FIG. 7) of the upper (drain) substrate. During a first half-cycle, current may be switched (by turning on the first group of parallel SiC MOSFETs) through, drain to source, the first group of parallel SiC MOSFETs to the lower (source) substrate, where the source plane on the first or left side of the lower (source) substrate allows current to flow out of the interconnect **630** to the load, e.g., to motor **190**.

[0193] During the next half cycle, current may flow along path **670** from interconnection **620** and along the source plane on a second side (the right side in FIG. 7) of the lower (source) substrate. The current may be switched (by turning on the first group of parallel SiC MOSFETs) through, source to drain, the second group of parallel SiC MOSFETs to the upper (drain) substrate, through the drain plane on the second or right side of the upper (drain) substrate, and through the electrically conductive spacers **650** to the lower (source) substrate and the load.

[0194] If such a half-bridge arrangement is used in an inverter, the current flow may be in either direction through the devices to the load. That is, current flow may be through path **660** or path **670**, as depicted in FIG. 6.

[0195] FIG. 8 depicts a cross-section view of an exemplary architecture for a power module **800** including electrically conductive spacers **860**, according to one or more embodiments. Power module **800** may be a dual-side-cooled power module according to one or more embodiments is depicted in FIG. 8 in cross-section view.

[0196] A dual-side-cooled power module **800** according to one or more embodiments may provide a high current interconnect between a base substrate and cap substrate for a dual-side-cooled power module. However, while some embodiments herein are referred to as “dual-side cooled”, it is contemplated that the devices disclosed herein may be used in “single-side cooled” applications or combined active/passive cooling configurations. As shown in FIG. 8, upper substrate **805U** and lower substrate **805L**, both of ceramic, e.g., silicon nitride (Si.sub.3N.sub.4) middle layers having thick metallization, e.g., direct bond copper (DBC) or active metal brazing (AMB) **810** that may be employed on an outer surface and an inner surface of the ceramic middle layer. Each of the metallization layers **810** may include multiple conductive regions electrically separated from each other, as shown in FIG. 8. The power module **800** may include a semiconductor (e.g., silicon carbide (SiC)) die **815** that has a drain connection **820** to the upper substrate **805U**. The source connection **830** may be attached to the lower substrate **805L**. A polyimide or flex circuit **835** including a base polyimide material with an internal copper layer **840** may be used, thus making interconnect possible to the gate connection **825** of the SiC MOSFET **815**. Other components depicted in FIG. 8 may include a lead frame connection **845** for the positive supply voltage (from battery **195**, for example), and a lead frame connection **850** for the negative supply voltage. The assembly may be over-molded with a dielectric material **855**. The module may include one or more electrically conductive spacers **860** that provide high current interconnect between an inner surface

of upper substrate **805U** and an inner surface of lower substrate **805L**.

[0197] FIG. **9** depicts a single-sided cooling heat flow in a cross-section view of an exemplary architecture for a power module **800** including electrically conductive spacers, according to one or more embodiments, in cross-section view. As shown in FIG. **9**, the electrically conductive spacers **860** may allow heat to flow between upper substrate **805U** and lower substrate **805L**.

[0198] As shown in FIG. **9**, if the lower substrate **805L** only is used as the thermal sink, the heat from the upper substrate **805U** has a conductive path to an outer surface of the lower substrate **805L** by way of the various electrically conductive spacers **860**, thus reducing the overall thermal impedance. The heat paths from the upper substrate **805U** and SiC MOSFETs **815** to the lower substrate **805L** are shown by the arrows **965** in FIG. **9**.

[0199] A dual-side-cooled power module **800** according to one or more embodiments may include use of electrically conductive spacers **860** in conjunction with a second-level metal, such as polyimide or flex circuit **835**, to achieve a low inductance half H-bridge topology. The configuration of a dual-side-cooled power module **800** according to one or more embodiments, as discussed above, enables the placement of source referenced circuits onto a single substrate (e.g. a first SiC MOSFET **815** with a drain-to-source current path and a second SiC MOSFET **815** with a source-to-drain current path may both be similarly placed, without inversion relative to each other, on a lower substrate serving as a source plane). This configuration, thus, allows for bottom-up assembly and is compatible with Design for Manufacturing (DFM) objectives. Likewise, the electrically conductive spacers **860** used in this configuration enable all module high current interconnects (e.g. lead frame connection **845** for the positive supply voltage and lead frame connection **850** for the negative supply voltage, or interconnects **610**, **620**, and **630**) to be made on one substrate (e.g. lower substrate **805L**), thus improving overall efficiency of the device.

[0200] FIG. **10** depicts an assembly of a power module with devices on two substrates and an assembly of an exemplary power module with devices on a single substrate, according to one or more embodiments. FIG. **10** depicts differences in assembly between a device **1005** and a dual-side-cooled power module **1045** according to one or more embodiments.

[0201] A device **1005** may include components **1040** placed on both a top (top of FIG. **10**) substrate **1010** and a bottom (bottom of FIG. **10**) substrate **1030**, where the assembly includes a drain connection for half the switches and a gate/source connection for half the switches. Compared to the manufacture of the separate components, the blind interconnect of the separate substrates when the top substrate is assembled to the bottom is difficult because the geometry of the interconnects are different. In a device **1005**, all source components may be assembled, half of the components may be placed on each of the two substrates, and the source and gate connections may be made as shown. Next, one substrate may be flipped and the drain connection on the top on one half and the drain connection on the bottom on the other half are then made. Corresponding geometry interconnects must be made with half of the interconnects on the top and half on the bottom. In dual-side-cooled power module **1045**, all the MOSFETs may be facing the same way. The interconnects made while assembling the first substrate may be identical. The second substrate may have no components, and all the interconnects made during the substrate to substrate attachment may be similar. Electrically conductive spacers **860** may provide an electrical connection from one substrate to the other.

[0202] In a device **1005** having components **1040** placed on both a top (top of FIG. **10**) substrate **1010** and a bottom (bottom of FIG. **10**) substrate **1030**, during assembly, the two substrates must be joined, face-to-face, such that necessary electrical connections between the components **1040** on the top substrate **1010** and bottom substrate **1030** are made. For example, connections between gates may be only 1 millimeter by 1 millimeter, requiring precise alignment of the top substrate **1010** and bottom substrate **1030**. Improper registration during assembly may lead to production loss and higher costs. A dual-side-cooled power module **1045** according to one or more embodiments, as depicted in FIG. **10**, may provide all components placed on a single (e.g., exactly

one, only one, or no more than one) substrate, such as top substrate **1050**, for example, thus avoiding issues of improper registration during assembly when the top substrate **1050** is joined with bottom substrate **1060**.

[0203] In addition, the electrically conductive spacers **860** may be both electrically and thermally conductive, thus providing a thermal conduction path from top substrate **1050** to bottom substrate **1060**. Although the thermal path through the electrically conductive spacers **860** may be less efficient than a thermal path directly through each substrate, use of this thermal path through the electrically conductive spacers **860** may enable single sided cooling in lower power applications.

[0204] Further, the electrically conductive spacers **860** used in this configuration may be of small geometry and may use a small amount of extra space in the circuit topology, and may not significantly compromise the drain and source planes, the power module size, or the power module overall loop inductance.

[0205] Accordingly, the use of electrically conductive spacers **860** in a dual-side-cooled power module **800** according to one or more embodiments, as discussed above, may provide advantages in device efficiency without incurring significant compromises.

[0206] FIG. **11** depicts an assembly of an exemplary power module **1110** including a substrate **1140** and a flex layer **1150**, according to one or more embodiments. For dual-side-cooled power module and switch applications desiring a high power density, a second routing layer may be employed such that the gate connection does not interfere with either (a) the current capability of the source connection, or (b) the thermal performance of the substrate in increasing a thermal impedance of the substrate.

[0207] FIG. **11** depicts a layered construction of such a power module according to one or more embodiments. As shown in FIG. **11**, a power module **1110** according to one or more embodiments may include a substrate **1140** and a polyimide flex layer **1150**. The flex layer **1150** may include a second layer of metal including the gate routing **1170**. Openings **1160** may receive gate pads of the die (e.g. lower phase switches **148**). The substrate **1140** may be combined with flex layer **1150** to form a flex on substrate **1180**.

[0208] The flex on substrate **1180** may route the gate connection without compromising the source connection, and may reduce or eliminate cuts in the source plane that may otherwise be needed to route the gate signals. The flex on substrate **1180** may reduce electrical impedance for the source and gate, and may eliminate gate voltage offsets and their effects that may be produced by the impedance in the source path. The flex on substrate **1180** may not compromise the source thermal path as the connections are made through the polyimide.

[0209] FIG. **12** depicts a cross-section view of an exemplary architecture for a power module including a surface mount component, according to one or more embodiments. According to one or more embodiments, a second metal layer may be employed by a power module **1200**. As shown in FIG. **12**, in cross section, the power module **1200** may include upper substrate **1205U** and lower substrate **1205L**, both of ceramic, e.g., silicon nitride (Si.sub.3N.sub.4) having thick metallization, e.g., direct bond copper (DBC) or active metal brazing (AMB) **1210** may be employed. Upper substrate **1205U** and lower substrate **1205L** may be similar to upper substrate **805U** and lower substrate **805L** discussed above. The dual-side-cooled power module **1200** may further include a SiC die **1215** (e.g. upper phase switches **144**) that may have a drain connection **1220** to the upper substrate **1205U**. The source connection **1230** may, as shown in FIG. **12**, be attached to the lower substrate **1205L**. A polyimide or flex circuit, which may include a base polyimide material **1235** with an internal copper layer **1240** and a coverlet **1245**, may provide an interconnect (as shown in FIG. **11**, for example) to the gate **1225** of the SiC MOSFET. The polyimide or flex circuit may further include, for example, a surface mount component **1255** such as, for example, a temperature sensor, thermistor, capacitor, resistor, or another integrated circuit (IC), such as a gate driver, etc. The dual-side-cooled power module **1200** may further include a lead frame connection **1265** for the drain (upper substrate **1205U**) and a lead frame connection **1260** for the source (lower substrate



**1205L**). The assembly may be over-molded with a dielectric material **1270**. The polyimide layer may provide via connections **1275** to the source plane and may also provide a solder stop **1250** for various components.

[0210] Although the use of a polyimide layer is depicted as an example implementation, alternate constructions using printed and fired conductive layers, such as, for example, silver (Ag) alloys, could also be used. A dual-side-cooled power module **1200** according to one or more embodiments may utilize solder interconnection of various components, but other methods of component interconnection, such as sintering, may be used.

[0211] A dual-side-cooled power module **1200** according to one or more embodiments may represent a mixed medium approach to a multilayer board construction, which may be similar in some respects to a rigid flex construction, but with different materials and purpose. For example, a high current, thermally conductive substrate, such as copper bonded DBC or AMB on Si.sub.3N.sub.4, Aluminum Nitride (AlN), Alumina 96% (Al.sub.2O.sub.3) or other ceramic, may be used for thermal performance, and a flex circuit laminated on top of the substrate may be used for low level signal interconnect.

[0212] A dual-side-cooled power module **1200** according to one or more embodiments, also referred to herein as “flex on substrate” (FoS), may allow the full use of the source thermal path by using openings (e.g. openings **1160**) in the dielectric (e.g. flex layer **1150**) to directly make connection to the lower substrate copper. For example, as shown in FIG. **11**, the thin layers of polyimide may route under the die to make the gate connections without interference with the source.

[0213] An FoS construction, according to one or more embodiments, eliminates a need to cut into the source plane with the gate runners, and, thus, may allow for planed copper to be directly connected to the source for low impedance electrical connection. That is, in some embodiments, the source plane or source material of a substrate and of a power module does not include any electrical connections to the gate. Such removal of the cuts in the source plane may further minimize any warpage that might be produced due to unequal copper on front and back of the substrate. Thus, the exposed surface of the source material may be substantially continuous and smooth, without any cuts, indents, recesses, or the like. The absence of cuts can be visualized in substrate **1140** in FIG. **11**.

[0214] In addition, an FoS construction, according to one or more embodiments, may further insulate the gate connection that is routed under the die, across the die edge, where a high standoff may be required due to the presence of drain voltages, and around the perimeter of the die. The presence of the polyimide may increase the dielectric strength at that point, which may reduce an overall thickness of the assembly and the thermal resistance.

[0215] An FoS construction, according to one or more embodiments, may allow circuits, the SiC gate, and other dies to be referenced to the source plane for smaller loop areas. The return path for the generated signals may be returned to the source of the signal along the source plane that exists below the routing path. That is, an FoS construction, according to one or more embodiments, may prevent disruption of the source plane that may cause electromagnetic susceptibility issues in some circuits.

[0216] An FoS construction, according to one or more embodiments, may further allow for greater trace routing density over conventional DBC or AMB designs, which may require signal routing, and which may have lines and space that are limited due to the copper thickness.

[0217] FIG. **13** depicts a cross-section view of an exemplary architecture for a power module **1300** including a shifted substrate, according to one or more embodiments. A dual-side-cooled power module according to one or more embodiments may represent a general methodology and resultant topology shift in maximizing the load current capability of a high current power module used in bridge applications such as a three phase traction inverter, without compromising the dual-side cooling and the overall material thickness within the cooling path.

[0218] The limitations of any semiconductor power switch are based upon allowed temperature rise of the die, the temperature capability of the die attach material, and the temperature of the cooling system. The losses associated with switching the required load current are applied to the conductive thermal impedance, and result in a temperature rise at the junction of the SiC FET/IGBT. This temperature rise is to be constrained and must remain within allowable temperature limitations. Limitations at the high end might be somewhat lower than the maximum die temperature. For example, a module may have transient excursions and temperature sensing accuracy limitations, making the actual junction temperature uncertain, so that power de-rating needs to occur at approximately 25 degrees less than that maximum. Limitations at the low end may be constrained by a 65 C max coolant temperature, but might have a fluid temperature increase within the cooling rails so that 75 C is the lower limit.

[0219] A direct way to widen the limits is to move the upper boundary, as it may not be constrained by a customer requirement, but rather a supplier requirement. For example, some suppliers allow the maximum junction of the die to be increased from 175 C to 185 C, but the die attach and the rest of the thermal stack should be considered.

[0220] Another method of increasing current density is to reduce switching losses. A SiC die is an enabler for reduced switching times. However, improved gate control is necessary to take advantage of the improvement. Improved gate control can reduce switching time, while controlling overshoots with dynamic control of the gate current during the turn-on and turn-off events. Issues with voltage drops across the source plane are inherent at high currents.

[0221] Improved gate control relies on being able to dynamically control the current during turn-on and turn-off and requires a low gate loop inductance. A second metal layer, including a polyimide flex material bonded over the source DBC/AMB copper may be employed by a dual-side-cooled power module according to one or more embodiments, thus enabling a reduced loop area for the gate current and its return current.

[0222] Exposing both the source and drain side of a die to a thermal sink in dual side cooling would ideally halve the thermal impedance. However, with the smaller source surfaces, and the drain side having a larger thermal impedance through the device itself, the thermal impedance may be estimated at six tenths of a design using only drain side cooling, as most power modules do. If the magnitude of a thermal resistance for one path out of a die is the length of that thermal path divided by the material conductivity and area, then the only difference being considered out of a second path for a dual side cooled die may be that the full area is not available because of the gate. If 75% of the area is available, the thermal resistance being  $4/3$  the original thermal resistance results in a parallel combination of the two thermal resistances of  $(4/3)/(1+4/3)$  times the original thermal resistance, or 0.57 of the original single sided thermal resistance. If 50% of the area is available, the thermal resistance being twice the original thermal resistance, then the parallel combination becomes  $(2)/(1+2)$  times the original thermal resistance, or 0.66 the original value, where a best combined resistance is 0.5 the original value.

[0223] A die, being a flattened rectangular solid object, may only have two sides for cooling. Some systems cool the drain side of the die, as there are no obstructions on this side. The source side of the die, however, has some area dedicated to the gate signal and some are for the source. Some systems may routing the gate signals out, while avoiding close proximity to drain voltages and without contacting the source, using a loop of wire from the gate to the drain side substrate. This results in a high current source connection requiring some space to avoid contact with the wire loop. Any component in series with the source to make an electrical connection may increase the thermal resistance of the source connection, and increase the overall thermal impedance. Using wire-bonds and clips interferes with the ability to use dual side cooling. Therefore, embodiments of this disclosure do not use any wire-bonds or clips within the power module. The second metal layer that provides the gate connection must not interfere with the thermal path of the source. If the source attach requires a pedestal to provide clearance for the gate attach, the increased thermal

resistance of this pedestal counters some of the benefit of dual sided cooling.

[0224] A dual-side-cooled power module **1300** according to one or more embodiments may utilize voided areas in the polyimide to enable direct connection of the source to the source plane of the DBC, while the gate layer is connected to the second metal of the polyimide flex circuit. In general, reduction of the power module thickness and the use of materials having higher thermal conductivity also allows current capabilities to be increased. The use of clips and spacers in series with the source and drain connection increases the thermal impedance. Use of channels in the DBC copper to route gate traces increase the warpage of the substrate that needs to be accommodated at some point in the thermal stack.

[0225] A dual-side-cooled power module according to one or more embodiments may increase the upper temperature boundary condition by utilizing SiC MOSFETs with higher junction temperature to increase the upper temperature limit and increase the die size to 5.5 mm×5.5 mm, for example, and modify the thermal stack so the materials do not exceed the specified capability. A dual-side-cooled power module according to one or more embodiments may utilize an internal ASIC for temperature sensing without a custom SiC FET or thermistors. Such a configuration may support temperature sensing of upper and lower phases of a half-H switch without the use of a thermistor, which may have poor accuracy. One or more embodiments may use an ASIC to accurately sense temperature, but the use of thermistors or SiC/IGBT devices with temperature sensing are not precluded.

[0226] A dual-side-cooled power module according to one or more embodiments may reduce switching losses by employing an ASIC for dynamic gate control. The power module may further support multiple pins for gate control. A dual-side-cooled power module according to one or more embodiments may employ a second metal layer for gate routing in order to enable dynamic control of the gate voltage. Such a second metal layer may enable low gate loop inductance, and may enable the source plane to be an efficient signal return path. Polyimide offers very high dielectric breakdown of 200 kV/mm.

[0227] A dual-side-cooled power module according to one or more embodiments may obtain decreased thermal resistance through material thickness reduction and use of high thermal conductivity materials to allow high currents in the switching devices. Polyimide avoids attachment of drain or source connection to anything other than the DBC, and does not require spacers from the source to the surface of the substrate or the use of wire-bonds or clips. Polyimide may reduce or minimize routing on the DBC/AMB substrate to avoid warpage, thus effecting a planar contact to the heat rail.

[0228] As shown in FIG. **13**, dual-side-cooled power module **1300** according to one or more embodiments may include upper substrate **1305U** and lower substrate **1305L**, both of ceramic, e.g., silicon nitride (Si.sub.3N.sub.4) having thick metallization, e.g., direct bond copper (DBC) or active metal brazing (AMB) **1310**. The dual-side-cooled power module **1300** may further include multiple, such as eight, for example SiC dies **1315** that may have a drain connection **1320** to the upper substrate **1305U**. The source connection **1330** may, as shown in FIG. **13**, be attached to the lower substrate **1305L**. A polyimide or flex circuit, which may include a base polyimide layer **1335** with an internal copper layer **1340**, may provide an interconnect to the gates **1325** of the SiC MOSFETs including SiC dies **1315**. The polyimide or flex circuit may further include, for example, a surface mount component such as, for example, a temperature sensor, thermistor, capacitor, resistor, or another integrated circuit (IC) such as a gate driver, etc. The dual-side-cooled power module may further include a lead frame connection **1345** for the drain (on upper substrate **1305U**) and a lead frame connection **1350** for the source (on lower substrate **1305L**). The assembly may be over-molded with a dielectric material **1355**. The polyimide layer **1335** may provide via connections **1360** to the source plane and may also provide solder stops **1365** for various components. As shown in FIG. **13**, upper substrate **1305U** may be offset **1370** from lower substrate **1305L**. Such an offset **1370** may enable the use of thicker lead-frames and higher currents. The

power leads **1345** and **1350** may be sintered, soldered, or ultrasonically welded to dual-side-cooled power module **1300**.

[0229] FIG. **14** depicts an assembly of an exemplary power module **1300** including a shifted substrate, according to one or more embodiments. FIG. **14** depicts various layers of a dual-side-cooled power module **1300** according to one or more embodiments, and an assembly of the layers into a complete device. In FIG. **14**, the reference numbers refer to the same components as depicted in FIG. **13**. Power module **1300** may include solder pre-forms (or in-forms) **1375**. As shown in FIG. **14**, upper substrate **1305U** and lower substrate **1305L** may be individually assembled, and then integrated to form power module **1300**.

[0230] The assembly may include laminating polyimide film onto the source substrate. The polyimide, carrying the second metal, may replace a solder mask on the source substrate. The assembly may include using placed informs rather than a solder print operation, and may provide a consistency in height necessary to reduce a variation in thickness. Placed informs may also allow introduction of a higher temperature solder. The assembly may include an offset substrate requiring different fixturing during over-mold. The offset substrate may allow for a thicker lead frame to be used, which may carry higher currents. The power module **1300** may provide a significant increase in current capability relative to some systems.

[0231] FIG. **15** depicts a cross-section view of an exemplary architecture for a sintered power module including a shifted substrate, according to one or more embodiments. FIG. **15** depicts a cross-section view of a dual-side-cooled power module **1500** according to one or more embodiments using a sintered assembly.

[0232] In contrast to the power module **1300** depicted in FIG. **13**, which uses a soldered assembly, the power module **1500** depicted in FIG. **15** shows a sintered assembly and further includes via **1560** to AMB or DBC copper, one or more sinter preforms **1575**, and sinter film **1580**. Elements common to both power module **1300** and power module **1500** are not re-numbered from FIG. **13**.

[0233] FIGS. **16A** and **16B** depict an assembly of an exemplary sintered power module including a shifted substrate, according to one or more embodiments. FIG. **16A** and FIG. **16B** depict various layers of a dual-side-cooled power module **1500** using a sintered assembly according to one or more embodiments, and an assembly of the layers into a complete device. As shown in FIG. **14**, upper substrate **1305U** and lower substrate **1305L** may be individually assembled, and then integrated to form power module **1500**.

[0234] A sintered power module **1500** may have increased reliability of the interconnect, which may allow the die to maintain higher temperatures for longer periods without inducing creep failure modes. FIG. **16A** and FIG. **16B** depict sintering for both the gate and the source, compared to some systems which may use a wire-bonded gate. FIG. **16B** depicts an opening in the polyimide for both the gate and the source. The gate may be on an island opened on the first metal (substrate). The second metal gate runner carried by the polyimide may make a connection to the island through a via between the first and second metal. The via may provide a substrate height at the interface that is the same between the gate and the source, which may avoid compliancy at the gate pad relative to polyimide being under the gate.

[0235] FIG. **17** depicts a cross-section view of an exemplary architecture for a power module including a point-of-use switch controller, according to one or more embodiments. One or more embodiments may include a power module (e.g. upper phase power module **140** and/or lower phase power module **145**) to accommodate an on-board gate driver (e.g. point-of-use upper phase B controller **142B**), which may also be referred to as a point-of-use switch controller, a point-of-use controller, an internal IC, or an integrated gate driver. A point-of-use controller may improve control of a gate of power device switches (e.g. upper phase B switches **144B**) of the power module. Improved gate control may reduce switching time, while controlling overshoots with dynamic control of the gate current during the turn-on and turn-off events. A gate driver may include multiple individually controlled gate drivers (e.g. north switches control and diagnostics

controller **450N** and south switches control and diagnostics controller **450S**).

[0236] Improved gate control may rely on being able to dynamically control the current to the gate during turn-on and turn-off operations of the power switch, and may require a low gate loop inductance. One or more embodiments may increase the upper temperature boundary condition for the power module. For example, one or more embodiments may use SiC MOSFETs with a higher junction temperature to increase the upper temperature limit. A thermal stack may be configured so the materials do not exceed the specified capability. One or more embodiments may include an internal ASIC (point-of-use controller) for temperature sense without a custom SiC FET or thermistors. Thus, one or more embodiments may support temperature sensing of upper and lower portions of a half-H switch. One or more embodiments may use only a point-of-use controller to accurately sense temperature. One or more embodiments may additionally or alternatively use thermistors or SiC/IGBT devices with temperature sensing functions.

[0237] One or more embodiments may provide a power module that may experience reduced switching losses. One or more embodiments may support multiple pins for gate control.

[0238] FIG. **17** shows a power module **1700** including two stacked substrates including upper substrate **1705U** and lower substrate **1705L**, both of ceramic, e.g., silicon nitride (Si.sub.3N.sub.4) having thick metallization, e.g., direct bond copper (DBC) or active metal brazing (AMB) **1710** may be employed. The power module **1700** may include a semiconductor (e.g., silicon carbide (SiC)) die **1715** that has a drain connection **1720** to the upper substrate **1705U**. The source connection **1730** may be attached to the lower substrate **1705L**. A polyimide or flex circuit **1735** including a base polyimide material with an internal copper layer **1740** may be used, thus making interconnect possible to the gate connection **1725** of the SiC MOSFET and, for example, a surface mount component such as integrated gate driver **1732**. The surface mount component for power module **1700** is not limited to integrated gate driver **1732**, and other components such as temperature sensors, capacitors, or resistors could be surface mount components.

[0239] Power module **1700** may be an implementation of upper phase power module **140** and/or lower phase power module **145**, for example. Integrated gate driver **1732** may be an implementation of point-of-use upper phase A controller **142A**, for example. The SiC MOSFET including SiC die **1715** and gate connection **1725** may be an implementation of upper phase A switches **144A**, for example.

[0240] The integrated gate driver **1732** may also be mounted to the internal copper layer **1740** carried by the polyimide circuit **1735** with solder bumps **1734**. Other items in power module **1700** may include electrically conductive spacers **1760** that provide a high current interconnect between the upper substrate **1705U** and lower substrate **1705L**, the lead frame **1745** connection for the drain of the upper switch (left side SiC die **1715**), and lead frame **1750** connection for the source of the lower switch (right side SiC die **1715**). The assembly may include overmold with a dielectric material **1755**. The polyimide or flex circuit **1735** may provide via connections **1780** to the source plane and solder stop **1782** for various components. The upper substrate **1705U** and lower substrate **1705L** may be offset from each other to enable the use of thicker lead frames to enable conduction of higher currents than typically supported with thin power module designs. The power leads **1745** and **1750** may be sintered, soldered, or ultrasonically welded to power module **1700**.

[0241] Via connections **1780** may be used for current sense. The power module **1700** may incorporate voids in the polyimide or flex circuit **1735** to enhance the epoxy fill beneath the polyimide layer. The power module **1700** may incorporate a second metal layer in polyimide or flex circuit **1735** to allow circuit interconnects without consuming DBC substrate area in order to maintain a minimum form factor.

[0242] Power connections and signal connections are shown to utilize a copper leadframe, but other interconnect methods such as flex circuits are contemplated. One or more embodiments may include a power module **1700** including an on-substrate snubber network and decoupling capacitor.

[0243] FIG. **18** depicts an assembly of an exemplary power module including a point-of-use switch

controller, according to one or more embodiments. FIG. 18 shows a planar view of a possible design using the same numbering scheme as FIG. 17. As shown in FIG. 18, power module 1700 may be assembled by adding layers to a lower substrate 1705L. The second metal layer within the polyimide may provide signal routing as fine lines and spaces that are not possible on the substrate due to the metal thickness. The solder openings may be about 250  $\mu\text{m}$  in diameter. FIG. 18 depicts an array of round openings in the coverlet that provide a solder-stop for the second layer signals. [0244] Other embodiments of the disclosure will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

## Claims

1. A power module, comprising: a first substrate having an outer surface and an inner surface, the first substrate extending in a longitudinal direction from a first longitudinal end toward a second longitudinal end; a semiconductor die coupled to the inner surface of the first substrate; a second substrate having an outer surface and an inner surface, the semiconductor die being coupled to the inner surface of the second substrate, the second substrate extending from a first longitudinal end toward a second longitudinal end; and a first lead frame coupled to the inner surface of the second substrate; wherein the first longitudinal end of the first substrate is longitudinally offset from the first longitudinal end of the second substrate, wherein the second longitudinal end of the first substrate is longitudinally offset from the second longitudinal end of the second substrate, and wherein a distance, at the first lead frame, from the inner surface of the first substrate to the inner surface of the second substrate is less than a thickness of the first lead frame at the inner surface of the second substrate in a direction perpendicular to the longitudinal direction.
2. The power module of claim 1, wherein the longitudinal offset provides a first region on the inner surface of the second substrate for the first lead frame while maintaining a pre-offset distance between the inner surface of the first substrate and the inner surface of the second substrate.
3. The power module of claim 1, wherein a length of the first substrate is approximately equal to a length of the second substrate.
4. The power module of claim 1, wherein a length of the second substrate is greater than a length of the first substrate.
5. The power module of claim 2, further including a second lead frame coupled to the inner surface of the second substrate.
6. The power module of claim 5, wherein the distance is less than a thickness of the second lead frame at the inner surface of the second substrate in a direction perpendicular to the longitudinal direction.
7. The power module of claim 5, wherein the longitudinal offset provides a second region on the inner surface of the second substrate for the second lead frame while maintaining a pre-offset distance between the inner surface of the first substrate and the inner surface of the second substrate.
8. The power module of claim 1, wherein the first lead frame has a thickness greater than 500 microns.
9. The power module of claim 1, wherein the first lead frame has a thickness greater than 700 microns.
10. The power module of claim 1, wherein the first lead frame has a thickness greater than a space between the inner surface of the first substrate and the inner surface of the second substrate.
11. The power module of claim 1, further including an overmold coupled to the first substrate, the second substrate, and the semiconductor die.
12. An inverter comprising the power module of claim 1.

**13.** A vehicle comprising the inverter of claim 12.

**14.** A power module, comprising: a first substrate having an outer surface and an inner surface, the first substrate extending from a first longitudinal end toward a second longitudinal end; a semiconductor die coupled to the inner surface of the first substrate; a second substrate having an outer surface and an inner surface, the semiconductor die being coupled to the inner surface of the second substrate, the second substrate extending from a first longitudinal end toward a second longitudinal end; and a lead frame coupled to the inner surface of the first substrate, wherein a thickness of the lead frame is greater than a distance from the inner surface of the first substrate to the inner surface of the second substrate.

**15.** A system comprising: an inverter configured to convert DC power from a battery to AC power to drive a motor, wherein the inverter includes: a power module including: a lower substrate including a lower conductive layer extending in a lower plane; and an upper substrate including an upper conductive layer extending in an upper plane separated from the lower plane, wherein an end of the upper substrate is offset in the upper plane from a corresponding end of the lower substrate so that a normal vector from the upper plane at the end of the upper substrate does not intersect the lower substrate.

**16.** The system of claim 15, further comprising: a first lead frame connected to the lower conductive layer, wherein at least a portion of the first lead frame is in the upper plane; and a second lead frame connected to the upper conductive layer, wherein at least a portion of the second lead frame is in the lower plane.

**17.** The system of claim 16, wherein one or more of the first lead frame or the second lead frame has a thickness greater than 500 microns.

**18.** The system of claim 17, wherein a distance between an inner surface of the upper substrate and an inner surface of the lower substrate is less than 500 microns.

**19.** The system of claim 15, wherein a length of the lower substrate is approximately equal to a length of the upper substrate.

**20.** The system of claim 15, further comprising: the battery configured to supply the DC power to the inverter; and the motor configured to receive the AC power from the inverter to drive the motor.

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