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Through-substrate vias with improved connections

Abstract

A device includes a substrate, and a plurality of dielectric layers over the substrate. A plurality of metallization layers is formed in the plurality of dielectric layers, wherein at least one of the plurality of metallization layers comprises a metal pad. A through-substrate via (TSV) extends from the top level of the plurality of the dielectric layers to a bottom surface of the substrate. A deep conductive via extends from the top level of the plurality of dielectric layers to land on the metal pad. A metal line is formed over the top level of the plurality of dielectric layers and interconnecting the TSV and the deep conductive via.

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Background/Summary

PRIORITY CLAIM (1) This application is a continuation of U.S. patent application Ser. No. 16/459,387, filed on Jul. 1, 2019 and entitled “Through-Substrate Vias with Improved Connections,” which is a continuation U.S. patent application Ser. No. 15/645,928, filed on Jul. 10, 2017, now U.S. Pat. No. 10,340,205 issued on Jul. 2, 2019, and entitled “Through-Substrate Vias with Improved Connections,” which is a divisional of U.S. patent application Ser. No. 15/056,935, filed on Feb. 29, 2016, now U.S. Pat. No. 9,704,783 issued on Jul. 11, 2017, and entitled “Through-Substrate Vias with Improved Connections,” which application claims the benefit to and is a continuation of U.S. patent application Ser. No. 12/769,251, filed on Apr. 28, 2010, now U.S. Pat. No. 9,293,366 issued on Mar. 22, 2016, and entitled “Through-Substrate Vias with Improved Connections” which applications are incorporated herein by reference.

TECHNICAL FIELD

(1) This disclosure relates generally to integrated circuit structures, and more particularly to forming through-substrate vias with improved electrical connections.

BACKGROUND

(2) Among the efforts for reducing the size of integrated circuits and reducing RC delay, three-dimensional integrated circuit (3DIC) and stacked dies are commonly used. Through-substrate vias (TSVs) are thus used in 3DIC and stacked dies. In this case, TSVs are often used to connect the integrated circuits on a die to the backside of the die. In addition, TSVs are also used to provide short grounding paths for grounding the integrated circuits through the backside of the die, which may be covered by a grounded metallic film.

(3) There are two commonly used approaches for forming TSVs, via-first approach and via-last approach. When formed using the via-first approach, vias are formed before the back-end-of-line (BEOL) processes are performed. Accordingly, the TSVs are formed before the formation of metallization layers. Due to the thermal budget in the BEOL processes, however, the TSVs formed using the via-first approach suffer from problems such as copper popping and metal-1 to metal-2 bridging.

(4) On the other hand, the via-last approach, although being cost effective and having a short time-to-market, the resulting structures are less efficient in power connection. For example, FIGS. **1** and **2** illustrate two interconnect structures comprising via-last TSVs. In FIG. **1**, die **4** is bonded to die **2** through a face-to-face bonding. In FIG. **2**, die **4** is bonded to die **2** through a face-to-back bonding. TSVs **6** are formed in dies **2**, and are used for connecting power to the devices in dies **2**. It is observed that regardless whether the power is introduced into die **2** from bump **12** as in FIG. **1**, or introduced into die **2** from die **4** as in FIG. **2**, the connection of the power to device **8** in dies **4** have long paths, as illustrated by arrows **14**. Further, each of the long power paths **14** includes a plurality of metal lines and vias. Accordingly, the resistances of the power paths are also high.

SUMMARY
(5) In accordance with one aspect, a device includes a substrate, and an interconnect structure over the substrate. The interconnect structure includes a plurality of metallization layers including a bottom metallization layer (M**1**) and a top metallization layer (Mtop). A dielectric layer is over the Mtop. A through-substrate via (TSV) is formed to extend from a top surface of the dielectric layer to a bottom surface of the substrate. A deep conductive via is formed to extend from the top surface of the dielectric layer to land on a metal pad in one of the plurality of metallization layers. A metal line is over the dielectric layer and interconnects the TSV and the deep conductive via.
(6) Other embodiments are also disclosed.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
(1) For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:
(2) FIGS. **1** and **2** illustrate conventional connections of power into dies through through-substrate vias (TSVs);
(3) FIGS. **3** through **9** and **9**B are cross-sectional views of intermediate stages in the manufacturing of a wafer comprising a TSV and deep conductive vias connected to the TSV in accordance with various embodiments; and
(4) FIG. **10** illustrates a wafer comprising a TSV and deep conductive vias, wherein a metal line connecting the TSV and the deep conductive vias is formed in a process step separated from the process step for forming the TSV and the deep conductive via.
(5) FIG. **11** illustrates a wafer comprising a TSV and deep conductive vias, wherein the TSV extends through a substrate that is substantially free from an integrated circuit device.
DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS
(6) The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments provide many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative, and do not limit the scope of the disclosure.
(7) A novel method for forming through-silicon vias (TSVs, also sometimes known as through-silicon vias when they are formed in a silicon substrate) is provided. The intermediate stages of manufacturing an embodiment are illustrated. The variations of the embodiment are then discussed. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.
(8) Referring to FIG. **3**, wafer **20**, which includes substrate **22** and integrated circuits **24** (symbolized by a transistor) therein, is provided. In accordance with various embodiments, wafer **20** is a device wafer comprising active integrated circuit devices such as transistors. Substrate **22** may be a semiconductor substrate, such as a bulk silicon substrate, although it may be formed of other semiconductor materials such as silicon germanium, gallium arsenide, and/or the like. Semiconductor devices such as transistors (a symbolized by transistor **24**) may be formed at the front surface **22***a* of substrate **22**. Interconnect structure **26** is formed on the front side of substrate **22**. Interconnect structure **26** may include inter-layer dielectric (ILD) **28** (in which the electrodes of transistor is located) and contact plugs **30** in ILD **28**, wherein contact plugs **30** may be formed of tungsten or other metallic materials.
(9) Furthermore, interconnect structure **26** include inter-metal dielectrics (IMDs) **34**, and metal lines/pads **38** (including **38**A and **38**B) and vias **40** in IMDs **34**. IMDs **34** may be formed of low-k dielectric materials having low k values, for example, lower than about 2.5, or even lower than

about 2.0. Interconnect structure **26** may include a bottom metallization layer (commonly known as M**1**) and a top metallization layer (commonly known as Mtop), and a plurality of metallization layers therebetween, including the metallization layer (M**2**) immediately over M**1**, the metallization layer (M**3**) immediately over M**2**, and the like. The metal features in interconnect structure **26** may be electrically coupled to semiconductor devices **24**. Metal lines/pad **38** and vias **40** may be formed of copper or copper alloys, and may be formed using the well-known damascene processes. Metal lines/pads **38** include metal lines **38**A and metal pads **38**B, with metal pads **38**B being used for landing the subsequently formed deep vias.

(10) Interconnect structure **26** may further include one or more passivation layer(s) **47** that is immediately over metallization layer Mtop. Passivation layer **47** may be a non-low-k dielectric layer, and may be formed of silicon oxide, silicon nitride, un-doped silicate glass, polyimide, or the like. Further, additional metal lines/pads and vias (not shown) may be formed in passivation layer(s) **47**.

(11) In alternative embodiments, such as in the example of FIG. **11**, wafer **20** is an interposer wafer, and is substantially free from integrated circuit devices, including active devices such as transistors and diodes formed therein. In these embodiments, substrate **22** may be formed of a semiconductor material or a dielectric material. The dielectric material may be silicon oxide, an organic material such as polyimide, a hybrid material such as molding compound, glass, or the like. Furthermore, interposer wafer **20** may include, or may be free from, passive devices such as capacitors, resistors, inductors, varactors, and/or the like.

(12) Referring to FIG. **4**, after the formation of interconnect structure **26**, which may or may not include layer(s) **47**, TSV opening **44** and deep via openings **46** (including **46**A, **46**B, **46**C, **46**D, and possibly more that are not illustrated) are formed. In an embodiment, photo resist **50** is formed and patterned. TSV opening **44** and deep via openings **46** are then formed simultaneously by etching. TSV opening **44** extends into substrate **22**, while deep via openings **46** stop at respective metal pads **38**B, with metal pads **38**B exposed through deep vias **46**. Further, the formation of deep via openings **46** may stop at metal pads **38**B in any one of different metallization layers ranging from M**1** through Mtop in any desirable combination.

(13) In an embodiment, pattern loading effect is used to form TSV opening **44** and deep vias openings **46**, which have different depths, simultaneously. It is observed that when certain via openings are formed, the via openings having greater horizontal sizes may have greater depths than the via openings having smaller sizes, even if they are formed by a same etching process. As a result of the pattern loading effect in the etching process, and also due to the size difference between TSV opening **44** and deep via openings **46**, the resulting TSV opening **44** and deep via openings **46** will have different depths. With properly adjusted horizontal sizes W**1** through W**5**, when the desirable depth D**1** of TSV opening **44** is reached, desirable depths D**2**, D**3**, D**4**, D**5**, and the like are also reached. This may reduce the undesirable over-etching of metal pads **38**B, and hence the undesirable damage to metal pads **38**B may be minimized. Accordingly, the horizontal dimension W**1** (which may be a diameter or a length/width, depending on the shape of TSV opening **44**) of TSV opening **44** is greater than horizontal dimensions W**2**, W**3**, W**4**, and W**5** of deep via openings **46**. In an embodiment, a ratio of W**1**/W**2** (or W**1**/W**3**, W**1**/W**4**, and so on) may be greater than about 1.5, greater than about 5, or even greater than about 100. Further, depth D**1** of TSV opening **44** is greater than depth D**2** of deep via openings **46**. In an embodiment, a ratio of D**1**/D**2** (or D**1**/D**3**, D**1**/D**4**, and so on) may be greater than about 5, or even greater than about 5,000. Further, in the illustrated embodiments, W**2** may be greater than W**3** with ratio W**2**/W**3** being greater than about 1.2, W**3** may be greater than W**4** with ratio W**3**/W**4** being greater than about 1.2, and W**4** may be greater than W**5** with ratio W**4**/W**5** being greater than about 1.2.

(14) Referring to FIG. **5**, insulation layer **52** is formed and patterned, and metal pads **38**B are exposed through the openings in insulation layer **52**. Next, diffusion barrier layer **54**, also referred to as a glue layer, is blanket formed, covering the sidewalls and the bottom of TSV opening **44**.

Diffusion barrier layer **54** may include commonly used barrier materials such as titanium, titanium nitride, tantalum, tantalum nitride, and combinations thereof, and can be formed using physical vapor deposition, for example. Next, a thin seed layer (not shown) may be blanket formed on diffusion barrier layer **54**. The materials of the seed layer may include copper or copper alloys, and metals such as silver, gold, aluminum, and combinations thereof may also be included. In an embodiment, the seed layer is formed of sputtering. In other embodiments, other commonly used methods such as electro or electroless plating may be used.

(15) Referring to FIG. **6**, mask **56** is formed on the previously formed structure. In an embodiment, mask **56** comprises a photo resist, for example. Mask **56** is then patterned. In an exemplary embodiment, the resulting TSV needs to be connected to metal pads **38**B. Accordingly, opening **58** is formed in mask **56**, exposing TSV opening **44** and deep via openings **46**.

(16) In FIG. **7**, a metallic material is filled into openings **44**, **46**, and **58**, forming TSV **60** in TSV opening **44**, deep conductive vias **62** in deep via openings **46**, and metal line **66** in the opening **58**. In various embodiments, the filling material includes copper or copper alloys, although other metals, such as aluminum, silver, gold, and combinations thereof, may also be used. The formation methods may include printing, electro plating, electroless plating, and the like. In the same deposition process in which TSV opening **44** is filled with the metallic material, the same metallic material may also be filled in opening **58**, forming metal line **66**, which is also referred to a redistribution line.

(17) Next, as is shown in FIG. **8**, mask **56** is removed. Passivation layer(s) **72** and Under-bump metallurgy (UBM) **74** may then be formed, as shown in FIG. **9**. Metal bump **76** is also formed. Metal bump **76** may be a solder bump, a copper bump, and may include other layers/materials such as nickel, gold, solder, and/or the like.

(18) After the formation of Metal bump **76**, the backside of wafer **20** may be grinded, so that TSV **60** is exposed. A backside interconnect structure, which may include UBM **78** and bond pad/metal bump **80**, is then formed on the backside of wafer **20**. Further, a backside interconnect structure including a plurality of redistribution layers may be formed between, and electrically coupling, TSV **60** and metal bump **80**, as shown by redistribution layers **71** illustrated in FIG. **9**B.

(19) FIG. **10** illustrates an alternative embodiment. This embodiment is essentially the same as the embodiment shown in FIG. **9**, except that metal line **66** is not formed in the same process as forming TSV **60** and deep vias **62**. In the respect formation process, after the formation of the structure shown in FIG. **5**, TSV opening **44** and deep via openings **46** are filled, followed by a planarization process such as a chemical mechanical polish (CMP) to remove excess metal, and hence TSV **60** and deep vias **62** are formed. However, after the CMP, TSV **60** and deep vias **62** are electrically disconnected from each other. Next, metal line **66** is formed to electrically couple TSV **60** to deep vias **62**. In the resulting structure, diffusion barrier layer **67** separates TSV **60** and deep vias **62** from metal line **66**. Diffusion barrier layer **67** may comprise titanium, titanium nitride, tantalum, tantalum nitride, or the like. In the structure shown in FIG. **9**, however, no diffusion barrier layer is formed to separate TSV **60** and deep vias **62** from metal line **66**.

(20) Although in the illustrated figures, device dies including semiconductor devices are used as examples, the teaching provided by the embodiments may be readily applied to interposers comprising no integrated circuits such as transistors, resistors, diodes, capacitors, and/or the like. Similarly, by using the embodiments, deep vias can be formed on interconnect structures on either one, or both, of the front-side interconnect structure and backside interconnect structure, with the deep vias connected to TSVs in interposers.

(21) In the embodiments, with the formation of deep vias **62**, the power (or signal) introduced to TSV **60** may be provided to metal pads **38**B through deep vias **62** that have different lengths. Compared to conventional via-last structures, the paths to metal features that are on different metallization layers are significantly shortened. As a result, the power connection efficiency is improved.

(22) In some aspects, embodiments described herein provide for a method of manufacturing a device that includes etching a first opening in a dielectric structure, the dielectric structure comprising a plurality of metallization layers formed in a plurality of respective dielectric layers, wherein the first opening exposes a metal pad disposed in at least one of the plurality of dielectric layers. The method also includes etching a second opening through the dielectric structure and into a portion of a substrate disposed below the dielectric structure, wherein the etching the first opening and the etching the second opening occur simultaneously, and simultaneously filling the first opening and the second opening with a conductive material.
(23) In other aspects, embodiments described herein provide for a method of manufacturing a device including forming a interconnect structure over a substrate, the interconnect structure including a plurality of conductive pads formed in respective dielectric layers of a plurality of dielectric layers. The method also includes etching a first opening aligned with a first conductive pad, the first opening having a first width, and simultaneously with etching the first opening, etching a second opening that extends at least partially through the substrate, the second opening have a second width greater than the first width. The method also includes simultaneously forming a first conductive via in the first opening and a second conductive via in the second opening.
(24) In yet other aspects, embodiments described herein may provide for a device comprising a substrate and an interconnect structure over the substrate. The interconnect structure comprises a plurality of low-k dielectric layers, and a plurality of metallization layers in the plurality of low-k dielectric layers and comprising metal pads, wherein the metal pads comprises copper, and a dielectric layer over the plurality of metallization layers, wherein a k value of the dielectric layer is higher than k values of the plurality of low-k dielectric layers. The device further includes a through-substrate via (TSV) extending from a top surface of the dielectric layer to a bottom surface of the substrate, a first deep conductive via extending from the top surface of the dielectric layer to land on a first metal pad in a first one of the plurality of metallization layers, and a second deep conductive via extending from the top surface of the dielectric layer to land on a second metal pad in a second one of the plurality of metallization layers different from the first one. A metal line is over the dielectric layer and electrically couples the TSV to the first and the second deep conductive vias.
(25) One general aspect of embodiments disclosed herein includes a device including: a substrate; an interconnect structure over the substrate, the interconnect structure including: a plurality of low-k dielectric layers; a plurality of metallization layers in the plurality of low-k dielectric layers and including metal pads, where the metal pads includes copper; and a dielectric layer over the plurality of metallization layers, where a k value of the dielectric layer is higher than k values of the plurality of low-k dielectric layers; a through-substrate via (TSV) extending from a top surface of the dielectric layer to a bottom surface of the substrate; a first deep conductive via extending from the top surface of the dielectric layer to land on a first metal pad in a first one of the plurality of metallization layers; a second deep conductive via extending from the top surface of the dielectric layer to land on a second metal pad in a second one of the plurality of metallization layers different from the first one; and a metal line over the dielectric layer and electrically coupling the TSV to the first and the second deep conductive vias.
(26) Another general aspect of embodiments disclosed herein includes a device including: a substrate; an interconnect structure on the substrate, the interconnect structure including stacked metallization layers; a dielectric layer over the stacked metallization layers; a first conductive via extending from a top surface of the dielectric layer to at least partially into the substrate; a second conductive via extending from the top surface of the dielectric layer to a metal pad of the interconnect structure; and a single continuous metal feature filling the first conductive via, extending over the top surface of the dielectric layer, and filling the conductive second via.
(27) Yet another general aspect of embodiments disclosed herein includes a device including: a substrate, an interconnect structure over the substrate, a through-substrate via (TSV) extending

from the top level of the interconnect structure to a bottom surface of the substrate, a deep conductive via extending from the top level of the interconnect structure and contacting a metal pad in the interconnect structure, a barrier layer extending between the deep conductive via and the interconnect structure, a metal line over the top level of the interconnect structure extending continuously from the TSV to the deep conductive via, and a passivation layer over the metal line.

(28) One general aspect of embodiments disclosed herein includes a device including: a substrate; an interconnect structure over the substrate, the interconnect structure including a stacked plurality of metal layers, the interconnect structure having a topmost metal layer surface; and a dielectric layer over the topmost metal layer surface, where a k value of the dielectric layer is higher than k values of the plurality of low-k dielectric layers; a through-substrate via (TSV) extending through the dielectric layer and into the substrate; a first conductive via extending through the dielectric layer and terminating on a first layer of the stacked plurality of metal layers; a second conductive via extending through the dielectric layer and terminating on a second metal layer of the stacked plurality of metal layers different from the first layer of the stacked plurality of metal layers; and a conductor above the interconnect structure and electrically coupling the TSV to the first and the second conductive vias.

(29) Another general aspect of embodiments disclosed herein includes a device including: a substrate; an interconnect structure over the substrate, the interconnect structure including: a plurality of metallization layers including: a bottom metallization layer (M**1**); an intermediate metallization layer (M**2**) over the m**1** layer; a second metallization layer (M**3**) over the m**2**; and a top metallization layer (Mtop) over the M**2**; and a through-substrate via (TSV) extending from the Mtop to a bottom surface of the substrate; a first conductive via extending from a top surface of the Mtop through at least a bottom surface of the Mtop and physically and electrically contacting the m**2**; a second conductive via extending from a top surface of the Mtop through at least a bottom surface of the Mtop and physically and electrically contacting the m**3**; and a metal line electrically connecting the TSV and one of the first conductive via and the second conductive via.

(30) Yet another general aspect of embodiments disclosed herein includes a device including: a plurality of dielectric layers; a plurality of metallization layers formed respectively in the plurality of dielectric layers; a first conductive via extending from the top level of the plurality of dielectric layers and physically and electrically connecting with a first metallization layer of the plurality of metallization layers; a second conductive via extending from the top level of the plurality of dielectric layers and physically and electrically connecting with a second metallization layer of the plurality of metallization layers, the second metallization layer being above the first metallization layer; a metal line over the top level of the plurality of dielectric layers, the metal line electrically connecting the first conductive via to a through-substrate via (TSV); and a passivation layer covering the metal line.

(31) Notwithstanding the foregoing, embodiments described herein may include but are not limited to a method including providing a substrate having first and second surfaces, where the substrate is defined with a device region and a frame region. The method also includes forming at least one through silicon via (TSV) opening and a trench in the substrate, where the trench extends from the first surface of the substrate to a depth shallower than a depth of the TSV opening. The method also includes providing a dielectric liner layer over the substrate, where the dielectric liner layer lines sidewalls of the TSV opening and sidewalls of the trench. The method also includes providing a conductive layer over the substrate, where the conductive layer fills at least the TSV opening to form a TSV contact.

(32) The disclosures provided herein will inform one skilled in the art of, e.g. a method including providing a substrate having first and second surfaces, where the substrate is defined with a device region and a frame region adjacent the device region. The method also includes forming at least one through silicon via (TSV) opening in the substrate, where the TSV opening extends through the first and second surfaces of the substrate. The method also includes forming a trench in the

substrate, where the trench extends from the first surface of the substrate to a depth shallower than a depth of the TSV opening. The method also includes providing a dielectric liner layer over the substrate, where the dielectric liner layer lines sidewalls of the TSV opening. The method also includes providing a conductive layer over the substrate, where the conductive layer fills at least the TSV opening to form TSV. The method also includes and forming a redistribution layer (RDL) over the substrate.

(33) One manner of characterizing some but not all of the embodiments described, disclosed, and/or taught herein is that of a method including providing a substrate having first and second surfaces, where the substrate is defined with a device region and a frame region adjacent the device region. The method also includes forming at least one through silicon via (TSV) opening and an trench, where the trench extends from the first surface of the substrate into the substrate to a depth shallower than a depth of the TSV opening. The method also includes providing a dielectric liner layer over the substrate, where the dielectric liner layer is a continuous layer which extends over the first surface of the substrate and at least lines sidewalls of the TSV opening and sidewalls of the trench. The method also includes providing a conductive layer over the substrate, where the conductive layer fills at least the TSV opening to form a TSV contact. The method also includes and processing the conductive layer to form the TSV contact such that a top surface of the TSV contact is about coplanar with a top surface of the portion of the dielectric liner layer which extends over the first surface of the substrate.

(34) Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

Claims

1. A method for forming a device comprising: providing a structure having first and second surfaces, wherein the structure includes a plurality of metallization layers respectively contained within respective ones of a plurality of dielectric layers; forming a through silicon via (TSV) opening, a first deep via opening extending to a first metal line located in one layer of the plurality of metallization layers, a second deep via opening to a second metal line located in a different layer of the plurality of metal layers and laterally displaced from the first metal line, and a trench in the structure, wherein the trench extends from the first surface of the structure to a depth shallower than a depth of the TSV opening, and further wherein the TSV opening, the first deep via opening, and the second deep via opening are etched into the structure at the same time; providing a dielectric liner layer over the structure, wherein the dielectric liner layer lines sidewalls of the TSV opening and sidewalls of the trench; and providing a conductive layer over the structure to form a continuous structure, wherein the conductive layer fills at least the TSV opening to form a TSV, and wherein the continuous conductive structure electrically connects the first metal line to the second metal line.

2. The method of claim 1, wherein subsequent to the step of forming a trench, another feature is

formed aligned to the trench.
3. The method of claim 1, further comprising planarizing the TSV.
4. The method of claim 1 wherein the metal line is laterally displaced from the TSV and from another metal line in a direction that is parallel to a major surface of the structure.
5. The method of claim 1 further comprising forming a re-distribution layer (RDL) over the structure, wherein a bottom RDL level of the RDL electrically connects the TSV to a connector.
6. The method of claim 1 wherein the step of providing a dielectric liner layer over the structure includes forming a continuous layer which at least lines sidewalls of the TSV opening and extends over the first surface of the structure and sidewalls of the trench.
7. The method of claim 1 further comprising processing the conductive layer to form the TSV such that a top surface of the TSV is about coplanar with a top surface of the portion of the dielectric liner layer which extends over the first surface of the structure.
8. The method of claim 5 wherein a portion of the RDL overlaps the trench and is in contact with a portion of the dielectric liner.
9. A method for forming a device comprising: providing a structure having first and second surfaces, the structure further having multiple layers of interconnections; simultaneously forming a through silicon via (TSV) opening extending from the first surface to a first depth into the structure, a first deep via opening extending from the first surface to a second depth less than the first depth into the structure, and a second deep via opening extending from the first surface to a third depth less than the second depth into in the structure; forming a trench in the structure, wherein the trench extends starting from the first surface of the structure to a depth shallower than the first depth of the TSV opening; providing a dielectric liner layer over the structure, wherein the dielectric liner layer lines sidewalls of the TSV opening; providing a conductive layer over the structure, wherein the conductive layer fills at least the TSV opening to form a TSV, and wherein the conductive layer further provides a conductive path extending vertically from a first interconnection layer of the multiple layers of interconnections to a second, different layer of the multiple layers of interconnections; and forming a redistribution layer (RDL) over the structure.
10. The method of claim 9 wherein the step of providing a dielectric liner layer over the structure includes forming a continuous layer which lines sidewalls of the TSV opening, extends over the first surface of the structure, and lines sidewalls of the trench.
11. The method of claim 9 wherein the conductive layer further provides a conductive path extending horizontally from the first interconnection layer to the second layer.
12. The method of claim 9 further including processing the conductive layer to form a TSV contact such that a top surface of the TSV contact is about coplanar with a top surface of the portion of the dielectric liner layer which extends over the first surface of the structure.
13. The method of claim 9 wherein the at least one TSV opening and the trench are formed simultaneously in the structure.
14. The method of claim 9 wherein the dielectric liner layer is provided to simultaneously line the sidewalls of the TSV opening and sidewalls of the trench.
15. The method of claim 9 wherein subsequent to the step of forming a trench, another feature is formed aligned to the trench.
16. A method for forming a device comprising: providing a structure having first and second surfaces; simultaneously forming at least one through silicon via (TSV) opening, a first deep via opening, a second deep via opening, and a trench, wherein the trench extends from the first surface of the structure into the structure to a first depth shallower than a depth of the TSV opening, further wherein the first deep via opening extends from the first surface of the structure into the structure to a second depth greater than the first depth, and further wherein the second deep via opening extends from the first surface of the structure into the structure to a third depth greater than the second depth; providing a dielectric liner layer over the structure, wherein the dielectric liner layer is a continuous layer which extends over the first surface of the structure and at least lines sidewalls

of the TSV opening and sidewalls of the trench; providing a conductive layer over the structure, wherein the conductive layer fills at least the TSV opening to form TSV contact, and wherein the conductive layer connects a first metal line located in a first metal layer of the structure to a second metal line located in a second metal layer above the first metal layer of the structure; and processing the conductive layer to form the TSV contact and a conductive interconnect, such that a top surface of the TSV contact is about coplanar with a top surface of the portion of the dielectric liner layer which extends over the first surface of the structure.

17. The method of claim 16 wherein the conductive layer fills the trench to form a conductive via.

18. The method of claim 17, wherein subsequent to the step of forming the conductive via, another feature is formed aligned to the conductive via.

19. The method of claim 18, wherein the another features is a redistribution line.

20. The method of claim 16, wherein the second metal line is laterally displaced from the first metal line.