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(54) **METHOD OF MANUFACTURING SEMICONDUCTOR PACKAGE**

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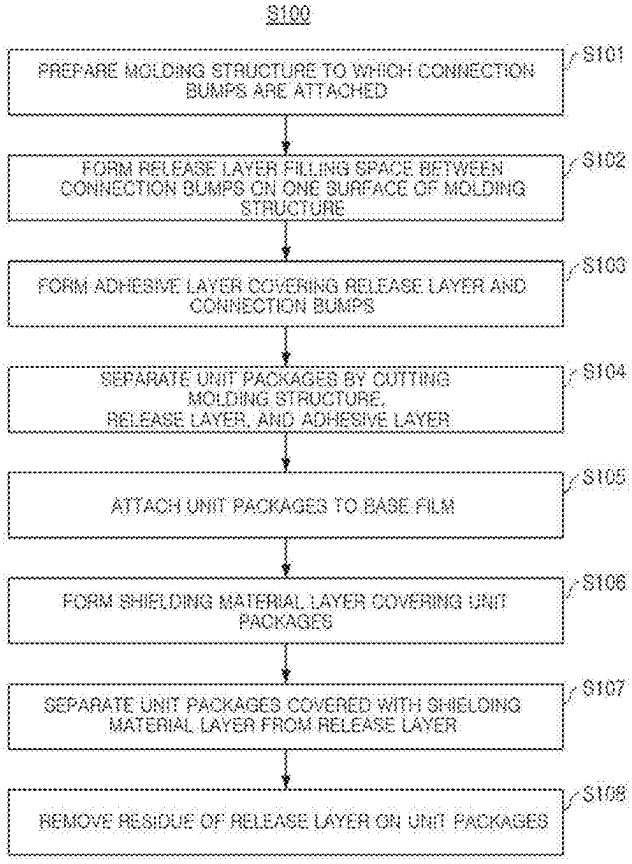
(57) **ABSTRACT**

A method of manufacturing a semiconductor package includes preparing a molding structure on which connection bumps are provided, forming a release layer at least partially filling spaces between the connection bumps, where the release layer includes a silicon (Si)-based polymer, forming an adhesive layer covering the release layer and the connection bumps, separating unit packages on which the release layer and the adhesive layer are formed by cutting the molding structure, the release layer, and the adhesive layer, attaching the unit packages to a base film by the adhesive layer, where the adhesive layer faces the base film, forming a shielding material layer covering at least a portion of each of the unit packages, at least a portion of the release layer, and at least a portion the adhesive layer, and separating the unit packages covered with the shielding material layer from the release layer.



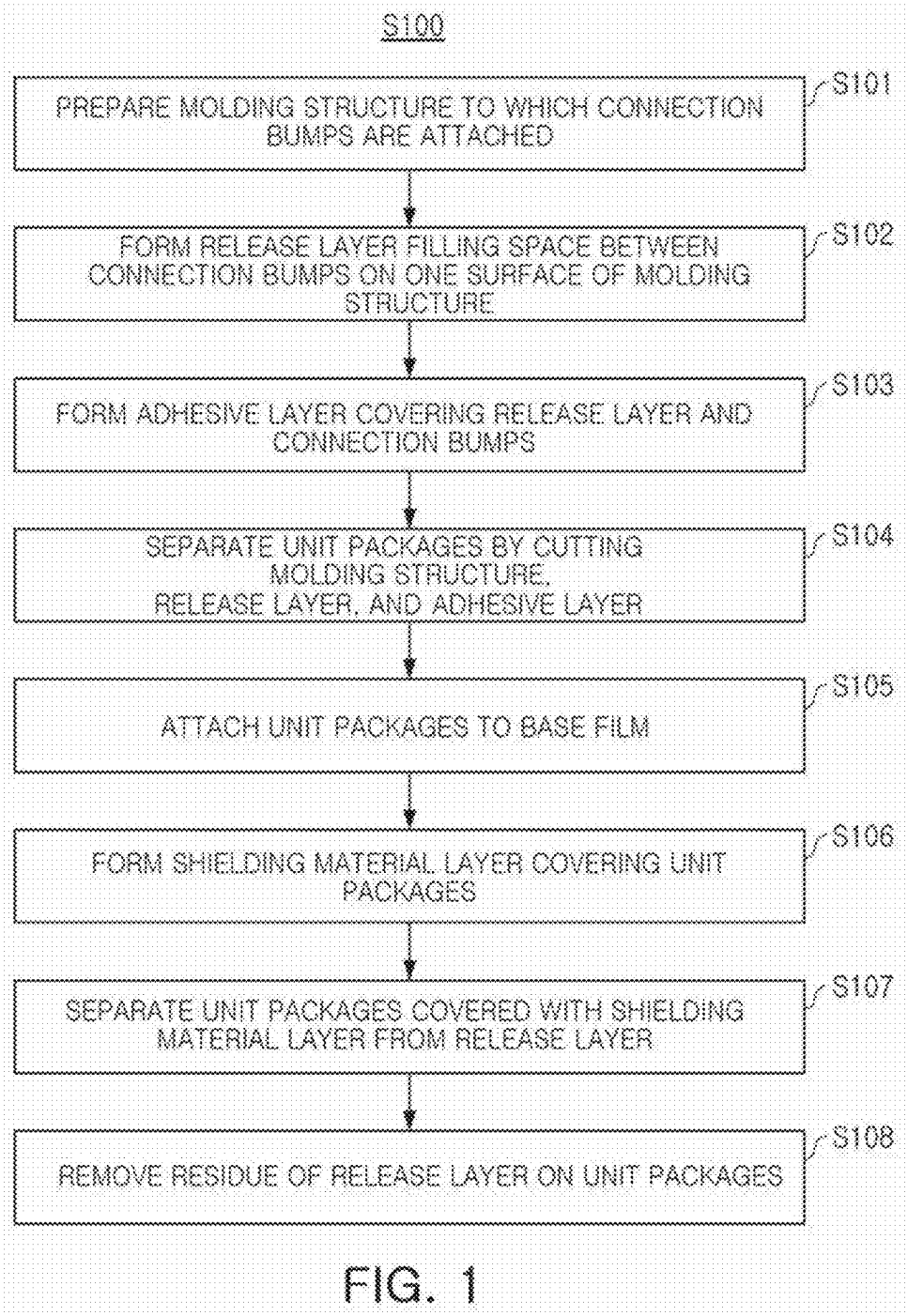

S100
PREPARE MOLDING STRUCTURE TO WHICH CONNECTION BUMPS ARE ATTACHED
S101
FORM RELEASE LAYER FILLING SPACE BETWEEN CONNECTION BUMPS ON ONE SURFACE OF MOLDING STRUCTURE
S102
FORM ADHESIVE LAYER COVERING RELEASE LAYER AND CONNECTION BUMPS
S103
SEPARATE UNIT PACKAGES BY CUTTING MOLDING STRUCTURE, RELEASE LAYER, AND ADHESIVE LAYER
S104
ATTACH UNIT PACKAGES TO BASE FILM
S105
FORM SHIELDING MATERIAL LAYER COVERING UNIT PACKAGES
S106
SEPARATE UNIT PACKAGES COVERED WITH SHIELDING MATERIAL LAYER FROM RELEASE LAYER
S107
REMOVE RESIDUE OF RELEASE LAYER ON UNIT PACKAGES
S108

FIG. 1

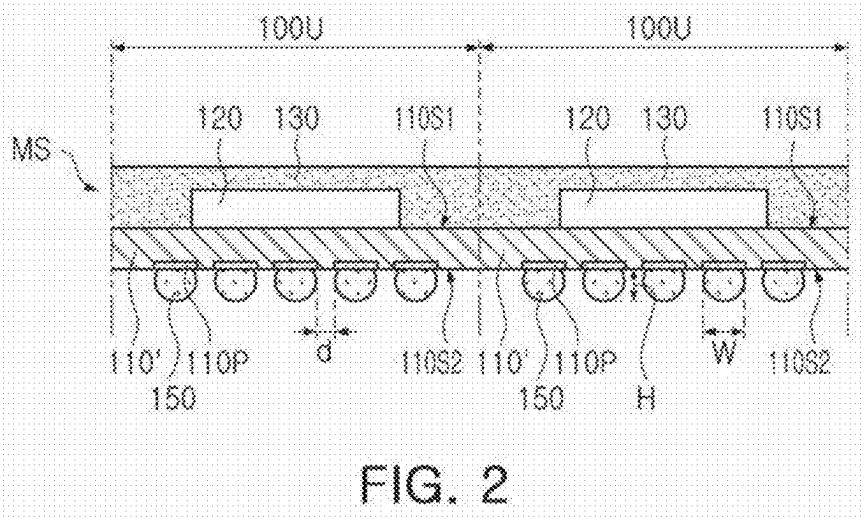

100U
100U
120
130
110S1
120
130
110S1
MS
110'
110P
150
d
110S2
110'
110P
150
H
W
110S2

FIG. 2

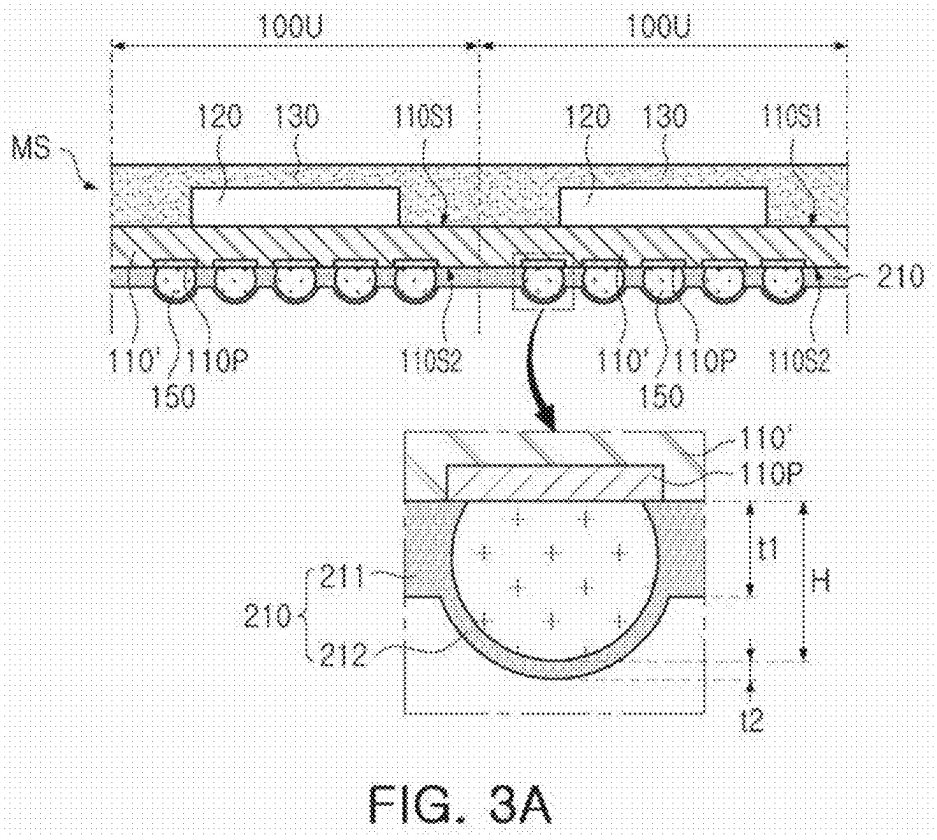

100U
100U
120
130
110S1
120
130
110S1
MS
210
110'
110P
150
110S2
110'
110P
150
110S2
110'
110P
211
210
212
t1
H
t2

FIG. 3A

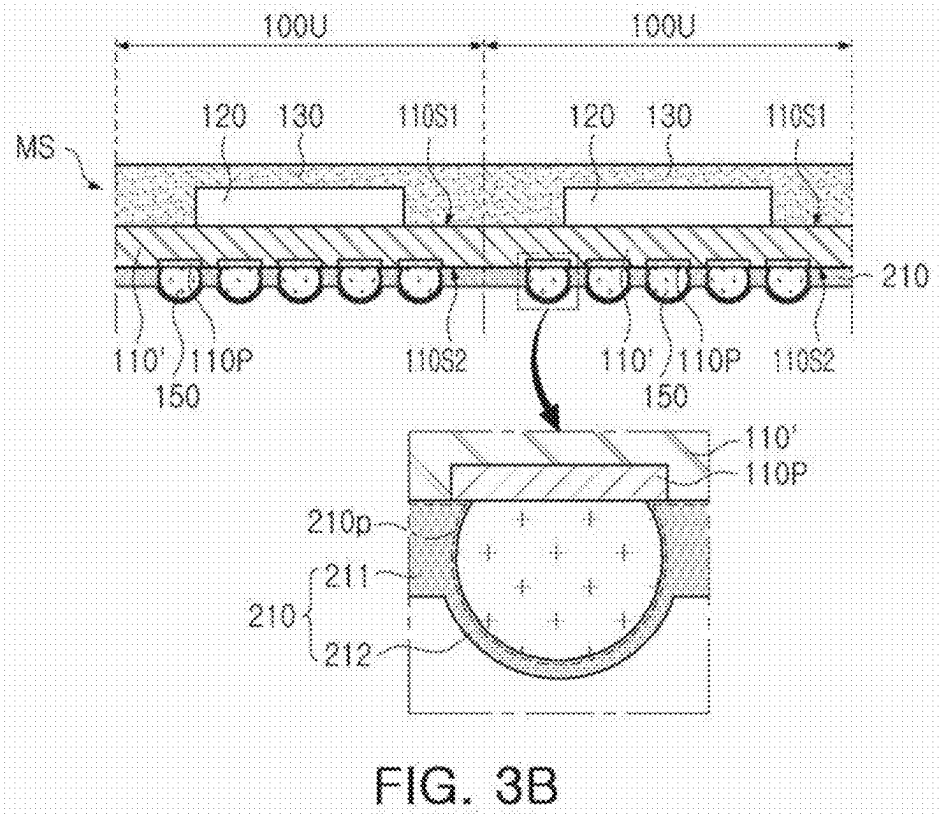

100U
100U
120
130
110S1
120
130
110S1
MS
210
110'
110P
150
110S2
110'
110P
150
110S2
110'
110P
210p
211
210
212

FIG. 3B

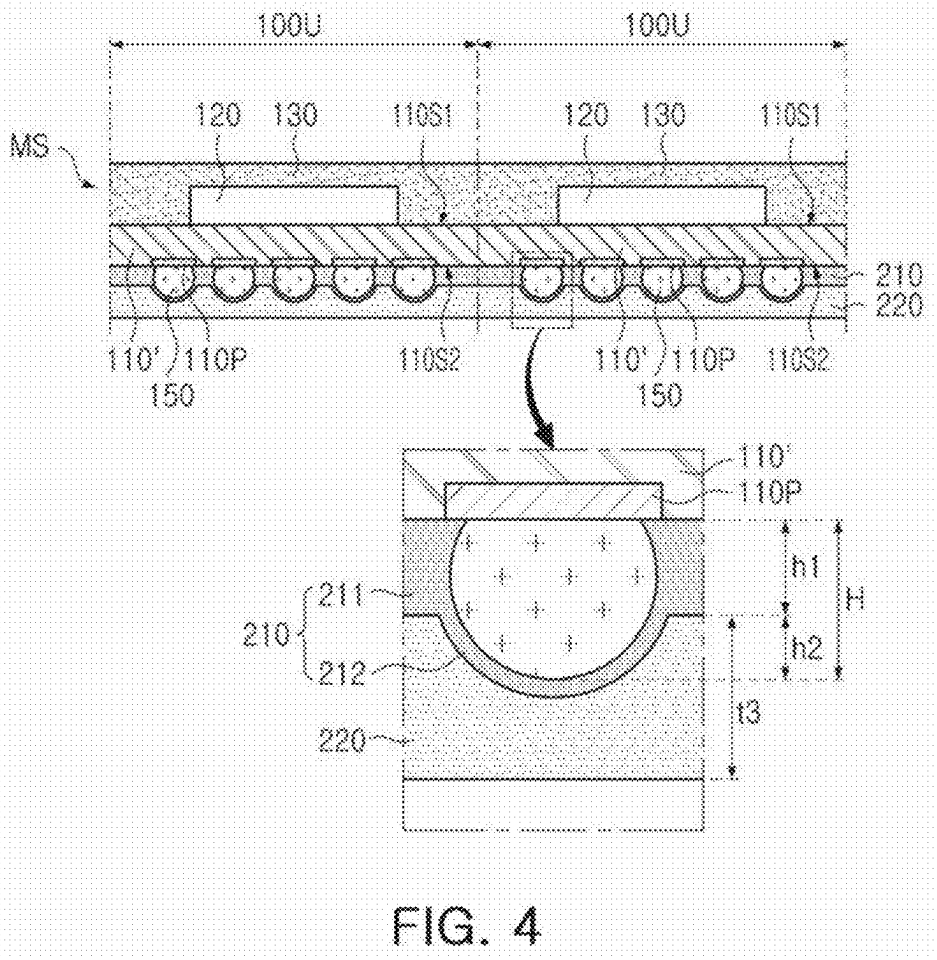

100U
100U
120
130
110S1
120
130
110S1
MS
210
220
110'
110P
150
110S2
110'
110P
150
110S2
110'
110P
h1
H
211
210
h2
212
t3
220

FIG. 4

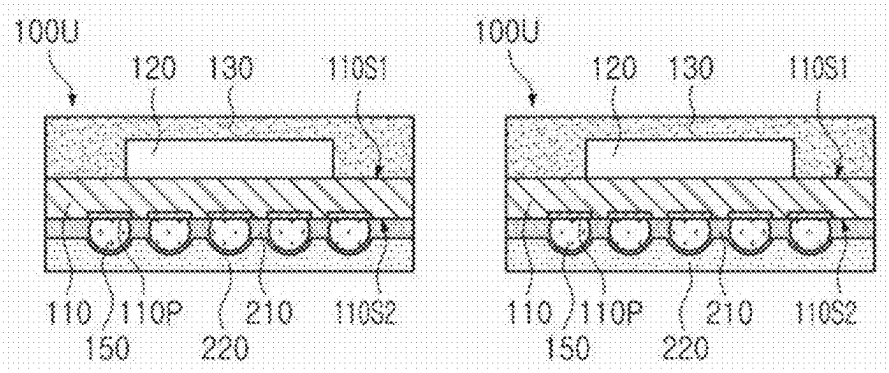

100U
120
130
110S1
110
110P
150
210
220
110S2
100U
120
130
110S1
110
110P
150
210
220
110S2

FIG. 5

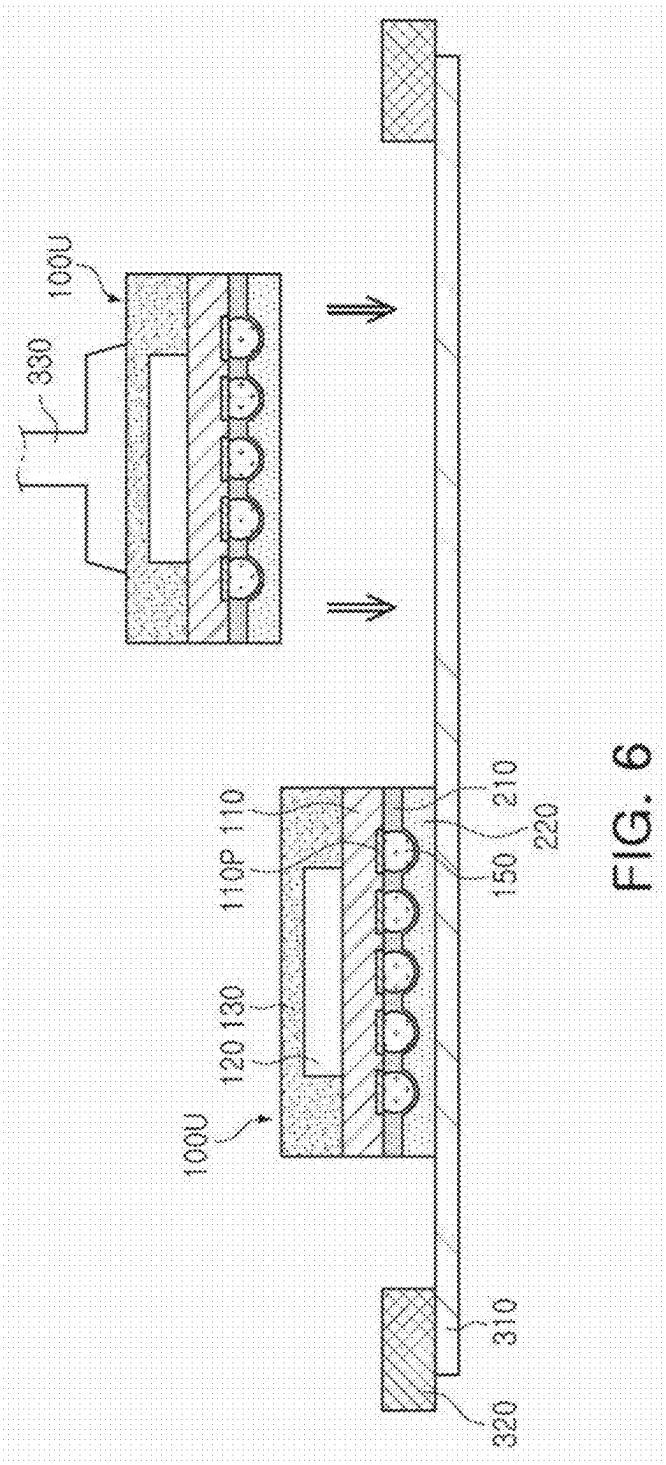


FIG. 6

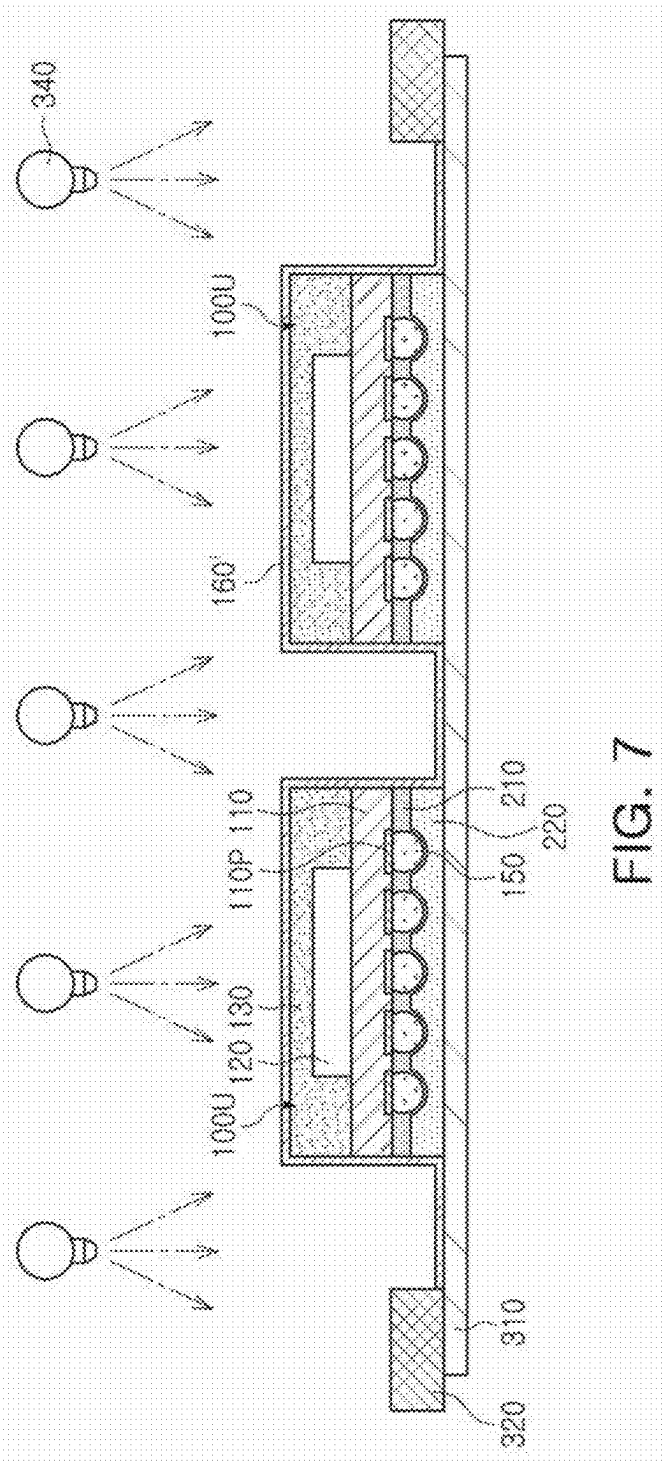


FIG. 7

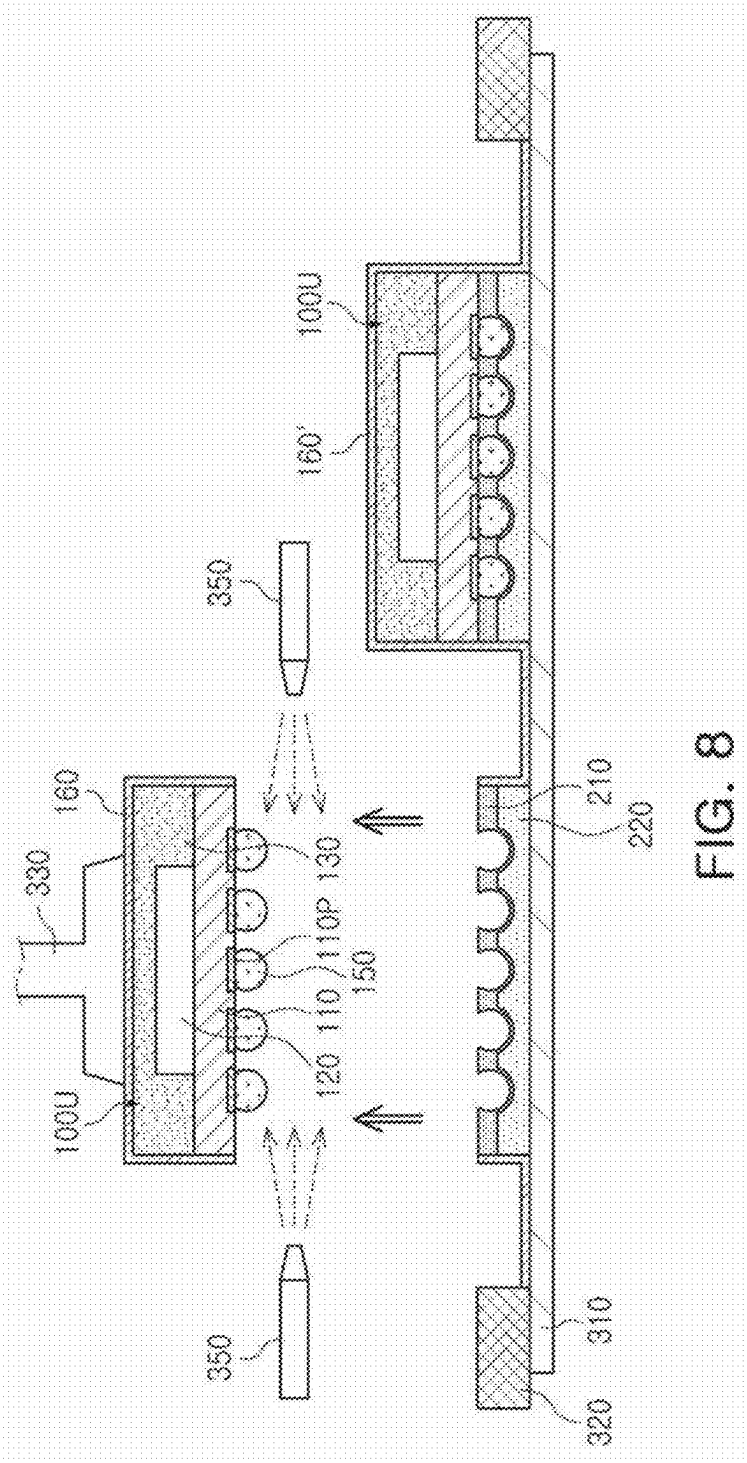

100U
160'
350
160
330
130
110P
150
110
120
100U
350
210
220
310
320

FIG. 8

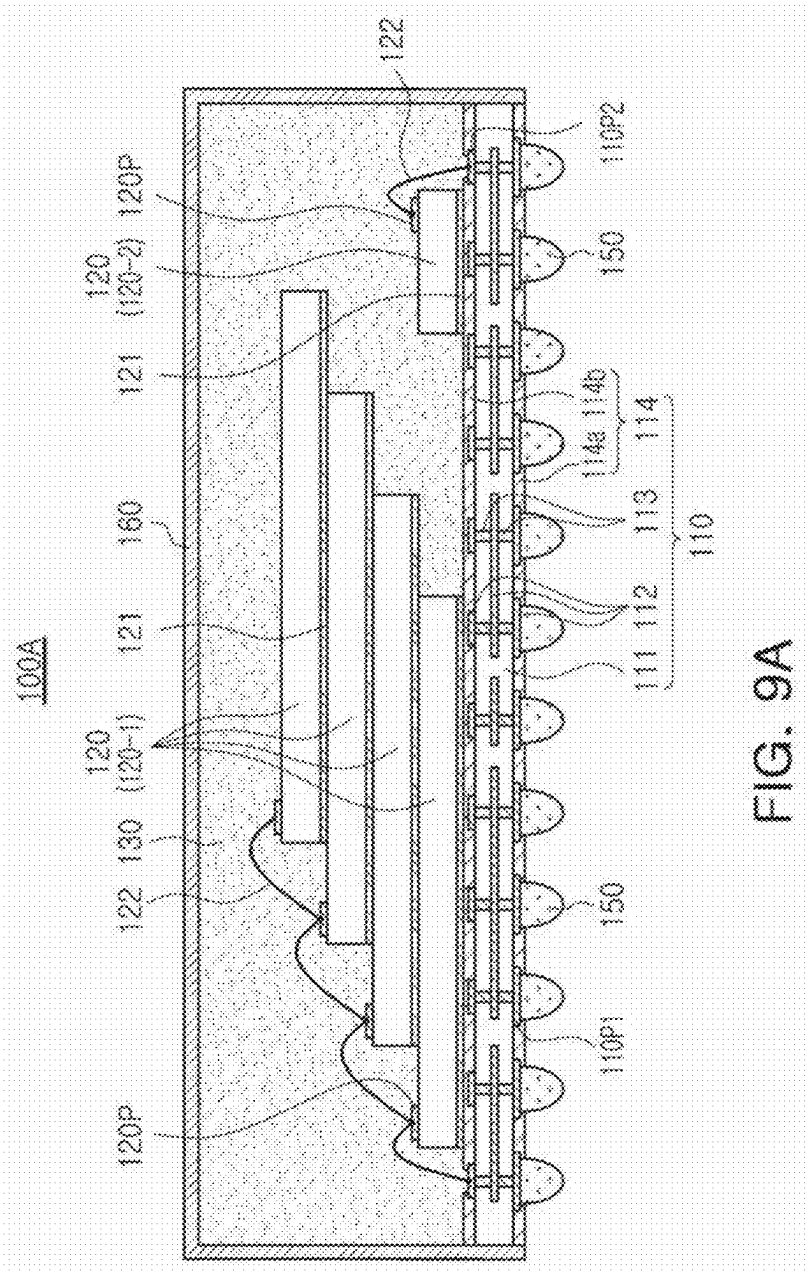

100A
120P
120 (120-1)
130
122
121
160
121
120 (120-2)
120P
122
110P2
150
114b
114a
114
113
112
111
110
150
110P1

FIG. 9A

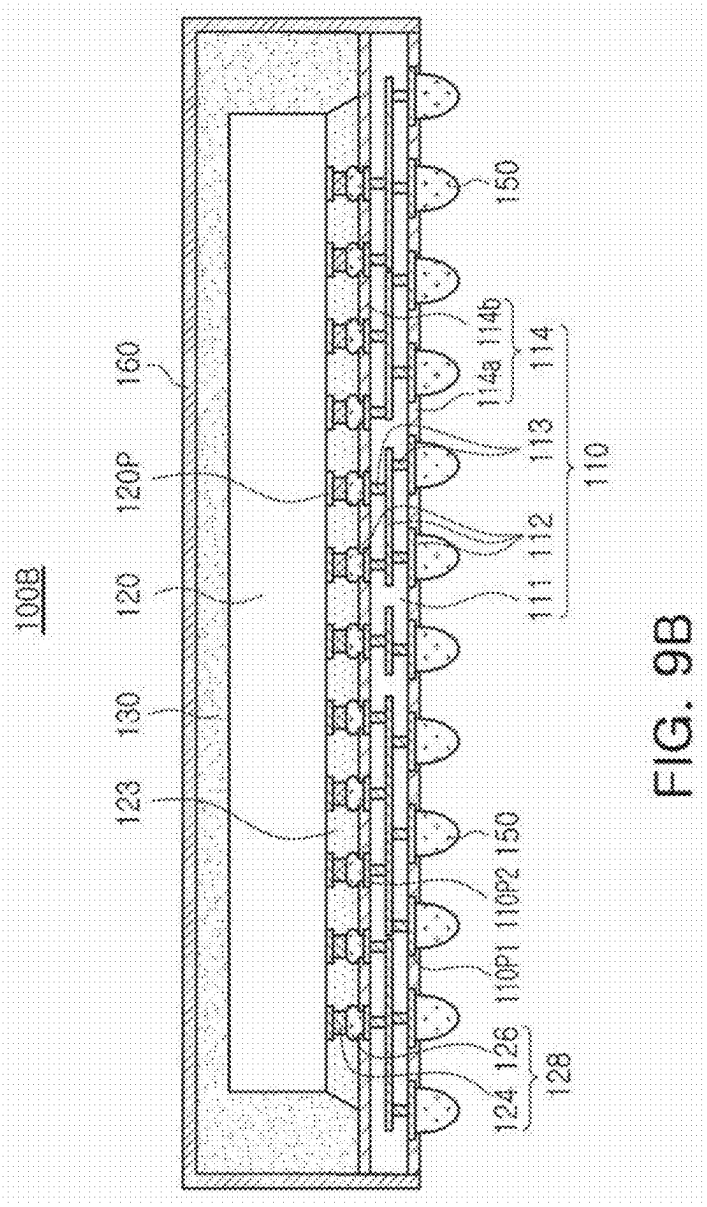

100B
160
120P
120
130
123
150
114a 114b
114
113
110
111 112
124 126
128
110P1 110P2 150

FIG. 9B

METHOD OF MANUFACTURING SEMICONDUCTOR PACKAGE

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application is based on and claims priority to Korean Patent Application No. 10-2024-0019793, filed on Feb. 8, 2024, in the Korean Intellectual Property Office, the disclosure of which is incorporated by reference herein in its entirety.

BACKGROUND

[0002] Example embodiments of the disclosure relate to a method of manufacturing a semiconductor package.

[0003] In order to protect users of electronic devices or semiconductor chips from electromagnetic interference (EMI), EMI shielding of semiconductor packages is required. Accordingly, manufacturing technology for semiconductor packages including an electromagnetic wave shielding layer is being developed.

[0004] Information disclosed in this Background section has already been known to or derived by the inventors before or during the process of achieving the embodiments of the present application, or is technical information acquired in the process of achieving the embodiments. Therefore, it may contain information that does not form the prior art that is already known to the public.

SUMMARY

[0005] One or more example embodiments provide a method of manufacturing a semiconductor package having improved reliability.

[0006] Additional aspects will be set forth in part in the description which follows and, in part, will be apparent from the description, or may be learned by practice of the presented embodiments.

[0007] According to an aspect of one or more embodiments, a method of manufacturing a semiconductor package may include preparing a molding structure on which connection bumps are provided, forming a release layer at least partially filling spaces between the connection bumps, where the release layer includes a silicon (Si)-based polymer, forming an adhesive layer covering the release layer and the connection bumps, separating unit packages on which the release layer and the adhesive layer are formed by cutting the molding structure, the release layer, and the adhesive layer, attaching the unit packages to a base film by the adhesive layer, where the adhesive layer faces the base film, forming a shielding material layer covering at least a portion of each of the unit packages, at least a portion of the release layer, and at least a portion the adhesive layer, separating the unit packages covered with the shielding material layer from the release layer, and removing residue of the release layer that is on the unit packages using an etchant including at least one of fluorine ions, hydroxide ions, and hydrogen ions.

[0008] According to an aspect of one or more embodiments, a method of manufacturing a semiconductor package may include preparing a molding structure on which connection bumps are provided, forming a release layer at least partially filling spaces between the connection bumps, forming an adhesive layer covering the release layer and the connection bumps, separating unit packages on which the release layer and the adhesive layer are formed by cutting the molding structure, the release layer, and the adhesive layer, attaching the unit packages to a base film, forming a shielding material layer covering at least a portion of each of the unit packages, at least a portion of the release layer, and at least a portion of the adhesive layer, and separating the unit packages covered with the shielding material layer from the release layer, where the release layer may include a first portion at least partially filling spaces between connection bumps that are adjacent to each other and a second portion at least partially covering a surface of each of the connection bumps, and a first thickness of the first portion of the release layer is different from a second thickness of the second portion of the release layer.

[0009] According to an aspect of one or more embodiments, a method of manufacturing a semiconductor package may include preparing a molding structure on which connection bumps are provided, forming a release layer at least partially filling spaces between the connection bumps, forming an adhesive layer covering the release layer and the connection bumps, separating unit packages on which the release layer and the adhesive layer are formed by cutting the molding structure, the release layer, and the adhesive layer, attaching the unit packages to a base film, forming a shielding material layer covering at least a portion of each of the unit packages, at least a portion of the release layer, and at least a portion of the adhesive layer, and separating the unit packages covered with the shielding material layer from the release layer, where the release layer may include polydimethylsiloxane (PDMS) or cross-linked silicone polymer.

BRIEF DESCRIPTION OF DRAWINGS

[0010] The above and other aspects, features, and advantages of certain example embodiments of the present disclosure will be more apparent from the following description taken in conjunction with the accompanying drawings, in which:

[0011] FIG. **1** is a flowchart illustrating a method of manufacturing a semiconductor package according to one or more embodiments;

[0012] FIG. **2** is a cross-sectional view illustrating operation S**101** of FIG. **1** according to one or more embodiments;

[0013] FIGS. **3**A and **3**B are cross-sectional views illustrating operation S**102** of FIG. **1** according to one or more embodiments;

[0014] FIG. **4** is a cross-sectional view illustrating operation S**103** of FIG. **1** according to one or more embodiments;

[0015] FIG. **5** is a cross-sectional view illustrating operation S**104** of FIG. **1** according to one or more embodiments;

[0016] FIG. **6** is a cross-sectional view illustrating operation S**105** of FIG. **1** according to one or more embodiments;

[0017] FIG. **7** is a cross-sectional view illustrating operation S**106** of FIG. **1** according to one or more embodiments;

[0018] FIG. **8** is a cross-sectional view illustrating operations S**107** and S**108** of FIG. **1** according to one or more embodiments; and

[0019] FIGS. **9**A and **9**B are cross-sectional views illustrating semiconductor packages according to one or more embodiments.

DETAILED DESCRIPTION

[0020] Hereinafter, example embodiments of the disclosure will be described in detail with reference to the accompanying drawings. The same reference numerals are used for the same components in the drawings, and redundant descriptions thereof will be omitted. The embodiments described herein are example embodiments, and thus, the disclosure is not limited thereto and may be realized in various other forms.

[0021] As used herein, expressions such as "at least one of," when preceding a list of elements, modify the entire list of elements and do not modify the individual elements of the list. For example, the expression, "at least one of a, b, and c," should be understood as including only a, only b, only c, both a and b, both a and c, both b and c, or all of a, b, and c.

[0022] Unless otherwise specified, terms, such as "upper portion," "upper surface," "lower portion," "lower surface," "side surface," etc. are based on the drawings, and may vary used in the directions in which components are actually arranged.

[0023] It will be understood that when an element or layer is referred to as being "over," "above," "on," "below," "under," "beneath," "connected to" or "coupled to" another element or layer, it can be directly over, above, on, below, under, beneath, connected or coupled to the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly over," "directly above," "directly on," "directly below," "directly under," "directly beneath," "directly connected to" or "directly coupled to" another element or layer, there are no intervening elements or layers present.

[0024] As used herein, the terms "covering" and "filling" may refer to a partial covering/filling or a full covering/filling as will be understood by one or ordinary skill in the art from the disclosure herein.

[0025] In addition, ordinal numbers, such as "first," "second," "third," etc. may be used as labels for specific elements, steps, directions, etc. to distinguish various elements, steps, directions, etc. from each other. Terms that are not described using "first," "second," etc. in the specification may still be referred to as "first" or "second" in the claims. In addition, terms referenced by a particular ordinal number may be described elsewhere with a different ordinal number.

[0026] FIG. **1** is a flowchart illustrating a method S**100** of manufacturing a semiconductor package according to one or more embodiments.

[0027] Referring to FIG. **1**, the method S**100** of manufacturing a semiconductor package according to one or more embodiments may include operation S**101** of preparing a molding structure to which connection bumps are attached, operation S**102** of forming a release layer filling a space between the connection bumps on one surface of the molding structure, operation S**103** of forming an adhesive layer covering the release layer and the connection bumps on the molding structure, operation S**104** of separating unit packages on which the release layer and the adhesive layer are formed by cutting the molding structure, the release layer, and the adhesive layer, operation S**105** of attaching the unit packages to a base film, operation S**106** of forming a shielding material layer covering at least a portion of each of the unit packages, the release layer, and the adhesive layer, and operation S**107** of separating the unit packages covered with the shielding material layer from the release layer. According to one or more embodiments, the method S**100** of manufacturing a semiconductor package may further include operation S**108** of removing residues of the release layer on the unit packages.

[0028] According to one or more embodiments, by using a release layer including a silicon (Si)-based polymer, the unit packages may be mechanically separated from the release layer without an additional process to remove adhesive force between the release layer and the connection bumps. That is, the unit packages may be separated from the release layer while the release layer and the adhesive layer remain adhered to the base film. In addition, the release layer including a silicon (Si)-based polymer may sufficiently fill the space between adjacent connection bumps even if the size of the connection bumps, for example, a horizontal width and/or height, increases, thereby preventing the occurrence of voids and back-spill defects.

[0029] Hereinafter, the method S**100** of manufacturing a semiconductor package according to one or more embodiments is described in detail with reference to FIGS. **2** to **8**.

[0030] FIG. **2** is a cross-sectional view illustrating the operation S**101** of FIG. **1** according to one or more embodiments.

[0031] Referring to FIGS. **1** and **2**, a molding structure MS including a plurality of unit packages **100**U may be prepared. The molding structure MS may include a substrate strip **110'**, semiconductor chips **120**, a mold layer **130**, and connection bumps **150**.

[0032] The substrate strip **110'** may include a plurality of package substrates (e.g., printed circuit boards (PCBs)) connected as one body. The semiconductor chips **120** may be electrically connected to a first surface **110**S**1** of the substrate strip **110'** using a flip-chip method or a wire bonding method. The semiconductor chips **120** may be provided in larger numbers than that shown in the drawing. For example, each of the plurality of unit packages **100**U may include a plurality of semiconductor chips arranged vertically and/or horizontally on the substrate strip **110'** or the package substrate.

[0033] The semiconductor chips **120** may include logic chips, such as a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), an application processor (AP), a digital signal processor, a cryptographic processor, a microprocessor, a microcontroller, an analog-to-digital converter, and application-specific integrated circuits (ASICs), and/or memory chips including volatile memories, such as dynamic random-access memory (RAM) (DRAM) static RAM (SRAM), etc., and nonvolatile memories, such as phase change RAM (PRAM), magnetic RAM (MRAM), resistive RAM (RRAM), flash memory, etc.

[0034] The mold layer **130** may include an insulating resin sealing the semiconductor chips **120**, such as a thermosetting resin, such as an epoxy resin, a thermoplastic resin, such as polyimide, or prepreg, Ajinomoto build-up film (ABF), FR-4, bismaleimide-triazine (BT), epoxy molding compound (EMC), etc.

[0035] The connection bumps **150** may be arranged on a second surface **110**S**2** of the substrate strip **110'**. The connection bumps **150** may be attached to a lower terminal **110**P of the substrate strip **110'**. The connection bumps **150** may include a low melting point metal, such as tin (Sn) or an alloy including tin (Sn) (e.g., Sn—Ag—Cu, Sn—Ag, etc.).

According to one or more embodiments, the connection bumps **150** may have a form of a combination of a pillar and a ball.

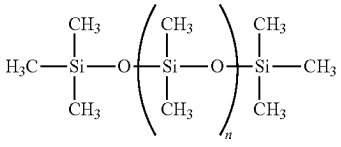
[0036] A height H of the connection bumps **150** may be about 180 μm or greater. For example, the height H of the connection bumps **150** may be about 180 μm to about 400 μm, but is not limited thereto. A horizontal width W of the connection bumps **150** may be about 180 μm or greater. For example, the horizontal width W of the connection bumps **150** may be about 180 μm to about 400 μm, but is not limited thereto. A spacing d between adjacent connection bumps **150** may be about 180 μm to about 400 μm, but is not limited thereto. Since the connection bumps **150** are completely impregnated with a release layer to be described below, in the method S**100** of manufacturing a semiconductor package of one or more embodiments, an electromagnetic wave shielding layer for a semiconductor package may be formed without restrictions depending on the size of the connection bumps **150**.

[0037] FIGS. **3**A and **3**B are cross-sectional views illustrating operation S**102** of FIG. **1** according to one or more embodiments.

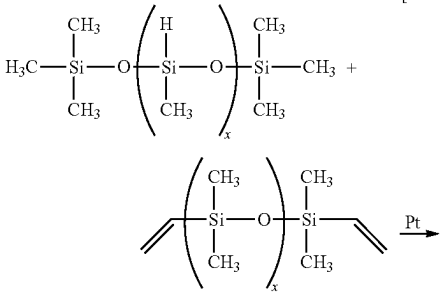
[0038] Referring to FIGS. **1** and **3**A, a release layer **210** may be formed on the molding structure MS. The release layer **210** may be coated directly on the second surface **110**S**2** of the substrate strip **110'**. The release layer **210** may be formed using, for example, spin coating or slit coating. The release layer **210** may include a silicon (Si)-based polymer.

[0039] The release layer **210** may include, for example, polydimethylsiloxane (PDMS) or cross-linked silicone polymer. In one or more embodiments, the release layer **210** may include a compound represented by Chemical Formula (1) or Chemical Formula (2) below. Chemical Formula (1) below represents a structural formula of PDMS, and Chemical Formula (2) below represents a polymerization formula of a cross-linked silicone polymer using methicone and vinyl dimethicone.

[Chemical Formula (1)]



[Chemical Formula (2)]



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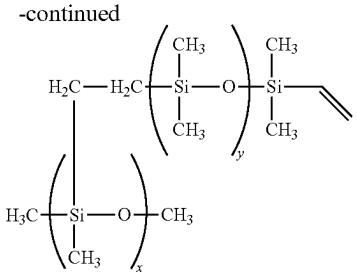


[0040] The viscosity of the release layer **210** may range from about 0.5 mPa's to about 30000 mPas, or from about 10 mPa's to about 1000 mPa's (@25° C.). If the viscosity of the release layer **210** exceeds about 30000 mPa s, filling properties of the release layer **210** between the connection bumps **150** may be reduced. If the viscosity of the release layer **210** is less than about 0.5 mPas, it may be difficult for the release layer **210** to cover curved surfaces of the connection bumps **150**. In addition, in order to minimize the occurrence of debris during a sawing process of the release layer **210** (see FIG. **5**), the elastic modulus of the release layer **210** may range from about 0.1 MPa to about 5 MPa or about 0.5 MPa to about 3 MPa, but is not limited thereto.

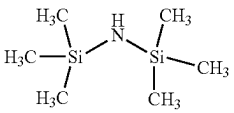
[0041] The release layer **210** may be formed using a silicon (Si)-based polymer mixed with various additives to have the aforementioned physical properties. For example, the release layer **210** of the example embodiment may be formed using a silicon (Si)-based polymer in which a polymer including silicon (Si) (e.g., PDMS, methicone, vinyl dimethicone, etc.) is mixed with a crosslinking agent at a ratio of about 5:1 to about 20:1.

[0042] The release layer **210** may include a first portion **211** filling the space between adjacent connection bumps **150** and a second portion **212** covering at least a portion of the curved surface of each of the connection bumps **150**. The first portion **211** of the release layer **210** may cover ½ or more of the height H of the connection bumps **150**. That is, the first portion **211** may extend from the surface **110**S**2** to at least half of the height H of the connection bumps **150**. The second portion **212** of the release layer **210** may extend conformally along at least a portion of the curved surface of each of the connection bumps **150**. A first thickness t**1** of the first portion **211** of the release layer **210** and a second thickness t**2** of the second portion **212** of the release layer **210** may be different from each other. The first thickness t**1** of the first portion **211** of the release layer **210** may be ½ or more of the height H of the connection bumps **150**. The second thickness t**2** of the second portion **212** may be less than the first thickness t**1** of the first portion **211** of the release layer **210**. For example, the first thickness t**1** of the first portion **211** of the release layer **210** may be about 90 μm to about 300 μm, but is not limited thereto. The first thickness t**1** of the first portion **211** of the release layer **210** may be determined by considering the height H, horizontal width W, and spacing d of the connection bumps **150**.

[0043] Referring to FIGS. **1** and **3**B, according to one or more embodiments, an operation of surface-treating the molding structure MS and the connection bumps **150** may be further included before forming the release layer **210**. A surface treatment layer **210***p* may be further formed between the release layer **210** and the molding structure MS and between the release layer **210** and the connection bumps

150. The surface treatment layer **210***p* may modify the surface of the connection bumps **150** and the molding structure MS to be hydrophobic, allowing the release layer **210** to be easily separated in a subsequent process. When the molding structure MS is separated from the release layer **210**, the surface treatment layer **210***p* may suppress the occurrence of residues on the release layer **210** and prevent damage to the connection bumps **150**. According to a process, a boundary between the surface treatment layer **210***p* and the release layer **210** may not be apparent. For example, when the release layer **210** includes PDMS, the surface treatment layer **210***p* may include a compound represented by Chemical Formula (3) below. The Chemical Formula (3) below represents hexamethyldisiloxane (HMDS).

[Chemical Formula (3)]



[0044] FIG. **4** is a cross-sectional view illustrating the operation S**103** of FIG. **1** according to one or more embodiments.

[0045] Referring to FIGS. **1** and **4**, an adhesive layer **220** may be formed on the molding structure MS. The adhesive layer **220** may be formed to cover the entire release layer **210** and the connection bumps **150** (e.g., the exposed surfaces of the connection bumps **150**). The adhesive layer **220** may include a thermosetting polymer or a photocurable polymer. In one or more embodiments, the adhesive layer **220** may include thermosetting siloxane polymer or photocurable silicone acryl polymer.

[0046] The connection bumps **150** may include an upper region covered by the first portion **211** of the release layer **210** and a lower region covered by the second portion **212** of the release layer **210**. A height h**1** of the upper region of the connection bumps **150** may be equal to or greater than a height h**2** of the lower region. A third thickness t**3** of the adhesive layer **220** may be greater than the height h**2** of the lower region of the connection bumps **150**. For example, the third thickness t**3** of the adhesive layer **220** may be about 100 μm to about 250 μm, but is not limited thereto. The third thickness t**3** of the adhesive layer **220** may be determined by considering the height h**2** of the lower region of the connection bumps **150**, etc.

[0047] FIG. **5** is a cross-sectional view illustrating the operation S**104** of FIG. **1** according to one or more embodiments.

[0048] Referring to FIGS. **1** and **5**, unit packages **100**U in which the release layer **210** and the adhesive layer **220** are formed may be separated. The unit packages **100**U may include the package substrate **110** separated from the substrate strip **110'**, at least one semiconductor chip **120**, a mold layer **130** disposed on the upper surface **110S1** of the package substrate **110**, and the connection bumps **150** disposed on the lower surface **110S2** of the package substrate **110**. The unit packages **100**U may be formed by cutting the molding structure MS, the release layer **210**, and the adhesive layer **220**. The molding structure MS, release layer **210**, and adhesive layer **220** may be cut by a sawing process.

[0049] FIG. **6** is a cross-sectional view illustrating the operation S**105** of FIG. **1** according to one or more embodiments.

[0050] Referring to FIGS. **1** and **6**, the unit packages **100**U may be attached to a base film **310**. The unit packages **100**U may be arranged so that the adhesive layer **220** faces the base film **310**. The unit packages **100**U may be arranged on the base film **310** pickup device **330** to be spaced apart from each other in a horizontal direction. A frame **320** may be attached to an end of the base film **310**. The frame **320** may be formed of metal, but is not limited thereto. The base film **310** may be a film coated with an adhesive on at least one side thereof. For example, the base film **310** may include a polyimide (PI) film, a polyethylene terephthalate (PET) film, or a polyethylene-naphthalate (PEN) film.

[0051] FIG. **7** is a cross-sectional view illustrating the operation S**106** of FIG. **1** according to one or more embodiments.

[0052] Referring to FIGS. **1** and **7**, a shielding material layer **160'** covering the unit packages **100**U may be formed. The shielding material layer **160'** may cover at least a portion of each of the unit packages **100**U, the release layer **210**, and the adhesive layer **220**. The shielding material layer **160'** may be conformally formed by a coating device **340**. The coating device **340** may form the shielding material layer **160'** by performing a deposition process, such as physical vapor deposition (PVD) or chemical vapor deposition (CVD). For example, the coating device **340** may be a sputtering device, but is not limited thereto.

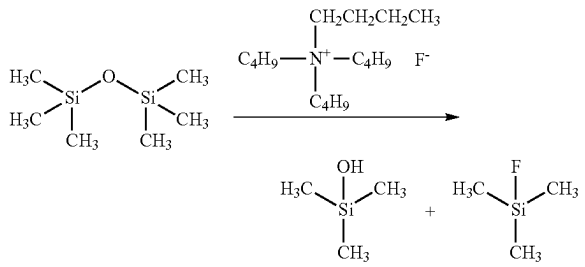
[0053] The shielding material layer **160'** may be a thin film formed on the surface of each of the unit packages **100**U, the release layer **210**, and the adhesive layer **220**. A thickness of the shielding material layer **160'** may be about 5 μm or less, but is not limited thereto. The shielding material layer **160'** may include a conductive material for electromagnetic interference (EMI) shielding, such as iron (Fe), nickel (Ni), gold (Au), silver (Ag), copper (Cu), and alloys thereof. The shielding material layer **160'** may include at least one conductive thin film. For example, the shielding material layer **160'** may be a three-layer thin film in which a stainless steel (SUS) film, a copper (Cu) film, and a stainless steel (SUS) film are sequentially stacked.

[0054] FIG. **8** is a cross-sectional view illustrating the operations S**107** and S**108** of FIG. **1** according to one or more embodiments.

[0055] Referring to FIGS. **1** and **8**, the unit packages **100**U on which an electromagnetic wave shielding layer **160** is formed (i.e., by the shielding material layer **160'**) may be separated from the release layer **210**. The pickup device **330** may pick up the unit packages **100**U on which the shielding material layer **160'** is formed. Since the release layer **210** has a relatively weak adhesive force compared to the adhesive layer **220**, the unit packages **100**U may be separated from the release layer **210** by the pickup device **330**, and the shielding material layer **160'** may be cut to form the electromagnetic wave shielding layer **160** covering the unit packages **100**U. In this manner, according to the method S**100** of manufacturing a semiconductor package of one or more embodiments, the unit packages **100**U may be separated without an additional process to remove the adhesive force between the release layer **210** and the connection bumps **150**. That is, the unit packages **100**U may be separated while the release layer **210** and the adhesive layer **220** remain adhered to the base film **310**.

[0056] According to one or more embodiments, an operation of removing residues of the release layer **210** on the unit packages **100**U may be further performed. The residues of the release layer **210** may be removed by a wet etching process using an etchant. For example, the etchant may be sprayed toward the lower surfaces and/or connection bumps **150** of the unit packages **100**U using a nozzle **350**. The etchant may include at least one of fluorine ions (F−), hydroxide ions (OH−), and hydrogen ions (H+). For example, the etchant may remove the residues of the release layer **210** through a reaction of Chemical Formula (4) below. Chemical Formula (4) below represents a decomposition reaction of silicon-based polymer by an etchant including tetra-n-butylammonium fluoride (TBMF).

[Chemical Formula 4]



[0057] FIGS. **9**A and **9**B are cross-sectional views of semiconductor packages according to one or more embodiments. FIGS. **9**A and **9**B illustrate semiconductor packages formed by the manufacturing method of FIG. **1**, respectively.

[0058] Referring to FIG. **9**A, the semiconductor package **100**A of one or more embodiments may include a package substrate **110**, a plurality of semiconductor chips **120**, a mold layer **130**, connection bumps **150**, and an electromagnetic wave shielding layer **160**.

[0059] The package substrate **110** may be a semiconductor package substrate including a PCB, a ceramic substrate, a glass substrate, or a tape wiring substrate. For example, the package substrate **110** may be a double-sided PCB or a multi-layer PCB. The package substrate **110** may include an insulating layer **111**, interconnection patterns **112**, and interconnection vias **113**.

[0060] The insulating layer **111** may include, for example, a thermosetting resin, such as an epoxy resin, a thermoplastic resin, such as polyimide, a prepreg including an inorganic filler or/and glass fiber (glass cloth or glass fabric), ABF, FR-4, and the like. The insulating layer **111** may include a plurality of insulating layers stacked in a vertical direction. For example, the insulating layer **111** may include a core layer and a build-up layer stacked on an upper surface and/or a lower surface of the core layer. According to a process, the boundaries between the plurality of insulating layers may not be apparent. According to one or more embodiments, the insulating layer **111** may include a photosensitive resin, such as photo imageable dielectric (PID).

[0061] The interconnection patterns **112** may form an electrical connection path within the insulating layer **111**. The interconnection patterns **112** may include, for example, at least one of copper (Cu), aluminum (Al), nickel (Ni), silver (Ag), gold (Au), platinum (Pt), tin (Sn), lead (Pb), titanium (Ti), chromium (Cr), palladium (Pd), indium (In), zinc (Zn), and carbon (C), or alloys including two or more metals thereof. Each of the interconnection patterns **112** may be formed of electrolytically deposited (ED) copper foil, rolled-annealed (RA) copper foil, ultra-thin copper foil, sputtered copper, copper alloys, and the like. The interconnection patterns **112** may include a plurality of pattern layers spaced apart from each other in the vertical direction. A plurality of pattern layers may extend in the horizontal direction on each vertical level. The interconnection patterns **112** may include fewer or more pattern layers than those shown in the drawing. The interconnection patterns **112** may include lower connection terminals **110**P**1** and upper connection terminals **110**P**2**. The lower connection terminals **110**P**1** may be a pad portion of the lowermost interconnection patterns **112**, and the upper connection terminals **110**P**2** may be a pad portion of the uppermost interconnection patterns **112**.

[0062] The interconnection vias **113** may electrically connect the interconnection patterns **112** within the insulating layer **111**. The interconnection vias **113** may include, for example, at least one of copper (Cu), aluminum (Al), nickel (Ni), silver (Ag), gold (Au), platinum (Pt), tin (Sn), lead (Pb), titanium (Ti), chromium (Cr), palladium (Pd), indium (In), zinc (Zn), and carbon (C) or alloys including two or more metals thereof. The interconnection vias **113** may include a conductive material completely filling a via hole penetrating through at least a portion of the insulating layer **111** or include a conductive material conformally formed along the wall of the via hole. According to one or more embodiments, at least some of the interconnection vias **113** may be formed such that a conductive material is applied along the wall of the via hole and an internal space of the via hole surrounded by the conductive material is filled with an insulating material.

[0063] The package substrate **110** may further include a protective layer **114**. The protective layer **114** may be formed on upper and/or lower surface of the insulating layer **111**. For example, the protective layer **114** may include a lower protective layer **114***a* and an upper protective layer **114***b*. The lower protective layer **114***a* may include an opening exposing at least a portion of the lower connection terminals **110**P**1**. The upper protective layer **114***b* may include an opening exposing at least a portion of the upper connection terminals **110**P**2**. The protective layer **114** may be formed using, for example, solder resist.

[0064] A plurality of semiconductor chips **120** may be mounted on the package substrate **110**. The plurality of semiconductor chips **120** may be electrically connected to the package substrate **110** using a wire bonding method. The plurality of semiconductor chips **120** may be attached to the package substrate **110** and other vertically adjacent semiconductor chips **120** using an adhesive film **121**. The adhesive film **121** may include an inorganic adhesive or a polymer adhesive. The polymer adhesive may include, for example, a thermosetting polymer, a thermoplastic polymer, or a hybrid resin that is a mixture of the thermosetting polymer and the thermoplastic polymer. Connection pads **120**P of the plurality of semiconductor chips **120** may be electrically connected to upper connection terminals **110**P**2** through a bonding wire **122**. The plurality of semiconductor chips **120** may be bare semiconductor chips without separate bumps or interconnection layers, but are not limited thereto and the plurality of semiconductor chips **120** may be packaged-type semiconductor chips. The plurality of semicon-

ductor chips **120** may include a semiconductor wafer including semiconductor elements, such as silicon, germanium or a semiconductor compound, such as silicon carbide (SiC), gallium arsenide (GaAs), indium arsenide (InAs), and indium phosphide (InP) and an integrated circuit (IC) formed on the semiconductor wafer. The plurality of semiconductor chips **120** may include different types of semiconductor chips **120-1** and **120-2**. For example, the plurality of semiconductor chips **120** may include a plurality of first semiconductor chips **120-1** and at least one second semiconductor chip **120-2**. According to one or more embodiments, at least some of the plurality of semiconductor chips **120** may be mounted using a flip-chip method.

[0065] The plurality of first semiconductor chips **120-1** may be memory semiconductor chips. The plurality of first semiconductor chips **120-1** may include nonvolatile memory devices, such as flash memory, PRAM, MRAM, ferroelectric random access memory (FeRAM), and RRAM and volatile memory devices, such as DRAM and SRAM. The flash memory may be, for example, V-NAND flash memory. The plurality of first semiconductor chips **120-1** may be shifted in at least one direction so that each of the connection pads **120**P is exposed upwardly, but the stacked form of the plurality of first semiconductor chips **120-1** is not limited to that illustrated in the drawings. The plurality of first semiconductor chips **120-1** may be electrically connected to each other through the bonding wires **122**.

[0066] The at least one second semiconductor chip **120-2** may be a control semiconductor chip. The at least one second semiconductor chip **120-2** may include various active and/or passive devices, such as field effect transistors (FETs) including planar FETs and FinFETs, logic devices, such as AND, OR, NOT, system large-scale integration (LSI) circuit, complementary metal-oxide semiconductor (CMOS) image sensor (CIS), and micro-electromechanical systems (MEMS).

[0067] The at least one second semiconductor chip **120-2** may control access to data stored in the plurality of first semiconductor chips **120-1**. At least one second semiconductor chip **120-2** may control write/read operations of the plurality of first semiconductor chips **120-1** according to control commands from an external host. The at least one second semiconductor chip **120-2** may perform wear leveling, garbage collection, bad block management, and error correction code (ECC). The at least one second semiconductor chip **120-2** may be disposed to be spaced apart from the plurality of first semiconductor chips **120-1**, but embodiments are not limited thereto.

[0068] The mold layer **130** may seal the plurality of semiconductor chips **120** on the package substrate **100**. The mold layer **130** may cover each of the plurality of first semiconductor chips **120-1** and the at least one second semiconductor chip **120-2**. The mold layer **130** may include, for example, an EMC.

[0069] The connection bumps **150** may be arranged on the lower surface of the package substrate **110**. The semiconductor package **100**A may be electrically connected to an external device, such as a module substrate or main board through the connection bumps **150**. The connection bumps **150** may include, for example, tin (Sn) or an alloy including tin (Sn) (e.g., Sn—Ag—Cu, Sn—Ag, etc.). The connection bumps **150** may have the size described above with reference to FIG. **2**, but are not limited thereto. In the method of manufacturing a semiconductor package of one or more embodiments, the electromagnetic wave shielding layer **160** may be formed without restrictions depending on the size of the connection bumps **150**.

[0070] The electromagnetic wave shielding layer **160** may cover the package substrate **110** and the mold layer **130**. The electromagnetic wave shielding layer **160** may be formed using a conformal shielding method. For example, the electromagnetic wave shielding layer **160** may extend to have a substantially constant thickness along the side surface of the package substrate **100** and the side surface and upper surface of the mold layer **130**. According to one or more embodiments, the electromagnetic wave shielding layer **160** may be connected to a ground pattern among the interconnection patterns **112**. The electromagnetic wave shielding layer **160** may be formed by, for example, a PVD method. According to one or more embodiments, the electromagnetic wave shielding layer **160** may be formed by a spray method. The electromagnetic wave shielding layer **160** may include a metal material, such as copper (Cu) or stainless steel, but is not limited thereto.

[0071] Referring to FIG. **9**B, a semiconductor package **100**B of one or more embodiments may include the package substrate **110**, at least one semiconductor chip **120**, the mold layer **130**, the connection bumps **150**, and the electromagnetic wave shielding layer **160**. The semiconductor package **100**B may include substantially the same or similar components as the semiconductor package **100**A illustrated in FIG. **9**A, except that at least one semiconductor chip **120** is mounted in a flip-chip manner. Accordingly, corresponding components are referred to by the same or similar reference numerals, and redundant descriptions may be omitted below.

[0072] The at least one semiconductor chip **120** may be disposed such that an active surface on which the connection pads **120**P are arranged faces the package substrate **110**. The at least one semiconductor chip **120** may be a bare semiconductor chip without a separate bump or interconnection layer, but is not limited thereto and the at least one semiconductor chip **120** may be a packaged-type semiconductor chip. The at least one semiconductor chip **120** may be electrically connected to the upper connection terminals **110**P2 through conductive bumps **128**. The conductive bumps **128** may include a pillar portion **124** and a solder portion **126**. The pillar portion **124** may include copper (Cu) or an alloy of copper (Cu), and the solder portion **126** may include a low melting point metal, for example, tin (Sn) or an alloy (Sn—Ag—Cu) including tin (Sn). According to one or more embodiments, the conductive bumps **128** may include only the pillar portion **124** or only the solder portion **126**. At least one semiconductor chip **120** may be a logic chip including a CPU, a GPU, an FPGA, an AP, a digital signal processor, a cryptographic processor, a microprocessor, a microcontroller, an analog-to-digital converter, an ASIC, and the like. According to one or more embodiments, the at least one semiconductor chip **120** may further include a memory chip including volatile memories, such as DRAM, SRAM and nonvolatile memories, such as PRAM, MRAM, RRAM, and flash memory.

[0073] According to one or more embodiments, the method of manufacturing a semiconductor package having improved reliability may be provided by introducing the release layer filling a space between the connection bumps.

[0074] Each of the embodiments provided in the above description is not excluded from being associated with one

or more features of another example or another embodiment also provided herein or not provided herein but consistent with the disclosure.

[0075] While the disclosure has been particularly shown and described with reference to embodiments thereof, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of the following claims.

1. A method of manufacturing a semiconductor package, the method comprising:
- preparing a molding structure on which connection bumps are provided;
- forming a release layer at least partially filling spaces between the connection bumps, wherein the release layer comprises a silicon (Si)-based polymer;
- forming an adhesive layer covering the release layer and the connection bumps;
- separating unit packages on which the release layer and the adhesive layer are formed by cutting the molding structure, the release layer, and the adhesive layer;
- attaching the unit packages to a base film by the adhesive layer, wherein the adhesive layer faces the base film;
- forming a shielding material layer covering at least a portion of each of the unit packages, at least a portion of the release layer, and at least a portion the adhesive layer;
- separating the unit packages covered with the shielding material layer from the release layer; and
- removing residue of the release layer that is on the unit packages using an etchant comprising at least one of fluorine ions, hydroxide ions, and hydrogen ions.

2. The method of claim **1**, wherein the unit packages are separated from the release layer while the release layer and the adhesive layer remain adhered to the base film.

3. The method of claim **1**, wherein the release layer comprises polydimethylsiloxane (PDMS) or cross-linked silicone polymer.

4. The method of claim **3**, wherein the release layer comprises polydimethylsiloxane (PDMS); and
- wherein the method further comprises surface-treating the molding structure and the connection bumps before forming the release layer.

5. The method of claim **4**, wherein a surface treatment layer between the release layer and the molding structure and between the release layer and the connection bumps comprises hexamethyldisiloxane (HMDS).

6. The method of claim **1**, wherein the release layer is formed by a spin coating process.

7. The method of claim **1**, wherein the release layer comprises a first portion at least partially filling spaces between connection bumps that are adjacent to each other and a second portion extending along a surface of at least a portion of each of the connection bumps.

8. (canceled)

9. The method of claim **7**, wherein a first thickness of the first portion of the release layer is at least half of a height of the connection bumps.

10. The method of claim **9**, wherein the height of the connection bumps ranges from about 180 μm to about 350 μm.

11. The method of claim **1**, wherein the adhesive layer comprises a thermosetting polymer or a photocurable polymer.

12. The method of claim **11**, wherein the adhesive layer comprises siloxane polymer or silicone acryl polymer.

13. (canceled)

14. The method of claim **1**, wherein the etchant comprises tetra-n-butylammonium fluoride (TBMF).

15. The method of claim **1**, wherein the molding structure comprises:
- a substrate strip;
- semiconductor chips provided on a first surface of the substrate strip; and
- a mold layer sealing the semiconductor chips, and
- wherein the connection bumps are provided on a second surface of the substrate strip.

16. The method of claim **1**, wherein each of the unit packages comprises:
- a package substrate separated from a substrate strip;
- a semiconductor chip; and
- a mold layer sealing the semiconductor chip and provided on an upper surface of the package substrate, and
- wherein the connection bumps are provided on a lower surface of the package substrate.

17. (canceled)

18. (canceled)

19. A method of manufacturing a semiconductor package, the method comprising:
- preparing a molding structure on which connection bumps are provided;
- forming a release layer at least partially filling spaces between the connection bumps;
- forming an adhesive layer covering the release layer and the connection bumps;
- separating unit packages on which the release layer and the adhesive layer are formed by cutting the molding structure, the release layer, and the adhesive layer;
- attaching the unit packages to a base film;
- forming a shielding material layer covering at least a portion of each of the unit packages, at least a portion of the release layer, and at least a portion of the adhesive layer; and
- separating the unit packages covered with the shielding material layer from the release layer,
- wherein the release layer comprises a first portion at least partially filling spaces between connection bumps that are adjacent to each other and a second portion at least partially covering a surface of each of the connection bumps, and
- wherein a first thickness of the first portion of the release layer is different from a second thickness of the second portion of the release layer.

20. (canceled)

21. The method of claim **20**, wherein each of the connection bumps comprise an upper region at least partially covered by the first portion of the release layer and a lower region at least partially covered by the second portion of the release layer,
- wherein a height of the upper region is equal to or greater than a height of the lower region, and
- wherein a third thickness of the adhesive layer is greater than the height of the lower region of the connection bumps.

22. The method of claim **19**, wherein the second portion of the release layer extends conformally along at least a portion of the surface of each of the connection bumps.

23. A method of manufacturing a semiconductor package, the method comprising:

preparing a molding structure on which connection bumps are provided;

forming a release layer at least partially filling spaces between the connection bumps;

forming an adhesive layer covering the release layer and the connection bumps;

separating unit packages on which the release layer and the adhesive layer are formed by cutting the molding structure, the release layer, and the adhesive layer;

attaching the unit packages to a base film;

forming a shielding material layer covering at least a portion of each of the unit packages, at least a portion of the release layer, and at least a portion of the adhesive layer; and

separating the unit packages covered with the shielding material layer from the release layer,

wherein the release layer comprises polydimethylsiloxane (PDMS) or cross-linked silicone polymer.

24. The method of claim **23**, wherein the adhesive layer comprises silicone acryl polymer.

25. The method of claim **23**, wherein the base film comprises polyimide (PI), polyethylene terephthalate (PET), or polyethylene-naphthalate (PEN).

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