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INJECTION LOCKED PHASE ROTATOR

Abstract

An injection locked ring oscillator (ILRO) system is disclosed. The ILRO system includes an ILRO circuit configured to receive a plurality of injection control signals and a phase control signal, and to generate a plurality of output clock signals; a phase detector circuit configured to receive the output clock signals and to generate a phase output signal based on phase differences of particular pairs of the output clock signals; and a phase to voltage circuit configured to receive the phase output signal from the phase detector circuit, and to generate the phase control signal based on the phase output signal, where the phase control signal presents a negative feedback phase signal to the ILRO circuit for the phase differences in the particular pairs of the output clock signals.

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Background/Summary

BACKGROUND

[0001] Conventional phase rotator circuits typically employ voltage-controlled oscillators (VCOs) or digital phase shifters, which often suffer from power consumption, speed, and precision issues. Injection-locked phase rotator circuits offer an innovative alternative by leveraging injection locking, where an external signal synchronizes the phase and frequency of an oscillator, enabling rapid and precise phase adjustments without VCOs' power consumption or digital phase shifters' complexity. These circuits are gaining attention for their potential to provide low-power, high-speed, and accurate phase control.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0003] FIG. **1** illustrates an injection locked phase rotator (ILPR) circuit according to some implementations.

[0004] FIG. **2** illustrates an ILPR decoder circuit according to some implementations.

[0005] FIG. **3** illustrates a portion of an injection locked ring oscillator (ILRO) circuit according to some implementations.

[0006] FIG. **4** illustrates a phase detector circuit according to some implementations.

[0007] FIG. **5** illustrates a phase to voltage circuit according to some implementations.

[0008] FIG. **6** illustrates a method of operating and ILPR circuit according to some implementations.

[0009] Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the implementations and are not necessarily drawn to scale. The edges of features drawn in the figures do not necessarily indicate the termination of the extent of the feature.

DETAILED DESCRIPTION OF ILLUSTRATIVE IMPLEMENTATIONS

[0010] The making and using of various implementations are discussed in detail below. It should be appreciated, however, that the various implementations described herein are applicable in a wide variety of specific contexts. The specific implementations discussed are merely illustrative of specific ways to make and use various implementations, and should not be construed in a limited scope. Throughout the discussion herein, unless otherwise specified, the same or similar reference numerals or labels in different figures refer to the same or similar component or signal.

[0011] Reference to “an implementation,” “one implementation,” “an embodiment,” or “one embodiment” in the framework of the present description is intended to indicate that a particular configuration, structure, or characteristic described in relation to the implementation/embodiment is included in at least one implementation/embodiment. Hence, phrases such as “in one implementation” or “in one embodiment” that may be present in one or more points of the present description do not necessarily refer to one and the same implementation/embodiment. Moreover, particular conformations, structures, or characteristics may be combined in any adequate way in one or more implementations/embodiments. The references used herein are provided merely for convenience and hence do not define the extent of protection or the scope of the implementations/embodiments.

[0012] Injection locked phase rotator circuits with a free-running injection-locked ring oscillator (ILRO) is a common way to implement injection locked phase rotator (ILPR) circuits. However, the ILPR circuits are sensitive to power, voltage, and temperature variation because there is no closed-loop frequency tracking over the power, voltage, and temperature variation. Some ILPR

circuits have closed-loop feedback using a digital assist engine to close the loop. However, this approach increases the complexity of the design.

[0013] The implementations discussed herein use an injection locked ring oscillator (ILRO) circuit having oscillator delay elements which have delays which are affected by a control voltage input. The control voltage input is generated based on phase differences in the output clocks in a feedback loop which optimizes the phase differences in the output clocks. In some implementations, the phase differences of output clocks separated by an of less than 90, 80, 70, 60, and 50 degrees are used. In some implementations, the phase differences of output clocks separated by 45 degrees, 22.5 degrees, 11.25 degrees, or another amount are used. In the example implementations discussed herein, the phase differences of output clocks separated by 45 degrees are used. Unless specified otherwise, the values of phase differences and phase angles disclosed herein are not limited to the exact value given and include some variation for component tolerances (e.g., phase difference of 45 degrees (within component tolerances)).

[0014] Accordingly, the implementations discussed herein provide analog-based techniques for maintaining high performance for frequency and phase control across power, voltage, and temperature variations.

[0015] FIG. **1** illustrates an injection locked phase rotator (ILPR) circuit **100** according to some implementations. ILPR circuit **100** generates eight output clock signals CK**0**, CK**45**, CK**90**, CK**135**, CK**180**, CK**225**, CK**270**, and CK**315**, which are separated by 45 degrees in phase. In the illustrated implementation, ILPR circuit **100** includes ILPR decoder circuit **110**, ILRO circuit **120**, phase detector circuit **130**, and phase to voltage circuit **140**.

[0016] ILPR decoder circuit **110** is configured to receive control signals and to generate injection control signals en_injo<2:0>, en_inj90<2:0>, en_inj180<2:0>, and en_inj270<2:0> based on the control signals. The injection control signals en_injo<2:0>, en_inj90<2:0>, en_inj180<2:0>, and en_inj270<2:0> are sequentially active, one at a time, in a repeating pattern. The active period of injection signal en_injo<2:0> sequentially follows the active period of injection signal en_inj270<2:0>. The active period of injection signal en_inj90<2:0> sequentially follows the active period of injection signal en_injo<2:0>. The active period of injection signal en_inj180<2:0> sequentially follows the active period of injection signal en_inj90<2:0>. The active period of injection signal en_inj270<2:0> sequentially follows the active period of injection signal en_inj180<2:0.

[0017] ILRO circuit **120** is configured to receive the injection control signals en_injo<2:0>, en_inj90<2:0>, en_inj180<2:0>, and en_inj270<2:0> from ILPR decoder circuit **110**, is configured to receive injection clocks INJ**0** and INJ**180**, and is configured to receive a phase control signal vcn. In addition, ILRO circuit **120** is configured to generate output clock signals CK**0**, CK**45**, CK**90**, CK**135**, CK**180**, CK**225**, CK**270**, and CK**315** based on the injection control signals from ILPR decoder circuit **110**, injection clocks INJ**0** and INJ**180**, and phase control signal vcn.

[0018] The injection clocks INJ**0** and INJ**180** are 180 degrees out of phase and define the frequency of the output clock signals CK**0**, CK**45**, CK**90**, CK**135**, CK**180**, CK**225**, CK**270**, and CK**315**. The injection control signals en_injo<2:0>, en_inj90<2:0>, en_inj180<2:0>, and en_inj270<2:0> define a magnitude or strength of the current injections which occur in response to the injection clocks INJ**0** and INJ**180**. The data defining the magnitude or strength of each of the injection control signals en_injo<2:0>, en_inj90<2:0>, en_inj180<2:0>, and en_inj270<2:0> is determined by a controller or processor or circuit. For example, a controller (or processor or circuit) can receive or process data that determines the magnitude or strength of each of the injection control signals. The controller can dynamically adjust the magnitude or strength of the control signals, based on predefined patterns, real-time feedback, external inputs (like sensors or user inputs), or the like, to control the current injections.

[0019] ILRO circuit **120** includes a number of delay elements having a circuit driving capacity which is influenced or determined by phase control signal von, which is generated by phase to

voltage circuit **140** in response to the phase output signal generated by phase detector circuit **130**.
[0020] Phase detector circuit **130** receives output clock signals CK**0**, CK**45**, CK**90**, CK**135**, CK**180**, CK**225**, CK**270**, and CK**315** from ILRO circuit **120**. In addition, phase detector circuit **130** generates a differential phase output signal for phase to voltage circuit **140** based on phase differences of pairs of output clock signals CK**0**, CK**45**, CK**90**, CK**135**, CK**180**, CK**225**, CK**270**, and CK**315**.
[0021] Phase to voltage circuit **140** receives the differential phase output signal from phase detector circuit **130**, and generates the phase control signal von based on the differential phase output signal.
[0022] In some implementations, phase differences between any of output clock signals CK**45** and CK**90**, output clock signals CK**135** and CK**180**, output clock signals CK**225** and CK**270**, and output clock signals CK**315** and CK**0**, cause the phase detector circuit **130** and the phase to voltage circuit **140** to cooperatively modify the phase control signal von such that the delay elements of ILRO circuit **120** have increased driving capacity. In some implementations, phase differences between any of output clock signals CK**0** and CK**45**, output clock signals CK**90** and CK**135**, output clock signals CK**180** and CK**225**, and output clock signals CK**270** and CK**315**, cause the phase detector circuit **130** and the phase to voltage circuit **140** to cooperatively modify the phase control signal von such that the delay elements of ILRO circuit **120** to have decreased driving capacity.
[0023] The combined effect of each of the listed pairs of output clock signals are represented in the phase control signal vcn such that the phase control signal vcn presents a negative feedback phase signal for both phase differences greater than 45 degrees and for phase differences less than 45 degrees. Therefore, phase differences greater than 45 degrees cause the delay elements to decrease their delay, and to, accordingly, reduce phase differences. Similarly, phase differences less than 45 degrees cause the delay elements to increase their delay, and to, accordingly increase phase differences. Therefore, after the loop settles, the phase differences are optimized to be equal to 45 degrees within component tolerances.
[0024] FIG. **2** illustrates an ILPR decoder circuit **200** according to some implementations. ILPR decoder circuit **200** may be used as ILPR decoder circuit **110** of FIG. **1**. ILPR decoder circuit **200** is configured to receive control signals and to generate injection control signals en_injo<2:0>, en_inj90<2:0>, en_inj180<2:0>, and en_inj270<2:0> based on the control signals.
[0025] For example, in this implementation, ILPR decoder circuit **200** is configured to receive an enable signal ENABLE, an injection data signal INJ DATA, a phase override enable signal OVRDEN, and an override data signal OVRDD. In addition, in the illustrated implementation, ILPR decoder circuit **200** is configured to receive a reset signal RESET, a counter enable signal CTREN, and a counter clock signal CTRCK. ILPR decoder circuit **200** comprises an AND gate **205**, two bit counter **210**, multiplexers **220**, a one hot decoder **230**, AND gate array **240**, and AND gate array **250**.
[0026] Two bit counter **210** includes two flip-flops which provide a count signal to multiplexers **220**. The two bit counter **210** is clocked by counter clock signal CTRCK conditioned by counter enable signal CTREN by AND gate **205**. The two bit counter **210** is reset, for example, to 00 in response to the reset signal RESET being active. In response to the reset signal RESET being inactive and, for example, to rising edges of the counter clock signal CTRCK, the two bit counter **210** counts.
[0027] Multiplexers **220** receive the count from the two bit counter as first input data, and receive override data signal OVRDD as second input data. Multiplexers **220** pass either the first input data or the second input data to one hot decoder **230**, according to the logic state of the phase override enable signal OVRDEN.
[0028] One hot decoder **230** receives the two bit output of multiplexers **220**, and decodes the two bits to generate a four bit output, where one of the four output bits is active, and where which of the four bits is active corresponds with the received two bit output of multiplexers **220**. For example, if the two bit output of multiplexers **220** are 00, 01, 10, and 11, the respective outputs of one hot

decoder **230** may be 0001, 0010, 0100, and 1000.
[0029] AND gate array **240** comprises 12 AND gates organized as four sets of three two bit AND gates. The AND gates of each of the four sets receives a corresponding one of the four output bits of the one hot decoder **230**. In addition, the AND gates of each of the four sets receives one of the three bits of the injection data signal INJ DATA.
[0030] Accordingly, AND gate array **240** generates **12** output bits logically organized as four sets of three output bits. One of the four sets of three output bits is equal to the three bits of the injection data signal INJ DATA, and the other three of the four sets of three output bits is equal to 0. Which one of the four sets of three output bits is equal to the three bits of the injection data signal INJ DATA is determined by the one hot decoder **230** based on the count received from the two bit counter.
[0031] AND gate array **250** includes 12 two bit AND gates, each receiving an output of one of the AND gates of AND gate array **240**. Each of the 12 two bit AND gates of AND gate array **250** also receives the enable signal ENABLE. Accordingly, AND gate array **250** generates **12** output bits, and when the enable signal ENABLE is active, one of the four sets of three output bits is equal to the three bits of the injection data signal INJ DATA, and the other three of the four sets of three output bits is equal to 0. Which one of the four sets of three output bits is equal to the three bits of the injection data signal INJ DATA is determined by the one hot decoder **230** based on the count received from the two bit counter. When the enable signal ENABLE is inactive, all 12 bits of the output of AND gate array **250** are 0.
[0032] FIG. **3** illustrates a portion of an injection locked ring oscillator (ILRO) circuit **300** according to some implementations. ILRO circuit **300** may be used as ILRO circuit **120** of FIG. **1**. ILRO circuit **300** includes delay elements **310**, clock buffers **320**, injection drivers **330**, and dummy injection drivers **340**.
[0033] ILRO circuit **300** is configured to receive injection control signals en_injo<2:0>, en_inj90<2:0>, en_inj180<2:0>, and en_inj270<2:0> from an ILPR decoder circuit, such as ILPR decoder circuit **200**. In addition, ILRO circuit **300** is configured to receive injection clocks INJ**0** and INJ**180**, and is configured to receive a phase control signal vcn. Furthermore, ILRO circuit **300** is configured to generate output clock signals CK**0**, CK**45**, CK**90**, CK**135**, CK**180**, CK**225**, CK**270**, and CK**315** based on the injection control signals from ILPR decoder circuit **110**, injection clocks INJ**0** and INJ**180**, and phase control signal vcn.
[0034] Delay elements **310** and injection drivers **330** form an injection locked ring oscillator circuit, which operates based on delay times of the delay elements **310** and based on injection signals from injection drivers **330**. The injection signals are generated based on injection control signals en_injo<2:0>, en_inj90<2:0>, en_inj180<2:0>, and en_inj270<2:0>. The delay times of the delay elements **310** are influenced by the phase control signal ven. For example, a detailed implementation of a delay element **310** is shown and illustrates an example of the effect of phase control signal vcn.
[0035] The injection clocks INJ**0** and INJ**180** are 180 degrees out of phase and define the frequency of the output clock signals CK**0**, CK**45**, CK**90**, CK**135**, CK**180**, CK**225**, CK**270**, and CK**315**. The injection clocks INJ**0** and INJ**180** are aligned with the injection control signals en_injo<2:0>, en_inj90<2:0>, en_inj180<2:0>, and en_inj270<2:0>, such that the injection control signals en_injo<2:0>, en_inj90<2:0>, en_inj180<2:0>, and en_inj270<2:0> define a magnitude or strength of the current injections which occur in response to the injection clocks INJ**0** and INJ**180**.
[0036] Dummy injection drivers **340** have structure similar or identical to injection drivers **330**, but do not function to generate injection signals. However dummy injection drivers **340** present loads which are similar or identical to injection drivers **330**.
[0037] FIG. **4** illustrates a phase detector circuit **400** according to some implementations. Phase detector circuit **400** may be used, for example, as phase detector circuit **130** of FIG. **1**. In this implementation, phase detector circuit **400** includes eight mixers **410**.

[0038] Phase detector circuit **400** receives output clock signals CK**0**, CK**45**, CK**90**, CK**135**, CK**180**, CK**225**, CK**270**, and CK**315** and generates a differential phase output signal (up-dn) based on phase differences of pairs of the output clock signals CK**0**, CK**45**, CK**90**, CK**135**, CK**180**, CK**225**, CK**270**, and CK**315**.
[0039] In the illustrated implementation, phase differences between any of output clock signals CK**45** and CK**90**, output clock signals CK**135** and CK**180**, output clock signals CK**225** and CK**270**, and output clock signals CK**315** and CK**0**, cause the phase detector circuit **400** to increase the differential phase output signal. In the illustrated implementation, phase differences between any of output clock signals CK**0** and CK**45**, output clock signals CK**90** and CK**135**, output clock signals CK**180** and CK**225**, and output clock signals CK**270** and CK**315**, cause the phase detector circuit **400** to decrease the differential phase output signal.
[0040] FIG. **5** illustrates a phase to voltage circuit **500** according to some implementations. Phase to voltage circuit **500** may be used, for example, as phase to voltage circuit **140** of FIG. **1**. Phase to voltage circuit **500** includes voltage to current circuit **510**, and capacitor **520**. Phase to voltage circuit **500** is configured to receive a differential phase output signal, and to generate a phase control signal vcn based on the differential phase output signal.
[0041] Voltage to current circuit **510** may be any voltage to current circuit known in the art. For example, voltage to current circuit **510** may be configured to generate a current substantially equal to a constant times a difference between the up and dn input signals. Accordingly, in response to the up signal being greater than the dn signal, the output current from the voltage to current circuit **510** is greater than 0, and, in response to the up signal being less than the dn signal, the output current from the voltage to current circuit **510** is less than 0.
[0042] The voltage of capacitor **520** (equal to the phase control signal vcn), represents an integration of the current output of the voltage to current circuit **510**. Accordingly, in response to the up signal being greater than the dn signal, the output current from the voltage to current circuit **510** is greater than 0 and the phase control signal von increases, and, in response to the up signal being less than the dn signal, the output current from the voltage to current circuit **510** is less than 0 and the phase control signal von decreases.
[0043] FIG. **6** illustrates a method **600** of operating an ILPR circuit according to some implementations. For example, ILPR circuit **100** may operate according to method **600**.
[0044] At block **610**, the ILPR circuit generates eight output clock signals separated by 45 degrees. For example, the ILPR circuit may generate eight output clock signals, such as CK**0**, CK**45**, CK**90**, CK**135**, CK**180**, CK**225**, CK**270**, and CK**315** generated by ILPR circuit **100**. The eight output clock signals may be generated based on injection signals, and based on a control signal, where the control signal influences a delay of a plurality of delay elements of an ILRO circuit of the ILPR circuit.
[0045] At block **620**, a phase error signal may be generated based on the eight output clock signals. For example, a differential phase signal may be generated based on particular pairs of the output clocks. For example, phase differences between any of output clock signals CK**45** and CK**90**, output clock signals CK**135** and CK**180**, output clock signals CK**225** and CK**270**, and output clock signals CK**315** and CK**0**, may cause the differential phase signal to increase, and phase differences between any of output clock signals CK**0** and CK**45**, output clock signals CK**90** and CK**135**, output clock signals CK**180** and CK**225**, and output clock signals CK**270** and CK**315**, may cause the differential phase signal to decrease.
[0046] At block **630**, the control signal used at block **610** to generate the eight output clock signals is adjusted based on the phase error signal generated at block **620**. For example, in response to the differential phase signal increasing, the control signal may be increased, and, in response to the differential phase signal decreasing, the control signal may be decreased.
[0047] The combined effect of each of the listed pairs of output clock signals are represented in the phase control signal von such that the phase control signal von presents a negative feedback phase

signal for both phase differences greater than 45 degrees and for phase differences less than 45 degrees. By injecting the ILRO circuit at 90 degrees phase separation, and using 45 degree as the reference plane for the phase error detection, the phase detector output can maintain the same polarity at all times while rotating the phase. The phase error is consistent when the phase control signal von rotates the injection phase, and the polarity at the phase detector output doesn't vary with the injection phase. Accordingly, phase differences greater than 45 degrees cause the delay elements to decrease their delay, and to, accordingly, reduce the phase differences. Similarly, phase differences less than 45 degrees cause the delay elements to increase their delay, and to, accordingly increase the phase differences. Therefore, after the loop settles, the phase differences are optimized to be equal to 45 degrees within component tolerances.

[0048] One general aspect is an injection locked ring oscillator (ILRO) system, including an ILRO circuit configured to receive a plurality of injection control signals and a phase control signal, and to generate a plurality of output clock signals; a phase detector circuit configured to receive the output clock signals and to generate a phase output signal based on phase differences of particular pairs of the output clock signals; and a phase to voltage circuit configured to receive the phase output signal from the phase detector circuit, and to generate the phase control signal based on the phase output signal, where the phase control signal presents a negative feedback phase signal to the ILRO circuit for the phase differences in the particular pairs of the output clock signals.

[0049] Implementations may include one or more of the following features. The ILRO system, where the phase control signal presents the negative feedback phase signal to the ILRO circuit both for phase differences greater than 45 degrees in the particular pairs of the output clock signals and for phase differences less than 45 degrees in the particular pairs of the output clock signals. The ILRO system, where the output clock signals include eight output clock signals, where a first output clock has an about 0 degree phase, a second clock has an about 45 degree phase, a third clock has an about 90 degree phase, a fourth clock has an about 135 degree phase, a fifth clock has an about 180 degree phase, a six clock has an about 225 degree phase, a seventh clock has an about 270 degree phase, and an eighth clock has an about 315 degree phase, where the phase control signal is generated based on phase differences of the first and second clocks, the second and third clocks, the third and fourth clocks, the fourth and fifth clocks, the fifth and sixth clocks, the sixth and seventh clocks, the seventh and eighth clocks, and the eighth and first clocks. The ILRO system, where the ILRO circuit includes a plurality of delay components, and where the phase differences of the first and second clocks, the third and fourth clocks, the fifth and sixth clocks, and the seventh and eighth clocks cause the phase control signal to increase a delay of the delay components. The ILRO system, where the ILRO circuit includes a plurality of delay elements, and where the phase differences of the second and third clocks, the fourth and fifth clocks, the sixth and seventh clocks, and the eighth and first clocks cause the phase control signal to decrease a delay of the delay components. The ILRO system, where the ILRO circuit includes a plurality of delay components, and where changes in the phase differences of the first and second clocks, the third and fourth clocks, the fifth and sixth clocks, and the seventh and eighth clocks change a current, where the change in the current causes the phase control signal to decrease a delay of the delay components. The ILRO system, where the ILRO circuit includes a plurality of delay components, and where changes in the phase differences of the second and third clocks, the fourth and fifth clocks, the sixth and seventh clocks, and the eighth and first clocks change a current, where the change in the current causes the phase control signal to increase a delay of the delay components.

[0050] Another general aspect is an injection locked phase rotator (ILPR) circuit, including an ILPR decoder circuit configured to generate a plurality of injection control signals; an injection locked ring oscillator (ILRO) circuit configured to receive the injection control signals and a phase control signal, and configured to generate a plurality of output clock signals; a phase detector circuit configured to receive the output clock signals and to generate a phase output signal based on phase differences of particular pairs of the output clock signals separated by 45 degrees or less; and

a phase to voltage circuit configured to receive the phase output signal, and to generate the phase control signal based on the phase output signal.

[0051] Implementations may include one or more of the following features. The ILPR circuit, where the phase control signal presents a negative feedback phase signal to the ILRO circuit both for phase differences greater than 45 degrees in the particular pairs of the output clock signals and for phase differences less than 45 degrees in the particular pairs of the output clock signals. The ILPR circuit, where the output clock signals include eight output clock signals, where a first output clock has an about 0 degree phase, a second clock has an about 45 degree phase, a third clock has an about 90 degree phase, a fourth clock has an about 135 degree phase, a fifth clock has an about 180 degree phase, a six clock has an about 225 degree phase, a seventh clock has an about 270 degree phase, and an eighth clock has an about 315 degree phase, where the phase control signal is generated based on phase differences of the first and second clocks, the second and third clocks, the third and fourth clocks, the fourth and fifth clocks, the fifth and sixth clocks, the sixth and seventh clocks, the seventh and eighth clocks, and the eighth and first clocks. The ILPR circuit, where the ILRO circuit includes a plurality of delay components, and where the phase differences of the first and second clocks, the third and fourth clocks, the fifth and sixth clocks, and the seventh and eighth clocks cause the phase control signal to increase a delay of the delay components. The ILPR circuit, where the ILRO circuit includes a plurality of delay components, and where the phase differences of the second and third clocks, the fourth and fifth clocks, the sixth and seventh clocks, and the eighth and first clocks cause the phase control signal to decrease a delay of the delay components. The ILPR circuit, where the ILRO circuit includes a plurality of delay components, and where changes in the phase differences of the first and second clocks, the third and fourth clocks, the fifth and sixth clocks, and the seventh and eighth clocks change a current, where the change in the current causes the phase control signal to decrease a delay of the delay components. The ILPR circuit, where the ILRO circuit includes a plurality of delay components, and where changes in the phase differences of the second and third clocks, the fourth and fifth clocks, the sixth and seventh clocks, and the eighth and first clocks change a current, where the change in the current causes the phase control signal to increase a delay of the delay components.

[0052] Another general aspect is a method of operating an injection locked phase rotator (ILPR) circuit, the method including, with an ILPR decoder circuit, generating a plurality of injection control signals; with an injection locked ring oscillator (ILRO) circuit, receiving the injection control signals from the ILPR decoder circuit; with the ILRO circuit, receiving injection clocks; with the ILRO circuit, receiving a phase control signal; with the ILRO circuit, generating a plurality of output clock signals based on the injection control signals, the injection clocks, and the phase control signal; with a phase detector circuit, receiving the output clock signals; with the phase detector circuit, generating a phase output signal based on phase differences of particular pairs of the output clock signals, where the particular pairs of the output clock signals are separated by 45 degrees or less; with a phase to voltage circuit, receiving the phase output signal from the phase detector circuit; and with the phase to voltage circuit, generating the phase control signal based on the phase output signal.

[0053] Implementations may include one or more of the following features. The method, where the phase control signal presents a negative feedback phase signal to the ILRO circuit both for phase differences greater than 45 degrees in the particular pairs of the output clock signals and for phase differences less than 45 degrees in the particular pairs of the output clock signals. The method, where the output clock signals include eight output clock signals, where a first output clock has an about 0 degree phase, a second clock has an about 45 degree phase, a third clock has an about 90 degree phase, a fourth clock has an about 135 degree phase, a fifth clock has an about 180 degree phase, a six clock has an about 225 degree phase, a seventh clock has an about 270 degree phase, and an eighth clock has an about 315 degree phase, where the phase control signal is generated based on phase differences of the first and second clocks, the second and third clocks, the third and

fourth clocks, the fourth and fifth clocks, the fifth and sixth clocks, the sixth and seventh clocks, the seventh and eighth clocks, and the eighth and first clocks. The method, where the ILRO circuit includes a plurality of delay components, and where the phase differences of the first and second clocks, the third and fourth clocks, the fifth and sixth clocks, and the seventh and eighth clocks cause the phase control signal to increase a delay of the delay components. The method, where the ILRO circuit includes a plurality of delay components, and where the phase differences of the second and third clocks, the fourth and fifth clocks, the sixth and seventh clocks, and the eighth and first clocks cause the phase control signal to decrease a delay of the delay components. The method, where the ILRO circuit includes a plurality of delay components, and where changes in the phase differences of the first and second clocks, the third and fourth clocks, the fifth and sixth clocks, and the seventh and eighth clocks change a current, where the change in the current causes the phase control signal to decrease a delay of the delay components.

[0054] While this invention has been described with reference to illustrative implementations, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative implementations, as well as other implementations of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or implementations.

Claims

1. An injection locked ring oscillator (ILRO) system, comprising: an ILRO circuit configured to receive a plurality of injection control signals and a phase control signal, and to generate a plurality of output clock signals; a phase detector circuit configured to receive the output clock signals and to generate a phase output signal based on phase differences of particular pairs of the output clock signals; and a phase to voltage circuit configured to receive the phase output signal from the phase detector circuit, and to generate the phase control signal based on the phase output signal, wherein the phase control signal presents a negative feedback phase signal to the ILRO circuit for the phase differences in the particular pairs of the output clock signals.

2. The ILRO system of claim 1, wherein the phase control signal presents the negative feedback phase signal to the ILRO circuit both for phase differences greater than 45 degrees in the particular pairs of the output clock signals and for phase differences less than 45 degrees in the particular pairs of the output clock signals.

3. The ILRO system of claim 1, wherein the output clock signals comprise eight output clock signals, wherein a first output clock has an about 0 degree phase, a second clock has an about 45 degree phase, a third clock has an about 90 degree phase, a fourth clock has an about 135 degree phase, a fifth clock has an about 180 degree phase, a six clock has an about 225 degree phase, a seventh clock has an about 270 degree phase, and an eighth clock has an about 315 degree phase, wherein the phase control signal is generated based on phase differences of the first and second clocks, the second and third clocks, the third and fourth clocks, the fourth and fifth clocks, the fifth and sixth clocks, the sixth and seventh clocks, the seventh and eighth clocks, and the eighth and first clocks.

4. The ILRO system of claim 3, wherein the ILRO circuit comprises a plurality of delay components, and wherein the phase differences of the first and second clocks, the third and fourth clocks, the fifth and sixth clocks, and the seventh and eighth clocks cause the phase control signal to increase a delay of the delay components.

5. The ILRO system of claim 3, wherein the ILRO circuit comprises a plurality of delay elements, and wherein the phase differences of the second and third clocks, the fourth and fifth clocks, the sixth and seventh clocks, and the eighth and first clocks cause the phase control signal to decrease a delay of the delay components.

6. The ILRO system of claim 3, wherein the ILRO circuit comprises a plurality of delay

components, and wherein changes in the phase differences of the first and second clocks, the third and fourth clocks, the fifth and sixth clocks, and the seventh and eighth clocks change a current, wherein the change in the current causes the phase control signal to decrease a delay of the delay components.

7. The ILRO system of claim 3, wherein the ILRO circuit comprises a plurality of delay components, and wherein changes in the phase differences of the second and third clocks, the fourth and fifth clocks, the sixth and seventh clocks, and the eighth and first clocks change a current, wherein the change in the current causes the phase control signal to increase a delay of the delay components.

8. An injection locked phase rotator (ILPR) circuit, comprising: an ILPR decoder circuit configured to generate a plurality of injection control signals; an injection locked ring oscillator (ILRO) circuit configured to receive the injection control signals and a phase control signal, and configured to generate a plurality of output clock signals; a phase detector circuit configured to receive the output clock signals and to generate a phase output signal based on phase differences of particular pairs of the output clock signals separated by 45 degrees or less; and a phase to voltage circuit configured to receive the phase output signal, and to generate the phase control signal based on the phase output signal.

9. The ILPR circuit of claim 8, wherein the phase control signal presents a negative feedback phase signal to the ILRO circuit both for phase differences greater than 45 degrees in the particular pairs of the output clock signals and for phase differences less than 45 degrees in the particular pairs of the output clock signals.

10. The ILPR circuit of claim 8, wherein the output clock signals comprise eight output clock signals, wherein a first output clock has an about 0 degree phase, a second clock has an about 45 degree phase, a third clock has an about 90 degree phase, a fourth clock has an about 135 degree phase, a fifth clock has an about 180 degree phase, a six clock has an about 225 degree phase, a seventh clock has an about 270 degree phase, and an eighth clock has an about 315 degree phase, wherein the phase control signal is generated based on phase differences of the first and second clocks, the second and third clocks, the third and fourth clocks, the fourth and fifth clocks, the fifth and sixth clocks, the sixth and seventh clocks, the seventh and eighth clocks, and the eighth and first clocks.

11. The ILPR circuit of claim 10, wherein the ILRO circuit comprises a plurality of delay components, and wherein the phase differences of the first and second clocks, the third and fourth clocks, the fifth and sixth clocks, and the seventh and eighth clocks cause the phase control signal to increase a delay of the delay components.

12. The ILPR circuit of claim 10, wherein the ILRO circuit comprises a plurality of delay components, and wherein the phase differences of the second and third clocks, the fourth and signal to decrease a delay of the delay components.

13. The ILPR circuit of claim 10, wherein the ILRO circuit comprises a plurality of delay components, and wherein changes in the phase differences of the first and second clocks, the third and fourth clocks, the fifth and sixth clocks, and the seventh and eighth clocks change a current, wherein the change in the current causes the phase control signal to decrease a delay of the delay components.

14. The ILPR circuit of claim 10, wherein the ILRO circuit comprises a plurality of delay components, and wherein changes in the phase differences of the second and third clocks, the fourth and fifth clocks, the sixth and seventh clocks, and the eighth and first clocks change a current, wherein the change in the current causes the phase control signal to increase a delay of the delay components.

1. A method of operating an injection locked phase rotator (ILPR) circuit, the method comprising: with an ILPR decoder circuit, generating a plurality of injection control signals; with an injection locked ring oscillator (ILRO) circuit, receiving the injection control signals from the ILPR decoder

circuit; with the ILRO circuit, receiving injection clocks; with the ILRO circuit, receiving a phase control signal; with the ILRO circuit, generating a plurality of output clock signals based on the injection control signals, the injection clocks, and the phase control signal; with a phase detector circuit, receiving the output clock signals; with the phase detector circuit, generating a phase output signal based on phase differences of particular pairs of the output clock signals, wherein the particular pairs of the output clock signals are separated by 45 degrees or less; with a phase to voltage circuit, receiving the phase output signal from the phase detector circuit; and with the phase to voltage circuit, generating the phase control signal based on the phase output signal.

2. The method of claim **15**, wherein the phase control signal presents a negative feedback phase signal to the ILRO circuit both for phase differences greater than 45 degrees in the particular pairs of the output clock signals and for phase differences less than 45 degrees in the particular pairs of the output clock signals.

3. The method of claim **15**, wherein the output clock signals comprise eight output clock signals, wherein a first output clock has an about 0 degree phase, a second clock has an about 45 degree phase, a third clock has an about 90 degree phase, a fourth clock has an about 135 degree phase, a fifth clock has an about 180 degree phase, a six clock has an about 225 degree phase, a seventh clock has an about 270 degree phase, and an eighth clock has an about 315 degree phase, wherein the phase control signal is generated based on phase differences of the first and second clocks, the second and third clocks, the third and fourth clocks, the fourth and fifth clocks, the fifth and sixth clocks, the sixth and seventh clocks, the seventh and eighth clocks, and the eighth and first clocks.

4. The method of claim **17**, wherein the ILRO circuit comprises a plurality of delay components, and wherein the phase differences of the first and second clocks, the third and fourth clocks, the fifth and sixth clocks, and the seventh and eighth clocks cause the phase control signal to increase a delay of the delay components.

5. The method of claim **17**, wherein the ILRO circuit comprises a plurality of delay components, and wherein the phase differences of the second and third clocks, the fourth and signal to decrease a delay of the delay components.

6. The method of claim **17**, wherein the ILRO circuit comprises a plurality of delay components, and wherein changes in the phase differences of the first and second clocks, the third and fourth clocks, the fifth and sixth clocks, and the seventh and eighth clocks change a current, wherein the change in the current causes the phase control signal to decrease a delay of the delay components.