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(54) **DISPLAY PANEL, DRIVING METHOD AND DISPLAY DEVICE**

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(21) Appl. No.: **19/193,853**

(22) Filed: **Apr. 29, 2025**

Related U.S. Application Data

(63) Continuation of application No. 18/202,528, filed on May 26, 2023, now Pat. No. 12,307,949, which is a continuation of application No. 17/103,329, filed on Nov. 24, 2020, now abandoned.

(30) **Foreign Application Priority Data**

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G09G 3/32 (2016.01)

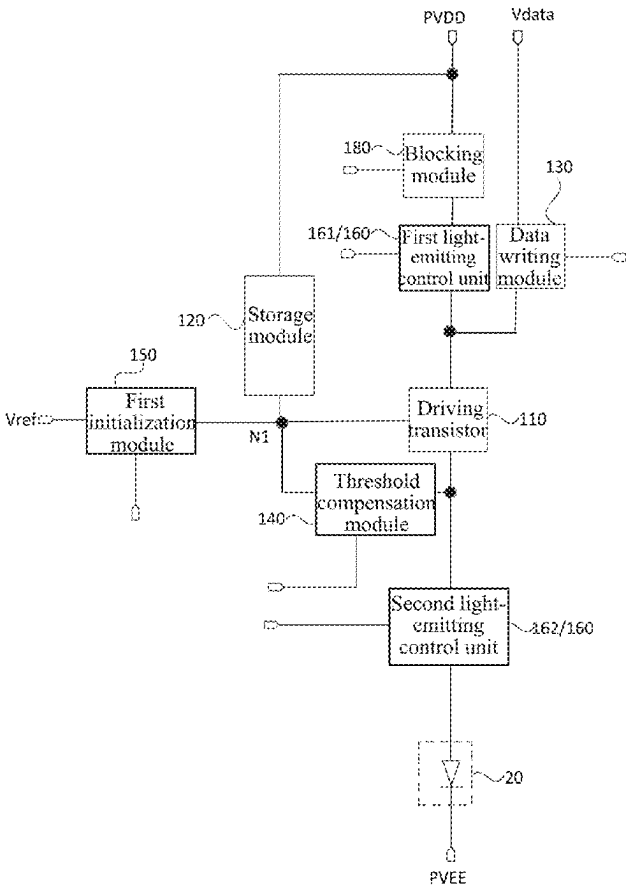
G09G 3/20 (2006.01)

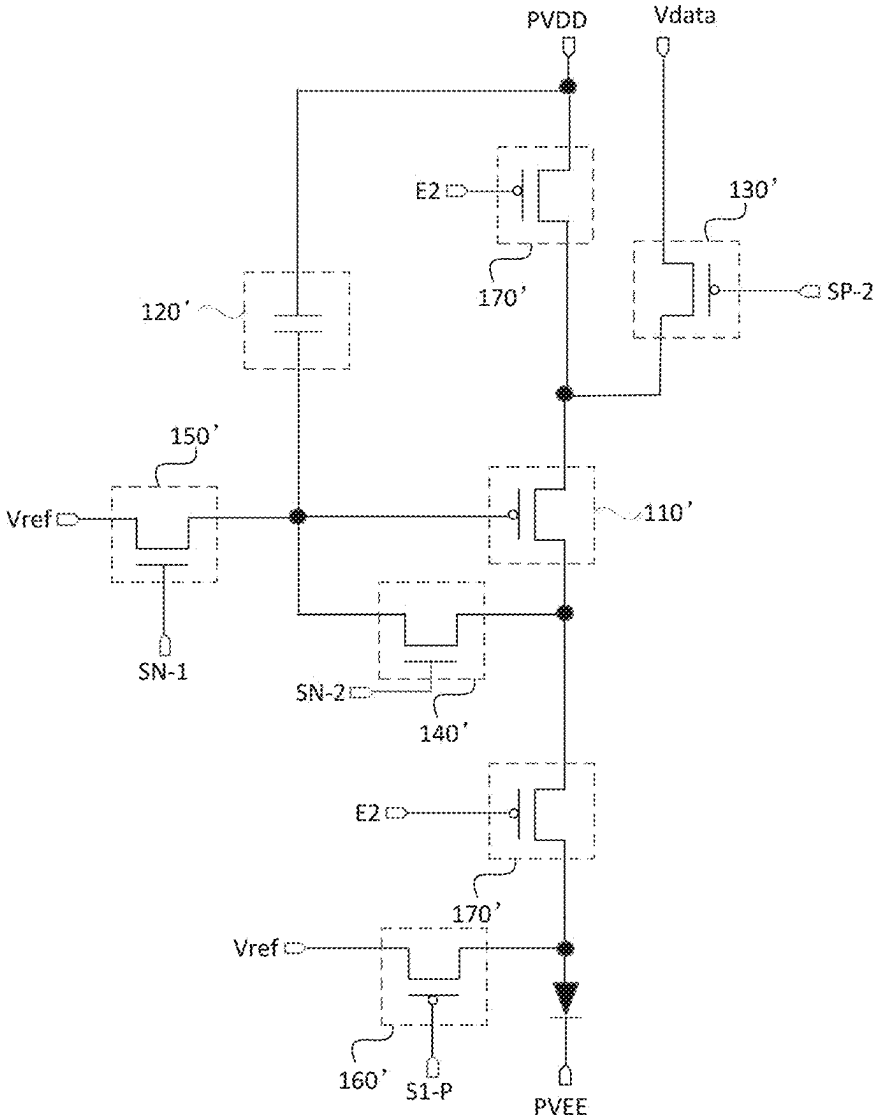
(52) **U.S. Cl.**

CPC ***G09G 3/32*** (2013.01); ***G09G 3/2092*** (2013.01); *G09G 2310/0275* (2013.01); *G09G 2330/028* (2013.01)

(57) **ABSTRACT**

Provided are a display panel, a driving method, and a display device. The display panel includes: a gate driving circuit, a pixel driving circuit, and a light-emitting component. The pixel driving circuit includes a driving transistor, a data writing module, a threshold compensation module, and a light-emitting control module. A control terminal of the threshold compensation module and a control terminal of the light-emitting control module are electrically connected to a same gate driving circuit. The light-emitting control module includes a first light-emitting control unit and a second light-emitting control unit. The pixel driving circuit further comprises a blocking module which is electrically connected between the first power signal terminal and the first terminal of the driving transistor, and is connected in series to the first light-emitting control unit.





--Prior Art--

FIG. 1

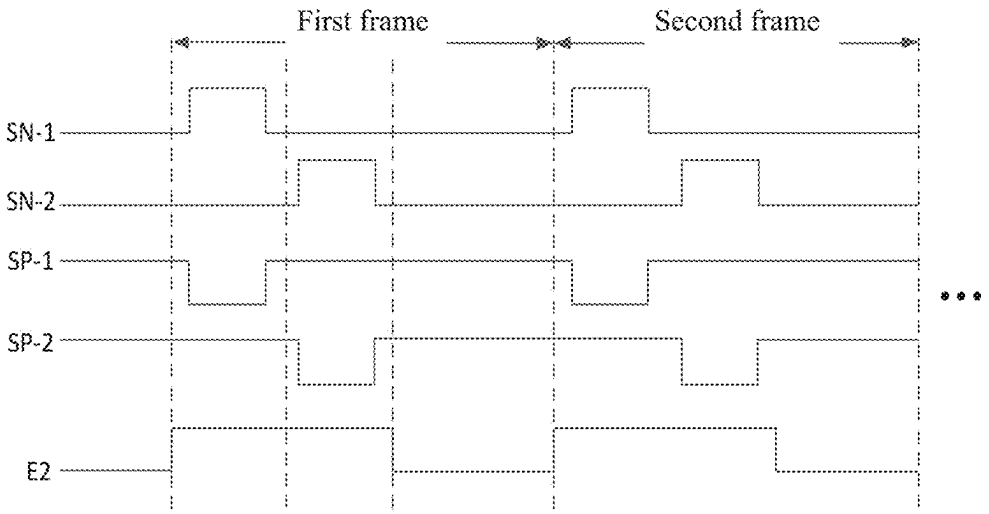


FIG. 2

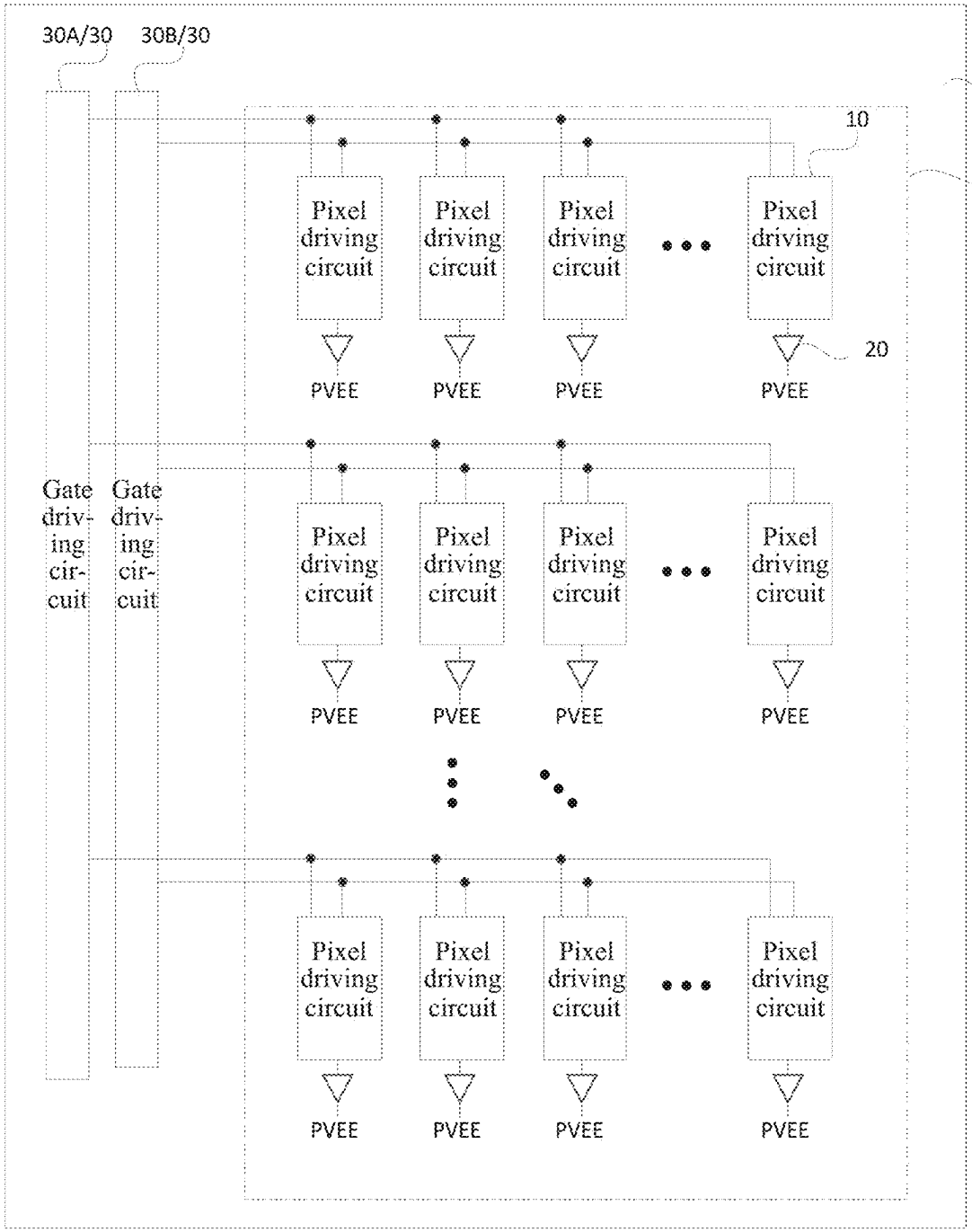

30A/30
30B/30
DA
10
AA
Pixel driving circuit
PVEE
20
Gate driving circuit
Gate driving circuit

FIG. 3

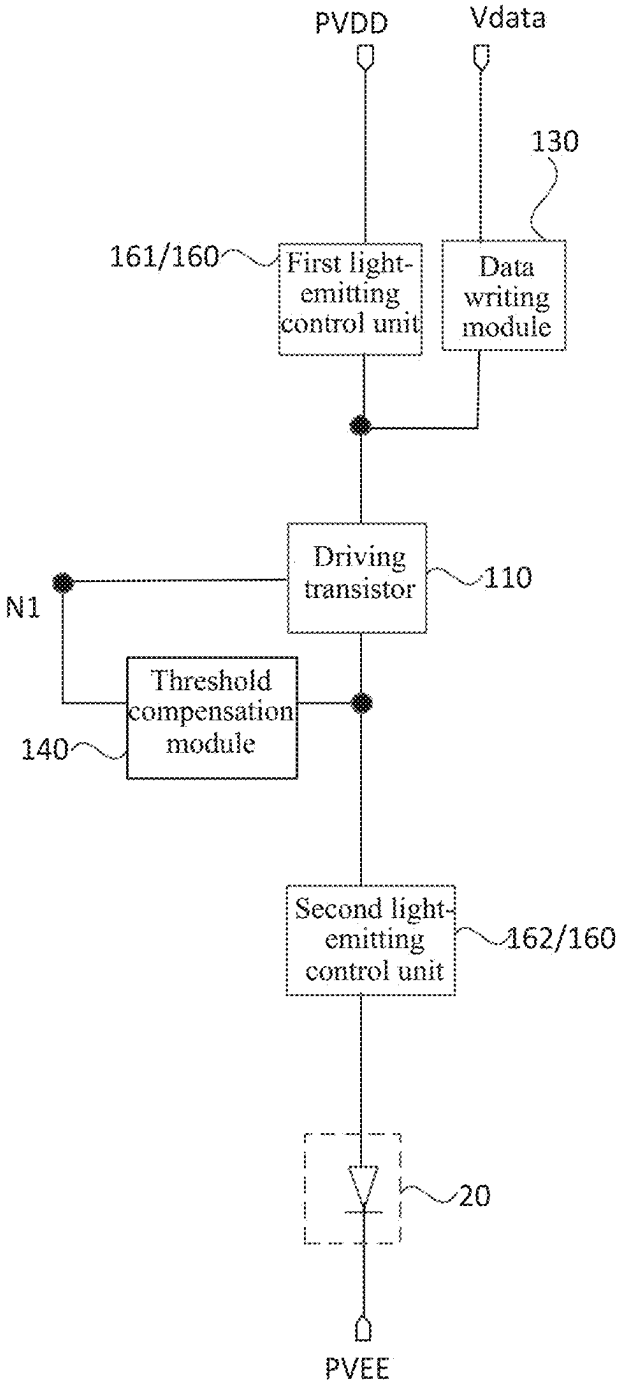

PVDD
Vdata
130
161/160
First light-emitting control unit
Data writing module
Driving transistor
110
N1
Threshold compensation module
140
Second light-emitting control unit
162/160
20
PVEE

FIG. 4

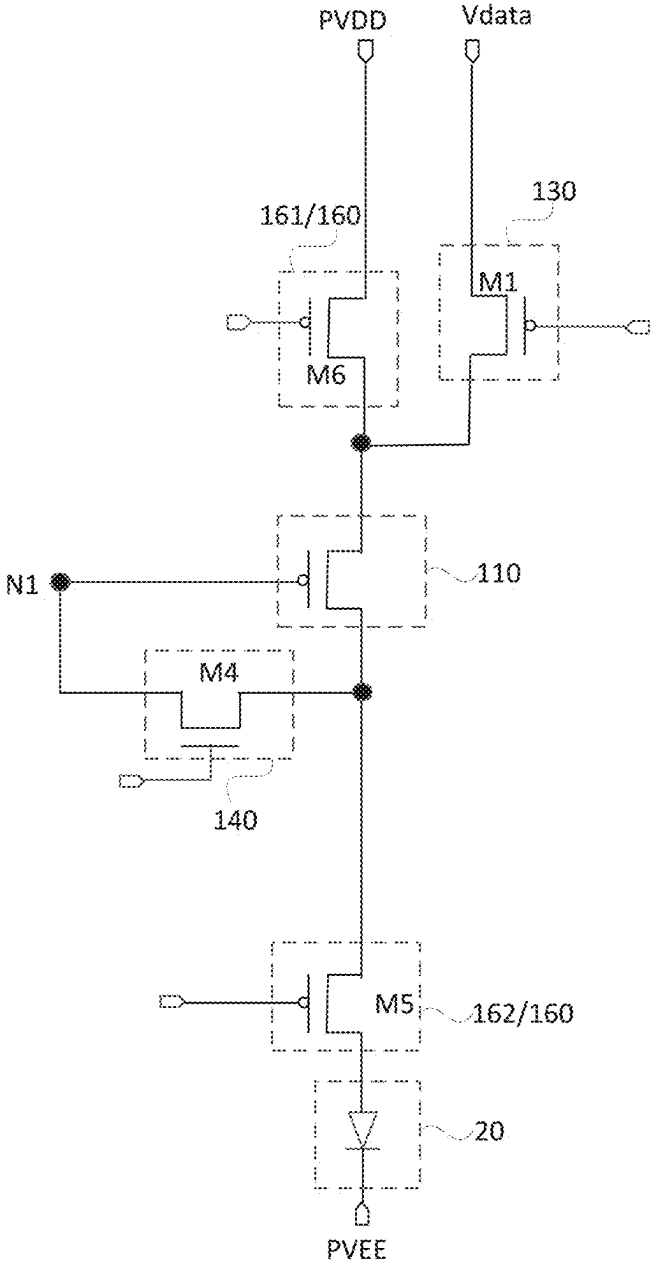


FIG. 5

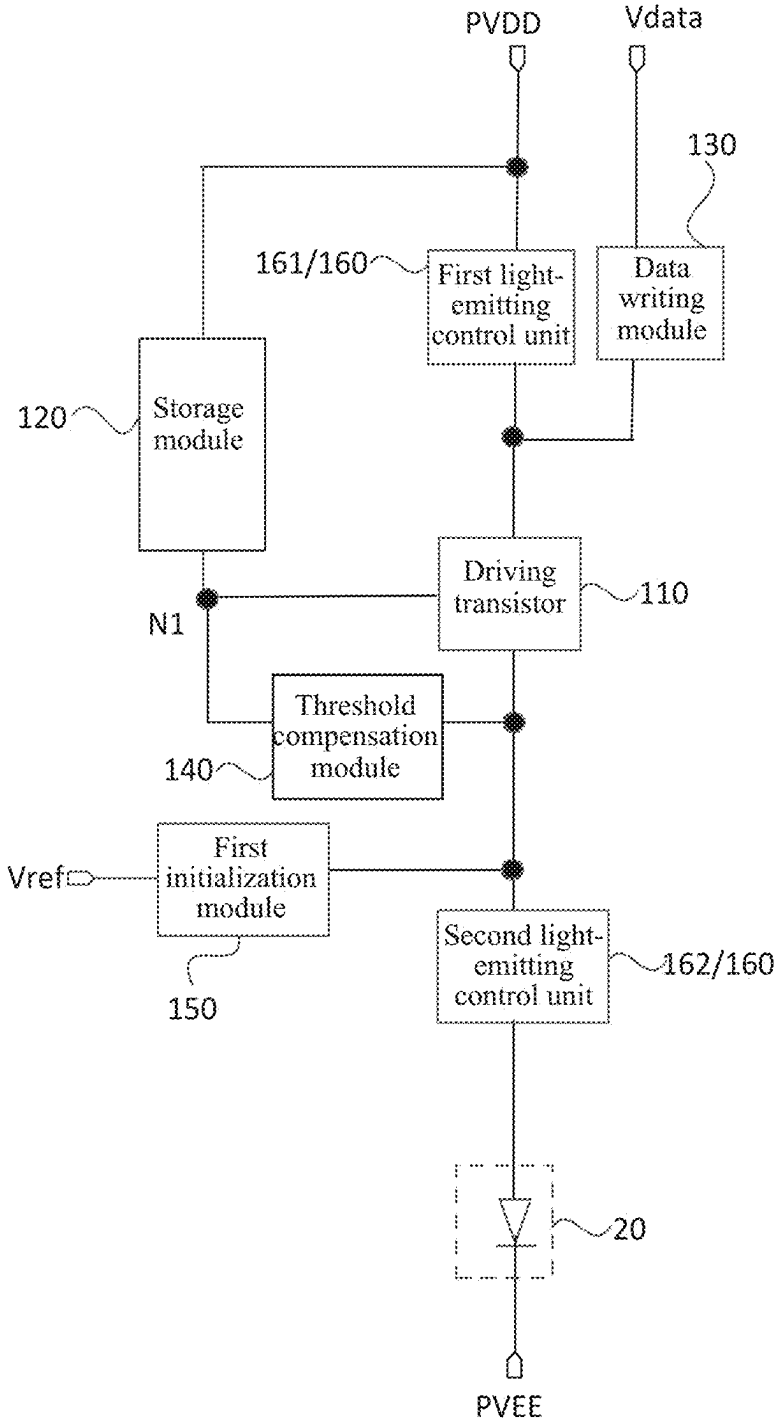

PVDD
Vdata
130
161/160
First light-emitting control unit
Data writing module
120
Storage module
Driving transistor
110
N1
Threshold compensation module
140
Vref
First initialization module
150
Second light-emitting control unit
162/160
20
PVEE

FIG. 6

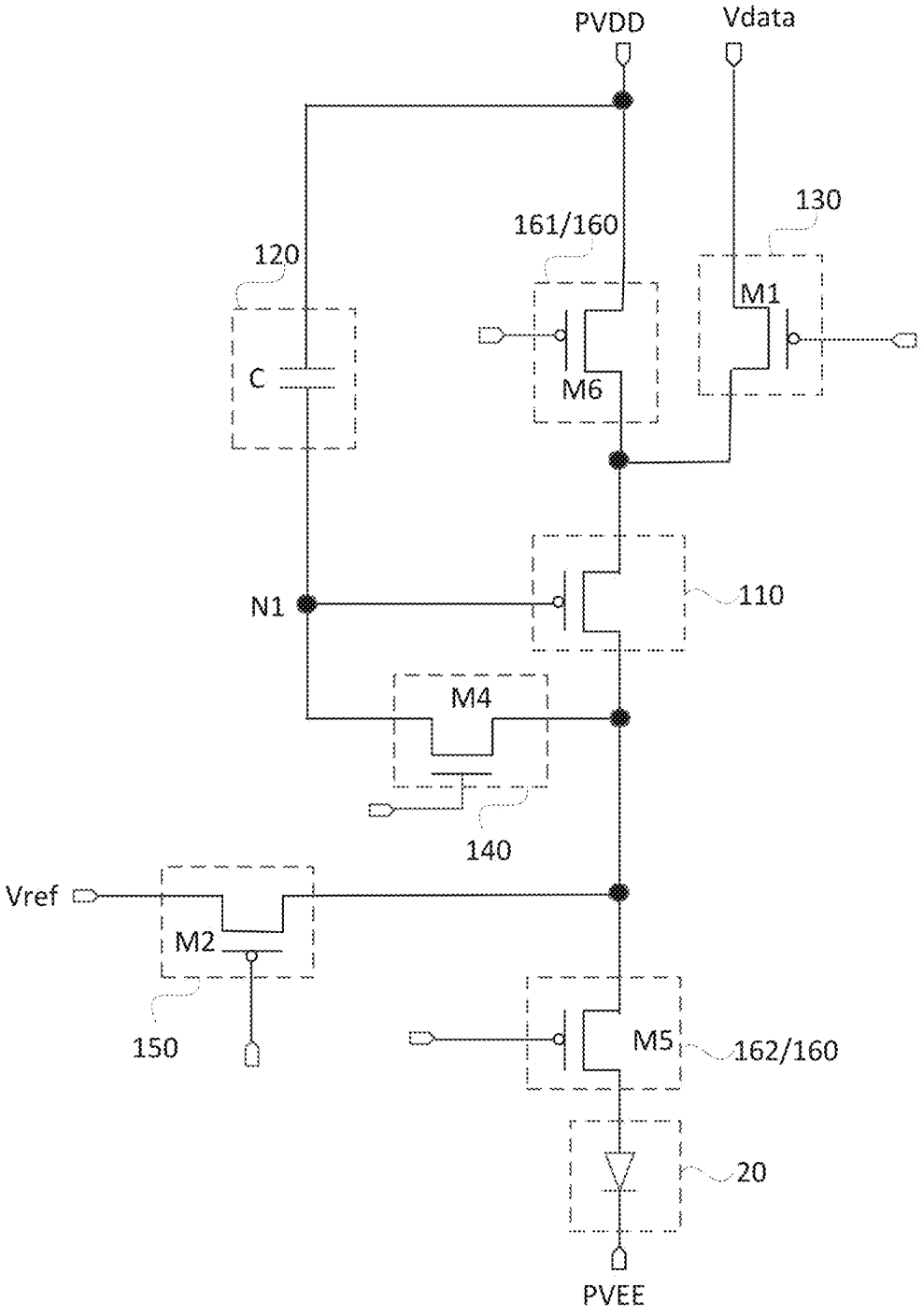

PVDD
Vdata
130
161/160
120
M1
C
M6
N1
110
M4
140
Vref
M2
150
M5
162/160
20
PVEE

FIG. 7

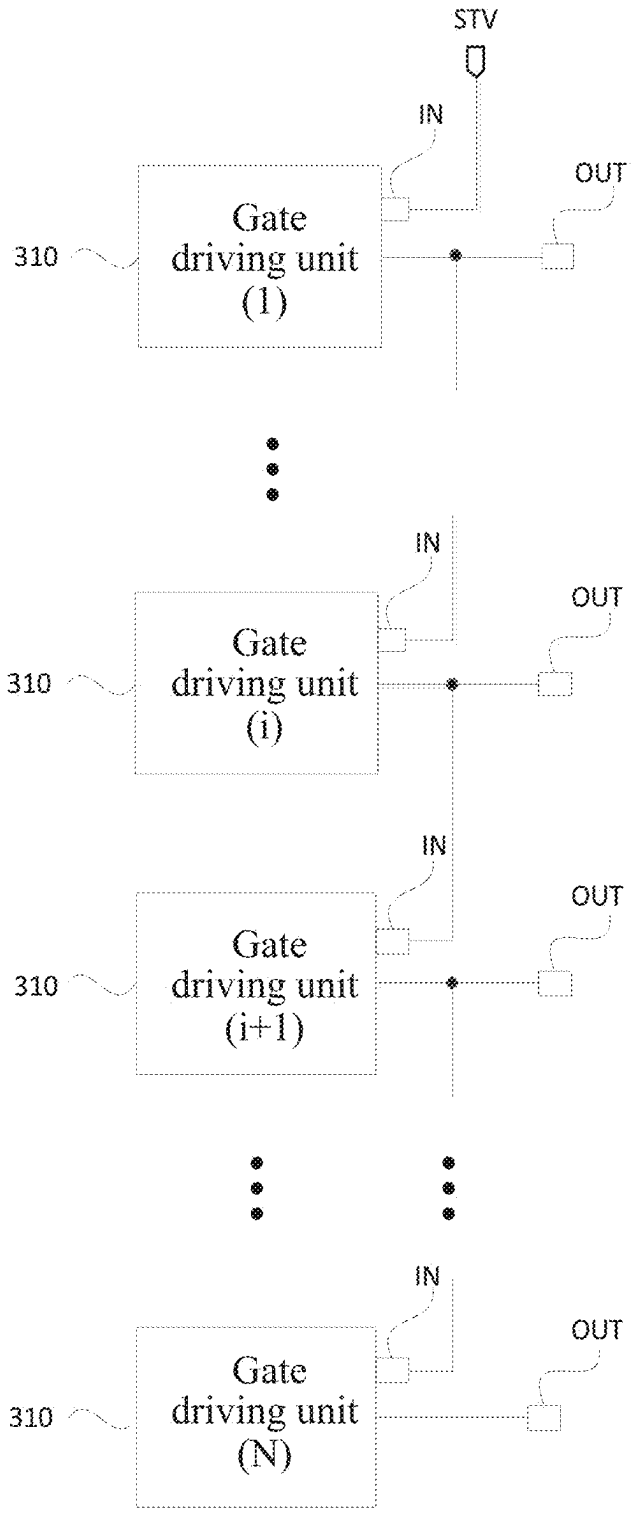

STV
IN
OUT
310
Gate driving unit (1)
IN
OUT
310
Gate driving unit (i)
IN
OUT
310
Gate driving unit (i+1)
IN
OUT
310
Gate driving unit (N)

FIG. 8

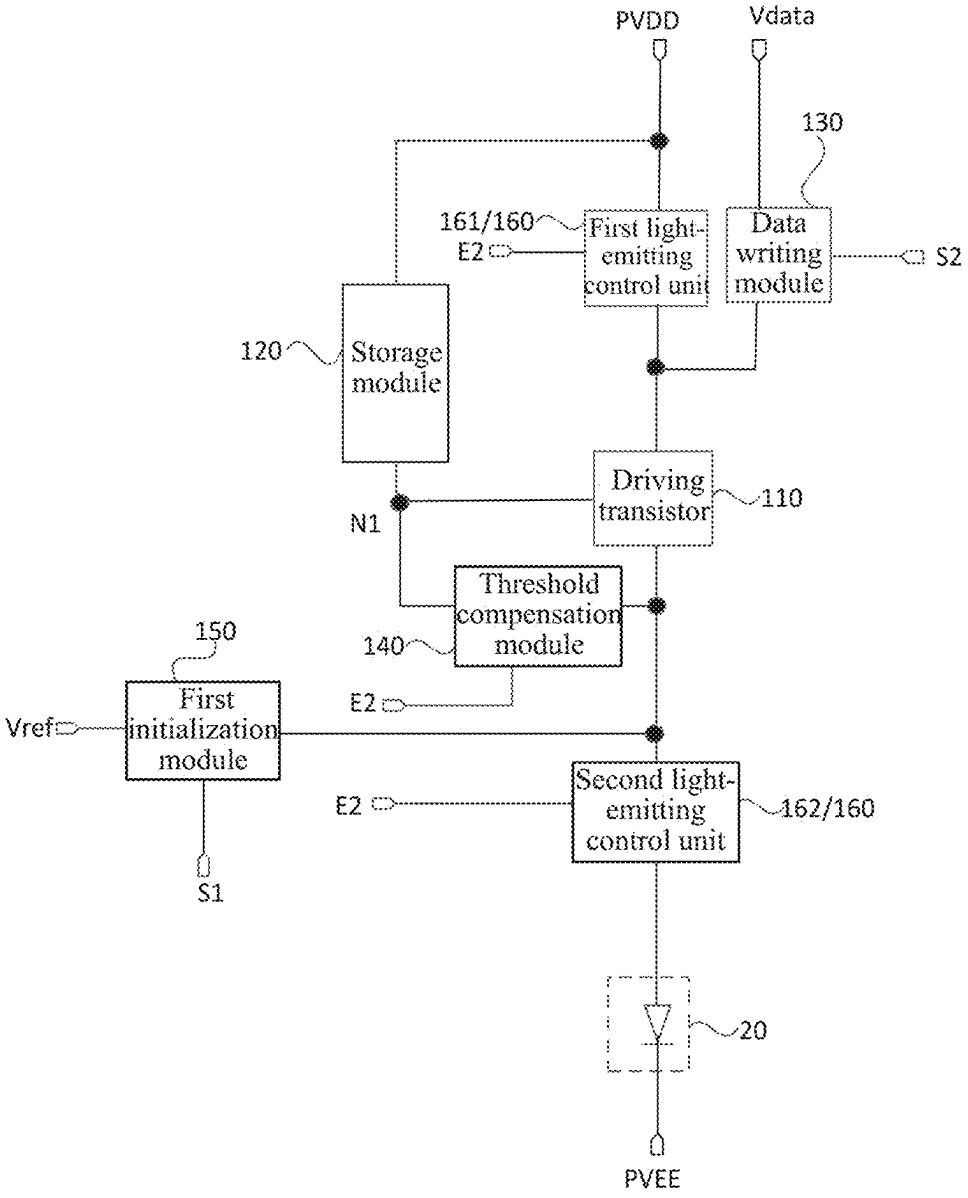

PVDD
Vdata
130
161/160
First light-emitting control unit
E2
Data writing module
S2
120
Storage module
Driving transistor
110
N1
Threshold compensation module
140
150
First initialization module
Vref
E2
S1
E2
Second light-emitting control unit
162/160
20
PVEE

FIG. 9

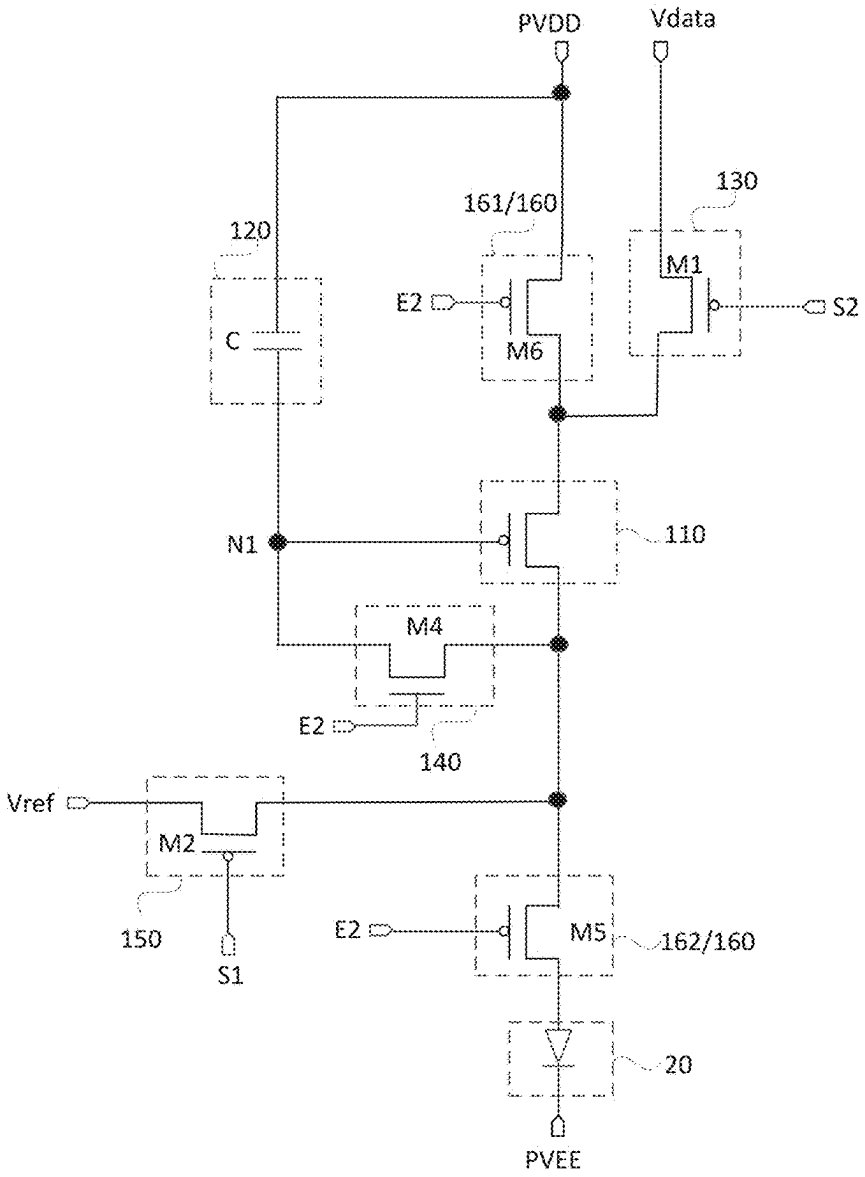

PVDD
Vdata
130
161/160
120
M1
E2
S2
C
M6
N1
110
M4
E2
140
Vref
M2
150
S1
E2
M5
162/160
20
PVEE

FIG. 10

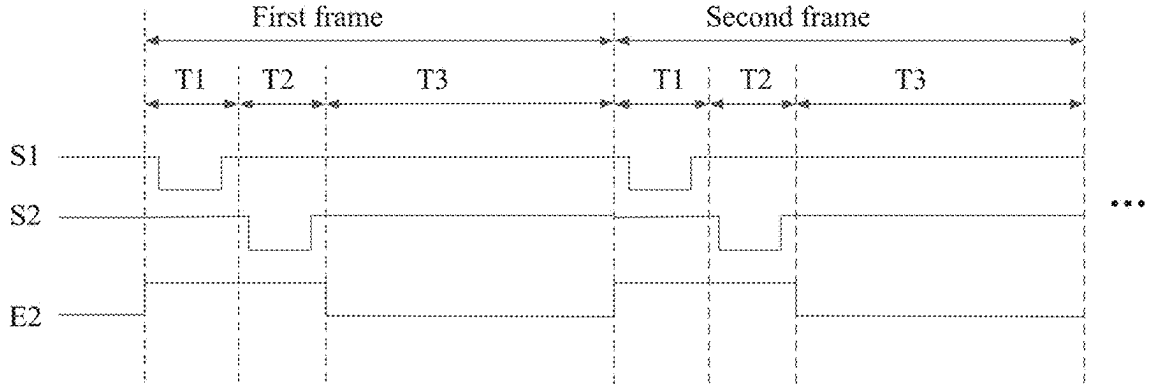

First frame
Second frame
T1
T2
T3
T1
T2
T3
S1
S2
E2
...

FIG. 11

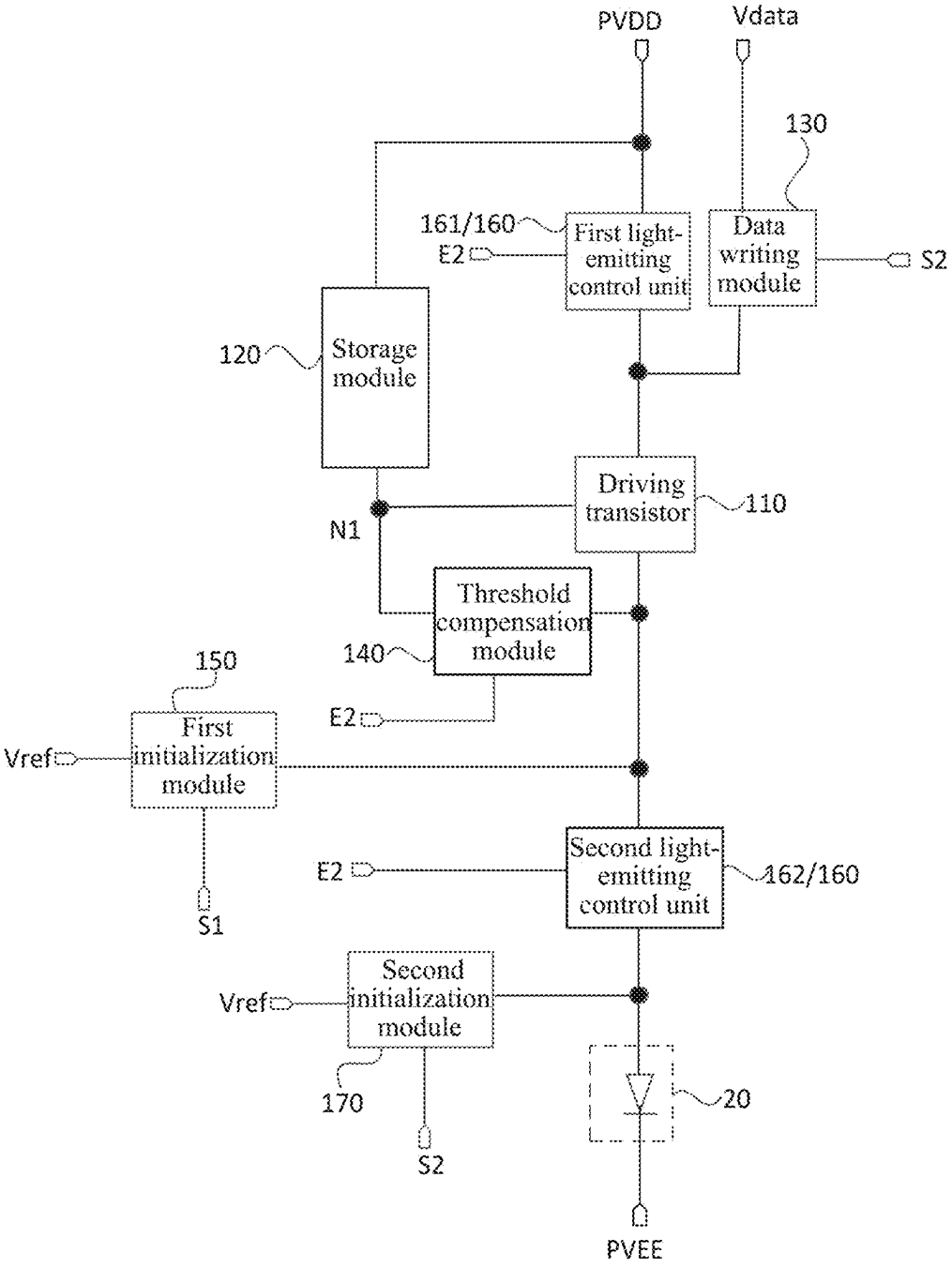

PVDD
Vdata
130
161/160
First light-emitting control unit
Data writing module
E2
S2
120
Storage module
Driving transistor
110
N1
Threshold compensation module
140
150
E2
First initialization module
Vref
S1
Second light-emitting control unit
E2
162/160
Second initialization module
Vref
170
S2
20
PVEE

FIG. 12

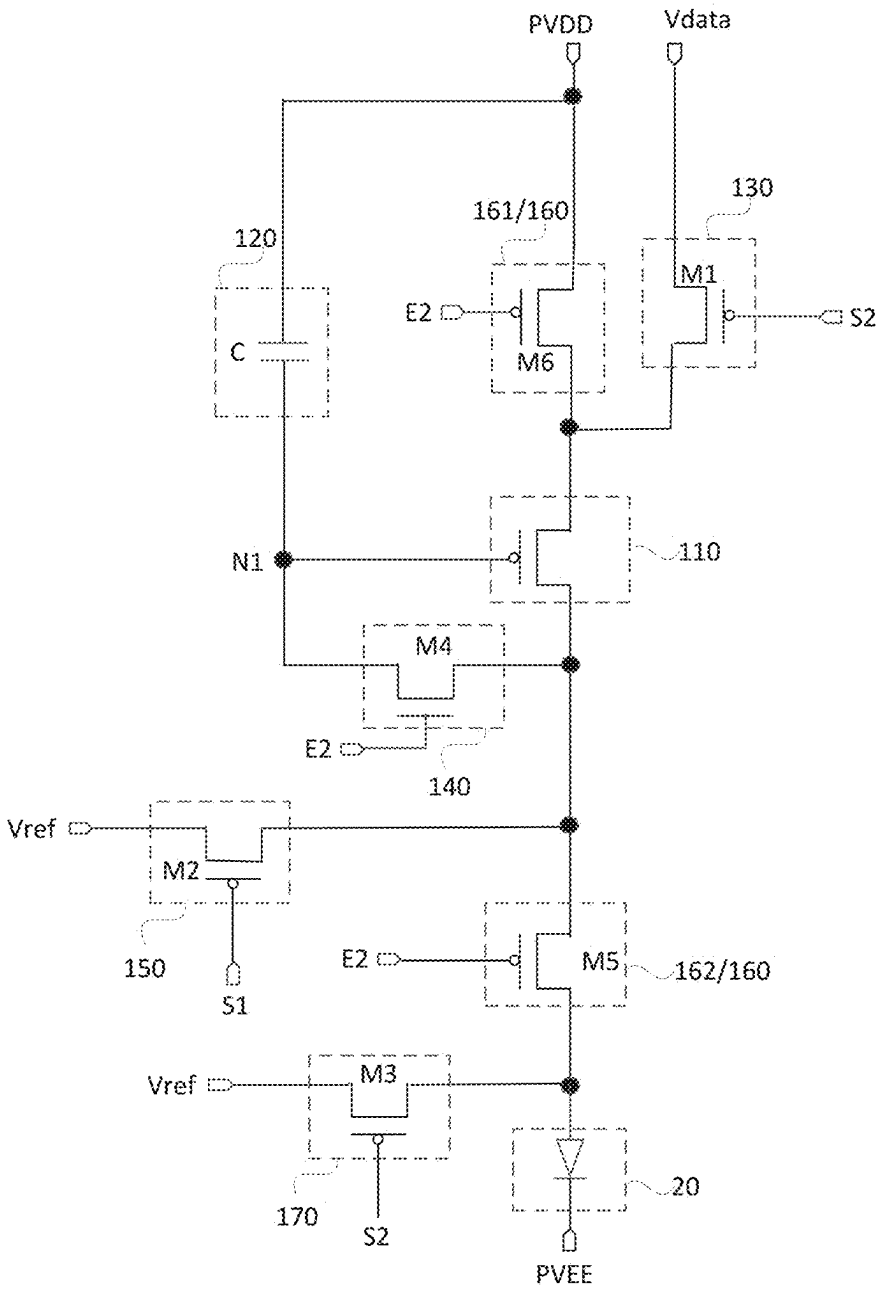

PVDD
Vdata
130
161/160
120
M1
E2
S2
C
M6
N1
110
M4
E2
140
Vref
M2
150
S1
E2
M5
162/160
Vref
M3
170
S2
20
PVEE

FIG. 13

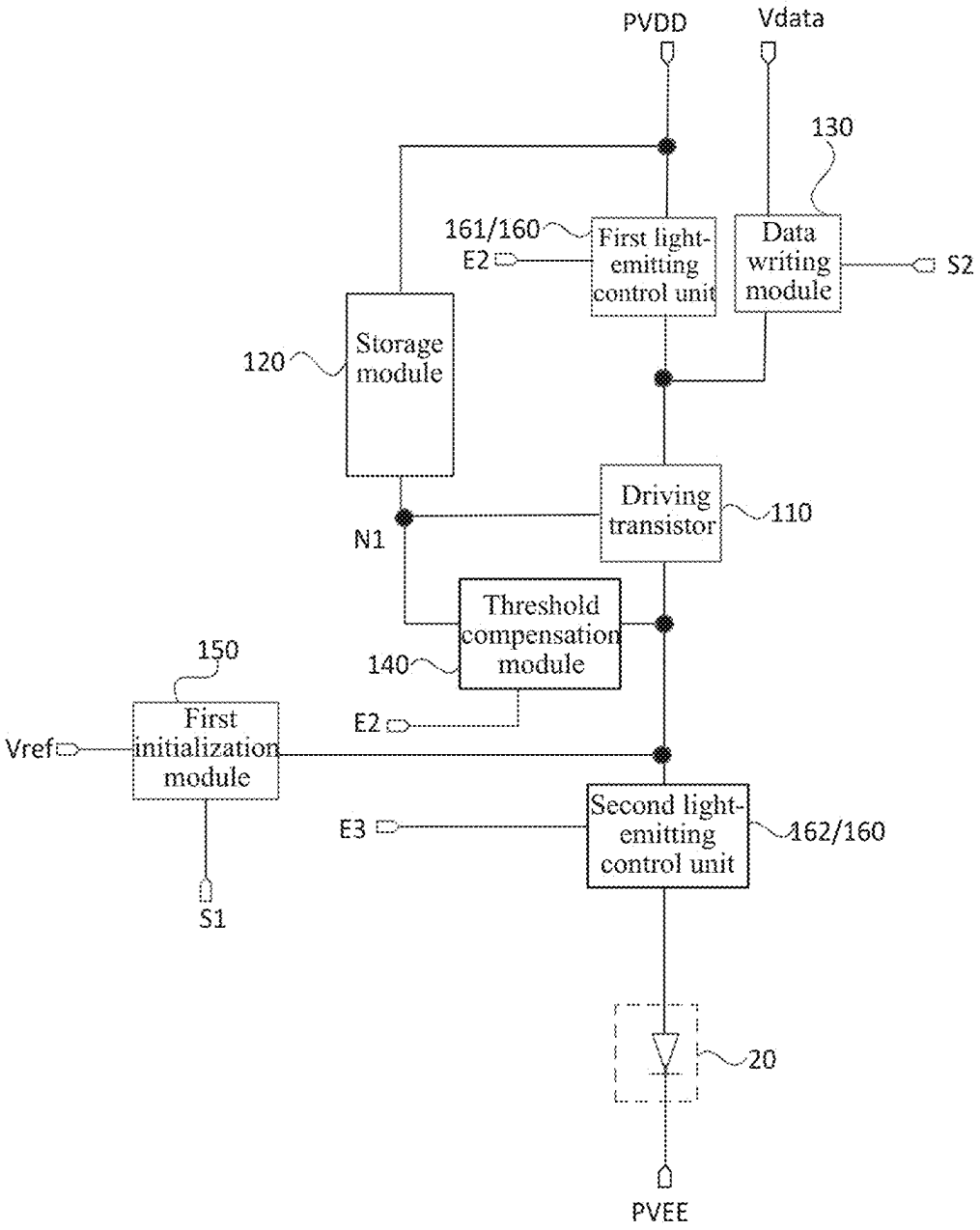

PVDD
Vdata
130
161/160
E2
First light-emitting control unit
Data writing module
S2
120
Storage module
Driving transistor
110
N1
Threshold compensation module
140
150
First initialization module
Vref
E2
E3
Second light-emitting control unit
162/160
S1
20
PVEE

FIG. 14

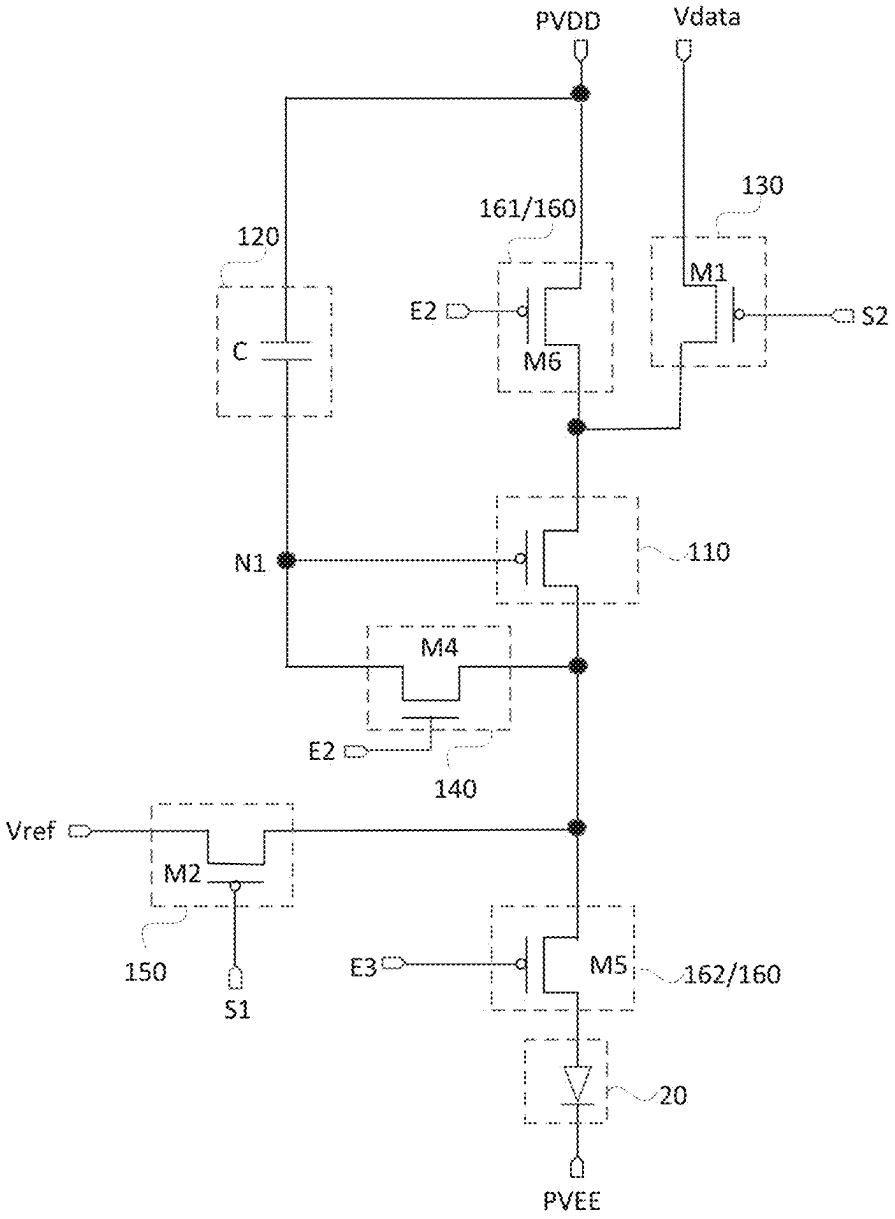

PVDD
Vdata
130
161/160
120
M1
E2
S2
C
M6
N1
110
M4
E2
140
Vref
M2
150
S1
E3
M5
162/160
20
PVEE

FIG. 15

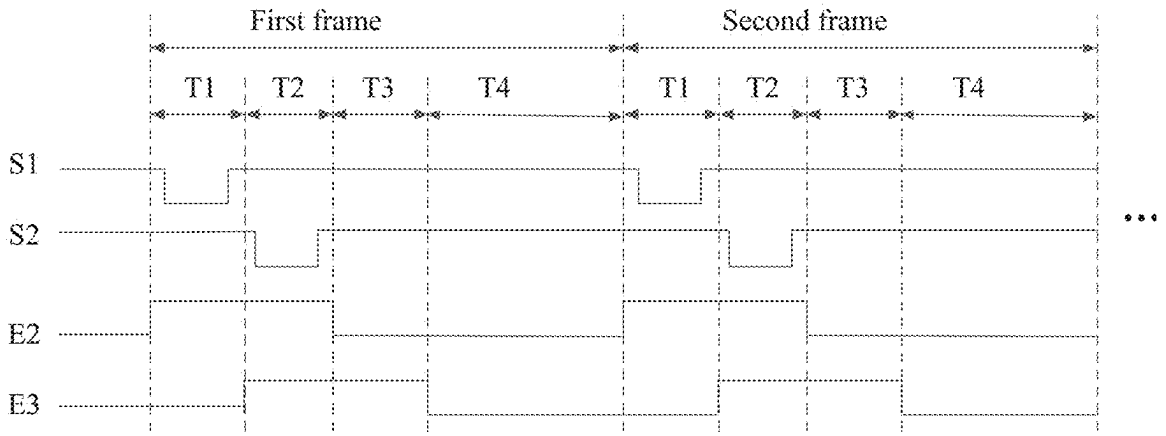


FIG. 16

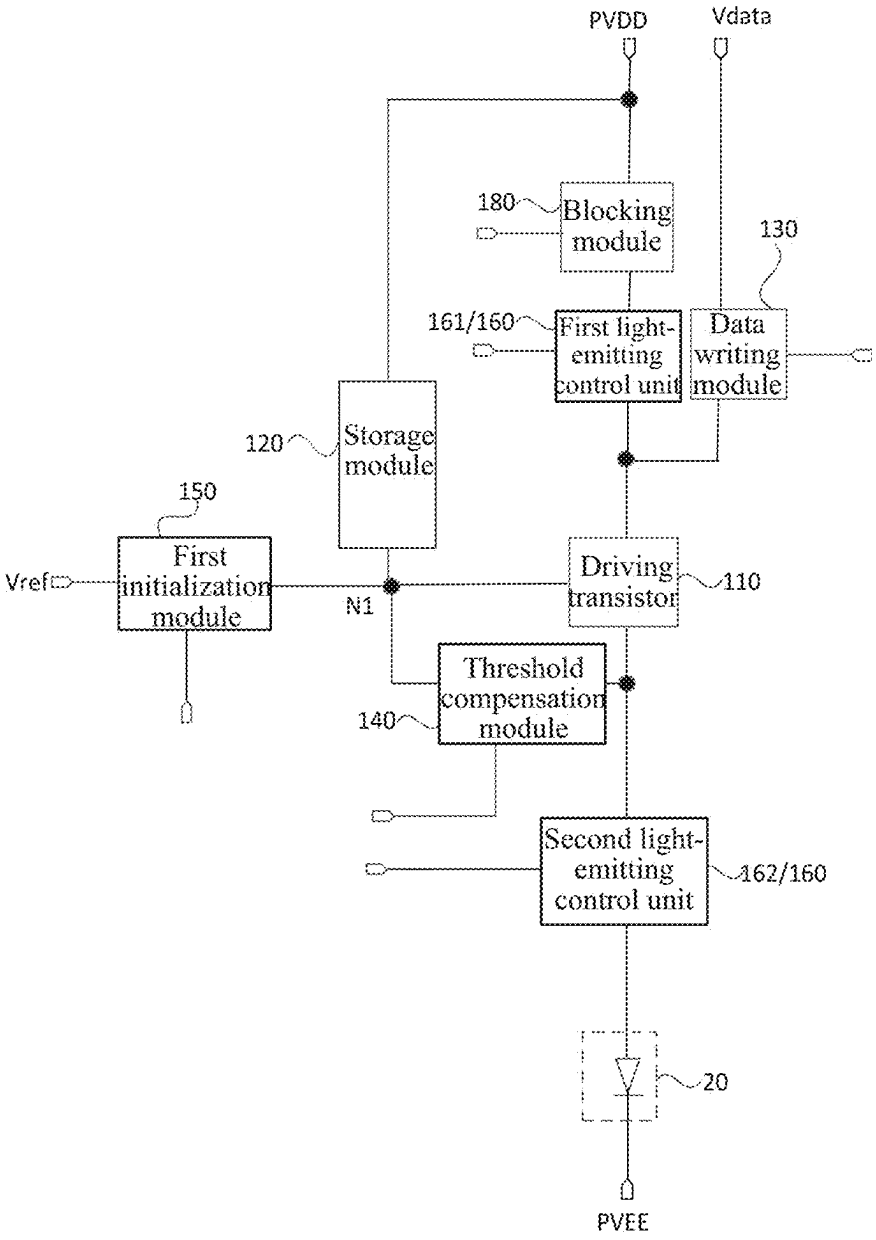

PVDD
Vdata
180
Blocking module
130
161/160
First light-emitting control unit
Data writing module
120
Storage module
150
Vref
First initialization module
N1
Driving transistor
110
Threshold compensation module
140
Second light-emitting control unit
162/160
20
PVEE

FIG. 17

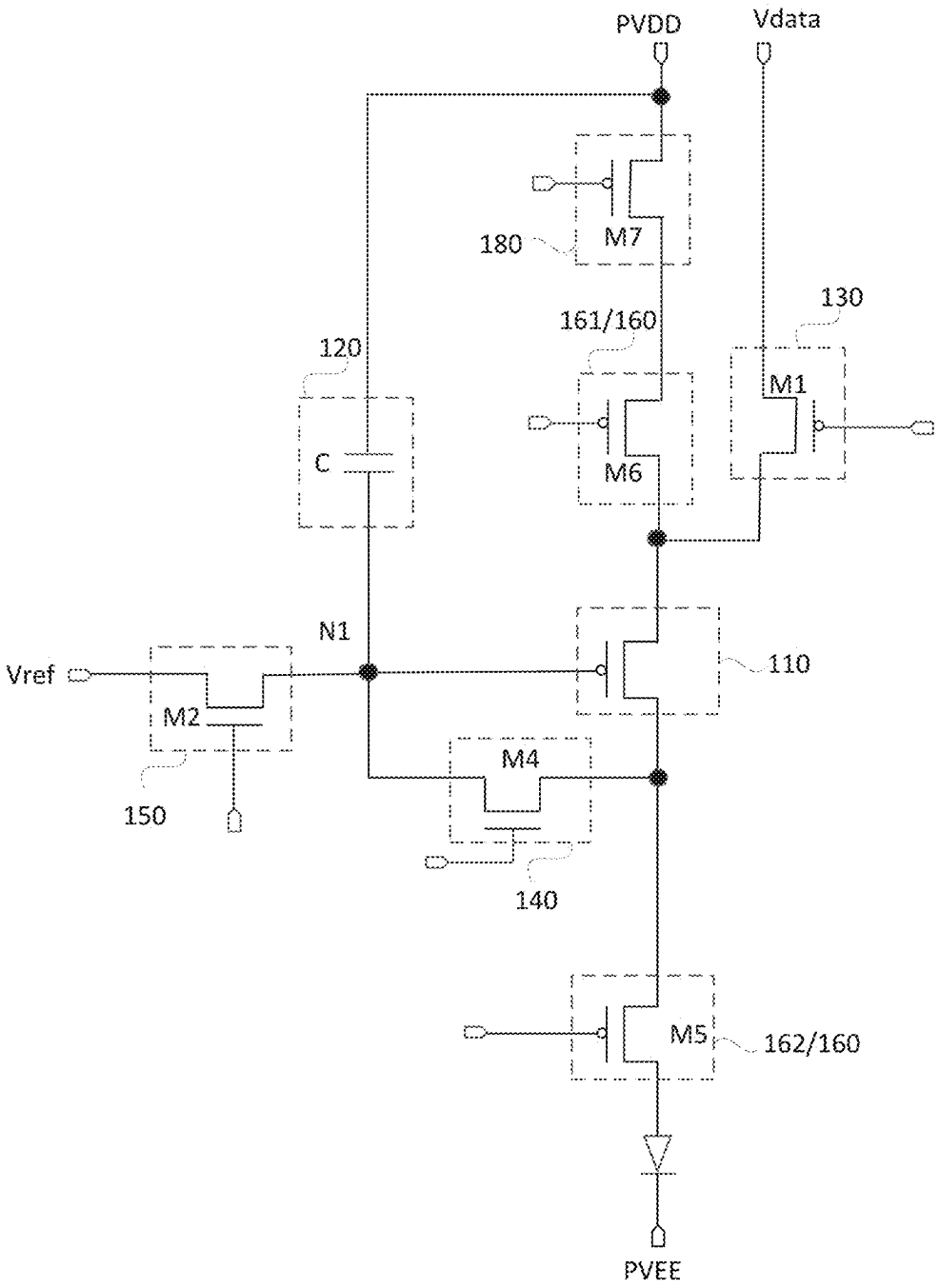

PVDD
Vdata
180
M7
130
161/160
120
M1
C
M6
N1
Vref
110
M2
M4
150
140
M5
162/160
PVEE

FIG. 18

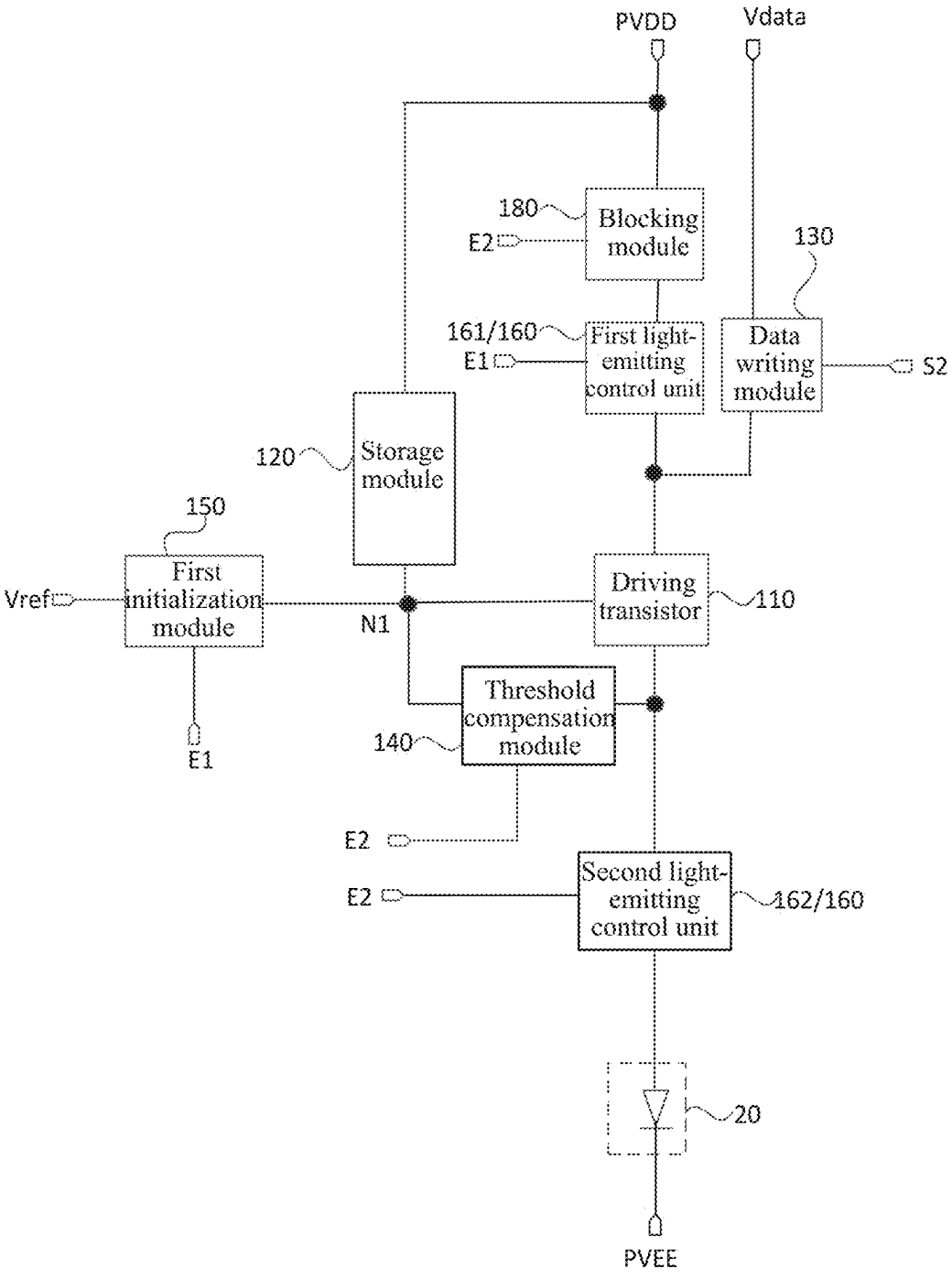

PVDD
Vdata
180
Blocking module
E2
130
161/160
First light-emitting control unit
E1
Data writing module
S2
120
Storage module
150
First initialization module
Vref
N1
Driving transistor
110
Threshold compensation module
140
E1
E2
E2
Second light-emitting control unit
162/160
20
PVEE

FIG. 19

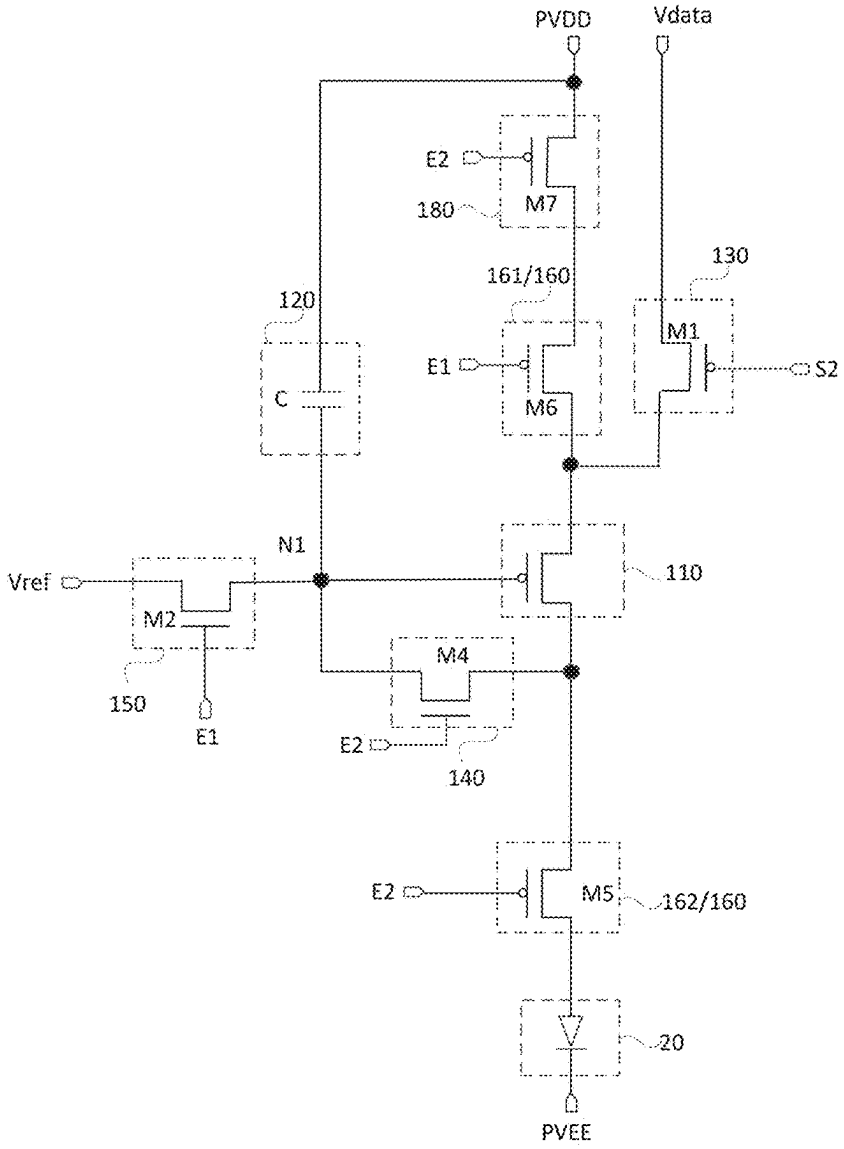

PVDD
Vdata
E2
180
M7
130
161/160
120
M1
E1
S2
C
M6
N1
Vref
110
M2
M4
150
E1
E2
140
E2
M5
162/160
20
PVEE

FIG. 20

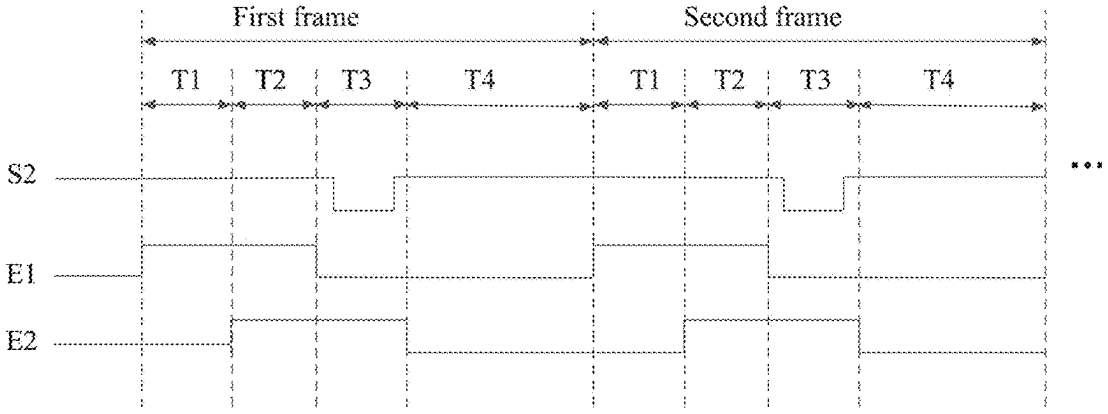

First frame
Second frame
T1
T2
T3
T4
T1
T2
T3
T4
S2
E1
E2

FIG. 21

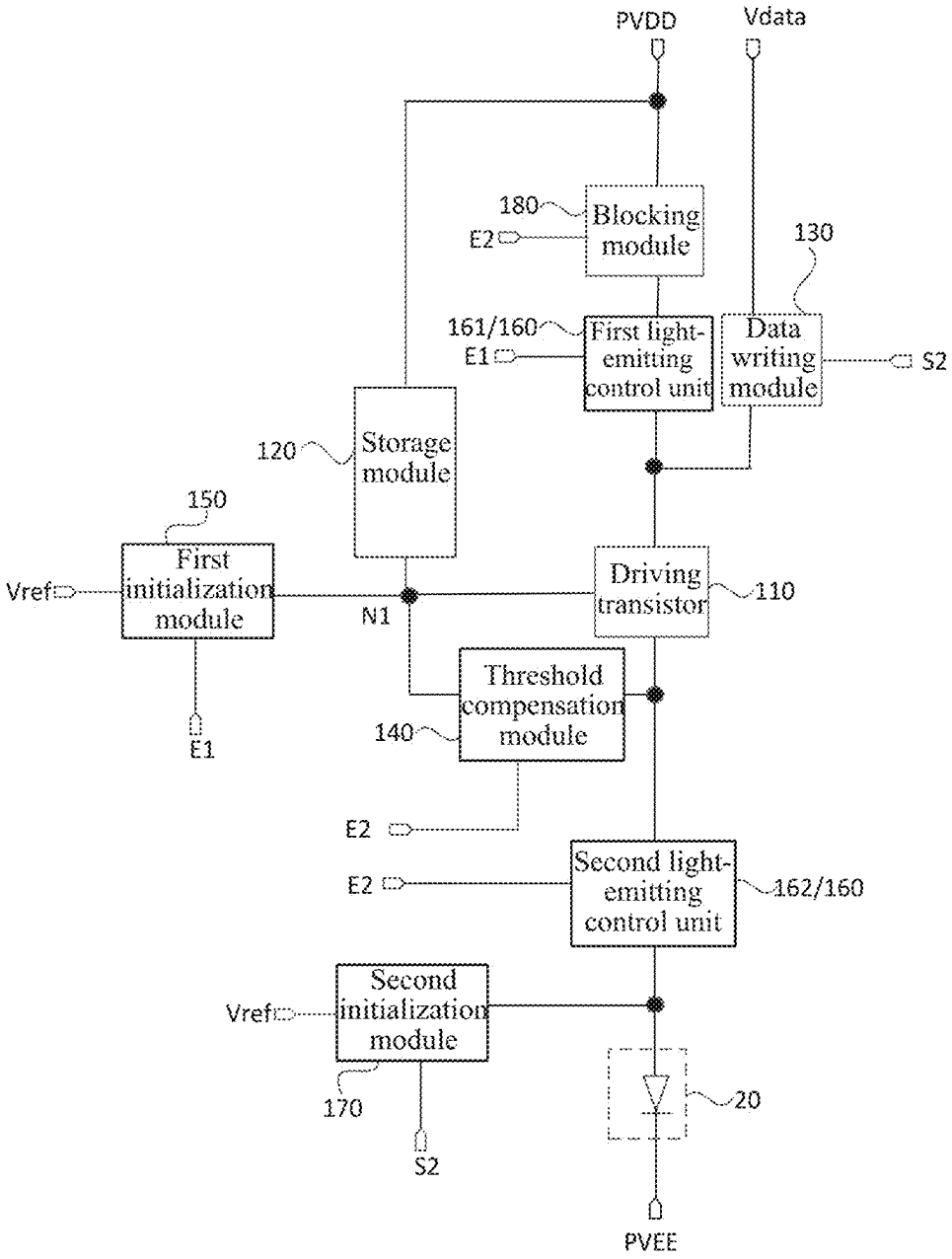

PVDD
Vdata
180
Blocking module
E2
130
161/160
First light-emitting control unit
E1
Data writing module
S2
120
Storage module
150
First initialization module
Vref
N1
Driving transistor
110
Threshold compensation module
140
E1
E2
E2
Second light-emitting control unit
162/160
Second initialization module
Vref
170
S2
20
PVEE

FIG. 22

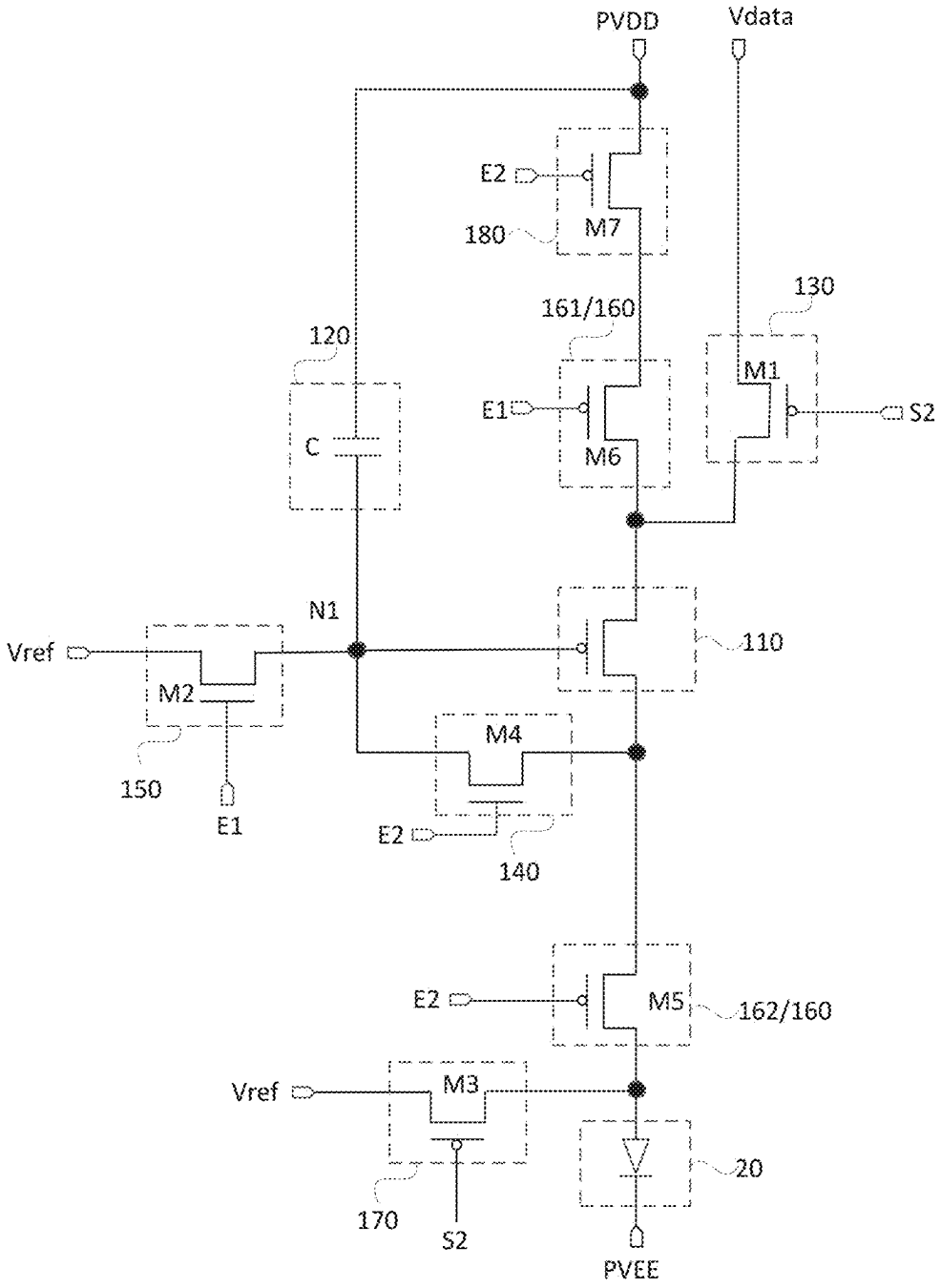

PVDD
Vdata
E2
180
M7
130
161/160
120
M1
S2
E1
C
M6
N1
Vref
110
M2
M4
150
E1
E2
140
E2
M5
162/160
Vref
M3
20
170
S2
PVEE

FIG. 23

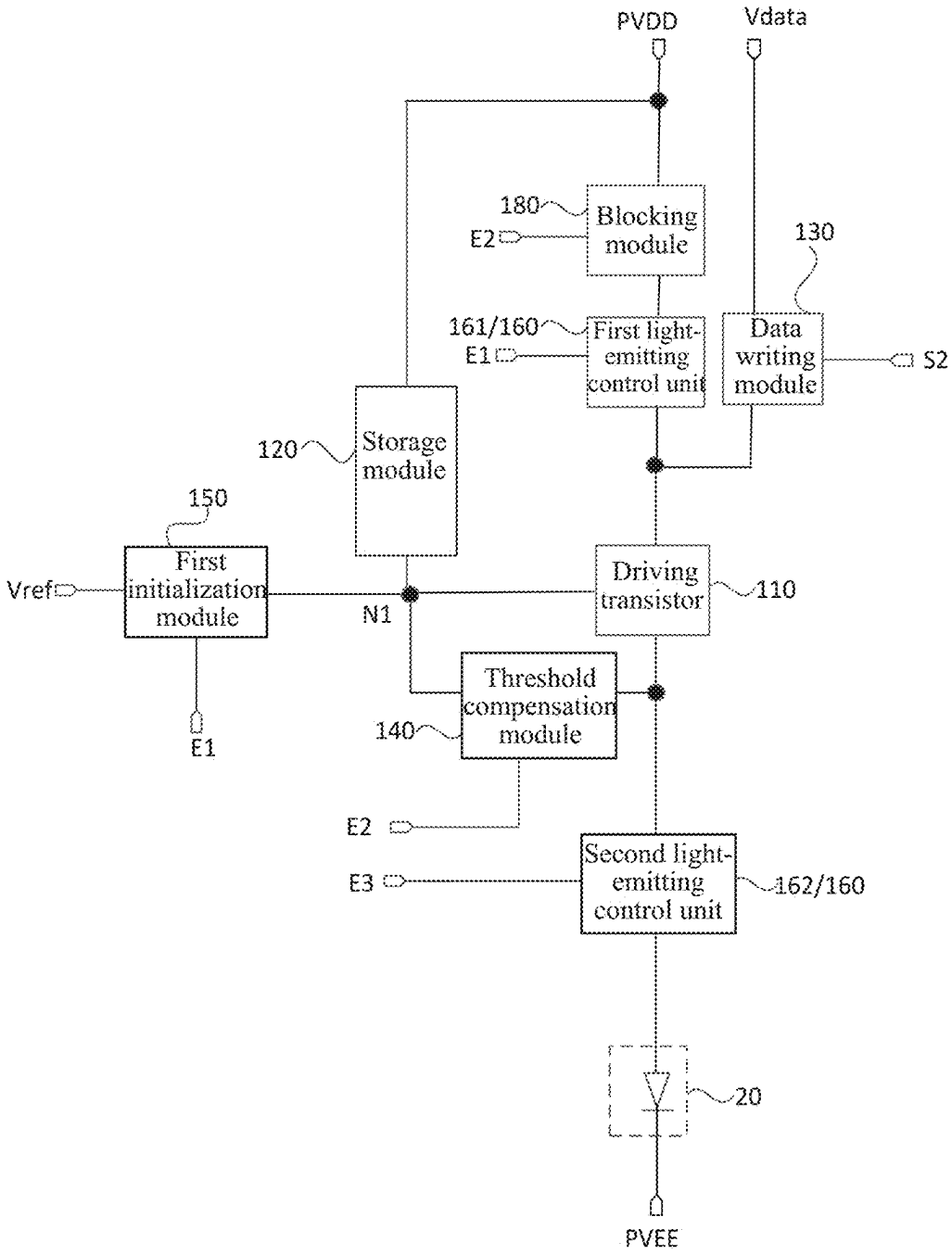

PVDD
Vdata
180
E2
Blocking module
130
161/160
E1
First light-emitting control unit
Data writing module
S2
120
Storage module
150
Vref
First initialization module
N1
Driving transistor
110
Threshold compensation module
140
E1
E2
E3
Second light-emitting control unit
162/160
20
PVEE

FIG. 24

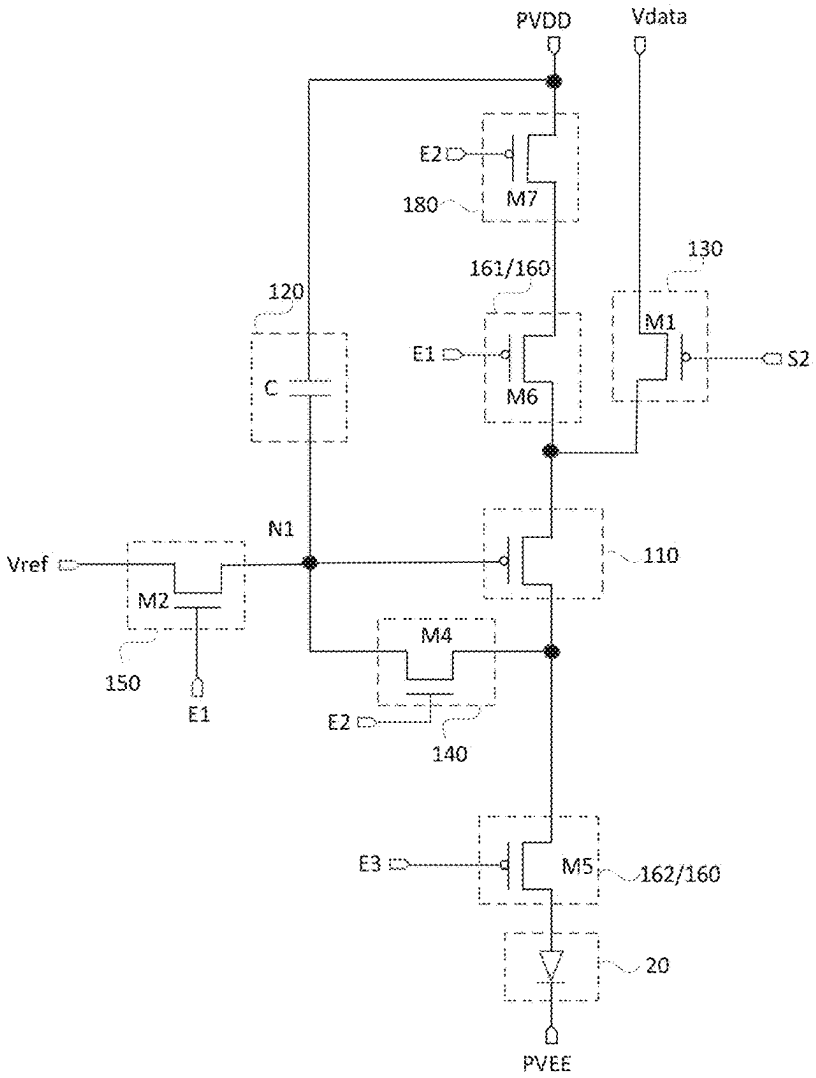

PVDD
Vdata
E2
M7
180
130
161/160
120
M1
E1
S2
C
M6
N1
110
Vref
M2
M4
150
E1
E2
140
E3
M5
162/160
20
PVEE

FIG. 25

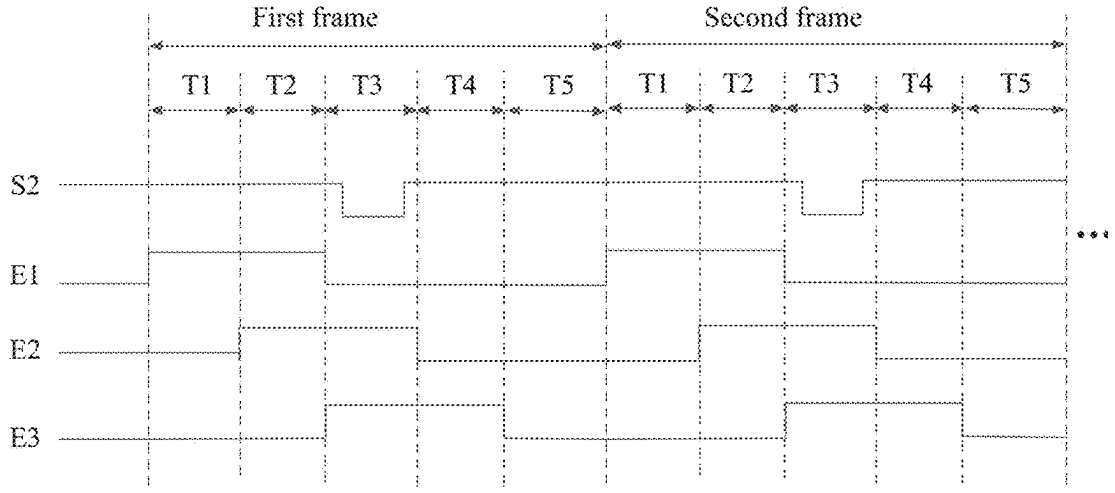

First frame
Second frame
T1
T2
T3
T4
T5
T1
T2
T3
T4
T5
S2
E1
E2
E3

FIG. 26

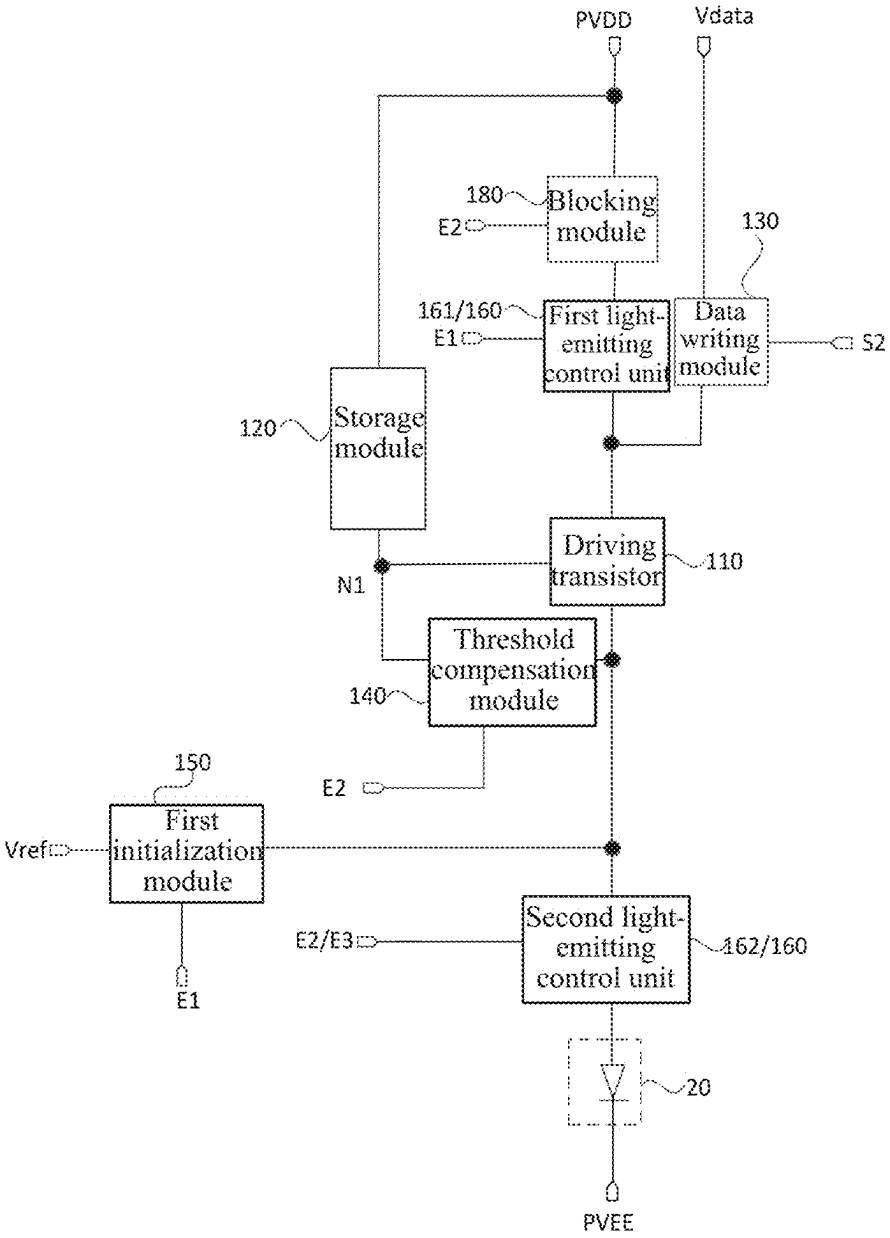

PVDD
Vdata
180
Blocking module
E2
130
161/160
First light-emitting control unit
E1
Data writing module
S2
120
Storage module
Driving transistor
110
N1
Threshold compensation module
140
150
E2
First initialization module
Vref
Second light-emitting control unit
E2/E3
162/160
E1
20
PVEE

FIG. 27

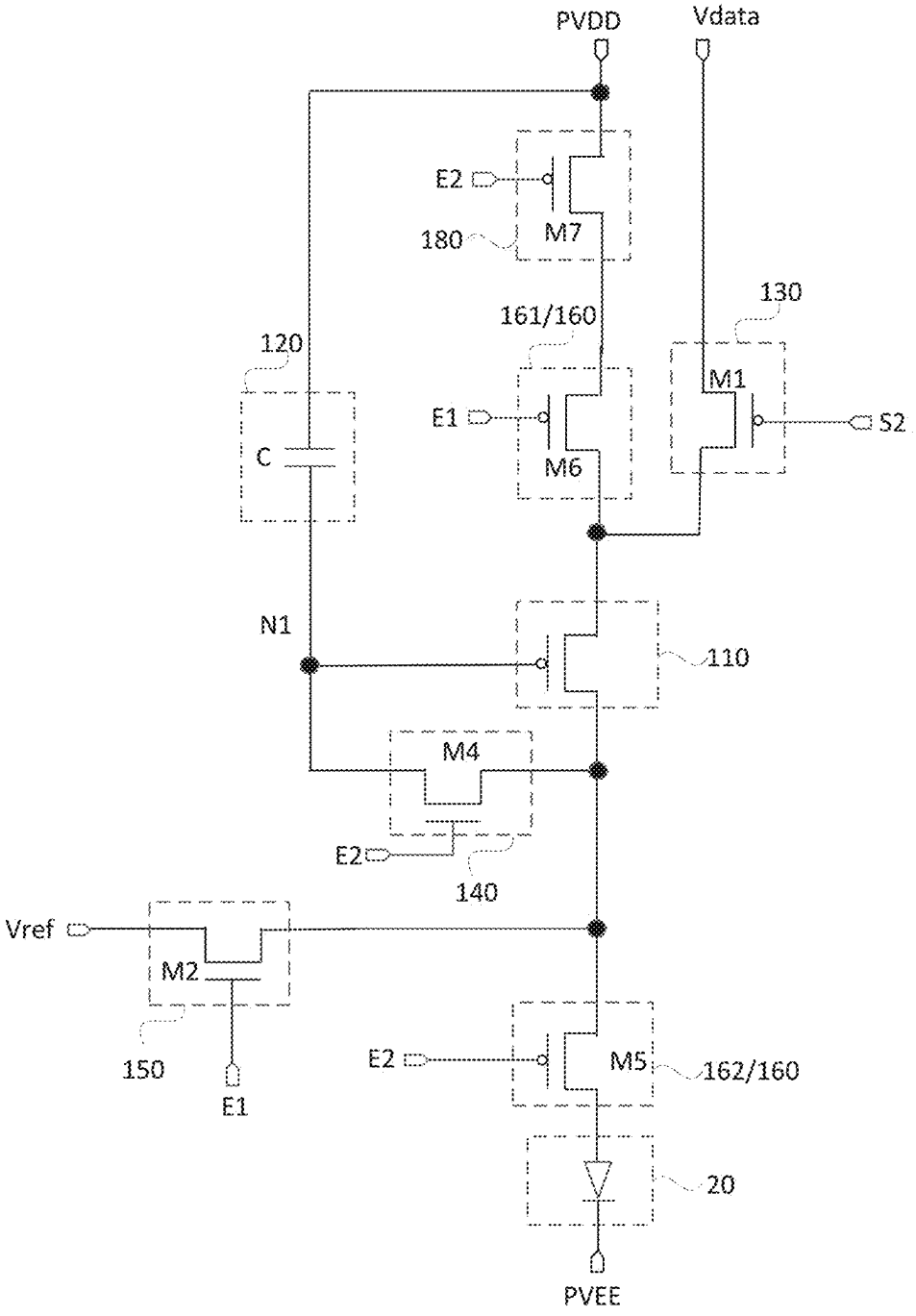

PVDD
Vdata
E2
180
M7
130
161/160
120
M1
E1
S2
C
M6
N1
110
M4
E2
140
Vref
M2
150
E1
E2
M5
162/160
20
PVEE

FIG. 28

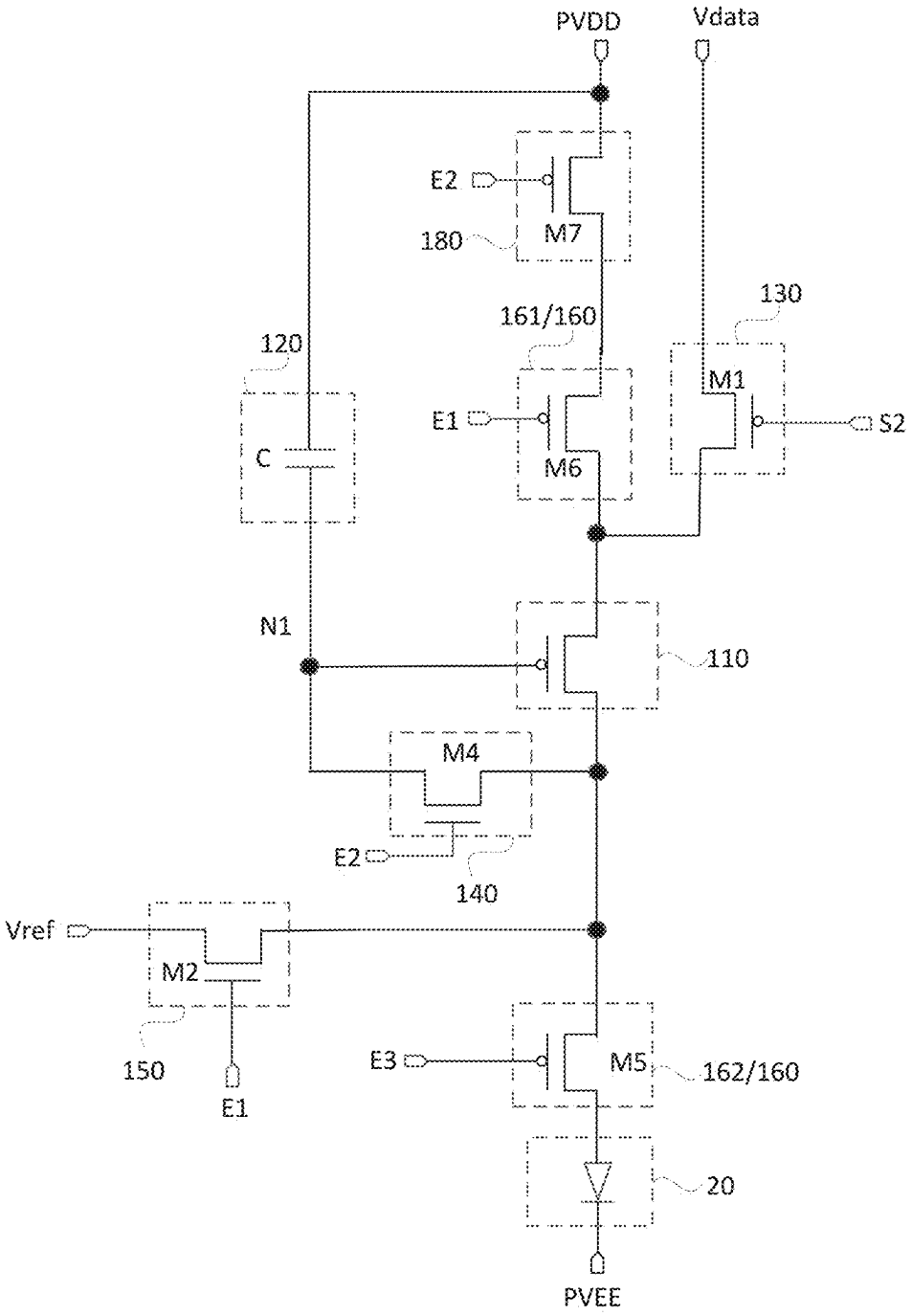

PVDD
Vdata
E2
180
M7
130
161/160
120
M1
E1
S2
C
M6
N1
110
M4
E2
140
Vref
M2
150
E1
E3
M5
162/160
20
PVEE

FIG. 29

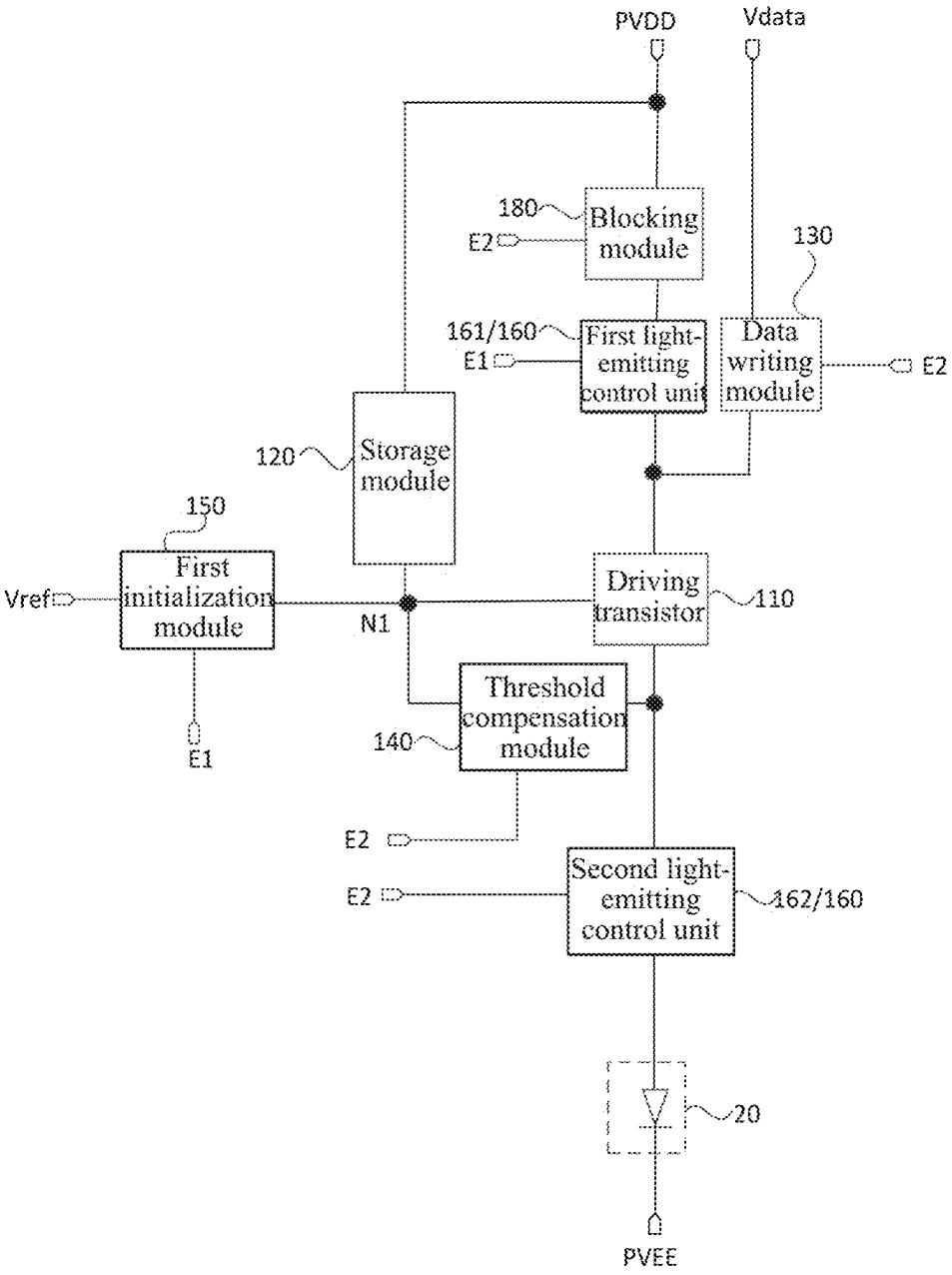

PVDD
Vdata
180
Blocking module
E2
130
161/160
First light-emitting control unit
E1
Data writing module
E2
120
Storage module
150
First initialization module
Vref
N1
Driving transistor
110
Threshold compensation module
140
E1
E2
E2
Second light-emitting control unit
162/160
20
PVEE

FIG. 30

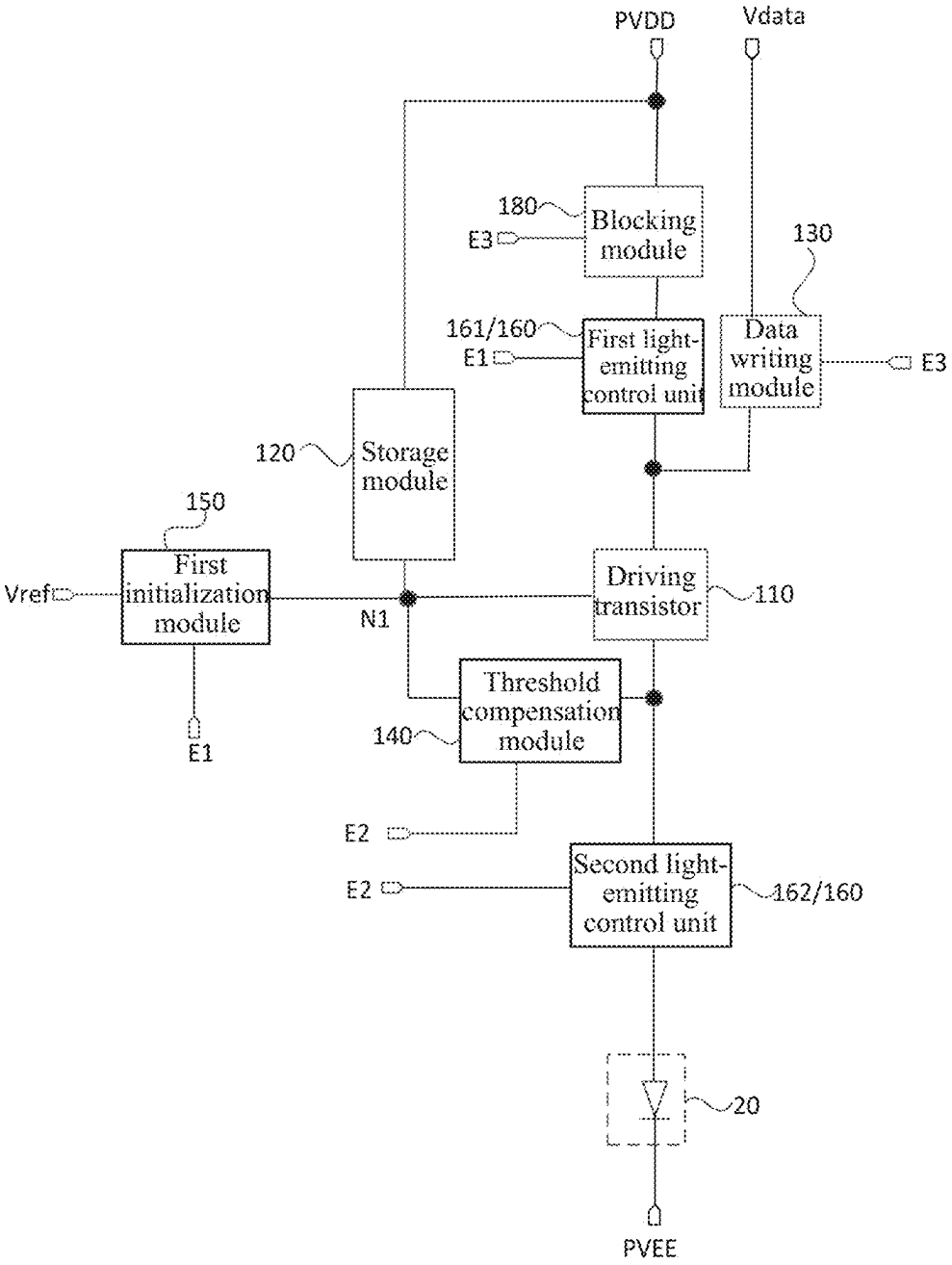

PVDD
Vdata
180
E3
Blocking module
130
161/160
E1
First light-emitting control unit
Data writing module
E3
120
Storage module
150
Vref
First initialization module
N1
Driving transistor
110
E1
140
Threshold compensation module
E2
E2
Second light-emitting control unit
162/160
20
PVEE

FIG. 31

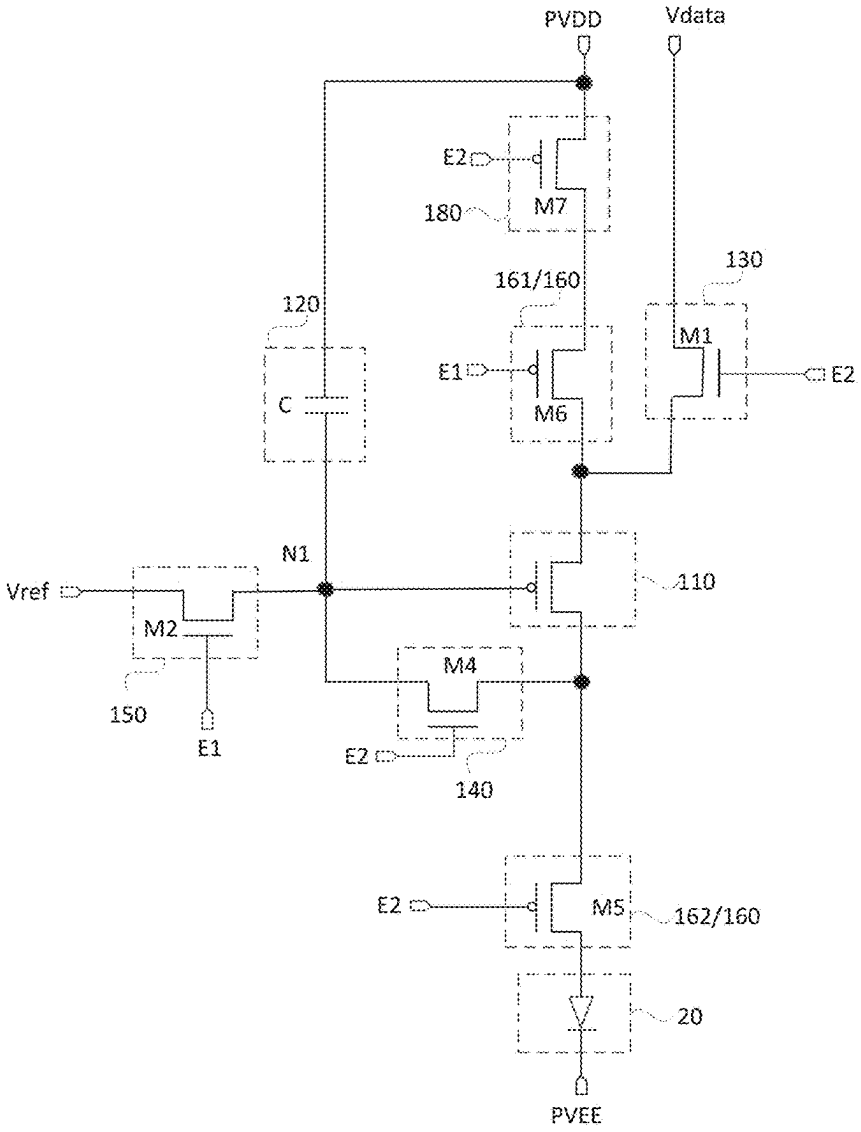

PVDD
Vdata
E2
180
M7
130
161/160
120
M1
E2
E1
M6
C
N1
110
Vref
M2
M4
150
E1
E2
140
E2
M5
162/160
20
PVEE

FIG. 32

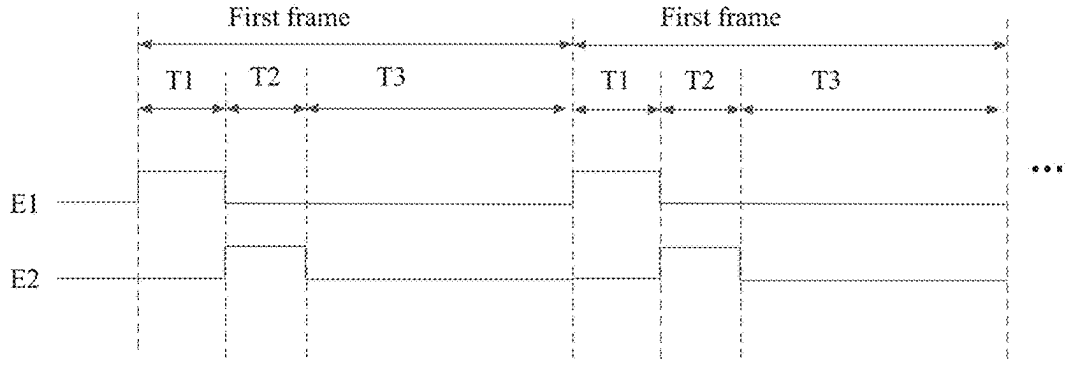

First frame
First frame
T1
T2
T3
T1
T2
T3
E1
E2

FIG. 33

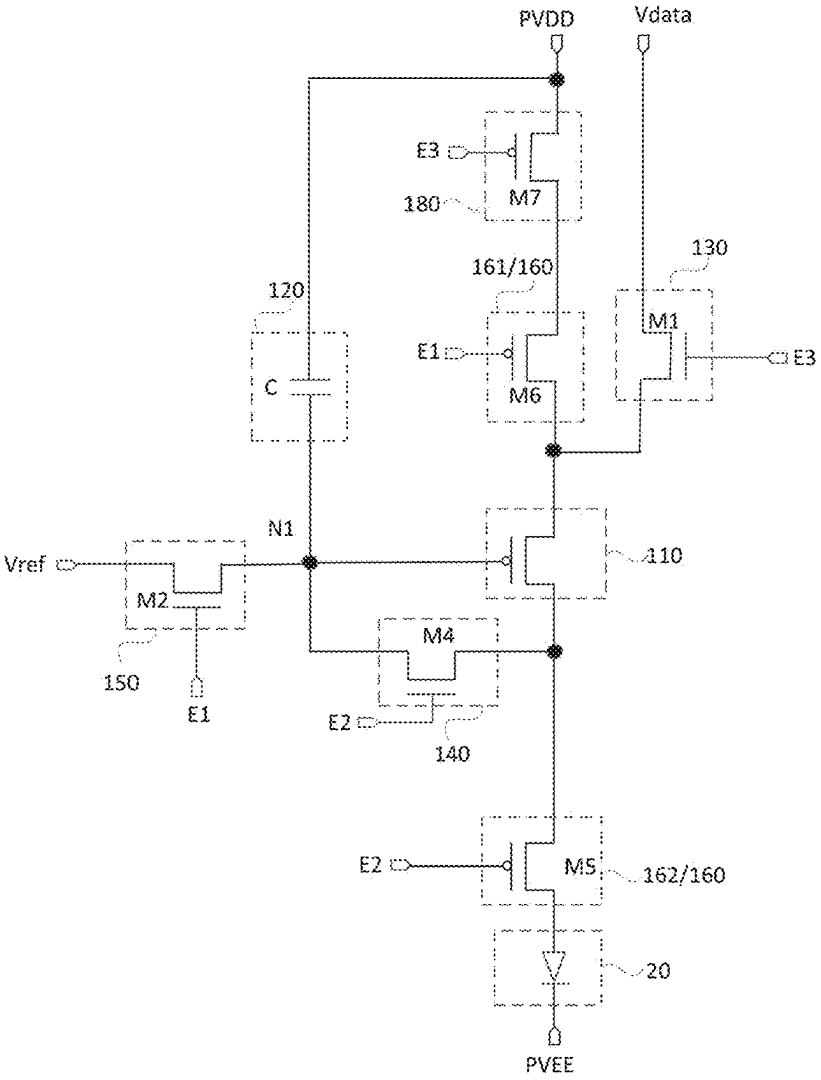

PVDD
Vdata
E3
180
M7
130
161/160
120
M1
E1
E3
C
M6
N1
110
Vref
M2
M4
150
E1
E2
140
E2
M5
162/160
20
PVEE

FIG. 34

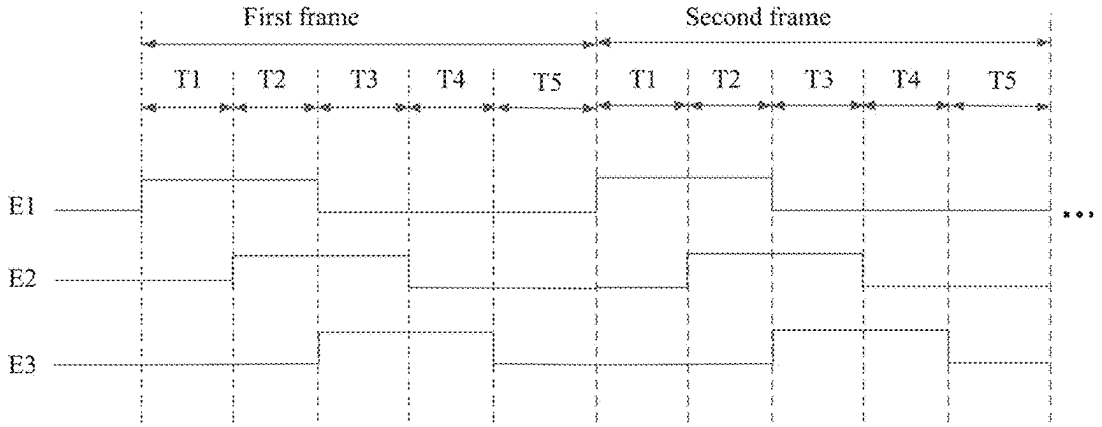

First frame
Second frame
T1
T2
T3
T4
T5
T1
T2
T3
T4
T5
E1
E2
E3

FIG. 35

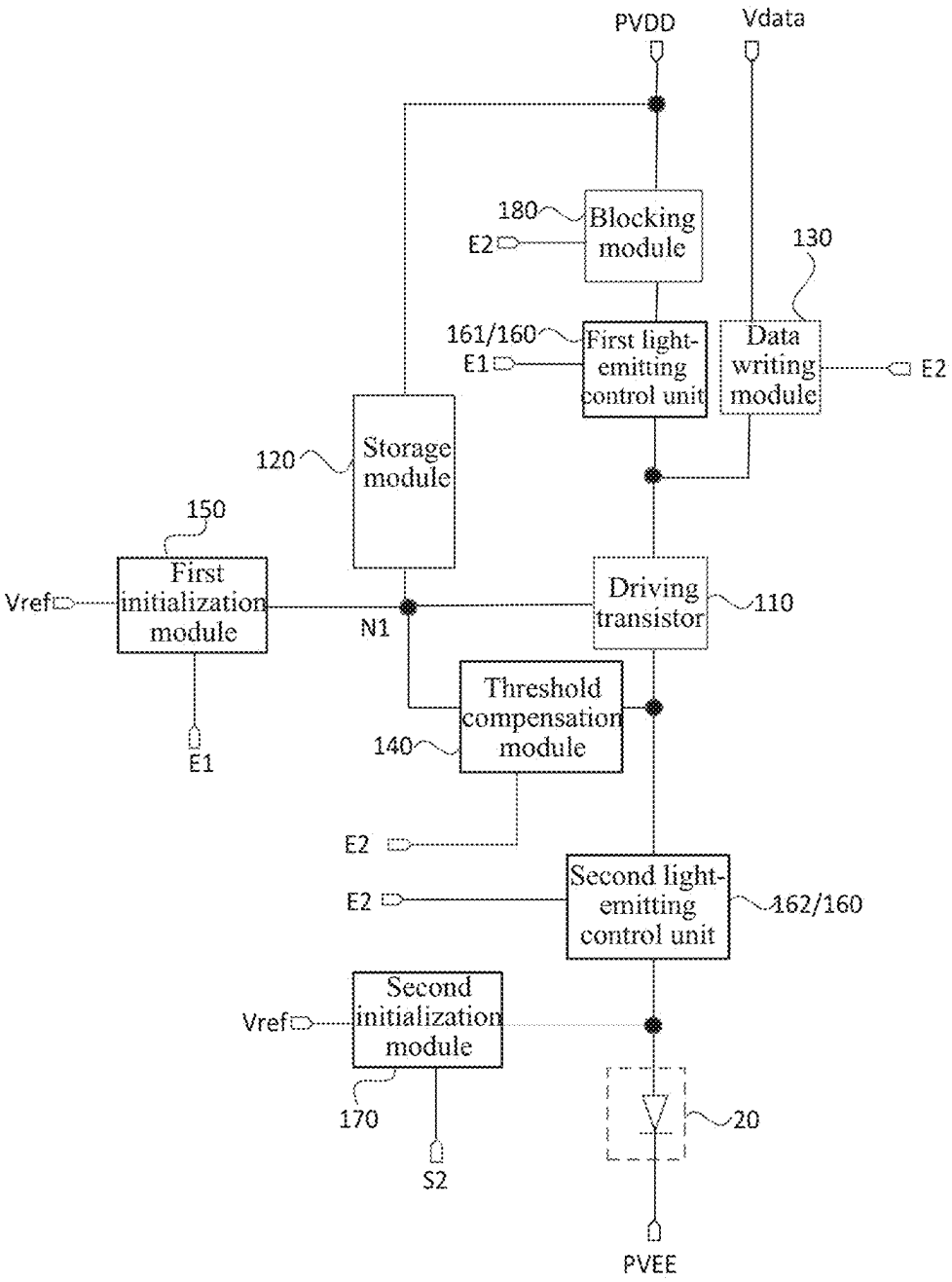

PVDD
Vdata
180
Blocking module
E2
130
161/160
First light-emitting control unit
E1
Data writing module
E2
120
Storage module
150
First initialization module
Vref
N1
Driving transistor
110
E1
Threshold compensation module
140
E2
E2
Second light-emitting control unit
162/160
Second initialization module
Vref
170
S2
20
PVEE

FIG. 36

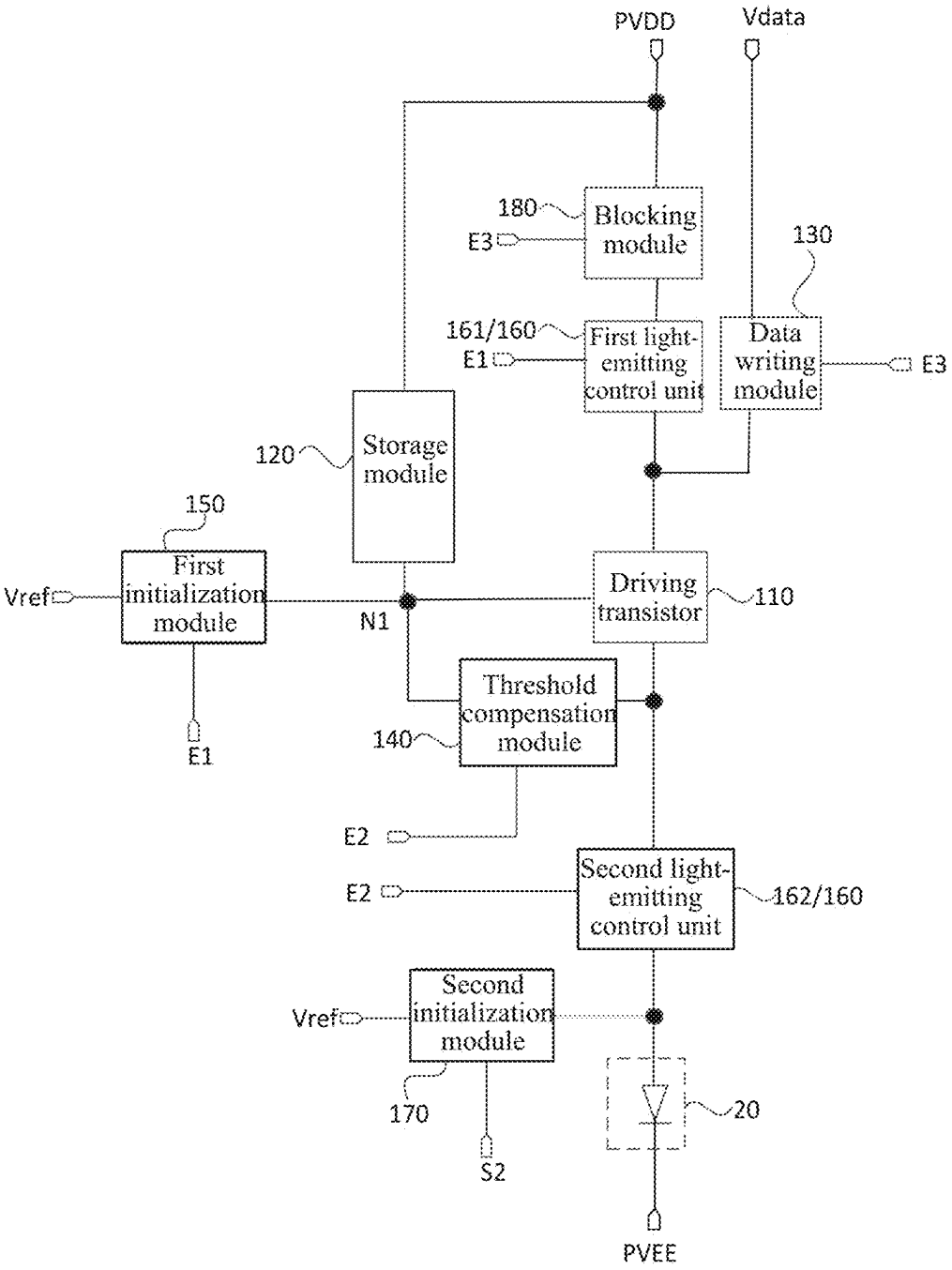

PVDD
Vdata
180
E3
Blocking module
130
161/160
E1
First light-emitting control unit
Data writing module
E3
120
Storage module
150
Vref
First initialization module
N1
Driving transistor
110
E1
Threshold compensation module
140
E2
E2
Second light-emitting control unit
162/160
Vref
Second initialization module
170
S2
20
PVEE

FIG. 37

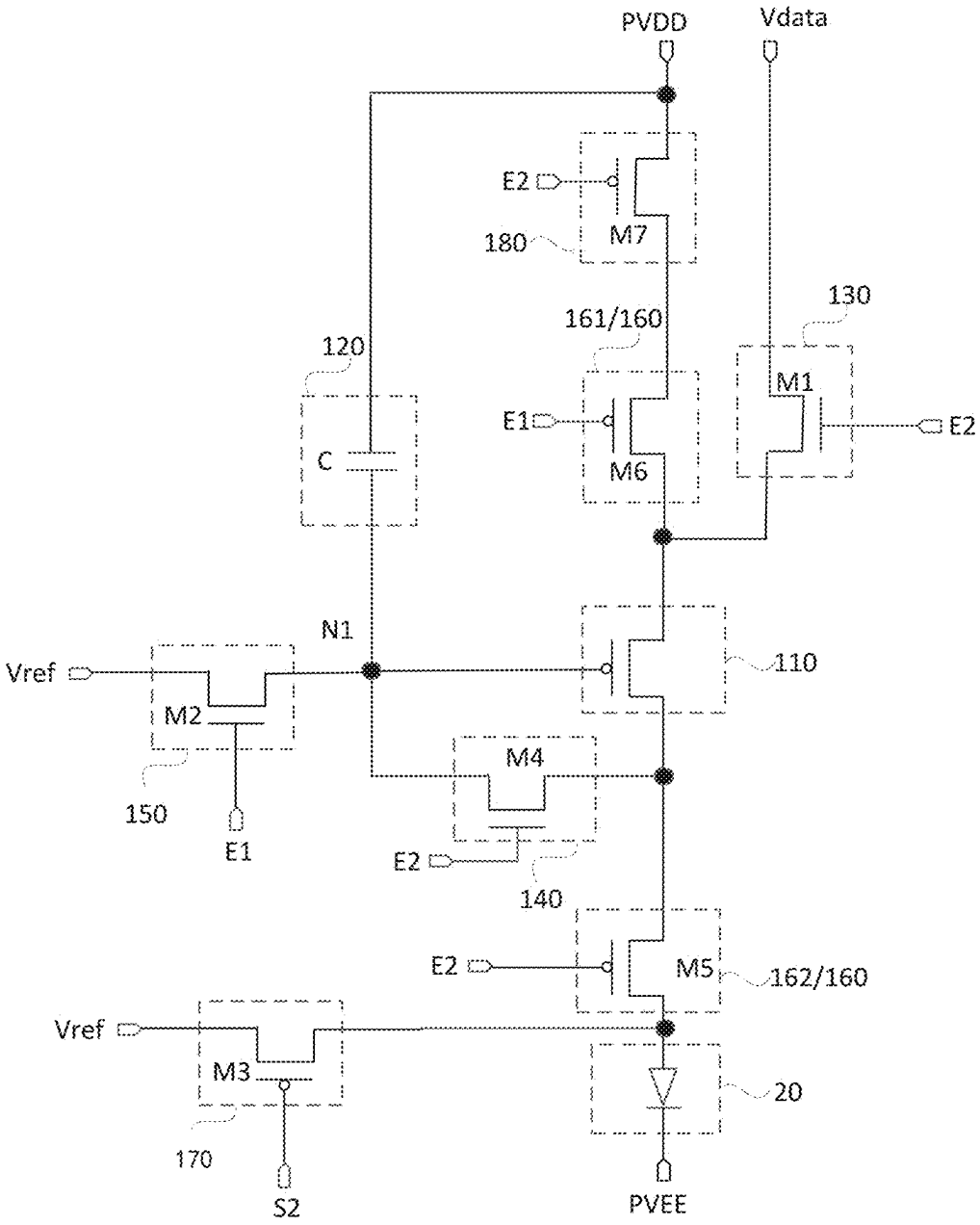

PVDD
Vdata
E2
M7
180
130
161/160
120
M1
E1
E2
C
M6
N1
Vref
110
M2
M4
150
E1
E2
140
E2
M5
162/160
Vref
M3
20
170
S2
PVEE

FIG. 38

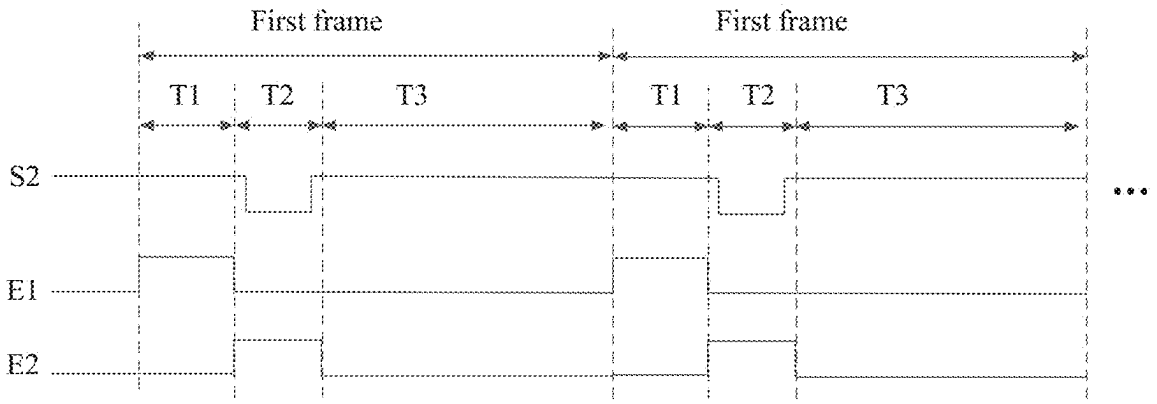


FIG. 39

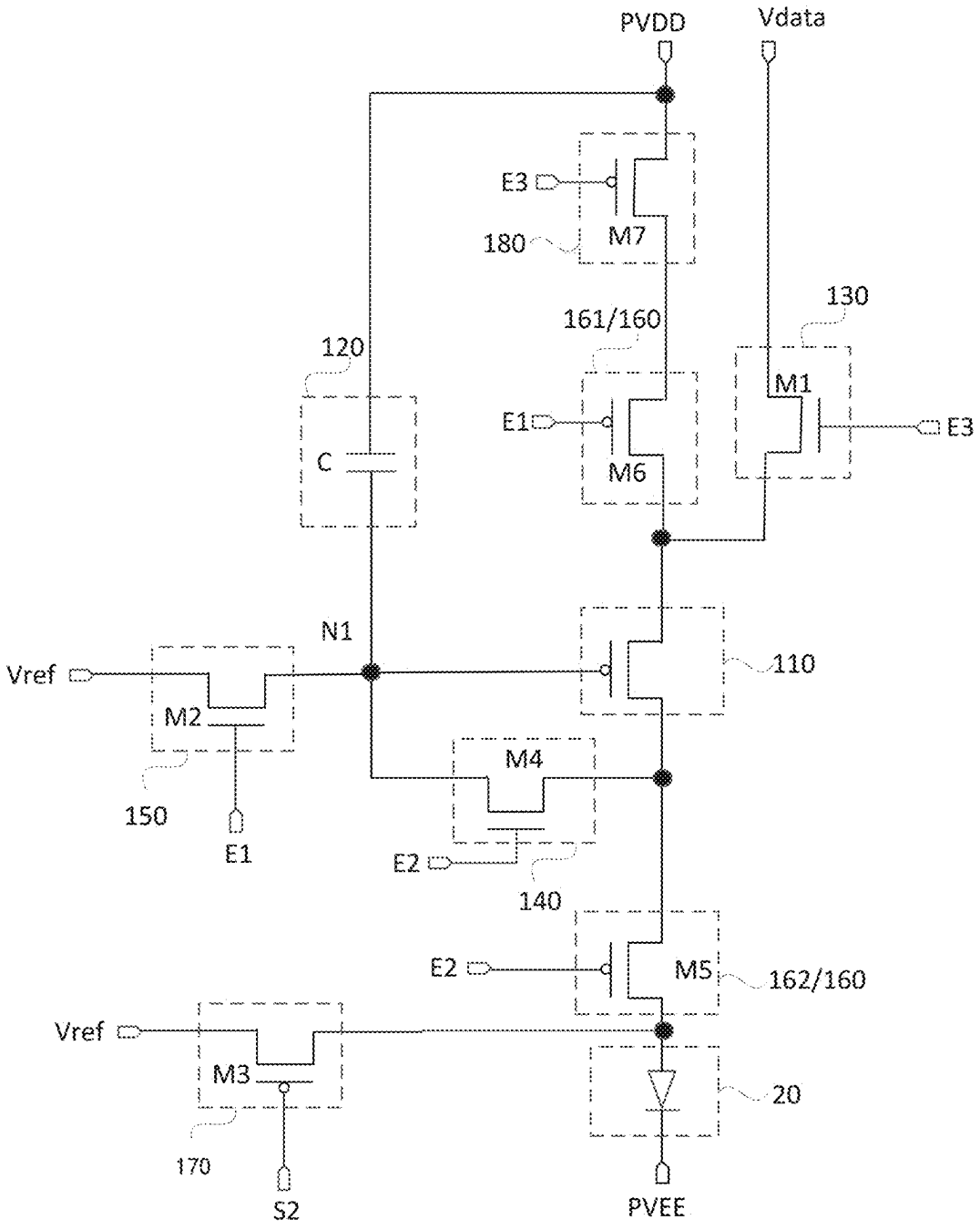

PVDD
Vdata
E3
180
M7
130
161/160
120
M1
E1
E3
C
M6
N1
Vref
110
M2
M4
150
E1
E2
140
E2
M5
162/160
Vref
M3
20
170
S2
PVEE

FIG. 41

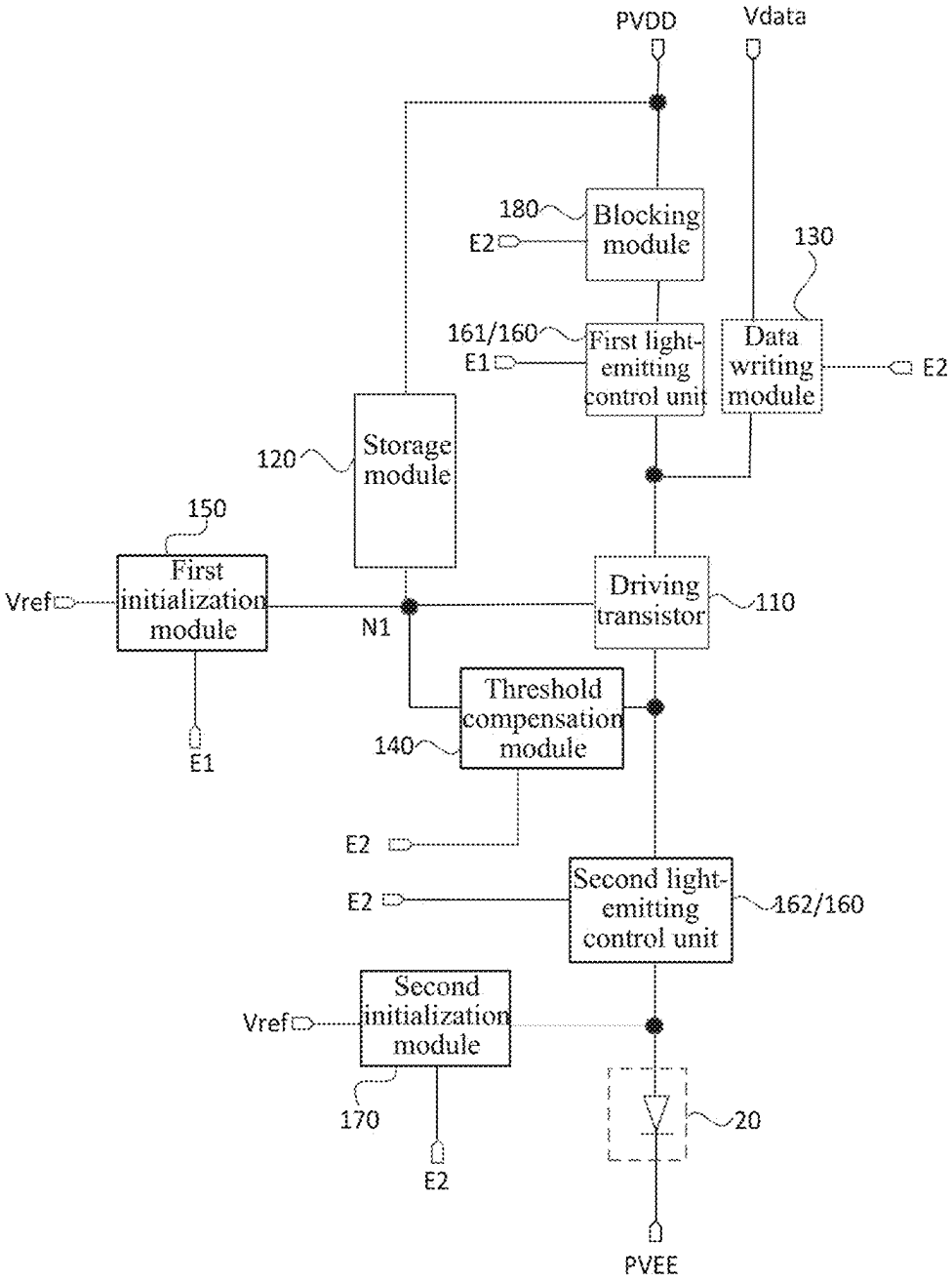

PVDD
Vdata
180
Blocking module
E2
130
161/160
First light-emitting control unit
E1
Data writing module
E2
120
Storage module
150
First initialization module
Vref
N1
Driving transistor
110
Threshold compensation module
140
E1
E2
E2
Second light-emitting control unit
162/160
Second initialization module
Vref
170
E2
20
PVEE

FIG. 41

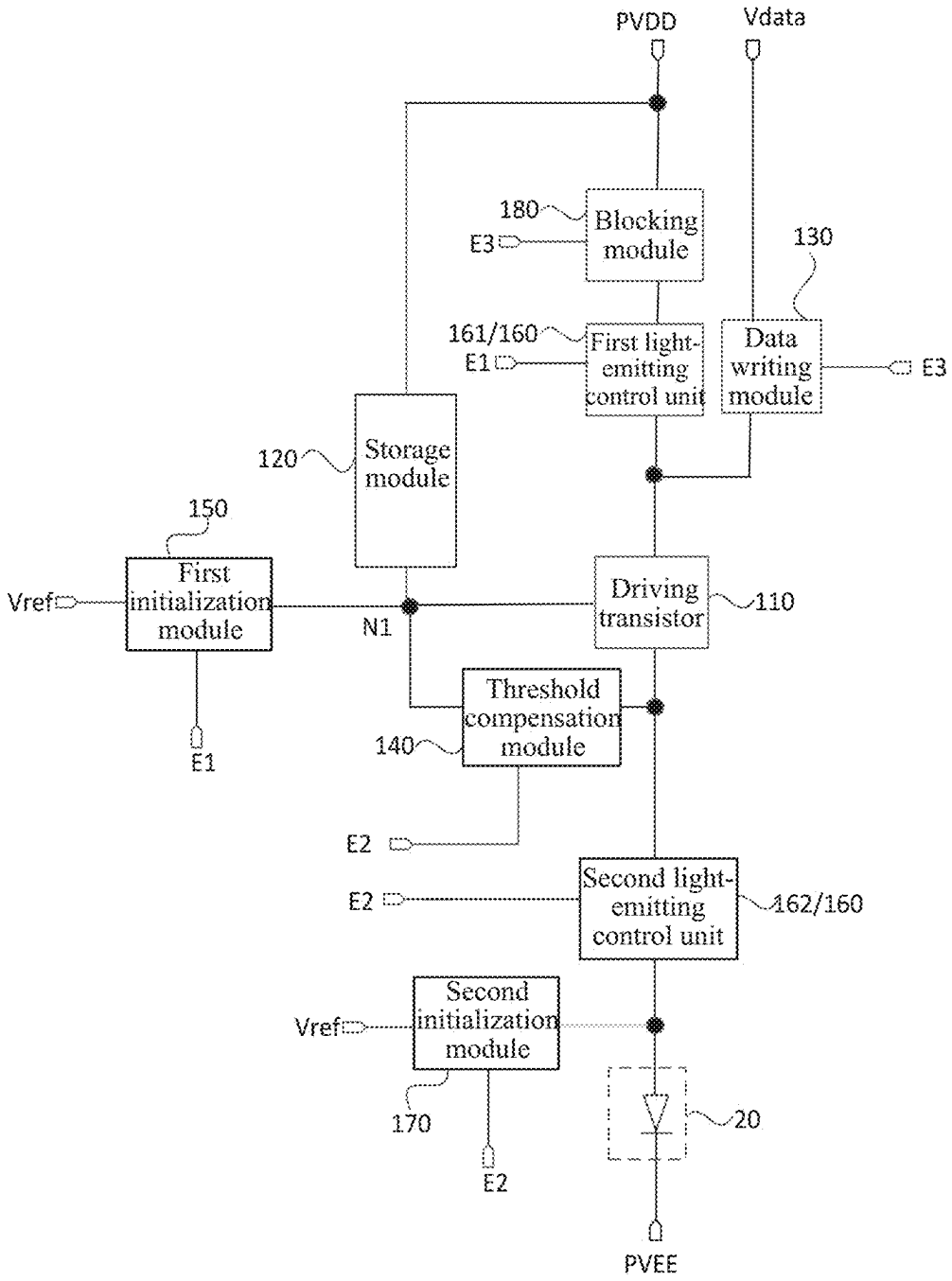

PVDD
Vdata
180
E3
Blocking module
130
161/160
E1
First light-emitting control unit
Data writing module
E3
120
Storage module
150
Vref
First initialization module
N1
Driving transistor
110
E1
Threshold compensation module
140
E2
E2
Second light-emitting control unit
162/160
Vref
Second initialization module
170
E2
20
PVEE

FIG. 42

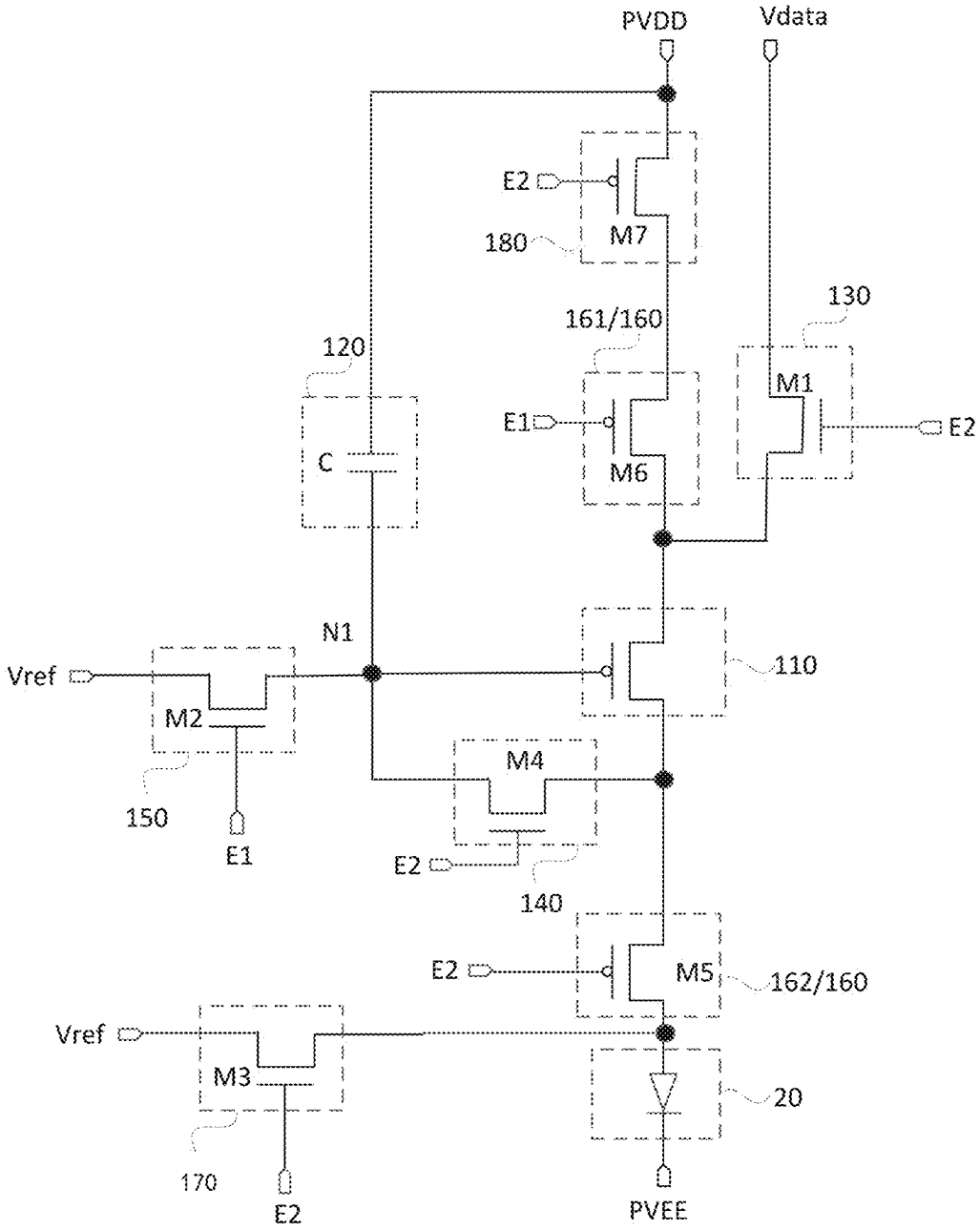

PVDD
Vdata
E2
M7
180
130
161/160
120
M1
E1
E2
C
M6
N1
Vref
110
M2
M4
150
E1
E2
140
E2
M5
162/160
Vref
M3
20
170
E2
PVEE

FIG. 43

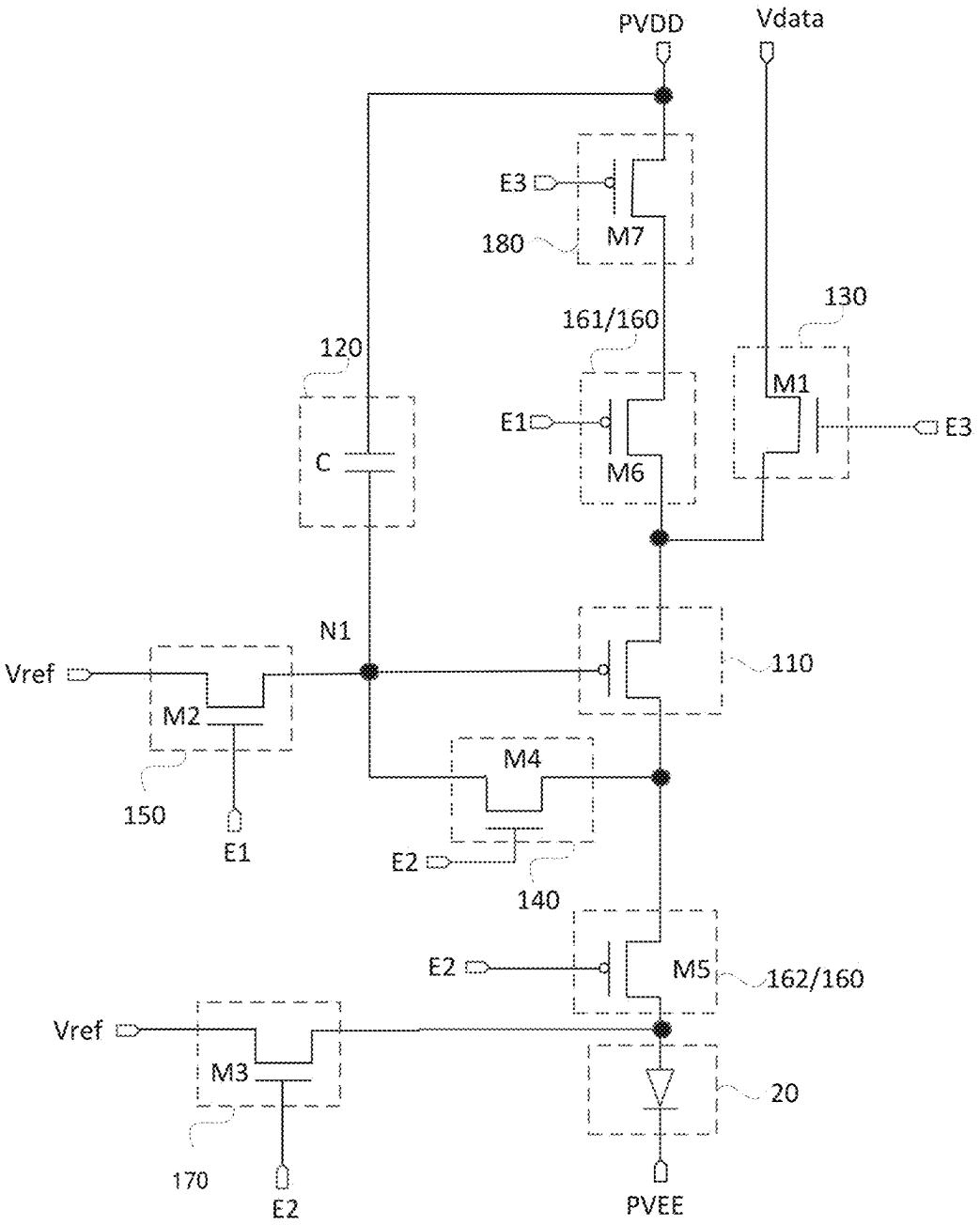

PVDD
Vdata
E3
180
M7
130
161/160
120
M1
E1
E3
C
M6
N1
110
Vref
M2
M4
150
E1
E2
140
E2
M5
162/160
Vref
M3
20
170
E2
PVEE

FIG. 44

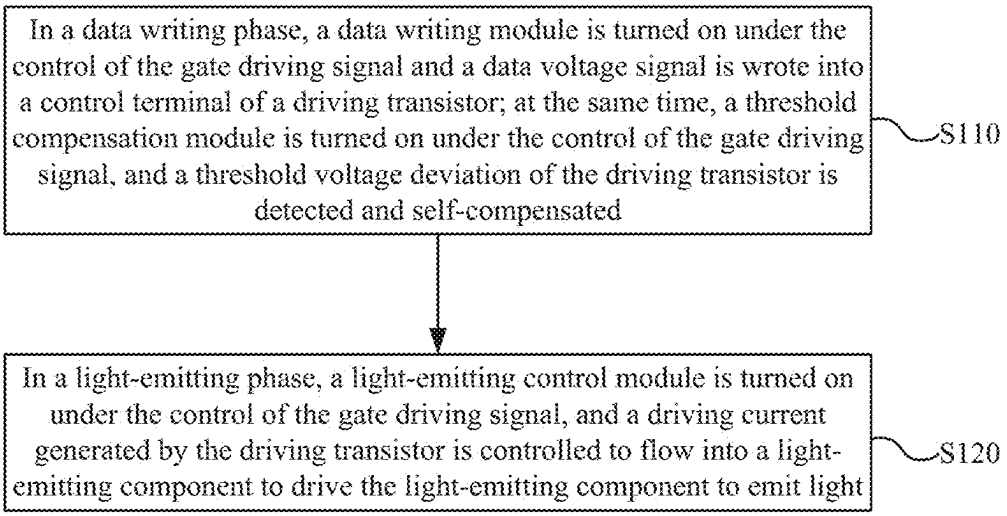

In a data writing phase, a data writing module is turned on under the control of the gate driving signal and a data voltage signal is wrote into a control terminal of a driving transistor; at the same time, a threshold compensation module is turned on under the control of the gate driving signal, and a threshold voltage deviation of the driving transistor is detected and self-compensated
S110
In a light-emitting phase, a light-emitting control module is turned on under the control of the gate driving signal, and a driving current generated by the driving transistor is controlled to flow into a light-emitting component to drive the light-emitting component to emit light
S120

FIG. 45

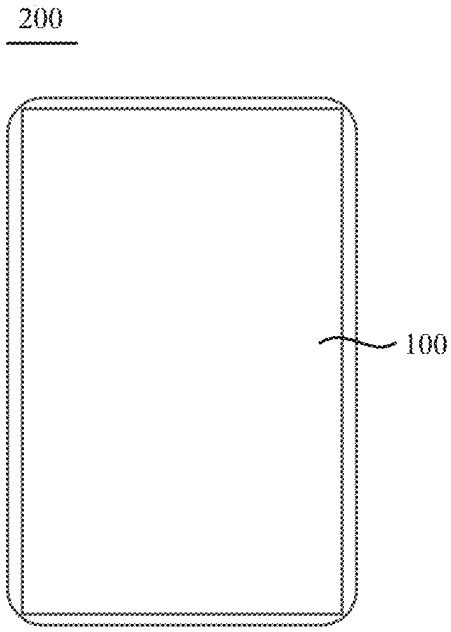

200
100

FIG. 46

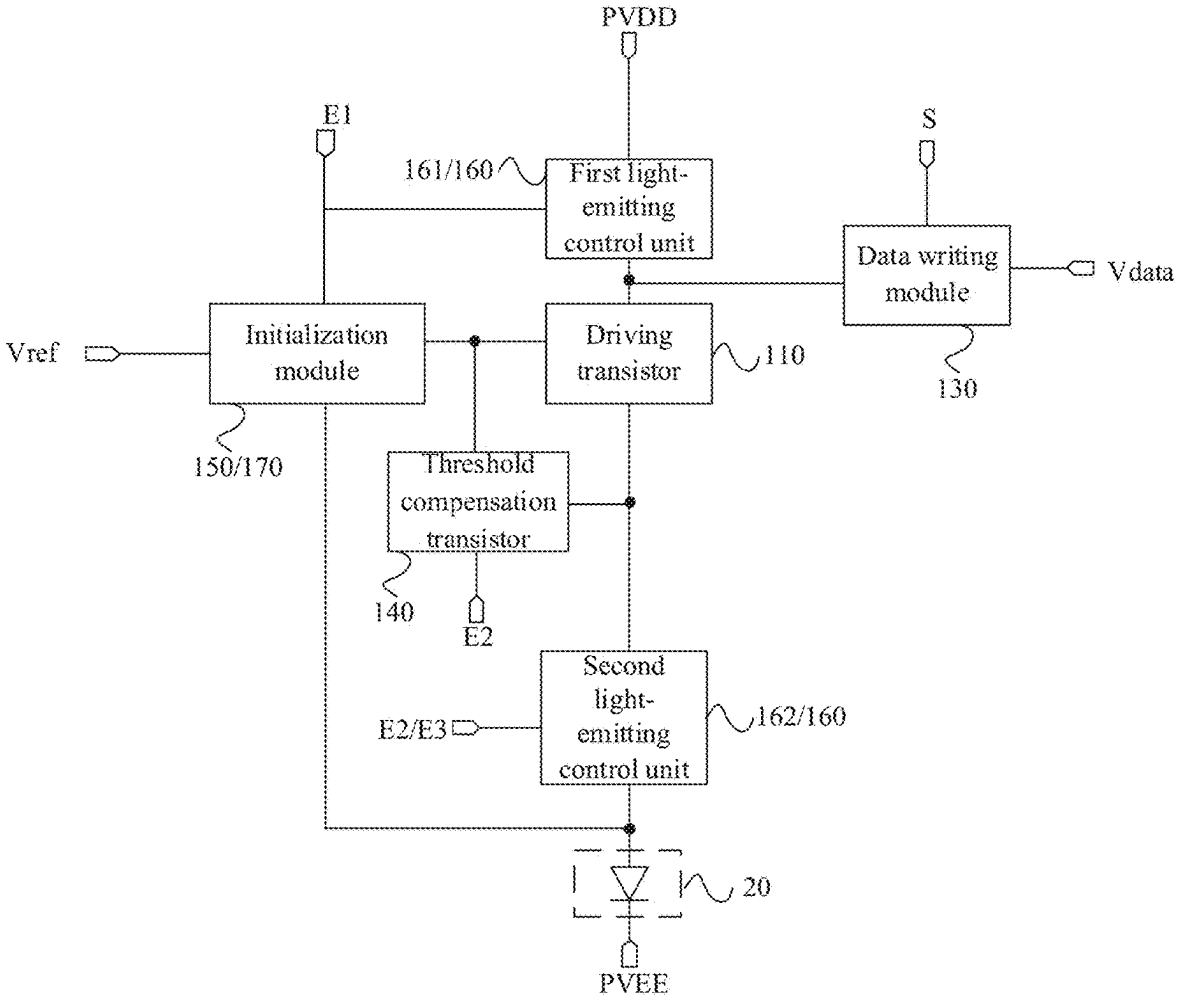

PVDD
E1
S
161/160
First light-emitting control unit
Data writing module
Vdata
Vref
Initialization module
Driving transistor
110
130
150/170
Threshold compensation transistor
140
E2
Second light-emitting control unit
E2/E3
162/160
20
PVEE

FIG. 47

DISPLAY PANEL, DRIVING METHOD AND DISPLAY DEVICE

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a continuation application of U.S. application Ser. No. 18/202,528 filed on May 26, 2023, which is a continuation application of U.S. application Ser. No. 17/103,329 filed on Nov. 24, 2020, which claims priority to Chinese patent application NO. 202010784841.1 filed on Aug. 6, 2020, the disclosures of all of which are incorporated herein by reference in their entireties.

TECHNICAL FIELD

[0002] Embodiments of the present disclosure relate to the field of display technologies and, in particular, to a display panel, a driving method, and a display device.

BACKGROUND

[0003] A light-emitting display panel usually includes a display area and a non-display area. The display area is provided with multiple pixel driving circuits and light-emitting components. The pixel driving circuit is used for driving the light-emitting components to emit light for displaying images. The non-display area is provided with a gate driving circuit to provide a control signal for the pixel driving circuit, so that the light-emitting components are lit up row by row under the driving of the pixel driving circuits.

[0004] At present, for an organic light-emitting display panel, a 7TIC-type pixel driving circuit usually requires at least three gate driving circuits to provide a control signal for this pixel driving circuit. Therefore, the non-display area needs to reserve positions for three gate driving circuits, which is not beneficial to implementing the narrow bezel.

SUMMARY

[0005] The present disclosure provides a display panel, a driving method and a display device to reduce the number of gate driving circuits, the cost, and the frame width.

[0006] In a first aspect, an embodiment of the present disclosure provides a display panel, including a gate driving circuit, a pixel driving circuit, and a light-emitting component; the pixel driving circuit includes a driving transistor, a data writing module, a threshold compensation module, and a light-emitting control module.

[0007] The data writing module is used for transmitting a data voltage signal to a control terminal of the driving transistor such that the driving transistor generates a driving current according to the data voltage signal provided by a data signal terminal.

[0008] The threshold compensation module is used for detecting and self-compensating a threshold voltage deviation of the driving transistor.

[0009] The light-emitting control module is connected in series between a first power signal terminal and the light-emitting component.

[0010] A transistor in the threshold compensation module is a P-type transistor and a transistor in the light-emitting control module is an N-type transistor, or the transistor in the threshold compensation module is an N-type transistor and the transistor in the light-emitting control module is a P-type transistor; a control terminal of the threshold compensation module and a control terminal of the light-emitting control module are electrically connected to a same gate driving circuit.

[0011] In a second aspect, an embodiment of the present disclosure further provides a driving method of a display panel. The driving method is applicable to the display panel described in the first aspect and includes steps described below.

[0012] In a data writing phase, a data writing module is turned on under the control of the gate driving signal and a data voltage signal is written into a control terminal of a driving transistor; at the same time, a threshold compensation module is turned on under the control of the gate driving signal, and a threshold voltage deviation of the driving transistor is detected and self-compensated.

[0013] In a light-emitting phase, a light-emitting control module is turned on under the control of the gate driving signal, and a driving current generated by the driving transistor is controlled to flow into a light-emitting component to drive the light-emitting component to emit light.

[0014] The threshold compensation module and the light-emitting control module are controlled by the gate driving signal output by a same gate driving circuit, and the threshold compensation module is turned on in response to the gate driving signal being at a first level, and the light-emitting control module is turned on in response to the gate driving signal being at a second level; the first level and the second level are different.

[0015] In a third aspect, an embodiment of the present disclosure further provides a display device including the display panel described in the first aspect.

[0016] In the display panel provided by the embodiment of the present disclosure, through configuring a same gate driving circuit to provide the control signal for the threshold compensation module and the light-emitting control module, there is no need to separately provide a gate driving circuit for the threshold compensation module, which reduces the total number of gate driving circuits for providing the control signal for the pixel driving circuit, thereby reducing the width of the frame area, solving the problem of low screen-to-body ratio and achieving the effect of reducing the number of gate driving circuits, the cost and the frame.

BRIEF DESCRIPTION OF DRAWINGS

[0017] FIG. **1** is a schematic diagram showing circuit components of a pixel driving circuit provided by the related art;

[0018] FIG. **2** is a driving timing graph illustrating a pixel driving circuit illustrated in FIG. **1**;

[0019] FIG. **3** is a structural diagram of a display panel provided by an embodiment of the present disclosure;

[0020] FIG. **4** is a block diagram of a pixel driving circuit provided by an embodiment of the present disclosure;

[0021] FIG. **5** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **4**;

[0022] FIG. **6** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure;

[0023] FIG. **7** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **6**;

[0024] FIG. **8** is a block diagram of a gate driving circuit provided by an embodiment of the present disclosure;

[0025] FIG. **9** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure;

[0026] FIG. **10** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **9**;

[0027] FIG. **11** is a driving timing graph provided by an embodiment of the present disclosure;

[0028] FIG. **12** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure;

[0029] FIG. **13** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **12**;

[0030] FIG. **14** is a block diagram of a pixel driving circuit provided by an embodiment of the present disclosure;

[0031] FIG. **15** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **14**;

[0032] FIG. **16** is another driving timing graph provided by an embodiment of the present disclosure;

[0033] FIG. **17** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure;

[0034] FIG. **18** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **17**;

[0035] FIG. **19** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure;

[0036] FIG. **20** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **19**;

[0037] FIG. **21** is another driving timing graph provided by an embodiment of the present disclosure;

[0038] FIG. **22** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure;

[0039] FIG. **23** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **22**;

[0040] FIG. **24** is a block diagram of a pixel driving circuit provided by an embodiment of the present disclosure;

[0041] FIG. **25** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **24**;

[0042] FIG. **26** is another driving timing graph provided by an embodiment of the present disclosure;

[0043] FIG. **27** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure;

[0044] FIG. **28** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **27**;

[0045] FIG. **29** is another schematic diagram of circuit components of a pixel driving circuit shown in FIG. **27**;

[0046] FIG. **30** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure;

[0047] FIG. **31** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure;

[0048] FIG. **32** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **30**;

[0049] FIG. **33** is a diagram illustrating a driving timing sequence provided by an embodiment of the present disclosure;

[0050] FIG. **34** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **31**;

[0051] FIG. **35** is another driving timing graph provided by an embodiment of the present disclosure;

[0052] FIG. **36** is a block diagram of a pixel driving circuit provided by an embodiment of the present disclosure;

[0053] FIG. **37** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure;

[0054] FIG. **38** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **36**;

[0055] FIG. **39** is another driving timing graph provided by an embodiment of the present disclosure;

[0056] FIG. **40** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **37**;

[0057] FIG. **41** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure;

[0058] FIG. **42** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure;

[0059] FIG. **43** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **41**;

[0060] FIG. **44** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **42**;

[0061] FIG. **45** is a flowchart of a driving method of a display panel provided by an embodiment of the present disclosure;

[0062] FIG. **46** is a structural diagram of a display device provided by an embodiment of the present disclosure; and

[0063] FIG. **47** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0064] Hereinafter the present disclosure will be further described in detail in conjunction with the drawings and embodiments. It is to be understood that the embodiments set forth herein are intended to explain the present disclosure and not to limit the present disclosure. Additionally, it is to be noted that for ease of description, merely part, not all, of the structures related to the present disclosure are illustrated in the drawings.

[0065] FIG. **1** is a schematic diagram showing circuit components of a pixel driving circuit provided by the related art. FIG. **2** is a driving timing graph illustrating a pixel driving circuit illustrated in FIG. **1**. Referring to FIG. **1**, the pixel driving circuit includes: a driving transistor **110'**, a storage module **120'**, a data writing module **130'**, a threshold compensation module **140'**, a first initialization module **150'**, a second initialization module **160'**, and a light-emitting control module **170'**. The gate driving circuit used for providing a control signal for the pixel driving circuit includes a first gate driving circuit, a second gate driving circuit, and a third gate driving circuit. The first gate driving circuit provides the control signal for the first initialization module **110'** and the threshold compensation module **140'**. Specifically, the first gate driving circuit includes multiple cascaded first gate driving units, a control terminal of the first initialization module **150'** is electrically connected to an output terminal SN-1 of the first gate driving unit at a previous stage; a control terminal of the threshold compensation module **140'** is electrically connected to an output terminal SN-2 of the first gate driving unit at a current stage. The second gate driving circuit provides the control signal for the second initialization module **160'** and the data writing module **130'**. Specifically, the second gate driving circuit includes multiple second gate driving units. A control terminal of the second initialization module **160'** is electrically connected to an output terminal SP-1 of the second gate driving unit at a previous stage, and a control terminal of the data writing module **130'** is electrically connected to an output terminal SP-2 of the second gate driving unit at a current stage. The third gate driving circuit provides the control signal for the light-emitting control module **170'**. Specifically, the third gate driving circuit includes multiple cascaded third gate driving units, and a control terminal of the light-emitting control module **170'** is electrically connected to an output terminal E**2** of the third gate driving unit at a current stage. It can be seen that the display panel including the pixel driving circuit needs to reserve space for

the three gate driving circuits in a non-display area, which is not beneficial to implementing the narrow bezel.

[0066] In view of the above problems, an embodiment of the present disclosure provides a display panel, including a gate driving circuit, a pixel driving circuit, and a light-emitting component; the pixel driving circuit includes a driving transistor, a data writing module, a threshold compensation module, and a light-emitting control module.

[0067] The data writing module is used for transmitting a data voltage signal to a control terminal of the driving transistor such that the driving transistor generates a driving current according to the data voltage signal provided by a data signal terminal.

[0068] The threshold compensation module is used for detecting and self-compensating a threshold voltage deviation of the driving transistor;

[0069] The light-emitting control module is connected in series between a first power signal terminal and the light-emitting component.

[0070] A transistor in the threshold compensation module is a P-type transistor and a transistor in the light-emitting control module is an N-type transistor, or the transistor in the threshold compensation module is an N-type transistor and the transistor in the light-emitting control module is a P-type transistor; a control terminal of the threshold compensation module and a control terminal of the light-emitting control module are electrically connected to a same gate driving circuit.

[0071] The preceding is the core idea of this application, and technical solutions in embodiments of the present disclosure will be described clearly and completely in conjunction with the drawings in embodiments of the present disclosure. Apparently, the embodiments described below are part, not all of the embodiments of the present disclosure. Based on embodiments of the present disclosure, all other embodiments obtained by those skilled in the art without creative work are within the scope of the present disclosure.

[0072] FIG. **3** is a structural diagram of a display panel provided by an embodiment of the present disclosure. FIG. **4** is a block diagram of a pixel driving circuit provided by an embodiment of the present disclosure. FIG. **5** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **4**. Referring to FIGS. **3** to **5**, a display panel includes: a gate driving circuit **30**, a pixel driving circuit **10**, and a light-emitting component **20**; the pixel driving circuit **10** includes a driving transistor **110**, a data writing module **130**, a threshold compensation module **140** and a light-emitting control module **160**. The data writing module **130** is used for transmitting a data voltage signal to a control terminal of the driving transistor **110** such that the driving transistor **110** generates a driving current according to the data voltage signal provided by a data signal terminal. The threshold compensation module **140** is used for detecting and self-compensating a threshold voltage deviation of the driving transistor **110**. The light-emitting control module **160** is connected in series between a first power signal terminal PVDD and the light-emitting component **20**. A transistor in the threshold compensation module **140** is a P-type transistor and a transistor in the light-emitting control module **160** is an N-type transistor, or the transistor in the threshold compensation module **140** is an N-type transistor and the transistor in the light-emitting control module **160** is P-type transistor; a control terminal (not shown in FIGS. **4** and **5**) of the threshold compensation module **140** and a control terminal (not shown in FIGS. **4** and **5**) of the light-emitting control module **160** are electrically connected to a same gate driving circuit **30**.

[0073] Referring to FIGS. **4** and **5**, optionally, the driving transistor **110** is electrically connected between the data writing module **130** and the threshold compensation module **140**; the data writing module **130** is electrically connected to a data line signal terminal Vdata and a first terminal of the driving transistor **110**; a first terminal of the threshold compensation module **140** and the control terminal of the driving transistor **110** are electrically connected to a first node N**1**, and a second terminal of the threshold compensation module **140** is electrically connected to a second terminal of the driving transistor **110**.

[0074] Referring to FIGS. **4** and **5**, optionally, a control terminal (not shown in FIGS. **4** and **7**) of the data writing module **130** is electrically connected to the gate driving circuit **30**.

[0075] FIG. **6** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure. FIG. **7** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **6**. Referring to FIGS. **3**, **6**, and **7**, a display panel further includes a first initialization module **150**. A control terminal (not shown in FIGS. **6** and **7**) of the first initialization module **150** is electrically connected to a gate driving circuit **30**; and the first initialization module **150** is used for providing an initialization voltage signal to a control terminal of a driving transistor.

[0076] Referring to FIGS. **6** and **7**, optionally, the display panel further includes a storage module **120** which is electrically connected between a first power signal terminal PVDD and the control terminal of the driving transistor and is used for stabilizing a voltage of the control terminal of the driving transistor in a light-emitting phase.

[0077] Specifically, the display panel includes a display area AA and a non-display area DA around the display area AA. The display area AA is provided with multiple sub-pixels. Each sub-pixel includes a pixel driving circuit **10** and a light-emitting component **20**. The pixel driving circuit **10** is configured to drive the light-emitting component **20** to emit light to display image information. The non-display area DA is used for setting peripheral circuits such as a gate driving circuit **30**. Exemplarily, FIG. **8** is a block diagram of a gate driving circuit provided by an embodiment of the present disclosure. Referring to FIG. **8**, the gate driving circuit **30** includes N cascaded gate driving units **310**, where a gate driving unit (i) represents an i-th stage gate driving unit. The meaning of cascade is that an output terminal OUT of the i-th stage gate driving unit is electrically connected to an input terminal IN of an (i+1)-th stage gate driving unit, and an input terminal IN of a first stage gate driving unit is electrically connected to an enabling signal terminal STV of the display panel, where N is a positive integer greater than or equal to 1, i is an integer, and $1 \leq i \leq N-1$. An output terminal of each gate driving unit **310** may output a gate driving signal which is used for controlling turn-on and turn-off of the data writing module **130**, the threshold compensation module **140**, the first initialization module **150**, and the light-emitting control module **160** in the pixel driving circuit **10**, thereby enabling the pixel driving circuit **10** to drive the light-emitting component **20** to emit light.

[0078] Specifically, in the pixel driving circuit **10**, an initialization signal terminal Vref is used for receiving the initialization voltage signal, a first power signal terminal

PVDD is used for receiving a first power voltage signal, and a data line signal terminal Vdata is used for receiving a data voltage signal. The brightness of the light-emitting component **20** driven by the pixel driving circuit **10** is determined by the voltage value of the data voltage signal. Exemplarily, the initialization voltage signal, the first power voltage signal, and the data voltage signal may all be provided by a driving IC.

[0079] Specifically, a first terminal of the first initialization module **150** is electrically connected to the initialization signal terminal Vref. The first initialization module **150** is at least turned on in an initialization phase, and writes the initialization voltage signal into a first node N**1**, so that the driving transistor **110** is able to be turned on in a data writing phase, and further the data voltage signal is able to be written into the first node N**1**. It should be noted that FIGS. **6** and **7** only exemplarily show that a second terminal of the first initialization module **150** is electrically connected to a second terminal of the driving transistor **110**, but this is not a limitation to the present disclosure. For example, in other embodiments, the second terminal of the first initialization module **150** may also be electrically connected to the first node N**1**. It should also be noted that by reasonably configuring a connection position of the second terminal of the first initialization module **150** in the pixel driving circuit **10**, and reasonably configuring a connection mode between each module in the pixel driving circuit **10** and the gate driving unit in the gate driving circuit **30**, the first initialization module **150** may also be used for providing the initialization voltage signal for an anode of the light-emitting component **20** in some embodiments. This part of contents will be described in detail later and not be described here. Referring to FIG. **7**, optionally, the first initialization module **150** includes a second transistor M**2**. A first terminal of the second transistor M**2** is electrically connected to the initialization signal terminal Vref. What kind of device is connected to a second terminal of the second transistor M**2** will be described in detail later, a control terminal of the second transistor M**2** is electrically connected to an output terminal of the gate driving circuit **30**.

[0080] Specifically, the storage module **120** may include one capacitor C (as shown in FIG. **7**), or multiple capacitors C connected in parallel. The storage module **120** is used for storing a voltage provided by the data voltage signal in a data writing phase to maintain the voltage of the first node N**1** almost unchanged in the entire light-emitting phase. Specifically, the driving transistor **110** is used for generating a driving current having a corresponding size according to a size of the data voltage signal in the light-emitting phase, so that the light-emitting brightness of the light-emitting component **20** matches the size of the data voltage signal.

[0081] Specifically, in the data writing phase, the data writing module **130** is turned on under the control of the gate driving signal, and writes the data voltage signal of the data signal terminal Vdata into the first node N**1**, and at the same time, the threshold compensation module **14** is turned on under the control of the gate driving signal and compensates a threshold voltage of the driving transistor **110** to the first node N**1**. Referring to FIG. **7**, optionally, the data writing module **130** includes a first transistor M**1**, a first terminal of the first transistor M**1** is electrically connected to the data signal terminal Vdata, a second terminal of the first transistor M**1** is electrically connected to the first terminal of the driving transistor **110**, and a control terminal of the first transistor M**1** is electrically connected to the output terminal of the gate driving circuit **30**. Optionally, the threshold compensation module **140** includes a fourth transistor M**4**, a first terminal of the fourth transistor M**4** is electrically connected to the first node N**1**, a second terminal of the fourth transistor M**4** is electrically connected to the second terminal of the driving transistor **110**, and a control terminal of the fourth transistor M**4** is electrically connected to the output terminal of the gate driving circuit **30**.

[0082] Referring to FIG. **4**, optionally, the light-emitting control module **160** includes a first light-emitting control unit **161** and a second light-emitting control unit **162**; the first light-emitting control unit **161** is electrically connected between the first power signal terminal PVDD and the first terminal of the driving transistor **110**; and the second light-emitting control unit **162** is electrically connected between the second terminal of the driving transistor **110** and the light-emitting component **20**. Referring to FIG. **7**, optionally, the first light-emitting control unit **161** includes a sixth transistor M**6**, a first terminal of the sixth transistor M**6** is electrically connected to the first power signal terminal PVDD, and a second terminal of the sixth transistor M**6** is electrically connected to the first terminal of the driving transistor **110**, and a gate of the sixth transistor M**6** is electrically connected to the output terminal of the gate driving circuit **30**; the second light-emitting control unit **162** includes a fifth transistor M**5**, and a first terminal of the fifth transistor M**5** is electrically connected to the second terminal of the driving transistor **110**, a second terminal of the fifth transistor M**5** is electrically connected to the anode of the light-emitting component **20**, a cathode of the light-emitting component **20** is electrically connected to the second power signal terminal PVEE, and the second power signal terminal PVEE is used for receiving a second power voltage signal, exemplarily, the second power voltage signal may be provided by the driving IC.

[0083] Specifically, a working process of the pixel driving circuit **10** usually includes the initialization phase, the data writing phase, and the light emitting phase. In the initialization phase, the first initialization module **150** is turned on under the control of the gate driving signal, and at least writes the initialization voltage signal into the first node N**1** to initialize the first node N**1**. In the data writing phase, the data writing module **130** is turned on under the control of the gate driving signal and writes the data voltage signal into the first node N**1**, and at the same time, the threshold compensation module **140** is turned on under the control of the gate driving signal and compensates the threshold voltage of the driving transistor **110** to the first node N**1**. In the light-emitting phase, the light-emitting control module **160** is turned on under the control of the gate driving signal, and controls the driving current generated by the driving transistor **110** to flow into the light-emitting component **20** to drive the light-emitting component **20** to emit light. Specifically, how the gate driving signal output by each gate driving unit controls the data writing module **130**, the threshold compensation module **140**, the first initialization module **150**, and the light-emitting control module **160** in the corresponding pixel driving circuit **10** will be described later in detail, and thus no further details are provided herein.

[0084] It is understandable that since the threshold compensation module **140** and the light-emitting control module **160** are provided with the gate driving signal by a same gate driving circuit **30**, compared with the related art, at least one

gate driving circuit **30** may be saved in the display panel, according to design concepts of saving the cost and reducing the frame, optionally, the display panel includes at most two gate driving circuits **30**. Specifically, the display panel may include one or two gate driving circuits **30**. Compared with a case where at least three gate driving circuits **30** need to be configured in the existing art, at most two gate driving circuits **30** are configured to provide the control signal for the pixel driving circuit **10**, which may reduce a size of a space reserved by the non-display area DA, thereby reducing the frame area.

[0085] In the display panel provided by the embodiment of the present disclosure, through configuring a same gate driving circuit to provide the control signal for the threshold compensation module and the light-emitting control module, there is no need to separately provide a gate driving circuit for the threshold compensation module, which reduces the total number of gate driving circuits for providing the control signal for the pixel driving circuit, thereby reducing the width of the frame area, solving the problem of low screen-to-body ratio and implementing the effect of reducing the number of gate driving circuits, the cost and the frame.

[0086] Specifically, when the display panel includes one gate driving circuit **30** or two gate driving circuits **30**, there are many specific implementation modes of the pixel driving circuit **10** and specific connection modes of the gate driving circuit **30** and the pixel driving circuit **10**. Typical examples are described below, but the present application is not limited thereto.

[0087] FIG. **9** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure. Referring to FIGS. **3** and **7**, optionally, a display panel includes a first gate driving circuit **30**A and a second gate driving circuit **30**B. The first gate driving circuit **30**A includes multiple cascaded first gate driving units, and the second gate driving circuit **30**B includes multiple cascaded second gate driving units. A control terminal of a data writing module **130** is electrically connected to an output terminal S**2** of the second gate driving unit at a current stage; a control terminal of a first light-emitting control unit **161** and a control terminal of a threshold compensation module **140** are electrically connected to an output terminal E**2** of the first gate driving unit at a current stage; a control terminal of a second light-emitting control unit **162** is electrically connected to an output terminal E**2** of the first gate driving unit at a current stage; a first initialization module **150** is electrically connected between an initialization signal terminal Vref and a second terminal of a driving transistor **110**, and a control terminal of the first initialization module **150** is electrically connected to an output terminal S**1** of the second gate driving unit at a previous stage.

[0088] Specifically, for a certain pixel driving circuit **10** in the display panel, the first gate driving unit at the current stage, the first gate driving unit at the subsequent stage, the second gate driving unit at the previous stage, and the second gate driving unit at the current stage corresponding to the certain pixel driving circuit **10** is related to a specific position of the certain pixel driving circuit **10** in the display panel. Optionally, multiple pixel driving circuits **10** are arranged in X rows and Y columns. The first gate driving circuit **30**A includes X-stage cascaded first gate driving units, and the second gate driving circuit **30**B includes (X+1)-stage cascaded second gate driving units. The first gate driving unit at the current stage of the pixel driving circuit **10** located in a j-th row is a first gate driving unit in a j-th stage, and the second gate driving unit at the current stage is a second gate driving unit in a (j+1)-th stage, the second gate driving unit at the previous stage is a second gate driving unit in a j-th stage, where X and Y are both positive integers greater than or equal to 1, and $1 \leq j \leq X$.

[0089] FIG. **10** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **9**. FIG. **11** is a driving timing graph provided by an embodiment of the present disclosure. A working process of the pixel driving circuit **10** shown in FIG. **10** at a driving timing shown in FIG. **11** is as follows.

[0090] In a T**1** phase, i.e., in an initialization phase, a second gate driving signal at the previous stage output by the output terminal S**1** of the second gate driving unit at the previous stage is a logic low-level signal, and a second transistor M**2** is turned on; the second gate driving signal at the current stage output by the output terminal S**2** of the second gate driving unit is a logic high-level signal, and a first transistor M**1** is turned off; the first gate driving signal at the current stage output by the output terminal E**2** of the first gate driving unit at the current stage is a logic high-level signal, a fourth transistor M**4** is turned on, and a fifth transistor M**5** and a sixth transistor M**6** are turned off. The initialization voltage signal of the initialization signal terminal Vref is written into a first node N**1** through the turned-on second transistor M**2** and the turned-on fourth transistor M**4**, where the initialization voltage signal provided by the initialization signal terminal Vref is a logic low-level signal to ensure the driving transistor **110**M**3** in a next phase is able to be turned on.

[0091] In a T**2** stage, i.e., in a data writing phase, the second gate driving signal at the previous stage is the logic high-level signal, the second transistor M**2** is turned off; the second gate driving signal at the current stage is the logic low-level signal, the first transistor M**1** is turned on; and the first gate driving signal at the current stage is the logic high-level signal, the fourth transistor M**4** is turned on, and the fifth transistor M**5** and the sixth transistor M**6** are turned off. The data voltage signal Vd of the data signal terminal Vdata is written into the control terminal of the driving transistor **110** (i.e., the first node N**1**) and a first electrode plate of the capacitor C (i.e., an electrode plate connected to the driving transistor **110**) through the first transistor M**1**, the driving transistor **110**, and the fourth transistor M**4** sequentially, so that a voltage of the control terminal of the driving transistor **110** gradually increases until a voltage difference between the voltage of the control terminal of the driving transistor **110** and the voltage of a first terminal of the driving transistor **110** is equal to the threshold voltage Vth of the driving transistor **110**, that is, a voltage of the control terminal of the driving transistor $VN1=Vd-|Vth|$, where Vd is the data voltage signal provided by the data signal terminal Vdata; at the same time, the voltage of the control terminal of the driving transistor **110** is stored in the capacitor C.

[0092] In a T**3** stage, i.e., in a light-emitting phase, the second gate driving signal at the previous stage is the logic high-level signal, the second transistor M**2** is turned off; the second gate driving signal at the current stage is the logic high-level signal, the first transistor M**1** is turned off; and the first gate driving signal at the current stage is the logic low-level signal, the fourth transistor M**4** is turned off, and the fifth transistor M**5** and the sixth transistor M**6** are turned

on. The power signal voltage Vpvdd of the first power signal terminal PVDD is written into the first terminal of the driving transistor **110** through the turned-on sixth transistor M**6**. At this time, the voltage difference between the voltage of the first terminal of the driving transistor **110** and the voltage of the control terminal of the driving transistor **110** is Vsg=Vpvdd−Vd+|Vth|, the driving transistor **110** generates a driving current, the driving current flows into the light-emitting component **20** through the fifth transistor M**5**, and drives the light-emitting component **20** to emit light. A driving current I_d is:

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{sg} - |V_{th}|)^2 = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{pvdd} - V_d + |V_{th}| - |V_{th}|)^2 = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{pvdd} - V_d)^2$$

[0093] μ is a carrier mobility, C_{ox} is a channel capacitance C of the driving transistor **110** per unit area, and W/L is a width-to-length ratio of the driving transistor **110**.

[0094] FIG. **12** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure.

[0095] FIG. **13** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **12**.

[0096] A difference between a pixel driving circuit **10** shown in FIG. **12** and a pixel driving circuit **10** shown in FIG. **9** is that, optionally, the pixel driving circuit **10** further includes a second initialization module **170** which is electrically connected between an initialization signal terminal Vref and an anode of a light-emitting component **20**. A control terminal of the second initialization module **170** is electrically connected to an output terminal S**2** of a second gate driving unit at the current stage; the second initialization module **170** is used for providing an initialization voltage signal to the anode of the light-emitting component **20**. Referring to FIG. **13**, optionally, the second initialization module **170** includes a third transistor M**3**. A first terminal of the third transistor M**3** is electrically connected to the initialization signal terminal Vref, and a second terminal of the third transistor M**3** is connected to the anode of the light-emitting component **20**, a control terminal of the third transistor M**3** is electrically connected to the output terminal S**2** of the second gate driving unit at the current stage.

[0097] A working process of the pixel driving circuit **10** shown in FIG. **13** at the driving timing shown in FIG. **11** is as follows.

[0098] In a T**1** phase, i.e., in an initialization phase, a second gate driving signal at a previous stage output by an output terminal S**1** of the second gate driving unit at the previous stage is a logic low-level signal, and a second transistor M**2** is turned on; a second gate driving signal at the current stage output by the output terminal S**2** of the second gate driving unit at the current stage is a logic high-level signal, and a first transistor M**1** and a third transistor is turned off; a first gate driving signal at the current stage output by the output terminal E**2** of the first gate driving unit at the current stage is a logic high-level signal, a fourth transistor M**4** is turned on, and a fifth transistor M**5** and a sixth transistor M**6** are turned off. The initialization voltage signal of the initialization signal terminal Vref is written into a first node N**1** through the turned-on second transistor M**2** and the turned-on fourth transistor M**4**.

[0099] In a T**2** stage, i.e., in a data writing phase, the second gate driving signal at the previous stage is the logic high-level signal, the second transistor M**2** is turned off; the second gate driving signal at the current stage is the logic low-level signal, the first transistor M**1** and the third transistor M**3** is turned on; and the first gate driving signal at the current stage is the logic high-level signal, the fourth transistor M**4** is turned on, and the fifth transistor M**5** and the sixth transistor M**6** are turned off. The data voltage signal of the data signal terminal Vdata is written into a control terminal of the driving transistor **110** and a first electrode plate of the capacitor C through the first transistor M**1**, the driving transistor **110**, and the fourth transistor M**4** sequentially. Reference may be made to the previous contents for the specific process, and details are not described here again. At the same time, the initialization voltage signal of the initialization signal terminal Vref is written into the anode of the light-emitting component **20** through the turned-on third transistor M**3**, and an anode potential of the light-emitting component **20** is initialized, thus the influence of the voltage of the anode of the light-emitting component **20** in a previous frame on the voltage of the anode of the light-emitting component **20** in a subsequent frame is reduced and the uniformity of the display is improved.

[0100] In a T**3** stage, i.e., in a light-emitting phase, the second gate driving signal at the previous stage is the logic high-level signal, the second transistor M**2** is turned off; the second gate driving signal at the current stage is the logic high-level signal, the first transistor M**1** and the third transistor M**3** is turned off; and the first gate driving signal at the current stage is the logic low-level signal, the fourth transistor M**4** is turned off, and the fifth transistor M**5** and the sixth transistor M**6** are turned on. A power signal voltage of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on sixth transistor M**6**, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M**5** to drive the light-emitting component **20** to emit light.

[0101] FIG. **14** is a block diagram of a pixel driving circuit provided by an embodiment of the present disclosure. A difference between the pixel driving circuit shown in FIG. **14** and the pixel driving circuit shown in FIG. **9** is that, optionally, a control terminal of a second light-emitting control unit **162** is electrically connected to an output terminal E**3** of a first gate driving unit at a subsequent stage. A first initialization module **150** is used for providing an initialization voltage signal for a control terminal of a driving transistor and an anode of a light-emitting component **20**.

[0102] Optionally, multiple pixel driving circuits **10** are arranged in X rows and Y columns. The first gate driving circuit **30**A includes (X+1)-stage cascaded first gate driving units, and the second gate driving circuit **30**B includes (X+1)-stage cascaded second gate driving units. A first gate driving unit at a current stage of the pixel driving circuit **10** located in a j-th row is a first gate driving unit in a j-th stage, and a first gate driving unit at a subsequent stage is a first gate driving unit in a (j+1)-th stage, a second gate driving unit at the current stage is a second gate driving unit in a j-th stage, a second gate driving unit at a previous stage is a second gate driving unit in a j-th stage, where X and Y are both positive integers greater than or equal to 1, and 1≤j≤X.

[0103] FIG. **15** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **14**. FIG. **16** is another driving timing graph provided by an embodiment of the present disclosure. A working process of the pixel driving circuit **10** shown in FIG. **15** under the control of driving timing shown in FIG. **16** is as follows.

[0104] In a T**1** phase, i.e., in an initialization phase, a second gate driving signal at a previous stage output by an output terminal S**1** of the second gate driving unit at the previous stage is a logic low-level signal, and the second transistor M**2** is turned on; a second gate driving signal at a current stage output by an output terminal S**2** of the second gate driving unit at the current stage is a logic high-level signal, and a first transistor M**1** is turned off; a first gate driving signal at the current stage output by an output terminal E**2** of a first gate driving unit at the current stage is a logic high-level signal, a fourth transistor M**4** is turned on, and the sixth transistor M**6** is turned off; and a first gate driving signal at a subsequent stage output by an output terminal E**3** of a first gate driving unit at the subsequent stage is the logic low-level signal, the fifth transistor M**5** is turned on. The initialization voltage signal of an initialization signal terminal Vref is written into a first node N**1** through the turned-on second transistor M**2** and the turned-on fourth transistor M**4**. At the same time, the initialization voltage signal is written into the anode of the light-emitting component **20** through the turned-on second transistor M**2** and the turned-on fifth transistor M**5**.

[0105] In a T**2** phase, i.e., in a data writing phase, the second gate driving signal at the previous stage is the logic high-level signal, the second transistor M**2** is turned off; the second gate driving signal at the current stage is the logic low-level signal, the first transistor M**1** is turned on; and the first gate driving signal at the current stage is the logic high-level signal, the fourth transistor M**4** is turned on and the sixth transistor M**6** is turned off; and the first gate driving signal at the subsequent stage is the logic high-level signal, the fifth transistor M**5** is turned off. A data voltage signal of a data signal terminal Vdata is written into a control terminal of the driving transistor **110** (i.e., the first node N**1**) through the first transistor M**1**, the driving transistor **110**, and the fourth transistor M**4** sequentially. Reference may be made to the previous contents for the specific process, and at the same time, a voltage of the control terminal of the driving transistor **110** is stored in the capacitor C.

[0106] In a T**3** phase, the second gate driving signal at the previous stage is the logic high-level signal, the second transistor M**2** is turned off; the second gate driving signal at the current stage is the logic high-level signal, the first transistor M**1** is turned off; and the first gate driving signal at the current stage is the logic low-level signal, the fourth transistor M**4** is turned off and the sixth transistor M**6** is turned on; and the first gate driving signal at the subsequent stage is the logic high-level signal, the fifth transistor M**5** is turned off, and no action.

[0107] In a T**4** phase, i.e., in the light-emitting phase, the second gate driving signal at the previous stage is the logic high-level signal, the second transistor M**2** is turned off; the second gate driving signal at the current stage is the logic high-level signal, the first transistor M**1** is turned off; and the first gate driving signal at the current stage is the logic low-level signal, the fourth transistor M**4** is turned off and the sixth transistor M**6** is turned on; and the first gate driving signal at the subsequent stage is the logic low-level signal, the fifth transistor M**5** is turned on. A power signal of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on sixth transistor M**6**, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M**5** to drive the light-emitting component **20** to emit light.

[0108] It should be noted that FIGS. **10**, **15**, and **13** exemplarily show that the first transistor M**1**, the second transistor M**2**, the fifth transistor M**5**, the sixth transistor M**6**, and the driving transistor **110** are P-type transistors, and the fourth transistor M**4** is an N-type transistor. FIG. **13** also exemplarily shows that the third transistor M**3** is a P-type transistor, but this is not a limitation to the present disclosure. Generally, the P-type transistor is turned on under the control of the logic low-level signal and turned off under the control of the logic high-level signal. The N-type transistor is turned on under the control of the logic high-level signal, and turned off under the control of the logic low-level signal. In some optional embodiments, the transistors in the pixel driving circuit **10** may all be N-type transistors or P-type transistors, or some transistors in the pixel driving circuit **10** are N-type transistors and some transistors in the pixel driving circuit **10** are P-type transistors. The type of each transistor in the pixel driving circuit **10** is not specifically limited in the embodiment of the present disclosure.

[0109] FIG. **17** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure. FIG. **18** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **17**. Referring to FIGS. **17** and **18**, optionally, a pixel driving circuit **10** further includes a blocking module **180** which is electrically connected between a first power signal terminal PVDD and a first terminal of the driving transistor **110**, and is connected in series to a first light-emitting control unit **161**; a control terminal of the blocking module **180** is electrically connected to an output terminal of a gate driving circuit **30** (not shown in FIGS. **17** and **18**), and the blocking module **180** is used for blocking a first power voltage signal of the first power signal terminal PVDD from being transmitted to the first terminal of the driving transistor **110** in a data writing phase.

[0110] Specifically, at least in the data writing phase, the blocking module **180** is turned off under the control of the gate driving signal to block the first power voltage signal from being transmitted to the first terminal of the driving transistor **110**, thereby ensuring that a data voltage signal is successfully written into a first node N**1**; at least in the light-emitting phase, the blocking module **180** is turned on under the control of the gate driving signal, the first power voltage signal is written into the first terminal of the driving transistor **110** through the turned-on blocking module **180** and the first light-emitting control unit **161**, and enables the driving transistor **110** to generate a driving current.

[0111] Still referring to FIG. **18**, optionally, the blocking module **180** includes a seventh transistor M**7**, and a control terminal of the seventh transistor M**7** is electrically connected to an output terminal of the gate driving circuit **30**. It should be noted that FIG. **18** only exemplarily shows that a first terminal of the seventh transistor M**7** is electrically connected to the first power signal terminal PVDD, and a second terminal of the seventh transistor M**7** is electrically connected to a first terminal of the first light-emitting control unit **161**, but this is not a limitation to the present disclosure.

In other implementation modes, the first terminal of the seventh transistor M7 may also be electrically connected to a second terminal of the first light-emitting control unit **161**, and the second terminal of the seventh transistor M7 is electrically connected to the first terminal of the driving transistor **110**. It should be further noted that FIG. **18** only exemplarily shows that a second terminal of the first initialization module **150** is electrically connected to a second terminal of the driving transistor **110**, but this is not a limitation to the present disclosure. For example, in other embodiments, the second terminal of the first initialization module **150** may also be electrically connected to the second terminal of the driving transistor **110**.

[0112] FIG. **19** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure. Referring to FIGS. **3** and **19**, optionally, a display panel includes a first gate driving circuit **30**A and a second gate driving circuit **30**B. The first gate driving circuit **30**A includes multiple cascaded first gate driving units, the second gate driving circuit **30**B includes multiple cascaded second gate driving units. A control terminal of a data writing module **130** is electrically connected to an output terminal S**2** of the second gate driving unit at a current stage; a control terminal of a first light-emitting control unit **161** is electrically connected to an output terminal E**1** of the first gate driving unit at a previous stage; a control terminal of a blocking module **180** and a control terminal of a threshold compensation module **140** are electrically connected to an output terminal E**2** of the first gate driving unit at the current stage; a control terminal of a second light-emitting control unit **162** is electrically connected to the output terminal E**2** of the first gate driving unit at the current stage; and a control terminal of a first initialization module **150** is electrically connected between an initialization signal terminal Vref and a first node N**1**, and the control terminal of the first initialization module **150** is electrically connected to the output terminal E**1** of the first gate driving unit at the previous stage.

[0113] Optionally, multiple pixel driving circuits **10** are arranged in X rows and Y columns. The first gate driving circuit **30**A includes (X+1)-stage cascaded first gate driving units; and the second gate driving circuit **30**B includes X-stage cascaded second gate driving units. The first gate driving unit at the current stage of the pixel driving circuit **10** located in a j-th row is a first gate driving unit at a (j+1)-th stage, and the first gate driving unit at the previous stage is a first gate driving unit at a j-th stage, the second gate driving unit at the current stage is a second gate driving unit at a j-th stage, where X and Y are both positive integers greater than or equal to 1, and $1 \leq j \leq X$.

[0114] FIG. **20** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **19**. FIG. **21** is another driving timing graph provided by an embodiment of the present disclosure. A working process of the pixel driving circuit **20** shown in FIG. **10** under the control of the driving timing shown in FIG. **21** is as follows.

[0115] In a T**1** phase, i.e., a first sub-initialization phase in an initialization phase, a second gate driving signal at a current stage output by an output terminal S**2** of a second gate driving unit at the current stage is a logic high-level signal, and a first transistor M**1** is turned off; a first gate driving signal at a previous stage output by an output terminal E**1** of the first gate driving unit at the previous stage is a logic high-level signal, a second transistor M**2** is turned on and a sixth transistor M**6** is turned off; a first gate driving signal at the current stage output by an output terminal E**2** of the first gate driving unit at the current stage is a logic low-level signal, a seventh transistor M**7** is turned on, a fourth transistor M**4** is turned off, and a fifth transistor M**5** is turned on. An initialization voltage signal of the initialization signal terminal Vref is written into the first node N**1** through the turned-on second transistor M**2**.

[0116] In a T**2** phase, i.e., in a second sub-initialization phase in the initialization phase, the second gate driving signal at the current stage is the logic high-level signal, and the first transistor M**1** is turned off; the first gate driving signal at the previous stage is the logic high-level signal, the second transistor M**2** is turned on and the sixth transistor M**6** is turned off; the first gate driving signal at the current stage is the logic high-level signal, the seventh transistor M**7** is turned off, the fourth transistor M**4** is turned on, and the fifth transistor M**5** is turned off. An initialization voltage signal of the initialization signal terminal Vref is written into the first node N**1** through the turned-on second transistor M**2**.

[0117] In a T**3** phase, i.e., in a data writing phase, the second gate driving signal at the current stage is the logic low-level signal, and the first transistor M**1** is turned on; the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M**2** is turned off and the sixth transistor M**6** is turned on; the first gate driving signal at the current stage is the logic high-level signal, the seventh transistor M**7** is turned off, the fourth transistor M**4** is turned on, and the fifth transistor M**5** is turned off. A data voltage signal of a data signal terminal Vdata is written into a control terminal of the driving transistor **110** (i.e., the first node N**1**) through the first transistor M**1**, the driving transistor **110**, and the fourth transistor M**4** sequentially. Reference may be made to the previous contents for the specific process, and at the same time, a voltage of the control terminal of the driving transistor **110** is stored in the capacitor C.

[0118] In a T**4** phase, i.e., in a light-emitting phase, the second gate driving signal at the current stage is the logic high-level signal, the first transistor M**1** is turned off; the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M**2** is turned off and the sixth transistor M**6** is turned on; the first gate driving signal at the current stage is the logic low-level signal, the seventh transistor M**7** is turned on, the fourth transistor M**4** is turned off, and the fifth transistor M**5** is turned on. A power signal of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on seventh transistor M**7** and the turned-on sixth transistor M**6**, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M**5** to drive the light-emitting component **20** to emit light.

[0119] FIG. **22** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure. FIG. **23** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **22**. The difference between a pixel driving circuit **10** shown in FIG. **22** and a pixel driving circuit **10** shown FIG. **19** is that, optionally, the pixel driving circuit **10** further includes a second initialization module **170** which is electrically connected between an initialization signal terminal Vref and an anode of a light-emitting component **20**. A control terminal of a second initialization module **170** is electrically connected to an

output terminal S2 of a second gate driving unit at a current stage; the second initialization module **170** is used for providing an initialization voltage signal to the anode of the light-emitting component **20**. Referring to FIG. **23**, optionally, the second initialization module **170** includes a third transistor M3, a first terminal of the third transistor M3 is electrically connected to the initialization signal terminal Vref, a second terminal of the third transistor M3 is electrically connected to the anode of the light-emitting component **20**, and a control terminal of the third transistor M3 is electrically connected to the output terminal S2 of the second gate driving unit at the current stage.

[0120] A working process of the pixel driving circuit **23** shown in FIG. **10** under the control of driving timing shown in FIG. **21** is as follows.

[0121] In a T1 phase, i.e., a first sub-initialization phase in an initialization phase, a second gate driving signal at a current stage output by the output terminal S2 of the second gate driving unit at the current stage is a logic high-level signal, and a first transistor M1 is turned off and a third transistor M3 is turned off; a first gate driving signal at a previous stage output by an output terminal E1 of a first gate driving unit at the previous stage is a logic high-level signal, a second transistor M2 is turned on and a sixth transistor M6 is turned off; a first gate driving signal at the current stage output by an output terminal E2 of a first gate driving unit at the current stage is a logic low-level signal, a seventh transistor M7 is turned on, a fourth transistor M4 is turned off, and a fifth transistor M5 is turned on. The initialization voltage signal of the initialization signal terminal Vref is written into the first node N1 through the turned-on second transistor M2.

[0122] In a T2 phase, i.e., in a second sub-initialization phase in the initialization phase, the second gate driving signal at the current stage is the logic high-level signal, and the first transistor M1 is turned off and the third transistor M3 is turned off; the first gate driving signal at the previous stage is the logic high-level signal, the second transistor M2 is turned on and the sixth transistor M6 is turned off; the first gate driving signal at the current stage is the logic high-level signal, the seventh transistor M7 is turned off, the fourth transistor M4 is turned on, and the fifth transistor M5 is turned off. The initialization voltage signal of the initialization signal terminal Vref is written into the first node N1 through the turned-on second transistor M2.

[0123] In a T3 phase, i.e., in a data writing phase, the second gate driving signal at the current stage is the logic low-level signal, and the first transistor M1 is turned on and the third transistor M3 is turned on; the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic high-level signal, the seventh transistor M7 is turned off, the fourth transistor M4 is turned on, and the fifth transistor M5 is turned off. A data voltage signal of a data signal terminal Vdata is written into a control terminal of the driving transistor **110** (i.e., the first node N1) through the first transistor M1, the driving transistor **110**, and the fourth transistor M4 sequentially. Reference may be made to the previous contents for the specific process; a voltage of the control terminal of the driving transistor is stored in the capacitor C; and at the same time, the initialization voltage signal of the initialization signal terminal Vref is written into the anode of the light-emitting component **20** through the turned-on third transistor M3.

[0124] In a T4 phase, i.e., in a light-emitting phase, the second gate driving signal at the current stage is the logic high-level signal, and the first transistor M1 is turned off and the third transistor M3 is turned off; the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic low-level signal, the seventh transistor M7 is turned on, the fourth transistor M4 is turned off, and the fifth transistor M5 is turned on. A power signal of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on seventh transistor M7 and the turned-on sixth transistor M6, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M5 to drive the light-emitting component **20** to emit light.

[0125] FIG. **24** is a block diagram of a pixel driving circuit provided by an embodiment of the present disclosure. The difference between the pixel driving circuit **10** shown in FIG. **24** and the pixel driving circuit **10** shown in FIG. **19** is that, optionally, a control terminal of a second light-emitting control unit **162** is electrically connected to an output terminal E3 of a first gate driving unit at a subsequent stage. At this time, a first initialization module **150** is used for providing an initialization voltage signal for a control terminal of a driving transistor and an anode of a light-emitting component **20**.

[0126] Optionally, multiple pixel driving circuits **10** are arranged in X rows and Y columns. The first gate driving circuit **30**A includes (X+2)-stage cascaded first gate driving units; and the second gate driving circuit **30**B includes X-stage cascaded second gate driving units. A first gate driving unit at a previous stage of the pixel driving circuit **10** located in a j-th row is a first gating driving unit at a j-th stage, and a first gate driving unit at a current stage is a first gate driving unit at a (j+1)-th stage, the first gate driving unit at the subsequent stage is a first gate driving unit at a (j+2)-th stage, a second gate driving unit at the current stage is a second gate driving unit at a j-th stage, where X and Y are both positive integers greater than or equal to 1, and $1 \leq j \leq X$.

[0127] FIG. **25** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **24**. FIG. **26** is another driving timing graph provided by an embodiment of the present disclosure. A working process of the pixel driving circuit **25** shown in FIG. **10** under the control of the driving timing shown in FIG. **26** is as follows.

[0128] In a T1 phase, i.e., a first sub-initialization phase in an initialization phase, a second gate driving signal at a current stage output by an output terminal S2 of a second gate driving unit at the current stage is a logic high-level signal, and a first transistor M1 is turned off; a first gate driving signal at a previous stage output by an output terminal E1 of the first gate driving unit at the previous stage is a logic high-level signal, a second transistor M2 is turned on and a sixth transistor M6 is turned off; a first gate driving signal at the current stage output by an output terminal E2 of the first gate driving unit at the current stage is a logic low-level signal, a seventh transistor M7 is turned on, a fourth transistor M4 is turned off, and the first gate driving signal at the subsequent stage is the logic low-level signal, a fifth transistor M5 is turned on. The initialization voltage

signal of the initialization signal terminal Vref is written into the first node N1 through the turned-on second transistor M2.

[0129] In a T2 phase, i.e., in a second sub-initialization phase in the initialization phase, the second gate driving signal at the current stage is the logic high-level signal, and the first transistor M1 is turned off; the first gate driving signal at the previous stage is the logic high-level signal, the second transistor M2 is turned on and the sixth transistor M6 is turned off; the first gate driving signal at the current stage is the logic high-level signal, the seventh transistor M7 is turned off and the fourth transistor M4 is turned on; the first gate driving signal at the subsequent stage is the logic low-level signal, the fifth transistor M5 is turned on. The initialization voltage signal of the initialization signal terminal Vref is written into the first node N1 through the turned-on second transistor M2. At the same time, the initialization voltage signal is written into the anode of the light-emitting component **20** through the turned-on second transistor M2, the turned-on fourth transistor M4 and the turned-on fifth transistor M5.

[0130] In a T3 phase, i.e., in a data writing phase, the second gate driving signal at the current stage is the logic low-level signal, and the first transistor M1 is turned on; the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic high-level signal, the seventh transistor M7 is turned off, the fourth transistor M4 is turned on; and the first gate driving signal at the subsequent stage is the logic high-level signal, the fifth transistor M5 is turned off. A data voltage signal of a data signal terminal Vdata is written into a control terminal of the driving transistor **110** (i.e., the first node N1) through the first transistor M1, the driving transistor **110**, and the fourth transistor M4 sequentially. Reference may be made to the previous contents for the specific process, and a voltage of the control terminal of the driving transistor is stored in the capacitor C.

[0131] In a T4 phase, the second gate driving signal at the current stage is the logic high-level signal, the first transistor M1 is turned off; the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic low-level signal, the seventh transistor M7 is turned on and the fourth transistor M4 is turned off; the first gate driving signal at the subsequent stage is the logic high-level signal, the fifth transistor M5 is turned off and no action.

[0132] In a T5 phase, i.e., a light-emitting phase, the second gate driving signal at the current stage is the logic high-level signal, the first transistor M1 is turned off; the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic low-level signal, the seventh transistor M7 is turned on and the fourth transistor M4 is turned off; the first gate driving signal at the subsequent stage is the logic low-level signal, the fifth transistor M5 is turned on. A power signal of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on seventh transistor M7 and the turned-on sixth transistor M6, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M5 to drive the light-emitting component **20** to emit light.

[0133] It should be noted that FIGS. **20**, **23**, and **25** exemplarily show that the first transistor M1, the fifth transistor M5, the sixth transistor M6, the seventh transistor M7, and the driving transistor **110** are P-type transistors, and the second transistor M2 and the fourth transistor M4 are N-type transistors. FIG. **23** also exemplarily shows that the third transistor M3 is a P-type transistor, but this is not a limitation to the present disclosure. In some optional embodiments, the transistors in the pixel driving circuit **10** may all be N-type transistors, or P-type transistors, or some transistors in the pixel driving circuit **10** are N-type transistors and some transistors in the pixel driving circuit **10** are P-type transistors. The type of each transistor in the pixel driving circuit **10** is not specifically limited in the embodiment of the present disclosure.

[0134] FIG. **27** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure. Referring to FIGS. **3** and **27**, a display panel includes a first gate driving circuit **30**A and a second gate driving circuit **30**B. The first gate driving circuit **30**A includes multiple cascaded first gate driving units, and the second gate driving circuit **30**B includes multiple cascaded second gate driving units. A control terminal of a data writing module **130** is electrically connected to an output terminal S2 of the second gate driving unit at a current stage; a control terminal of a first light-emitting control unit **161** is electrically connected to an output terminal E1 of the first gate driving unit at a previous stage; a control terminal of a blocking module **180** and a control terminal of a threshold compensation module **140** are electrically connected to an output terminal E2 of the first gate driving unit at the current stage; a control terminal of a second light-emitting control unit **162** is electrically connected to the output terminal E2 of the first gate driving unit at the current stage or an output terminal E3 of the first gate driving unit at a subsequent stage; and a first initialization module **150** is electrically connected between an initialization signal terminal Vref and a second terminal of a driving transistor **110**, a control terminal of the first initialization module **150** is electrically connected to the output terminal E1 of the first gate driving unit at the previous stage, and the first initialization module **150** is used for providing an initialization voltage signal to a control terminal of the driving transistor and an anode of a light-emitting component **20**.

[0135] Optionally, multiple pixel driving circuits **10** are arranged in X rows and Y columns. When the control terminal of the second light-emitting control unit **162** is electrically connected to the output terminal E2 of the first gate driving unit at the current stage, the first gate driving circuit **30**A includes (X+1)-stage cascaded first gate driving units. When the control terminal of the second light-emitting control unit **162** is electrically connected to the output terminal E3 of the first gate driving unit at the subsequent stage, the first gate driving circuit **30**A includes (X+2)-stage cascaded first gate driving units and the second gate driving circuit **30**B includes X-stage cascaded second gate driving units. The first gate driving unit at the previous stage of the pixel driving circuit **10** located in a j-th row is a first gating driving unit at a j-th stage, and a first gate driving unit at the current stage is a first gate driving unit at a (j+1)-th stage, the first gate driving unit at the subsequent stage is a first gate

driving unit at a (j+2)-th stage, the second gate driving unit at the current stage is a second gate driving unit at a j-th stage, where X and Y are both positive integers greater than or equal to 1, and 1≤j≤X.

[0136] FIG. **28** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **27**. A working process of the pixel driving circuit **28** shown in FIG. **10** under the control of the driving timing shown in FIG. **21** is as follows.

[0137] In a T**1** phase, i.e., a first sub-initialization phase in an initialization phase, a second gate driving signal at the current stage output by an output terminal S**2** of the second gate driving unit at the current stage is a logic high-level signal, and a first transistor M**1** is turned off; a first gate driving signal at the previous stage output by an output terminal E**1** of the first gate driving unit at the previous stage is a logic high-level signal, a second transistor M**2** is turned on and a sixth transistor M**6** is turned off; and a first gate driving signal at the current stage output by an output terminal E**2** of the first gate driving unit at the current stage is a logic low-level signal, a seventh transistor M**7** is turned on, a fourth transistor M**4** is turned off, and a fifth transistor M**5** is turned on. The initialization voltage signal of the initialization signal terminal Vref is written into the anode of the light-emitting component **20** through the turned-on second transistor M**2** and the turned-on fifth transistor M**5**.

[0138] In a T**2** phase, i.e., in a second sub-initialization phase in the initialization phase, the second gate driving signal at the current stage is the logic high-level signal, and the first transistor M**1** is turned off; the first gate driving signal at the previous stage is the logic high-level signal, the second transistor M**2** is turned on and the sixth transistor M**6** is turned off; and the first gate driving signal at the current stage is the logic high-level signal, the seventh transistor M**7** is turned off, the fourth transistor M**4** is turned on, and the fifth transistor M**5** is turned off. The initialization voltage signal of the initialization signal terminal Vref is written into a first node N**1** through the turned-on second transistor M**2** and the turned-on fourth transistor M**4**.

[0139] In a T**3** phase, i.e., in a data writing phase, the second gate driving signal at the current stage is the logic low-level signal, and the first transistor M**1** is turned on; the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M**2** is turned off and the sixth transistor M**6** is turned on; and the first gate driving signal at the current stage is the logic high-level signal, the seventh transistor M**7** is turned off, the fourth transistor M**4** is turned on, and the fifth transistor M**5** is turned off. A data voltage signal of a data signal terminal Vdata is written into a control terminal of the driving transistor **110** (i.e., the first node N**1**) through the first transistor M**1**, the driving transistor **110**, and the fourth transistor M**4** sequentially. Reference may be made to the previous contents for the specific process, and at the same time, a voltage of the control terminal of the driving transistor **110** is stored in the capacitor C.

[0140] In a T**4** phase, i.e., in a light-emitting phase, the second gate driving signal at the current stage is the logic high-level signal, the first transistor M**1** is turned off; the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M**2** is turned off and the sixth transistor M**6** is turned on; and the first gate driving signal at the current stage is the logic low-level signal, the seventh transistor M**7** is turned on, the fourth transistor M**4** is turned off, and the fifth transistor M**5** is turned on. A power signal of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on seventh transistor M**7** and the turned-on sixth transistor M**6**, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M**5** to drive the light-emitting component **20** to emit light.

[0141] FIG. **29** is another schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **27**. A working process of the pixel driving circuit **29** shown in FIG. **10** under the control of the driving timing shown in FIG. **26** is as follows.

[0142] In a T**1** phase, i.e., a first sub-initialization phase in an initialization phase, a second gate driving signal at the current stage output by an output terminal S**2** of the second gate driving unit at the current stage is a logic high-level signal, and a first transistor M**1** is turned off; a first gate driving signal at a previous stage output by an output terminal E**1** of the first gate driving unit at the previous stage is a logic high-level signal, a second transistor M**2** is turned on and a sixth transistor M**6** is turned off; a first gate driving signal at the current stage output by an output terminal E**2** of the first gate driving unit at the current stage is a logic low-level signal, a seventh transistor M**7** is turned on, a fourth transistor M**4** is turned off, and a first gate driving signal at the subsequent stage is the logic low-level signal, a fifth transistor M**5** is turned on. The initialization voltage signal of the initialization signal terminal Vref is written into the anode of the light-emitting component **20** through the turned-on second transistor M**2** and the turned-on fifth transistor M**5**.

[0143] In a T**2** phase, i.e., in a second sub-initialization phase in the initialization phase, the second gate driving signal at the current stage is the logic high-level signal, and the first transistor M**1** is turned off; the first gate driving signal at the previous stage is the logic high-level signal, the second transistor M**2** is turned on and the sixth transistor M**6** is turned off; the first gate driving signal at the current stage is the logic high-level signal, the seventh transistor M**7** is turned off and the fourth transistor M**4** is turned on; the first gate driving signal at the subsequent stage is the logic low-level signal, the fifth transistor M**5** is turned on. The initialization voltage signal of an initialization signal terminal Vref is written into a first node N**1** through the turned-on second transistor M**2** and the turned-on fourth transistor M**4**. At the same time, the initialization voltage signal is written into the anode of the light-emitting component **20** through the turned-on second transistor M**2** and the turned-on fifth transistor M**5**.

[0144] In a T**3** phase, i.e., in a data writing phase, the second gate driving signal at the current stage is the logic low-level signal, and the first transistor M**1** is turned on; the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M**2** is turned off and the sixth transistor M**6** is turned on; the first gate driving signal at the current stage is the logic high-level signal, the seventh transistor M**7** is turned off, the fourth transistor M**4** is turned on; and the first gate driving signal at the subsequent stage is the logic high-level signal, the fifth transistor M**5** is turned off. A data voltage signal of a data signal terminal Vdata is written into a control terminal of the driving transistor **110** (i.e., the first node N**1**) through the first transistor M**1**, the driving transistor **110**, and the fourth

transistor M4 sequentially. Reference may be made to the previous contents for the specific process, and a voltage of the control terminal of the driving transistor is stored in the capacitor C.

[0145] In a T4 phase, the second gate driving signal at the current stage is the logic high-level signal, the first transistor M1 is turned off; the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic low-level signal, the seventh transistor M7 is turned on and the fourth transistor M4 is turned off; the first gate driving signal at the subsequent stage is the logic high-level signal, the fifth transistor M5 is turned off and no action.

[0146] In a T5 phase, i.e., a light-emitting phase, the second gate driving signal at the current stage is the logic high-level signal, the first transistor M1 is turned off; the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic low-level signal, the seventh transistor M7 is turned on and the fourth transistor M4 is turned off; the first gate driving signal at the subsequent stage is the logic low-level signal, the fifth transistor M5 is turned on. A power signal of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on seventh transistor M7 and the turned-on sixth transistor M6, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M5 to drive the light-emitting component **20** to emit light.

[0147] It should be noted that FIGS. **28** and **29** exemplarily show that the first transistor M1, the fifth transistor M5, the sixth transistor M6, the seventh transistor M7, and the driving transistor **110** are P-type transistors, and the second transistor M2 and the fourth transistor M4 are N-type transistors, but this is not a limitation to the present disclosure. In some optional embodiments, the transistors in the pixel driving circuit **10** may all be N-type transistors or P-type transistors, or some transistors in the pixel driving circuit **10** are N-type transistors and some transistors in the pixel driving circuit **10** are P-type transistors. The type of each transistor in the pixel driving circuit **10** is not specifically limited in the embodiment of the present disclosure.

[0148] FIG. **30** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure. FIG. **31** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure. Referring to FIGS. **30** and **31**, a display panel includes a first gate driving circuit, and the first gate driving circuit includes multiple cascaded first gate driving units. A control terminal of a first light-emitting control unit **161** is electrically connected to an output terminal E1 of the first gate driving unit at the previous stage; a control terminal of a blocking module **180** and a control terminal of a data writing module **130** are electrically connected to an output terminal E2 of the first gate driving unit at the current stage (as shown in FIG. **30**) or an output terminal E3 of the first gate driving unit at the subsequent stage (as shown in FIG. **31**); a control terminal of the threshold compensation module **140** and a control terminal of the second light-emitting control unit **162** are electrically connected to the output terminal E2 of the first gate driving unit at the current stage; and the first initialization module **150** is electrically connected between the initialization signal terminal Vref and the control terminal of the driving transistor, and a control terminal of the first initialization module **150** is electrically connected to the output terminal E1 of the first gate driving unit at the previous stage.

[0149] Optionally, multiple pixel driving circuits **10** are arranged in X rows and Y columns. When the control terminal of the blocking module **180** and the control terminal of the data writing module **130** are electrically connected to the output terminal E2 of the first gate driving unit at the current stage, the first gate driving circuit includes (X+1)-stage cascaded first gate driving units. When the control terminal of the blocking module **180** and the control terminal of the data writing module **130** are electrically connected to the output terminal E3 of the first gate driving unit at the subsequent stage, the first gate driving circuit includes (X+2)-stage cascaded first gate driving units. The first gate driving unit at the previous stage of the pixel driving circuit **10** located in a j-th row is a first gate driving unit at a j-th stage, and the first gate driving unit at the current stage is a first gate driving unit at a (j+1)-th stage, the first gate driving unit at the subsequent stage is a first gate driving unit at a (j+2)-th stage, where X and Y are both positive integers greater than or equal to 1, and $1 \leq j \leq X$.

[0150] FIG. **32** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **30**. FIG. **33** is a driving timing graph provided by an embodiment of the present disclosure. A working process of the pixel driving circuit shown in FIG. **32** under the control of the driving timing shown in FIG. **33** is as follows.

[0151] In a T1 phase, i.e., in an initialization phase, a first gate driving signal at the previous stage output by the first gate driving unit at the previous stage is a logic high-level signal, and a second transistor M2 is turned on and a sixth transistor M6 is turned off; the first gate driving signal at the current stage is a logic high-level signal, a seventh transistor M7 is turned on and a fourth transistor M4 is turned off, a first transistor M1 is turned off and a fifth transistor M5 is turned on. The initialization voltage signal of the initialization signal terminal Vref is written into a first node N1 through the turned-on second transistor M2.

[0152] In a T2 phase, i.e., in a data writing phase, the first gate driving signal at the previous stage is the logic low-level signal, and the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal output by the first gate driving unit at the current stage is the logic high-level signal, the seventh transistor M7 is turned off and the fourth transistor M4 is turned on, the first transistor M1 is turned on and the fifth transistor M5 is turned off. A data voltage signal of a data signal terminal Vdata is written into a control terminal of the driving transistor **110** (i.e., the first node N1) through the first transistor M1, the driving transistor **110**, and the fourth transistor M4 sequentially. Reference may be made to the previous contents for the specific process, and at the same time, a voltage of the control terminal of the driving transistor **110** is stored in the capacitor C.

[0153] In a T3 phase, i.e., in a light-emitting phase, the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M2 is turned off, and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic low-level signal, the seventh transistor M7 is turned on, the fourth transistor M4

is turned off, the first transistor M1 is turned off, and the fifth transistor M5 is turned on. A first power voltage signal of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on seventh transistor M7 and the turned-on sixth transistor M6, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M5 to drive the light-emitting component **20** to emit light.

[0154] FIG. **34** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **31**. FIG. **35** is another driving timing graph provided by an embodiment of the present disclosure. A working process of the pixel driving circuit **10** shown in FIG. **34** under the control of the driving timing shown in FIG. **35** is as follows.

[0155] In a T1 phase, i.e., a first sub-initialization phase in an initialization phase, the first gate driving signal at the previous stage output by the first gate driving unit at the previous stage is a logic high-level signal, and the second transistor M2 is turned on and the sixth transistor M6 is turned off; the first gate driving signal at the current stage output by the first gate driving unit at the current stage is the logic low-level signal, the fourth transistor M4 is turned off and the fifth transistor M5 is turned on, the first gate driving signal at the subsequent stage output by the first gate driving unit at the subsequent stage is the logic low-level signal, the first transistor M1 is turned off and the seventh transistor M7 is turned on. The initialization voltage signal of the initialization signal terminal Vref is written into the first node N1 through the turned-on second transistor M2.

[0156] In a T2 phase, i.e., in a second sub-initialization phase in the initialization phase, the first gate driving signal at the previous stage is the logic high-level signal, and the second transistor M2 is turned on and the sixth transistor M6 is turned off; the first gate driving signal at the current stage is the logic high-level signal, the fourth transistor M4 is turned on and the fifth transistor M5 is turned off, the first gate driving signal at the subsequent stage is the logic low-level signal, the first transistor M1 is turned off and the seventh transistor M7 is turned on. The initialization voltage signal of the initialization signal terminal Vref is written into the first node N1 through the turned-on second transistor M2.

[0157] In a T3 phase, i.e., in a data writing phase, the first gate driving signal at the previous stage is the logic low-level signal, and the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic high-level signal, the fourth transistor M4 is turned on and the fifth transistor M5 is turned off, the first gate driving signal at the subsequent stage is the logic high-level signal, the first transistor M1 is turned on and the seventh transistor M7 is turned off. The data voltage signal of the data signal terminal Vdata is written into a control terminal of the driving transistor **110** (i.e., the first node N1) through the first transistor M1, the driving transistor **110**, and the fourth transistor M4 sequentially. Reference may be made to the previous contents for the specific process, and at the same time, a voltage of the control terminal of the driving transistor **110** is stored in the capacitor C.

[0158] In a T4 phase, the first gate driving signal at the previous stage is the logic low-level signal, and the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic low-level signal, the fourth transistor M4 is turned off and the fifth transistor M5 is turned on, the first gate driving signal at the subsequent stage is the logic high-level signal, the first transistor M1 is turned on, the seventh transistor M7 is turned off and no action.

[0159] In a T5 phase, i.e., in the light-emitting phase, the first gate driving signal at the previous stage is the logic low-level signal, and the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic low-level signal, the fourth transistor M4 is turned off and the fifth transistor M5 is turned on, the first gate driving signal at the subsequent stage is the logic low-level signal, the first transistor M1 is turned off, the seventh transistor M7 is turned on. A first power voltage signal of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on seventh transistor M7 and the turned-on sixth transistor M6, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M5 to drive the light-emitting component **20** to emit light.

[0160] It should be noted that FIGS. **32** and **34** exemplarily show that the fifth transistor M5, the sixth transistor M6, the seventh transistor M7, and the driving transistor **110** are P-type transistors, the first transistor M1, the second transistor M2 and the fourth transistor M4 are N-type transistors, but this is not a limitation to the present disclosure. In some optional embodiments, the transistors in the pixel driving circuit **10** may all be N-type transistors or P-type transistors, or some transistors in the pixel driving circuit **10** are N-type transistors and some transistors in the pixel driving circuit **10** are P-type transistors. The type of each transistor in the pixel driving circuit **10** is not specifically limited in the embodiment of the present disclosure.

[0161] FIG. **36** is a block diagram of a pixel driving circuit provided by an embodiment of the present disclosure. FIG. **37** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure. Referring to FIGS. **30**, **31**, **36**, and **37**, a difference between the pixel driving circuit **10** shown in FIG. **36** and the pixel driving circuit **10** shown in FIG. **30**, and the difference between the pixel driving circuit **10** shown in FIG. **37** and pixel driving circuit **10** shown FIG. **31** is that, optionally, the display panel also includes a second gate driving circuit. The second gate driving circuit includes multiple cascaded second gate driving units. The pixel driving circuit **10** also includes a second initialization module **170** which is electrically connected between an initialization signal terminal Vref and an anode of a light-emitting component **20**, a control terminal of the second initialization module **170** is electrically connected to an output terminal S2 of the second gate driving unit at a current stage; and the second initialization module **170** is used for providing an initialization voltage signal to the anode of the light-emitting component **20**.

[0162] Optionally, the second gate driving circuit includes X-stage cascaded second gate driving units. The second gate driving unit at the current stage of the pixel driving circuit **10** located in a j-th row is a second gate driving unit in a j-th stage, where X and Y are both positive integers greater than or equal to 1, and $1 \leq j \leq X$.

[0163] FIG. **38** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **36**. FIG. **39** is another driving timing graph provided by an embodi-

ment of the present disclosure. A working process of the pixel driving circuit **10** shown in FIG. **38** under the control of the driving timing shown in FIG. **39** is as follows.

[0164] In a T**1** phase, i.e., in an initialization phase, a first gate driving signal at the previous stage output by the first gate driving unit at the previous stage is a logic high-level signal, and a second transistor M**2** is turned on and a sixth transistor M**6** is turned off; the first gate driving signal at the current stage is the logic high-level signal, a seventh transistor M**7** is turned on and a fourth transistor M**4** is turned off, a first transistor M**1** is turned off and a fifth transistor M**5** is turned on; and a second gate driving signal at the current stage output by the second gate driving unit at the current stage is the logic high-level signal, a third transistor M**3** is turned off. The initialization voltage signal of the initialization signal terminal Vref is written into the first node N**1** through the turned-on second transistor M**2**.

[0165] In a T**2** phase, i.e., in a data writing phase, the first gate driving signal at the previous stage is the logic low-level signal, and the second transistor M**2** is turned off and the sixth transistor M**6** is turned on; the first gate driving signal output by the first gate driving unit at the current stage is the logic high-level signal, the seventh transistor M**7** is turned off and the fourth transistor M**4** is turned on, the first transistor M**1** is turned on and the fifth transistor M**5** is turned off; and the second gate driving signal at the current stage is the logic low-level signal, the third transistor M**3** is turned on. A data voltage signal of a data signal terminal Vdata is written into a control terminal of the driving transistor **110** (i.e., the first node N**1**) through the first transistor M**1**, the driving transistor **110**, and the fourth transistor M**4** sequentially. Reference may be made to the previous contents for the specific process; a voltage of the control terminal of the driving transistor is stored in the capacitor C; and at the same time, the initialization voltage signal is written into the anode of the light-emitting component **20** through the turned-on third transistor M**3**.

[0166] In a T**3** phase, i.e., in a light-emitting phase, the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M**2** is turned off, and the sixth transistor M**6** is turned on; the first gate driving signal at the current stage is the logic low-level signal, the seventh transistor M**7** is turned on, the fourth transistor M**4** is turned off, the first transistor M**1** is turned off, and the fifth transistor M**5** is turned on; and the second gate driving signal at the current stage is the logic high-level signal, the third transistor M**3** is turned off. A first power voltage signal of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on seventh transistor M**7** and the turned-on sixth transistor M**6**, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M**5** to drive the light-emitting component **20** to emit light.

[0167] FIG. **40** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **37**. A working process of the pixel driving circuit **10** shown in FIG. **40** under the control of the driving timing shown in FIG. **26** is as follows.

[0168] In a T**1** phase, i.e., a first sub-initialization phase in an initialization phase, the first gate driving signal at the previous stage output by the first gate driving unit at the previous stage is a logic high-level signal, and the second transistor M**2** is turned on and the sixth transistor M**6** is turned off; the first gate driving signal at the current stage output by the first gate driving unit at the current stage is the logic low-level signal, the fourth transistor M**4** is turned off and the fifth transistor M**5** is turned on, the first gate driving signal at the subsequent stage output by the first gate driving unit at the subsequent stage is the logic low-level signal, the first transistor M**1** is turned off and the seventh transistor M**7** is turned on; and the second gate driving signal at the current stage is the logic high-level signal, the third transistor M**3** is turned off. The initialization voltage signal of the initialization signal terminal Vref is written into the first node N**1** through the turned-on second transistor M**2**.

[0169] In a T**2** phase, i.e., in a second sub-initialization phase in the initialization phase, the first gate driving signal at the previous stage is the logic high-level signal, and the second transistor M**2** is turned on and the sixth transistor M**6** is turned off; the first gate driving signal at the current stage is the logic high-level signal, the fourth transistor M**4** is turned on and the fifth transistor M**5** is turned off, the first gate driving signal at the subsequent stage is the logic low-level signal, the first transistor M**1** is turned off and the seventh transistor M**7** is turned on; and the second gate driving signal at the current stage is the logic high-level signal, the third transistor M**3** is turned off. The initialization voltage signal of the initialization signal terminal Vref is written into the first node N**1** through the turned-on second transistor M**2**.

[0170] In a T**3** phase, i.e., in a data writing phase, the first gate driving signal at the previous stage is the logic low-level signal, and the second transistor M**2** is turned off and the sixth transistor M**6** is turned on; the first gate driving signal at the current stage is the logic high-level signal, the fourth transistor M**4** is turned on and the fifth transistor M**5** is turned off, the first gate driving signal at the subsequent stage is the logic high-level signal, the first transistor M**1** is turned on and the seventh transistor M**7** is turned off; and the second gate driving signal at the current stage is the logic low-level signal, the third transistor M**3** is turned off. A data voltage signal of a data signal terminal Vdata is written into a control terminal of the driving transistor **110** (i.e., the first node N**1**) through the first transistor M**1**, the driving transistor **110**, and the fourth transistor M**4** sequentially. Reference may be made to the previous contents for the specific process; a voltage of the control terminal of the driving transistor is stored in the capacitor C; and at the same time, the initialization voltage signal is written into the anode of the light-emitting component **20** through the turned-on third transistor M**3**.

[0171] In a T**4** phase, the first gate driving signal at the previous stage is the logic low-level signal, and the second transistor M**2** is turned off and the sixth transistor M**6** is turned on; the first gate driving signal at the current stage is the logic low-level signal, the fourth transistor M**4** is turned off and the fifth transistor M**5** is turned on, the first gate driving signal at the subsequent stage is the logic high-level signal, the first transistor M**1** is turned on, the seventh transistor M**7** is turned off; and the second gate driving signal at the current stage is the logic high-level signal, the third transistor M**3** is turned off and no action.

[0172] In a T**5** phase, i.e., in the light-emitting phase, the first gate driving signal at the previous stage is the logic low-level signal, and the second transistor M**2** is turned off and the sixth transistor M**6** is turned on; the first gate driving signal at the current stage is the logic low-level signal, the

fourth transistor M4 is turned off and the fifth transistor M5 is turned on, the first gate driving signal at the subsequent stage is the logic low-level signal, the first transistor M1 is turned off, the seventh transistor M7 is turned on; and the second gate driving signal at the current stage is the logic high-level signal, the third transistor M3 is turned off. A first power voltage signal of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on seventh transistor M7 and the turned-on sixth transistor M6, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M5 to drive the light-emitting component **20** to emit light.

[0173] It should be noted that, in the driving timing sequence shown in FIG. **26**, initialization of the anode of the light-emitting component **20** occurs at the T3 phase, but this is not a limitation to the present disclosure. In other embodiments, the initialization of the anode of the light-emitting component **20** may also occur at T1 phase and/or T2 phase.

[0174] It should be noted that FIGS. **38** and **40** exemplarily show that the third transistor M3, the fifth transistor M5, the sixth transistor M6, the seventh transistor M7 and the driving transistor **110** are P-type transistors, and the first transistor M1, the second transistor M2, the fourth transistor M4 are N-type transistors, but this is not a limitation to the present disclosure. In some optional embodiments, the transistors in the pixel driving circuit **10** may all be N-type transistors, or P-type transistors, or some transistors in the pixel driving circuit **10** are N-type transistors and some transistors in the pixel driving circuit **10** are P-type transistors. The type of each transistor in the pixel driving circuit **10** is not specifically limited in the embodiment of the present disclosure.

[0175] FIG. **41** is a block diagram of a pixel driving circuit provided by an embodiment of the present disclosure. FIG. **42** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure. Referring to FIGS. **30**, **31**, **41**, and **42**, a difference between a pixel driving circuit **10** shown in FIG. **41** and a pixel driving circuit **10** shown FIG. **30** and a difference between a pixel driving circuit **10** shown in FIG. **42** and a pixel driving circuit **10** shown FIG. **31** are that, optionally, the pixel driving circuit **10** further includes a second initialization module **170** which is electrically connected between an initialization signal terminal Vref and an anode of a light-emitting component **20**. A control terminal of a second initialization module **170** is electrically connected to an output terminal E2 of a first gate driving unit at a current stage, and the second initialization module **170** is used for providing an initialization voltage signal to the anode of the light-emitting component **20**.

[0176] FIG. **43** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **41**. A working process of the pixel driving circuit **10** shown in FIG. **43** under the control of the driving timing shown in FIG. **33** is as follows.

[0177] In a T1 phase, i.e., in an initialization phase, a first gate driving signal at the previous stage output by the first gate driving unit at the previous stage is a logic high-level signal, and a second transistor M2 is turned on and a sixth transistor M6 is turned off; the first gate driving signal at the current stage is a logic high-level signal, a seventh transistor M7 is turned on and a fourth transistor M4 is turned off, a first transistor M1 is turned off, a fifth transistor M5 is turned on and a third transistor M3 is turned off. The initialization voltage signal of the initialization signal terminal Vref is written into the first node N1 through the turned-on second transistor M2.

[0178] In a T2 phase, i.e., in a data writing phase, the first gate driving signal at the previous stage is the logic low-level signal, and the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal output by the first gate driving unit at the current stage is the logic high-level signal, the seventh transistor M7 is turned off and the fourth transistor M4 is turned on, the first transistor M1 is turned on, the fifth transistor M5 is turned off and the third transistor M3 is turned on. A data voltage signal of a data signal terminal Vdata is written into a control terminal of the driving transistor **110** (i.e., the first node N1) through the first transistor M1, the driving transistor **110**, and the fourth transistor M4 sequentially. Reference may be made to the previous contents for the specific process; a voltage of the control terminal of the driving transistor is stored in the capacitor C; and at the same time, the initialization voltage signal of the initialization signal terminal Vref is written into the anode of the light-emitting component **20** through the turned-on third transistor M3.

[0179] In a T3 phase, i.e., in a light-emitting phase, the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M2 is turned off, and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic low-level signal, the seventh transistor M7 is turned on, the fourth transistor M4 is turned off, the first transistor M1 is turned off, the fifth transistor M5 is turned on and the third transistor M3 is turned off. A first power voltage signal of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on seventh transistor M7 and the turned-on sixth transistor M6, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M5 to drive the light-emitting component **20** to emit light.

[0180] FIG. **44** is a schematic diagram showing circuit components of a pixel driving circuit shown in FIG. **42**. A working process of the pixel driving circuit **10** shown in FIG. **44** under the control of the driving timing shown in FIG. **35** is as follows.

[0181] In a T1 phase, i.e., a first sub-initialization phase in an initialization phase, the first gate driving signal at the previous stage output by the first gate driving unit at the previous stage is a logic high-level signal, and the second transistor M2 is turned on and the sixth transistor M6 is turned off; the first gate driving signal at the current stage output by the first gate driving unit at the current stage is the logic low-level signal, the fourth transistor M4 is turned off, the fifth transistor M5 is turned on and the third transistor M3 is turned off; and the first gate driving signal at the subsequent stage output by the first gate driving unit at the subsequent stage is the logic low-level signal, the first transistor M1 is turned off and the seventh transistor M7 is turned on. The initialization voltage signal of the initialization signal terminal Vref is written into the first node N1 through the turned-on second transistor M2.

[0182] In a T2 phase, i.e., in a second sub-initialization phase in the initialization phase, the first gate driving signal at the previous stage is the logic high-level signal, and the second transistor M2 is turned on and the sixth transistor M6

is turned off; the first gate driving signal at the current stage is the logic high-level signal, the fourth transistor M4 is turned on, the fifth transistor M5 is turned off, and the third transistor M3 is turned on; and the first gate driving signal at the subsequent stage is the logic low-level signal, the first transistor M1 is turned off and the seventh transistor M7 is turned on. The initialization voltage signal of the initialization signal terminal Vref is written into the first node N1 through the turned-on second transistor M2. At the same time, the initialization voltage signal is written into the anode of the light-emitting component **20** through the turned-on third transistor M3.

[0183] In a T3 phase, i.e., in a data writing phase, the first gate driving signal at the previous stage is the logic low-level signal, and the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic high-level signal, the fourth transistor M4 is turned on, the fifth transistor M5 is turned off and the third transistor M3 is turned on; and the first gate driving signal at the subsequent stage is the logic high-level signal, the first transistor M1 is turned on and the seventh transistor M7 is turned off. A data voltage signal of a data signal terminal Vdata is written into a control terminal of the driving transistor **110** (i.e., the first node N1) through the first transistor M1, the driving transistor **110**, and the fourth transistor M4 sequentially. Reference may be made to the previous contents for the specific process; a voltage of the control terminal of the driving transistor is stored in the capacitor C; and at the same time, the initialization voltage signal is written into the anode of the light-emitting component **20** through the turned-on third transistor M3.

[0184] In a T4 phase, the first gate driving signal at the previous stage is the logic low-level signal, the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic low-level signal, the fourth transistor M4 is turned off, the fifth transistor M5 is turned on and the third transistor M3 is turned off, the first gate driving signal at the subsequent stage is the logic high-level signal, the first transistor M1 is turned on, the seventh transistor M7 is turned off and no action.

[0185] In a T5 phase, i.e., in the light-emitting phase, the first gate driving signal at the previous stage is the logic low-level signal, and the second transistor M2 is turned off and the sixth transistor M6 is turned on; the first gate driving signal at the current stage is the logic low-level signal, the fourth transistor M4 is turned off, the fifth transistor M5 is turned on and the third transistor M3 is turned off; and the first gate driving signal at the subsequent stage is the logic low-level signal, the first transistor M1 is turned off and the seventh transistor M7 is turned on. A first power voltage signal of a first power signal terminal PVDD is written into a first terminal of the driving transistor **110** through the turned-on seventh transistor M7 and the turned-on sixth transistor M6, the driving transistor **110** generates a driving current, and the driving current flows into the light-emitting component **20** through the fifth transistor M5 to drive the light-emitting component **20** to emit light.

[0186] It should be noted that FIGS. **43** and **44** exemplarily show that the fifth transistor M5, the sixth transistor M6, the seventh transistor M7, and the driving transistor **110** are P-type transistors, and the first transistor M1, the second transistor M2, the fourth transistor M4, and the third transistor M3 are N-type transistors, but this is not a limitation to the present disclosure. Generally, the P-type transistor is turned on under the control of the logic low-level signal and turned off under the control of the logic high-level signal. The N-type transistor is turned on under the control of the logic high-level signal, and turned off under the control of the logic low-level signal. In some optional embodiments, the transistors in the pixel driving circuit **10** may all be N-type transistors or P-type transistors, or some transistors in the pixel driving circuit **10** are N-type transistors and some transistors in the pixel driving circuit **10** are P-type transistors. The type of each transistor in the pixel driving circuit **10** is not specifically limited in the embodiment of the present disclosure.

[0187] Based on the above technical solution, optionally, a transistor in the threshold compensation module **140** is a semiconductor oxide transistor. Exemplarily, a transistor in the threshold compensation module **140** may be an indium gallium zinc oxide transistor. It can be understood that the relatively small leakage current of the semiconductor oxide transistor is beneficial to stabilizing the voltage of the first node N1, thereby stabilizing the driving current generated by the driving transistor **110** and improving the uniformity of the luminous luminance of the light-emitting component **20**.

[0188] Optionally, when a second terminal of the first initialization module **150** is electrically connected to the first node N1, a transistor in the first initialization module **150** is a semiconductor oxide transistor. Exemplarily, a transistor in the first initialization module **150** may be an indium gallium zinc oxide transistor. In this way, it is beneficial to stabilize the voltage of the first node N1, thereby stabilizing the driving current generated by the driving transistor **110**, and is beneficial to improving the uniformity of the luminous luminance of the light-emitting component **20**.

[0189] Based on the above inventive concept, the embodiments of the present disclosure further provide a driving method of a display panel. The driving method is applicable to the display panel described in any embodiment of the present disclosure, and a gate driving circuit is used for outputting a gate driving signal. FIG. **45** is a flowchart of a driving method of a display panel according to an embodiment of the present disclosure. Referring to FIG. **45**, the method includes steps described below.

[0190] In S**110**, in a data writing phase, a data writing module is turned on under the control of the gate driving signal and a data voltage signal is written into a control terminal of a driving transistor; at the same time, a threshold compensation module is turned on under the control of the gate driving signal, and a threshold voltage deviation of the driving transistor is detected and self-compensated.

[0191] In S**120**, in a light-emitting phase, a light-emitting control module is turned on under the control of the gate driving signal, and a driving current generated by the driving transistor is controlled to flow into a light-emitting component to drive the light-emitting component to emit light.

[0192] The threshold compensation module and the light-emitting control module are controlled by the gate driving signal output by a same gate driving circuit, and the threshold compensation module is turned on in response to the gate driving signal being at a first level, and the light-emitting control module is turned on in response to the gate driving signal being at a second level; the first level and the second level are different.

[0193] Optionally, the display panel further includes a first initialization module, a control terminal of the first initialization module is electrically connected to the gate driving circuit. The first initialization module is configured for providing an initialization voltage signal at least for the control terminal of the driving transistor; the method further includes steps described below.

[0194] In an initialization phase, the first initialization module is turned on under the control of the gate driving signal and at least the initialization voltage signal is provided for the control terminal of the driving transistor.

[0195] Based on the above solution, optionally, the light-emitting control module includes a first light-emitting control unit and a second light-emitting control unit. The first light-emitting control unit is electrically connected between a first power signal terminal and a first terminal of the driving transistor. The second light-emitting control unit is electrically connected between a second terminal of the driving transistor and the light-emitting component; the display panel includes a first gate driving circuit and a second gate driving circuit; the first gate driving circuit includes multiple cascaded first gate driving units and the second gate driving circuit includes multiple cascaded second gate driving units; a control terminal of the data writing module is electrically connected to an output terminal of the second gate driving unit at the current stage; a control terminal of the light-emitting control unit and a control terminal of the threshold compensation module are electrically connected to an output terminal of the first gate driving unit at the current stage; a control terminal of the second light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the current stage or an output terminal of the first gate driving unit at the subsequent stage; the first initialization module is electrically connected between the initialization signal terminal and the second terminal of the driving transistor, and the control terminal of the first initialization module is electrically connected to the output terminal of the second gate driving unit at the previous stage; when the control terminal of the second light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the current stage, the first initialization module is used for providing the initialization voltage signal to the control terminal of the driving transistor; when the control terminal of the second light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the subsequent stage, the first initialization module is used for providing the initialization voltage signal for the control terminal of the driving transistor and the anode of the light-emitting component, as shown in FIGS. **9** and **14**.

[0196] The step in which in the initialization phase, the first initialization module is turned on under the control of the gate driving signal and at least the initialization voltage signal is provided for the control terminal of the driving transistor includes steps described below.

[0197] In the initialization phase, the first initialization module is turned on under the control of the second gate driving signal at the previous stage, at the same time, the threshold compensation module is turned on under the control of the first gate driving signal at the current stage, and provides the initialization voltage signal for the control terminal of the driving transistor.

[0198] The step in which in the data writing phase, the data writing module is turned on under the control of the gate driving signal and the data voltage signal is written into the control terminal of the driving transistor; at the same time, the threshold compensation module is turned on under the control of the gate driving signal, and the threshold voltage deviation of the driving transistor is detected and self-compensated includes steps described below.

[0199] In the data writing phase, the data writing module is turned on under the control of the second gate driving signal at the current stage and the data voltage signal is written into the control terminal of the driving transistor; at the same time, the threshold compensation module is turned on under the control of the first gate driving signal at the current stage, and the threshold voltage deviation of the driving transistor is detected and self-compensated.

[0200] The step in which in the light-emitting phase, the light-emitting control module is turned on under the control of the gate driving signal, and the driving current generated by the driving transistor is controlled to flow into the light-emitting component to drive the light-emitting component to emit light includes steps described below.

[0201] In the light-emitting phase, the first light-emitting control unit and the second light-emitting control unit are turned on under the control of the first gate driving signal at the current stage, and the driving current generated by the driving transistor is controlled to flow into the light-emitting component; or the first light-emitting control unit is turned on under the control of the first gate driving signal at the current stage and the second light-emitting control unit is turned on under the control of the first gate driving signal at the subsequent stage, the driving current generated by the driving transistor is controlled to flow into the light-emitting component.

[0202] When the control terminal of the second light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the subsequent stage, the method further includes: in the initialization phase, turning on the first initialization module under the control of the first gate driving signal at the previous stage and turning on the second light-emitting control unit under the control of the first gate driving signal at the subsequent stage, providing the initialization voltage signal for the anode of the light-emitting component.

[0203] Optionally, the control terminal of the second light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the current stage; the pixel driving circuit further includes a second initialization module which is electrically connected between the initialization signal terminal and the anode of the light-emitting component, a control terminal of the second initialization module is electrically connected to the output terminal of the second gate driving unit at the current stage, as shown in FIG. **12**.

[0204] The method further includes: in the data writing phase, turning on the second initialization module under the control of the second gate driving signal at the current stage and providing the initialization voltage signal for the anode of the light-emitting component.

[0205] Optionally, the light-emitting control module includes the first light-emitting control unit and the second light-emitting control unit; the first light-emitting control unit is electrically connected between the first power signal terminal and the first terminal of the driving transistor; the second light-emitting control unit is electrically connected between the second terminal of the driving transistor and the

light-emitting component; the pixel driving circuit further includes a blocking module, which is electrically connected between the first power signal terminal and the first terminal of the driving transistor and is connected in series to the first light-emitting control unit, a control terminal of the blocking module is electrically connected to an output terminal of the gate driving circuit, as shown in FIG. **17**.

[0206] The method further includes a step described below. In the data writing phase, the blocking module is turned off under the control of the gate driving signal to block a first power voltage signal of the first power signal terminal from being transmitted to the first terminal of the driving transistor.

[0207] Optionally, the display panel includes the first gate driving circuit and the second gate driving circuit. The first gate driving circuit includes multiple cascaded first gate driving units and the second gate driving circuit includes multiple cascaded second gate driving units; the control terminal of the data writing module is electrically connected to the output terminal of the second gate driving unit at the current stage; a control terminal of the first light-emitting control unit is electrically connected to an output terminal of the first gate driving unit at the previous stage; the control terminal of the blocking module and a control terminal of the threshold compensation module are electrically connected to the output terminal of the first gate driving unit at the current stage; a control terminal of the second light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the current stage or the output terminal of the first gate driving unit at the subsequent stage; the first initialization module is electrically connected between the initialization signal terminal and the control terminal of the driving transistor, and the control terminal of the first initialization module is electrically connected to the output terminal of the first gate driving unit at the previous stage; when the control terminal of the second light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the current stage, the first initialization module is used for providing the initialization voltage signal to the control terminal of the driving transistor; when the control terminal of the second light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the subsequent stage, the first initialization module is used for providing the initialization voltage signal for the control terminal of the driving transistor and the anode of the light-emitting component, as shown in FIGS. **19** and **24**.

[0208] The step in which in the initialization phase, the first initialization module is turned on under the control of the gate driving signal and at least the initialization voltage signal is provided for the control terminal of the driving transistor includes steps described below.

[0209] In the initialization phase, the first initialization module is turned on under the control of the first gate driving signal at the previous stage and the initialization voltage signal is provided for the control terminal of the driving transistor.

[0210] The step in which in the data writing phase, the blocking module is turned off under the control of the gate driving signal to block the first power voltage signal of the first power signal terminal from being transmitted to the first terminal of the driving transistor includes a step described below.

[0211] In the data writing phase, the blocking module is turned off under the control of the first gate driving signal at the current stage to block the first power voltage signal of the first power signal terminal from being transmitted to the first terminal of the driving transistor.

[0212] The step in which in the data writing phase, the data writing module is turned on under the control of the gate driving signal and the data voltage signal is written into the control terminal of the driving transistor; at the same time, the threshold compensation module is turned on under the control of the gate driving signal, and the threshold voltage deviation of the driving transistor is detected and self-compensated includes steps described below.

[0213] In the data writing phase, the data writing module is turned on under the control of the second gate driving signal at the current stage and the data voltage signal is written into the control terminal of the driving transistor; at the same time, the threshold compensation module is turned on under the control of the first gate driving signal at the current stage, and the threshold voltage deviation of the driving transistor is detected and self-compensated.

[0214] The step in which in the light-emitting phase, the light-emitting control module is turned on under the control of the gate driving signal, and the driving current generated by the driving transistor is controlled to flow into the light-emitting component to drive the light-emitting component to emit light includes steps described below.

[0215] In the light-emitting phase, the first light-emitting control unit is turned on under the control of the first gate driving signal at the previous stage and the second light-emitting control unit is turned on under the control of the first gate driving signal at the current stage, at the same time, the blocking module is turned on under the control of the first gate driving signal at the current stage and the driving current generated by the driving transistor is controlled to flow into the light-emitting component; or the first light-emitting control unit is turned on under the control of the first gate driving signal at the previous stage and the second light-emitting control unit is turned on under the control of the first gate driving signal at the subsequent stage, at the same time, the blocking module is turned on under the control of the first gate driving signal at the current stage and the driving current generated by the driving transistor is controlled to flow into the light-emitting component.

[0216] When the control terminal of the second light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the subsequent stage, the method further includes steps described below. In the initialization phase, the first initialization module is turned on under the control of the first gate driving signal at the previous stage and the second light-emitting control unit is turned on under the control of the first gate driving signal at the subsequent stage, the initialization voltage signal is provided for the anode of the light-emitting component.

[0217] Optionally, the control terminal of the second light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the current stage; the pixel driving circuit further includes a second initialization module which is electrically connected between the initialization signal terminal and the anode of the light-emitting component, a control terminal of the second initialization module is electrically connected to the output terminal of the second gate driving unit at the current stage, as shown in FIG. **22**.

[0218] The method further includes steps described below. In the data writing phase, the second initialization module is turned on under the control of the second gate driving signal at the current stage and the initialization voltage signal is provided for the anode of the light-emitting component.

[0219] Optionally, the display panel includes the first gate driving circuit and the second gate driving circuit; the first gate driving circuit includes multiple cascaded first gate driving units, the second gate driving circuit includes multiple cascaded second gate driving units; the control terminal of the data writing module is electrically connected to the output terminal of the second gate driving unit at the current stage; the control terminal of the first light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the previous stage; the control terminal of the blocking module and the control terminal of the threshold compensation module are electrically connected to the output terminal of the first gate driving unit at the current stage; the control terminal of the second light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the current stage or the output terminal of the first gate driving unit at the subsequent stage; and the first initialization module is electrically connected between the initialization signal terminal and the second terminal of the driving transistor, the control terminal of the first initialization module is electrically connected to the output terminal of the first gate driving unit at the previous stage, and the first initialization module is used for providing the initialization voltage signal to the control terminal of the driving transistor and the anode of the light-emitting component.

[0220] The step in which in the initialization phase, the first initialization module is turned on under the control of the gate driving signal and at least the initialization voltage signal is provided for the control terminal of the driving transistor includes steps described below.

[0221] In the initialization phase, the first initialization module is turned on under the control of the first gate driving signal at the previous stage, at the same time, the threshold compensation module is turned on under the control of the first gate driving signal at the current stage, and the initialization voltage signal is provided for the control terminal of the driving transistor.

[0222] The step in which in the data writing phase, the blocking module is turned off under the control of the gate driving signal to block the first power voltage signal of the first power signal terminal from being transmitted to the first terminal of the driving transistor includes a step described below.

[0223] In the data writing phase, the blocking module is turned off under the control of the first gate driving signal at the current stage to block the first power voltage signal of the first power signal terminal from being transmitted to the first terminal of the driving transistor.

[0224] The step in which in the data writing phase, the data writing module is turned on under the control of the gate driving signal and the data voltage signal is written into the control terminal of the driving transistor; at the same time, the threshold compensation module is turned on under the control of the gate driving signal, and the threshold voltage deviation of the driving transistor is detected and self-compensated includes steps described below.

[0225] In the data writing phase, the data writing module is turned on under the control of the second gate driving signal at the current stage and the data voltage signal is written into the control terminal of the driving transistor; at the same time, the threshold compensation module is turned on under the control of the first gate driving signal at the current stage, and the threshold voltage deviation of the driving transistor is detected and self-compensated.

[0226] The step in which in the light-emitting phase, the light-emitting control module is turned on under the control of the gate driving signal, and the driving current generated by the driving transistor is controlled to flow into the light-emitting component to drive the light-emitting component to emit light includes steps described below.

[0227] In the light-emitting phase, the first light-emitting control unit is turned on under the control of the first gate driving signal at the previous stage and the second light-emitting control unit is turned on under the control of the first gate driving signal at the current stage, at the same time, the blocking module is turned on under the control of the first gate driving signal at the current stage and the driving current generated by the driving transistor is controlled to flow into the light-emitting component; or the first light-emitting control unit is turned on under the control of the first gate driving signal at the previous stage and the second light-emitting control unit is turned on under the control of the first gate driving signal at the subsequent stage, at the same time, the blocking module is turned on under the control of the first gate driving signal at the current stage and the driving current generated by the driving transistor is controlled to flow into the light-emitting component.

[0228] When the control terminal of the second light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the subsequent stage, the method further includes steps described below. In the initialization phase, the first initialization module is turned on under the control of the first gate driving signal at the previous stage and the second light-emitting control unit is turned on under the control of the first gate driving signal at the subsequent stage, the initialization voltage signal is provided for the anode of the light-emitting component.

[0229] Optionally, the display panel includes the first gate driving circuit, and the first gate driving circuit includes multiple cascaded first gate driving units. The control terminal of the first light-emitting control unit is electrically connected to the output terminal of the first gate driving unit at the previous stage, and the control terminal of the blocking module and the control terminal of the data writing module are electrically connected to the output terminal of the first gate driving unit at the current stage or the output terminal of the first gate driving unit at the subsequent stage. The control terminal of the threshold compensation module and the control terminal of the second light-emitting control unit are electrically connected to the output terminal of the first gate driving unit at the current stage, and the first initialization module is electrically connected between the initialization signal terminal and the control terminal of the driving transistor. The control terminal of the first initialization module is electrically connected to the output terminal of the first gate driving unit at the previous stage, and the first initialization module is used for providing the initialization voltage signal for the control terminal of the driving transistor, as shown in FIGS. **30** and **31**.

[0230] The step in which in the initialization phase, the first initialization module is turned on under the control of the gate driving signal and at least the initialization voltage

signal is provided for the control terminal of the driving transistor includes steps described below.

[0231] In the initialization phase, the first initialization module is turned on under the control of the first gate driving signal at the previous stage and the initialization voltage signal is provided for the control terminal of the driving transistor.

[0232] The step in which in the data writing phase, the blocking module is turned off under the control of the gate driving signal to block the first power voltage signal of the first power signal terminal from being transmitted to the first terminal of the driving transistor; the data writing module is turned on under the control of the gate driving signal and the data voltage signal is written into the control terminal of the driving transistor; at the same time, the threshold compensation module is turned on under the control of the gate driving signal, and the threshold voltage deviation of the driving transistor is detected and self-compensated, in the light-emitting phase, the light-emitting control module is turned on under the control of the gate driving signal, and the driving current generated by the driving transistor is controlled to flow into the light-emitting component includes steps described below.

[0233] In the data writing phase, the blocking module is turned off under the control of the first gate driving signal at the current stage to block the first power voltage signal of the first power signal terminal from being transmitted to the first terminal of the driving transistor; the data writing module is turned on under the control of the first gate driving signal at the current stage and the data voltage signal is wrote into the control terminal of the driving transistor; at the same time, the threshold compensation module is turned on under the control of the first gate driving signal at the current stage, and the threshold voltage deviation of the driving transistor is detected and self-compensated, in the light-emitting phase, the first light-emitting control unit is turned on under the control of the first gate driving signal at the previous stage and the second light-emitting control unit is turned on under the control of the first gate driving signal at the current stage, at the same time, the blocking module is turned on under the control of the first gate driving signal at the current stage and the driving current generated by the driving transistor is controlled to flow into the light-emitting component.

[0234] Alternatively, in the data writing phase, the blocking module is turned off under the control of the first gate driving signal at the subsequent stage to block the first power voltage signal of the first power signal terminal from being transmitted to the first terminal of the driving transistor; the data writing module is turned on under the control of the first gate driving signal at the subsequent stage and the data voltage signal is wrote into the control terminal of the driving transistor; at the same time, the threshold compensation module is turned on under the control of the first gate driving signal at the current stage, and the threshold voltage deviation of the driving transistor is detected and self-compensated, in the light-emitting phase, the first light-emitting control unit is turned on under the control of the first gate driving signal at the previous stage and the second light-emitting control unit is turned on under the control of the first gate driving signal at the current stage, at the same time, the blocking module is turned on under the control of the first gate driving signal at the subsequent stage and the driving current generated by the driving transistor is controlled to flow into the light-emitting component.

[0235] Optionally, the display panel further includes the second gate driving circuit, the second gate driving circuit includes multiple cascaded second gate driving units; the pixel driving circuit further includes the second initialization module, the second initialization module is electrically connected between the initialization signal terminal and the anode of the light-emitting component, the control terminal of the second initialization module is electrically connected to the output terminal of the second gate driving unit at the current stage.

[0236] As shown in FIG. **36**, when the control terminal of the blocking module and the control terminal of the data writing module are electrically connected to the output terminal of the first gate driving unit at the current stage, the method further includes steps described below. In the data writing phase, the second initialization module is turned on under the control of the second gate driving signal at the current stage and the initialization voltage signal is provided for the anode of the light-emitting component.

[0237] As shown in FIG. **37**, when the control terminal of the blocking module and the control terminal of the data writing module are electrically connected to the output terminal of the first gate driving unit at the subsequent stage, the method further includes steps described below. In the initialization phase, the second initialization module is turned on under the control of the second gate driving signal at the current stage and the initialization voltage signal is provided for the anode of the light-emitting component.

[0238] Optionally, the pixel driving circuit further includes the second initialization module which is electrically connected between the initialization signal terminal and the anode of the light-emitting component, and the control terminal of the second initialization module is electrically connected to the output terminal of the first gate driving unit at the current stage.

[0239] As shown in FIG. **41**, when the control terminal of the blocking module and the control terminal of the data writing module are electrically connected to the output terminal of the first gate driving unit at the current stage, the method further includes steps described below. In the data writing phase, the second initialization module is turned on under the control of the first gate driving signal at the current stage and the initialization voltage signal is provided for the anode of the light-emitting component.

[0240] As shown in FIG. **42**, when the control terminal of the blocking module and the control terminal of the data writing module are electrically connected to the output terminal of the first gate driving unit at the subsequent stage, the method further includes steps described below. In the initialization phase and the data writing phase, the second initialization module is turned on under the control of the first gate driving signal at the current stage and the second initialization module provides the initialization voltage signal for the anode of the light-emitting component.

[0241] Based on the above inventive concept, the embodiments of the present disclosure further provide a display device. The display device includes the display panel described in any embodiment of the present disclosure. Therefore, the display device also has the beneficial effects of the display panel provided by the embodiments of the

present disclosure, and the same content may be understood by referring to the above description and is not repeated hereinafter.

[0242] Exemplarily, FIG. **46** is a structural diagram of a display device provided by an embodiment of the present disclosure. As shown in FIG. **46**, the display device **200** provided by this embodiment of the present disclosure includes the display panel **100** provided by the embodiments of the present disclosure. The display device **200**, for example, may be a touch display screen, a mobile phone, a tablet, a laptop, a television, or any electronic device having a display function.

[0243] Exemplarily, FIG. **47** is a block diagram of another pixel driving circuit provided by an embodiment of the present disclosure. As shown in FIG. **47**, the pixel driving circuit includes the driving transistor **110**, the data writing module **130**, the initialization module **150/170**, the threshold compensation transistor **140**, the first light-emitting control unit **161**, and the second light-emitting control unit **162**. The data writing module **130** is configured for transmitting a data voltage signal Vdata to a control terminal of the driving transistor **110**. The first light-emitting control unit **161** is electrically connected between a positive power signal terminal PVDD and the first terminal of the driving transistor **110**, and the second light-emitting control unit **162** is electrically connected between the second terminal of the driving transistor **110** and the light-emitting component **20**; a control terminal of the initialization module **150/170** and the control terminal of the first light-emitting control unit **161** are configured for receiving a transmit driving signal generated by an output terminal E**1** of a previous-stage transmit driving unit. The control terminal of the second light-emitting control unit **162** is configured for receiving a transmit driving signal generated by an output terminal E**2** of a current-stage transmit driving unit, or the control terminal of the second light-emitting control unit **162** is configured for receiving a transmit driving signal generated by an output terminal E**3** of a subsequent-stage transmit driving unit. The threshold compensation transistor **140** is electrically connected between the control terminal of the driving transistor **110** and the second terminal of the driving transistor **110**, the control terminal of the threshold compensation transistor **140** is configured for receiving the transmit driving signal generated by the output terminal E**2** of the current-stage transmit driving unit.

[0244] It is to be noted that the above are merely preferred embodiments of the present disclosure and the technical principles used therein. It is to be understood by those skilled in the art that the present disclosure is not limited to the specific embodiments described herein. Those skilled in the art can make various apparent modifications, adaptations, combinations, and substitutions without departing from the scope of the present disclosure. Therefore, while the present disclosure has been described in detail through the preceding embodiments, the present disclosure is not limited to the preceding embodiments and may further include more other equivalent embodiments without departing from the concept of the present disclosure. The scope of the present disclosure is determined by the scope of the appended claims.

What is claimed is:

1. A display panel, comprising:

a gate driving circuit, a pixel driving circuit, and a light-emitting component;

wherein the pixel driving circuit comprises a driving transistor, a data writing module, an initialization module, and a light-emitting control module;

wherein the data writing module is configured for transmitting a data voltage signal to a control terminal of the driving transistor such that the driving transistor generates a driving current according to the data voltage signal provided by a data signal terminal;

wherein the initialization module is configured for providing an initialization voltage signal to at least one of the control terminal of the driving transistor or an anode of the light-emitting component;

wherein the light-emitting control module is connected in series between a positive power signal terminal and the light-emitting component; and

wherein a transistor in the initialization module is a P-type transistor and a transistor in the light-emitting control module is an N-type transistor, or a transistor in the initialization module is an N-type transistor and a transistor in the light-emitting control module is a P-type transistor;

wherein a control terminal of the initialization module and a control terminal of the light-emitting control module are configured for receiving a gate driving signal generated by a same gate driving circuit.

2. The display panel of claim **1**, wherein the gate driving circuit comprises a transmit driving circuit, the gate driving signal is a transmit driving signal.

3. The display panel of claim **1**, wherein the pixel driving circuit is configured for receiving at most two types of gate driving signals.

4. The display panel of claim **1**, wherein the pixel driving circuit further comprises a first light-emitting control unit and a second light-emitting control unit;

the first light-emitting control unit is electrically connected between the positive power signal terminal and a first terminal of the driving transistor, and the second light-emitting control unit is electrically connected between a second terminal of the driving transistor and the light-emitting component.

5. The display panel of claim **4**, wherein the initialization module comprises a gate initialization transistor which is electrically connected between an initialization signal terminal and the control terminal of the driving transistor;

the gate driving circuit comprises a transmit driving circuit, the transmit driving circuit comprises a plurality of cascaded transmit driving units; and

a control terminal of the gate initialization transistor and a control terminal of the first light-emitting control unit are configured for receiving a transmission driving signal generated by a previous-stage transmission driving unit.

6. The display panel of claim **5**, wherein a control terminal of the second light-emitting control unit is configured for receiving a transmit driving signal generated by a current-stage transmit driving unit.

7. The display panel of claim **5**, wherein a control terminal of the second light-emitting control unit is configured for receiving a transmit driving signal generated by a subsequent-stage transmit driving unit.

8. The display panel of claim 1, wherein the pixel driving circuit further comprises a threshold compensation transistor electrically connected between the control terminal of the driving transistor and a second terminal of the driving transistor, and the control terminal of the initialization module and a control terminal of the threshold compensation transistor are configured for receiving a gate driving signal generated by a same gate driving circuit.

9. The display panel of claim 8, wherein the gate driving circuit comprises a transmit driving circuit, the transmit driving circuit comprises a plurality of cascaded transmit driving units, and the control terminal of the threshold compensation transistor is configured for receiving a transmit driving signal generated by a current-stage transmit driving unit.

10. The display panel of claim 8, wherein a transistor in the initialization module and the threshold compensation transistor are each a semiconductor oxide transistor.

11. The display panel of claim 5, wherein the gate initialization transistor is configured for initializing the anode of the light-emitting component.

12. The display panel of claim 5, wherein the pixel driving circuit further comprises an anode initialization transistor electrically connected between the initialization signal terminal and the anode of the light-emitting component; and

the gate driving circuit comprises a scan driving circuit, a control terminal of the anode initialization transistor is configured for receiving a scan driving signal generated by the scan driving circuit.

13. The display panel of claim 5, wherein the pixel driving circuit further comprises an anode initialization transistor electrically connected between the initialization signal terminal and the anode of the light-emitting component, and a control terminal of the anode initialization transistor is configured for receiving a transmit driving signal generated by a current-stage transmit driving unit.

14. The display panel of claim 4, wherein the initialization module comprises an initialization transistor electrically connected between an initialization signal terminal and the second terminal of the driving transistor;

the gate driving circuit comprises a transmit driving circuit, the transmit driving circuit comprises a plurality of cascaded transmit driving units; and

a control terminal of the initialization transistor and a control terminal of the first light-emitting control unit are configured for receiving a transmit driving signal generated by a previous-stage transmit driving unit.

15. The display panel of claim 14, wherein a control terminal of the second light-emitting control unit is configured for receiving a transmit driving signal generated by a current-stage transmit driving unit.

16. The display panel of claim 14, wherein a control terminal of the second light-emitting control unit is configured for receiving a transmit driving signal generated by a subsequent-stage transmit driving unit.

17. The display panel of claim 14, wherein the pixel driving circuit further comprises an initialization phase, a data writing phase and a light-emitting phase, the initialization transistor is configured for initializing both the control terminal of the driving transistor and the anode of the light-emitting component during the initialization phase.

18. The display panel of claim 14, wherein a transistor in the initialization module is a semiconductor oxide transistor.

19. The display panel of claim 5, wherein the data writing module comprises a data writing transistor electrically connected between a data voltage signal terminal and the first terminal of the driving transistor; and

the gate driving circuit further comprises a scan driving circuit, a control terminal of the data writing transistor is configured for receiving a scan driving signal generated by a scan driving circuit.

20. A display panel, comprising:

a transmit driving circuit, a pixel driving circuit, and a light-emitting component;

wherein the pixel driving circuit comprises a driving transistor, a data writing transistor, a semiconductor oxide initialization transistor, and a light-emitting control transistor;

wherein the data writing transistor is configured for transmitting a data voltage signal to a control terminal of the driving transistor such that the driving transistor generates a driving current according to the data voltage signal provided by a data signal terminal;

wherein the semiconductor oxide initialization transistor is configured for providing an initialization voltage signal for a gate of the driving transistor;

wherein the light-emitting control transistor is connected in series between a positive power signal terminal and the light-emitting component;

wherein a gate of the semiconductor oxide initialization transistor and a gate of the light-emitting control transistor are configured for receiving a transmit driving signal generated by a transmit driving circuit.

21. The display panel of claim 20, wherein the light-emitting control transistor comprises a first light-emitting control transistor and a second light-emitting control transistor;

the first light-emitting control transistor is electrically connected between the positive power signal terminal and a first terminal of the driving transistor, and the second light-emitting control transistor is electrically connected between a second terminal of the driving transistor and the light-emitting component.

22. The display panel of claim 20, wherein the semiconductor oxide initialization transistor is electrically connected between an initialization signal terminal and the gate of the driving transistor;

the transmit driving circuit comprises a plurality of cascaded transmit driving units, and a gate of the semiconductor oxide initialization transistor and a gate of the first light-emitting control transistor are configured for receiving a transmit driving signal generated by a previous-stage transmit driving unit.

23. The display panel of claim 22, wherein a gate of the second light-emitting control transistor is configured for receiving a transmit driving signal generated by a current-stage transmit driving unit.

24. The display panel of claim 22, wherein a gate of the second light-emitting control transistor is configured for receiving a transmit driving signal generated by a subsequent-stage transmit driving unit.

25. The display panel of claim **24**, wherein the pixel driving circuit comprises an initialization phase, a data writing phase and a light-emitting phase, the semiconductor oxide initialization transistor is configured for initializing an anode of the light-emitting component.

26. The display panel of claim **23**, wherein the pixel driving circuit further comprises a semiconductor oxide anode initialization transistor which is electrically connected between an initialization signal terminal and an anode of the light-emitting component, and a gate of the semiconductor oxide anode initialization transistor is configured for receiving a transmit driving signal generated by a current-stage transmit driving unit.

27. The display panel of claim **23**, wherein the pixel driving circuit further comprises an anode initialization transistor which is electrically connected between the initialization signal terminal and an anode of the light-emitting component;

wherein the display panel further comprises a scan driving circuit, a gate of the anode initialization transistor is configured for receiving a scan driving signal generated by a scan driving circuit.

28. The display panel of claim **22**, wherein the pixel driving circuit comprises a semiconductor oxide threshold compensation transistor which is electrically connected to the gate of the driving transistor and one terminal of the driving transistor, and the gate of the semiconductor oxide initialization transistor and the semiconductor oxide threshold compensation transistor are configured for receiving a transmit driving signal generated by a transmit driving circuit.

29. The display panel of claim **28**, wherein the gate of the semiconductor oxide initialization transistor is configured for receiving a transmit driving signal generated by a current-stage transmit driving unit.

30. The display panel of claim **28**, wherein the data writing transistor is electrically connected between a data voltage signal terminal and an other terminal of the driving transistor;

wherein the display panel further comprises a scan driving circuit, a gate of the data writing transistor is configured for receiving a scan driving signal generated by a scan driving circuit.

31. A display device, comprising a display panel,

wherein the display panel comprises:

a gate driving circuit, a pixel driving circuit, and a light-emitting component;

wherein the pixel driving circuit comprises a driving transistor, a data writing module, an initialization module, and a light-emitting control module;

wherein the data writing module is configured for transmitting a data voltage signal to a control terminal of the driving transistor such that the driving transistor generates a driving current according to the data voltage signal provided by a data signal terminal;

wherein the initialization module is configured for providing an initialization voltage signal to at least one of the control terminal of the driving transistor or an anode of the light-emitting component;

wherein the light-emitting control module is connected in series between a positive power signal terminal and the light-emitting component; and

wherein a transistor in the initialization module is a P-type transistor and a transistor in the light-emitting control module is an N-type transistor, or a transistor in the initialization module is an N-type transistor and a transistor in the light-emitting control module is a P-type transistor;

wherein a control terminal of the initialization module and a control terminal of the light-emitting control module are configured for receiving a gate driving signal generated by a same gate driving circuit.

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