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Semiconductor device and method of manufacturing semiconductor device

Abstract

Provided is a semiconductor device capable of suppressing breakdown of the semiconductor device by a full depletion of a semiconductor layer. The semiconductor device includes: a first semiconductor layer of a first conductivity type provided on a second main surface side of a semiconductor base body; a second semiconductor layer of the first conductivity type having a first conductivity type impurity concentration lower than that of the first semiconductor layer and provided closer to a first main surface than the first semiconductor layer is; and a third semiconductor layer of a second conductivity type provided closer to the first main surface than the second semiconductor layer is. An impurity concentration distribution of the third semiconductor layer with respect to thickness direction of the semiconductor base body has a plurality of peaks. A thickness W of the third semiconductor layer satisfies a certain condition.

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Background/Summary

BACKGROUND OF THE INVENTION
Field of the Invention
(1) The present disclosure relates to a semiconductor device and a method of manufacturing the semiconductor device.
Description of the Background Art
(2) Japanese Patent Application Laid-Open No. 2013-021142 discloses a semiconductor device that

have a configuration for decreasing switching losses.

(3) In semiconductor devices, there is a problem that a semiconductor layer is fully-depleted and the semiconductor device is broken down during recovery operations with high current and high voltage.

SUMMARY

(4) The present disclosure has an object to provide a semiconductor device capable of suppressing full depletion of a semiconductor layer in recovery operation with high current and high voltage, and capable of suppressing breakdown of the semiconductor device by the full depletion of the semiconductor layer.

(5) The semiconductor device of the present disclosure includes: a semiconductor base body having a first main surface and a second main surface; a first electrode; and a second electrode. The semiconductor base body includes: a first semiconductor layer of a first conductivity type provided on the second main surface side of the semiconductor base body; a second semiconductor layer of the first conductivity type having a first conductivity type impurity concentration lower than that of the first semiconductor layer and provided closer to the first main surface than the first semiconductor layer is; and a third semiconductor layer of a second conductivity type provided closer to the first main surface than the second semiconductor layer is. The first semiconductor layer is electrically connected to the second electrode in the second main surface. The third semiconductor layer is electrically connected to the first electrode in the first main surface. An impurity concentration distribution of the third semiconductor layer with respect to thickness direction of the semiconductor base body has a plurality of peaks. A thickness W of the third semiconductor layer, a thickness W_{N-} of the second semiconductor layer, the elementary charge q, a relative permittivity ε_s of the semiconductor material, the vacuum permittivity ε_0, a rated voltages V_r, a rated current density J_r, a carrier lifetime τ of a second conductivity type carrier in the second semiconductor layer, a dose amount D_A of the third semiconductor layer, and $\alpha(\tau)=4.15/(\ln(2.58\tau+1))^{4.77}+225)$ which represents a relation between an average carrier concentration of the second semiconductor layer in on-state of the semiconductor device and an electric charge concentration in a depletion layer around a border of the second semiconductor layer and the third semiconductor layer among the second semiconductor layer in recovery process of the semiconductor device, satisfies $W > (1.6\varepsilon_s\varepsilon_0 V_r)/qD_A - (2qW_{N-}D_A)/(2.5\alpha(\tau)J_r\tau)$.

(6) According to the present disclosure, a semiconductor device capable of suppressing full depletion of a semiconductor layer in the recovery operation with high current and high voltage, and capable of suppressing breakdown of the semiconductor device by the full depletion of the semiconductor layer.

(7) These and other objects, features, aspects and advantages of the present disclosure will become more apparent from the following detailed description of the present disclosure when taken in conjunction with the accompanying drawings.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) FIG. **1** is a diagram showing a semiconductor device according to the embodiment 1.

(2) FIG. **2** is a diagram showing a semiconductor device according to the embodiment 2.

(3) FIG. **3** is a diagram showing the impurity concentration distribution according to the embodiment 1 and comparative example.

(4) FIG. **4** is a diagram showing the relation between the maximum value of the impurity concentration and the maximum recovery blocking power in the semiconductor devices according to the embodiment 1 and according to the comparative example.

(5) FIG. **5** is a diagram showing the relation between forward voltage drop and recovery loss of the semiconductor devices according to the embodiment 1 and the comparative examples.

(6) FIG. **6** is a diagram showing leak current of the semiconductor devices of the comparative examples and the embodiment 1.

(7) FIGS. **7** to **9** are diagrams showing a state of the semiconductor device during manufacturing in the manufacturing method according to the embodiment 1.

(8) FIGS. **10** to **12** are diagrams showing the time dependence of current and voltage during recovery operation of the semiconductor device according to the embodiment 1.

(9) FIG. **13** is a diagram showing the electric field distribution around the PN junction part **6**, which is the border between the N− type substrate **1** and the P type diffusion layer **3**, in the semiconductor device according to the embodiment 1.

(10) FIGS. **14** to **16** are diagrams showing carrier concentrations in in on-states and recovery states in the semiconductor device according to the embodiment 1.

(11) FIG. **17** is a diagram showing the factor of proportionality $\alpha(\tau)$ which is empirically obtained.

(12) FIG. **18** is a diagram showing a representative value of the power supply voltage for each of the rated voltages in the semiconductor devices according to the embodiment 1.

(13) FIG. **19** is a diagram showing a representative value of rated current density and a representative value of high current density in on-state just before a switching for each of the rated voltages in the semiconductor devices according to the embodiment 1.

(14) FIG. **20** is a diagram showing a representative value of the thickness of the N− type substrate **1** for each of the rated voltages in the semiconductor devices according to the embodiment 1.

(15) FIGS. **21** and **22** are diagrams showing the semiconductor devices according to comparative examples.

(16) FIG. **23** is a flowchart showing a manufacturing method of a semiconductor device according to embodiments 1.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(17) In the following description N type and P type, which are the conductivity types of the semiconductor, are interchangeable.

COMPARATIVE EXAMPLE

(18) FIG. **21** shows a semiconductor device **10z1** according to a comparative example. FIG. **22** shows a semiconductor device **10z2** according to a comparative example.

(19) The semiconductor device **10z1** includes a semiconductor base body **100**, an anode electrode **4**, and a cathode electrode **5**.

(20) The semiconductor base body **100** has a first main surface **100***a* and a second main surface **100***b*. The semiconductor base body **100** includes an N− type substrate **1**, an N type diffusion layer **2**, and a P type diffusion layer **3z1**.

(21) The N type diffusion layer **2** is located on the second main surface **100***b* side of the semiconductor base body **100**. The N− type substrate **1** is closer to the first main surface **100***a* than the N type diffusion layer **2** is. The P type diffusion layer **3** is closer to the first main surface **100***a* than the N− type substrate **1** is. N type impurity concentration of the N− type substrate **1** is lower than N type impurity concentration of the N type diffusion layer **2**.

(22) Compared to the semiconductor device **10z1**, the semiconductor device **10z2** includes a P type diffusion layer **3z2** instead of the P type diffusion layer **3z1**. In addition, lifetime killers **7** are provided in the N− type substrate **1** in the semiconductor device **10z2**.

(23) The semiconductor device **10z1** and the semiconductor device **10z2** are each a diode. In the following description, the semiconductor device **10z1** may be referred to as a comparative example 1, and the semiconductor device **10z2** may be referred to as a comparative example 2.

(24) FIG. **3** shows the impurity concentration of the P type diffusion layer **3z1** and the N− type substrate **1** along the B-B line shown in FIG. **21** (comparative example 1 in FIG. **3**).

(25) FIG. **3** shows the impurity concentration of the P type diffusion layer **3z2** and the N− type

substrate **1** along the C-C line shown in FIG. **22** (comparative example 2 in FIG. **3**).

(26) In FIG. **3**, horizontal axis represents positions with respect to thickness direction. In FIG. **3**, the position with depth 0 μm corresponds to the first main surface **100***a*.

(27) In the semiconductor device **10z1**, to reduce switching loss, the dose amount to the P type diffusion layer **3z1** is lowered and the impurity concentration of the P type diffusion layer **3z1** is lowered. Nevertheless, in a case where the impurity concentration of the P type diffusion layer **3z1** is lower than or equal to 2.5 E 16 cm.sup.−3, during a recovery operation after a switching from an on-state in which a high voltage is applied and a high current flowed in forward direction, a depletion layer around the border of the P type diffusion layer **3z1** and the N− type substrate **1** reach to the anode electrode **4**, and the device is broken down by the recovery current in the P type diffusion layer **3z1**. Thus, there is a limit to the reduction in switching loss by lowering the impurity concentration of the P type diffusion layer **3z1**.

(28) In the semiconductor device **10z2**, lifetime killers **7** are provided in the N− type substrate **1** to reduce the switching loss. The lifetime killers **7** are formed by electron beam irradiation from the second main surface **100***b* side. Since the electron beam passes the N type diffusion layer **2** which is a surface layer of the semiconductor base body **100** in the second main surface **100***b* side, the electron beam irradiation increases the unevenness of the properties among the semiconductor devices **10z2**.

(29) To reduce the switching loss, configurations in which the impurity concentration of the P type diffusion layer **3z1** or the P type diffusion layer **3z2** varies depending in-plane position, and P+ regions with relatively high impurity concentration and P regions with relatively low impurity concentration are disposed alternatively in one of in-plane directions may be adopted. In this case, when the reverse high voltage is applied during the recovery operation after the switching from on-state with high forward current, an avalanche current is generated by the concentration of the electric field on the border portion between the P+ regions and the P regions, and the border portion between the P+ regions and the P regions is broken down by the heat.

A. Embodiment 1

(30) <A-1. Configuration and Operation>

(31) FIG. **1** shows a semiconductor device **10** according to the embodiment 1.

(32) The semiconductor device **10** includes a semiconductor base body **100**, an anode electrode **4**, and a cathode electrode **5**.

(33) The semiconductor base body **100** has a first main surface **100***a* and a second main surface **100***b*. The semiconductor base body **100** includes an N− type substrate **1** (an example of a second semiconductor layer), an N type diffusion layer **2** (an example of a first semiconductor layer), and a P type diffusion layer **3** (an example of a third semiconductor layer). The semiconductor base body **100** includes the P type diffusion layer **3**, which is composed of semiconductor layer with one conductive type, in the surface layer on the first main surface **100***a*.

(34) The junction part between the N− type substrate **1** and the P type diffusion layer **3** is referred to as the PN junction part **6**.

(35) The P type diffusion layer **3** is electrically connected to the anode electrode **4** in the first main surface **100***a*. The N type diffusion layer **2** is electrically connected to the cathode electrode **5** in the second main surface **100***b*.

(36) The P type diffusion layer **3** includes a P type diffusion layer **3***a*, a P type diffusion layer **3***b*, and a P type diffusion layer **3***c*.

(37) The N type diffusion layer **2** is located in the surface layer on the second main surface **100***b* side of the semiconductor base body **100**.

(38) The N− type substrate **1** is closer to the first main surface **100***a* than the N type diffusion layer **2** is. The P type diffusion layer **3** is closer to the first main surface **100***a* than the N− type substrate **1** is. The N type impurity concentration of the N− type substrate **1** is lower than the N type impurity concentration of the N type diffusion layer **2**.

(39) The N− type substrate **1** is a semiconductor layer containing, for example, arsenic or phosphorus as N type impurities.

(40) Diode structure is formed by the N type diffusion layer **2**, the P type diffusion layer **3**, and the N− type substrate **1**.

(41) The semiconductor device **10** is a diode. The semiconductor device **10** may be a power semiconductor device which includes a diode as a part thereof, such as a reverse-conducting insulated gate bipolar transistor (RC-IGBT).

(42) The N type impurity concentration of the N− type substrate **1** is 1.0E12 cm.sup.−3 to 1.0E14 cm.sup.−3.

(43) The N type diffusion layer **2** is a semiconductor layer containing, for example, arsenic or phosphorus as N type impurities. The N type impurity concentration of the N type diffusion layer **2** is 1.0E14 cm.sup.−3 to 1.0E21 cm.sup.−3.

(44) The P type diffusion layer **3** is a semiconductor layer containing, for example, boron or aluminum as P type impurities. The P type impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction has plurality of peaks. In the following, a case is described where the P type impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction has two peaks, as an example. Nevertheless, the P type impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction may have more than two peaks.

(45) The P type diffusion layer **3***a* and the P type diffusion layer **3***c* are each the region around each of the two peaks of the P type impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction. The P type diffusion layer **3***b* is a region between the two peaks, namely a region between the P type diffusion layer **3***a* and the P type diffusion layer **3***c*.

(46) FIG. **3** shows an example of the impurity concentration distribution along the A-A line in FIG. **1** (shown as the embodiment 1 in FIG. **3**). In FIG. **3**, the position with depth 0 μm corresponds to the first main surface **100***a*. In FIG. **3**, the difference of the N type impurity concentration and the P type impurity concentration is plotted. In the P type diffusion layer **3***b*, the impurity concentration of the P type impurity is higher than the impurity concentration of the N type impurity. In the N− type substrate **1**, the impurity concentration of the N type impurity is higher than the impurity concentration of the P type impurity.

(47) The maximum value of the impurity concentration distribution of the P type diffusion layer **3** is less than or equal to 1.0E17 cm.sup.−3.

(48) The P type impurity concentration of the P type diffusion layer **3***b* is higher than the N type impurity concentration N.sub.D of the N− type substrate **1**. As a result, latch-up is suppressed. The same applies for the case where P type impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction has more than two peaks. Namely, in a region of the P type diffusion layer **3** which locates between the peak closest to the first main surface **100***a* and the peak closest to the second main surface **100***b* among the peaks of the impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction, the minimum value of the P type impurity concentration is higher than the N type impurity concentration of the N− type substrate **1**.

(49) The P type impurity concentration of the P type diffusion layer **3***b* is higher than 1.0E13 cm.sup.−3.

(50) Of the two peaks of the P type impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction, impurity concentrations are highest at the peak closer to the first main surface **100***a*. In the case where P type impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction has more than two peaks, impurity concentrations are highest at the peak closest to the first main surface **100***a* among the more than two peaks, for example.

(51) The P type impurity concentration distribution of the P type diffusion layer **3** with respect to

the thickness direction may be such that it has two peaks and the impurity concentrations are highest at the peak closer to the second main surface **100***b* of the two peaks. Similarly, in the case where P type impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction has more than two peaks, the impurity concentrations may be highest at the peak closest to the second main surface **100***b* among the more than two peaks, for example.

(52) <A-2. Comparison with the Comparative Example>

(53) FIGS. **4** to **6** show the result of comparison between the semiconductor devices according to the present embodiment and the semiconductor devices according to the comparative example.

(54) FIG. **4** shows the relation between the maximum value of the impurity concentration of the P type diffusion layer **3** and the maximum recovery blocking power Prr in the semiconductor devices **10***z*1 of the comparative example and in the semiconductor devices **10** of the embodiment 1. FIG. **4** shows the data at 150° C. The maximum recovery blocking power is a maximum value of the electric power of the reverse current which is allowed to the semiconductor devices **10***z*1 or the semiconductor devices **10**. As shown in FIG. **4**, in the configuration of the comparative example 1, Prr substantially decrease in the case where the maximum value of the impurity concentration of the P type diffusion layer **3***z*1 is lower than or equal to 2.5E16 cm.sup.−3. On the other hand, in the configuration of the current embodiment, Prr do not show substantial decrease even in the case where the maximum value of the impurity concentration of the P type diffusion layer **3** is lower than or equal to 2.5E16 cm.sup.−3. As described above, with the configuration in which the P type impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction has two peaks, impurity implantation amount into the P type diffusion layer **3** can be lowered with the decrease of the maximum recovery blocking power Prr suppressed. By lowering the impurity implantation amount into the P type diffusion layer **3**, flow of holes from P type diffusion layer **3** into the N− type substrate **1** is suppressed, and the switching loss is suppressed.

(55) FIG. **5** shows the trade-off relation between forward voltage drop Vf and the recovery loss Erec of the semiconductor devices of the embodiment 1, the comparative example 1, the comparative example 2, and a comparative example 3. In FIG. **5**, the comparative example 3 represents the configuration in which a change to increase the P type impurity concentration of the P type diffusion layer **3***z*1 is made with respect to the comparative example 1. In the semiconductor device **10***z*1 of the comparative example 1, suppression of the decrease of the maximum recovery blocking power Prr is incompatible with the configuration with low Erec. In the semiconductor device of the comparative example 3, the forward voltage drop Vf is lower and the recovery loss Erec is larger compared to those of the comparative example 2. In the semiconductor device **10** of the current embodiment and the semiconductor device **10***z*2 of the comparative example 2, decrease of the maximum recovery blocking power Prr is suppressed and Erec is low. In the semiconductor device **10** of the current embodiment, Erec almost comparable to Erec of the semiconductor device **10***z*2 of the comparative example 2 is realized without forming lifetime killers by electron beam irradiation.

(56) FIG. **6** shows the leak current Irrm of the semiconductor devices of the comparative examples and the semiconductor device **10** of the embodiment 1. In FIG. **6**, variation of the Irr among the products is shown with error bars. In the semiconductor devices **10***z*2 in which the lifetime killers **7** is formed by electron beam irradiation, the variation of the leak current among the products is increased, because the electron beam passes the N type diffusion layer **2** in the electron beam irradiation. As a result, in the semiconductor devices **10***z*2, the variation of the reverse recovery safe operation area (RRSOA) among products increases. In the semiconductor devices **10** of the current embodiment, the variation of the leak current is suppressed compared to that of the semiconductor devices **10***z*2. As a result, in the semiconductor devices **10** of the current embodiment, the variation of the RRSOA among products is suppressed.

(57) <A-3. Thickness W of the P Type Diffusion Layer **3**>

(58) The thickness W of the P type diffusion layer **3** preferably is less than or equal to 20 μm

because of the restriction by high-energy (namely, MeV class) ion implantation devices and the restriction by the time and temperature in thermal diffusion.

(59) Lower limit of the thickness W of the P type diffusion layer **3** depends on usage of the semiconductor device **10**, carrier lifetime of the N− type substrate **1**, thickness W.sub.N− of the N− type substrate **1**, and dose amount D.sub.A of the P type diffusion layer **3**. The usage of the semiconductor device **10** means how are the current density J and power supply voltage V.sub.cc in the on-state, for example. In the following, lower limit of the thickness W of the P type diffusion layer **3** which is desirable for avoiding breakdown of the semiconductor device **10** is described.

(60) <A-3-1. Causes of Breakdown of the Semiconductor Devices **10**>

(61) Causes of breakdown of the Semiconductor device **10** in recovery operations include current breakdown and voltage breakdown. There are three types of voltage breakdown: full depletion of the P type diffusion layer **3**, dynamic avalanche, and overshoot of voltage.

(62) The full depletion of the P type diffusion layer **3** occurs while the voltage V.sub.ka, which is voltage between anode electrode **4** and cathode electrode **5**, is rising toward the power supply voltage V.sub.cc after the voltage V.sub.ka changed from forward voltage to reverse voltage. The voltage V.sub.ka is defined to be positive when reverse voltage is applied. Low impurity concentration of the P type diffusion layer **3**, high current density in on-state, long carrier lifetime in the N− type substrate **1**, and the like make the full depletion of the P type diffusion layer **3** more likely to occur. The mechanism of the breakdown of the semiconductor device **10** by the full depletion of the P type diffusion layer **3** is as follows. Since the carrier concentration in the N− type substrate **1** is high, the depletion layer which extends toward the P type diffusion layer **3** from the border between the N− type substrate **1** and the P type diffusion layer **3** reach to the anode electrode **4**. The anode layer is fully depleted without the electric field in the PN junction part **6**, which is the border between the N− type substrate **1** and the P type diffusion layer **3**, exceed the critical electric field. As a result, recovery current drastically increases in the depletion layer, and then the semiconductor device **10** is broken down.

(63) The dynamic avalanche occurs while the V.sub.ka is rising toward the power supply voltage V.sub.cc after the voltage V.sub.ka changed from forward voltage to reverse voltage. High impurity concentration of P type diffusion layer **3**, high current density in on-state, long carrier lifetime in the N− type substrate **1**, and the like make the dynamic avalanche more likely to occur. The mechanism of the breakdown of the semiconductor device **10** by the dynamic avalanche is as follows. Since the carrier concentration in the P type diffusion layer **3** and the N− type substrate **1** is high, the electric field in the PN junction part **6**, which is the border between the N− type substrate **1** and the P type diffusion layer **3**, exceeds the critical electric field even though the V.sub.ka is lower than or equal to the static breakdown voltage, and then an avalanche breakdown occur.

(64) The overshoot of voltage (also called snap off) occurs while the voltage V.sub.ka is rising beyond the power supply voltage V.sub.cc after the voltage V.sub.ka changed from forward voltage to reverse voltage. Low current density in on-state, short carrier lifetime in the N− type substrate **1**, and the like make the overshoot of voltage more likely to occur. The mechanism of the breakdown of the semiconductor device **10** by the overshoot of voltage is as follows. The carrier concentration in the N− type substrate **1** drastically decrease, a voltage higher than the static breakdown voltage is instantly applied between the anode electrode **4** and the cathode electrode **5**, the electric field in the PN junction part **6**, which is the border between the N− type substrate **1** and the P type diffusion layer **3**, exceeds the critical electric field, and then an avalanche breakdown occur.

(65) In the following, lower limit of the thickness W of the P type diffusion layer **3** is derived as a condition to suppress the full depletion of the P type diffusion layer **3** among the voltage breakdown.

(66) <A-3-2. Depletion of the P Type Diffusion Layer **3** in Recovery Operation>

(67) The impurity concentration of the P type diffusion layer **3** is higher than the impurity

concentration of the N− type substrate **1**, and the former is 10.sup.4 to 10.sup.7 times as high as the latter, for example. As a result, when the reverse voltage is statically applied to the semiconductor device **10**, the depletion layer around the border of the N− type substrate **1** and the P type diffusion layer **3** mainly extends toward the N− type substrate **1**, and the extent of the depletion layer in the P type diffusion layer **3** is negligible.

(68) On the other hand, how the depletion layer around the border of the N− type substrate **1** and the P type diffusion layer **3** extends during the recovery operation is different from that in the case where the reverse voltage is statically applied to the semiconductor device **10**.

(69) In the on-state of the semiconductor device **10**, carriers flow into the N− type substrate **1** from the P type diffusion layer **3** and the N type diffusion layer **2**, and conductivity modulation occurs. In the on-state of the semiconductor device **10**, carrier concentration of the N− type substrate **1** is higher than the impurity concentration of the N− type substrate **1**, and the former is 10.sup.2 to 10.sup.5 times as high as the latter. Immediately after the switching of the semiconductor device **10**, namely immediately after the voltage applied to the semiconductor device **10** is changed from forward direction to reverse direction, the carrier concentration of the N− type substrate **1** remains high, and the carrier concentration of the N− type substrate **1** and the carrier concentration of the P type diffusion layer **3** are relatively close to each other. As a result, during the recovery operation after the switching of the semiconductor device **10**, the depletion layer around the border between the N− type substrate **1** and the P type diffusion layer **3** extends both toward the N− type substrate **1** and toward the P type diffusion layer **3**.

(70) If the current in the on-state is high, since the carrier concentration of the N− type substrate **1** during the recovery operation is high, and thus the extent of the depletion layer in the P type diffusion layer **3** is large. If the impurity concentration of the P type diffusion layer **3** is low, the extent of the depletion layer in the P type diffusion layer **3** is large. For the purpose of increasing the switching speed of the semiconductor device **10**, there are cases in which the impurity concentration of the P type diffusion layer **3** is set as low as the carrier concentration of the N− type substrate **1** in the on-state, for example.

(71) In such cases, the depletion layer spread easily in the P type diffusion layer **3**.

(72) <A-3-3. Timing in which the Depletion Layer is Largest in the P Type Diffusion Layer **3** in Recovery Operation>

(73) In recovery operation, if the voltage V.sub.ka between the anode electrode **4** and the cathode electrode **5** is high, the depletion layer is large. If the reverse current during the recovery operation is high, the electric charge density in the N− type substrate **1** is high, thus the depletion layer in the P type diffusion layer **3** is large. Therefore, when the voltage V.sub.ka and the reverse current is nearly highest during the recovery operation, the depletion layer in the P type diffusion layer **3** is largest and the semiconductor device **10** is more likely to be broken down due to the depletion of the P type diffusion layer **3**.

(74) FIGS. **10** to **12** show the time dependence of the voltage V.sub.ka and the current **1** during the recovery operation of the semiconductor devices **10** with different configurations in the scope described in <A. Embodiment 1>. In FIGS. **10** to **12**, the current **1** is defined to be positive when the current is forward current.

(75) As shown in FIGS. **10** to **12**, after the switching around time t=1 μs, absolute value of the current **1** take nearly maximum value around the time t.sub.1 at which V.sub.ka is equal to the power supply voltage V.sub.cc. Thus, it is approximately assumed that the depletion layer in the anode layer is largest when V.sub.ka is equal to the power supply voltage V.sub.cc.

(76) <A-3-4. Analysis of the Structural Factor of the Depletion of the P Type Diffusion Layer **3**>

(77) Based on the previous analysis, in the following, how the depletion layer in the P type diffusion layer **3** depends on the configuration of the semiconductor device **10** is analyzed. Based on the analysis in <A-3-3. Timing in which the Depletion Layer is Largest in the P Type Diffusion Layer **3** in Recovery Operation>, width W.sub.A of the depletion layer in the P type diffusion layer

3 in a state (hereafter referred to as the state S) in which the reverse voltage which is equal to V.sub.cc is applied to the PN junction part **6** during a recovery operation is considered.

(78) FIG. **13** shows the electric field distribution around the PN junction part **6**, which is the border between the N− type substrate **1** and the P type diffusion layer **3**, in the state S. For analyzing, the PN junction part **6** is modelized as an abrupt PN junction, namely, electric charge distribution around the PN junction part **6** change stepwise. Based on the Poisson's equation, the voltage V.sub.cc applied to the PN junction part **6** in the state S, the average impurity concentration N.sub.A in the P type diffusion layer **3**, the width W.sub.A of the depletion layer in the P type diffusion layer **3** in the state S, the electric charge density N′.sub.D in the depletion layer in the N− type substrate **1** in the state S, and the width W.sub.DD of the depletion layer in the N− type substrate **1** in the state S satisfy following relations shown in Formula 1 and Formula 2.

(79) $$V_{cc} = \frac{1}{2}\frac{qN_A}{\epsilon_s\epsilon_0}W_A^2 + \frac{1}{2}\frac{qN_D'}{\epsilon_s\epsilon_0}W_{DD}^2 \quad <\text{Formula1}> \qquad \frac{qN_A}{\epsilon_s\epsilon_0}W_A = \frac{qN_D'}{\epsilon_s\epsilon_0}W_{DD} \quad <\text{Formula2}>$$

(80) Here, q is the elementary charge, ε.sub.s is relative permittivity of the semiconductor material of the P type diffusion layer **3** and the N− type substrate **1**, and ε.sub.0 is the vacuum permittivity. N.sub.A is average impurity concentration of the P type diffusion layer **3**. For the purpose of approximate modeling, unevenness of the P type impurity concentration of the P type diffusion layer **3** with respect to the position in the thickness direction is neglected, and the average impurity concentration N.sub.A is used.

(81) From Formula 2, Formula 1 leads to Formula 3.

(82) $$V_{cc} = \frac{1}{2}\frac{qN_A}{\epsilon_s\epsilon_0}W_A^2 + \frac{1}{2}\frac{qN_D'}{\epsilon_s\epsilon_0}\left(\frac{N_A W_A}{N_D}\right)^2 \quad <\text{Formula3}>$$

(83) From Formula 3, the width W.sub.A of the depletion layer in the P type diffusion layer **3** in the state S is obtained as Formula 6, through Formula 4 and Formula 5.

(84) $$V_{cc} = \frac{1}{2}\frac{qN_A}{\epsilon_s\epsilon_0}W_A^2 + \frac{1}{2}\frac{qN_A^2}{\epsilon_s\epsilon_0 N_0}W_A^2 \quad <\text{Formula4}>$$

$$\frac{2\epsilon_s\epsilon_0 V_{cc}}{qN_A} = W_A^2 + \frac{N_A}{N_D}W_A^2 \quad <\text{Formula5}> \qquad W_A = \sqrt{\frac{2\epsilon_s\epsilon_0 V_{cc}}{qN_A\left(1+\frac{N_A}{N_D}\right)}} \quad <\text{Formula6}>$$

(85) To avoid the full depletion of the P type diffusion layer **3**, it is necessary that the thickness W of the P type diffusion layer **3** is larger than the width W.sub.A of the depletion layer in the P type diffusion layer **3**. Thus, the thickness W of the P type diffusion layer **3** is preferably satisfies the condition of Formula 7.

(86) $$W > W_A = \sqrt{\frac{2\epsilon_s\epsilon_0 V_{cc}}{qN_A\left(1+\frac{N_A}{N_D}\right)}} \quad <\text{Formula7}>$$

(87) In the following, the condition of Formula 7 is transformed into the form which does not include the electric charge density N′.sub.D in the depletion layer in the N− type substrate **1** in the state S.

(88) To that end, at first, relation is considered between average carrier concentration n.sub.Avg in the N− type substrate **1** in on-states before switching, current density J in on-states before switching, and lifetime τ of the carrier whose conductivity type is same with the P type diffusion layer**3** (namely, the P type carrier) in the N− type substrate **1**, and the thickness W.sub.N− of the N− type substrate **1**.

(89) FIGS. **14** to **16** represent carrier concentrations in the N− type substrate **1** in on-states and recovery states of the semiconductor device **10**. In the on-states, since electron concentration and hole concentration are nearly the same, both of the electron concentration and the hole concentration are shown as carrier concentration by the same line in the figures.

(90) FIG. **14** shows data in the case where the current density in the on-state is low (lines **14**a, **14**b, and **14**c in FIG. **14**) and in the case where the current density in the on-state is high (lines **14**d, **14**e, and **14**f in FIG. **14**).

(91) FIG. **15** shows data in the case in which the carrier lifetime of the P type carrier in the N− type substrate **1** is short (lines **15a**, **15b**, and **15c** in FIG. **15**) and in the case in which the carrier lifetime of the P type carrier in the N− type substrate **1** is long (lines **15d**, **15e**, and **15f** in FIG. **15**).

(92) FIG. **16** shows data in the case in which the N− substrate **1** is thick (lines **16a**, **16b**, and **16c** in FIG. **16**) and in the case in which the N− substrate **1** is thin (lines **16d**, **16e**, and **16f** in FIG. **16**).

(93) In FIGS. **14** to **16**, lines **14a, 15a, 16a, 14d, 15d**, and **16d** represent the carrier concentrations in the on-states.

(94) In FIGS. **14** to **16**, lines **14b, 15b, 16b, 14e, 15e**, and **16e** represent hole concentrations during the recovery states.

(95) In FIGS. **14** to **16**, line **14c, 15c, 16c, 14f, 15f**, and **16f** represent the hole concentrations during the recovery states.

(96) In FIGS. **14** to **16**, horizontal axis X represents positions in thickness direction of the N− type substrate **1**. In FIGS. **14** and **15**, X=X.sub.0 represents the border between the N− type substrate **1** and the P type diffusion layer **3**, and X=X.sub.1 represents border between the N− type substrate **1** and the N type diffusion layer **2**. In FIG. **16**, X=X.sub.0 represents border between the N− type substrate **1** and the P type diffusion layer **3**, and X=X.sub.1 represents the border between the N− type substrate **1** and the N type diffusion layer **2** in the case in which the N− type substrate **1** is thick.

(97) In FIGS. **14** to **16**, each data of the recovery states is data in the moment when the voltage V.sub.ka between the anode electrode **4** and the cathode electrode **5** take the same certain value in the recovery state.

(98) From FIGS. **14** to **16**, following relations (a), (b), and (c) are derived.

(99) (a) The higher the current density J in the on-state is, the higher the carrier concentration in the N− type substrate **1** in the on-state is.

(100) (b) The longer the carrier lifetime c of the P type carrier in the N− type substrate **1** is, the higher the carrier concentration in the N− type substrate **1** in the on-state is.

(101) (c) The thinner the thickness W.sub.N− of the N− type substrate **1** is, the higher the carrier concentration in the N− type substrate **1** in the on-state is.

(102) Therefore, the average carrier concentration n.sub.Avg in the N− type substrate **1** in the on-state is approximately represented by using the current density J in the on-state, the carrier lifetime τ of the P type carrier in the N− type substrate **1**, and the thickness W.sub.N− of the N− type substrate **1**. Following relation in Formula 8 is known (e.g. refer to Baliga, B. Jayant, "Fundamentals of Power Semiconductor Devices", p.212, Springer, 2008).

(103) $n_{avg} = \dfrac{J\tau}{2qW_{N-}}$ < Formula8 >

(104) Next, we derive the relation between the electric charge density N′.sub.D in the depletion layer in the N− type substrate **1** in the state S and the average carrier concentration n.sub.Avg in the N− type substrate **1** in the on-state. The electric charge density N′.sub.D in the depletion layer in the N− type substrate **1** in the state S can be represented as sum of four elements as shown in Formula 9.

N′.sub.D=p−n+N.sub.D−R   <Formula 9>

(105) Here, p is the hole concentration in the N− type substrate **1** in the state S, n is the electron concentration in the N− type substrate **1** in the state S, and N.sub.D is the impurity concentration of the N− type substrate **1**. R represents contribution of electrons and holes to the electric charge density which are captured in deep levels in the N− type substrate **1** in the state S. R is obtained by subtracting the concentration of holes captured in the deep levels from the concentration of electrons captured in the deep levels. In a recombination in the deep levels, one electron and one hole recombinate. Nevertheless, during the process of recombinations, the number of electrons and holes trapped in the deep levels are different, thus the electrons and holes trapped in the deep levels contributes to electric charge as a whole.

(106) From FIGS. **14** to **16**, it can be seen that p>>N.sub.D and p>n. Thus, Formula 9 leads to Formula 10.

N'.sub.D $\approx p - n - R$ <Formula 10>

(107) From FIGS. **14** to **16**, it can be seen that the higher the average carrier concentration n.sub.Avg in the N− type substrate **1** in the on-state is, the higher the carrier concentration in the depletion layer in the N− type substrate **1** in the state S is. From FIGS. **14** to **16**, it can be also seen that the carrier concentration in the depletion layer in the N− type substrate **1** in the state S depends on the average carrier concentration n.sub.Avg in the N− type substrate **1** in the on-state.

(108) The contribution R to the electric charge density from electrons and holes which are captured in deep levels in the N− type substrate **1** depends on the carrier lifetime τ of the hole in the N− type substrate **1**. Thus, the relation between N′.sub.D and n.sub.Avg is approximately represented as Formula 11.

N'.sub.D $= \alpha(\tau)n$.sub.Avg   <Formula 11>

(109) Here, $\alpha(\tau)$ is factor of proportionality empirically obtained. From a fitting to simulation results, we obtained the expression in Formula 12.

(110) $\alpha(\tau) = \dfrac{4.15}{(\ln(2.85\tau + 1))^{4.77} + 225}$ < Formula12 >

(111) In the right hand side of Formula 12, τ represents the value when τ is represented in the unit of μs. FIG. **17** shows $\alpha(\tau)$ obtained by the simulations and Formula 12 obtained by the fitting. In FIG. **17**, $\alpha(\tau)$ obtained by the simulations are shown in open triangles, and Formula 12 is shown in by a solid line. Differences between Formula 12 and $\alpha(\tau)$ obtained by the simulations are within 5%. FIG. **17** also shows N′.sub.D and n.sub.Avg obtained by simulations.

(112) By using Formula 8 and Formula 12, Formula 7 leads to Formulae 13 to 15.

(113) $W > \sqrt{\dfrac{2\epsilon_s \epsilon_0 V_{cc}}{qN_A(1 + \frac{N_A}{\alpha(\tau)n_{avg}})}}$ < Formula13 > $W > \sqrt{\dfrac{2\epsilon_s \epsilon_0 V_{cc}}{qN_A(1 + \frac{N_A}{\alpha(\tau)\frac{J\tau}{2qW_{N-}}})}}$ < Formula14 >

$W > \sqrt{\dfrac{2\epsilon_s \epsilon_0 V_{cc}}{qN_A(1 + \frac{2qW_{N-} N_A}{\alpha(\tau)n_{avg}})}}$ < Formula15 >

(114) The average impurity concentration N.sub.A in the P type diffusion layer **3**, the dose amount D.sub.A, and the thickness W of the P type diffusion layer **3** satisfy the relation of Formula 16.

(115) $N_A = \dfrac{D_A}{W_D}$ < Formula16 >

(116) Therefore Formula 15 is rewritten as Formulae 17 to 20 by using Formula 16.

(117) $W > \sqrt{\dfrac{2\epsilon_s \epsilon_0 V_{cc}}{q\frac{D_A}{W}(1 + \frac{2qW_{N-} D_A}{\alpha(\tau)J\tau W})}}$ < Formula17 > $W^2 > \dfrac{2\epsilon_s \epsilon_0 V_{cc}}{q\frac{D_A}{W}(1 + \frac{2qW_{N-} D_A}{\alpha(\tau)J\tau W})}$ < Formula18 >

$W^2 \frac{1}{W}(1 + \dfrac{2qW_{N-} D_A}{\alpha(\tau)J\tau W}) > \dfrac{2\epsilon_s \epsilon_0 V_{cc}}{qD_A}$ < Formula19 >

$W + \dfrac{2qW_{N-} D_A}{\alpha(\tau)J\tau} > \dfrac{2\epsilon_s \epsilon_0 V_{cc}}{qD_A}$ < Formula20 >

(118) From the above argument, it is desirable that the thickness W of the P type diffusion layer **3** satisfies the relation of Formula 20 to suppress the full depletion of the P type diffusion layer **3** during the recovery operation.

(119) After the switching, V.sub.ka temporarily becomes higher than the power supply voltage V.sub.cc, as shown in FIGS. **10** to **12** for example. In order for V.sub.ka not to exceed rated voltage, the power supply voltage V.sub.cc when the semiconductor device **10** is used is set to be lower than the rated voltage V.sub.r. FIG. **18** shows a representative value of the power supply voltage V.sub.cc assumed for each of the rated voltages V.sub.r of the semiconductor devices **10**. For example, in the case where the thickness W of the P type diffusion layer **3** satisfies the condition obtained by substituting 0.8 times the rated voltages V.sub.r for the power supply voltage V.sub.cc in Formula 20, the full depletion of the P type diffusion layer **3** during the recovery operation of the semiconductor device **10** is suppressed when the power supply voltage V.sub.cc shown in FIG. **18**

is used. In the case where the thickness W of the P type diffusion layer **3** satisfies the condition obtained by substituting 0.9 times the rated voltages V.sub.r for the power supply voltage V.sub.cc in Formula 20, the full depletion of the P type diffusion layer **3** during the recovery operation of the semiconductor device **10** is further suppressed.

(120) Rated current density J.sub.r may be used as the current density J in the on-state. Since the full depletion of the P type diffusion layer **3** occur in the case when the current in the on-state just before the switching is high, a case where the current density J in the on-state just before the switching is higher than the rated current density J.sub.r may be taken into account, to secure a design margin. A representative value of the current density J assumed as a high current density in the on-state just before the switching is 2.5 times the rated current density J.sub.r, for example.

(121) FIG. **19** shows the rated current density J.sub.r which is representative value assumed and 2.5 times the rated current density J.sub.r, which is the representative value of the current density assumed as a high current density in the on-state just before the switching, for each of the rated voltages V.sub.r of the semiconductor devices **10**.

(122) By assuming 2.5 times the rated current density J.sub.r as the current density J in the on-state just before the switching, the full depletion of the P type diffusion layer **3** is suppressed in the case when a large current is flowing in the on-state just before the switching. By assuming 3 times the rated current density J.sub.r as the current density J in the on-state just before a switching, the full depletion of the P type diffusion layer **3** is further suppressed.

(123) In the case where the power supply voltage V.sub.cc is assumed as 0.8 times the rated voltage V.sub.r and the current density J in the on-state just before the switching is assumed as 2.5 times the rated current density J.sub.r, the thickness W of the P type diffusion layer **3** satisfies

(124) $0 \; W > \frac{1.6 \epsilon_s \epsilon_0 V_r}{q D_A} - \frac{2q W_{N-} D_A}{2.5 \alpha(\tau) J_r \tau}$ < Formula21 >

(125) Thereby, the full depletion of the P type diffusion layer **3** during the recovery operation of high current and high voltage in the semiconductor device **10** is suppressed.

(126) In the case where the power supply voltage V.sub.cc is assumed as 0.9 times the rated voltage V.sub.r and the current density J in the on-state just before the switching is assumed as 2.5 times the rated current density J.sub.r, the thickness W of the P type diffusion layer **3** satisfies

(127) $W > \frac{1.8 \epsilon_s \epsilon_0 V_r}{q D_A} - \frac{2q W_{N-} D_A}{2.5 \alpha(\tau) J_r \tau}$ < Formula22 >

(128) In the case where the power supply voltage V.sub.cc is assumed as 0.8 times the rated voltage V.sub.r and the current density J in the on-state just before the switching is assumed as 3 times the rated current density J.sub.r, the thickness W of the P type diffusion layer **3** satisfies

(129) $W > \frac{1.6 \epsilon_0 V_r}{q D_A} - \frac{2q W_{N-} D_A}{3 \alpha(\tau) J_r \tau}$ < Formula23 >

(130) In the case where the power supply voltage V.sub.cc is assumed as 0.9 times the rated voltage V.sub.r and the current density J in the on-state just before the switching is assumed as 3 times the rated current density J.sub.r, the thickness W of the P type diffusion layer **3** satisfies

(131) $W > \frac{1.8 \epsilon_s \epsilon_0 V_r}{q D_A} - \frac{2q W_{N-} D_A}{3 \alpha(\tau) J_r \tau}$ < Formula24 >

(132) The problem of the full depletion of the P type diffusion layer **3** during the recovery operation of high current and high voltage is more likely to occur in semiconductor devices for high-speed application (e.g. for electric trains), than in semiconductor devices for low-speed application (e.g. for electric power system). In the semiconductor device **10** having the configuration described in the current embodiment, even if it is for high-speed application, the full depletion of the P type diffusion layer **3** during the recovery operation of large current and large voltage can be suppressed, and breakdown of the semiconductor device **10** by the full depletion of the P type diffusion layer **3** is suppressed.

(133) The rated current density J.sub.r is obtained by dividing the rated current of the

semiconductor device **10** by the area of the active region, namely the region where the current flows, in the plan view. In the case where the semiconductor devices **10** is combined with a transistor as in the case of RC-IGBT, the rated current density J.sub.r is obtained by dividing the rated current of the forward direction of the diode by the area of the active region of the diode which includes the N− type substrate**1**, the N type diffusion layer **2**, and the P type diffusion layer **3**.

(134) FIG. **20** shows a representative value of the thickness W.sub.N− of the N− type substrate **1** for each of the rated voltages of the semiconductor devices **10**.

(135) For the purpose of lowering the switching loss of the semiconductor device **10**, it is desirable that the maximum value of the impurity concentration of the P type diffusion layer **3** is less than or equal to 1.0E17 cm.sup.−3. Accordingly, it is desirable that the dose amount D.sub.A of the P type diffusion layer **3** is determined so that the maximum value of the impurity concentration of the P type diffusion layer **3** is less than or equal to 1.0E17 cm.sup.−3.

(136) In the derivations of Formulae 21 to 24, it is assumed that the P type impurity concentration in P type diffusion layer **3** is constant with respect to the thickness direction. Accordingly, it is desirable that the impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction is not too different from the assumption. Namely, it is desirable that the minimum value of the P type impurity concentration in the P type diffusion layer **3***b* is larger than or equal to the 1/10 times the maximum value of the impurity concentration of the P type diffusion layer **3***a*, and is larger than or equal to the 1/10 times the maximum value of the impurity concentration of the P type diffusion layer **3***c*. The same holds for the case where impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction has more than two peaks. Namely, in the region of the P type diffusion layer **3** which locates between the peak closest to the first main surface **100***a* and the peak closest to the second main surface **100***b* among the peaks of the impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction, it is desirable that the minimum value of the impurity concentration of the region is larger than 1/10 times of the maximum value of the impurity concentration distribution in the P type diffusion layer **3** with respect to the thickness direction.

(137) <A-4. Manufacturing Method>

(138) FIG. **23** is a flowchart showing a manufacturing method of the semiconductor device **10**.

(139) FIGS. **7** and **8** show a state in a process of the manufacturing of the semiconductor device **10**.

(140) First, in step S**1**, the N− type substrate **1** is prepared.

(141) Next, in step S**2**, first ion implantation is performed into the surface layer of the first main surface **100***a* side of the N− type substrate **1** (see FIG. **7**). As a result, impurity-introduced region **30** is formed in the N− type substrate **1**. The ions implanted into the N− type substrate **1** in step S**2** are boron, for example.

(142) Next, in step S**3**, second ion implantation is performed into the surface layer of the first main surface **100***a* side of the N− type substrate **1** (see FIG. **8**). As a result, impurity-introduced region **31** is formed in the N− type substrate **1**. In step S**3**, ions are implanted into the region which is shallower than the region into which ions are implanted in the ion implantation in step S**2**. The ions implanted into the N− type substrate **1** in step S**3** are boron, for example.

(143) Next, in step S**4**, by heat treatment, the impurities implanted in step S**2** and step S**3** are activated. As a result, the P type diffusion layer **3** is formed (see FIG. **1**).

(144) Next, in step S**5**, anode electrode **4** is formed.

(145) Next, in step S**6**, N type diffusion layer **2** is formed by ion implantation and heat treatment.

(146) Next, in step S**7**, cathode electrode **5** is formed.

(147) Through the processes described above, semiconductor device **10** shown in FIG. **1** is obtained.

(148) In the manufacturing method of the semiconductor device of the present embodiment, the thickness W of the P type diffusion layer **3** is decided to satisfy Formula 21. In step S**2** and step S**3**,

for example, by adjusting energy of ion beam, the depth of the ion implantation can be adjusted and the thickness W of the P type diffusion layer **3** can be adjusted.

(149) By adjusting the amount of the ions implanted in step S**2** and step S**3**, impurity concentration at the peak of the impurity concentration distribution of the P type diffusion layer **3** can be adjusted.

(150) As described above, in the manufacturing method of the semiconductor device of the present embodiment, the relation between the average carrier concentration n.sub.Avg in the N− type substrate **1** in the on-state and electric charge concentration in the depletion layer around the border of the N− type substrate **1** and the P type diffusion layer **3** among the N− type substrate **1** in the recovery process is obtained, and then the thickness of the P type diffusion layer **3** is decided based on the relation.

B. Second Embodiment

(151) FIG. **2** shows a semiconductor device **10**b of the second embodiment.

(152) In the semiconductor device **10**b, the impurity concentration of the P type diffusion layer **3**a varies depending on in-plane position. With respect to other aspects, the semiconductor device **10**b is the same with the semiconductor device **10** of the embodiment 1.

(153) In the semiconductor device **10**b, the P type diffusion layer **3**a includes P type diffusion layers **3**a**1** and P type diffusion layers **3**a**2**. The P type impurity concentration of the P type diffusion layers **3**a**1** is higher than the P type impurity concentration of the P type diffusion layers **3**a**2**. The P type impurity concentration of the P type diffusion layers **3**a**2** is higher than the P type impurity concentration of the P type diffusion layer **3**b. The maximum value of the impurity concentration of the P type diffusion layers **3**a**2** is less than or equal to 1.0 E 17 cm.sup.−3.

(154) The P type diffusion layers **3**al and the P type diffusion layers **3**a**2** are disposed alternately in one of in-plane directions as shown in FIG. **2**, for example. The P type diffusion layers **3**al and the P type diffusion layers **3**a**2** are disposed alternately in the one of in-plane directions with a constant cycle, for example. The P type diffusion layers **3**a**1** and the P type diffusion layers **3**a**2** may extend in a direction intersecting the one of in-plane directions. The P type diffusion layers **3**a**1** and the P type diffusion layers **3**a**2** may also be disposed alternatively in the direction intersecting the one of in-plane directions.

(155) The same holds for the case where impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction has more than two peaks. The impurity concentration at the peak closest to the first main surface **100**a, the peak among the peaks of the impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction, varies depending on in-plane position. The P type impurity concentration at the peak closest to the first main surface **100**a, the peak among the peaks of the impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction, are disposed alternately in the one of in-plane directions, for example. The P type impurity concentration at the peak closest to the first main surface **100**a, the peak among the peaks of the impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction, are disposed alternately in the one of in-plane directions with a constant cycle, for example.

(156) The impurity concentration of the P type diffusion layer **3**a varies depending on in-plane position, thus the resistance of the P type diffusion layer **3**a and the anode electrode **4** is suppressed, and flow of holes from P type diffusion layer **3** into the N− type substrate **1** is suppressed. The recovery loss can be lowered by the suppression of the flow of holes into the N− type substrate **1**.

(157) As explained in <Comparative Example> above, if the impurity concentration of the P type diffusion layer **3**z**1** of the semiconductor device **10**z**1** or the impurity concentration of the P type diffusion layer **3**z**2** of the semiconductor device **10**z**2** varies depending on the in-plane position, full depletion of the P type diffusion layer **3**z**1** or the P type diffusion layer **3**z**2** may occur in the position where the impurity concentration is low, and the semiconductor devices may be broken

down. In the present embodiment, the full depletion of the P type diffusion layer **3** during the recovery operation of high current and high voltage is suppressed and the breakdown of the semiconductor device by the full depletion is suppressed, because the P type impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction has plurality of peaks, and the impurity concentration at the peak closest to the first main surface **100***a* varies depending on the in-plane direction.

(158) The P type impurity concentration distribution of the P type diffusion layer **3** with respect to the thickness direction has plurality of peaks, thus the in-plane gradient of the impurity concentration in the P type diffusion layer **3***a* is mitigated in the portion of P type diffusion layer **3***a* on the N− type substrate **1** side, and the breakdown of the semiconductor device **10***b* by the dynamic avalanche is suppressed.

(159) While the disclosure has been shown and described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications and variations can be devised.

Claims

1. A semiconductor device comprising: a semiconductor base body having a first main surface and a second main surface; a first electrode; and a second electrode, wherein the semiconductor base body includes: a first semiconductor layer of a first conductivity type provided on the second main surface side of the semiconductor base body; a second semiconductor layer of the first conductivity type having a first conductivity type impurity concentration lower than that of the first semiconductor layer and provided closer to the first main surface than the first semiconductor layer is; and a third semiconductor layer of a second conductivity type provided closer to the first main surface than the second semiconductor layer is, wherein the first semiconductor layer is electrically connected to the second electrode in the second main surface, wherein the third semiconductor layer is electrically connected to the first electrode in the first main surface, wherein an impurity concentration distribution of the third semiconductor layer with respect to thickness direction of the semiconductor base body has a plurality of peaks, wherein a thickness W of the third semiconductor layer, a thickness W.sub.N− of the second semiconductor layer, elementary charge q, a relative permittivity ε.sub.s of a semiconductor material of the semiconductor base body, vacuum permittivity ε.sub.0, a rated voltages V.sub.r, a rated current density J.sub.r, a carrier lifetime τ of a second conductivity type carrier in the second semiconductor layer, a dose amount D.sub.A of the third semiconductor layer, an average carrier concentration n.sub.Avg, an electric charge density N′.sub.D, and α(τ) which is given as Formula 2 below and which represents a relation between an average carrier concentration of the second semiconductor layer in on-state of the semiconductor device and an electric charge concentration in a depletion layer around a border of the second semiconductor layer and the third semiconductor layer among the second semiconductor layer in recovery process of the semiconductor device, wherein α(τ) is a factor of proportionality represented by Formula 1 below, satisfy Formula 3 below

$$N'_D = \alpha(\tau) n_{Avg} \quad < \text{Formula1} > \qquad \alpha(\tau) = \frac{4.15}{(\ln(2.58\tau + 1))^{4.77} + 225} \quad < \text{Formula2} >$$

$$W > \frac{1.6\epsilon_s \epsilon_0 V_r}{q D_A} - \frac{2q W_{N\sim} D_A}{2.5\alpha(\tau) J_r \tau} . \quad < \text{Formula3} >$$

2. The semiconductor device according to claim 1, wherein the thickness W of the third semiconductor layer, the thickness W.sub.N− of the second semiconductor layer, the elementary charge q, the relative permittivity ε.sub.s of the semiconductor material, the vacuum permittivity ε.sub.0, the rated voltages V.sub.r, the rated current density J.sub.r, the carrier lifetime τ of the second conductivity type carrier in the second semiconductor layer, the dose amount D.sub.A of the third semiconductor layer, and the α(τ) satisfy Formula 4 below

$$W > \frac{1.8\epsilon_s\epsilon_0 V_r}{qD_A} - \frac{2qW_{N\sim}D_A}{2.5\alpha(\tau)J_r\tau}.$$ < Formula4 >

3. The semiconductor device according to claim 1, wherein the thickness W of the third semiconductor layer, the thickness W.sub.N− of the second semiconductor layer, the elementary charge q, the relative permittivity ε.sub.s of the semiconductor material, the vacuum permittivity ε.sub.0, the rated voltages V.sub.r, the rated current density J.sub.r, the carrier lifetime τ of the second conductivity type carrier in the second semiconductor layer, the dose amount D.sub.A of the third semiconductor layer, and the α(τ) satisfy Formula 4 below

$$W > \frac{1.6\epsilon_0 V_r}{qD_A} - \frac{2qW_{N-}D_A}{3\alpha(\tau)J_r\tau}.$$ < Formula4 >

4. The semiconductor device according to claim 1, wherein the thickness W of the third semiconductor layer, the thickness W.sub.N− of the second semiconductor layer, the elementary charge q, the relative permittivity ε.sub.s of the semiconductor material, the vacuum permittivity ε.sub.0, the rated voltages V.sub.r, the rated current density J.sub.r, the carrier lifetime τ of the second conductivity type carrier in the second semiconductor layer, the dose amount D.sub.A of the third semiconductor layer, and the α(τ) satisfy Formula 4 below

$$W > \frac{1.8\epsilon_s\epsilon_0 V_r}{qD_A} - \frac{2qW_{N\sim}D_A}{3\alpha(\tau)J_r\tau}.$$ < Formula4 >

5. The semiconductor device according to claim 1, wherein a minimum value of a second conductivity type impurity concentration in a region of the third semiconductor layer between a peak closest to the first main surface of the plurality of peaks of the impurity concentration distribution and a peak closest to the second main surface of the plurality of peaks of the impurity concentration distribution is higher than a first conductivity type impurity concentration of the second semiconductor layer.

6. The semiconductor device according to claim 1, wherein a maximum value of the impurity concentration distribution of the third semiconductor layer is less than or equal to 1.0E17 cm.sup.−3.

7. The semiconductor device according to claim 1, wherein a maximum value of the impurity concentration distribution of the third semiconductor layer is less than or equal to 2.5E16 cm.sup.−3.

8. The semiconductor device according to claim 1, wherein a minimum value of a second conductivity type impurity concentration in a region of the third semiconductor layer between a peak closest to the first main surface of the plurality of peaks of the impurity concentration distribution and a peak closest to the second main surface of the plurality of peaks of the impurity concentration distribution is larger than or equal to 1/10 times a maximum value of the impurity concentration distribution of the third semiconductor layer.

9. The semiconductor device according to claim 1, wherein an impurity concentration in the third semiconductor layer is highest at a peak closest to the second main surface of the plurality of peaks of the impurity concentration distribution of the third semiconductor layer.

10. The semiconductor device according to claim 1, wherein in the third semiconductor layer, an impurity concentration in a peak closest to the first main surface of the plurality of peaks of the impurity concentration distribution varies depending on in-plane position.

11. The semiconductor device according to claim 10, wherein in the third semiconductor layer, in the peak closest to the first main surface of the plurality of peaks of the impurity concentration distribution, regions with relatively high impurity concentration and regions with relatively low impurity concentration are disposed alternatively in one of in-plane directions.

12. A method of manufacturing a semiconductor device, comprising: forming a semiconductor base body having a first main surface and a second main surface; forming a first electrode; and forming a second electrode, wherein the semiconductor base body includes: a first semiconductor layer of a first conductivity type provided on the second main surface side of the semiconductor base body; a second semiconductor layer of the first conductivity type having a first conductivity type impurity

concentration lower than that of the first semiconductor layer and provided closer to the first main surface than the first semiconductor layer is; and a third semiconductor layer of a second conductivity type provided closer to the first main surface than the second semiconductor layer is, wherein the first semiconductor layer is electrically connected to the second electrode in the second main surface, wherein the third semiconductor layer is electrically connected to the first electrode in the first main surface, wherein an impurity concentration distribution of the third semiconductor layer with respect to thickness direction of the semiconductor base body has a plurality of peaks, wherein a thickness W of the third semiconductor layer, a thickness W.sub.N− of the second semiconductor layer, elementary charge q, a relative permittivity ε.sub.s of a semiconductor material of the semiconductor base body, vacuum permittivity ε0, a rated voltages V.sub.r, a rated current density J.sub.r, a carrier lifetime τ of a second conductivity type carrier in the second semiconductor layer, a dose amount D.sub.A of the third semiconductor layer, an average carrier concentration n.sub.Avg, an electric charge density N′.sub.D, and α(τ) which is given as Formula 2 below and which is a factor of proportionality between an average carrier concentration of the second semiconductor layer in on-state of the semiconductor device and an electric charge concentration in a depletion layer around a border of the second semiconductor layer and the third semiconductor layer among the second semiconductor layer in recovery process of the semiconductor device, wherein α(τ) is a factor of proportionality represented by Formula 1 below, satisfy Formula 3 below

$$N'_D = \alpha(\tau)n_{Avg} \quad < \text{Formula1} >$$

$$\alpha(\tau) = \frac{4.15}{(\ln(2.58\tau + 1))^{4.77} + 225} \quad < \text{Formula2} > \qquad W > \frac{1.6\epsilon_s \epsilon_0 V_r}{qD_A} - \frac{2qW_{N\sim} D_A}{2.5\alpha(\tau)J_r \tau} . \quad < \text{Formula3} >$$