US 20250259693A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2025/0259693 A1**

LEE (43) **Pub. Date: Aug. 14, 2025**

(54) **MEMORY SYSTEM INCLUDING A SUB-CONTROLLER AND OPERATING METHOD OF THE SUB-CONTROLLER**

(71) Applicant: **SK hynix Inc.**, Gyeonggi-do (KR)

(72) Inventor: **Jong Joo LEE**, Gyeonggi-do (KR)

(21) Appl. No.: **19/192,354**

(22) Filed: **Apr. 29, 2025**

Related U.S. Application Data

(60) Continuation of application No. 18/438,732, filed on Feb. 12, 2024, which is a division of application No. 17/529,970, filed on Nov. 18, 2021, now Pat. No. 11,901,027.

(30) **Foreign Application Priority Data**

Jun. 7, 2021 (KR) 10-2021-0073738

Publication Classification

(51) **Int. Cl.**

G11C 29/42	(2006.01)
G11C 8/18	(2006.01)
G11C 29/12	(2006.01)

(52) **U.S. Cl.**

CPC ***G11C 29/42*** (2013.01); ***G11C 8/18*** (2013.01); ***G11C 29/1201*** (2013.01); ***G11C 29/12015*** (2013.01)

(57) **ABSTRACT**

There are provided a memory system and an operating method of the memory system. The memory system includes: a main controller for transmitting main data having N bits through a main channel, where N is a positive integer; memory devices for storing sub-data constituting the main data, and transmitting the sub-data through sub-channels; and a sub-controller for communicating with the main controller through the main channel, and communicating with the memory devices through the sub-channels. The sub-controller generates the sub-data each having n bits where n is a positive integer less than N, by dividing the main data, generates sub-data strobe clocks by decreasing a frequency of a main data strobe clock synchronized with the main data, and transmits/receives the sub-data to/from the memory devices in synchronization with the sub-data strobe clocks.

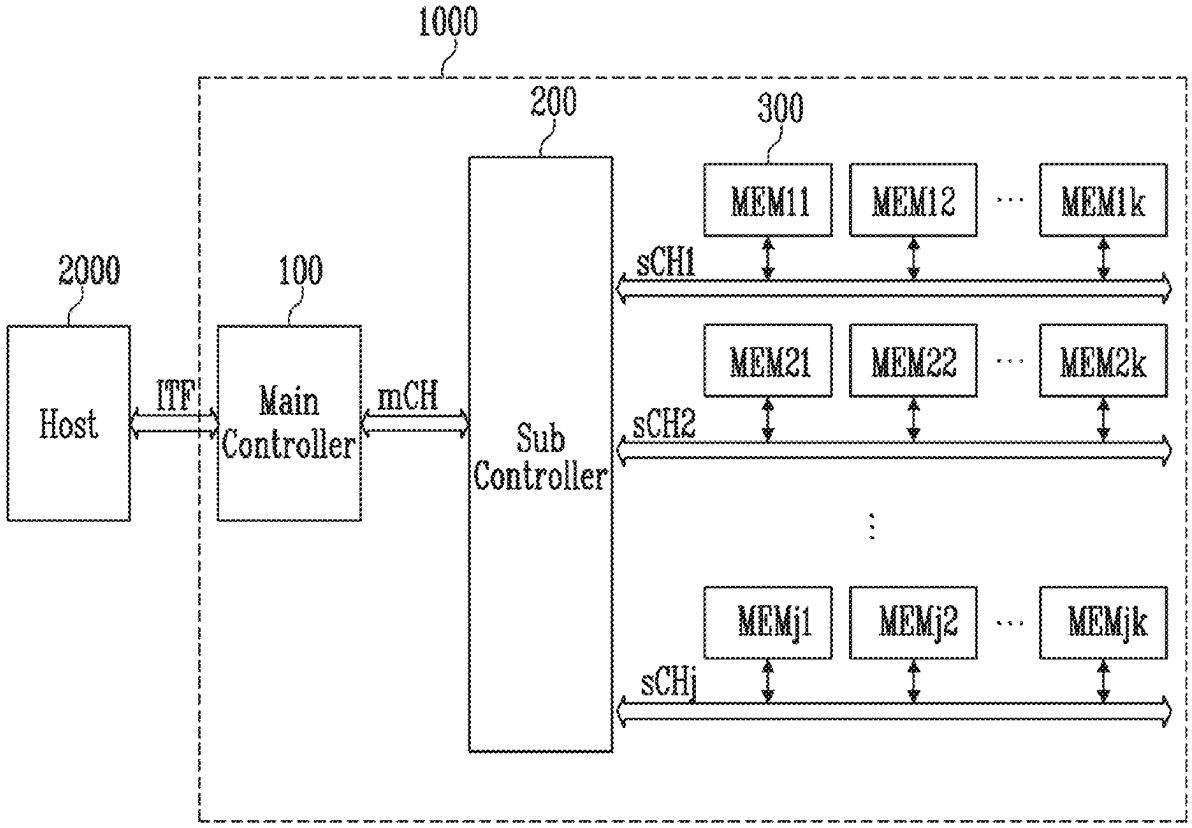


FIG. 1

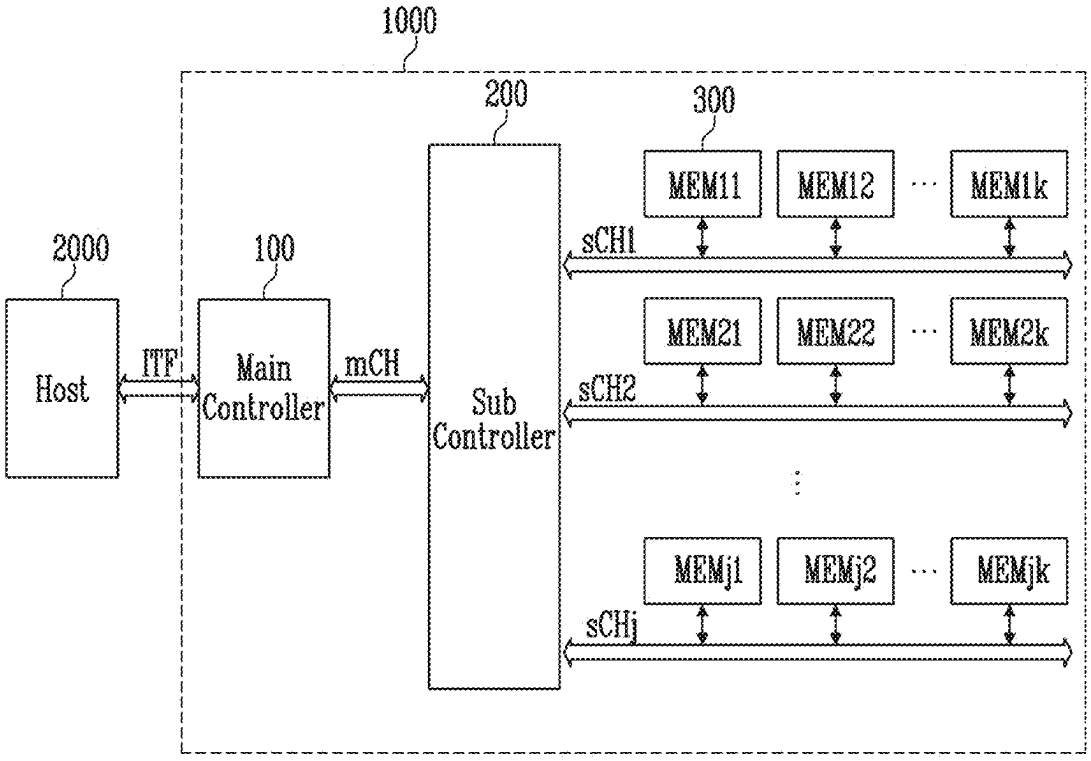

1000
200
300
2000
100
Host
ITF
Main Controller
mCH
Sub Controller
MEM11
MEM12
MEM1k
sCH1
MEM21
MEM22
MEM2k
sCH2
MEMj1
MEMj2
MEMjk
sCHj

FIG. 2

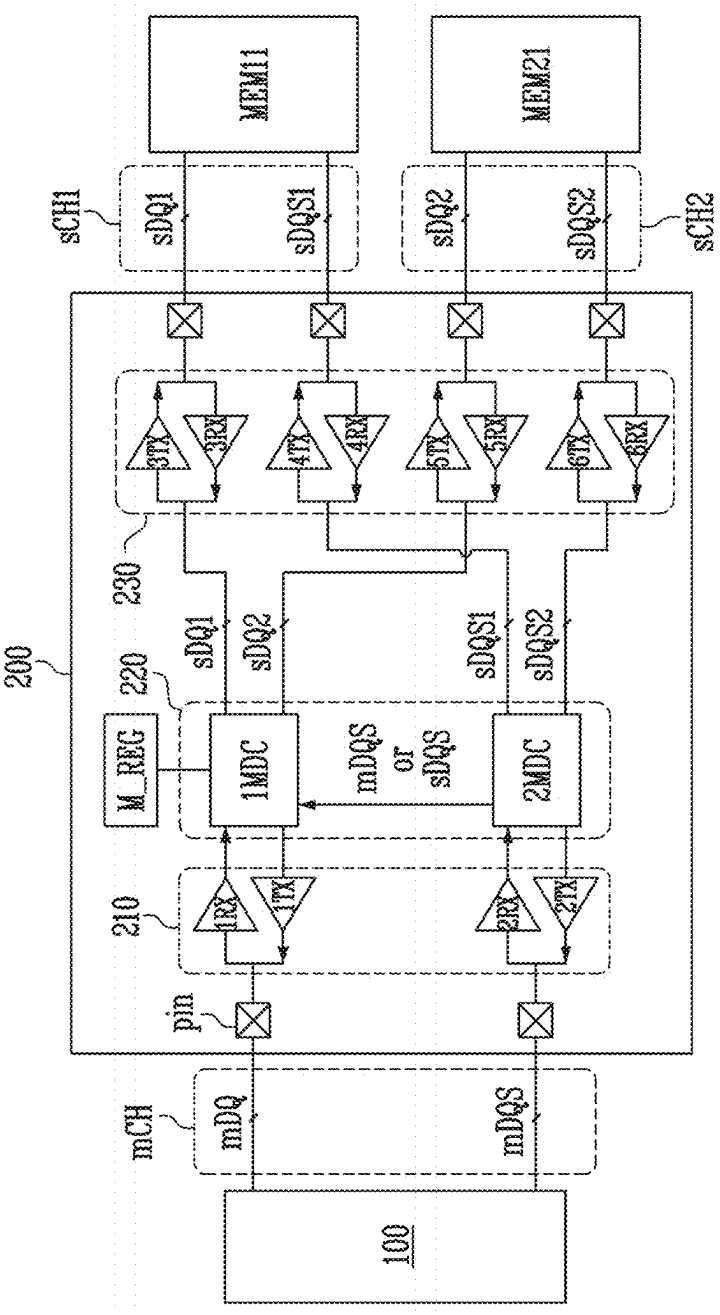

MEM11
MEM21
sCH1
sDQ1
sDQS1
sDQ2
sDQS2
sCH2
3TX
3RX
4TX
4RX
5TX
5RX
6TX
6RX
230
200
220
M_REG
1MDC
mDQS
or
sDQS
2MDC
210
1RX
1TX
2RX
2TX
pin
mCH
mDQ
mDQS
100

FIG. 3

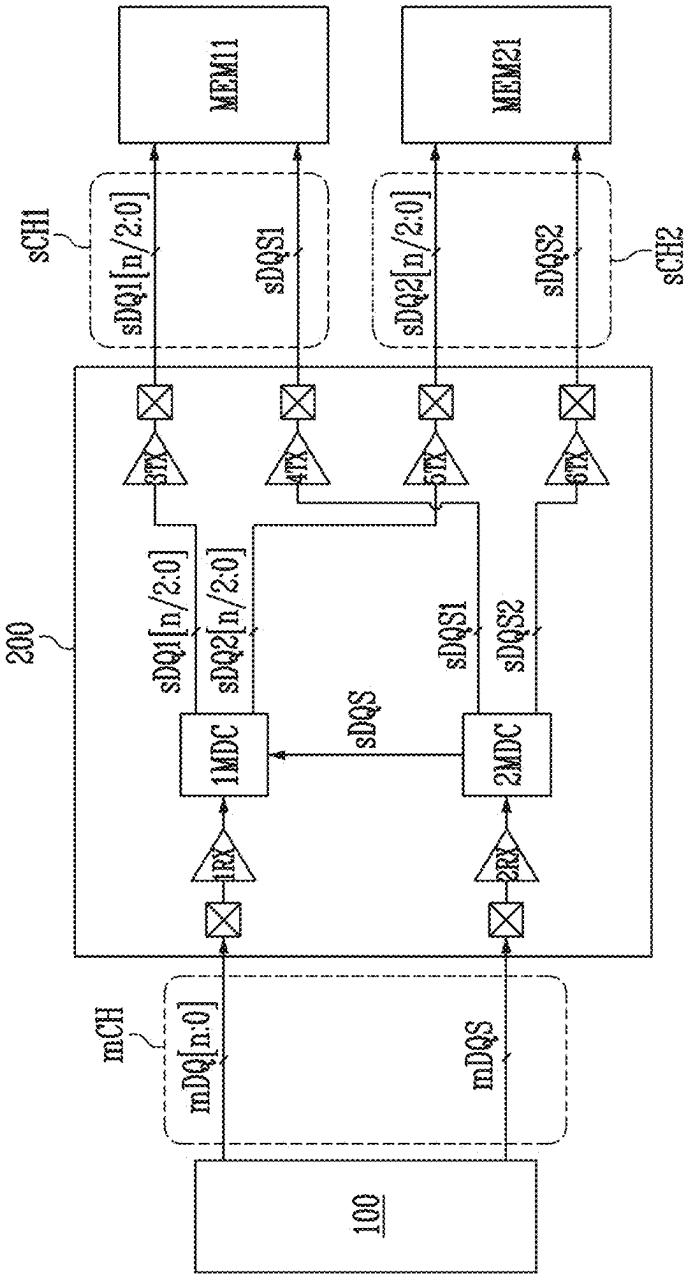

MEM11
MEM21
sCH1
sDQ1[n/2:0]
sDQS1
sDQ2[n/2:0]
sDQS2
sCH2
3TX
4TX
5TX
6TX
200
sDQ1[n/2:0]
sDQ2[n/2:0]
sDQS1
sDQS2
sDQS
1MDC
2MDC
1RX
2RX
mCH
mDQ[n:0]
mDQS
100

FIG. 4

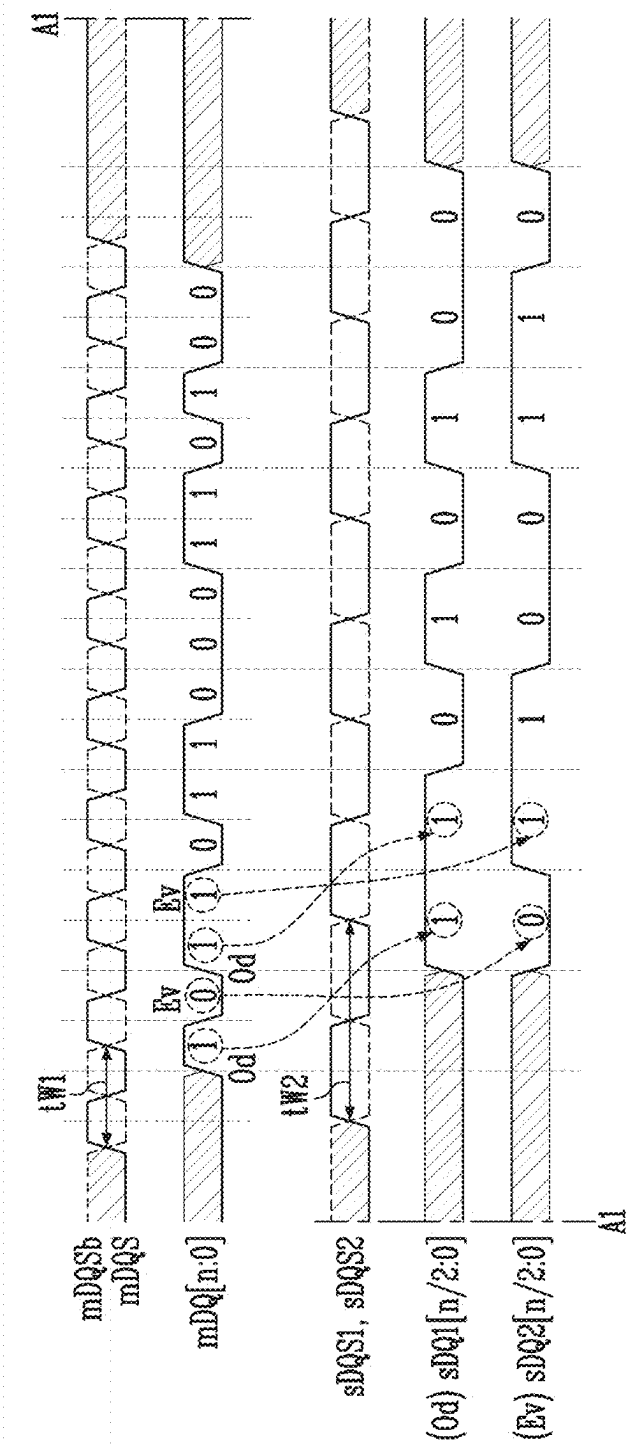

A1
tW1
tW2
Ev
Od
mDQSb
mDQS
mDQ[n:0]
sDQS1, sDQS2
(Od) sDQ1[n/2:0]
(Ev) sDQ2[n/2:0]
A1

FIG. 5

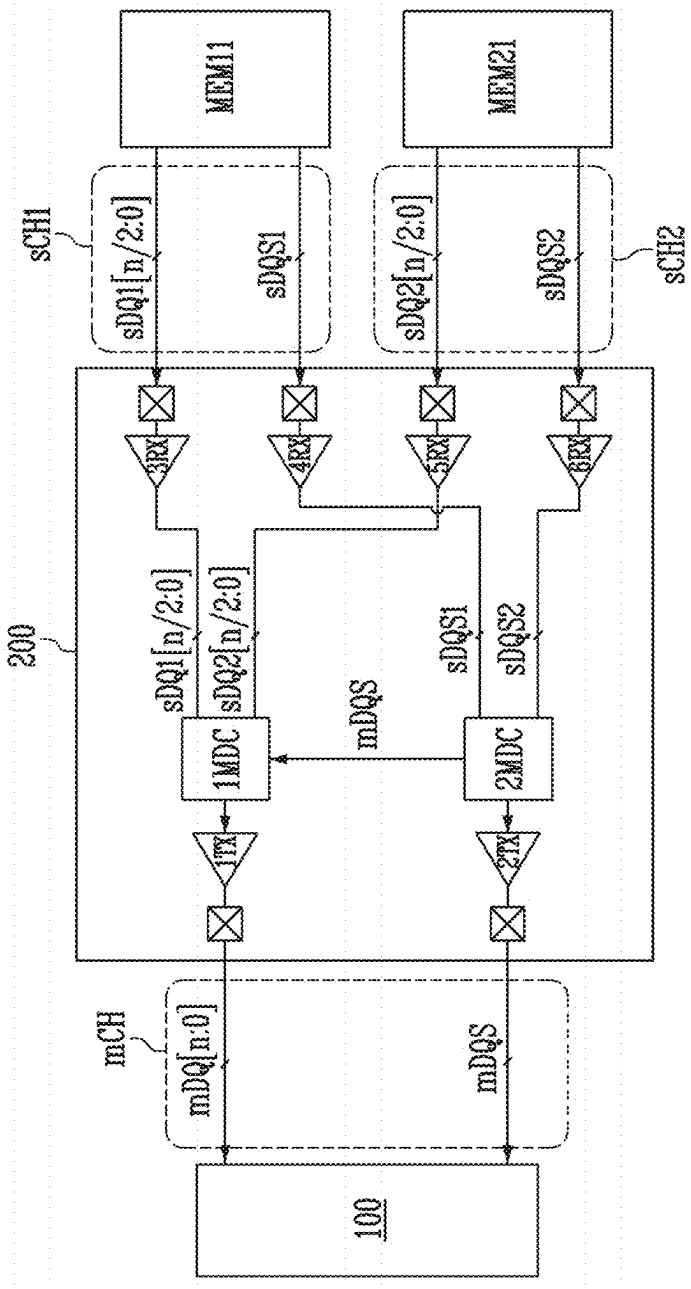

MEM11
MEM21
sCH1
sDQ1[n/2:0]
sDQS1
sDQ2[n/2:0]
sDQS2
sCH2
3RX
4RX
5RX
6RX
200
sDQ1[n/2:0]
sDQ2[n/2:0]
sDQS1
sDQS2
mDQS
1MDC
2MDC
1TX
2TX
mCH
mDQ[n:0]
mDQS
100

FIG. 6

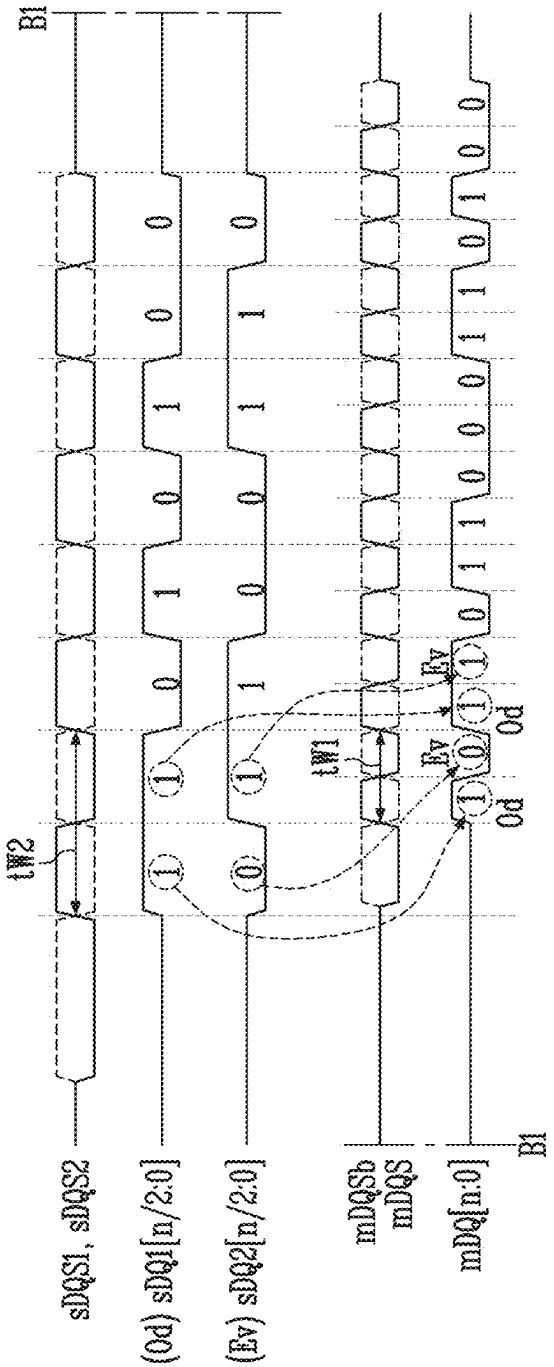

B1
tW2
tW1
Ev
Od
sDQS1, sDQS2
(Od) sDQ1[n/2:0]
(Ev) sDQ2[n/2:0]
mDQSb
mDQS
mDQ[n:0]
B1

FIG. 7

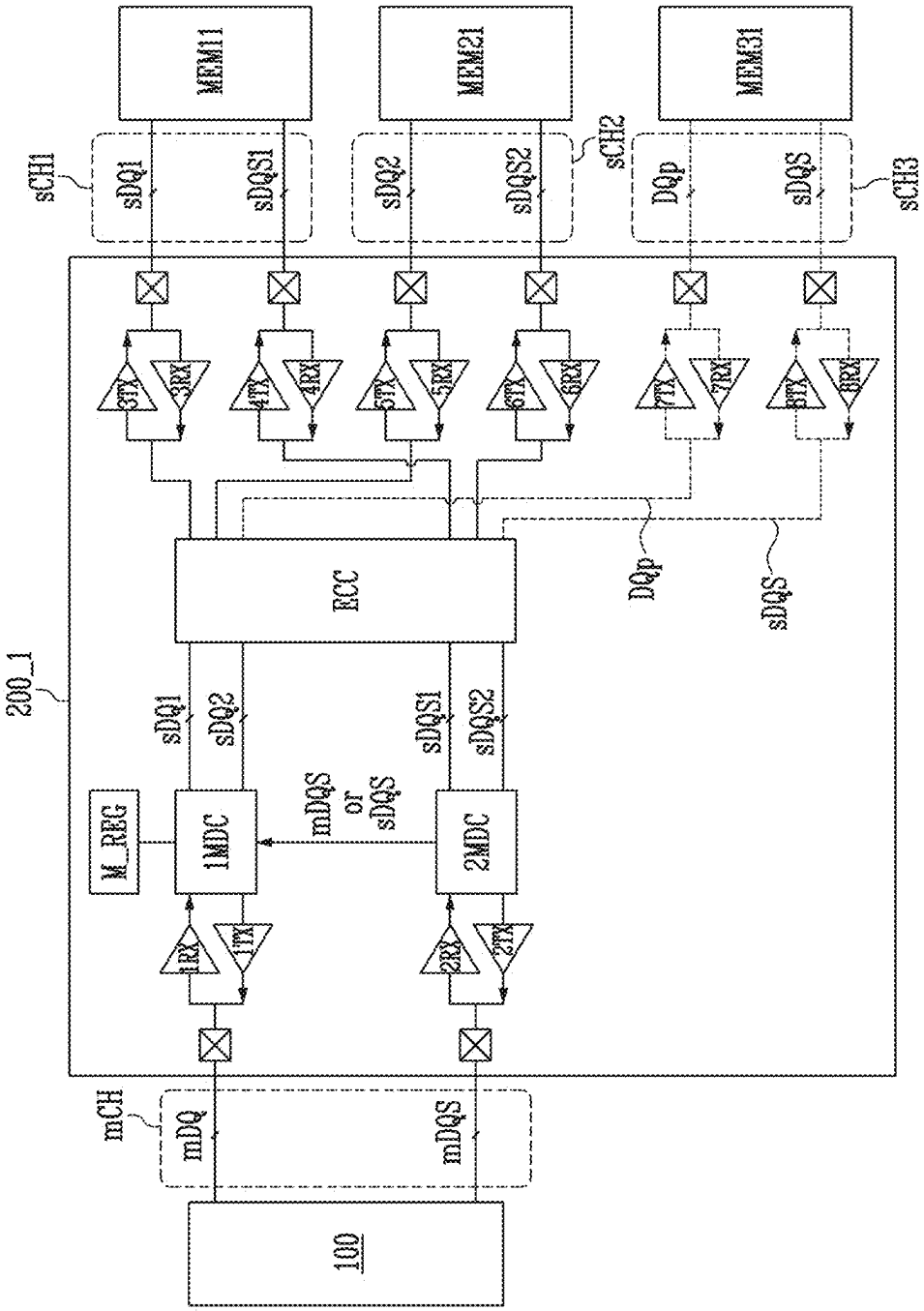

MEM11
MEM21
MEM31
sCH1
sDQ1
sDQS1
sDQ2
sDQS2
sCH2
DQp
sDQS
sCH3
3TX
3RX
4TX
4RX
5TX
5RX
6TX
6RX
7TX
7RX
8TX
8RX
ECC
DQp
sDQS
200_1
sDQ1
sDQ2
sDQS1
sDQS2
M_REG
1MDC
mDQS
or
sDQS
2MDC
1RX
1TX
2RX
2TX
mCH
mDQ
mDQS
100

FIG. 8

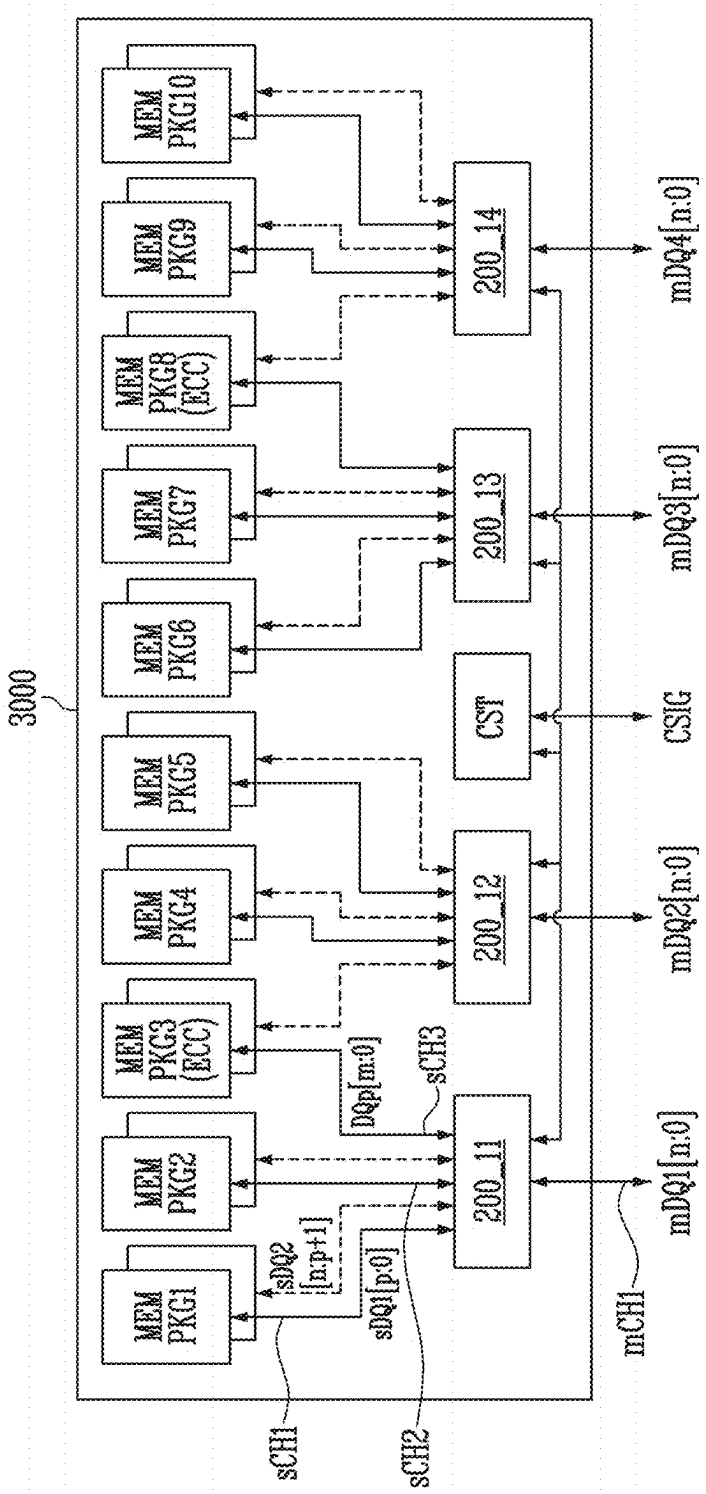

3000
MEM PKG1
MEM PKG2
MEM PKG3 (ECC)
MEM PKG4
MEM PKG5
MEM PKG6
MEM PKG7
MEM PKG8 (ECC)
MEM PKG9
MEM PKG10
200_11
200_12
CST
200_13
200_14
sDQ2 [n:p+1]
sDQ1[p:0]
DQp[m:0]
sCH3
sCH1
sCH2
mCH1
mDQ1[n:0]
mDQ2[n:0]
CSIG
mDQ3[n:0]
mDQ4[n:0]

FIG. 9

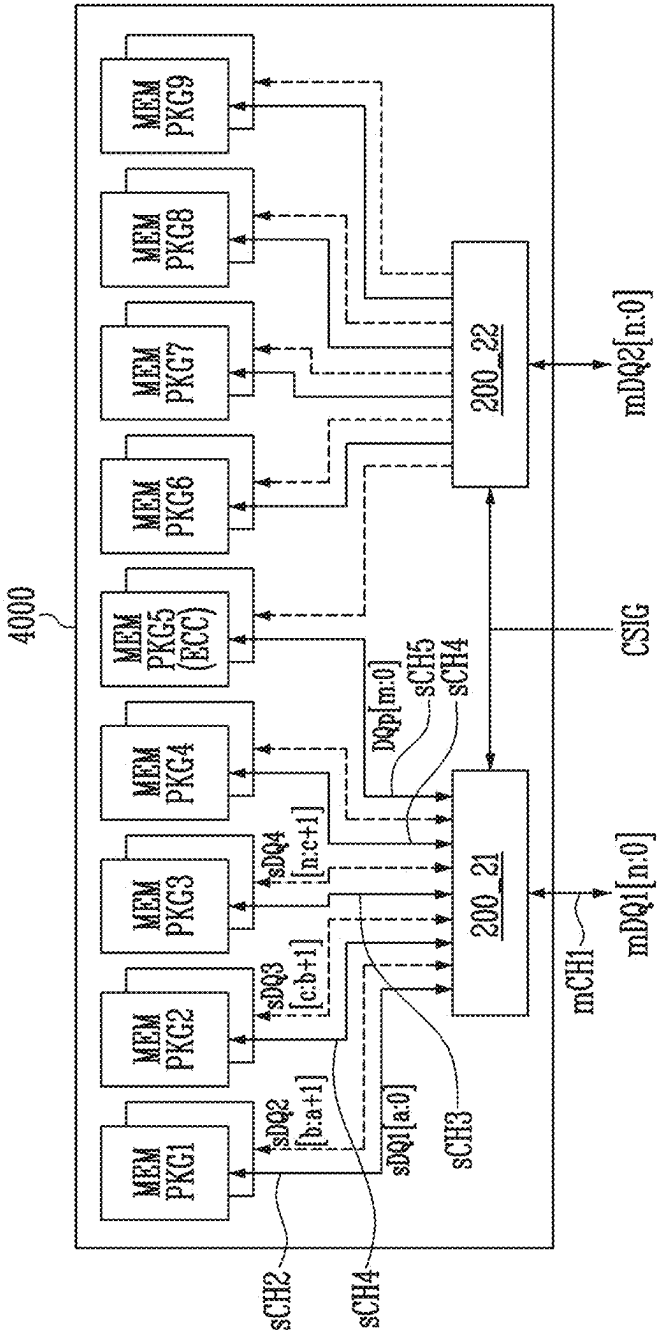

4000
MEM PKG1
MEM PKG2
MEM PKG3
MEM PKG4
MEM PKG5 (ECC)
MEM PKG6
MEM PKG7
MEM PKG8
MEM PKG9
200_21
200_22
CSIG
mCH1
mDQ1[n:0]
mDQ2[n:0]
sCH2
sCH4
sCH3
sCH5
sCH4
sDQ1[a:0]
sDQ2 [b:a+1]
sDQ3 [c:b+1]
sDQ4 [n:c+1]
DQp[m:0]

FIG. 10

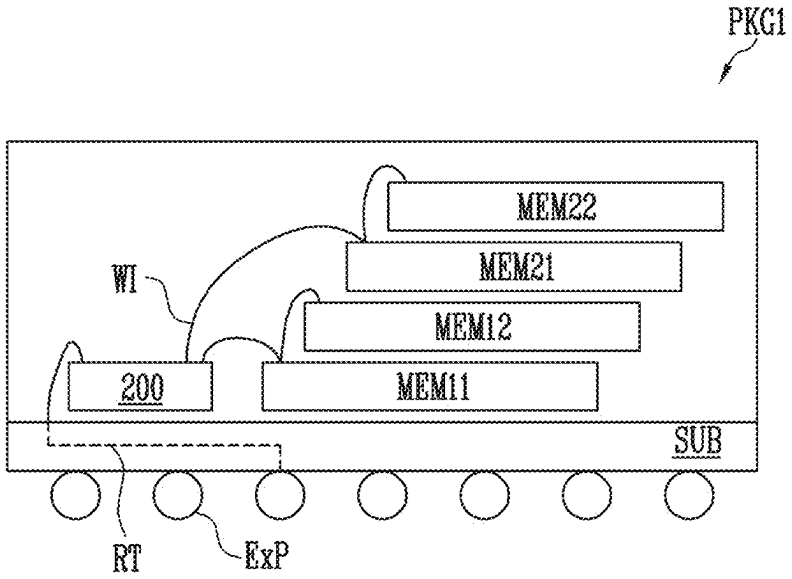


FIG. 11

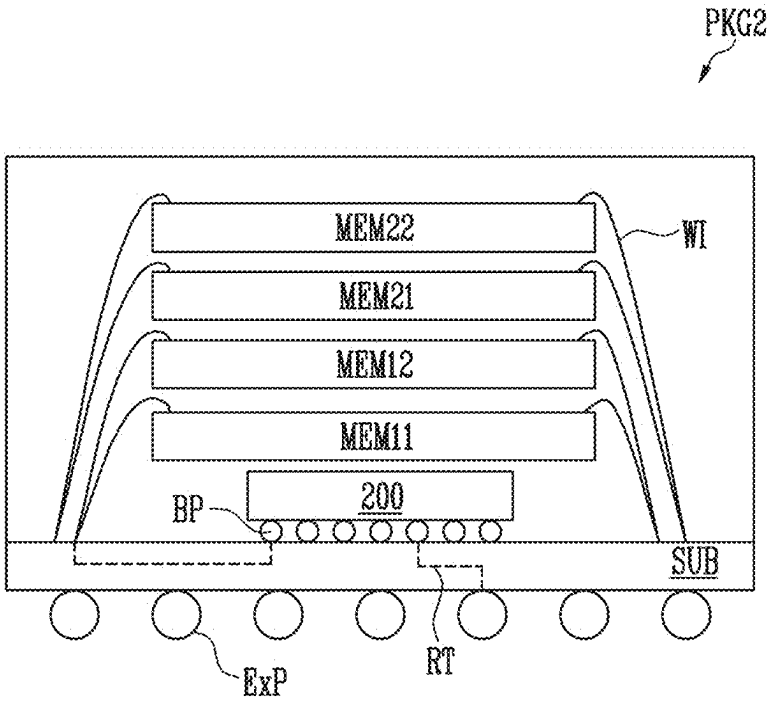


FIG. 12

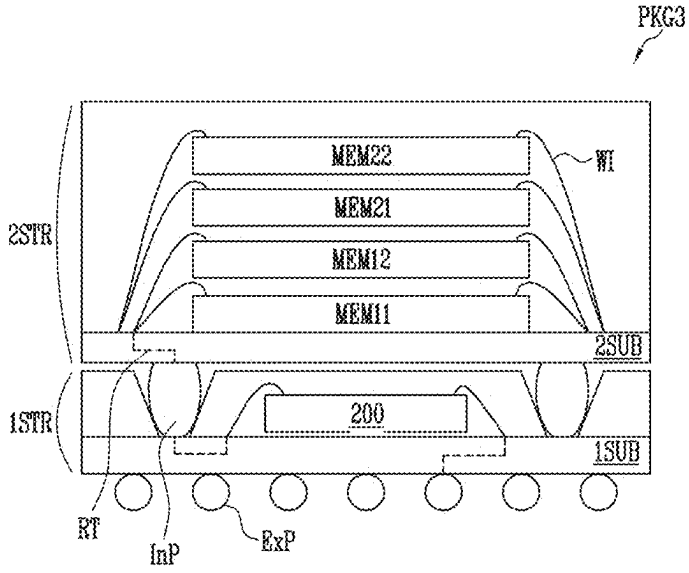
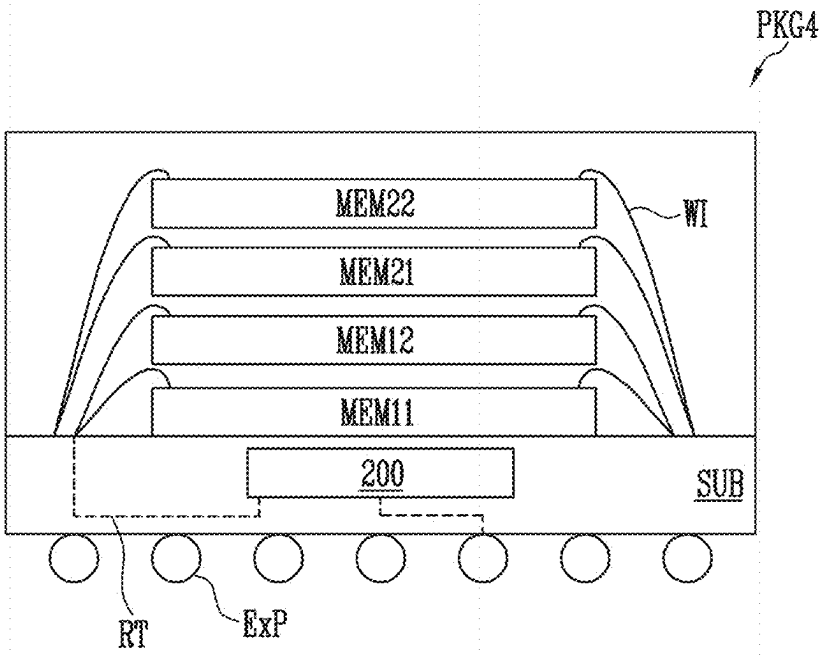

PKG3
MEM22
MEM21
MEM12
MEM11
WI
2STR
2SUB
1STR
200
1SUB
RT
InP
ExP

FIG. 13



MEMORY SYSTEM INCLUDING A SUB-CONTROLLER AND OPERATING METHOD OF THE SUB-CONTROLLER

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation of U.S. patent application Ser. No. 18/438,732 filed on Feb. 12, 2024, which is a division of U.S. patent application Ser. No. 17/529,970 filed on Nov. 18, 2021 and issued as U.S. Pat. No. 11,901,027 on Feb. 13, 2024, which claims priority under 35 U.S.C. § 119(a) to Korean patent application number 10-2021-0073738, filed on Jun. 7, 2021, and which is incorporated herein by reference in its entirety.

BACKGROUND

Field of Invention

[0002] The present disclosure generally relates to a memory system including a sub-controller and an operating method of the sub-controller, and more particularly, to a memory system including a main controller and a sub-controller, and an operating method of the memory system.

Description of Related Art

[0003] A memory system is widely used to store data in various electronic devices such as computers, wireless communication devices, cameras, and digital displays. Data may be programmed in a plurality of memory cells included in the memory system, and be read from programmed memory cells.

[0004] A memory device in which data is stored in the memory system may be divided into various devices according to the structure and operating method thereof. For example, the memory device may include a magnetic hard disk, a Random Access Memory (RAM), a Read Only Memory (ROM), a Dynamic RAM (DRAM), a Synchronous Dynamic RAM (SDRAM), a Ferromagnetic RAM (Fe-RAM), a Magnetic RAM (MRAM), a Resistive RAM (RRAM), a flash memory, a Phase Change Memory (PCM), and the like. A nonvolatile memory such as a flash memory and a PCM may retain data even when the supply of external power is interrupted. In volatile memory devices such as a DRAM, data disappears when the supply of external power is interrupted. Therefore, a periodic refresh operation is required.

[0005] The amount of data processed in electronic devices is gradually increasing as the use of electronic devices increases. Therefore, a memory system including a plurality of memory devices has been used.

[0006] However, when a plurality of memory devices are simultaneously used, signal distortion may occur, and therefore, the processing speed of data may be lowered due to the signal distortion.

SUMMARY

[0007] Embodiments of the present disclosure provide a memory system capable of processing large-capacity data at high speed without signal distortion.

[0008] In accordance with an aspect of the present disclosure, there is provided a memory system including: a main controller configured to transmit main data having N bits through a main channel, where N is a positive integer; memory devices configured to store sub-data constituting the main data, and transmit the sub-data through sub-channels; and a sub-controller configured to communicate with the main controller through the main channel, and communicate with the memory devices through the sub-channels, wherein the sub-controller generates the sub-data each having n bits, where n is a positive integer less than N by dividing the main data, generates sub-data strobe clocks by decreasing a frequency of a main data strobe clock synchronized with the main data, and transmits/receives the sub-data to/from the memory devices in synchronization with the sub-data strobe clocks.

[0009] In accordance with another aspect of the present disclosure, there is provided a method for operating a sub-controller, the method including: receiving main data in synchronization with a main data strobe clock; generating a sub-data strobe clock by decreasing a frequency of the main data strobe clock; dividing the main data to generate sub-data; and outputting the sub-data in synchronization with the sub-data strobe clock.

[0010] In accordance with still another aspect of the present disclosure, there is provided a method for operating a sub-controller, the method including: receiving sub-data in synchronization with sub-data strobe clocks; generating a main data strobe clock having a frequency higher than that of the sub-data strobe clocks; generating main data by merging the sub-data; and outputting the main data in synchronization with the main data strobe clock.

[0011] In accordance with another aspect of the present disclosure, there is provided a system including: a master device configured to process a main data piece; J number of slave devices each configured to process a sub data piece; and an arbitrator device coupled to: exchange the main data piece with the master device at a main frequency through a main channel, exchange in parallel the J number of the sub data pieces with the slave devices at a sub frequency through respective sub channels, and perform conversion between the main data piece and the J number of the sub data pieces, wherein the main data piece is J times greater than the sub data piece, and wherein the main frequency is J times greater than the sub frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] Various embodiments of the present disclosure will now be described more fully hereinafter with reference to the accompanying drawings; however, the embodiments may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the embodiments to those skilled in the art.

[0013] In the drawing figures, dimensions may be exaggerated for clarity of illustration. It will be understood that when an element is referred to as being "between" two elements, it can be the only element between the two elements, or one or more intervening elements may also be present. Like reference numerals refer to like elements throughout.

[0014] FIG. **1** is a diagram illustrating a memory system in accordance with an embodiment of the present disclosure.

[0015] FIG. **2** is a diagram illustrating a sub-controller in accordance with an embodiment of the present disclosure.

[0016] FIG. **3** is a diagram illustrating a program operation using the sub-controller in accordance with an embodiment of the present disclosure.

[0017] FIG. **4** is a diagram illustrating data and clocks, which are modulated in the program operation in accordance with an embodiment of the present disclosure.

[0018] FIG. **5** is a diagram illustrating a read operation using the sub-controller in accordance with an embodiment of the present disclosure.

[0019] FIG. **6** is a diagram illustrating data and clocks, which are modulated in the read operation in accordance with an embodiment of the present disclosure.

[0020] FIG. **7** is a diagram illustrating a sub-controller in accordance with another embodiment of the present disclosure.

[0021] FIGS. **8** and **9** are diagrams illustrating memory systems in accordance with other embodiments of the present disclosure.

[0022] FIGS. **10** to **13** are diagrams illustrating a package including a sub-controller in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0023] The specific structural or functional description disclosed herein is merely illustrative for the purpose of describing embodiments according to the concept of the present disclosure. The embodiments according to the concept of the present disclosure can be implemented in various forms, and cannot be construed as limited to the embodiments set forth herein.

[0024] FIG. **1** is a diagram illustrating a memory system in accordance with an embodiment of the present disclosure.

[0025] Referring to FIG. **1**, the memory system **1000** may be configured to store data output from a host **2000** or output read data to the host **2000**.

[0026] The memory system **1000** may include a main controller **100**, a sub-controller **200**, and eleventh to jkth memory devices MEM**11** to MEMjk, where j and k are positive integers.

[0027] Each of the eleventh to jkth memory devices MEM**11** to MEMjk may be implemented with a Random Access Memory (RAM), a Read Only Memory (ROM), a Dynamic RAM (DRAM), a Synchronous Dynamic RAM (SDRAM), a Ferromagnetic RAM (FeRAM), a Magnetic RAM (MRAM), a Resistive RAM (RRAM), a flash memory, a Phase Change Memory (PCM), and the like, which can store data.

[0028] The main controller **100** may be configured to communicate with the host **2000** through an interface ITF and communicate with the sub-controller **200** through a main channel mCH. For example, in a program operation, the main controller **100** may receive at least one of a request, a logical address, and data, which are output from the host **2000**, through the interface ITF, convert the request into a command used in the memory system **1000**, and convert the logical address into a physical address. The main controller **100** may transmit at least one of the command, the physical address, and data to the sub-controller **200** through the main channel mCH.

[0029] The sub-controller **200** may be configured to communicate with the main controller **100** through the main channel mCH and communicate with the eleventh to jkth memory devices MEM**11** to MEMjk through first to jth sub-channels sCH**1** to sCHj. For example, the sub-controller **200** may divide main data received through the main channel mCH into a plurality of sub-data according to the number of the first to jth sub-channels sCH**1** to sCHj, and transmit sub-data to selected memory devices through the first to jth sub-channels sCH**1** to sCHj. That is, an amount of sub-data transmitted to the selected memory device is smaller than that of the main data received through the main channel mCH, and therefore, the sub-controller **200** may decrease a burst length and a transmission speed of data loaded to the first to jth sub-channels sCH**1** to sCHj as compared with those of data loaded to the main channel mCH. For example, in order to adjust a time when the main data is transmitted/received and a time when the sub-data is transmitted/received to be equal to each other, the sub-controller **200** may set a frequency of a data strobe clock when the sub-data is transmitted/received to be lower than that of the data strobe clock when the main data is transmitted/received. The sub-controller **200** may set a frequency of the data strobe clock to be in proportion to the number of the first to jth sub-channels sCH**1** to sCHj, when the sub-data is transmitted/received. For example, when the number of the memory devices (e.g., the memory devices MEM**11** to MEMj**1** illustrated in FIG. **1**) each coupled to a corresponding one of the first to jth sub-channels sCH**1** to sCHj is 'J' or the number of the first to jth sub-channels sCH**1** to sCHj is 'J', the main data piece may be J times greater than the sub data piece according to an embodiment. The main data may be divided into the J number of sub data pieces when modulating the main data to generate the sub data piece. The J number of sub data pieces may be merged into the main data when modulating the sub data pieces to generate the main data. Also, the main frequency may be J times greater than the sub frequency. The main frequency may be that of the main data strobe clock and the sub frequency may be that of the sub data strobe clock. The main data strobe clock may be utilized when the main data is transferred between the main controller **100** and the sub controller **200** through the main channel mCH. The sub data strobe clock may be utilized when the sub data piece is transferred between the sub controller **200** and each of the memory devices (e.g., the memory devices MEM**11** to MEMj**1**) through a corresponding one of the first to jth sub-channels sCH**1** to sCHj.

[0030] The host **2000** may be a main processor of various electronic devices such as a computer, a wireless communication device, a camera, and a digital display.

[0031] FIG. **2** is a diagram illustrating a sub-controller in accordance with an embodiment of the present disclosure.

[0032] Referring to FIG. **2**, the sub-controller **200** may be configured to communicate with the main controller **100** through the main channel mCH and communicate with memory devices MEM**11** and MEM**21** through sub-channels sCH**1** and sCH**2**. Although the sub-controller **200** shown in FIG. **2** is connected to an eleventh memory device MEM**11** through a first sub-channel sCH**1** and is connected to a twenty-first memory device MEM**2** through a second sub-channel sCH**2**, the number of sub-channels and memory devices, which are connected to the sub-controller **200**, are not limited to those of the sub-channels and the memory devices, which are shown in FIG. **2**.

[0033] The main channel mCH may include a plurality of lines configured to transmit main data mDQ and a main data strobe clock mDQS between the main controller **100** and the sub-controller **200**. For example, the main channel mCH may include data lines configured to transmit the main data

mDQ and clock lines configured to transmit the main data strobe clock mDQS. The data lines and the clock lines may be configured as lines physically different from each other. For example, the main data mDQ may be transmitted bit by bit in response to the main data strobe clock mDQS.

[0034] To improve the reliability of a data transmission operation, the sub-controller **200** may be configured to decrease signal distortion which may occur in the first and second sub-channels sCH**1** and sCH**2**. The sub-controller **200** may be configured such that a burst length of the first and second sub-channels sCH**1** and sCH**2** decreases as compared with that of the main channel mCH. For example, when the first and second sub-channels sCH**1** and sCH**2** are connected to the sub-controller **200**, the sub-controller **200** may divide an amount of data loaded to the main channel mCH by 2 which is the number of sub-channels, and communicate the divided data with the eleventh memory device MEM**11** and the twenty-first memory device MEM**21** respectively through the first sub-channel sCH**1** and the second sub-channel sCH**2**. That is, when N sub-channels are connected to the sub-controller **200**, where N is an integer greater than 1, and the burst length of the main channel mCH is 1, the burst length of each of the N sub-channels may be set to 1/N. In order to adjust the burst length as described above, the sub-controller **200** may be configured as follows.

[0035] The sub-controller **200** may include a main input/output circuit group **210**, a modulation circuit group **220**, and a sub-input/output circuit group **230**.

[0036] The main input/output circuit group **210** may be configured to input or output the main data mDQ and the main data strobe clock mDQS between the main channel mCH and the modulation circuit group **220**. For example, the main input/output circuit group **210** may include a first input driver **1**RX and a first output driver **1**TX, which are configured to input or output the main data mDQ, and a second input driver **2**RX and a second output driver **2**TX, which are configured to input or output the main data strobe clock mDQS. For example, the first input driver IRX and the first output driver **1**TX may be connected to the data lines which transmit the main data mDQ through a pin, and the second input driver **2**RX and the second output driver **2**TX may be connected to the clock lines which transmit the main data strobe clock mDQS through a pin. For example, the first input driver **1**RX may be configured to transmit the main data mDQ received through the pin to the modulation circuit group **220**, and the first output driver **1**TX may be configured to output the main data mDQ transmitted from the modulation circuit group **220** through the pin. For example, the second input driver **2**RX may be configured to transmit the main data strobe clock mDQS received through the pin to the modulation circuit group **220**, and the second output driver **2**TX may be configured to output the main data strobe clock mDQs transmitted from the modulation circuit group **220** through the pin.

[0037] The modulation circuit group **220** may be configured to modulate data and clocks. For example, the modulation circuit group **220** may include a first modulation circuit **1**MDC configured to modulate the data and a second modulation circuit **2**MDC configured to modulate the clocks.

[0038] The first modulation circuit **1**MDC may be configured to divide the main data mDQ into first and second sub-data sDQ**1** and sDQ**2** and then output the first and second sub-data sDQ**1** and sDQ**2**, or merge the first and second sub-data sDQ**1** and sDQ**2** into the main data mDQ and then output the main data mDQ. For example, the first modulation circuit **1**MDC may generate first sub-data sDQ**1** by grouping some of the main data mDQ transmitted from the first input driver **1**RX, generate second sub-data sDQ**2** by grouping the other of the main data mDQ, and output the first and second sub-data sDQ**1** and sDQ**2** respectively through output lines. The first modulation circuit **1**MDC may modulate a bit number of the first and second sub-data sDQ**1** and sDQ**2** according to a number of sub-channels connected to the sub-controller **200**. For example, the first modulation **1**MDC may store information on the number of sub-channels, and adjust a bit number of data included in each of the first and second sub-data sDQ**1** and sDQ**2** according to the information on the number of sub-channels.

[0039] The second modulation circuit **2**MDC may be configured to divide the main data strobe clock mDQS into first and second sub-data strobe clocks sDQS**1** and sDQS**2** and then output the first and second sub-data strobe clocks sDQS**1** and sDQS**2**, or merge the first and second sub-data strobe clocks sDQS**1** and sDQS**2** into the main data strobe clock mDQS and then output the main data strobe clock mDQS. For example, the second modulation circuit **2**MDC may generate the first and second sub-data strobe clocks sDQS**1** and sDQS**2** by decreasing a frequency of the main data strobe clock mDQS transmitted from the second input driver **2**RX, and output the first and second sub-data strobe clocks sDQS**1** and sDQS**2** respectively through output lines. The second modulation circuit **2**MDC may modulate a frequency of the first and second sub-data strobe clocks sDQS**1** and sDQS**2** according to the number of sub-channels connected to the sub-controller **200**. For example, the second modulation circuit **2**MDC may store information on the number of sub-channels, and adjust the frequency of the first and second sub-data strobe clocks sDQS**1** and sDQS**2** according to the information on the number of sub-channels. The second sub-data strobe clock sDQS**2** is output through an output line different from that of the first sub-data strobe clock sDQS**1**, but may be set to have the same frequency and the same output time as the first sub-data strobe clock sDQS**1**. That is, the first and second sub-data strobe clocks sDQS**1** and sDQS**2** may be the same.

[0040] The second modulation circuit **2**MDC may transmit the main strobe clock mDQS or a sub-data strobe clock sDQS to the first modulation circuit **1**MDC. The sub-data strobe clock sDQS may be the first or second sub-data strobe clock sDQS**1** or sDQS**2**.

[0041] A program operation will be described as an example. The second modulation circuit **2**MDC may generate the first and second sub-data strobe clocks sDQS**1** and sDQS**2** by modulating the frequency of the main data strobe clock mDQS, and transmit the first or second sub-data strobe clock sDQS**1** or sDQS**2** as the sub-data strobe clock sDQS to the first modulation circuit **1**MDC. The first modulation circuit **1**MDC may output the first or second sub-data sDQ**1** or sDQ**2** in response to the sub-data strobe clock sDQS.

[0042] A read operation will be described as an example. The second modulation circuit **2**MDC may generate the main data strobe clock mDQS by modulating the frequency of the first or second sub-data strobe clock sDQS**1** or sDQS**2**, and transmit the main data strobe clock mDQS to the first modulation circuit **1**MDC. The first modulation circuit **1**MDC may output the main data mDQ in response to the main data strobe clock mDQS.

[0043] The sub-input/output circuit group **230** may be configured to input or output the first and second sub-data sDQ**1** and sDQ**2** and the first and second sub-data strobe clocks sDQS**1** and sDQS**2** between the first and second sub-channels sCH**1** and sCH**2** and the modulation circuit group **220**. For example, the sub-input/output circuit group **230** may include third to sixth output drivers **3**TX to **6**TX and third to sixth input drivers **3**RX to **6**RX. The third output driver **3**TX may be configured to output the first sub-data sDQ**1** output from the first modulation circuit **1**MDC to the first sub-channel sCH**1** through a pin, and the third input driver **3**RX may be configured to transmit the first sub-data sDQ**1** input through the pin to the first modulation circuit IMDC.

[0044] The fourth output driver **4**TX may be configured to output the first sub-data strobe clock sDQS**1** output from the second modulation circuit **2**MDC to the first sub-channel sCH**1** through a pin, and the fourth input driver **4**RX may be configured to transmit the first sub-data strobe clock sDQS**1** input through the pin to the second modulation circuit **2**DMC.

[0045] The fifth output driver **5**TX may be configured to output the second sub-data sDQ**2** output from the first modulation circuit **1**MDC to the second sub-channel sCH**2** through a pin, and the fifth input driver **5**RX may be configured to transmit the second sub-data sDQ**2** input through the pin to the first modulation circuit **1**MDC.

[0046] The sixth output driver **6**TX may be configured to output the second sub-data strobe clock sDQS**2** output from the second modulation circuit **2**MDC to the second sub-channel sCH**2** through a pin, and the sixth input driver **6**RX may be configured to transmit the second sub-data strobe cock sDQS**2** input through the pin to the second modulation circuit **2**MDC.

[0047] The first sub-data sDQ**1** loaded to the first sub-channel sCH**1** may be transmitted to the eleventh memory device MEM**11** or the third input driver **3**RX in synchronization with the first sub-data strobe clock sDQS**1** loaded to the first sub-channel sCH**1**. Since the sub-channel is configured with two sub-channels corresponding to the first and second sub-channels sCH**1** and sCH**2**, the first sub-data sDQ**1** may be configured as data of N/2 bits, when the main data mDQ is configured as data of N bits. When the frequency of the main data strobe clock mDQS is M, where M is a positive rational number, the frequency of the first sub-data strobe clock sDQS**1** may be decreased as M/2.

[0048] The second sub-data sDQ**2** loaded to the second sub-channel sCH**2** may be transmitted to the twenty-first memory device MEM**21** or the fifth input driver **5**RX in synchronization with the second sub-data strobe clock sDQS**2** loaded to the second sub-channel sCH**2**. Since the sub-channel is configured with two sub-channels corresponding to the first and second sub-channels sCH**1** and sCH**2**, the second sub-data sDQ**2** may be configured as data of N/2 bits, when the main data mDQ is configured as data of N bits. When the frequency of the main data strobe clock mDQS is M, the frequency of the second sub-data strobe clock sDQS**2** may be decreased as M/2.

[0049] Since the first and second sub-data strobe clocks sDQS**1** and sDQS**2** have the same frequency and are simultaneously output from the fourth and sixth output drivers **4**TX and **6**TX, the first and second sub-data sDQ**1** and sDQ**2** may also be simultaneously transmitted to the eleventh and twenty-first memory devices MEM**11** and MEM**21** or the third and fifth input drivers **3**RX and **5**RX.

[0050] That is, a time required to transmit the first sub-data sDQ**1** through the first sub-channel sCH**1**, a time required to transmit the second sub-data sDQ**2** through the second sub-channel sCH**2**, and a time required to transmit the main data mDQ through the main channel mCH are the same.

[0051] Thus, the first and second sub-data sDQ**1** and sDQ**2** obtained by distributing the main data mDQ are transmitted through different first and second sub-channels sCH**1** and sCH**2** in synchronization with sub-data strobe clocks having a low frequency, and hence signal distortion which may occur in a process in which sub-data is transmitted through the first and second sub-channels sCH**1** and sCH**2** can be reduced. Accordingly, the reliability of a transmission operation in the memory system can be improved even when the amount of the main data mDQ increases.

[0052] In addition to the above-described components, the sub-controller **200** may include a mode register M_REG. Mode information of the eleventh and twenty-first memory devices MEM**11** and MEM**21** connected to the sub-controller **200** may be stored in the mode register M_REG. For example, the mode information may be information on whether the eleventh and twenty-first memory devices MEM**11** and MEM**21** are double data rate (DDR) memory devices, low power DDR (LPDDR) memory devices, LPDDR3 memory devices, or LPDDR4 memory devices. The mode register M_REG may be connected to the first modulation circuit **1**MDC, and the first modulation circuit **1**MDC may modulate data and clocks to be suitable for standards of a clock, a data transmission speed, a bandwidth, and a voltage according to the mode information stored in the mode register M_REG.

[0053] An operation of the above-described sub-controller **200** will be described as follows.

[0054] FIG. **3** is a diagram illustrating a program operation using the sub-controller in accordance with an embodiment of the present disclosure.

[0055] Referring to FIG. **3**, in the program operation, the sub-controller **200** may receive a main data strobe clock mDQS output from the main controller **100** through the main channel mCH, and output first and second sub-data strobe clocks sDQS**1** and sDQS**2** generated by modulating a frequency of the main data strobe clock mDQS through the first and second sub-channels sCH**1** and sCH**2**.

[0056] The sub-controller **200** may receive main data mDQ[*n*:0] where n is a positive integer, output from the main controller **100**, and transmit first and second sub-data sDQ**1**[*n*/2:0] and sDQ**2**[*n*/2:0] generated by modulating the main data mDQ[*n*:0] respectively to the eleventh and twenty-first memory devices MEM**11** and MEM**21** through the first and second sub-channels sCH**1** and sCH**2** in synchronization with the first and second sub-data strobe clocks sDQS**1** and sDQS**2**.

[0057] For example, when the main data strobe clock mDQS is input having a frequency of M where M is a positive integer, the second input driver **2**RX may transmit the input main data strobe clock mDQS to the second modulation circuit **2**MDC. The second modulation circuit **2**MDC may generate a plurality of sub-data strobe clocks having a frequency lower than M according to information on a number of sub-channels. A case where the number of sub-channels is 2 will be described as an example. The

second modulation circuit **2**MDC may generate a first sub-data strobe clock sDQS**1** and a second sub-data strobe clock sDQS**2**, which have a frequency of M/2 by dividing the frequency of the main data strobe clock mDQS by 2.

[0058] The second modulation circuit **2**MDC may transmit, to the first modulation circuit **1**MDC, a sub-data strobe clock sDQS having the same frequency as the first and second sub-data strobe clocks sDQS**1** and sDQS**2**.

[0059] The first modulation circuit **1**MDC may transmit the first sub-data sDQ**1**[*n*/2:0] to the third output driver **3**TX and transmit the second sub-data sDQ**2**[*n*/2:0] to the fifth output driver **5**TX, in response to the sub-data strobe clock sDQS.

[0060] The first sub-data strobe clock sDQS**1** generated in the second modulation circuit **2**MDC may be transmitted to the fourth output driver **4**TX, and the second sub-data strobe clock sDQS**2** may be transmitted to the sixth output driver **6**TX.

[0061] When the fourth output driver **4**TX outputs the first sub-data strobe clock sDQS**1** through the first sub-channel sCH**1**, the third output driver **3**TX may transmit the first sub-data sDQ**1**[*n*/2:0] to the eleventh memory device MEM**11** in synchronization with the first sub-data strobe clock sDQS**1**.

[0062] When the sixth output driver **6**TX outputs the second sub-data strobe clock sDQS**2** through the second sub-channel sCH**2**, the fifth output driver **5**TX may transmit the second sub-data sDQ**2**[*n*/2:0] to the twenty-first memory device MEM**21** in synchronization with the second sub-data strobe clock sDQS**2**.

[0063] The data and the clocks, which are described with reference to FIG. **3**, will be described in more detail as follows.

[0064] FIG. **4** is a diagram illustrating data and clocks, which are modulated in the program operation in accordance with an embodiment of the present disclosure.

[0065] Referring to FIGS. **3** and **4**, a time required in one cycle of the main data strobe clock mDQS is a first time tW**1**. Although a case where the main data strobe clock mDQS is input through the main channel mCH has been illustrated in FIG. **3**, a main data strobe inverted clock mDQSb may be simultaneously input with the main data strobe clock mDQS through another line of the main channel mCH.

[0066] The main data mDQ[*n*:0] may be input to the first modulation circuit **1**MDC in response to the main data strobe clock mDQS. For example, the main data mDQ[*n*:0] of 16 bits, i.e., '1011011000110100' may be sequentially input to the first modulation circuit **1**MDC in synchronization with the main data strobe clock mDQS.

[0067] When the main data mDQ[*n*:0] are all input to the first modulation circuit **1**MDC (A**1**), the second modulation circuit **2**MDC may output the first and second sub-data strobe clocks sDQS**1** and sDQS**2** having a frequency of M/2. A speed of the first and second sub-data strobe clocks sDQS**1** and sDQS**2** is slower by ½ than that of the main data strobe clock mDQS, and therefore, a time required in one cycle of the first and second sub-data strobe clocks sDQS**1** and sDQS**2** may be a second time tW**2** longer than the first time tW**1**. That is, a time required in two cycles of the main data strobe clock mDQS may be equal to that required in one cycle of the first and second sub-data strobe clocks sDQS**1** and sDQS**2**.

[0068] The first modulation circuit **1**MDC may generate the first sub-data sDQ**1**[*n*/2:0] by extracting odd-numbered bits Od from a plurality of bits included in the main data mDQ[*n*:0], and generate the second sub-data sDQ**2**[*n*/2:0] by extracting even-numbered bits Ev from the plurality of bits included in the main data mDQ[*n*:0]. That is, all of the bits of the main data mDQ[*n*:0] may be classified into first and second sub-data sDQ**1**[*n*/2:0] and sDQ**2**[*n*/2:0]. For example, the first sub-data sDQ**1**[*n*/2:0] may include '11010100' corresponding to the odd-numbered bits Od of the main data mDQ[*n*:0], and the second sub-data sDQ**2**[*n*/2:0] may include '01100110' corresponding to the even-numbered bits Ev of the main data mDQ[*n*:0]. That is, each of the first and second sub-data sDQ**1**[*n*/2:0] and sDQ**2**[*n*/2:0] may be configured with 8 bits.

[0069] The first sub-data sDQ**1**[*n*/2:0] may be transmitted to the eleventh memory device MEM**11** through the first sub-channel sCH in synchronization with the first sub-data strobe clock sDQS**1**, and the second sub-data sDQ**2**[*n*/2:0] may be transmitted to the twenty-first memory device MEM**21** through the second sub-channel sCH**2** in synchronization with the second sub-data strobe clock sDQS**2**.

[0070] FIG. **5** is a diagram illustrating a read operation using the sub-controller in accordance with an embodiment of the present disclosure.

[0071] Referring to FIG. **5**, in the read operation, the sub-controller **200** may receive first and second sub-data strobe clocks sDQS**1** and sDQS**2** output from the eleventh and twenty-first memory devices MEM**11** and MEM**21** through the first and second sub-channels sCH**1** and sCH**2**, and output, to the main controller **100**, a main data strobe clock mDQS generated by modulating the frequency of the first and second sub-data strobe clocks sDQS**1** and sDQS**2** through the main channel mCH.

[0072] The sub-controller **200** may receive first and second sub-data sDQ**1**[*n*/2:0] and sDQ**2**[*n*/2:0] output from the eleventh and twenty-first memory devices MEM**11** and MEM**21** through the first and second sub-channels sCH**1** and sCH**2**, generate main data mDQ[*n*:0] by merging the first and second sub-data sDQ**1**[*n*/2:0] and sDQ**2**[*n*/2:0], and output the main data mDQ[*n*:0] to the main controller **100** through the main channel mCH.

[0073] For example, when the first sub-data strobe clock sDQS**1** having a frequency of M/2 is input where M is a positive integer, the fourth input driver **4**RX may transmit the first sub-data strobe clock sDQS**1** to the second modulation circuit **2**MDC. When the second sub-data strobe clock sDQS**2** having a frequency of M/2 is input, the sixth input driver **6**RX may transmit the second sub-data strobe clock sDQS**2** to the second modulation circuit **2**MDC.

[0074] The second modulation circuit **2**MDC may generate the main data strobe clock mDQS having a frequency higher than M/2 according to information on a number of sub-channels. A case where the number of sub-channels is 2 will be described as an example. The second modulation circuit **2**MDC may generate the main data strobe clock mDQS having a frequency of M by multiplying M/2 as the frequency of the first and second sub-data strobe clocks sDQS**1** and sDQS**2** by 2.

[0075] The third input driver **3**RX may receive first sub-data sDQ**1**[*n*/2:0] output from the eleventh memory device MEM**11**, and transmit the received first sub-data sDQ**1**[*n*/2:0] to the first modulation circuit **1**MDC.

[0076] The fifth input driver **5**RX may receive second sub-data sDQ**2**[*n*/2:0] output from the twenty-first memory device MEM**21**, and transmit the received second sub-data sDQ**2**[*n*/2:0] to the first modulation circuit **1**MDC.

[0077] The first modulation circuit **1**MDC may generate the main data mDQ[*n*:0] by sequentially merging, bit by bit, the first and second sub-data sDQ**1**[*n*/2:0] and sDQ**2**[*n*/2:0], and output the main data mDQ[*n*:0] to the main channel mCH in synchronization with the main data strobe clock mDQS output from the second modulation circuit **2**MDC.

[0078] When the second modulation circuit **2**MDC outputs the main data strobe clock mDQS to the first modulation circuit **1**MDC, the second modulation circuit **2**MDC may also output the main data strobe clock mDQS to the main channel mCH. Therefore, the main data mDQ loaded to the main channel mCH may be input to the main controller **100** in synchronization with the main data strobe clock mDQS.

[0079] The data and the clocks, which are described with reference to FIG. **5**, will be described in more detail as follows.

[0080] FIG. **6** is a diagram illustrating data and clocks, which are modulated in the read operation in accordance with an embodiment of the present disclosure.

[0081] Referring to FIGS. **5** and **6**, a time required in one cycle of the first and second sub-data strobe clocks sDQS**1** and sDQS**2** is a second time tW**2**. The first and second sub-data sDQ**1**[*n*/2:0] and sDQ**2**[*n*/2:0] may be input to the first modulation circuit **1**MDC in response to the first and second sub-data strobe clocks sDQS**1** and sDQS**2**. For example, the first sub-data sDQ**1**[*n*/2:0] of 8 bits, i.e., '11010100' and the second sub-data sDQ**2**[*n*/2:0] of 8 bits, i.e., '01100110' may be sequentially input to the first modulation circuit **1**MDC in synchronization with the first and second sub-data strobe clocks sDQS**1** and sDQS**2**.

[0082] When both of the first and second sub-data sDQ**1**[*n*/2:0] and sDQ**2**[*n*/2:0] are input to the first modulation circuit **1**MDC (B**1**), the second modulation circuit **2**MDC may output the main data strobe clock mDQS having a frequency of M. A speed of the main data strobe clock mDQS is faster by two times than that of the first and second sub-data strobe clocks sDQS**1** and sDQS**2**, and therefore, a time required in one cycle of the main data strobe clock mDQS may be a first time tW**1** shorter than the second time tW**2**. That is, the time required in one cycle of the first and second sub-data strobe clocks sDQS**1** and sDQS**2** may be equal to that required in two cycles of the main data strobe clock mDQS.

[0083] The first modulation circuit **1**MDC may generate main data mDQ[*n*:0] by sequentially merging a plurality of bits included in the first and second sub-data sDQ**1**[*n*/2:0] and sDQ**2**[*n*/2:0]. That is, the main data mDQ may be generated as both the first and second sub-data sDQ**1**[*n*/2:0] and sDQ**2**[*n*/2:0] are merged. For example, the main data mDQ[*n*:0] configured with 16 bits, i.e., '1011011000110100' may be generated as the first and second sub-data sDQ**1**[*n*/2:0] and sDQ**2**[*n*/2:0], each of which is configured with 8 bits are merged.

[0084] The main data mDQ[*n*:0] may be transmitted to the main controller **100** through the main channel mCH in synchronization with the main data strobe clock mDQS.

[0085] FIG. **7** is a diagram illustrating a sub-controller in accordance with another embodiment of the present disclosure.

[0086] Referring to FIG. **7**, the sub-controller **200_1** may further include an error correction circuit ECC, seventh and eighth output drivers **7**TX and **8**TX, and seventh and eighth input drivers **7**RX and **8**RX.

[0087] The error correction circuit ECC may generate parity data DQp about the first and second sub-data sDQ**1** and sDQ**2** in a program operation, and detect and correct an error of the first and second sub-data sDQ**1** and sDQ**2** by using the parity data DQp.

[0088] Various methods using a hamming code, a low density parity check (LDPC), or the like may be performed as a method for generating parity data DQp and detecting and correcting an error of data, using the parity data DQp. In addition, various methods for error correction have been published, and therefore, a detailed description of a method for generating parity data DQp and using the parity data DQp will be omitted in this embodiment.

[0089] In the program operation, the error correction circuit ECC may receive first and second sub-data sDQ**1** and sDQ**2** from the first modulation circuit **1**MDC, and generate parity data DQp about the received first and second sub-data sDQ**1** and sDQ**2**. When the parity data DQp is generated, the error correction circuit ECC may transmit the first sub-data sDQ**1** to the third output driver **3**TX, transmit the second sub-data sDQ**2** to the fifth output driver **5**TX, and transmit the parity data DQp to the seventh output driver **7**TX. The error correction circuit ECC may receive first and second sub-data strobe clocks sDQS**1** and sDQS**2** from the second modulation circuit **2**MDC, transmit the first sub-data strobe clock sDQS**1** to the fourth output driver **4**TX, transmit the second sub-data strobe clock sDQS**2** to the sixth output driver **6**TX, and transmit a sub-data strobe clock sDQS to the eighth output driver **8**TX. The sub-data strobe clock sDQS may be the first or second sub-data strobe clock sDQS**1** or sDQS**2**.

[0090] The parity data DQp may be transmitted to a thirty-first memory device MEM**31** connected to a third sub-channel sCH**3**, which is different from the eleventh and twenty-first memory devices MEM**11** and MEM**21**. For example, the seventh output driver **7**TX may transmit the parity data DQp to the thirty-first memory device MEM**31** through the third sub-channel sCH**3**, and the eighth output driver **8**TX may transmit the sub-data strobe clock sDQS to the thirty-first memory device MEM**31** through the third sub-channel sCH**3**.

[0091] In the above-described embodiments, information on a number of sub-channels is stored in the first and second modulation circuits **1**MDC and **2**MDC, and a bit number of the first and second sub-data sDQ**1** and sDQ**2** and a frequency of the first and second sub-data strobe clocks sDQS**1** and sDQS**2** are determined according to the information on the number of sub-channels. However, the third sub-channel sCH**3** connected to the thirty-first memory device MEM**31** for storing the parity data DQp is not included in the information on the number of sub-channels.

[0092] In a read operation, the error correction circuit ECC may receive the first and second sub-data sDQ**1** and sDQ**2** from the eleventh and twenty-first memory devices MEM**11** and MEM**21**, and receive the parity data DQp from the thirty-first memory device MEM**31**. The error correction circuit ECC may detect and correct an error of the first and second sub-data sDQ**1** and sDQ**2** by using the parity data DQp, and transmit final first and second sub-data sDQ**1** and sDQ**2** to the first modulation circuit **1**MDC. Also, the error

correction circuit ECC may receive first and second sub-data strobe clocks sDQS**1** and sDQS**2**, and transmit the received first and second sub-data strobe clocks sDQS**1** and sDQS**2** to the second modulation circuit **2**MDC.

[0093] FIGS. **8** and **9** are diagrams illustrating memory systems in accordance with other embodiments of the present disclosure.

[0094] Referring to FIG. **8**, a memory system **3000** may include a plurality of sub-controllers **200_11** to **200_14**, a control signal transmission circuit CST, and a plurality of memory packages MEM PKG**1** to MEM PKG**10**, which are implemented on one printed circuit board (PCB). For example, each of eleventh to fourteenth sub-controllers **200_11** to **200_14** may be configured identically to the sub-controller **200** or **200_1** described in FIG. **2** or **7**. Each of first to tenth memory packages MEM PKG**1** to MEM PKG**10** may be configured as a package including a plurality of memory devices (**300** shown in FIG. **1**) connected to different sub-channels. For example, the first memory package MEM PKG**1** may include memory devices connected to different sub-channels, and the second memory package MEM PKG**2** may include memory devices connected to different sub-channels. The control signal transmission circuit CST may be configured to transmit control signals CSIG output from a main controller to the eleventh to fourteenth sub-controllers **200_11** to **200_14**. The control signals CSIG may include a command for controlling the plurality of memory packages MEM PKG**1** to MEM PKG**10**, and the like.

[0095] When an error correction circuit (ECC shown in FIG. **7**) is included in the eleventh to fourteenth sub-controllers **200_11** to **200_14**, some memory packages among the first to tenth memory packages MEM PKG**1** to MEM PKG**10** may be used to store parity data DQp[*m*:0], and the other packages among the first to tenth memory packages MEM PKG**1** to MEM PKG**10** may be used to store sub-data.

[0096] The eleventh sub-controller **200_11** among the eleventh to fourteenth sub-controller **200_11** to **200_14** will be described as an example.

[0097] The eleventh sub-controller **200_11** may be configured to communicate with the main controller through a first main channel mCH**1**. For example, the eleventh sub-controller **200_11** may receive or output first main data mDQ**1**[*n*:0] through the first main channel mCH**1**. The first to third memory packages MEM PKG**1** to MEM PKG**3** may be connected to the eleventh sub-controller **200_11**, and the parity data DQp[*m*:0] may be stored in the third memory package MEM PKG**3** among the first to third memory packages MEM PKG**1** to MEM PKG**3**.

[0098] The eleventh sub-controller **200_11** may transmit/receive first main data mDQ**1**[*n*:0] through the first main channel mCH**1**, transmit/receive first sub-data sDQ**1**[*p*:0] through a first sub-channel sCH**1**, transmit/receive second sub-data sDQ**2**[*n*:*p*+1] through a second sub-channel sCH**2**, and transmit/receive parity data DQp[*m*:0] through a third sub-channel sCH**3**.

[0099] When parity data DQ[*m*:0] about the first and second sub-data sDQ**1**[*p*:0] and sDQ**2**[*n*:*p*+1] is stored in a first memory device among memory devices included in the third memory package MEM PKG**3**, another parity data output from the twelfth sub-controller **200_12** may be stored in another memory device included in the third memory package MEM PKG**3**. The first and second sub-data sDQ**1**[*p*:0] and sDQ**2**[*n*:*p*+1] is not a group in which bits of the first main data mDQ**1**[*n*:0] are divided into odd and even numbers, but may be data in which sequentially input bits are divided in ½.

[0100] Referring to FIG. **9**, a memory system **4000** may include a plurality of sub-controllers **200_21** and **200_22** and a plurality of memory packages MEM PKG**1** to MEM PKG**9**, which are implemented on one printed circuit board (PCB). In the memory system **4000** shown in FIG. **9**, the control signal transmission circuit CST shown in FIG. **8** may be omitted. Therefore, control signals CSIG output from the main controller may be directly applied to twenty-first and twenty-second sub-controllers **200_21** and **200_22**.

[0101] In the memory system **4000** shown in FIG. **9**, five memory packages, e.g., first to fifth memory packages MEM PKG**1** to MEM PKG**5** are connected to the twenty-first sub-controller **200_21**, and the fifth memory package MEM PKG**5** among the first to fifth memory packages MEM PKG**1** to MEM PKG**5** is set to store the parity data DQp[*m*:0]. Therefore, the first main data mDQ[*n*:0] may be distributed and stored in the first to fourth memory packages MEM PKG**1** to MEM PKG**4**. For example, each of first to fourth sub-data sDQ**1**[*a*:0], sDQ**1**[*b*:*a*+1], sDQ**1**[*c*:*b*+1], and sDQ**1**[*n*:*c*+1] may be configured with bits obtained by dividing the first main data mDQ[*n*:0] in ¼.

[0102] FIGS. **10** to **13** are diagrams illustrating a package including a sub-controller in accordance with an embodiment of the present disclosure.

[0103] Referring to FIGS. **10** to **13**, the sub-controller **200** in accordance with the present disclosure along with a plurality of memory devices MEM**11** to MEM**22** may constitute one package.

[0104] Referring to FIG. **10**, a first package PKG**1** is a package having a side-by-side structure, and may be frequently used when the number of the memory devices MEM**11** to MEM**22** included in the package is small.

[0105] For example, the sub-controller **200** and the plurality of memory devices MEM**11** to MEM**22** may be stacked on a substrate SUB. The sub-controller **200** may communicate with the plurality of memory devices MEM**11** to MEM**22** through wires WI, and communicate with an external device through a routing RT and external connection pads ExP. The external device may be the main controller (**100** shown in FIG. **1**).

[0106] Referring to FIG. **11**, a second package PKG**2** may include a sub-controller **200** and a plurality of memory devices MEM**11** to MEM**22**, which are stacked on a substrate SUB. The sub-controller **200** may communicate with the plurality of memory devices MEM**11** to MEM**22** through bonding pads BP and wires WI, and communicate with an external device through a routing RT and external connection pads ExP.

[0107] Referring to FIG. **12**, a third package PKG**3** may include first and second stacked structures **1**STR and **2**STR, which are stacked with each other. The first stacked structure **1**STR may include a sub-controller **200** formed on a first substrate **1**SUB. The second stacked structure **2**STR may include a second substrate **2**SUB stacked on the first stacked structure **1**STR and a plurality of memory devices MEM**11** to MEM**22** stacked on the second substrate **2**SUB. The first and second stacked structures **1**STR and **2**STR may be configured to communicate with each other through internal connection pads InP, and the sub-controller **200** may com-

municate with the plurality of memory devices MEM**11** to MEM**22** through a routing RT, the internal connection pads InP, and wires WI.

[0108] Referring to FIG. **13**, a fourth package PKG**4** may include a sub-controller **200** formed in a substrate SUB and a plurality of memory devices MEM**11** to MEM**22** stacked on the substrate SUB. The sub-controller **200** may communicate with an external device through a routing RT and external connection pads ExP, and communicate with the plurality of memory devices MEM**11** to MEM**22** through the routing RT and wires WI.

[0109] In accordance with the present disclosure, large-capacity data can be programmed or read at high speed without signal distortion, and thus the reliability of the memory system which processes data can be improved.

[0110] Various embodiments of the present disclosure have been described in the drawings and specification. Although specific terminologies are used here, those are only to describe the embodiments of the present disclosure. Therefore, the present disclosure is not restricted to the above-described embodiments and many variations are possible within the spirit and scope of the present disclosure. It should be apparent to those skilled in the art that various modifications can be made on the basis of the technological scope of the present disclosure in addition to the embodiments disclosed herein.

[0111] So far as not being differently defined, all terms used herein including technical or scientific terminologies have meanings that are commonly understood by those skilled in the art to which the present disclosure pertains. The terms having the definitions as defined in the dictionary should be understood such that they have meanings consistent with the context of the related technique. So far as not being clearly defined in this application, terms should not be understood in an ideally or excessively formal way.

[0112] Although a memory system and an operating method thereof have been described with reference to the specific embodiments, these are merely examples, and the present disclosure is not limited thereto, and should be interpreted to have the widest scope according to the basic idea disclosed in the present specification. Those skilled in the art may carry out unspecified embodiments by combining and substituting the disclosed embodiments, but these also do not depart from the scope of the present disclosure. In addition, those skilled in the art may easily change or modify the embodiments disclosed based on the present specification, and it is apparent that such changes or modifications also fall within the scope of the present disclosure and the following claims. Furthermore, the embodiments may be combined to form additional embodiments.

What is claimed is:

1. A memory system comprising:

a main controller configured to transmit main data in synchronization with a main data strobe clock;

a sub-controller configured to receive the main data from the main controller, generate first and second sub-data using the main data, and generate first and second sub-data strobe clocks by adjusting a frequency of the main data strobe clock; and

memory devices configured to store the first and second sub-data received from the sub-controller,

wherein the sub-controller is further configured to:

receive the first sub-data from the memory devices through a first sub-channel in synchronization with the first sub-data strobe clock and the second sub-data from the memory devices through a second sub-channel in synchronization with the second sub-data strobe clock;

obtain the main data using the first sub-data and the second sub data; and

output the main data in synchronization with the main data strobe clock.

2. The memory system of claim **1**, wherein the sub-controller divides the main data received from the main controller into the first and second sub-data and merges the first and second sub-data received from the memory devices to obtain the main data.

3. The memory system of claim **1**, wherein a length of the main data is equal to sum of a length of the first sub-data and a length of the second sub-data.

4. The memory system of claim **1**, the sub-controller generates the first and second sub-data strobe clocks by increasing the frequency of the main data strobe clock.

5. The memory system of claim **1**, the sub-controller generates the first sub-data strobe clock by increasing the frequency of the main data strobe clock and the second sub-data strobe clock by decreasing the frequency of the main data strobe clock.

6. The memory system of claim **1**, the sub-controller generates the first sub-data strobe clock by decreasing the frequency of the main data strobe clock at a first ratio and the second sub-data strobe clock by decreasing the frequency of the main data strobe clock at a second ratio.

7. The memory system of claim **6**, wherein each of the first ratio and the second ratio is determined based on at least one of a number of sub-channels through which the first and second sub-data are transmitted and types of the memory devices connected to the sub-channels.

8. The memory system of claim **7**, wherein types of memory devices connected to the first sub-channel are different from types of memory devices connected to the second sub-channel.

9. A method for operating a memory system, the method comprising:

generating a main data strobe clock used for transferring main data;

generating sub-data strobe clocks by adjusting a frequency of the main data strobe clock at different ratios according to sub-channels corresponding to the respective sub-data strobe clocks;

receiving sub-data in synchronization with the sub-data strobe clocks;

merging the sub-data from the different sub-channels to obtain the main data; and

outputting the main data in synchronization with the main-data strobe clock.

10. The method of claim **9**, wherein the different ratios are determined based on at least one of a number of the sub-channels through which the sub-data are transmitted and types of memory devices connected to the sub-channels.

11. The method of claim **9**, wherein generating the sub-data strobe clocks comprises generating the respective sub-data strobe clocks by increasing the frequency of the main data strobe clock.

12. The method of claim **9**, wherein generating the sub-data strobe clocks comprises generating a first sub-data strobe clock among the sub-data strobe clocks by increasing the frequency of the main data strobe clock and a second

sub-data strobe clock among the sub-data strobe clocks by decreasing the frequency of the main data strobe clock.

13. The method of claim **9**, wherein generating the sub-data strobe clocks comprises generating a first sub-data strobe clock by decreasing the frequency of the main data strobe clock at a first ratio and a second sub-data strobe clock by decreasing the frequency of the main data strobe clock at a second ratio different from the first ratio.

14. The method of claim **9**, wherein receiving the sub-data comprises:

receiving a first piece of the sub-data in synchronization with a first sub-data strobe clock among the sub-data strobe clocks through a first sub-channel among the sub-channels; and

receiving a second piece of the sub-data in synchronization with a second sub-data strobe clock among the sub-data strobe clocks through a second sub-channel among the sub-channels.

15. The method of claim **14**, wherein generating the sub-data strobe clocks comprises:

generating the first sub-data strobe clock by decreasing the frequency of the main data strobe clock at a first ratio among the different ratios; and

generating the second sub-data strobe clock by decreasing the frequency of the main data strobe clock at a second ratio among the different ratios.

16. The method of claim **15**, wherein generating the sub-data strobe clocks comprises:

generating the first sub-data strobe clock by decreasing the frequency of the main data strobe clock at a first ratio among the different ratios; and

generating and the second sub-data strobe clock by decreasing the frequency of the main data strobe clock at a second ratio among the different ratios.

17. The method of claim **16**, wherein types of memory devices connected to the first sub-channel are different from types of memory devices connected to the second sub-channel.

18. The method of claim **14**, wherein a length of the main data is equal to sum of a length of the first piece of the sub-data and a length of the second piece of the sub-data.

* * * * *