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A SEMICONDUCTOR DEVICE COMPRISING DIFFERENT TYPES OF MICROELECTROMECHANICAL SYSTEMS DEVICES

Abstract

Various embodiments of the present disclosure are directed towards an integrated chip. The integrated chip includes a first movable element over a first substrate. A second movable element overlies the first substrate. A first functional layer is on the first movable element. The first functional layer comprises a first material different from a material of the first movable element. A second functional layer is on the second movable element.

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Background/Summary

REFERENCE TO RELATED APPLICATIONS [0001] This Application is a Continuation of U.S. application Ser. No. 18/365,449, filed on Aug. 4, 2023, which is a Divisional of U.S. application Ser. No. 16/907,607, filed on Jun. 22, 2020 (now U.S. Pat. No. 11,851,323, issued on Dec. 26, 2023), which claims the benefit of U.S. Provisional Application No. 62/891,489, filed on Aug. 26, 2019. The contents of the above-referenced Patent Applications are hereby incorporated by reference in their entirety.

BACKGROUND
[0002] Microelectromechanical systems (MEMS) is a technology that integrates miniaturized mechanical and electro-mechanical elements on an integrated chip. MEMS devices are often made using micro-fabrication techniques. In recent years, MEMS devices have found a wide range of applications. For example, MEMS devices are found in cell phones (e.g., accelerometers, gyroscopes, digital compasses), pressure sensors, micro-fluidic elements (e.g., valves, pumps), optical switches (e.g., mirrors), imaging devices (e.g., micromachined ultrasonic transducers (MUTs)), etc.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0003] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.
[0004] FIG. **1** illustrates a cross-sectional view of some embodiments of a semiconductor device comprising different types of microelectromechanical system (MEMS) devices.
[0005] FIG. **2** illustrates a cross-sectional view of some more detailed embodiments of the semiconductor device of FIG. **1**.
[0006] FIG. **3** illustrates a cross-sectional view of some other embodiments of the semiconductor device of FIG. **2**.
[0007] FIG. **4** illustrates a cross-sectional view of some other embodiments of the semiconductor device of FIG. **2**.
[0008] FIGS. **5**A-**5**B illustrate various views of some embodiments of an area of the semiconductor device of FIG. **4**.
[0009] FIGS. **6**A-**6**B illustrate various views of some other embodiments of the area of the semiconductor device of FIG. **4**.
[0010] FIG. **7** illustrates a cross-sectional view of some other embodiments of the semiconductor device of FIG. **2**.
[0011] FIG. **8** illustrates a cross-sectional view of some other embodiments of the semiconductor device of FIG. **2**.
[0012] FIG. **9** illustrates a cross-sectional view of some other embodiments of the semiconductor device of FIG. **2**.
[0013] FIG. **10** illustrates a simplified layout view of some embodiments of the semiconductor

device of FIG. **2**.
[0014] FIGS. **11**-**22** illustrate a series of cross-sectional views of some embodiments of a method for forming some embodiments of the semiconductor device of FIG. **4**.
[0015] FIG. **23** illustrates a flowchart of some embodiments of a method for forming a semiconductor device comprising different types of microelectromechanical system (MEMS) devices.
DETAILED DESCRIPTION
[0016] The present disclosure will now be described with reference to the drawings wherein like reference numerals are used to refer to like elements throughout, and wherein the illustrated structures are not necessarily drawn to scale. It will be appreciated that this detailed description and the corresponding figures do not limit the scope of the present disclosure in any way, and that the detailed description and figures merely provide a few examples to illustrate some ways in which the inventive concepts can manifest themselves.
[0017] The present disclosure provides many different embodiments, or examples, for implementing different features of this disclosure. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.
[0018] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.
[0019] In some embodiments, a semiconductor device (e.g., integrated chip) comprises a microelectromechanical systems (MEMS) device. The MEMS device comprises a cavity and a movable membrane. The configuration (e.g., structural configuration) of the MEMS device is dependent on the type of MEMS device. For example, if the MEMS device is a capacitive micromachined ultrasonic transducer (CMUT), the MEMS device has a first configuration that corresponds to the CMUT, while on the other hand if the MEMS device is a piezoelectric micromachined ultrasonic transducer (PMUT), the MEMS device has a second configuration different than the first configuration that corresponds to the PMUT. It will be appreciated that a CMUT and a PMUT are not the only type of MEMS devices with different configurations, rather differences may exist between many other types of MEMS devices, such as a CMUT, PMUT, contact-type ultrasonic MEMS sensor (e.g., fingerprint sensor), non-contact-type ultrasonic MEMS sensor (e.g., gesture sensor), a resonant-type mechanical MEMS device (e.g., radio frequency (RF) switch, RF filter, etc.), pressure sensor, moisture sensor, fluid sensor (e.g., gas composition sensor), biosensor (e.g., MEMS-based glucose sensor), IR sensor (e.g., IR detection sensor, IR image sensor, etc.), etc.
[0020] One difference in the configurations of different types of MEMS devices is a difference in the chemical composition of a functional structure that overlies the movable membrane. For example, if the MEMS device is an IR sensor, the MEMS device may have a first functional structure having a first chemical composition overlying the movable membrane of the MEMS

device. On the other hand, if the MEMS device is a PMUT, the MEMS device may have a second functional structure having a second chemical composition different than the first chemical composition overlying the movable membrane of the MEMS device. It will be appreciated that differences in configurations between different types of MEMS devices is not limited to a difference in the chemical compositions of the functional structure, rather other types of differences may exist between the different types of MEMS devices, such as differences in doping concentrations of the movable membrane, the presence versus absence of the functional structure, etc.

[0021] Typically, the semiconductor device only comprises MEMS devices of the same type. For example, if the semiconductor device comprises the CMUT, the semiconductor device will only comprise CMUTs. On the other hand, if the semiconductor device comprises the PMUT, the semiconductor device will only comprise PMUTs. Thus, a single semiconductor device comprising different types of MEMS devices is desirable to reduce manufacturing costs, reduce packaging sizes, reduce power consumption, etc.

[0022] Various embodiments of the present application are directed toward a semiconductor device comprising different types of MEMS devices. The semiconductor device comprises an interconnect structure disposed over a semiconductor substrate. A dielectric structure is disposed over the interconnect structure. A microelectromechanical system (MEMS) substrate is disposed over the dielectric structure. A first MEMS device is disposed over the semiconductor substrate. The first MEMS device comprises a first cavity disposed in the dielectric structure, and a first movable membrane of the MEMS substrate that overlies the first cavity. Further, the first MEMS device comprises a first functional structure overlying the first movable membrane and the first cavity. The first functional structure comprises a first material having a first chemical composition. A second MEMS device is disposed over the semiconductor substrate and laterally spaced from the first MEMS device. The second MEMS device comprises a second cavity disposed in the dielectric structure, and a second movable membrane of the MEMS substrate that overlies the second cavity. Further, the second MEMS device comprises a second functional structure overlying the second movable membrane and the second cavity. The second functional structure comprises a second material having a second chemical composition that is different than the first chemical composition.

[0023] Because the second material has a different chemical composition than the first material, a physical property of the first functional structure may change in response to a first external stimulus while a physical property of the second functional structure may change in response to a second stimulus that is different than the first stimulus. Thus, the MEMS device is a first type of MEMS device and the second MEMS device is a second type of MEMS device different than the first type. Accordingly, the semiconductor device comprises different types of MEMS devices, which may reduce manufacturing costs, reduce packaging sizes, reduce power consumption, etc.

[0024] FIG. **1** illustrates a cross-sectional view of some embodiments of a semiconductor device **100** comprising different types of microelectromechanical system (MEMS) devices.

[0025] As shown in FIG. **1**, the semiconductor device **100** comprises an integrated circuit (IC) structure **102**. The IC structure **102** comprises a semiconductor substrate **104**. The semiconductor substrate **104** may comprise any type of semiconductor body (e.g., monocrystalline silicon/CMOS bulk, silicon-germanium (SiGe), silicon on insulator (SOI), etc.).

[0026] In some embodiments, one or more IC devices **106** are disposed on/over the semiconductor substrate **104**. The IC devices **106** may be or comprise, for example, active electronic devices (e.g., transistors), passive electronic devices (e.g., resistors, capacitors, inductors, fuses, etc.), some other electronic devices, or a combination of the foregoing. For example, one of the IC devices **106** may be a metal-oxide-semiconductor field-effect transistor (MOSFET) comprising a pair of source/drain regions **108** disposed in the semiconductor substrate **104**, a gate dielectric **110** disposed over the semiconductor substrate **104** and between the source/drain regions **108**, and a gate electrode **112**

disposed over the semiconductor substrate **104** and overlying the gate dielectric **110**. For readability, only some of the IC devices **106** are specifically labeled. In further embodiments, the IC structure **102** is a complementary metal-oxide-semiconductor (CMOS) structure and the IC devices **106** are part of a CMOS circuit.

[0027] The IC structure **102** comprises an interconnect structure **114**, a first dielectric structure **116**, a second dielectric structure **119**, a third dielectric structure **124**, and a plurality of electrodes **128** disposed over the semiconductor substrate **104** and the IC devices **106**. The interconnect structure **114** comprises one or more first conductive contacts **118**, one or more first conductive vias **120**, one or more first conductive lines **122**, a plurality of second conductive vias **121**, a plurality of second conductive lines **123**, and a plurality of third conductive vias **126**. The first conductive contacts **118**, the first conductive vias **120**, and the first conductive lines **122** are embedded in the first dielectric structure **116**. In some embodiments, the first conductive contacts **118**, the first conductive vias **120**, and the first conductive lines **122** are referred to as a CMOS interconnect structure. The CMOS interconnect structure interconnects the IC devices **106** together in a predefined pattern.

[0028] The second dielectric structure **119** is disposed over the first dielectric structure **116**, the first conductive contacts **118**, the first conductive vias **120**, and the first conductive lines **122**. The second conductive vias **121** and the second conductive lines **123** are embedded in the second dielectric structure **119**. The third dielectric structure **124** is disposed over the second dielectric structure **119**, the second conductive vias **121**, and the second conductive lines **123**. The third conductive vias **126** and the electrodes **128** are embedded in the third dielectric structure **124**.

[0029] The interconnect structure **114** electrically couples the IC devices **106** to the electrodes **128**. For example, the interconnect structure **114** electrically couples one or more of the IC devices **106** to a first electrode **128***a* of the electrodes **128** and/or one or more of the IC devices **106** to a second electrode **128***b* of the electrodes **128**. For readability, only some of the first conductive contacts **118**, only some of the first conductive vias **120**, only some of the first conductive lines **122**, only some of the second conductive vias **121**, only some of the second conductive lines **123**, only some of the third conductive vias **126**, and only some of the electrodes **128** are specifically labeled.

[0030] The first conductive contacts **118**, the first conductive vias **120**, the first conductive lines **122**, and/or the third conductive vias **126** may be or comprise, for example, a metal (e.g., copper (Cu), aluminum (Al), tungsten (W), or the like), a metal nitride (e.g., titanium nitride (TiN)), polysilicon (e.g., doped polysilicon), some other conductive material, or a combination of the foregoing. The second conductive vias **121** and the second conductive lines **123** may comprise, for example, a metal (e.g., Al, Cu, aluminum-copper (AlCu), titanium (Ti), silver (Ag), gold (Au), or the like), a metal nitride (e.g., TiN), some other conductive material, or a combination of the foregoing. The electrodes **128** may be or comprise, for example, a metal (e.g., Al, Cu, AlCu, Ti, or the like), a metal nitride (e.g., TiN), some other conductive material, or a combination of the foregoing. The first dielectric structure **116**, the second dielectric structure **119**, and the third dielectric structure **124** comprise one or more stacked dielectric layers, which may respectively comprise a low-k dielectric (e.g., a dielectric material with a dielectric constant less than about 3.9), an oxide (e.g., silicon dioxide (SiO.sub.2)), or the like.

[0031] A fourth dielectric structure **130** is disposed over the interconnect structure **114** and the third dielectric structure **124**. The fourth dielectric structure **130** comprises a first dielectric layer **132** and a second dielectric layer **134**. The second dielectric layer **134** is disposed over the first dielectric layer **132**. In some embodiments, the first dielectric layer **132** covers the electrodes **128**.

[0032] The first dielectric layer **132** may be or comprise, for example, a nitride (e.g., silicon nitride (SiN)), an oxide (e.g., SiO.sub.2), an oxy-nitride (e.g., silicon oxy-nitride (SiO.sub.XN.sub.Y)), some other dielectric material, or a combination of the foregoing. The second dielectric layer **134** may be or comprise, for example, an oxide (e.g., SiO.sub.2), a nitride (e.g., SiN), an oxy-nitride (e.g., SiO.sub.XN.sub.Y), some other dielectric material, or a combination of the foregoing. In

some embodiments, the first dielectric layer **132** may be a different dielectric material than the second dielectric layer **134**. For example, the first dielectric layer **132** may be SiN and the second dielectric layer **134** may be SiO.sub.2. While the fourth dielectric structure **130** is illustrated comprising the first dielectric layer **132** and the second dielectric layer **134**, it will be appreciated that the fourth dielectric structure **130** may comprise any number of dielectric layers.

[0033] A microelectromechanical system (MEMS) substrate **136** is disposed over the fourth dielectric structure **130** and the IC structure **102**. In some embodiments, the MEMS substrate **136** is disposed on the fourth dielectric structure **130**. In further embodiments, a bond interface exists at an interface of the MEMS substrate **136** and the fourth dielectric structure **130**. For example, in some embodiments, the MEMS substrate **136** is bonded to the fourth dielectric structure **130** via a bonding process (e.g., fusion bonding), thereby forming the bond interface at the interface of the MEMS substrate **136** and the fourth dielectric structure **130**. The MEMS substrate **136** may be or comprise, for example, a semiconductor material (e.g., polysilicon, amorphous silicon, monocrystalline silicon, SiGe, Ge, or the like), a metal (e.g., Al, Cu, AlCu), an oxide (e.g., SiO.sub.2), a nitride (e.g., SiN), some other suitable MEMS substrate, or a combination of the foregoing. In some embodiments in which the MEMS substrate **136** is or comprises a semiconductor material, the semiconductor material may be doped or undoped. In yet further embodiments, the MEMS substrate **136** is a single semiconductor structure comprising the semiconductor material.

[0034] A third dielectric layer **138** is disposed over the MEMS substrate **136** and the fourth dielectric structure **130**. A plurality of fourth conductive vias **140** extend vertically through the third dielectric layer **138**, the MEMS substrate **136**, the fourth dielectric structure **130**, and the third dielectric structure **124** to contact at least one of the second conductive lines **123**, such that the fourth conductive vias **140** are electrically coupled to the interconnect structure **114**. For example, a fifth conductive via **140***a*, which is one of the fourth conductive vias **140**, extends vertically through the third dielectric layer **138**, the MEMS substrate **136**, the fourth dielectric structure **130**, and the third dielectric structure **124** to contact a third conductive line **123***a*, which is one of the second conductive lines **123**, so that the fifth conductive via **140***a* is electrically coupled to the interconnect structure **114**. Further, a sixth conductive via **140***b*, which is another one of the fourth conductive vias **140**, extends vertically through the third dielectric layer **138**, the MEMS substrate **136**, the fourth dielectric structure **130**, and the third dielectric structure **124** to contact a fourth conductive line **123***b*, which is another one of the second conductive lines **123**, so that the sixth conductive via **140***b* is electrically coupled to the interconnect structure **114**. The fourth conductive vias **140** are laterally spaced from one another. In some embodiments, the fourth conductive vias **140** are electrically isolated from one another. In further embodiments, the fourth conductive vias **140** extend laterally over an upper surface of the third dielectric layer **138**.

[0035] The fourth conductive vias **140** line a plurality of via openings **142**, respectively. For example, the fifth conductive via **140***a* lines a first via opening **142***a*, which is one of the via openings **142**, and the sixth conductive via **140***b* lines a second via opening **142***b*, which is another one of the via openings **142**. The via openings **142** are disposed in the third dielectric layer **138**, the MEMS substrate **136**, the fourth dielectric structure **130**, and the third dielectric structure **124**. The via openings **142** extend vertically through the third dielectric layer **138**, the MEMS substrate **136**, the fourth dielectric structure **130**, and the third dielectric structure **124** to expose one or more of the second conductive lines **123**. For example, the first via opening **142***a* extends vertically through the third dielectric layer **138**, the MEMS substrate **136**, the fourth dielectric structure **130**, and the third dielectric structure **124** to expose the third conductive line **123***a*. The via openings **142** are at least partially defined by the third dielectric layer **138**, the MEMS substrate **136**, the fourth dielectric structure **130**, and the second conductive lines **123**. For example, sidewalls of the first via opening **142***a* are defined by sidewalls of the third dielectric layer **138**, sidewalls of the MEMS substrate **136**, sidewalls of the fourth dielectric structure **130**, and sidewalls of the third dielectric

structure **124**, and a bottom surface of the first via opening **142***a* is at least partially defined by an upper surface of the third conductive line **123***a*.

[0036] A plurality of second conductive contacts **144** are disposed over the MEMS substrate **136** and the third dielectric layer **138**. For example, a third conductive contact **144***a*, which is one of the second conductive contacts **144**, and a fourth conductive contact **144***b*, which is another one of the second conductive contacts **144**, are disposed over the MEMS substrate **136** and the third dielectric layer **138**. In some embodiments, the second conductive contacts **144** extend through the third dielectric layer **138** and contact the MEMS substrate **136**. In further embodiments, the second conductive contacts **144** are electrically coupled to the MEMS substrate **136**. For readability, only some of the second conductive contacts **144** are specifically labeled. The second conductive contacts **144** may be electrically coupled to the interconnect structure **114** via the fourth conductive vias **140**. For example, the third conductive contact **144***a* is electrically coupled to the fifth conductive via **140***a*, and the fourth conductive contact **144***b* is electrically coupled to the sixth conductive via **140***b*.

[0037] The third dielectric layer **138** may be or comprise, for example, an oxide (e.g., SiO.sub.2), a nitride (e.g., SiN), an oxy-nitride (e.g., SiO.sub.XN.sub.Y), some other dielectric material, or a combination of the foregoing. The fourth conductive vias **140** may be or comprise, for example, a metal (e.g., Al, Cu, AlCu, Ti, Ag, Au, or the like), a metal nitride (e.g., TiN), some other conductive material, or a combination of the foregoing. The second conductive contacts **144** may be or comprise, for example, a metal (e.g., Al, Cu, AlCu, Ti, Ag, Au, or the like), a metal nitride (e.g., TiN), some other conductive material, or a combination of the foregoing. In some embodiments, the fourth conductive vias **140** and the second conductive contacts **144** are a same material. In further embodiments, the fourth conductive vias **140** may have a thickness between about 0.05 micrometers (um) and about 1 um. In yet further embodiments, the second conductive contacts **144** may have a thickness between about 0.05 um and about 1 um.

[0038] The semiconductor device **100** comprises a plurality of MEMS devices **146** that are disposed over the semiconductor substrate **104** and the second dielectric structure **119**. The MEMS devices **146** are laterally spaced from one another. The MEMS devices **146** comprise a first plurality of cavities **148**, respectively, a first plurality of movable membranes **150**, respectively, and the electrodes **128**, respectively. The cavities **148** are laterally spaced from one another. The movable membranes **150** are laterally spaced from one another. The movable membranes **150** are portions of the MEMS substrate **136** that are configured to move (e.g., flex) in response to one or more stimuli (e.g., pressure, voltage, etc.). In some embodiments, the electrodes **128** are laterally spaced from one another. For readability, only some of the MEMS devices **146**, some of the cavities **148**, and some of the movable membranes **150** are specifically labeled.

[0039] For example, the MEMS devices **146** comprise a first MEMS device **146***a* and a second MEMS device **146***b*. The first MEMS device **146***a* is laterally spaced from the second MEMS device **146***b*. The first MEMS device **146***a* comprises a first cavity **148***a* of the cavities **148**, a first movable membrane **150***a* of the movable membranes **150**, and the first electrode **128***a*. The second MEMS device **146***b* comprises a second cavity **148***b* of the cavities **148**, a second movable membrane **150***b* of the movable membranes **150**, and the second electrode **128***b*. The first cavity **148***a* is laterally spaced from the second cavity **148***b*. The first movable membrane **150***a* is laterally spaced from the second movable membrane **150***b*.

[0040] Each of the MEMS devices **146** are a different type of MEMS device. For example, the first MEMS device **146***a* is a first type of MEMS device, and the second MEMS device **146***b* is a second type of MEMS device that is different than the first type of MEMS device. The MEMS devices **146** may be, for example, a capacitive micromachined ultrasonic transducer (CMUT), a piezoelectric micromachined ultrasonic transducer (PMUT), a contact-type ultrasonic MEMS sensor (e.g., fingerprint sensor), a non-contact-type ultrasonic MEMS sensor (e.g., gesture sensor), a resonant-type mechanical MEMS device (e.g., radio frequency (RF) switch, RF filter, etc.), a

pressure sensor, a moisture sensor, a fluid sensor (e.g., gas composition sensor), a biosensor (e.g., MEMS-based glucose sensor), an IR sensor (e.g., IR detection sensor, IR image sensor, etc.), or some other type of MEMS device. For example, the first MEMS device **146***a* may be an IR detection sensor, and the second MEMS device may be any other type of MEMS device besides the IR detection sensor (e.g., a CMUT, a different type of IR sensor, etc.). Because the semiconductor device **100** comprises different types of MEMS devices, the semiconductor device **100** may reduce manufacturing costs, reduce packaging sizes, reduce power consumption, etc.

[0041] The MEMS devices **146** have different configurations (e.g., structural configurations) that are dependent on the MEMS devices **146** respective type of MEMS device. For example, the first MEMS device **146***a* has a first configuration that is dependent on the type of the first MEMS device **146***a* (e.g., IR detection sensor), and the second MEMS device **146***b* has a second configuration different than the first configuration that is dependent on the type of the second MEMS device **146***b* (e.g., CMUT). Some embodiments of different types of MEMS devices with different configurations are described in more detail herein.

[0042] In some embodiments, the MEMS devices **146** comprise functional structures **152**, respectively. The functional structures **152** overlie the movable membranes **150** of the MEMS devices **146**, respectively. In further embodiments, the functional structures **152** may be laterally spaced. For example, the first MEMS device **146***a* comprises a first functional structure **152***a* that overlies the first movable membrane **150***a*, and the second MEMS device **146***b* comprises a second functional structure **152***b* that overlies the second movable membrane **150***b*. The first functional structure **152***a* is laterally spaced from the second functional structure **152***b*. In some embodiments, bottommost surfaces of the functional structures **152** are substantially co-planar. For example, a bottommost surface of the first functional structure **152***a* is substantially co-planar with a bottommost surface of the second functional structure **152***b*.

[0043] Physical properties of the functional structures **152** change in response to being exposed to stimuli, respectively. For example, a physical property of the first functional structure **152***a* changes in response to being exposed to a first stimulus, and a physical property of the second functional structure **152***b* changes in response to being exposed to a second stimulus. In some embodiments, the type of MEMS device is at least partially dependent on the physical properties of the functional structures **152** that change in response to the stimuli and/or the stimuli that cause the physical properties of the functional structures **152** to change. For example, if a physical property of the first functional structure **152***a* changes in response to being exposed to IR, the first MEMS device **146***a* is an IR sensor. Further, if the first MEMS device **146***a* is configured to detect IR, the IR sensor is an IR detection sensor. On the other hand, if the first MEMS device **146***a* is configured to generate an image based on IR, the first MEMS device **146***a* is an IR image sensor. It will be appreciated that the type of MEMS devices may be dependent on other characteristics of the MEMS devices **146** (e.g., working principle, such as a thermoelectric IR sensor, pyroelectric IR sensor, bolometer IR sensor, etc.).

[0044] In some embodiments, the physical properties of the functional structures **152** that change in response to the stimuli and/or the stimuli that cause the physical properties of the functional structures **152** to change are at least partially dependent on the chemical composition of the functional structures. For example, if the first MEMS device **146***a* is an IR sensor, the first functional structure **152***a* may be or comprise an infrared sensitive material, and if the second MEMS device **146***b* is a PMUT, the second functional structure **152***b* may be or comprise a piezoelectric material. Accordingly, the configurations of different types of MEMS devices may be different in respect to the chemical composition of their respective functional structures.

[0045] The MEMS devices **146** may be MEMS sensors, MEMS actuators, MEMS transceivers, or a combination of the foregoing. For example, if the first MEMS device **146***a* is a MEMS sensor, the first MEMS device **146***a* is configured to sense the change in the physical property of the first functional structure **152***a*. In some embodiments, a shape of the first functional structure **152***a* may

change in response to being exposed to the first stimulus (e.g., an electrical signal (e.g., voltage), a fluid (e.g., a gas), a biological element (e.g., blood), radiation (e.g., IR), etc.). The change in shape of the first functional structure **152***a* may deflect the first movable membrane **150***a* causing the first MEMS device **146***a* to output an electrical signal that corresponds to a distance in which the first movable membrane **150***a* is spaced from the first electrode **128***a* (e.g., due to a change in capacitance between the first movable membrane **150***a* and the first electrode **128***a*). The electrical signal may be output via the first electrode **128***a* and analyzed by one or more of the IC devices **106**. In other embodiments, the change in physical property may change a capacitance between the first functional structure **152***a* and the first electrode **128***a* (e.g., due to the physical property changing a voltage of the first functional structure **152***a*).

[0046] In some embodiments, a shape of the second functional structure **152***b* may change in response to being exposed to the second stimulus (e.g., an electrical signal (e.g., voltage), a fluid (e.g., a gas), a biological element (e.g., blood), radiation (e.g., IR), etc.). The change in shape of the second functional structure **152***b* may deflect the second movable membrane **150***b* causing the second MEMS device **146***b* to output an electrical signal that corresponds to a distance in which the second movable membrane **150***b* is spaced from the second electrode **128***b* (e.g., due to a change in capacitance between the second movable membrane **150***b* and the second electrode **128***b*). The electrical signal may be output via the second electrode **128***b* and analyzed by one or more of the IC devices **106**. In other embodiments, the change in physical property may change a capacitance between the second functional structure **152***b* and the second electrode **128***b* (e.g., due to the physical property changing a voltage of the second functional structure **152***b*). In yet further embodiments, if the MEMS devices **146** are MEMS sensors, the functional structures **152** may be referred to as sensing structures.

[0047] If the first MEMS device **146***a* is a MEMS actuator, the change in the physical property of the first functional structure **152***a* causes the first MEMS device to output an action (e.g., mechanical movement, magnetic field, heat, etc.). If the first MEMS device **146***a* is a MEMS transducer (e.g., CMUT), the first MEMS device **146***a* may operate as both a receiver (e.g., MEMS sensor) and a transmitter (e.g., MEMS actuator) to both output an action and sense a response to the action. It will be appreciated that a MEMS sensor, a MEMS actuator, and a MEMS transceiver may be different types of MEMS devices.

[0048] The functional structures **152** may be or comprise, for example, a piezoelectric material (e.g., molybdenum (Mo), lead zirconate titanate (PZT), aluminum nitride (AlN), zinc oxide (ZnO), etc), a biosensitive material (e.g., a bio-recognition component disposed on (or part of) a metal (e.g., Au, Ag, platinum (Pt), etc.)), an IR sensitive material (e.g., vanadium oxide (VOx), mercury cadmium telluride (HgCdTe), silicon (Si), cadmium zinc telluride (CdZnTe), etc.), a polymer (e.g., polyimide, SU-8, negative/positive photoresist, etc.), or the like. In some embodiments, if the first functional structure **152***a* is a piezoelectric material, the first MEMS device **146***a* may be a PMUT; if the first functional structure **152***a* is a biosensitive material, the first MEMS device **146***a* may be a biosensor; if the first functional structure **152***a* is an IR sensitive material, the first MEMS device **146***a* may be an IR sensor; and if the first functional structure **152***a* is a polymer, the first MEMS device **146***a* may some other type of MEMS sensor (e.g., pressure sensor, gas sensor, moisture sensor, etc.).

[0049] Accordingly, it will be appreciated that, in some embodiments, the first functional structure **152***a* is or comprises a first type of material while the second functional structure **152***b* is not (or does not comprise) the first type of material. For example, the first functional structure **152***a* is (or comprises) an IR sensitive material and the second functional structure **152***b* is not (or does not comprise) the IR sensitive material, the first functional structure **152***a* is (or comprises) a piezoelectric material and the second functional structure **152***b* is not (or does not comprise) the piezoelectric material, the first functional structure **152***a* is (or comprises) a biosensitive material and the second functional structure **152***b* is not (or does not comprise) the biosensitive material, the

first functional structure **152***a* is (or comprises) a polymer and the second functional structure **152***b* is not (or does not comprise) the polymer, etc.

[0050] In some embodiments, the functional structures **152** may each have a thickness between about 0.0005 um and about 50 um. If the functional structures **152** have a thickness that is less than about 0.0005 um, the MEMS devices **146** may not be able to sense a change in the physical properties of the functional structures **152** (and/or cause a change in the physical properties of the functional structures **152**). If the functional structures **152** have a thickness that is greater than about 50 um, a cost to manufacture the semiconductor device **100** may be increased without an appreciable benefit. More specifically, if the functional structures **152** comprise a polymer, the functional structures **152** may have a thickness between about 0.0005 um and about 10 um; if the functional structures **152** comprise an IR sensitive material, the functional structures **152** may have a thickness between about 0.1 um and about 0.2 um; and if the functional structures **152** comprise a piezoelectric material, the functional structures **152** may have a thickness between about 0.05 um and about 50 um.

[0051] If the functional structures **152** comprise a polymer and have a thickness less than about 0.0005 um, the MEMS devices **146** may not be able to sense a change in the physical properties of the functional structures **152** (and/or cause a change in the physical properties of the functional structures **152**). If the functional structures **152** comprise a polymer and have a thickness greater than about 10 um, a cost to manufacture the semiconductor device **100** may be increased without an appreciable benefit. If the functional structures **152** comprise an IR sensitive material and have a thickness less than about 0.1 um, the MEMS devices **146** may not be able to sense a change in the physical properties of the functional structures **152** (and/or cause a change in the physical properties of the functional structures **152**). If the functional structures **152** comprise an IR sensitive material and have a thickness greater than about 0.2 um, a cost to manufacture the semiconductor device **100** may be increased without an appreciable benefit. If the functional structures **152** comprise a piezoelectric material and have a thickness less than about 0.05 um, the MEMS devices **146** may not be able to sense a change in the physical properties of the functional structures **152** (and/or cause a change in the physical properties of the functional structures **152**). If the functional structures **152** comprise a piezoelectric material and have a thickness greater than about 50 um, a cost to manufacture the semiconductor device **100** may be increased without an appreciable benefit.

[0052] In some embodiments, the thicknesses of the functional structures **152** may be substantially the same. For example, a thickness of the first functional structure **152***a* may be substantially the same as the second functional structure **152***b*. In other embodiments, the thicknesses of the functional structures **152** may be different. For example, a thickness of the first functional structure **152***a* may be different than the thickness of the second functional structure **152***b*.

[0053] In some embodiments, the third conductive contact **144***a*, the fifth conductive via **140***a*, and the third conductive line **123***a* are part of a first MEMS routing structure that is electrically coupled to one or more of the IC devices **106**. The fourth conductive contact **144***b*, the sixth conductive via **140***b*, and the fourth conductive line **123***b* may be part of a second MEMS routing structure that is electrically coupled to one or more of the IC devices **106**. The first MEMS routing structure electrically couples the first MEMS device **146***a* to the one or more of the IC devices **106**, and the second MEMS routing structure electrically couples the second MEMS device **146***b* to the one or more IC devices **106**. In some embodiments, the first MEMS routing structure may be electrically coupled to one or more of the IC devices **106** and the first functional structure **152***a*. In further embodiments, the second MEMS routing structure may be electrically coupled to one or more of the IC devices **106** and the second functional structure **152***b*.

[0054] In some embodiments, the first MEMS routing structure and the second MEMS routing structure may be electrically isolated from one another. In further embodiments, the first MEMS routing structure and the second MEMS routing structure may be electrically coupled to different

(or a different set) of IC devices **106**. In other embodiments, the first MEMS routing structure and the second MEMS routing structure may be electrically coupled to one or more of the same IC devices **106**. It will be appreciated that, in some embodiments, the semiconductor device **100** comprises a MEMS routing structure for each MEMS devices **146**.

[0055] FIG. **2** illustrates a cross-sectional view of some more detailed embodiments of the semiconductor device **100** of FIG. **1**.

[0056] As shown in FIG. **2**, the second dielectric structure **119** comprises a fourth dielectric layer **202** and a fifth dielectric layer **204**. The fourth dielectric layer **202** may be or comprise, for example, a low-k dielectric (e.g., a dielectric material with a dielectric constant less than about 3.9), an oxide (e.g., silicon dioxide (SiO.sub.2)), or the like. The fifth dielectric layer **204** is disposed over the fourth dielectric layer **202**. The fifth dielectric layer **204** may be or comprise, for example, a low-k dielectric (e.g., a dielectric material with a dielectric constant less than about 3.9), an oxide (e.g., silicon dioxide (SiO.sub.2)), or the like. In some embodiments, the second conductive lines **123** are disposed in the fifth dielectric layer **204**. The second conductive vias **121** may be disposed in the fourth dielectric layer **202**. In further embodiments, the second conductive vias **121** and/or the fourth dielectric layer **202** are disposed vertically between the first dielectric structure **116** and the fifth dielectric layer **204**.

[0057] The third dielectric structure **124** comprises a sixth dielectric layer **206**, a first outgassing prevention layer **208**, a seventh dielectric layer **210**, and an eighth dielectric layer **212**. The first outgassing prevention layer **208** is disposed over the sixth dielectric layer **206**, the seventh dielectric layer **210** is disposed over the first outgassing prevention layer **208**, and the eighth dielectric layer **212** is disposed over the seventh dielectric layer **210**. In some embodiments, the electrodes **128** are disposed in the eighth dielectric layer **212**. In further embodiments, the third conductive vias **126** extend vertically through the sixth dielectric layer **206**, the first outgassing prevention layer **208**, and the seventh dielectric layer **210**. In yet further embodiments, the electrodes **128** may have a thickness between about 0.05 um and about 1 um.

[0058] The first outgassing prevention layer **208** prevents gases (e.g., oxygen, carbon dioxide, or the like) from outgassing from other features of the semiconductor device **100** into the cavities **148**. In some embodiments, the first outgassing prevention layer **208** may be or comprise, for example, a nitride (e.g., SiN), an oxy-nitride (e.g., SiO.sub.XN.sub.Y), some other outgassing prevention material, or a combination of the foregoing. In further embodiments, the sixth dielectric layer **206**, the seventh dielectric layer **210**, and/or the eighth dielectric layer **212** may be, for example, a low-k dielectric (e.g., a dielectric material with a dielectric constant less than about 3.9), an oxide (e.g., silicon dioxide (SiO.sub.2)), or the like.

[0059] The fourth dielectric structure **130** comprises a ninth dielectric layer **214**, the first dielectric layer **132**, a second outgassing prevention layer **216**, and the second dielectric layer **134**. The first dielectric layer **132** is disposed over the ninth dielectric layer **214**, the second outgassing prevention layer **216** is disposed over the first dielectric layer **132**, and the second dielectric layer **134** is disposed over the second outgassing prevention layer **216**. The second outgassing prevention layer **216** prevents gases (e.g., oxygen, carbon dioxide, or the like) from outgassing from other features of the semiconductor device **100** into the cavities **148**. In some embodiments, the second outgassing prevention layer **216** may be or comprise, for example, a nitride (e.g., SiN), an oxy-nitride (e.g., SiO.sub.XN.sub.Y), some other outgassing prevention material, or a combination of the foregoing. In further embodiments, the ninth dielectric layer **214** may be or comprise, for example, a low-k dielectric (e.g., a dielectric material with a dielectric constant less than about 3.9), an oxide (e.g., silicon dioxide (SiO.sub.2)), or the like.

[0060] In some embodiments, the MEMS substrate **136** comprises a first MEMS structure **217** and a second MEMS structure **218**. The first MEMS structure **217** is disposed over the second MEMS structure **218**. In some embodiments, the first MEMS structure **217** is a semiconductor structure comprising the semiconductor material (e.g., polysilicon, amorphous silicon, monocrystalline

silicon, SiGe, Ge, or the like). In further embodiments, the second MEMS structure **218** comprises one or more dielectric layers, which respectively comprise an oxide (e.g., SiO.sub.2), a nitride (e.g., SiN), or the like. In yet further embodiments, the second MEMS structure **218** may be a single layer of SiO.sub.2. The bond interface may exist at an interface of the second MEMS structure **218** and the second dielectric layer **134**. For example, in some embodiments, the second MEMS structure **218** is bonded to the second dielectric layer **134** via a bonding process (e.g., fusion bonding), thereby forming the bond interface at the interface of the second MEMS structure **218** and the second dielectric layer **134**. In some embodiments, the second dielectric layer **134** may have a thickness between about 0.1 um and about 10 um. In further embodiments, the second MEMS structure **218** may have a thickness between about 0.0005 um and about 1 um.

[0061] An isolation trench **220** is disposed laterally between the fifth conductive via **140***a* and the sixth conductive via **140***b*. In some embodiments, the isolation trench **220** extends vertically through the third dielectric layer **138** and the first MEMS structure **217**. In further embodiments, the isolation trench extends vertically through the MEMS substrate **136**. The isolation trench **220** may extend laterally around the MEMS devices **146** in a closed path. The isolation trench **220** electrically isolates (or increases an electrical resistivity) between the fifth conductive via **140***a* and the sixth conductive via **140***b*. It will be appreciated that, in some embodiments, the isolation trench **220** may be one of a plurality of isolation trenches disposed laterally between the fourth conductive vias **140**, respectively.

[0062] A first passivation layer **222** is disposed over the MEMS substrate **136**, the third dielectric layer **138**, the fourth conductive vias **140**, and the second conductive contacts **144**. In some embodiments, the first passivation layer **222** lines the fourth conductive vias **140**, an upper surface of the third dielectric layer **138**, one or more sidewalls of the third dielectric layer **138**, one or more sidewalls of the first MEMS structure **217**, an upper surface of the second MEMS structure **218**, one or more sidewalls of the second conductive contacts **144**, and upper surfaces of the second conductive contacts **144**. In further embodiments, the first passivation layer **222** may contact an upper surface of the MEMS substrate **136** between the third dielectric layer **138** and the functional structures **152**.

[0063] In some embodiments, the first passivation layer **222** may laterally separate the functional structures **152** from the third dielectric layer **138**. In such embodiments, portions of the first passivation layer **222** may extend vertically from the MEMS substrate **136** between sidewalls of the functional structures **152** and sidewalls of the third dielectric layer **138**. In further such embodiments, the first passivation layer **222** may directly contact the MEMS substrate **136**, the sidewalls of the functional structures **152**, and/or the sidewalls of the third dielectric layer **138**. The first passivation layer **222** may be a conformal layer. In some embodiments, the first passivation layer **222** may be or comprise, for example, an oxide (e.g., SiO.sub.2), a nitride (e.g., SiN), an oxy-nitride (e.g., SiO.sub.XN.sub.Y), some other dielectric material, or a combination of the foregoing. In further embodiments, the first passivation layer **222** has a different chemical composition than the functional structures **152**.

[0064] A second passivation layer **224** may be disposed over the MEMS substrate **136**, the third dielectric layer **138**, the fourth conductive vias **140**, the second conductive contacts **144**, the first passivation layer **222**, and the functional structures **152**. In some embodiments, the second passivation layer **224** lines the first passivation layer **222** and the functional structures **152**. In further embodiments, the second passivation layer **224** may line upper surfaces of the functional structures **152**. The second passivation layer **224** may be or comprise, for example, an oxide (e.g., SiO.sub.2), a nitride (e.g., SiN), an oxy-nitride (e.g., SiO.sub.XN.sub.Y), some other dielectric material, or a combination of the foregoing. In some embodiments, the second passivation layer **224** may have a thickness between about 0.05 um and about 2 um. In further embodiments, the second passivation layer **224** has a different chemical composition than the functional structures **152**.

[0065] One or more gas getter structures **226** may be disposed in the third dielectric structure **124**. In some embodiments, the gas getter structures **226** are disposed over the first outgassing prevention layer **208**. In further embodiments, the gas getter structures **226** are disposed in the eighth dielectric layer **212**. The gas getter structures **226** are configured to absorb and/or consume gases within the cavities **148**. The gas getter structures **226** may be or comprise, for example, Al, Cu, W, Ti, Au, some other suitable gas getter material, or a combination of the foregoing. In yet further embodiments, the gas getter structures **226** and the electrodes **128** comprise a same material. For readability, only some of the gas getter structures **226** are specifically labeled.
[0066] The cavities **148** are at least partially defined by the MEMS substrate **136** and the fourth dielectric structure **130**. In some embodiments, a bottom surface of the first MEMS structure **217** defines upper surfaces of the cavities **148**. In other embodiments, a bottom surface of the second MEMS structure **218** defines upper surfaces of the cavities **148**. In some embodiments, sidewalls of the cavities **148** are defined by sidewalls of the second dielectric layer **134**, the second outgassing prevention layer **216**, the first dielectric layer **132**, and the ninth dielectric layer **214**. In further embodiments, first lower surfaces of the cavities **148** are defined by upper surfaces of the first dielectric layer **132**. In yet further embodiments, second lower surfaces of the cavities **148** are defined by upper surfaces of the gas getter structures **226**. The second lower surfaces of the cavities **148** may be disposed between the first upper surfaces of the cavities **148** and the semiconductor substrate **104**.
[0067] FIG. **3** illustrates a cross-sectional view of some other embodiments of the semiconductor device **100** of FIG. **2**.
[0068] As shown in FIG. **3**, a plurality of fluid communication channels **302** are disposed in the fourth dielectric structure **130**. For readability, only some of the fluid communication channels **302** are specifically labeled. The fluid communication channels **302** extend laterally between the cavities **148**, such that each of the cavities **148** are in fluid communication with one another. In some embodiments, each of the fluid communication channels **302** extend laterally between two neighboring cavities of the cavities **148**, such that each of the cavities **148** are in fluid communication with one another. Because the cavities **148** are in fluid communication with one another, cavity pressures of the cavities **148** (e.g., pressures inside the cavities **148**) are substantially the same. Because the cavity pressures are substantially the same, device performance of the semiconductor device **100** may be improved (e.g., increased transmission/receiving sensitivity).
[0069] For example, the first MEMS device **146***a* and the second MEMS device **146***b* may be a configured to operate in conjunction with one another (e.g., a CMUT configured to operate as an ultrasonic receiver and a PMUT configured to operate as an ultrasonic transmitter). During operation of the first MEMS device **146***a* and the second MEMS device **146***b*, a same operating voltage may be applied to the first MEMS device **146***a* and the second MEMS device **146***b*. As such, a difference in the cavity pressures of the first MEMS device **146***a* and the second MEMS device **146***b* may decrease the transmission sensitivity and/or receiving sensitivity due to the difference in the cavity pressures causing variations in the deflections of the movable membranes **150**. However, because the fluid communication channels **302** extend laterally between the cavities **148**, such that each of the cavities **148** are in fluid communication with one another, the cavity pressures of the cavities **148** are substantially the same. Thus, the fluid communication channels **302** may increase the transmission sensitivity and/or receiving sensitivity of the MEMS devices **146**.
[0070] The fluid communication channels **302** are at least partially defined by the MEMS substrate **136** and the fourth dielectric structure **130**. In some embodiments, a bottom surface of the first MEMS structure **217** defines upper surfaces of the fluid communication channels **302**. In other embodiments, a bottom surface of the second MEMS structure **218** defines upper surfaces of the fluid communication channels **302**. In some embodiments, sidewalls of the fluid communication

channels **302** are defined by sidewalls of the second dielectric layer **134** and the second outgassing prevention layer **216**. In further embodiments, lower surfaces of the fluid communication channels **302** are defined by upper surfaces of the first dielectric layer **132**.

[0071] FIG. **4** illustrates a cross-sectional view of some other embodiments of the semiconductor device **100** of FIG. **2**.

[0072] As shown in FIG. **4**, one or more vent holes **402** are disposed in the MEMS substrate **136**. The vent holes **402** extend vertically through the MEMS substrate **136**, such that the vent holes **402** are in fluid communication with the cavities **148**. In some embodiments, the vent holes **402** are in fluid communication with the cavities **148** and the fluid communication channels **302**. In further embodiments, the vent holes **402** extend vertically through the MEMS substrate **136** and open up into the fluid communication channels **302**, respectively. In other embodiments, the vent holes **402** extend vertically through the MEMS substrate **136** and open up into the cavities **148**, respectively. The vent holes **402** are at least partially defined by the MEMS substrate **136**. For example, sidewalls of the vent holes **402** are at least partially defined by sidewalls of the first MEMS structure **217** and sidewalls of the second MEMS structure **218**. For readability, only some of the vent holes **402** are specifically labeled.

[0073] One or more plugs **404** are disposed over the MEMS substrate **136** and cover the vent holes **402**. For readability, only some of the plugs **404** are specifically labeled. The plugs **404** completely cover the vent holes **402**, respectively. The plugs **404** are configured to hermetically seal the cavities **148** and the vent holes **402** at a reference system pressure. In some embodiments, the plugs **404** are configured to hermetically seal the cavities **148**, the fluid communication channels **302**, and the vent holes **402** at the reference system pressure.

[0074] In some embodiments, the reference system pressure is less than or equal to 2standard atmosphere (atm). In further embodiments, the reference system pressure may be less than 0.1 atm (e.g., for a high-vacuum MEMS device). In yet further embodiments, the reference system pressure may be between 0.5 atm and 2 atm (e.g., for a standard pressure MEMS device). In comparison to a semiconductor device not comprising vent holes **402**, the vent holes **402** allow the cavities **148**, the fluid communication channels **302**, and the vent holes **402** to be hermetically sealed at a lower reference system pressure due to the plugs **404** being able to be formed at a lower pressure than the MEMS substrate **136** can be bonded to the fourth dielectric structure **130**. In some embodiments in which the semiconductor device **100** comprises the vent holes **402** and the plugs **404**, the reference system pressure may be less than 0.1 atm.

[0075] In some embodiments, the plugs **404** may be or comprise, for example, a metal (e.g., Al, Cu, AlCu, Ti, Ag, Au, or the like), a metal nitride (e.g., TiN), an oxide (e.g., SiO.sub.2), a nitride (e.g., SiN), an oxy-nitride (e.g., SiO.sub.XN.sub.Y), a semiconductor material (e.g., amorphous silicon, Ge, etc.), some other suitable material for covering and sealing the vent holes **402**, or a combination of the foregoing. In further embodiments, the plugs **404** may be a same material as the second conductive contacts **144**. In yet further embodiments, the plugs **404** are part of the first MEMS routing structure and/or the second MEMS routing structure.

[0076] FIGS. **5**A-**5**B illustrate various views of some embodiments of an area **406** (see, e.g., FIG. **4**) of the semiconductor device **100** of FIG. **4**. FIG. **5**A illustrates a cross-sectional view of some embodiments of the area **406** of the semiconductor device **100** of FIG. **4**. FIG. **5**B illustrates a cross-sectional view of some embodiments of the area **406** taken along line A-A of FIG. **5**A.

[0077] As shown in FIGS. **5**A-**5**B, the MEMS substrate **136** has a thickness T (e.g., a distance between an uppermost surface of the MEMS substrate **136** and a bottommost surface of the MEMS substrate **136**). The thickness T of the MEMS substrate may be between about 0.1 micrometers (um) and about 50 um. The vent holes **402** each have a minimum dimension D. The minimum dimension D of a given vent hole is a distance between nearest opposite sidewalls of the given vent hole. In some embodiments, the minimum dimension D is between about 0.1 um and about 2 um. In some embodiments in which the MEMS substrate **136** comprises or is a semiconductor material

(e.g., Si), the minimum dimension D is at least twenty times less than the thickness T of the MEMS substrate **136**. In further embodiments, the sidewalls of the vent holes **402** extend downward from an uppermost surface of the MEMS substrate **136** at an angle Θ. The angle Θ may be between about 85 degrees and 95 degrees.

[0078] FIGS. **6**A-**6**B illustrate various views of some other embodiments of the area **406** (see, e.g., FIG. **4**) of the semiconductor device **100** of FIG. **4**. FIG. **6**A illustrates a cross-sectional view of some embodiments of the area **406** of the semiconductor device **100** of FIG. **4**. FIG. **6**B illustrates a cross-sectional view of some embodiments of the area **406** taken along line A-A of FIG. **6**A.

[0079] As shown in FIGS. **6**A-**6**B, a third passivation layer **602** may be disposed over the second passivation layer **224**. In some embodiments, the third passivation layer **602** is disposed over the MEMS substrate **136**, the third dielectric layer **138**, the fourth conductive vias **140**, the second conductive contacts **144**, the first passivation layer **222**, the functional structures **152**, and the second passivation layer **224**. The third passivation layer **602** may be or comprise, for example, an oxide (e.g., SiO.sub.2), a nitride (e.g., SiN), an oxy-nitride (e.g., SiO.sub.XN.sub.Y), some other dielectric material, or a combination of the foregoing. In some embodiments, the third passivation layer **602** may be or comprise a same material as the first passivation layer **222**. For example, the first passivation layer **222** may be an oxide (e.g., SiO.sub.2), the second passivation layer **224** may be a nitride (e.g., SiN), and the third passivation layer **602** may be an oxide (e.g., SiO.sub.2).

[0080] In some embodiments, one or more of the plugs **404** may have a first indentation. The first indentation is disposed along a bottom surface of the one or more plugs **404**. The one or more plugs **404** may have a second indentation that corresponds to the first indentation. The second indentation is disposed along an upper surface of the one or more plugs **404**. In other embodiments, the upper surfaces of the plugs **404** may be substantially planar.

[0081] The first passivation layer **222** may have a third indentation that corresponds to the second indentation. The third indentation is disposed along an upper surface of the first passivation layer **222**. The second passivation layer **224** may have a fourth indentation that corresponds to the third indentation. The fourth indentation is disposed along an upper surface of the second passivation layer **224**. The third passivation layer **602** may have a fifth indentation that corresponds to the fourth indentation. The fifth indentation is disposed along an upper surface of the third passivation layer **602**. In other embodiments, the upper surface of the first passivation layer **222**, the upper surface of the second passivation layer **224**, and/or the upper surface of the third passivation layer **602** may be substantially planar.

[0082] FIG. **7** illustrates a cross-sectional view of some other embodiments of the semiconductor device **100** of FIG. **2**.

[0083] As shown in FIG. **7**, some of the MEMS devices **146** may comprise functional structures **152**, and some other of the MEMS devices **146** may not comprise functional structures **152**. For example, the first MEMS device **146***a* comprises the first functional structure **152***a*, but the second MEMS device **146***b* does not comprise the second functional structure **152***b*. Because the first MEMS device **146***a* comprises the first functional structure **152***a*, the first MEMS device **146***a* may sense (or actuate) based at least in part on a physical property of the first functional structure **152***a* changing in response to a stimulus (e.g., a shape of the first functional structure **152***a* changing in response to a stimulus causing the first movable membrane **150***a* to deflect). Because the second MEMS device **146***b* does not comprise the second functional structure **152***b*, the second MEMS device **146***b* does not rely on a physical property of a respective functional structure changing in repose to a stimulus to sense (or actuate). Rather, the second MEMS device **146***b* may sense (or actuate) based on a stimulus directly causing the second movable membrane **150***b* to deflect (e.g., rather than indirectly deflecting based on a physical property of the respective functional structure causing the second movable membrane **150***b* to deflect). Thus, the first MEMS device **146***a* is a first type of MEMS device and the second MEMS device **146***b* is a second type of MEMS device different than the first type. Accordingly, the semiconductor device **100** comprises different types

of MEMS devices, which may reduce manufacturing costs, reduce packaging sizes, reduce power consumption, etc.

[0084] In some embodiments, the first passivation layer **222** may be vertically spaced from the first movable membrane **150***a* and contact the second movable membrane **150***b*. In further embodiments, the first passivation layer **222** may have a first bottom surface disposed directly over the first movable membrane **150***a* and a second bottom surface disposed directly over the second movable membrane **150***b*. In yet further embodiments, the second bottom surface of the first passivation layer **222** may be disposed between the first bottom surface of the first passivation layer **222** and an upper surface of the first movable membrane.

[0085] In some embodiments, the first functional structure **152***a* may vertically separate the first passivation layer **222** from the first movable membrane **150***a*. In such embodiments, the first passivation layer **222** may line an upper surface of the first functional structure **152***a* directly over the first movable membrane **150***a* and line an upper surface of the second movable membrane **150***b*. In other embodiments, the third dielectric layer **138** may line the upper surface of the second movable membrane **150***b*. In such embodiments, the first passivation layer **222** may line the upper surface of the first functional structure **152***a* directly over the first movable membrane **150***a* and line an upper surface of the third dielectric layer **138** directly over the second movable membrane **150***b*.

[0086] FIG. **8** illustrates a cross-sectional view of some other embodiments of the semiconductor device **100** of FIG. **2**.

[0087] As shown in FIG. **8**, a first doped region **802** and a second doped region **804** are disposed in the MEMS substrate **136**. The first doped region **802** is disposed at least partially in the first movable membrane **150***a*, and the second doped region **804** is disposed at least partially in the second movable membrane **150***b*. In some embodiments, the first doped region **802** and the second doped region **804** are disposed in the first MEMS structure **217**.

[0088] The first doped region **802** has a first doping type (e.g., n-type/p-type) and the second doped region has a second doping type (e.g., n-type/p-type). In some embodiments, the first doping type and the second doping type are the same. In such embodiments, the first doped region **802** has a first doping concentration of first doping type dopants (e.g., phosphorus (n-type), boron (p-type), etc.), and the second doped region **804** has a second doping concertation of the first doping type dopants that is different than the first doping concentration. In other embodiments, the first doping type and the second doping type are the different.

[0089] Also shown in FIG. **8**, the first MEMS device **146***a* does not comprise the first functional structure **152***a* and the second MEMS device **146***b* does not comprise the second functional structure **152***b*. However, because the first doped region **802** is at least partially disposed in the first movable membrane **150***a* and the second doped region **804** is at least partially disposed in the second movable membrane **150***b*, the first MEMS device **146***a* may be a different type of MEMS device than the second MEMS device **146***b*. For example, due to the first doped region **802** having the first doping type (and/or first doping concentration) and the second doped region **804** having the second doping type (and/or second doping concentration), the first MEMS device **146***a* may be configured to transmit (or sense) acoustic waves at a first frequency while the second MEMS device **146***b* is configured to transmit (or sense) acoustic waves at a second frequency different than the first frequency. Thus, the first MEMS device **146***a* is a first type of MEMS device and the second MEMS device **146***b* is a second type of MEMS device different than the first type. Accordingly, the semiconductor device **100** comprises different types of MEMS devices, which may reduce manufacturing costs, reduce packaging sizes, reduce power consumption, etc.

[0090] FIG. **9** illustrates a cross-sectional view of some other embodiments of the semiconductor device **100** of FIG. **2**.

[0091] As shown in FIG. **9**, the first MEMS device **146***a* comprises the first functional structure **152***a* and the first doped region **802** is disposed in the MEMS substrate **136**. The second MEMS

device **146***b* comprises the second functional structure **152***b* and the second doped region **804** is disposed in the MEMS substrate **136**. In some embodiments in which the first doped region **802** and the second doped region **804** are disposed in the MEMS substrate **136**, the second functional structure **152***b* may have a same chemical composition as the first functional structure **152***a*. While the first functional structure **152***a* and the second functional structure **152***b* may have a same chemical composition, the first MEMS device **146***a* and the second MEMS device **146***b* may still be different types of MEMS devices due to the first doped region **802** having the first doping type (and/or first doping concentration) and the second doped region **804** having the second doping type (and/or second doping concentration). In other embodiments in which the first doped region **802** and the second doped region **804** are disposed in the MEMS substrate **136**, the first functional structure **152***a* may have a different chemical composition than the second functional structure **152***b*. It will be appreciated that, in some embodiments, the first MEMS device **146***a* and the second MEMS device **146***b* may be different types of MEMS devices due to the first functional structure **152***a* and the second functional structure **152***b* having different chemical compositions, the first doped region **802** and the second doped region **804** having different doping types (and/or doping concentrations), the first MEMS device **146***a* comprising the first functional structure **152***a* and the second MEMS device not comprising the second functional structure **152***b*, or a combination of the foregoing.

[0092] FIG. **10** illustrates a simplified layout view of some embodiments of the semiconductor device **100** of FIG. **2**. FIG. **10** is "simplified" because various features illustrated in FIG. **2** are not illustrated in FIG. **10**.

[0093] As shown in FIG. **10**, in some embodiments, the first MEMS device **146***a* comprises a first plurality of MEMS cells **1002***a*. The first plurality of MEMS cells **1002***a* comprises a second plurality of cavities **148***c*, respectively. For example, a first MEMS cell **1002***a*.sub.1 of the first plurality of MEMS cells **1002***a* comprises a third cavity **148***c*.sub.1 of the second plurality of cavities **148***c*, and a second MEMS cell **1002***a*.sub.2 of the first plurality of MEMS cells **1002***a* comprises a fourth cavity **148***c*.sub.2 of the second plurality of cavities **148***c*. In some embodiments, the cavities of the second plurality of cavities **148***c* have substantially similar structures as one another.

[0094] The first plurality of MEMS cells **1002***a* comprises a second plurality of movable membranes **150***c*, respectively. For example, the first MEMS cell **1002***a*.sub.1 comprises a third movable membrane **150***c*.sub.1 of the second plurality of movable membranes **150***c*, and the second MEMS cell **1002***a*.sub.2 comprises a fourth movable membrane **150***c*.sub.2 of the second plurality of movable membranes **150***c*. In some embodiments, the movable membranes of the second plurality of movable membranes **150***c* have substantially similar structures (and/or doping types/concentrations) as one another.

[0095] In some embodiments, the first plurality of MEMS cells **1002***a* comprises a first plurality of functional structures **152***c*, respectively. For example, the first MEMS cell **1002***a*.sub.1 comprises a third functional structure **152***c*.sub.1 of the first plurality of functional structures **152***c*, and the second MEMS cell **1002***a*.sub.2 comprises a fourth functional structure **152***c*.sub.2 of the first plurality of functional structures **152***c*. In some embodiments, the functional structures of the first plurality of functional structures **152***c* have substantially similar structures as one another. In further embodiments, each of the functional structures of the first plurality of functional structures **152***c* may have a same chemical composition. In yet further embodiments, each of the functional structures of the first plurality of functional structures **152***c* have a same chemical composition as the first functional structure **152***a*.

[0096] In some embodiments, the first plurality of MEMS cells **1002***a* are configured to operate in conjunction with one another (e.g., in unison). For example, the first MEMS device **146***a* may be a CMUT, and the first plurality of MEMS cells **1002***a* are individual cells of the CMUT. In further embodiments, during operation of the first MEMS device **146***a*, a same operating voltage may be

applied to each of the first plurality of MEMS cells **1002***a*.

[0097] The second MEMS device **146***b* may comprise a second plurality of MEMS cells **1002***b*. The second plurality of MEMS cells **1002***b* comprises a third plurality of cavities **148***d*, respectively. For example, a third MEMS cell **1002***b*.sub.1 of the second plurality of MEMS cells **1002***b* comprises a fifth cavity **148***d*.sub.1 of the third plurality of cavities **148***d*, and a fourth MEMS cell **1002***b*.sub.2 of the second plurality of MEMS cells **1002***b* comprises a sixth cavity **148***d*.sub.2 of the third plurality of cavities **148***d*. In some embodiments, the cavities of the third plurality of cavities **148***d* have substantially similar structures as one another.

[0098] The second plurality of MEMS cells **1002***b* comprises a third plurality of movable membranes **150***d*, respectively. For example, the third MEMS cell **1002***b*.sub.1 comprises a fifth movable membrane **150***d*.sub.1 of the third plurality of movable membranes **150***d*, and the fourth MEMS cell **1002***b*.sub.2 comprises a sixth movable membrane **150***d*.sub.2 of the third plurality of movable membranes **150***d*. In some embodiments, the movable membranes of the third plurality of movable membranes **150***d* have substantially similar structures (and/or doping types/concentrations) as one another.

[0099] In some embodiments, the second plurality of MEMS cells **1002***b* comprises a second plurality of functional structures **152***d*, respectively. For example, the third MEMS cell **1002***b*.sub.1 comprises a fifth functional structure **152***d*.sub.1 of the second plurality of functional structures **152***d*, and the fourth MEMS cell **1002***b*.sub.2 comprises a sixth functional structure **152***d*.sub.2 of the second plurality of functional structures **152***d*. In some embodiments, the functional structures of the second plurality of functional structures **152***d* have substantially similar structures as one another. In further embodiments, each of the functional structures of the second plurality of functional structures **152***d* may have a same chemical composition. In yet further embodiments, each of the functional structures of the second plurality of functional structures **152***d* have a same chemical composition as the second functional structure **152***b*.

[0100] In some embodiments, the second plurality of MEMS cells **1002***b* are configured to operate in conjunction with one another (e.g., in unison). For example, the second MEMS device **146***b* may be a PMUT, and the second plurality of MEMS cells **1002***b* are individual cells of the PMUT. In further embodiments, during operation of the second MEMS device **146***b*, a same operating voltage may be applied to each of the second plurality of MEMS cells **1002***b*.

[0101] FIGS. **11-22** illustrate a series of cross-sectional views of some embodiments of a method for forming some embodiments of the semiconductor device **100** of FIG. **4**.

[0102] As shown in FIG. **11**, an IC structure **102** is provided. The IC structure **102** comprises a semiconductor substrate **104**. One or more IC devices **106** (not shown) are formed on/over the semiconductor substrate **104**. In some embodiments, one or more of the IC devices **106** comprise a pair of source/drain regions **108**, a gate dielectric **110**, and a gate electrode **112**. The IC structure **102** comprises an interconnect structure **114**, a first dielectric structure **116**, a second dielectric structure **119**, a third dielectric structure **124**, a plurality of electrodes **128**, and one or more gas getter structures **226** disposed over the semiconductor substrate **104** and the IC devices **106**. The interconnect structure **114** comprises one or more first conductive contacts **118** (not shown), one or more first conductive vias **120**, one or more first conductive lines **122**, a plurality of second conductive vias **121**, a plurality of second conductive lines **123**, and a plurality of third conductive vias **126**. The second dielectric structure **119** comprises a fourth dielectric layer **202** and a fifth dielectric layer **204**. The third dielectric structure **124** comprises a sixth dielectric layer **206**, a first outgassing prevention layer **208**, a seventh dielectric layer **210**, and an eighth dielectric layer **212**. The IC structure **102** may be formed according to a CMOS manufacturing process.

[0103] Also shown in FIG. **11**, a fourth dielectric structure **130** is formed over the IC structure **102**. In some embodiments, the fourth dielectric structure **130** is formed over the third dielectric structure **124**, the gas getter structures **226**, and the electrodes **128**. The fourth dielectric structure **130** may comprise a ninth dielectric layer **214**, a first dielectric layer **132**, a second outgassing

prevention layer **216**, and a second dielectric layer **134**. The ninth dielectric layer **214** may be formed over the third dielectric structure **124**, the gas getter structures **226**, and the electrodes **128**. The first dielectric layer **132** may be formed over the ninth dielectric layer **214**. The second outgassing prevention layer **216** may be formed over the first dielectric layer **132**. The second dielectric layer **134** may be formed over the second outgassing prevention layer **216**.

[0104] In some embodiments, a process for forming the fourth dielectric structure **130** comprises depositing the ninth dielectric layer **214** on and covering the third dielectric structure **124**, the gas getter structures **226**, and the electrodes **128**. The ninth dielectric layer **214** may be deposited by, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), some other deposition process, or a combination of the foregoing. Thereafter, the first dielectric layer **132** is deposited over the ninth dielectric layer **214**. The first dielectric layer **132** may be deposited by, for example, CVD, PVD, ALD, some other deposition process, or a combination of the foregoing.

[0105] The second outgassing prevention layer **216** is then deposited over the first dielectric layer **132**. The second outgassing prevention layer **216** may be deposited by, for example, CVD, PVD, ALD, some other deposition process, or a combination of the foregoing. Thereafter, the second dielectric layer **134** is deposited over the second outgassing prevention layer **216**. The second dielectric layer **134** may be deposited by, for example, CVD, PVD, ALD, some other deposition process, or a combination of the foregoing. In some embodiments, the second dielectric layer **134** may be deposited with a thickness between about 0.1 um to about 10 um. In further embodiments, the ninth dielectric layer **214**, the first dielectric layer **132**, the second outgassing prevention layer **216**, and/or the second dielectric layer **134** may be formed as conformal layers.

[0106] As shown in FIG. **12**, a first plurality of openings **1202** are formed over the second dielectric structure **119**. The first plurality of openings **1202** are formed laterally spaced from one another. In some embodiments, the first plurality of openings **1202** are formed at least partially in the third dielectric structure **124** and at least partially in the fourth dielectric structure **130**. In further embodiments, the first plurality of openings **1202** expose one or more of the second conductive lines **123**. For example, in some embodiments, a first opening **1202***a* of the first plurality of openings **1202** exposes the third conductive line **123***a*, and a second opening **1202***b* of the first plurality of openings **1202** exposes the fourth conductive line **123***b*.

[0107] In some embodiments, a process for forming the first plurality of openings **1202** comprises forming a first patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) over the fourth dielectric structure **130**. In further embodiments, the first patterned masking layer may be formed by forming a masking layer (not shown) on the fourth dielectric structure **130**, exposing the masking layer to a pattern (e.g., via a lithography process, such as photolithography, extreme ultraviolet lithography, or the like), and developing the masking layer to form the first patterned masking layer. Thereafter, a first etching process is performed to remove unmasked portions of the fourth dielectric structure **130** and the third dielectric structure **124**, thereby forming the first plurality of openings **1202** over the second dielectric structure **119**. The first etching process may be a dry etching process, a wet etching process, a reactive ion etching (RIE) process, some other etching process, or a combination of the foregoing. Subsequently, in some embodiments, the first patterned masking layer is stripped away.

[0108] As shown in FIG. **13**, a plurality of cavity openings **1302** and a plurality of fluid communication channel openings **1304** are formed over the IC structure **102**. The cavity openings **1302** and the fluid communication channel openings **1304** are formed in the fourth dielectric structure **130**. In some embodiments, the cavity openings **1302** and the fluid communication channel openings **1304** are defined at least partially by the first dielectric layer **132**, the second dielectric layer **134**, and the second outgassing prevention layer **216**.

[0109] The cavity openings **1302** are formed laterally spaced from one another. The cavity openings **1302** are formed over the electrodes **128**, respectively. For example, a first cavity opening

1302*a* of the cavity openings **1302** is formed over the first electrode **128***a*, and a second cavity opening **1302***b* of the cavity openings **1302** is formed over the second electrode **128***b*. The fluid communication channel openings **1304** are formed extending laterally between the cavity openings **1302**, such that opposite ends of the fluid communication channel openings **1304** open up into corresponding cavity openings of the cavity openings **1302**. In some embodiments, each of the fluid communication channel openings **1304** are formed extending laterally between two neighboring cavity openings of the cavity openings **1302**, such that the opposite ends of each of the fluid communication channel openings **1304** open up into two neighboring cavity openings of the cavity openings **1302**.

[0110] In some embodiments, a process for forming the cavity openings **1302** and the fluid communication channel openings **1304** comprises forming a second patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) over the fourth dielectric structure **130**, over the second conductive lines **123**, and in the first plurality of openings **1202**. Thereafter, a second etching process is performed to remove unmasked portions of the second dielectric layer **134** and the second outgassing prevention layer **216**, thereby forming the cavity openings **1302** and the fluid communication channel openings **1304** in the fourth dielectric structure **130**. The second etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. Subsequently, in some embodiments, the second patterned masking layer is stripped away.

[0111] As shown in FIG. **14**, portions of the fourth dielectric structure **130** are removed to at least partially expose the gas getter structures **226**. In some embodiments, portions of the first dielectric layer **132** and portions of the ninth dielectric layer **214** are removed to at least partially expose the gas getter structures **226**. In some embodiments, a process for removing the portions of the fourth dielectric structure **130** to at least partially expose the gas getter structures **226** comprises forming a third patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) over the fourth dielectric structure **130**, over the second conductive lines **123**, in the first plurality of openings **1202**, in the cavity openings **1302**, and in the fluid communication channel openings **1304**. Thereafter, a third etching process is performed to remove unmasked portions of the fourth dielectric structure **130**, thereby at least partially exposing the gas getter structures **226**. The third etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. Subsequently, in some embodiments, the third patterned masking layer is stripped away.

[0112] As shown in FIG. **15**, a MEMS substrate **136** is bonded to the fourth dielectric structure **130**. By bonding the MEMS substrate **136** to the fourth dielectric structure **130**, a plurality of cavities **148** and a plurality of fluid communication channels **302** are formed over the IC structure **102**. For example, once the MEMS substrate **136** is bonded to the fourth dielectric structure **130**, the MEMS substrate **136** completely covers the cavity openings **1302** and the fluid communication channel openings **1304** (see, e.g., FIG. **14**), thereby forming the plurality of cavities **148** and the plurality of fluid communication channels **302**, respectively. In some embodiments, bonding the MEMS substrate **136** to the fourth dielectric structure **130** covers the first plurality of openings **1202**.

[0113] In some embodiments, the MEMS substrate **136** is bonded to the fourth dielectric structure **130** via a fusion bonding process. It will be appreciated that other types of bonding process (e.g., eutectic bonding) may be utilized to bond the MEMS substrate **136** to the fourth dielectric structure **130**. In further embodiments, the MEMS substrate **136** is bonded to the second dielectric layer **134**.

[0114] The MEMS substrate **136** may comprise a first MEMS structure **217** and a second MEMS structure **218**. In some embodiments, the first MEMS structure **217** may be bonded to the fourth dielectric structure **130**. In other embodiments, the MEMS substrate **136** may not comprise the second MEMS structure **218**. In such embodiments, the first MEMS structure **217** may be bonded to the fourth dielectric structure **130**.

[0115] In some embodiments, a third dielectric layer **138** is disposed over a side of the MEMS

substrate **136** that is opposite the side of the MEMS substrate **136** that is bonded to the fourth dielectric structure **130**. The third dielectric layer **138** may be disposed over the side of the MEMS substrate **136** before the MEMS substrate **136** is bonded to the fourth dielectric structure **130**. In other embodiments, the third dielectric layer **138** may be formed over the MEMS substrate **136** and the IC structure **102** after the MEMS substrate **136** is bonded to the third dielectric layer **138**. In further embodiments, a process for forming the third dielectric layer **138** over the MEMS substrate **136** and the IC structure **102** comprises depositing or growing the third dielectric layer **138** on the MEMS substrate **136** by, for example, CVD, PVD, ALD, thermal oxidation, some other deposition or growth process, or a combination of the foregoing.

[0116] As shown in FIG. **16**, a second plurality of openings **1602** are formed over the MEMS substrate **136**. The second plurality of openings **1602** are formed in the third dielectric layer **138**. In some embodiments, the second plurality of openings **1602** are part of one or more trenches that are disposed in the third dielectric layer **138** and extend over the MEMS substrate **136**. For readability, only some of the second plurality of openings **1602** are specifically labeled.

[0117] In some embodiments, a process for forming the second plurality of openings **1602** comprises forming a fourth patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) over the third dielectric layer **138**. Thereafter, a fourth etching process is performed to remove unmasked portions of the third dielectric layer **138**, thereby forming the second plurality of openings **1602**. The fourth etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. Subsequently, in some embodiments, the fourth patterned masking layer is stripped away.

[0118] As shown in FIG. **17**, a plurality of via openings **142** are formed extending vertically through the third dielectric layer **138**, the MEMS substrate **136**, the fourth dielectric structure **130**, and the third dielectric structure **124**. The via openings **142** expose one or more of the second conductive lines **123**. For example, in some embodiments, a first via opening **142***a* of the plurality of via openings **142** exposes the third conductive line **123***a*, and a second via opening **142***b* of the plurality of via openings **142** exposes the fourth conductive line **123***b*.

[0119] In some embodiments, a process for forming the via openings **142** comprises forming a fifth patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) over the third dielectric layer **138** and in some of the second plurality of openings **1602**. The fifth patterned masking layer at least partially exposes some other of the second plurality of openings **1602**. The openings of the second plurality of openings **1602** that are at least partially exposed by the fifth patterned masking layer correspond to the locations in which the via openings **142** are formed. Thereafter, a fifth etching process is performed to remove unmasked portions of the MEMS substrate **136**, thereby forming the via openings **142**. The unmasked portions of the MEMS substrate **136** that are removed to form the via openings **142** overlie the first plurality of openings **1202** (see, e.g., FIG. **16**), respectively. In other words, the first plurality of openings **1202** are exposed by removing the unmasked portions of the MEMS substrate **136**. The fifth etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. Subsequently, in some embodiments, the fifth patterned masking layer may be stripped away. It will be appreciated that, in some embodiments, the fifth patterned masking layer may not expose the some other of the second plurality of openings **1602**, but rather expose portions of the third dielectric layer **138**. In such embodiments, the fifth etching process removes unmasked portions of the third dielectric layer **138** and the unmasked portions of the MEMS substrate **136**, thereby forming the via openings **142**.

[0120] Also shown in FIG. **17**, one or more vent holes **402** are formed extending vertically through the MEMS substrate **136**. In some embodiments, the vent holes **402** are formed extending vertically through the MEMS substrate **136** and opening up into the fluid communication channels **302**, respectively. In other embodiments, the vent holes **402** may be formed extending vertically through the MEMS substrate **136** and opening up into the cavities **148**, respectively.

[0121] In some embodiments, a process for forming the vent holes **402** comprises forming a sixth patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) over the third dielectric layer **138** and in some of the second plurality of openings **1602**. The sixth patterned masking layer at least partially exposes some other of the second plurality of openings **1602**. The openings of the second plurality of openings **1602** that are at least partially exposed by the sixth patterned masking layer correspond to the locations in which the vent holes **402** are formed. Thereafter, a sixth etching process is performed to remove unmasked portions of the MEMS substrate **136**, thereby forming the vent holes **402**. The sixth etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. Subsequently, in some embodiments, the sixth patterned masking layer may be stripped away. It will be appreciated that, in some embodiments, the fifth etching process may form the vent holes **402**. It will be appreciated that, in some embodiments, the sixth patterned masking layer may not expose some other of the second plurality of openings **1602**, but rather expose portions of the third dielectric layer **138**. In such embodiments, the sixth etching process (or the fifth etching process) removes unmasked portions of the third dielectric layer **138** and the unmasked portions of the MEMS substrate **136**, thereby forming the vent holes **402**.
[0122] As shown in FIG. **18**, a plurality of fourth conductive vias **140**, a plurality of second conductive contacts **144**, and one or more plugs **404** are formed over the MEMS substrate **136**. The fourth conductive vias **140** are formed extending vertically through the third dielectric layer **138**, the MEMS substrate **136**, the fourth dielectric structure **130**, and the third dielectric structure **124** to contact a corresponding one of the second conductive lines **123**. For example, a fifth conductive via **140***a*, which is one of the fourth conductive vias **140**, is formed extending vertically through the third dielectric layer **138**, the MEMS substrate **136**, the fourth dielectric structure **130**, and the third dielectric structure **124** to contact the third conductive line **123***a*. A sixth conductive via **140***b*, which is one of the fourth conductive vias **140**, is formed extending vertically through the third dielectric layer **138**, the MEMS substrate **136**, the fourth dielectric structure **130**, and the third dielectric structure **124** to contact the fourth conductive line **123***b*.
[0123] The second conductive contacts **144** are formed extending through the third dielectric layer **138** and contacting the MEMS substrate **136**. The plugs **404** are formed extending through the third dielectric layer **138** and contacting the MEMS substrate **136**. By forming the plugs **404**, the cavities **148** and the fluid communication channels **302** are hermetically sealed at a reference system pressure (e.g., less than or equal to 2 atm). In some embodiments in which the vent holes **402** are formed, the reference system pressure may be less than 0.1 atm (e.g., for a high-vacuum MEMS device). It will be appreciated that, in some embodiments in which the vent holes **402** are not formed, the cavities **148** and the fluid communication channels **302** may be hermetically sealed by bonding the MEMS substrate **136** to the fourth dielectric structure **130**.
[0124] In some embodiments, a process for forming the fourth conductive vias **140**, the second conductive contacts **144**, and the plugs **404** comprises depositing a conductive layer (not shown) over the third dielectric layer **138**, over the second conductive lines **123**, in the via openings **142**, and in the second plurality of openings **1602**. In further embodiments, the conductive layer is deposited at least partially in the vent holes **402**. The conductive layer may be, for example, a metal (e.g., Al, Cu, AlCu, Ti, Ag, Au, or the like), a metal nitride (e.g., TiN), some other conductive material, or a combination of the foregoing. The conductive layer may be deposited by, for example, CVD, PVD, ALD, electroless plating, electrochemical plating, some other deposition process, or a combination of the foregoing. In some embodiments, the conductive layer may be deposited as a conformal layer. In further embodiments, the conductive layer may be formed having a thickness between about 0.05 um and about 1 um.
[0125] A seventh patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) is then formed over the conductive layer. A seventh etching process is then performed on the conductive layer to remove unmasked portions of the conductive layer, thereby

forming the fourth conductive vias **140**, the second conductive contacts **144**, and the plugs **404**. The seventh etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. Subsequently, in some embodiments, the sixth masking layer is stripped away.

[0126] It will be appreciated that, in some embodiments, rather than performing the seventh etching process, a planarization process (e.g., chemical-mechanical polishing (CM P)) may be performed on the conductive layer, thereby forming the fourth conductive vias **140**, the second conductive contacts **144**, and the plugs **404**. It will further be appreciated that, in some embodiments, the seventh patterned masking layer may be formed before the conductive layer is deposited. In such embodiments, after the conductive layer is deposited, a planarization process (e.g., (CM P)) may be performed on the conductive layer, thereby forming the fourth conductive vias **140**, the second conductive contacts **144**, and the plugs **404**.

[0127] It will further be appreciated that, in some embodiments, the fourth conductive vias **140**, the second conductive contacts **144**, and/or the plugs **404** may be formed by different deposition/etching/planarizing process(es). For example, in some embodiments, the plugs **404** comprise a different material than the fourth conductive vias **140** and the second conductive contacts **144**. In such embodiments, the plugs **404** may be formed before (or after) the fourth conductive vias **140** and the second conductive contacts **144** are formed. In further such embodiments, a process for forming the plugs **404** may comprise depositing or growing a plug material layer (not shown) over the third dielectric layer **138**, over the second conductive lines **123**, in the via openings **142**, in the second plurality of openings **1602**, and at least partially in the vent holes **402**.

[0128] Thereafter, an eighth patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) is formed over the plug material layer. A n eighth etching process is then performed to remove unmasked portions of the plug material layer, thereby forming the plugs **404**. The plug material layer may be, for example, a metal (e.g., Al, Cu, AlCu, Ti, Ag, Au, or the like), a metal nitride (e.g., TiN), an oxide (e.g., SiO.sub.2), a nitride (e.g., SiN), an oxy-nitride (e.g., SiO.sub.XN.sub.Y), a semiconductor material (e.g., amorphous silicon, Ge, etc.), some other suitable material for covering and sealing the vent holes **402**, or a combination of the foregoing. The plug material layer may be deposited or grown by, for example, CVD, PVD, ALD, epitaxy, electroless plating, electrochemical plating, some other deposition process, or a combination of the foregoing. The eighth etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. Subsequently, in some embodiments, the eighth patterned masking layer is stripped away.

[0129] As shown in FIG. **19**, a third plurality of openings **1902** are formed over the MEMS substrate **136**. The third plurality of openings **1902** are formed directly over the cavities **148**, respectively. For example, a third opening **1902***a* of the third plurality of openings **1902** is formed directly over the first cavity **148***a*, and a fourth opening **1902***b* of the third plurality of openings **1902** is formed directly over the second cavity **148***b*. In some embodiments, the plugs **404** (and/or the second conductive contacts **144**) separate the third plurality of openings **1902** from one another.

[0130] In some embodiments, a process for forming the third plurality of openings **1902** comprises forming a ninth patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) over the third dielectric layer **138**, the fourth conductive vias **140**, the second conductive contacts **144**, and the plugs **404**. Thereafter, a ninth etching process is performed to remove unmasked portions of the third dielectric layer **138**, thereby forming the third plurality of openings **1902**. The ninth etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. Subsequently, the ninth patterned masking layer may be stripped away.

[0131] Also shown in FIG. **19**, an isolation trench **220** is formed laterally between the fifth conductive via **140***a* and the sixth conductive via **140***b*. The isolation trench **220** is formed

extending vertically through the third dielectric layer **138** and into the MEMS substrate **136**. In some embodiments, a process for forming the isolation trench **220** comprises forming a tenth patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) over the third dielectric layer **138**, the fourth conductive vias **140**, the second conductive contacts **144**, the plugs **404**, and in the third plurality of openings **1902**. Thereafter, a tenth etching process is performed to remove unmasked portions of the third dielectric layer **138** and unmasked portions of the MEMS substrate **136**, thereby forming the isolation trench **220**. Subsequently, the tenth patterned masking layer may be stripped away. In some embodiments, the tenth etching process removes unmasked portions of the first MEMS structure **217** and stops at unmasked portions of the second MEMS structure **218**. The tenth etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. It will be appreciated that, in some embodiments, the isolation trench **220** may be at least partially formed by the ninth etching process.

[0132] As shown in FIG. **20**, a first passivation layer **222** is formed over the third dielectric layer **138**, the fourth conductive vias **140**, the second conductive contacts **144**, the plugs **404**, the first MEMS structure **217**, and the second MEMS structure **218**. In some embodiments, the first passivation layer **222** is formed lining the fourth conductive vias **140**, the second conductive contacts **144**, the plugs **404**, the isolation trench **220**, and the third plurality of openings **1902**. In further embodiments, a process for forming the first passivation layer **222** comprises depositing the first passivation layer **222** over the third dielectric layer **138**, the fourth conductive vias **140**, the second conductive contacts **144**, the plugs **404**, and the MEMS substrate **136**. The first passivation layer **222** may be deposited by, for example, CVD, PVD, ALD, some other deposition process, or a combination of the foregoing. In some embodiments, the first passivation layer **222** may be deposited as a conformal layer.

[0133] As shown in FIG. **21**, functional structures **152** are formed over the MEMS substrate **136**. The functional structures **152** are formed in the third plurality of openings **1902** (see, e.g., FIG. **20**), respectively. For example, a first functional structure **152***a* of the functional structures **152** is formed in the third opening **1902***a* (see, e.g., FIG. **20**), and a second functional structure **152***b* of the functional structures **152** is formed in the fourth opening **1902***b* (see, e.g., FIG. **20**). In some embodiments, the functional structures **152** are formed on the first MEMS structure **217**. In further embodiments, the functional structures **152** are formed with bottommost surfaces that are substantially co-planar.

[0134] In some embodiments, a process for forming the functional structures **152** comprises forming an eleventh patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) over the first passivation layer **222**. Thereafter, an eleventh etching process is performed to remove unmasked portions of the first passivation layer **222**. The unmasked portions of the first passivation layer **222** that are removed by the eleventh etching process are disposed in the third plurality of openings **1902** (see, e.g., FIG. **20**). The eleventh etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. In some embodiments, removing the unmasked portions of the first passivation layer **222** exposes portions of the MEMS substrate **136**. Subsequently, the eleventh patterned masking layer may be stripped away.

[0135] A first functional material layer (not shown) is then deposited over the first passivation layer **222** and over the MEMS substrate **136**. The first functional material layer may be or comprise, for example, a piezoelectric material (e.g., molybdenum (Mo), lead zirconate titanate (PZT), aluminum nitride (AlN), zinc oxide (ZnO), etc), a biosensitive material (e.g., a bio-recognition component disposed on (or part of) a metal (e.g., Au, Ag, platinum (Pt), etc.)), an IR sensitive material (e.g., vanadium oxide (VOx), mercury cadmium telluride (HgCdTe), silicon (Si), cadmium zinc telluride (CdZnTe), etc.), a polymer (e.g., polyimide, SU-8, negative/positive photoresist, etc.), or the like. The first functional material layer may be deposited by, for example, CVD, PVD, ALD, electroless

plating, electrochemical plating, some other deposition process, or a combination of the foregoing.
[0136] Thereafter, a twelfth patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) is formed over the first functional material layer. A twelfth etching process is then performed to remove unmasked portions of the first functional material layer, thereby forming the first functional structure **152***a*. The first functional structure **152***a* is a portion of the first functional material layer not removed by the twelfth etching process. The twelfth etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. Subsequently, the twelfth patterned masking layer may be stripped away.
[0137] In some embodiments, the first functional material layer may be formed as a conformal layer. In further embodiments, the first functional material layer may be formed having a thickness between about 0.0005 um and about 50 um. More specifically, if the first functional material layer is a polymer, the first functional material layer may be formed having a thickness between about 0.0005 um and about 10 um; if the first functional material layer is an IR sensitive material, the first functional material layer may be formed having a thickness between about 0.1 um and about 0.2 um; and if the first functional material layer is a piezoelectric material, the first functional material layer may be formed having a thickness between about 0.05 um and about 50 um.
[0138] After the first functional structure **152***a* is formed, a second functional material layer (not shown) is deposited over the first passivation layer **222**, over the MEMS substrate **136**, and over the first functional structure **152***a*. The second functional material layer may be or comprise, for example, a piezoelectric material (e.g., molybdenum (Mo), lead zirconate titanate (PZT), aluminum nitride (AlN), zinc oxide (ZnO), etc), a biosensitive material (e.g., a bio-recognition component disposed on (or part of) a metal (e.g., Au, Ag, platinum (Pt), etc.)), an IR sensitive material (e.g., vanadium oxide (VOx), mercury cadmium telluride (HgCdTe), silicon (Si), cadmium zinc telluride (CdZnTe), etc.), a polymer (e.g., polyimide, SU-8, negative/positive photoresist, etc.), or the like. The second functional material layer may be deposited by, for example, CVD, PVD, ALD, electroless plating, electrochemical plating, some other deposition process, or a combination of the foregoing. In some embodiments, the second functional material layer is a different material than the first functional material layer.
[0139] Thereafter, a thirteenth patterned masking layer (not shown) (e.g., positive/negative photoresist, hardmask, etc.) is formed over the second functional material layer. A thirteenth etching process is then performed to remove unmasked portions of the second functional material layer, thereby forming the second functional structure **152***b*. The second functional structure **152***b* is a portion of the second functional material layer not removed by the thirteenth etching process. The thirteenth etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. Subsequently, the thirteenth patterned masking layer may be stripped away.
[0140] In some embodiments, the second functional material layer may be formed as a conformal layer. In further embodiments, the second functional material layer may be formed having a thickness between about 0.0005 um and about 50 um. More specifically, if the second functional material layer is a polymer, the second functional material layer may be formed having a thickness between about 0.0005 um and about 10 um; if the second functional material layer is an IR sensitive material, the second functional material layer may be formed having a thickness between about 0.1 um and about 0.2 um; and if the second functional material layer is a piezoelectric material, the second functional material layer may be formed having a thickness between about 0.05 um and about 50 um. It will be appreciated that, in some embodiments, the second functional structure **152***b* may be formed before the first functional structure **152***a*.
[0141] In some embodiments, after the functional structures **152** are formed, formation of a plurality of MEMS devices **146** is complete. The MEMS devices **146** comprise the cavities **148**, movable membranes **150**, and the functional structures **152**, respectively. For example, a first

MEMS device **146***a* of the MEMS devices **146** comprises the first cavity **148***a*, a first movable membrane **150***a* of the movable membranes **150**, and the first functional structure **152***a*, and a second MEMS device **146***b* of the MEMS devices **146** comprises the second cavity **148***b*, a second movable membrane **150***b* of the movable membranes **150**, and the second functional structure **152***b*.

[0142] The first MEMS device **146***a* and the second MEMS device **146***b* are different types of MEMS devices. For example, in some embodiments, the second functional material layer is a different material than the first functional material layer. Thus, the first MEMS device **146***a* and the second MEMS device **146***b* are formed with different configurations due a difference in the chemical compositions of the first functional structure **152***a* and the second functional structure **152***b*. Accordingly, the first MEMS device **146***a* and the second MEMS device **146***b* may be different types of MEMS devices (e.g., IR detection sensor and a PMUT). Because the first MEMS device **146***a* and the second MEMS device **146***b* are different types of MEMS devices, manufacturing costs may be reduced, packaging sizes may be reduced, power consumption may be reduced, etc. It will be appreciated that differences in configurations between different types of MEMS devices is not limited to a difference in the chemical compositions of the functional structure, rather other types of differences may exist between the different types of MEMS devices, such as differences in doping concentrations of the movable membrane, the presence versus absence of the functional structure, etc.

[0143] As shown in FIG. **22**, a second passivation layer **224** is formed over the first passivation layer **222** and the functional structures **152**. In some embodiments, a process for forming the second passivation layer **224** comprises depositing the second passivation layer **224** over the first passivation layer **222** and the functional structures **152**. The second passivation layer **224** may be deposited by, for example, CVD, PVD, ALD, some other deposition process, or a combination of the foregoing. In some embodiments, the second passivation layer **224** may be formed as a conformal layer. In further embodiments, the second passivation layer **224** may be formed with a thickness between about 0.05 um and about 2 um.

[0144] Also shown in FIG. **22**, in some embodiments, a portion of the first passivation layer **222** disposed over the fifth conductive via **140***a* and a portion of the second passivation layer **224** disposed over the fifth conductive via **140***a* may be removed. In some embodiments, a process for removing the portion of the first passivation layer **222** and the portion of the second passivation layer **224** that are disposed over the fifth conductive via **140***a* comprises forming a fourteenth patterned masking layer over the second passivation layer **224**.

[0145] Thereafter, a fourteenth etching process is performed to remove an unmasked portion of the second passivation layer **224** and an unmasked portion of the first passivation layer **222**, thereby removing the portion of the first passivation layer **222** and the portion of the second passivation layer **224** that are disposed over the fifth conductive via **140***a*. The fourteenth etching process may be a dry etching process, a RIE process, a wet etching process, some other etching process, or a combination of the foregoing. Subsequently, the fourteenth patterned masking layer may be stripped away. In some embodiments, after the second passivation layer **224** is formed, formation of the semiconductor device **100** is complete.

[0146] FIG. **23** illustrates a flowchart of some embodiments of a method for forming a semiconductor device comprising different types of microelectromechanical system (MEMS) devices. While the flowchart **2300** of FIG. **23** is illustrated and described herein as a series of acts or events, it will be appreciated that the illustrated ordering of such acts or events is not to be interpreted in a limiting sense. For example, some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein. Further, not all illustrated acts may be required to implement one or more aspects or embodiments of the description herein, and one or more of the acts depicted herein may be carried out in one or more separate acts and/or phases.

[0147] At act **2302**, a dielectric structure is formed over an integrated circuit (IC) structure, where the IC structure comprises an interconnect structure disposed over a semiconductor substrate. FIG. **11** illustrates a cross-sectional view of some embodiments corresponding to act **2302**.
[0148] At act **2304**, a plurality of cavity openings are formed over the semiconductor substrate and in the dielectric structure. FIGS. **12-13** illustrate a series of cross-sectional views of some embodiments corresponding to act **2304**.
[0149] At act **2306**, a microelectromechanical system (MEMS) substrate is bonded to the dielectric structure, where bonding the MEMS substrate to the dielectric structure covers the cavity openings, thereby forming a plurality of cavities over the semiconductor substrate. FIGS. **14-15** illustrate a series of cross-sectional views of some embodiments corresponding to act **2306**.
[0150] At act **2308**, a plurality of conductive vias and a plurality of conductive contacts are formed over the MEMS substrate, where the conductive vias extend vertically through the MEMS substrate and the dielectric structure so that the conductive vias are electrically coupled to interconnect structure. FIGS. **16-18** illustrate a series of cross-sectional views of some embodiments corresponding to act **2308**.
[0151] At act **2310**, a first MEMS device is formed over the semiconductor substrate, where forming the first MEMS device comprises forming a first functional structure over the MEMS substrate and over a first cavity of the cavities. FIGS. **19-21** illustrate a series of cross-sectional views of some embodiments corresponding to act **2310**.
[0152] At act **2312**, a second MEMS device is formed over the semiconductor substrate and laterally spaced from the first MEMS device, where forming the second MEMS device comprises forming a second functional structure over the MEMS substrate and over a second cavity of the cavities, and where the second MEMS device is a different type of MEMS device than the first MEMS device. FIGS. **19-21** illustrate a series of cross-sectional views of some embodiments corresponding to act **2312**.
[0153] At act **2314**, a passivation layer is formed over the MEMS substrate, the first functional structure, the second functional structure, the conductive vias, and the conductive contacts. FIG. **22** illustrates a cross-sectional view of some embodiments corresponding to act **2314**.
[0154] In some embodiments, the present application provides a semiconductor device. The semiconductor device comprises an interconnect structure disposed over a semiconductor substrate. A first dielectric structure is disposed over the interconnect structure. A first cavity is disposed in the first dielectric structure. A second cavity is disposed in the first dielectric structure and laterally spaced from the first cavity. A microelectromechanical (MEMS) substrate is disposed over the first dielectric structure, where the MEMS substrate comprises a first movable membrane overlying the first cavity and a second movable membrane overlying the second cavity. A first functional structure overlies the first movable membrane and the first cavity, where the first functional structure comprises a first material having a first chemical composition. A second functional structure overlies the second movable membrane and the second cavity, where the second functional structure is laterally spaced from the first functional structure, and where the second functional structure comprises a second material having a second chemical composition different than the first chemical composition.
[0155] In some embodiments, the present application provides a semiconductor device. The semiconductor device comprises an interconnect structure disposed over a semiconductor substrate. A dielectric structure is disposed over the interconnect structure. A first cavity is disposed in the dielectric structure. A second cavity is disposed in the dielectric structure and laterally spaced from the first cavity. A microelectromechanical (MEMS) substrate is disposed over the dielectric structure, where the MEMS substrate comprises a first movable membrane overlying the first cavity and a second movable membrane overlying the second cavity. A sensing structure overlies the first movable membrane and the first cavity, where a physical property of the sensing structure changes in response to an external stimulus. A passivation layer is disposed over the MEMS

substrate, where the sensing structure vertical separates a first bottom surface of the passivation layer from an upper surface of the first movable membrane, and where a second bottom surface of the passivation layer overlies the second movable membrane and is disposed vertically between the first bottom surface and the upper surface of the first movable membrane.

[0156] In some embodiments, the present application provides a method for forming a semiconductor device. The method comprises receiving an integrated circuit (IC) structure, where the IC structure comprises an interconnect structure disposed over a semiconductor substrate of the IC structure. A dielectric structure is formed over the interconnect structure. A first opening is formed in the dielectric structure. A second opening is formed in the dielectric structure and laterally spaced from the first opening. A microelectromechanical (MEMS) substrate is bonded to the dielectric structure, where bonding the MEMS substrate to the dielectric structure covers the first opening and the second opening, thereby forming a first cavity and a second cavity, respectively. A first functional structure is formed over the MEMS substrate and overlying the first cavity. A second functional structure is formed over the MEMS substrate and overlying the second cavity, wherein the second functional structure has a different chemical composition than the first functional structure.

[0157] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1. An integrated chip, comprising: a first movable element overlying a first substrate; a second movable element overlying the first substrate; a first functional layer on the first movable element, wherein the first functional layer comprises a first material different from a material of the first movable element; and a second functional layer on the second movable element.

2. The integrated chip of claim 1, wherein the second functional layer comprises a second material different from the first material.

3. The integrated chip of claim 1, wherein the first functional layer is laterally offset from the second functional layer by a non-zero distance.

4. The integrated chip of claim 1, wherein the first functional layer is laterally aligned with a central region of the first movable element, and wherein a vertical distance between the first functional layer and the first movable element is zero.

5. The integrated chip of claim 1, wherein the first functional layer comprises a first outer sidewall facing a second outer sidewall of the second functional layer, wherein the first outer sidewall is laterally offset from the second outer sidewall by a non-zero distance, and wherein the first function layer is discrete from the second functional layer.

6. The integrated chip of claim 1, wherein a first thickness of the first functional layer is different from a second thickness of the second function layer, and wherein the first thickness and the second thickness are less than thicknesses of the first movable element and the second movable element.

7. The integrated chip of claim 1, wherein the first movable element and the second movable element are part of a second substrate, wherein the first movable element overlies a first cavity and the second movable element overlies a second cavity, wherein the integrated chip further comprises: a dielectric structure under the second substrate and between the first cavity and the second cavity; and a vent hole arranged in the second substrate and directly between the first

movable element and the second movable element, wherein a top of the vent hole is below top surfaces of the first and second functional layers.

8. The integrated chip of claim 7, further comprising: a lateral channel in the dielectric structure and fluidly connecting the first cavity to the second cavity, wherein the vent hole overlies and is coupled to the lateral channel; and a plug overlying and sealing the vent hole, wherein the first functional layer and the second function layer contact the plug.

9. An integrated chip, comprising: a dielectric structure over a first substrate; a first cavity in the dielectric structure; a second cavity in the dielectric structure and adjacent to the first cavity; a second substrate over the dielectric structure, wherein the second substrate comprises a first deflectable element over the first cavity and a second deflectable element over the second cavity; a first functional layer on the first deflectable element; and a second functional layer on the second deflectable element, wherein top surfaces of the first and second functional layers are above a top surface of the second substrate.

10. The integrated chip of claim 9, wherein the second functional layer is distinct from the second substrate.

11. The integrated chip of claim 9, wherein the first cavity and the second cavity are sealed at a first pressure.

12. The integrated chip of claim 9, wherein the first functional layer comprises a first material and the second function layer comprises a second material different from the first material.

13. The integrated chip of claim 12, wherein the first material is a metal and the second material is a non-metal.

14. The integrated chip of claim 12, wherein the first material and the second material are different from a material of the second substrate.

15. The integrated chip of claim 9, wherein a thickness of the first functional layer and a thickness of the second functional layer are each less than a thickness of the second substrate.

16. The integrated chip of claim 9, wherein the first functional layer comprises a planar bottom surface contacting an upper surface of the second substrate and overlying a central region of the first cavity, wherein an outer sidewall of the first functional layer overlies a peripheral region of the first cavity and is laterally offset from an outer sidewall of the second functional layer.

17. The integrated chip of claim 9, further comprising: a passivation layer overlying the second substrate, wherein the passivation layer contacts the top surface of the first functional layer and the top surface of the second functional layer.

18. An integrated chip, comprising: a first cavity over a first substrate; a second cavity over the first substrate and laterally offset from the first cavity; a second substrate over the first cavity and the second cavity; a first sensing layer over the second substrate and the first cavity; and a passivation layer over the second substrate, wherein the passivation layer continuously laterally extends from over the second cavity to the first sensing layer, wherein a material of the passivation layer is different from that of the first sensing layer and the second substrate.

19. The integrated chip of claim 18, further comprising: a second sensing layer over the second cavity, wherein the second sensing layer is laterally offset from the first sensing layer and is arranged between the passivation layer and the second substrate.

20. The integrated chip of claim 18, further comprising: a first doped region in the second substrate and over the first cavity; and a second doped region in the second substrate and over the second cavity, wherein the second doped region has a doping type and/or doping concentration different from that of the first doped region.