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Inventor(s)	Kim; YongCheol et al.

DISPLAY DEVICE

Abstract

A display device in one example includes a planarization layer disposed over a substrate, a first bank and a base layer disposed over the planarization layer, an anode disposed over the planarization layer and a side surface of the first bank, a reflective layer disposed to cover the base layer, a second bank covering a part of the anode and the first bank and disposed over the anode and the first bank, an organic layer disposed over the substrate on which the second bank is disposed, and a cathode disposed over the organic layer. The second bank is not formed over the reflection pattern to further improve the light extraction efficiency in accordance with the reduction in the non-emission area.

Inventors: **Kim; YongCheol (Gimpo-si, KR), Lee; Sohee (Paju-si, KR), Lee; Eunhyung (Goyang-si, KR)**

Applicant: **LG Display Co., Ltd.** (Seoul, KR)

Family ID: **1000008587443**

Assignee: **LG Display Co., Ltd. (Seoul, KR)**

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to Korean Patent Application No. 10-2024-0019773, filed on Feb. 8, 2024, in the Korean Intellectual Property Office, the entire disclosure of which is hereby expressly incorporated by reference into the present application.

BACKGROUND

Field

[0002] The present disclosure relates to a display device, and more particularly, to a display device with an improved light extraction efficiency.

Discussion of the Related Art

[0003] Currently, in a full-scale information era, a field of a display device which visually expresses electrical information signals has been rapidly developed and studies are continued to improve the performances of various display devices such as a thin-thickness, a light weight, and low power consumption.

[0004] Among various display devices, an electroluminescent display device is a self-emitting display device that does not need a separate light source, which is different from a liquid crystal display device. Therefore, the light emitting display device can be manufactured to have a light weight and a small thickness. Further, since the electroluminescent display device is driven at a low voltage, it is advantageous not only in terms of power consumption, but also in terms of color implementation, a response speed, a viewing angle, a contrast ratio (CR). Therefore, it is expected to be utilized in various fields.

[0005] In the meantime, light emitted from an emission layer of the electroluminescent display device passes through various components of the electroluminescent display device to be released to the outside of the electroluminescent display device. However, some of the light emitted from the emission layer can be trapped in the electroluminescent display device without being released to the outside of the electroluminescent display device, so that the light extraction efficiency of the electroluminescent display device can become an issue.

SUMMARY OF THE DISCLOSURE

[0006] An object to be achieved by the present disclosure is to provide a display device with an improved light extraction efficiency.

[0007] Another object to be achieved by the present disclosure is to provide a display device which improves a light extraction efficiency by reducing a non-emission area.

[0008] Still another object to be achieved by the present disclosure is to provide a display device which suppresses short-circuit due to metal burr and improves the light extraction efficiency.

[0009] Objects of the present disclosure are not limited to the above-mentioned objects, and other objects, which are not mentioned above, can be clearly understood by those skilled in the art from the following descriptions.

[0010] In order to achieve the objects as described above, according to an aspect of the present disclosure, a display device includes a planarization layer disposed over a substrate, a first bank and a base layer disposed on the planarization layer, an anode disposed over the planarization layer and a side surface of the first bank, a reflective layer disposed so as to cover the base layer, a second bank covering a part of the anode and the first bank and disposed over the anode and the first bank, an organic layer disposed over the substrate on which the second bank is disposed and a cathode disposed on the organic layer.

[0011] Other detailed matters of the example embodiments are included in the detailed description

and the drawings.
[0012] According to the present disclosure, the light extraction efficiency of the display device can be improved using a side mirror type anode.
[0013] According to aspects of the present disclosure, a reflection pattern is installed in a main emission area and an anode around the reflection pattern is shorted using a laser to induce reflective emission. At this time, a second bank is not formed over the reflection pattern to further improve the light extraction efficiency in accordance with the reduction in the non-emission area.
[0014] Further, according to the present disclosure, the reflection pattern is formed on a top surface of the planarization layer in which a part of a thickness is removed (etched) to suppress the short-circuit by the metal burr and improve the light extraction efficiency.
[0015] Therefore, low power can be implemented to reduce the power consumption and greenhouse gases generated by power use can be reduced to implement environment/social/governance (ESG).
[0016] The effects according to the present disclosure are not limited to the contents exemplified above, and more various effects are included in the present disclosure.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0017] The above and other aspects, features and other advantages of the present disclosure will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:
[0018] FIG. **1** is a view schematically illustrating a configuration of a display device according to a first embodiment of the present disclosure;
[0019] FIG. **2** is a plan view schematically illustrating a display panel of FIG. **1**;
[0020] FIG. **3** is a perspective view illustrating a structure in which a touch panel is embedded in a display panel according to the first embodiment of the present disclosure;
[0021] FIG. **4** is a cross-sectional view taken along the line I-I′ of FIG. **2**;
[0022] FIGS. **5**A and **5**B are a plan view and a perspective view illustrating a part of a sub pixel;
[0023] FIGS. **6**A and **6**B are views illustrating an emission image;
[0024] FIGS. **7**A to **7**F are views sequentially illustrating manufacturing processes of a display panel according to the first embodiment of the present disclosure of FIG. **4**;
[0025] FIG. **8** is a view illustrating a part of a cross-section of a display panel according to a second embodiment of the present disclosure;
[0026] FIGS. **9**A and **9**B are a plan view and a perspective view illustrating a part of a sub pixel;
[0027] FIGS. **10**A and **10**B are a plan view and a perspective view illustrating a part of a sub pixel according to a third embodiment of the present disclosure;
[0028] FIG. **11** is a view illustrating an emission image;
[0029] FIG. **12** is a view illustrating a part of a cross-section of a display panel according to a fourth embodiment of the present disclosure; and
[0030] FIG. **13** is a plan view illustrating a part of a sub pixel according to an embodiment of the present disclosure.
DETAILED DESCRIPTION OF THE EMBODIMENTS
[0031] Advantages and characteristics of the present disclosure and a method of achieving the advantages and characteristics will be clear by referring to embodiments described below in detail together with the accompanying drawings. However, the present disclosure is not limited to the embodiments disclosed herein but will be implemented in various forms. The embodiments are provided by way of example only so that those skilled in the art can fully understand the disclosures of the present disclosure and the scope of the present disclosure.

[0032] The shapes, sizes, ratios, angles, numbers, and the like illustrated in the accompanying drawings for describing the embodiments of the present disclosure are merely examples, and the present disclosure is not limited thereto. Like reference numerals generally denote like elements throughout the disclosure. Further, in the following description of the present disclosure, a detailed explanation of known related technologies can be omitted to avoid unnecessarily obscuring the subject matter of the present disclosure. The terms such as “including,” “having,” and “consist of” used herein are generally intended to allow other components to be added unless the terms are used with the term “only”. Any references to singular can include plural unless expressly stated otherwise.
[0033] Components are interpreted to include an ordinary error range even if not expressly stated.
[0034] When the position relation between two parts is described using the terms such as “on”, “over”, “above”, “below”, and “next”, one or more parts can be positioned between the two parts unless the terms are used with the term “immediately” or “directly”.
[0035] When an element or layer is disposed “on” another element or layer, another layer or another element may be interposed directly on the other element or therebetween.
[0036] Although the terms “first”, “second”, and the like are used for describing various components, these components are not confined by these terms. These terms are merely used for distinguishing one component from the other components, and may not define order or sequence. Therefore, a first component to be mentioned below can be a second component in a technical concept of the present disclosure.
[0037] Like reference numerals generally denote like elements throughout the disclosure. Further, the term “can” fully encompasses all the meanings and coverages of the term “may.”
[0038] A size and a thickness of each component illustrated in the drawing are illustrated for convenience of description, and the present disclosure is not limited to the size and the thickness of the component illustrated.
[0039] The features of various embodiments of the present disclosure can be partially or entirely adhered to or combined with each other and can be interlocked and operated in technically various ways, and the embodiments can be carried out independently of or in association with each other.
[0040] Hereinafter, various embodiments of the present disclosure will be described in detail with reference to the drawings. All the components of each display device according to all embodiments of the present disclosure are operatively coupled and configured.
[0041] FIG. **1** is a view schematically illustrating a configuration of a display device according to a first embodiment of the present disclosure.
[0042] For example, FIG. **1** illustrates a schematic configuration of a display device in which a touch panel TSP according to a first embodiment of the present disclosure is embedded. However, the present disclosure is not limited thereto and a display device according to the embodiments of the present disclosure may not include a display panel.
[0043] Referring to FIG. **1**, the display device according to the first embodiment of the present disclosure can provide both an image displaying function and a touch sensing function.
[0044] In order to provide an image displaying function, the display device according to the first embodiment of the present disclosure can include a display panel DISP, a gate driving circuit GDC, a data driving circuit DDC, and a timing controller TC.
[0045] For example, in the display panel DISP, a plurality of data lines and a plurality of gate lines are disposed and a plurality of sub pixels defined by the plurality of data lines and the plurality of gate lines can be disposed.
[0046] The data driving circuit DDC drives a plurality of data lines and the gate driving circuit GDC drives a plurality of gate lines, and the timing controller TC controls an operation of the data driving circuit DDC and the gate driving circuit GDC.
[0047] Each of the data driving circuit DDC, the gate driving circuit GDC, and the timing controller TC can be implemented by one or more individual components. In some cases, two or

more of the data driving circuit DDC, the gate driving circuit GDC, and the timing controller TC can be implemented to be integrated as one component. For example, the data driving circuit DDC and the timing controller TC can be implemented as one integrated chip (IC chip).
[0048] In order to provide a touch sensing function, the display device according to the first embodiment of the present disclosure can include a touch panel TSP and a touch sensing circuit TSC. The touch panel TSP includes a plurality of touch electrodes. The touch sensing circuit TSC supplies a touch driving signal to the touch panel TSP and detects a touch sensing signal from the touch panel TSP to sense the presence of a touch of a user or a touch position (touch coordinate) in the touch panel TSP based on the detected touch sensing signal.
[0049] For example, the touch sensing circuit TSC can include a touch driving circuit TDC, a touch controller TCTR, and the like. The touch driving circuit TDC supplies a touch driving signal to the touch panel TSP and detects a touch sensing signal from the touch panel TSP. The touch controller TCTR senses the presence of a touch of a user and/or a touch position in the touch panel TSP based on the touch sensing signal detected by the touch driving circuit TDC. The touch driving circuit TDC can include a first circuit part which supplies the touch driving signal to the touch panel TSP and a second circuit part which detects the touch sensing signal from the touch panel TSP.
[0050] For example, the touch driving circuit TDC and the touch controller TCTR can be implemented by separate components or in some cases, can be implemented to be integrated as one component.
[0051] For example, each of the data driving circuit DDC, the gate driving circuit GDC, and the touch driving circuit TDC can be implemented by one or more integrated circuits. From the viewpoint of electrical connection with the display panel DISP, the circuits can be implemented by a chip on glass (COG) type, a chip on film (COF) type, or a tape carrier package (TCP) type. Further, the gate driving circuit GDC can also be implemented by a gate in panel (GIP) type.
[0052] For example, each of circuit configurations DDC, GDC, and TC for display driving and circuit configurations TDC and TCTR for touch sensing can be implemented by one or more individual components. In some cases, one or more of circuit configurations DDC, GDC, and TC for display driving and one or more of circuit configurations TDC and TCTR for touch sensing are functionally integrated to be implemented by one or more components.
[0053] For example, the data driving circuit DDC and the touch driving circuit TDC can be implemented to be integrated in one or two or more integrated circuit chips. When the data driving circuit DDC and the touch driving circuit TDC are implemented to be integrated in two or more integrated circuit chips, each of two or more integrated circuit chips can have a data driving function and a touch driving function.
[0054] In the meantime, the display device according to the first embodiment of the present disclosure can be various types, such as a light emitting display device or a liquid crystal display device. Hereinafter, for the convenience of description, a light emitting display device will be described as an example of the display device. For example, even though the display panel DISP can be various types such as a light emitting display panel or a liquid crystal display panel, in the following description, for the convenience of description, a light emitting display panel will be described as an example of the display panel DISP.
[0055] Further, as it will be described below, the touch panel TSP can include a plurality of touch electrodes which is applied with a touch driving signal or detects a touch sensing signal and a plurality of touch routing lines which connects the plurality of touch electrodes to the touch driving circuit TDC.
[0056] The touch panel TSP can be provided at the outside of the display panel DISP. For example, the touch panel TSP and the display panel DISP can be separately manufactured to be combined. Such a touch panel TSP is called an external type or an add-on type.
[0057] In contrast, the touch panel TSP can be embedded in the display panel DISP. For example, when the display panel DISP is manufactured, a touch sensor structure such as a plurality of touch

electrodes and a plurality of touch routing lines which configure the touch panel TSP can be formed together with a plurality of electrodes and signal lines for display driving. Such a touch panel TSP is called an in-cell type.

[0058] Further, the touch panel TSP can be formed directly over an encapsulation unit of the display panel DISP. For example, the touch insulating film and the touch electrodes are patterned over the encapsulation unit and are connected to signal lines formed as electrodes for display driving to be driven. Such a touch panel TSP is called an on-cell type.

[0059] Hereinafter, for the convenience of description, an on-cell type in which the touch panel TSP is formed directly over the encapsulation unit will be described as an example.

[0060] FIG. **2** is a plan view schematically illustrating a display panel of FIG. **1**.

[0061] Referring to FIG. **2**, the display panel DISP can include an active area AA (or display area) in which images are displayed and a non-active area NA (or non-display area) which is an outer area of an outer boundary line BL of the active area AA. The non-active area NA can surround the active area AA entirely or only in part(s).

[0062] In the active area AA of the display panel DISP, a plurality of sub pixels SP for displaying images is disposed and various electrodes or signal lines for display driving are disposed.

[0063] Further, in the active area AA of the display panel DISP, a plurality of touch electrodes for touch sensing and a plurality of touch routing lines electrically connected thereto can be disposed. Accordingly, the active area AA can also be referred to as a touch sensing area which is capable of sensing the touch.

[0064] In the non-active area NA of the display panel DISP, link lines extending from various signal lines disposed in the active area AA or link lines which are electrically connected to various signal lines disposed in the active area AA, and pads which are electrically connected to the link lines can be disposed. The pads disposed in the non-active area NA can be bonded or electrically connected with the display driving circuit.

[0065] Further, in the non-active area NA of the display panel DISP, link lines extending from a plurality of touch routing lines disposed in the active area AA or link lines which are electrically connected to a plurality of touch routing lines disposed in the active area AA, and pads which are electrically connected to the link lines can be disposed. The pads disposed in the non-active area NA can be bonded or electrically connected with the touch driving circuit.

[0066] In the non-active area NA, a part of an outermost touch electrode, among a plurality of touch electrodes disposed in the active area AA, extends or one or more electrodes (touch electrodes) formed of the same material as the plurality of touch electrodes disposed in the active area AA can be further disposed.

[0067] For example, all the plurality of touch electrodes disposed in the display panel DISP can be present in the active area AA or some (for example, an outermost touch electrode) among the plurality of touch electrodes disposed in the display panel DISP can be present in the non-active area NA. Some (for example, an outermost touch electrode) among the plurality of touch electrodes disposed in the display panel DISP can be present over the active area AA and the non-active area NA.

[0068] In the meantime, referring to FIG. **2**, the display panel DISP according to the first embodiment of the present disclosure can include a dam area DA having a dam for suppressing any layer (for example, the encapsulation unit in the display panel) in the active area AA from passing over the outside of the display panel DISP.

[0069] The dam area DA can be located at a boundary of the active area AA and the non-active area NA or at any one position of a non-active area NA which is an outer area of the active area AA.

[0070] A dam disposed in the dam area DA can be disposed to enclose all directions of the active area AA or disposed only at an outside of one or two or more parts of the active area AA.

[0071] The dam disposed in the dam area DA can have one pattern which is connected or two or more separated patterns. Further, in the dam area DA, only a primary dam can be disposed or two

or more dams (primary dam and secondary dam) can be disposed, or three or more dams can also be disposed.

[0072] For example, in the dam area DA, in any one direction, only the primary dam is disposed and in the other direction, both the primary dam and the secondary dam can be disposed.

[0073] In the meantime, the display panel DISP of the first embodiment of the present disclosure can include an always-on-display (AOD) driving area which always drives a part of the active area AA even in a turned-off state of the display device to transfer information. The AOD driving area can include a state bar area which displays a state of the display device.

[0074] For example, when the AOD is displayed on the active area AA, sub pixels SP in the AOD driving area are activated, but sub pixels in areas other than the AOD driving area are inactivated. Accordingly, when the AOD is displayed on the active area AA, only sub pixels in the AOD driving area can be driven.

[0075] Further, for example, the display panel (DISP) driving circuit can drive only sub pixels SP of the AOD driving area in the AOD driving mode under the control of the timing controller (TC in FIG. **1**) to display data of predetermined AOD information in the sub pixels SP of the AOD driving area. Accordingly, in the AOD driving mode, only the sub pixels SP of the AOD driving area are activated and the sub pixels SP in an area other than the AOD driving area are not driven to be inactivated.

[0076] In the display device of the present disclosure, a side mirror (SM) structure is formed in a metal reflective plate having a height and a gradient in the vicinity of the emission area, for example, in the anode to apply an optical side mirror (OSM) technique which extracts light which is laterally lost, to the front surface. Light emitted from the light emitting diode in the sub pixel is reflected from the SM structure of the inclined anode to be extracted to the outside. The smaller the sub pixel, for example, the higher the pixels per inch (PPI), the shorter the distance from the taper so that the efficiency according to the application of the OSM technique can be further increased.

[0077] FIG. **3** is a perspective view illustrating a structure in which a touch panel is embedded in a display panel. Particularly, FIG. **3** is a perspective view illustrating a structure in which a touch panel is embedded in a display panel according to the first embodiment of the present disclosure.

[0078] Referring to FIG. **3**, for example, in the active area AA of the display panel (DISP in FIG. **2**), a plurality of sub pixels SP can be disposed over the substrate **111**.

[0079] Each sub pixel SP can include a light emitting diode **120**, a first transistor T**1** for driving the light emitting diode **120**, a second transistor T**2** for transmitting a data voltage VDATA to a first node N**1** of the first transistor T**1**, and a storage capacitor Cst for maintaining a constant voltage for one frame.

[0080] For example, the first transistor T**1** can include a first node N**1** to which the data voltage VDATA is applied, a second node N**2** which is electrically connected to the light emitting diode **120**, and a third node N**3** to which a driving voltage VDD is applied from a driving voltage line DVL. The first node N**1** can be a gate node, the second node N**2** can be a source node or a drain node, and the third node N**3** can be a drain node or a source node. The first transistor T**1** can also be referred to as a driving transistor which drives the light emitting diode **120**.

[0081] The light emitting diode **120** can include a first electrode (for example, an anode), an emission layer, and a second electrode (for example, a cathode). The first electrode is electrically connected to the second node N**2** of the first transistor T**1** and the second electrode can be applied with a base voltage VSS.

[0082] The emission layer in the light emitting diode **120** can be configured by an organic material or an inorganic material.

[0083] For example, the second transistor T**2** is controlled to be turned on or off by a scan signal SCAN applied through the gate line GL and can be electrically connected between the first node N**1** of the first transistor T**1** and the data line DL. Further, the second transistor T**2** can be referred to as a switching transistor.

[0084] For example, when the second transistor T**2** is turned on by the scan signal SCAN, the second transistor T**2** can transmit the data voltage VDATA supplied from the data line DL to the first node N**1** of the first transistor T**1**.
[0085] The storage capacitor Cst can be electrically connected between the first node N**1** and the second node N**2** of the first transistor T**1**.
[0086] Each sub pixel SP can have a 2T1C structure including two transistors T**1** and T**2** and one capacitor Cst and in some cases, can further include one or more transistors or further include one or more capacitors.
[0087] The storage capacitor Cst is not a parasitic capacitor (for example, Cgs or Cgd) which is an internal capacitor present between the first node N**1** and the second node N**2** of the first transistor T**1**, but can be an external capacitor which is intentionally designed at the outside of the first transistor T**1**.
[0088] The first transistor T**1** and the second transistor T**2** can be configured by an n-type transistor or a p-type transistor. As described above, in the display panel DISP, circuit elements such as a light emitting diode **120**, two or more transistors T**1** and T**2**, and one or more capacitors Cst can be disposed. The circuit element (specifically, the light emitting diode **120**) is vulnerable to external moisture or oxygen so that an encapsulation unit **140** for suppressing the external moisture or oxygen from permeating the circuit element can be disposed on the display panel DISP.
[0089] The encapsulation unit **140** can be formed by one layer, or also formed by a plurality of layers.
[0090] In the meantime, in the display device according to the first embodiment of the present disclosure, the touch panel TSP can be disposed over the encapsulation unit **140**. For example, in the display device according to the first embodiment of the present disclosure, a touch sensor structure, such as a plurality of touch electrodes TE which configures a touch panel TSP, can be disposed over the encapsulation unit **140**.
[0091] During the touch sensing, a touch driving signal or a touch sensing signal can be applied to the touch electrode TE. Accordingly, during the touch sensing, a potential difference is formed between the touch electrode TE and the cathode which are disposed with the encapsulation unit **140** therebetween so that an unnecessary parasitic capacitance can be formed. At this time, the parasitic capacitance can degrade a touch sensitivity. Therefore, in order to lower the parasitic capacitance, a distance between the touch electrode TE and the cathode can be designed to be equal to or larger than a predetermined value (for example, 1 μm) in consideration of a thickness of the display panel DISP, a display panel (DISP) manufacturing process, and a display performance. To this end, for example, the thickness of the encapsulation unit **140** can be designed to be at least 1 μm or larger.
[0092] In the meantime, the display device according to the first embodiment of the present disclosure can sense the touch based on capacitance formed in the touch electrode TE.
[0093] The display device according to the first embodiment of the present disclosure employs a capacitance-based touch sensing manner so that the touch can be sensed by a mutual-capacitance-based touch sensing manner or a self-capacitance-based touch sensing manner.
[0094] For example, according to the mutual-capacitance-based touch sensing manner, a plurality of touch electrodes TE can be classified into a driving touch electrode (a transmission touch electrode) to which a touch driving signal is applied and a sensing touch electrode (a reception touch electrode) which detects a touch sensing signal and forms a capacitance with the driving touch electrode.
[0095] In the case of the mutual-capacitance-based touch sensing manner, the touch sensing circuit can sense the presence of the touch and/or the touch coordinate based on the change in capacitance (mutual-capacitance) between the driving touch electrode and the sensing touch electrode depending on the presence of a pointer such as a finger or a pen.
[0096] According to the self-capacitance-based touch sensing manner, each touch electrode TE can serve as both a driving touch electrode and a sensing touch electrode. For example, the touch

sensing circuit applies a touch driving signal to one or more touch electrodes TE and detects a touch sensing signal by means of the touch electrode TE applied with the touch driving signal. The touch sensing circuit identifies the change in capacitance between a pointer such as a finger or a pen and the touch electrode TE based on the detected touch sensing signal to sense the presence of touch and/or the touch coordinate. In the self-capacitance-based touch sensing manner, the driving touch electrode and the sensing touch electrode are not distinguished.

[0097] As described above, the display device according to the first embodiment of the present disclosure can sense the touch in the mutual-capacitance-based touch sensing manner or the self-capacitance-based touch sensing manner. However, in the following description, for the convenience of description, it will be described that the display device performs mutual-capacitance-based touch sensing and includes a touch sensor structure therefor, as an example.

[0098] Hereinafter, a configuration of a sub pixel according to an embodiment of the present disclosure will be described in detail with reference to the drawings.

[0099] FIG. **4** is a cross-sectional view taken along the line I-I′ of FIG. **2**. FIGS. **5**A and **5**B are respectively a plan view and a perspective view illustrating a part of a sub pixel. FIGS. **6**A and **6**B are views illustrating an emission image.

[0100] More specifically, FIG. **4** illustrates a part of a cross-sectional structure of one sub pixel SP taken along the line I-I′ of FIG. **2** or **5**A.

[0101] FIG. **5**A is a plan view illustrating an example that a second bank **117** is disposed over the anode **122** of FIG. **4** and FIG. **5**B is a perspective view of FIG. **5**A. Here, in FIGS. **5**A and **5**B, for the convenience of description, configurations over the anode **122** and the second bank **117** are omitted.

[0102] FIG. **6**A illustrates an emission image of a comparative embodiment in which a second bank is formed over a reflection pattern and a cutting area is not formed around the reflection pattern. FIG. **6**B illustrates an emission image of the first embodiment in which a second bank **117** is not formed over a reflection pattern RP and the cutting area CA is formed around the reflection pattern RP.

[0103] Referring to FIGS. **4**, **5**A, and **5**B, the display panel of the first embodiment of the present disclosure can include a plurality of pixels configured by a first sub pixel, a second sub pixel, and a third sub pixel.

[0104] The first sub pixel, the second sub pixel, and the third sub pixel have different shapes, but have substantially the same configuration. However, these are not limited thereto and the first sub pixel, the second sub pixel, and the third sub pixel can have the same shape.

[0105] For example, the first sub pixel can be a red sub pixel. The second sub pixel can be a green sub pixel. The third sub pixel can be a blue sub pixel. However, the present disclosure is not limited thereto and can further include a fourth sub pixel which is a white sub pixel.

[0106] For example, the sub pixel SP can have an approximately rectangular shape, but is not limited thereto. At this time, a shape of the sub pixel SP can be defined by a shape of a first area **122***a* of the anode **122**, but it is not limited thereto.

[0107] In the meantime, in the first embodiment of the present disclosure, the anode **122** has a side mirror (SM) structure so that a first reflective emission area EA**2** is added in addition to the main emission area EA**1** so that each emission area can expand to be larger than each sub pixel SP.

[0108] Further, in the first embodiment of the present disclosure, a reflection pattern RP is installed in the main emission area EA**1** and a cut (ruptured) area CA in which the first area **122***a* of the anode **122** is cut is formed around the reflection pattern RP by means of the laser to add the second reflective emission area EA**3**. Specifically, a second bank **117** is not formed over the reflection pattern RP to further improve the light extraction efficiency in accordance with the reduction in the non-emission area.

[0109] A buffer layer **112**, such as a multi-buffer layer or a lower buffer layer, can be disposed over the substrate **111**.

[0110] The flexible substrate **111** can use a ductile material having a flexible characteristic, such as plastic.
[0111] The substrate **111** can be a film type including one of a group consisting of a polyester-based polymer, a silicon-based polymer, an acrylic polymer, a polyolefin-based polymer, and a copolymer thereof.
[0112] The substrate **111** can include a first substrate, a second substrate, and an insulating film. The insulating film can be disposed between the first substrate and the second substrate. As described above, the substrate **111** is configured by the first substrate, the second substrate, and the insulating film to suppress the moisture permeation. For example, the first substrate and the second substrate can be polyimide (PI) substrates.
[0113] For example, the multi-buffer layer can delay the spreading of the moisture or oxygen permeating the substrate **111** and can be formed by alternately laminating silicon nitride (SiNx) and silicon oxide (SiOx) at least once.
[0114] For example, the lower buffer layer can perform a function of protecting the semiconductor layer **134** and blocking various types of defects entering from the substrate **111**.
[0115] For example, the lower buffer layer can be formed by amorphous silicon, silicon nitride (SiNx), or silicon oxide (SiOx).
[0116] The switching thin film transistor (T**2** in the pixel driving circuit of FIG. **3**) and the driving thin film transistor **130** (T**1** in the pixel driving circuit of FIG. **3**) can be disposed over the buffer layer **112**.
[0117] The semiconductor layer **134** can be disposed in the active area on the buffer layer **112**.
[0118] For example, the semiconductor layer **134** can be formed of a polycrystalline semiconductor and include a channel region, a source region, and a drain region. However, it is not limited thereto and the semiconductor layer **134** can be configured by amorphous silicon or oxide semiconductor.
[0119] The gate insulating film **113** can be disposed on the semiconductor layer **134**.
[0120] The gate insulating film **113** can be configured by a single layer of silicon nitride (SiNx) or silicon oxide (SiOx) or a multilayer thereof.
[0121] A gate line is disposed in a first direction and a gate electrode **131** which is connected to the gate line can be disposed, on the gate insulating film **113**.
[0122] The gate electrode **131** can be disposed on the gate insulating film **113** so as to overlap the semiconductor layer **134**.
[0123] For example, the gate electrode **131** and the gate line can be configured by a single layer or multiple layers of copper (Cu), aluminum (Al), molybdenum (Mo), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), and neodymium (Nd) which are conductive metals or an alloy thereof, but are not limited thereto.
[0124] An interlayer insulating film **114** can be disposed on the gate electrode **131** so as to cover the gate electrode **131**.
[0125] For example, the interlayer insulating film **114** can be configured by a single layer of silicon nitride (SiNx) or silicon oxide (SiOx) or a multilayer thereof.
[0126] At this time, a partial area of the interlayer insulating film **114** and the gate insulating film **133** is selectively removed to form a plurality of contact holes which exposes both ends of the semiconductor layer **134**.
[0127] The data line can be disposed on the interlayer insulating film **114** in a second direction intersecting the gate line.
[0128] Further, a source electrode **132** and a drain electrode **133** which are connected to both ends of the semiconductor layer **134** are disposed on the interlayer insulating film **114**.
[0129] A protective film can be disposed on the data line and the source electrode **132** and the drain electrode **133**. The protective film can be omitted as needed.
[0130] The protective film can be formed as a single layer of silicon nitride (SiNx) or silicon oxide (SiOx) or a multilayer thereof.

[0131] A planarization layer **115** can be disposed on the protective film. The planarization layer **115** can have a multi-layered structure configured by at least two layers and for example, can include a first planarization layer **115***a* and a second planarization layer **115***b*. The first planarization layer **115***a* is disposed to cover the driving thin film transistor **130** and expose a part of the drain electrode **133** of the driving thin film transistor **130**.
[0132] A thickness of the planarization layer **115** is approximately 2 μm, but is not limited thereto.
[0133] The planarization layer **115** can be an overcoat layer, but is not limited thereto.
[0134] For example, the connection electrode **135** can be disposed on the first planarization layer **115***a* to electrically connect the driving thin film transistor **130** and the light emitting diode **120**. Further, various metal layers which serve as wiring lines/electrodes, such as a signal line, other than the data line, can be disposed on the first planarization layer **115***a*.
[0135] The connection electrode **135** can be configured with a material, such as copper (Cu), aluminum (Al), molybdenum (Mo), chrome (Cr), gold (Au), titanium (Ti), nickel (Ni), and neodymium (Nd), or an alloy thereof.
[0136] Further, the second planarization layer **115***b* can be disposed on the first planarization layer **115***a* and the connection electrode **135**.
[0137] For example, since various signal lines are increased in accordance with the increased resolution of the display panel, the planarization layer **115** is formed by two layers in the display panel according to the first embodiment of the present disclosure. Therefore, it can be difficult to dispose all the wiring lines on one layer while ensuring a minimum interval so that an additional layer is provided. Such an additional layer, for example, the second planarization layer **115***b* is added so that there is a margin for disposing wiring lines, which makes it easier to design and dispose the wiring lines/electrodes. Further, when a dielectric material is used for the planarization layer **115** configured by a plurality of layers, the planarization layer **115** can be utilized to form a capacitance between metal layers.
[0138] The second planarization layer **115***b* can be formed to expose a part of the connection electrode **135** and the drain electrode **133** of the driving thin film transistor **130** and the anode **122** of the light emitting diode **120** can be electrically connected by the connection electrode **135**.
[0139] The planarization layer **115** can be configured by one or more materials of acrylic resin, epoxy resin, phenolic resin, polyamides resin, polyimides resin, unsaturated polyesters resin, polyphenylene resin, benzocyclobutene, and polyphenylenesulfides resin, but is not limited thereto.
[0140] The first bank **116** can be disposed on the second planarization layer **115***b*.
[0141] For example, the first bank **116** can be disposed in a first non-emission area NEA**1** and a first reflective emission area EA**2** of the substrate **111** on the second planarization layer **115***b*. The first non-emission area NEA**1** and the first reflective emission area EA**2** can be disposed around the main emission area EA**1**.
[0142] The first non-emission area NEA**1** can be located so as to correspond to the first bank **116** in which the second area **122***b* of the anode **122** is not located. Further, a second non-emission area NEA**2** can be located between the main emission area EA**1** and the first reflective emission area EA**2**. The second non-emission area NEA**2**, the first reflective emission area EA**2**, and the first non-emission area NEA**1** can be sequentially disposed around the main emission area EA**1**.
[0143] The first bank **116** can be formed of an organic material. For example, the first bank **116** can be formed of polyimide, acrylic, or benzocyclobutene resin, but is not limited thereto.
[0144] Further, the first bank **116** can be formed of a black material. For example, the first bank **116** can be configured such that the black pigment is dispersed in an organic material, but is not limited thereto and as long as the first bank has a black color, the first bank can be configured by an arbitrary material. Further, for example, the organic material can be cardo-based polymer and polymer including epoxy acrylate, but is not limited thereto. As the first bank **116** includes the black material, the first bank **116** can reduce external light reflection, specifically, scattered reflection which can be generated by a transparent second bank **117**. For example, in order to

reduce the reflection of external light, an optical density of the first bank **116** can be configured to be 4 or lower at the thickness of 3 μm of the first bank **116**, but is not limited thereto. Further, in order to reduce the reflection of the external light, the reflectance of the first bank **116** can be 1% or lower, but is not limited thereto.

[0145] In the meantime, according to the first embodiment of the present disclosure, a reflection pattern RP with an inclined side surface is disposed over the second planarization layer **115***b* in which the first bank **116** is not disposed. For example, the reflection pattern RP can be located in the main emission area EA**1**.

[0146] The reflection pattern RP has an inclined side surface and a triangular cross-section overall, but is not limited thereto.

[0147] Further, for example, in the plan view, the reflection pattern RP can have a cross-shape which divides the main emission area EA**1** into four, but the present disclosure is not limited thereto and can have a lattice shape which divides the main emission area EA**1** into four or more.

[0148] When it is assumed that if a division number is 1, the main emission area EA**1** is divided into four and if a division number is 2, the main emission area EA**1** is divided into nine, if a taper height of the reflection pattern RP is 2 μm, the efficiency can be improved by approximately 100% to 150% with the division number of 2 to 6. Further, if a taper height of the reflection pattern RP is 1.5 the efficiency can be improved by approximately 140% to 180% with the division number of 2 to 6.

[0149] Further, the reflection pattern RP can be spaced apart from the first area **122***a* of the anode **122** by a predetermined distance. The reflection pattern RP of the present disclosure is not in contact with the first area **122***a* of the anode **122**.

[0150] For example, the reflection pattern RP can be configured by a base layer **116***e* formed of an organic material and a reflective layer **122***e* formed of a reflective material, but is not limited thereto.

[0151] For example, the base layer **116***e* can be configured by the same organic material as the first bank **116**, but is not limited thereto. The base layer **116***e* can be configured by the same process as the first bank **116**, but is not limited thereto. Further, the base layer **116***e* has an inclined side surface and a triangular cross-section, but is not limited thereto.

[0152] Further, for example, in the plan view, the base layer **116***e* can have a cross-shape which divides the main emission area EA**1** into four, but the present disclosure is not limited thereto and can have a lattice shape which divides the main emission area EA**1** into four or more. Here, an overall shape of the reflection pattern RP can be determined in accordance with the shape of the base layer **116***e*.

[0153] For example, the reflective layer **122***e* can be configured by the same conductive material as the anode **122**, but is not limited thereto. The reflective layer **122***e* can be formed by the same photo process as the anode **122**, but is not limited thereto. Further, the reflective layer **122***e* can be formed to cover a side surface of the base layer **116***e*. Further, the reflective layer **122***e* can be formed to cover the entire base layer **116***e*. The reflective layer **122***e* includes a reflective film of the anode **122** to reflect upwardly light which travels to the side surface of the reflection pattern RP to form a second reflective emission area EA**3** between the main emission areas EA**1**. At this time, a third non-emission area NEA**3** can be located between the main emission area EA**1** and the second reflective emission area EA**3**.

[0154] Further, for example, in the plan view, the reflective layer **122***e* can have a cross-shape which divides the main emission area EA**1** into four, but the present disclosure is not limited thereto and can have a lattice shape which divides the main emission area EA**1** into four or more.

[0155] In the meantime, according to the first embodiment of the present disclosure, a cut (ruptured) area CA in which the first area **122***a* of the anode **122** is cut (or removed) is provided around the reflection pattern RP. At this time, a third non-emission area NEA**3** can be located between the main emission area EA**1** and the second reflective emission area EA**3** by the cutting

area CA.
[0156] The cutting area CA is formed by cutting (or removing) the first area **122***a* of the anode **122** around the reflection pattern RP to expose the second planarization layer **115***b* therebelow. Accordingly, the reflective layer **122***e* of the reflection pattern RP can be separated from the first area **122***a* of the anode **122**. For example, the reflection pattern RP can be electrically isolated.
[0157] For example, in the plan view, the cutting area CA can have a cross-shape which divides the main emission area EA**1** into four in accordance with the shape of the reflection pattern RP, but the present disclosure is not limited thereto and can have a lattice shape which divides the main emission area EA**1** into four or more.
[0158] The cutting area CA can be formed using the laser.
[0159] In the meantime, as described above, according to the present disclosure, the second bank **117** is not formed over the reflection pattern RP. In this case, the non-emission area in the sub pixel SP is reduced to further improve the light extraction efficiency.
[0160] For example, referring to FIGS. **6**A and **6**B, when the side mirror shape anode is used, the first reflective emission area EA**2** is added around the main emission area EA**1** by the side mirror (SM) structure of the anode so that each emission area can expand to be larger than each sub pixel SP. Further, when the reflection pattern is installed in the main emission area EA**1**, the second reflective emission area EA**3** by the reflection pattern can be added.
[0161] However, when the reflection pattern is additionally formed in the sub pixel SP, the second bank needs to be formed over the reflection pattern to form the side mirror (SM) structure. In this case, referring to FIG. **6**A, the emission area can be reduced as much as the width of the second bank in the sub pixel SP. For example, the reduction in the emission area results in the degradation of the efficiency. In this case, the overall efficiency can be reduced because the reduction in the efficiency by the reduction in the emission area is greater than the increase of the efficiency added by the reflection pattern.
[0162] In the meantime, when the second bank is not formed over the reflection pattern, the organic layer can be deposited to be thinner by the taper of the reflection pattern and in this case, a dark spot defect can be generated due to the short-circuit between the anode and the cathode.
[0163] In contrast, when the cutting area is formed around the reflection pattern as in the first embodiment of the present disclosure, the reflection pattern can be electrically isolated by the cutting area so that there is no need to form the second bank over the reflection pattern. In this case, the emission area can be maximized by removing the second bank (see FIG. **6**B). For example, the increase of the efficiency added by the reflection pattern is greater than the reduction in the efficiency by the reduction in the emission area so that the overall efficiency can be increased.
[0164] In the meantime, the light emitting diode **120** which is electrically connected to the connection electrode **135** through a contact hole can be disposed over the second planarization layer **115***b*.
[0165] At this time, for example, the light emitting diode **120** can include an anode **122** connected to the drain electrode **133** of the driving thin film transistor **130**, a plurality of organic layers **124** disposed on the anode **122**, and a cathode **126** disposed on the organic layers **124**. The organic layer **124** can be referred to as a light emitting unit, but is not limited to the term.
[0166] Further, for example, the anode **122** can include a first area **122***a* which is disposed on the second planarization layer **115***b* to be in contact with the second planarization layer **115***b* and a second area **122***b* which extends from the first area **122***a* to be disposed on the side surface of the first bank **116**. The first area **112***a* has a surface substantially parallel to a surface of the substrate **111** and the second area **112***b* has a surface which has a predetermined angle with respect to the substrate **111**. The surface of the second area **122***b* may not be parallel to the surface of the substrate **111**.
[0167] Further, for example, the anode **122** can include a third area **122***c* which extends from the second area **122***b* in one direction to be electrically connected to the connection electrode **135**

through a contact hole. Further, a reflective layer **122***e* of the reflection pattern RP which is separated from the first area **122***a* of the anode **122** by the cutting area CA can be disposed in the sub pixel SP. For example, the reflective layer **122***e* can correspond to the second reflective emission area EA**3**.

[0168] The anode **122** can be electrically connected to the source electrode **132** or the drain electrode **133** of the driving thin film transistor **130**.

[0169] The anode **122** and the reflective layer **122***e* can include reflective films formed of a reflective metal.

[0170] In FIG. **4**, for the convenience of description, an example that the anode **122** and the reflective layer **122***e* are configured as a single layer is illustrated, but the present disclosure is not limited thereto and the anode **122** and the reflective layer **122***e* can be configured as a multi-layered structure. When the anode **122** and the reflective layer **122***e* are configured as a multi-layered structure, at least one layer can include a reflective metal.

[0171] For example, the anode **122** and the reflective layer **122***e* can have a multi-layered structure including a transparent film configured by a transparent conductive film and a reflective film configured by an opaque conductive film having a high reflection efficiency. For example, the transparent conductive film can be configured with a material having a high work function, such as indium-tin-oxide (ITO) or indium-zinc-oxide (IZO) and the opaque conductive film can be configured with a single or multi-layered structure including copper (Cu), silver (Ag), aluminum (Al), molybdenum (Mo), titanium (Ti), or an alloy thereof. Further, for example, the anode **122** and the reflective layer **122***e* can be configured by a structure in which a transparent conductive film, an opaque conductive film, and a transparent conductive film are sequentially laminated or can be configured by a structure in which a transparent conductive film and an opaque conductive film are sequentially laminated.

[0172] In the meantime, the second area **122***b* of the anode **122** of the present disclosure can be disposed on the side surface of the first bank **116** in accordance with a shape of the side surface of the first bank **116**. The second area **122***b* of the anode **122** disposed on the side surface of the first bank **116** can have a taper at an angle of approximately 30° to 60°, but is not limited thereto. Further, the reflective layer **122***e* of the present disclosure can be disposed so as to cover the base layer **116***e* in accordance with a shape of the base layer **116***e*. Further, the reflective layer **122***e* disposed on the side surface of the base layer **116***e* can have a taper at an angle of approximately 30° to 60°, but is not limited thereto. At this time, the second area **122***b* of the anode **122** and the reflective layer **122***e* including the reflective films can serve as a side mirror SM. Accordingly, the emission area according to the first embodiment of the present disclosure can further include a first reflective emission area EA**2** and a second reflective emission area EA**3** by the SM structure, in addition to the main emission area EA**1**. The first reflective emission area EA**2** can be formed between the main emission area EA**1** and the first non-emission area NEA**1** so as to correspond to the second area **122***b* of the anode **122**. The second reflective emission area EA**3** can be formed between the main emission areas EA**1** so as to correspond to the reflective layer **122***e* of the reflection pattern RP.

[0173] For example, in the plan view, the main emission area EA**1** has a rectangular shape, the first reflective emission area EA**2** has a rectangular frame shape, and the second reflective emission area EA**3** has a cross-shape, but the present disclosure is not limited thereto. Further, for example, the main emission area EA**1** can have a circular shape, an oval shape, or a polygonal shape and the first reflective emission area EA**2** can have a circular shape, an oval shape, or a polygonal frame shape. Further, the second reflective emission area EA**3** can have a circular shape, an oval shape, a polygonal shape, or a lattice shape.

[0174] When the display device according to the first embodiment of the present disclosure is a top emission type light emitting display device, the reflective films of the anode **122** and the reflective layer **122***e* can upwardly reflect the light emitted from the light emitting diode **120**. For example,

the light generated in the organic layer **124** of the light emitting diode **120** can be emitted not only upwardly, but also laterally. The laterally emitted light is directed into the display device, is trapped in the display device by the total reflection, or travels into the display device and then dissipates. Therefore, according to the present disclosure, the second area **122***b* of the anode **122** and the reflective layer **122***e* of the reflection pattern RP which include the reflective films are disposed on the side surfaces of the first bank **116** and the base layer **116***e*, respectively, to change a traveling direction of light which laterally travels to an upward direction. Therefore, the light extraction efficiency of the display device can be improved.

[0175] For example, the second bank **117** can be disposed over the first bank **116** and the anode **122** while covering a part of the anode **122**.

[0176] For example, the second bank **117** can cover a part of the first area **122***a* and the second area **122***b* and the third area **122***c* of the anode **122**. The second bank **117** can cover a part of an edge of the first area **122***a*. Further, the second bank **117** can cover the entire second area **122***b* and the entire third area **122***c*.

[0177] A part of the second bank **117** corresponding to the main emission area EA**1** can be open. For example, the second bank **117** can include an open area OA obtained by removing (opening) a part corresponding to the main emission area EA**1** of a sub pixel SP.

[0178] A part of the second bank **117** which corresponds to the second reflective emission area EA**3** and the third non-emission area NEA**3** can be additionally open. The reflection pattern RP can be located in the second reflective emission area EA**3** and the third non-emission area NEA**3** which are additionally open.

[0179] As described above, the sub pixel SP according to the first embodiment of the present disclosure can have a plurality of emission areas EA**1**, EA**2**, and EA**3** and a plurality of non-emission areas NEA**1**, NEA**2**, and NEA**3**.

[0180] In each sub pixel SP, the main emission area EA**1** can have a width larger than those of the first reflective emission area EA**2** and the second reflective emission area EA**3**. In each sub pixel SP, the first non-emission area NEA**1** can have a width larger than those of the second non-emission area NEA**2** and the third non-emission area NEA**3**, but it is not limited thereto.

[0181] For example, the second non-emission area NEA**2** can be located between the main emission area EA**1** and the first reflective emission area EA**2**. The third non-emission area NEA**3** can be located between the main emission area EA**1** and the second reflective emission area EA**3**.

[0182] In each sub pixel SP, the first reflective emission area EA**2** can be disposed around the main emission area EA**1** and the second reflective emission area EA**3** can be disposed in the main emission area EA**1** of each sub pixel SP.

[0183] The second bank **117** can be formed of an organic material. For example, the second bank **117** can be formed of polyimide, acrylic, or benzocyclobutene resin, but is not limited thereto.

[0184] Further, the second bank **117** can be formed of a transparent material, but is not limited thereto.

[0185] The organic layer **124** can also be disposed on the top surface and a side portion of the second bank **117**, including the open area OA of the second bank **117**. Further, the organic layer **124** can be disposed and extend over the top surface and the side portion of the reflection pattern RP, including the cutting area CA.

[0186] For example, the organic layer **124** can include a hole injection layer, a hole transport layer, an emission layer, an electron transport layer, and an electron injection layer. In a tandem structure in which a plurality of emission layers is overlaid, a charge generation layer can be further disposed between the emission layers. The emission layer can emit different color light in every sub pixel. For example, each of a red emission layer, a green emission layer, and a blue emission layer can be separately disposed in every sub pixel, but the present disclosure is not limited thereto. However, a common emission layer is formed in every sub pixel to emit white light regardless of the color and a color filter which distinguishes the color can be separately provided. In this case, the emission

layer can be individually disposed, but the hole injection layer, the electron injection layer, the hole transport layer, or the electron transport layer is provided as a common layer to be disposed in each sub pixel in the same way.

[0187] Further, the cathode **126** can be disposed on the organic layer **124** so as to be opposite to the anode **122** with the organic layer **124** therebetween. For example, when the cathode **126** is applied to a top emission type display device, the cathode can be configured by a transparent conductive film obtained by forming indium tin oxide (ITO), indium zinc oxide (IZO), or magnesium-silver (Mg—AG) to be thin.

[0188] The encapsulation unit **140** can be disposed over the cathode **126** to protect the light emitting diode **120**.

[0189] The light emitting diode **120** can react to external moisture and oxygen due to a characteristic of the organic material of the organic layer **124** to cause dark-spot or pixel shrinkage. In order to suppress this problem, the encapsulation unit **140** can be disposed over the cathode **126**. The encapsulation unit **140** can be configured by a first inorganic insulating film, a foreign material compensation layer, and a second inorganic insulating film, but is not limited thereto.

[0190] For example, the first inorganic insulating film can be disposed over the substrate **111** on which the cathode **126** is disposed to be the most adjacent to the light emitting diode **120**.

[0191] For example, the first inorganic insulating film can be configured by an inorganic insulating material on which low-temperature deposition is allowed, such as silicon nitride (SiNx), silicon oxide (SiOx), silicon oxynitride (SiON), or aluminum oxide (Al.sub.2O.sub.3). The first inorganic insulating film is deposited under a low temperature atmosphere so that the damage of the organic layer **124** including an organic material vulnerable to the high temperature atmosphere during the deposition can be suppressed.

[0192] A foreign material compensation layer can be disposed to have a smaller area than the first inorganic insulating film and can be configured to expose both ends of the first inorganic insulating film. The foreign material compensation layer can be formed of an organic insulating material, such as acrylic resin, epoxy resin, polyimide, polyethylene, or silicon oxycarbon (SiOC).

[0193] In the meantime, when the foreign material compensation layer is formed by an inkjet method, one or more dams can be disposed in a boundary area of the non-active area and the active area or a dam area corresponding to a partial area in the non-active area. In such a dam area, a primary dam adjacent to the active area and a secondary dam adjacent to the pad unit can be disposed.

[0194] When a liquid type foreign material compensation layer is dropped in the active area, one or more dams disposed in the dam area can suppress the liquid type foreign material compensation layer from collapsing in the direction of the non-active area to invade the pad unit.

[0195] The primary dam and/or secondary dam can be configured as a single layer or a multiple-layered structure. For example, the primary dam and/or secondary dam can be simultaneously configured with the same material as at least one of the planarization layer **115**, the first bank **116**, the second bank **117**, and the spacer. In this case, the dam structure can be configured without having the mask adding process and increasing the cost.

[0196] Further, the foreign material compensation layer including an organic material can be located only on an inner surface of the primary dam.

[0197] Further, the second inorganic insulating film can be disposed so as to cover an upper surface and a side surface of each of the first inorganic insulating film and the foreign material compensation layer. The second inorganic insulating film can serve to minimize or block the permeation of the external moisture or oxygen into the first inorganic insulating film and the foreign material compensation layer. The second inorganic insulating film can be formed of an inorganic insulating material, such as silicon nitride (SiNx), silicon oxide (SiOx), silicon oxynitride (SiON), and aluminum oxide (Al.sub.2O.sub.3).

[0198] A touch buffer film **151** can be disposed on the encapsulation unit **140**.

[0199] A bridge pattern **155** can be disposed on the touch buffer film **151**. However, it is not limited thereto and a touch electrode (or a touch line) can be disposed on the touch buffer film **151**.
[0200] The touch buffer film **151** can be located between the bridge pattern **155** and the encapsulation unit **140**.
[0201] For example, the touch buffer film **151** can be designed to maintain a predetermined minimum interval between the bridge pattern **155** and the cathode **126**. By doing this, a parasitic capacitance which can be formed between the bridge pattern **155** and the cathode **126** can be reduced or suppressed so that degradation of the touch sensitivity due to the parasitic capacitance can also be suppressed.
[0202] The bridge pattern **155** can be disposed over the encapsulation unit **140** without having the touch buffer film **151**.
[0203] The bridge pattern **155** can have a single layer or multi-layered structure formed of a metal having strong corrosion resistance and acid resistance, such as aluminum (Al), titanium (Ti), copper (Cu), or molybdenum (Mo).
[0204] The touch insulating film **152** can be disposed on the bridge pattern **155**.
[0205] For example, the touch insulating film **152** can use an organic film or an inorganic film which can be formed by a low temperature process. When the organic film is used for the touch insulating film **152**, after coating the organic film over the substrate **111**, the organic film is cured at a temperature of 100° C. or lower to form the touch insulating film **152** to suppress the damage of the organic layer **124** vulnerable to the high temperature. When the inorganic film is used for the touch insulating film **152**, in order to suppress the damage of the organic layer **124** vulnerable to the high temperature, a low temperature chemical vapor deposition (CVD) process and a washing process are repeated at least twice to form the touch insulating film **152** with a multi-layered structure.
[0206] A partial area of the touch insulating film **152** is selectively removed to form a touch contact hole to expose a part of the bridge pattern **155**.
[0207] A touch electrode (or a touch line) **156** can be disposed on the touch insulating film **152**. However, it is not limited thereto and the bridge pattern can be disposed on the touch insulating film **152**.
[0208] For example, the touch electrode **156** can be electrically connected to the bridge pattern **155** through the touch contact hole.
[0209] Further, the touch planarization layer **157** can be disposed on the touch electrode **156**, but is not limited thereto and the touch planarization layer can be omitted.
[0210] A black matrix **175** can be disposed on the touch planarization layer **157**.
[0211] The black matrix **175** can be located over the touch electrode **156**.
[0212] The black matrix **175** can be located so as to correspond to the first non-emission area NEA**1**.
[0213] A color filter layer **170** can be disposed in the main emission area EA**1**, the first reflective emission area EA**2**, the second reflective emission area EA**3**, the second non-emission area NEA**2**, and the third non-emission area NEA**3** between the back matrixes **175**.
[0214] For example, the color filter layer **170** can include a red color filter layer, a green color filter layer, and a blue color filter layer, but is not limited thereto and further include a white color filter layer.
[0215] The black matrix **175** can be disposed on the boundary of color filter layers **170** with different colors. Therefore, the black matrix **175** can define a sub pixel area. Sub pixel areas defined by the black matrix **175** can be a red sub pixel area, a green sub pixel area, and a blue sub pixel area. Further, the sub pixel area can further include a white sub pixel area. For example, an area in which the red color filter layer is disposed can correspond to a red sub pixel area, an area in which the green color filter layer is disposed can correspond to a green sub pixel area, and an area in which a blue color filter layer is disposed can correspond to a blue sub pixel area. Further, an

area in which a white color filter layer is disposed can correspond to a white sub pixel area.
[0216] For example, in the area in which the red color filter layer is disposed, red light can be emitted, in the area in which the green color filter layer is disposed, green light can be emitted, in the area in which the blue color filter layer is disposed, blue light can be emitted, and in the area in which the white color filter layer is disposed, white light can be emitted
[0217] Hereinafter, a manufacturing method of the display panel according to the first embodiment of the present disclosure configured as described above will now be described in detail with reference to the drawings.
[0218] FIGS. **7**A to **7**F are views sequentially illustrating manufacturing processes of the display panel according to the first embodiment of the present disclosure of FIG. **4**.
[0219] Hereinafter, the same configuration is denoted by the same reference numeral and the description of the same reference numeral can refer to FIGS. **1** to **5**B.
[0220] First, referring to FIG. **7**A, a buffer layer **112**, such as a multi-buffer layer or a lower buffer layer, can be formed over the substrate **111**.
[0221] The semiconductor layer **134** can be formed in the active area on the buffer layer **112**.
[0222] The gate insulating film **113** can be formed on the semiconductor layer **134**.
[0223] A gate line is formed in a first direction and a gate electrode **131** which is connected to the gate line can be formed, on the gate insulating film **113**.
[0224] An interlayer insulating film **114** can be formed on the gate electrode **131** so as to cover the gate electrode **131**.
[0225] At this time, a partial area of the interlayer insulating film **114** and the gate insulating film **133** is selectively removed to form a plurality of contact holes which exposes both ends of the semiconductor layer **134**.
[0226] The data line can be formed on the interlayer insulating film **114** in a second direction intersecting the gate line.
[0227] Further, a source electrode **132** and a drain electrode **133** which are connected to both ends of the semiconductor layer **134**, respectively, can be formed on the interlayer insulating film **114**.
[0228] The planarization layer **115** can be formed on the data line and the source electrode **132** and the drain electrode **133**.
[0229] The first bank **116** can be formed on the planarization layer **115**.
[0230] For example, the first bank **116** can be formed in a first non-emission area NEA**1** and a first reflective emission area EA**2** of the substrate **111** on the second planarization layer **115***b*.
[0231] A part of the first bank **116** which substantially corresponds to the main emission area EA**1**, the second non-emission area NEA**2**, and the third non-emission area NEA**3** can be open. For example, the first bank **116** can include a first open area OA**1** which is formed by removing (opening) a part which substantially corresponds to the main emission area EA**1**, the second non-emission area NEA**2**, and the third non-emission area NEA**3**.
[0232] The first open area OA**1** can have a larger size than an open area OA to be described below.
[0233] In the meantime, the base layer **116***e* with an inclined side surface can be formed over the second planarization layer **115***b* in which the first bank **116** is not disposed.
[0234] The base layer **116***e* can be formed to have an inclined side surface and a triangular cross-section overall, but is not limited thereto.
[0235] For example, the base layer **116***e* can be formed by the same organic material as the first bank **116**, but is not limited thereto. The base layer **116***e* can be configured by the same process as the first bank **116**, but is not limited thereto.
[0236] Further, for example, in the plan view, the base layer **116***e* can have a cross-shape which divides the main emission area EA**1** into four, but the present disclosure is not limited thereto and can have a lattice shape which divides the main emission area EA**1** into four or more.
[0237] Next, referring to FIG. **7**B, the anode **122** can be formed on the second planarization layer **115***b* and the first bank **116**.

[0238] Further, the reflective layer **122***e* can be formed on the base layer **116***e*.
[0239] The anode **122** can include a first area **122***a* which is disposed on the second planarization layer **115***b* to be in contact with the second planarization layer **115***b* and a second area **122***b* which extends from the first area **122***a* to be disposed on the side surface of the first bank **116**. The first area **112***a* has a surface substantially parallel to a surface of the substrate **111** and the second area **122***b* has a surface which has a predetermined angle with respect to the substrate **111**.
[0240] Further, for example, the anode **122** can include a third area **122***c* which extends from the second area **122***b* in one direction to be electrically connected to the connection electrode **135** through a contact hole.
[0241] For example, the reflective layer **122***e* can be formed by the same conductive material as the anode **122**, but is not limited thereto. The reflective layer **122***e* can be formed by the same photo process as the anode **122**, but is not limited thereto. Further, the reflective layer **122***e* can be formed to cover a side surface of the base layer **116***e*. Further, the reflective layer **122***e* can be formed to cover the entire base layer **116***e*.
[0242] The anode **122** and the reflective layer **122***e* can include reflective films formed of a reflective metal.
[0243] For example, the second area **122***b* of the anode **122** disposed on the side surface of the first bank **116** and the reflective layer **122***e* disposed on the side surface of the base layer **116***e* can be formed to have a taper at an angle of approximately 30° to 60°, but are not limited thereto.
[0244] Next, referring to FIG. **7**C, the first area **122***a* of the anode **122** around the reflective layer **122***e* is cut (or removed) using the laser cutting to form the cutting area CA.
[0245] The cutting area CA is formed by cutting (or removing) the first area **122***a* of the anode **122** around the reflective layer **122***e* to expose the second planarization layer **115***b* therebelow. Accordingly, the reflective layer **122***e* can be separated from the first area **122***a* of the anode **122**. The reflective layer **122***e* can be electrically isolated.
[0246] Here, the base layer **116***e* and the reflective layer **122***e* can configure the reflection pattern RP.
[0247] The reflection pattern RP can have an inclined side surface and a triangular cross-section overall, but is not limited thereto.
[0248] Further, for example, in the plan view, the reflection pattern RP can have a cross-shape which divides the main emission area EA**1** into four, but the present disclosure is not limited thereto and can have a lattice shape which divides the main emission area EA**1** into four or more.
[0249] Further, the reflection pattern RP can be spaced apart from the first area **122***a* of the anode **122** by a predetermined distance.
[0250] Next, referring to FIG. **7**D, the second bank **117** can be formed over the first bank **116** and the anode **122** while covering a part of the anode **122**.
[0251] For example, the second bank **117** can cover a part of the first area **122***a* and the second area **122***b* and the third area **122***c* of the anode **122**. The second bank **117** can cover a part of an edge of the first area **122***a*. Further, the second bank **117** can cover the entire second area **122***b* and the entire third area **122***c*.
[0252] A part of the second bank **117** corresponding to the main emission area EA**1** can be open. For example, the second bank **117** can include an open area OA obtained by removing (opening) a part corresponding to the main emission area EA**1** of a sub pixel SP.
[0253] According to the first embodiment of the present disclosure, the second bank **117** is not formed over the reflection pattern RP.
[0254] Next, referring to FIG. **7**E, the organic layer **124** can be disposed on the top surface and a side portion of the second bank **117**, including the open area OA of the second bank **117**.
[0255] Further, the organic layer **124** can be disposed and extend over the top surface and the side portion of the reflection pattern RP, including the cutting area CA.
[0256] Further, the cathode **126** can be formed on the organic layer **124** so as to be opposite to the

anode **122** with the organic layer **124** therebetween.
[0257] Next, referring to FIG. **7**F, an encapsulation unit **140** can be formed over the cathode **126** to protect the light emitting diode **120**.
[0258] A touch panel configured by a touch buffer film **151**, a bridge pattern **155**, a touch insulating film **152**, a touch electrode (or a touch line) **156**, and a touch planarization layer **157** can be disposed over the encapsulation unit **140**.
[0259] The black matrix **175** and the color filter layer **170** can be formed on the touch planarization layer **157**.
[0260] In the meantime, according to the present disclosure, in order to suppress the short-circuit caused by metal burrs generated during the laser cutting, the reflection pattern can be formed on the top surface of the planarization layer in which a part of the thickness is removed (etched), which will now be described in detail with reference to the drawings.
[0261] FIG. **8** is a view illustrating a part of a cross-section of a display panel according to a second embodiment of the present disclosure. FIGS. **9**A and **9**B are a plan view and a perspective view illustrating a part of a sub pixel of the display panel according to the second embodiment of the present disclosure.
[0262] The second embodiment of FIGS. **8**, **9**A, and **9**B is substantially the same as the first embodiment of FIGS. **4**, **5**A, and **5**B described above except that a reflection pattern RP is disposed on a top surface of a second planarization layer **215***b* in which a part of the thickness is removed (etched). Therefore, a redundant description will be omitted or may be briefly provided. The same configuration will be denoted with the same reference numeral. Hereinafter, the description for the same reference numeral can be understood by referring to FIGS. **1** to **5**B.
[0263] Particularly, FIG. **8** illustrates a part of a cross-sectional structure of one sub pixel SP taken along the line II-II′ of FIG. **9**A.
[0264] FIG. **9**A is a plan view illustrating an example that a second bank **117** is disposed over the anode **222** of FIG. **8** and FIG. **9**B is a perspective view of FIG. **9**A. Here, in FIGS. **9**A and **9**B, for the convenience of description, configurations over the anode **222** and the second bank **117** are omitted.
[0265] Referring to FIGS. **8**, **9**A, and **9**B, a planarization layer **215** can be disposed over the substrate **111**.
[0266] The planarization layer **215** can include a first planarization layer **215***a* and a second planarization layer **215***b*.
[0267] According to the second embodiment of the present disclosure, a groove pattern HP is formed by removing (etching) a part of an upper thickness of a partial area of the second planarization layer **215***b*. For example, the groove pattern HP can be formed by removing (etching) a part of the upper thickness of the second planarization layer **215***b* in which the reflection pattern RP is to be disposed. The groove pattern HP can have a predetermined depth by considering a height of the reflection pattern RP to be formed. When the reflection pattern RP has a cross shape which divides the main emission area EA**1** into four, the groove pattern HP can also have a cross shape which divides the main emission area EA**1** into four. In the plan view, the groove pattern HP can have a larger area than the reflection pattern RP to place the reflection pattern RP in the groove pattern HP.
[0268] The groove pattern HP can be formed by the photo process.
[0269] The first bank **116** can be disposed on the second planarization layer **215***b* in which the groove pattern HP is formed.
[0270] According to the second embodiment of the present disclosure, a reflection pattern RP having an inclined side surface is disposed in the groove pattern HP of the second planarization layer **215***b*.
[0271] The reflection pattern RP can have an inclined side surface and a triangular cross-section overall, but is not limited thereto.

[0272] Further, for example, in the plan view, the reflection pattern RP can have a cross-shape which divides the main emission area EA**1** into four, but the present disclosure is not limited thereto and can have a lattice shape which divides the main emission area EA**1** into four or more.
[0273] Further, the reflection pattern RP can be spaced apart from the first area **222***a* of the anode **222** by a predetermined distance.
[0274] The anode **222** can include a first area **222***a* which is disposed on the second planarization layer **215***b* to be in contact with the second planarization layer **215***b* and a second area **222***b* which extends from the first area **222***a* to be disposed on the side surface of the first bank **116**. The first area **222***a* has a surface substantially parallel to a surface of the substrate **111** and the second area **222***b* has a surface which has a predetermined angle with respect to the substrate **111**. Further, for example, the anode **222** can include a third area **222***c* which extends from the second area **222***b* in one direction to be electrically connected to the connection electrode **135** through a contact hole.
[0275] For example, the reflection pattern RP can be configured by a base layer **216***e* formed of an organic material and a reflective layer **222***e* formed of a reflective material, but is not limited thereto.
[0276] Further, according to the second embodiment of the present disclosure, a cut (ruptured) area CA in which the first area **222***a* of the anode **222** is cut (or removed) is provided around the reflection pattern RP. The cutting area CA can be located in the groove pattern HP around the reflection pattern RP.
[0277] The cutting area CA is formed by cutting (or removing) the first area **222***a* of the anode **222** around the reflection pattern RP to expose the second planarization layer **215***b* therebelow. Accordingly, the reflective layer **222***e* of the reflection pattern RP can be separated from the first area **222***a* of the anode **222**. For example, the reflection pattern RP can be electrically isolated.
[0278] The cutting area CA can be formed using the laser.
[0279] According to the second embodiment, the reflection pattern RP is formed in the groove pattern HP of the second planarization layer **215***b* in which a part of the thickness is removed (etched) so that the short-circuit caused by the metal burrs generated during the laser cutting can be suppressed. For example, when the cutting area CA is formed using the laser, a metal burr in which an end of the first area **222***a* of the anode **222** which is melted by the laser is rolled up is generated. According to the second embodiment of the present disclosure, the cutting area CA is formed in the groove pattern HP of the second planarization layer **215***b* so that the metal bur is not generated due to the step. Therefore, the reflection pattern RP can be surely electrically isolated from the anode **222** so that the light extraction efficiency can be improved.
[0280] The light emitting diode **220** configured by the anode **222**, the organic layer **224**, and the cathode **226** can be disposed over the second planarization layer **215***b*.
[0281] The light emitting diode **220** and configurations thereabove are substantially the same as the first embodiment described above so that a redundant description will be omitted.
[0282] In the meantime, according to the present disclosure, each of the main emission area, the first reflective emission area and the second reflective emission area has a shape other than the rectangular shape and the cross shape, which will now be described in detail with reference to the drawings.
[0283] FIGS. **10**A and **10**B are respectively a plan view and a perspective view illustrating a part of a sub pixel according to a third embodiment of the present disclosure. FIG. **11** is a view illustrating an emission image according to the third embodiment of the present disclosure.
[0284] The third embodiment of FIGS. **10**A, **10**B, and **11** is substantially the same as the second embodiment of FIGS. **8**, **9**A, and **9**B described above except for shapes of an anode **322**, a reflection pattern RP, and emission areas EA**1**, EA**2**, and EA**3** thereby so that a redundant description will be omitted or may be briefly provided. The same configuration will be denoted with the same reference numeral. Hereinafter, the description for the same reference numeral can be understood by referring to FIGS. **1** to **9**B.

[0285] Here, FIG. **10**A is a plan view illustrating an example that a second bank **317** is disposed over the anode **322** and FIG. **10**B is a perspective view of FIG. **10**A according to the third embodiment of the present disclosure. Further, in FIGS. **10**A and **10**B, for the convenience of description, configurations over the anode **322** and the second bank **317** are omitted.
[0286] FIG. **11** illustrates an emission image of the third embodiment in which a second bank **317** is not formed over the reflection pattern RP and the cutting area CA is formed around the reflection pattern RP.
[0287] Referring to FIGS. **10**A, **10**B, and **11**, the display panel of the third embodiment of the present disclosure can include a plurality of pixels configured by a first sub pixel, a second sub pixel, and a third sub pixel.
[0288] For example, the sub pixel SP can have an approximately circular shape, but is not limited thereto. At this time, a shape of the sub pixel SP can be defined by a shape of a first area **322***a* of the anode **322**, but it is not limited thereto. Further, the sub pixel SP can have an oval shape or a polygonal shape. Further, the sub pixel SP can have a mixed shape of a circular shape, an oval shape or a polygonal shape.
[0289] In the meantime, in the third embodiment of the present disclosure, the anode **322** has a side mirror (SM) structure so that a first reflective emission area EA**2** is added in addition to the main emission area EA**1** so that each emission area can expand as compared with each sub pixel SP.
[0290] Further, in the third embodiment of the present disclosure, a reflection pattern RP is installed in the main emission area EA**1** and a cut (ruptured) area CA in which the first area **322***a* of the anode **322** is cut is formed around the reflection pattern RP by means of the laser to add the second reflective emission area EA**3**. Specifically, a second bank **317** is not formed over the reflection pattern RP to further improve the light extraction efficiency in accordance with the reduction in the non-emission area.
[0291] Further, according to the third embodiment of the present disclosure, in the plan view, the reflection pattern RP has a circular shape in response to the shape of the sub pixel SP.
[0292] For example, the main emission area EA**1** can have a circular shape in response to the shape of the sub pixel SP and the first reflective emission area EA**2** can have a circular frame shape. Further, the second reflective emission area EA**3** can have a circular shape or a circular frame shape, in response to the shape of the reflection pattern RP.
[0293] In the meantime, the reflection pattern of the present disclosure can have a lattice shape which divides the main emission area into four or more, which will be described in detail.
[0294] FIG. **12** is a view illustrating a part of a cross-section of a display panel according to a fourth embodiment of the present disclosure. FIG. **13** is a plan view illustrating a part of a sub pixel of the display panel according to the fourth embodiment of the present disclosure.
[0295] The fourth embodiment of FIGS. **12** and **13** is substantially the same as the second embodiment of FIGS. **8**, **9**A, and **9**B except that the reflection pattern RP has a lattice shape which divides the main emission area EA**1** into four or more, so that a redundant description will be omitted or may be briefly provided. The same configuration will be denoted with the same reference numeral. Hereinafter, the description for the same reference numeral can refer to FIGS. **1** to **9**B.
[0296] At this time, FIG. **12** illustrates a part of a cross-sectional structure of one sub pixel SP taken along the line III-III′ of FIG. **13**. FIG. **13** is a plan view illustrating an example in which the second bank **117** is disposed over the anode **422** of FIG. **12** according to the fourth embodiment of the present disclosure. For the convenience of description, in FIG. **13**, configurations over the anode **422** and the second bank **117** are omitted.
[0297] Referring to FIGS. **12** and **13**, a planarization layer **415** can be disposed over the substrate **111**.
[0298] The planarization layer **415** can include a first planarization layer **415***a* and a second planarization layer **415***b*.

[0299] According to the fourth embodiment of the present disclosure, like the second and third embodiments, a groove pattern HP is formed by removing (etching) a part of an upper thickness of a partial area of the second planarization layer **415***b*. For example, the groove pattern HP can be formed by removing (etching) a part of the upper thickness of the second planarization layer **415***b* in which the reflection pattern RP is to be disposed. The groove pattern HP can have a predetermined depth by considering a height of the reflection pattern RP to be formed.
[0300] Further, according to the fourth embodiment of the present disclosure, when the reflection pattern RP has a lattice shape which divides the main emission area EA**1** into four or more, the groove pattern HP can also have a lattice shape which divides the main emission area EA**1** into four or more. In the plan view, the groove pattern HP can have a larger area than the reflection pattern RP to place the reflection pattern RP in the groove pattern HP.
[0301] For example, in the plan view, the reflection pattern RP can be a lattice shape, but can be separated to four rectangular shapes up, down, left, and right, but it not limited thereto. Therefore, the groove pattern HP also has a lattice shape overall, but can be separated to four rectangular shapes up, down, left, and right.
[0302] The groove pattern HP can be formed by the photo process.
[0303] The first bank **116** can be disposed on the second planarization layer **415***b* in which the groove pattern HP is formed.
[0304] According to the fourth embodiment of the present disclosure, a reflection pattern RP having an inclined side surface is disposed in the groove pattern HP of the second planarization layer **415***b*.
[0305] The reflection pattern RP can have an inclined side surface and a triangular cross-section overall, but is not limited thereto.
[0306] Further, the reflection pattern RP can be spaced apart from the first area **422***a* of the anode **422** by a predetermined distance.
[0307] The anode **422** can include a first area **422***a* which is disposed on the second planarization layer **415***b* to be in contact with the second planarization layer **415***b* and a second area **422***b* which extends from the first area **422***a* to be disposed on the side surface of the first bank **116**. The first area **422***a* has a surface substantially parallel to a surface of the substrate **111** and the second area **422***b* has a surface which has a predetermined angle with respect to the substrate **111**. Further, for example, the anode **422** can include a third area **422***c* which extends from the second area **422***b* in one direction to be electrically connected to the connection electrode **135** through a contact hole.
[0308] For example, the reflection pattern RP can be configured by a base layer **416***e* formed of an organic material and a reflective layer **422***e* formed of a reflective material, but is not limited thereto.
[0309] Further, according to the fourth embodiment of the present disclosure, a cut (ruptured) area CA in which the first area **422***a* of the anode **422** is cut (or removed) is provided around the reflection pattern RP. The cutting area CA can be located in the groove pattern HP around the reflection pattern RP.
[0310] The cutting area CA is formed by cutting (or removing) the first area **422***a* of the anode **422** around the reflection pattern RP to expose the second planarization layer **415***b* therebelow. Accordingly, the reflective layer **422***e* of the reflection pattern RP can be separated from the first area **422***a* of the anode **422**. For example, the reflection pattern RP can be electrically isolated.
[0311] The cutting area CA can be formed using the laser.
[0312] The light emitting diode **420** configured by the anode **422**, the organic layer **424**, and the cathode **426** can be disposed over the second planarization layer **415***b*.
[0313] The light emitting diode **420** and configurations thereabove are substantially the same as the first, second, and third embodiments described above so that a redundant description will be omitted.
[0314] The embodiments of the present disclosure can also be described as follows:

[0315] According to an aspect of the present disclosure, there is provided a display device. The display device includes a planarization layer disposed over a substrate, a first bank and a base layer disposed on the planarization layer, an anode which is disposed on the planarization layer, including a side surface of the first bank, a reflective layer disposed so as to cover the base layer, a second bank covering a part of the anode and the first bank and disposed over the anode and the first bank, an organic layer disposed over the substrate on which the second bank is disposed and a cathode disposed on the organic layer.
[0316] The display device can further comprise an encapsulation unit disposed over the cathode and a black matrix and a color filter layer disposed over the encapsulation unit.
[0317] The anode can include a first area which is disposed on the planarization layer to be in contact with the planarization layer, a second area which extends from the first area to be disposed on a side surface of the first bank and has a surface having a predetermined angle with respect to the substrate and a third area which extends from the second area in the other direction to be electrically connected to a thin film transistor through a contact hole.
[0318] The second bank can cover a part of an edge of the first area, the entire second area and the entire third area.
[0319] The base layer can be configured by the same organic material as the first bank.
[0320] The base layer can have an inclined side surface and a triangular cross-section.
[0321] The reflective layer can be configured by the same conductive material as the anode.
[0322] In a plan view, the base layer and the reflective layer can have a cross-shape or a lattice shape.
[0323] The reflective layer can be separated from the first area to be electrically isolated.
[0324] The base layer and the reflective layer can configure a reflection pattern.
[0325] A groove pattern can be configured by removing a part of an upper thickness in a partial area of the planarization layer and the reflection pattern can be disposed in the groove pattern.
[0326] The reflection pattern can have an inclined side surface and a triangular cross-section overall.
[0327] In a plan view, the reflection pattern can have a cross-shape or a lattice shape.
[0328] The reflection pattern can be disposed to be spaced apart from the first area with a predetermined distance.
[0329] A cutting area can be provided around the reflection pattern where the first area is cut and the cutting area can have a cross or lattice shape in accordance with a shape of the reflection pattern.
[0330] The cutting area can expose the planarization layer.
[0331] The organic layer can be disposed and extends over a top surface and a side portion of the reflection pattern, including the cutting area.
[0332] The second bank can be not disposed over the reflection pattern.
[0333] The second bank can include an open area configured by removing a part corresponding to a main emission area of each sub pixel, a first reflective emission area can be configured around the main emission area so as to correspond to the second area, and a second reflective emission area can be configured between the main emission areas so as to correspond to the reflective layer.
[0334] In a plan view, the main emission area can have a rectangular shape, the first reflective emission area can have a rectangular frame shape, and the second reflective emission area can have a cross-shape or the main emission area can have a circular shape, an oval shape, or a polygonal shape, the first reflective emission area can have a circular, oval, or polygonal frame shape, and the second reflective emission area can have the circular shape, the oval shape, or a lattice shape.
[0335] Although the embodiments of the present disclosure have been described in detail with reference to the accompanying drawings, the present disclosure is not limited thereto and can be embodied in many different forms without departing from the technical concept of the present disclosure. Therefore, the embodiments of the present disclosure are provided for illustrative

purposes only but not intended to limit the technical concept of the present disclosure. The scope of the technical concept of the present disclosure is not limited thereto.
[0336] Therefore, it should be understood that the above-described embodiments are illustrative in all aspects and do not limit the present disclosure. All the technical concepts in the equivalent scope of the present disclosure should be construed as falling within the scope of the present disclosure.

Claims

1. A display device, comprising: a planarization layer disposed over a substrate; a first bank and a base layer disposed over the planarization layer; an anode disposed over the planarization layer and a side surface of the first bank; a reflective layer disposed to cover the base layer; a second bank covering a part of the anode and the first bank and disposed over the anode and the first bank; an organic layer disposed over the substrate on which the second bank is disposed; and a cathode disposed over the organic layer.
2. The display device according to claim 1, further comprising: an encapsulation unit disposed over the cathode; and a black matrix and a color filter layer disposed over the encapsulation unit.
3. The display device according to claim 1, wherein the anode includes: a first area disposed over the planarization layer to be in contact with the planarization layer; a second area extending from the first area to be disposed over a side surface of the first bank, and including a surface having a predetermined angle with respect to the substrate; and a third area extending from the second area in another direction to be electrically connected to a thin film transistor through a contact hole.
4. The display device according to claim 3, wherein the second bank covers a part of an edge of the first area, the entire second area and the entire third area.
5. The display device according to claim 1, wherein the base layer includes a same organic material as the first bank.
6. The display device according to claim 1, wherein the base layer has an inclined side surface and a triangular cross-section.
7. The display device according to claim 1, wherein the reflective layer includes a same conductive material as the anode.
8. The display device according to claim 1, wherein in a plan view, the base layer and the reflective layer have a cross-shape or a lattice shape.
9. The display device according to claim 3, wherein the reflective layer is separated from the first area to be electrically isolated.
10. The display device according to claim 3, wherein the base layer and the reflective layer form a reflection pattern.
11. The display device according to claim 10, wherein a groove pattern is configured by removing a part of an upper thickness in a partial area of the planarization layer and wherein the reflection pattern is disposed in the groove pattern.
12. The display device according to claim 10, wherein the reflection pattern has an inclined side surface and a triangular cross-section overall.
13. The display device according to claim 10, wherein in a plan view, the reflection pattern has a cross-shape or a lattice shape.
14. The display device according to claim 10, wherein the reflection pattern is disposed to be spaced apart from the first area with a predetermined distance.
15. The display device according to claim 10, wherein a cutting area is provided around the reflection pattern where the first area is cut, and the cutting area has a cross or lattice shape in accordance with a shape of the reflection pattern.
16. The display device according to claim 15, wherein the cutting area exposes the planarization layer.
17. The display device according to claim 15, wherein the organic layer is disposed and extends

over a top surface and a side portion of the reflection pattern including the cutting area.

18. The display device according to claim 10, wherein the second bank is not disposed over the reflection pattern.

19. The display device according to claim 3, wherein the second bank includes an open area configured by removing a part corresponding to a main emission area of each sub pixel among a plurality of sub pixels, wherein a first reflective emission area is configured around the main emission area so as to correspond to the second area, and wherein a second reflective emission area is configured between the main emission areas so as to correspond to the reflective layer.

20. The display device according to claim 19, wherein in a plan view, the main emission area has a rectangular shape, the first reflective emission area has a rectangular frame shape, and the second reflective emission area has a cross-shape, or the main emission area has a circular shape, an oval shape, or a polygonal shape, the first reflective emission area has a circular, oval, or polygonal frame shape, and the second reflective emission area has a circular shape, an oval shape, or a lattice shape.