United States Patent Application Publication	20250261365
Kind Code	A1
Publication Date	August 14, 2025
Inventor(s)	JEONG; MOONYOUNG

SEMICONDUCTOR DEVICE INCLUDING VERTICAL CHANNEL TRANSISTORS

Abstract

A semiconductor device includes a peripheral structure disposed on a cell structure. The cell structure includes first and second memory blocks in a first horizontal direction. The peripheral structure includes first and second core circuit sections on the first and second memory blocks. Each of the first and second core circuit sections includes first peripheral transistors. Each of the first peripheral transistors includes an active pattern extending in a second horizontal direction perpendicular to the first horizontal direction, a first peripheral gate electrode adjacent to one sidewall of the active pattern, and a first peripheral impurity region and a second peripheral impurity region on a lower portion and an upper portion of the active pattern, respectively. In each of the first peripheral transistors, the first and second peripheral impurity regions are spaced apart from each other in a third direction perpendicular to the first and second horizontal directions.

Inventors: **JEONG; MOONYOUNG (Suwon-si, KR)**

Applicant: **Samsung Electronics Co., Ltd.** (Suwon-si, KR)

Family ID: **1000008113008**

Appl. No.: **18/823807**

Filed: **September 04, 2024**

Foreign Application Priority Data

KR	10-2024-0020417	Feb. 13, 2024

Publication Classification

Int. Cl.: **H10B12/00** (20230101); **H01L23/00** (20060101); **H01L25/00** (20060101); **H01L25/065** (20230101); **H01L25/18** (20230101); **H10B80/00** (20230101)

U.S. Cl.:

CPC **H10B12/50** (20230201); **H01L24/08** (20130101); **H01L24/80** (20130101); **H01L25/0657** (20130101); **H01L25/18** (20130101); **H01L25/50** (20130101); **H10B12/33** (20230201); **H10B80/00** (20230201); H01L2224/08145 (20130101); H01L2224/80006 (20130101); H01L2224/80895 (20130101); H01L2224/80896 (20130101); H01L2924/1431 (20130101); H01L2924/1436 (20130101)

Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This U.S. nonprovisional application claims priority under 35 U.S.C § 119 to Korean Patent Application No. 10-2024-0020417 filed on Feb. 13, 2024 in the Korean Intellectual Property Office, the disclosure of which is hereby incorporated by reference in its entirety.

BACKGROUND

[0002] The present inventive concepts relate to a semiconductor device, and more particularly, to a semiconductor device including vertical channel transistors.

[0003] As the design rules of semiconductor devices are reduced, fabrication techniques have been improved to enhance the integration, operating speed, and yield of these devices. To address these advancements, vertical channel transistors have been proposed to improve integration, resistance, current driving capability, and so forth.

SUMMARY

[0004] Some embodiments of the present inventive concepts provide a semiconductor device having improved electrical characteristics and increased integration.

[0005] The object of the present inventive concepts is not limited to the mentioned above, and other objects which have not been mentioned above will be clearly understood to those skilled in the art from the following description.

[0006] According to an aspect of the present disclosure, a semiconductor device includes a cell structure, and a peripheral structure disposed on the cell structure. The cell structure includes a first memory block and a second memory block that are side by side in a first horizontal direction. The peripheral structure includes a first core circuit section on the first memory block, and a second core circuit section on the second memory block. Each of the first and second memory blocks includes a plurality of cell transistors. Each of the first and second core circuit sections includes a plurality of first peripheral transistors. Each of the first peripheral transistors includes a first peripheral active pattern extending in a second horizontal direction perpendicular to the first horizontal direction, a first peripheral gate electrode adjacent to one sidewall of the first peripheral active pattern, and a first peripheral impurity region and a second peripheral impurity region on a lower portion and an upper portion of the first peripheral active pattern, respectively. In each of the plurality of first peripheral transistors, the first and second peripheral impurity regions are spaced apart from each other in a third direction perpendicular to the first and second horizontal directions.

[0007] According to an aspect of the present disclosure, a semiconductor device includes a substrate, and a pair transistor structure on the substrate. The pair transistor structure includes first, second, and third gate electrodes that are sequentially disposed in a first horizontal direction, a first active pattern between the first and second gate electrodes and extending in a vertical direction perpendicular to a top surface of the substrate, a second active pattern between the second and third gate electrodes and extending in the vertical direction perpendicular to the top surface of the substrate, a pair of first impurity regions on lower portions of the first and second active patterns, respectively, and a pair of second impurity regions on upper portions of the first and second active patterns, respectively. The pair of first impurity regions are spaced apart from the pair of second impurity regions, respectively, in the vertical direction. The first and second impurity regions,

among the pair of first and second impurity regions, of the first active pattern are doped with N-type impurities. The first and second impurity regions, among the pair of first and second impurity regions, of the second active pattern are doped with P-type impurities.

[0008] According to an aspect of the present disclosure, a semiconductor device includes a substrate, a plurality of pair transistor structures arranged in M rows and N columns on the substrate, and a plurality of wiring lines that connect the pair transistor structures with each other. Each of M and N is a natural number of equal to or greater than 2. Each of the pair transistor structures includes a left transistor and a right transistor that are symmetric with each other. Each of the left transistor and the right transistor includes an active pattern extending in a vertical direction perpendicular to a top surface of the substrate, a gate electrode adjacent to one side of the active pattern, a first impurity region on a lower portion of the active pattern, and a second impurity region on an upper portion of the active pattern. In each of the left transistor and the right transistor, the first impurity region and the second impurity region are spaced apart from each other in the vertical direction. The wiring lines include a first wiring line that connects the first impurity regions of the pair transistor structures with each other, a second wiring line that connects the second impurity regions of the pair transistor structures with each other, and a third wiring line that connects the gate electrodes of the pair transistor structures with each other.

Description

BRIEF DESCRIPTION OF DRAWINGS

[0009] FIG. **1**A illustrates a block diagram showing a semiconductor device according to some embodiments of the present inventive concepts.

[0010] FIG. **1**B illustrates a simplified perspective view showing a semiconductor memory device according to some embodiments of the present inventive concepts.

[0011] FIG. **2** illustrates a simplified perspective view showing a semiconductor device according to some embodiments of the present inventive concepts.

[0012] FIG. **3** illustrates a cross-sectional view taken along line A-A′ of FIG. **2**.

[0013] FIG. **4** illustrates a plan view illustrating a memory block according to some embodiments of the present inventive concepts.

[0014] FIG. **5**A illustrates a simplified enlarged view inversely showing section P**1** of FIG. **3**.

[0015] FIG. **5**B illustrates a detailed enlarged view inversely showing section P**1** of FIG. **3**.

[0016] FIG. **6** illustrates an enlarged view showing section P**2** of FIG. **3**.

[0017] FIG. **7**A illustrates an enlarged view showing section P**3** of FIG. **3**.

[0018] FIG. **7**B illustrates an enlarged view inversely showing section P**4** of FIG. **7**A.

[0019] FIG. **7**C illustrates an enlarged view showing section P**3** of FIG. **3**.

[0020] FIGS. **8**A to **8**J illustrate cross-sectional views showing a method of fabricating a semiconductor device of FIG. **3**.

[0021] FIGS. **9** and **10** illustrate cross-sectional views showing a semiconductor device according to some embodiments of the present inventive concepts.

[0022] FIG. **11** illustrates a cross-sectional view taken along line A-A′ of FIG. **2**.

[0023] FIGS. **12**A to **12**E illustrate cross-sectional views showing a method of fabricating a semiconductor device of FIG. **11**.

[0024] FIG. **13**A illustrates a cross-sectional view showing a semiconductor device according to some embodiments of the present inventive concepts.

[0025] FIGS. **13**B to **13**D illustrate circuit diagrams showing a semiconductor device that has a structure of FIG. **13**A.

[0026] FIGS. **14**A to **14**D illustrate cross-sectional views showing a semiconductor device according to some embodiments of the present inventive concepts.

[0027] FIGS. **15**A to **15**E illustrate cross-sectional views showing a semiconductor device according to some embodiments of the present inventive concepts.
[0028] FIG. **16**A illustrates a cross-sectional view showing a semiconductor device according to some embodiments of the present inventive concepts.
[0029] FIG. **16**B illustrates a circuit diagram showing a semiconductor device of FIG. **16**A.
[0030] FIG. **17**A illustrates a cross-sectional view showing a semiconductor device according to some embodiments of the present inventive concepts.
[0031] FIGS. **17**B and **17**C illustrate circuit diagrams showing a semiconductor device of FIG. **17**A.
[0032] FIG. **18**A illustrates a cross-sectional view showing a semiconductor device according to some embodiments of the present inventive concepts.
[0033] FIGS. **18**B and **18**C illustrate circuit diagrams showing a semiconductor device of FIG. **18**A.
[0034] FIG. **19**A illustrates a plan view showing a semiconductor device according to some embodiments of the present inventive concepts.
[0035] FIG. **19**B illustrates a cross-sectional view taken along line B-B′ of FIG. **19**A.
[0036] FIG. **20** illustrates a circuit diagram showing a logic transistor according to some embodiments of the present inventive concepts.
[0037] FIG. **21**A illustrates a plan view showing a logic transistor according to some embodiments of the present inventive concepts.
[0038] FIG. **21**B illustrates a cross-sectional view taken along line C-C′ of FIG. **21**A.
[0039] FIG. **22**A illustrates a plan view showing a logic transistor according to some embodiments of the present inventive concepts.
[0040] FIG. **22**B illustrates a cross-sectional view taken along line C-C′ of FIG. **22**A.
[0041] FIG. **23** illustrates a plan view showing a logic transistor according to some embodiments of the present inventive concepts.
[0042] FIG. **24**A illustrates a plan view showing a logic transistor according to some embodiments of the present inventive concepts.
[0043] FIG. **24**B illustrates a cross-sectional view taken along line C-C′ of FIG. **24**A.
[0044] FIG. **25** illustrates a plan view showing a logic transistor according to some embodiments of the present inventive concepts.
[0045] FIG. **26**A illustrates a plan view showing a logic transistor according to some embodiments of the present inventive concepts.
[0046] FIG. **26**B illustrates a cross-sectional view taken along line C-C′ of FIG. **26**A.

DETAILED DESCRIPTION OF EMBODIMENTS

[0047] A semiconductor device and a method of fabricating the same will hereinafter be discussed according to some embodiments of the present inventive concepts in conjunction with the accompanying drawings. In this description, the term “bottom electrode” may be called a first electrode, and the term “top electrode” may be called a second electrode. In this description, such terms as “first” and “second” may be used to simply distinguish identical or similar components from each other, and the sequence of such terms may be changed in accordance with the order of mention.
[0048] FIG. **1**A illustrates a block diagram showing a semiconductor device according to some embodiments of the present inventive concepts.
[0049] Referring to FIG. **1**A, a semiconductor memory device according to the present embodiment may include a cell array region **10**. The cell array region **10** may include word lines WL and bit lines BL that intersect each other. A plurality of memory cells MC may be two-dimensionally or three-dimensionally disposed on the cell array region **10**. Each of the memory cells MC may be connected between the word line WL and the bit line BL that cross each other.
[0050] A core circuit section **20** may be disposed around the cell array region **10**. The core circuit

section **20** may include a sub-word line driver **22** and a sense amplifier **24**. A peripheral circuit section **30** may be disposed around the core circuit section **20**. A row decoder **32**, a column decoder **34**, and a control logic **36** may be disposed on the peripheral circuit section **30**.

[0051] The row decoder **32** may decode a refresh address signal or a row address signal that is input from outside. In response to the row address signal or the refresh address signal, the sub-word line driver **22** may serve to select a specific word line WL.

[0052] In response to an address that is decoded from the column decoder **34**, the sense amplifier **24** may detect and amplify a voltage difference between a selected bit line BL and a reference bit line, and may then output the amplified voltage difference.

[0053] The column decoder **34** may provide a data delivery path between the sense amplifier **24** and an external device (e.g., a memory controller). The column decoder **34** may decode an address that is input from the outside and may select one of the bit lines BL.

[0054] The control logic **36** may generate control signals that control operations to write data to a memory cell array of the cell array region **10** and/or to read data from a memory cell array of the cell array region **10**.

[0055] FIG. **1**B illustrates a simplified perspective view showing a semiconductor memory device according to some embodiments of the present inventive concepts.

[0056] Referring to FIG. **1**B, a semiconductor memory device may include a substrate **100**, a peripheral structure PS, and a cell structure CS that are sequentially stacked. Unlike FIG. **1**B, the cell structure CS may be positioned between the substrate **100** and the peripheral structure PS. The peripheral structure PS may be called a peripheral circuit structure. The cell structure CS may be called a cell array structure.

[0057] The peripheral structure PS may include the core circuit section **20** and the peripheral circuit section **30** of FIG. **1**A. The core circuit section **20** may include sub-word line driver circuits SWD and sense amplifier circuits S/A. The peripheral circuit section **30** may include peripheral circuits PERI.

[0058] The cell structure CS may have various structures of a memory cell, such as dynamic random access memory (DRAM), vertical NAND (VNAND), Flash memory, resistive RAM (ReRAM), ferroelectric random access memory (FeRAM), phase change random access memory (PRAM), and static random access memory (SRA).

[0059] According to an embodiment, the cell structure CS may include bit lines BL, word lines WL, and memory cells MC between the bit lines BL and the word lines WL. The memory cells MC may be two-dimensionally or three-dimensionally arranged on a plane elongated in first and second directions D**1** and D**2** that intersect each other. Each of the memory cells MC may include a selection element TR and a data storage element DS.

[0060] The selection element TR may be a field effect transistor (FET). A gate electrode of a transistor may be connected to the word line WL, and source/drain terminals of the transistor may be correspondingly connected to the bit line BL and the data storage element DS. According to some embodiments, a vertical channel transistor (VCT) may be included as the selection element TR of each memory cell MC. The vertical channel transistor may have a structure in which a channel length extends in a direction (or a third direction D**3**) perpendicular to a top surface of the substrate **100**.

[0061] The data storage element DS may include a capacitor, a magnetic tunnel junction pattern, or a variable resistor. In the present embodiment, a capacitor may be provided as the data storage element DS of each memory cell MC.

[0062] FIG. **2** illustrates a simplified perspective view showing a semiconductor device according to some embodiments of the present inventive concepts.

[0063] Referring to FIG. **2**, in a semiconductor memory device, a cell structure CS and a peripheral structure PS may be sequentially stacked on a substrate **100**. The substrate **100** may be a silicon substrate, a silicon-on-insulator (SOI) substrate, or a dielectric substrate. The peripheral structure

PS may include a plurality of core circuit sections COR. For example, the peripheral structure PS may include a first peripheral circuit section PE(**1**) and first to eighth core circuit sections COR(**1**) to COR(**8**) that are two-dimensionally arranged along a first direction D**1** and a second direction D**2**. The first, third, fifth, and seventh core circuit sections COR(**1**), COR(**3**), COR(**5**), and COR(**7**) may be positioned in a front portion of the peripheral structure PS. The second, fourth, sixth, and eighth core circuit sections COR(**2**), COR(**4**), COR(**6**), and COR(**8**) may be positioned in a rear portion of the peripheral structure PS. The first peripheral circuit section PE(**1**) may be positioned in a region between the first, third, fifth, and seventh core circuit sections COR(**1**), COR(**3**), COR(**5**), and COR(**7**) and the second, fourth, sixth, and eighth core circuit sections COR(**2**), COR(**4**), COR(**6**), and COR(**8**). Although the present embodiment discloses eight core circuit sections COR, the number of core circuit sections is not limited thereto and may be less than eight or equal to or greater than nine. The arrangement of the first to eighth core circuit sections COR(**1**) to COR(**8**) and the first peripheral circuit section PE(**1**) may be variously changed without being limited to that of FIG. **2**.

[0064] The cell structure CS may include memory blocks BLK that are two-dimensionally arranged along the first direction D**1** and the second direction D**2**. Each of the memory blocks BLK may include various memory cells such as DRAM, VNAND, Flash memory, ReRAM, FeRAM, PRAM, and SRAM. The memory blocks BLK may include first to eighth memory blocks BLK(**1**) to BLK(**8**). The first, third, fifth, and seventh memory blocks BLK(**1**), BLK(**3**), BLK(**5**), and BLK(**7**) may be positioned in a front portion of the cell structure CS. The second, fourth, sixth, and eighth memory blocks BLK(**2**), BLK(**4**), BLK(**6**), and BLK(**8**) may be positioned in a rear portion of the cell structure CS.

[0065] The cell structure CS may further include a second peripheral circuit section PE(**2**) between the memory blocks BLK. The second peripheral circuit section PE(**2**) may be positioned in a space between the first, third, fifth, and seventh memory blocks BLK(**1**), BLK(**3**), BLK(**5**), and BLK(**7**) and the second, fourth, sixth, and eighth memory blocks BLK(**2**), BLK(**4**), BLK(**6**), and BLK(**8**). Although the present embodiment discloses eight memory blocks BLK, the number of the memory blocks BLK is not limited thereto and may be less than eight or equal to or greater than nine. The arrangement of the first to eighth memory blocks BLK(**1**) to BLK(**8**) and the second peripheral circuit section PE(**2**) may be variously changed without being limited to that of FIG. **2**. The cell structure CS may exclude the second peripheral circuit section PE(**2**).

[0066] The first to eighth memory blocks BLK(**1**) to BLK(**8**) may respectively vertically overlap the first to eighth core circuit sections COR(**1**) to COR(**8**). The first to eighth memory blocks BLK(**1**) to BLK(**8**) may be respectively connected to the first to eighth core circuit sections COR(**1**) to COR(**8**). The second peripheral circuit section PE(**2**) may vertically overlap the first peripheral circuit section PE(**1**). The second peripheral circuit section PE(**2**) may be connected to the first peripheral circuit section PE(**1**). Each of the first to eighth memory blocks BLK(**1**) to BLK(**8**) may include the bit lines BL, the word lines WL, and the memory cells MC that are discussed with reference to FIGS. **1**A and **1**B. Each of the first to eighth core circuit sections COR(**1**) to COR(**8**) may include the sub-word line driver **22** and the sense amplifier **24** that are discussed with reference to FIG. **1**A. The row decoders **32**, the column decoders **34**, and the control logics **36** may be disposed on the first peripheral circuit section PE(**1**) and the second peripheral circuit section PE(**2**).

[0067] FIG. **3** illustrates a cross-sectional view taken along line A-A′ of FIG. **2**. FIG. **4** illustrates a plan view illustrating a memory block according to some embodiments of the present inventive concepts. First and second memory blocks BLK(**1**) and BLK(**2**) of FIG. **3** may correspond to a cross-section taken along line A-A′ of FIG. **4**.

[0068] Referring to FIGS. **2** and **3**, a cell structure CS and a peripheral structure PS may be sequentially stacked on a substrate **100**. The substrate **100** may be a silicon substrate, a silicon-on-insulator (SOI) substrate, or a dielectric substrate.

[0069] Referring to FIGS. **2** to **4**, the cell structure CS may include first to eighth memory blocks BLK(**1**) to BLK(**8**) and a second peripheral circuit section PE(**2**). Each of the first to eighth memory blocks BLK(**1**) to BLK(**8**) may include cell connection pads CP**2**, a cell interlayer dielectric layer IL, cell transistors CTR, bit lines BL, shield lines SHL, word lines WL, back gate lines BGL, cell capacitors CAP**1**, first to fourth cell wiring lines IT**1** to IT**4**, and first to third cell contact plugs CT**1** to CT**3**. The cell interlayer dielectric layer IL may have a single-layered or multi-layered structure of at least one selected from silicon oxide, silicon nitride, silicon oxynitride, and porous dielectrics. The second peripheral circuit section PE(**2**) may include third peripheral transistors PTR**3**, peripheral capacitors CAP**2**, first to fourth cell wiring lines IT**1** to IT**4**, and first to third cell contact plugs CT**1** to CT**3**.
[0070] There are no limitations to those shown in figures, but there may be various changes in terms of the number, height, thickness, and stacking numbers of the cell connection pads CP**2**, the cell interlayer dielectric layer IL, the cell transistors CTR, the bit lines BL, the shield lines SHL, the word lines WL, the back gate lines BGL, the cell capacitors CAP**1**, the first to fourth cell wiring lines IT**1** to IT**4**, the first to third cell contact plugs CT**1** to CT**3**, the third peripheral transistors PTR**3**, and the peripheral capacitors CAP**2**.
[0071] The cell connection pads CP**2** may be in contact with corresponding peripheral connection pads CP**1**. The cell interlayer dielectric layer IL may have a top surface in contact with a bottom surface of a peripheral interlayer dielectric layer PL. The first cell wiring line IT**1** may be connected to first terminals of the third peripheral transistors PTR**3**. The second cell wiring line IT**2** may be connected to second terminals of the third peripheral transistors PTR**3** and the cell transistors CTR. The third cell wiring lines IT**3** may be connected to top electrodes UE of the peripheral capacitors CAP**2** and the cell capacitors CAP**1**. The fourth cell wiring line IT**4** may connect the first cell wiring line IT**1** to the cell connection pad CP**2**. The third cell wiring lines IT**3** may be thicker than the fourth cell wiring line IT**4**.
[0072] The first cell contact plug CT**1** may connect the third cell wiring line IT**3** to the second cell wiring line IT**2**. The second cell contact plugs CT**2** may be connected to corresponding third cell wiring lines of the third cell wiring lines IT**3**, respectively. The third cell contact plug CT**3** may connect the cell connection pad CP**2** to the fourth cell wiring lines IT**4** or may connect the cell connection pad CP**2** to the second cell wiring line IT**2**.
[0073] The following description will focus on the first to eighth memory blocks BLK(**1**) to BLK(**8**).
[0074] Referring to FIGS. **3** and **4**, the bit lines BL and the shield lines SHL may extend in a second direction D**2** and may be spaced apart from each other in a first direction D**1**. The shield lines SHL may be correspondingly interposed between the bit lines BL. The bit lines BL and the shield lines SHL may be located at the same level. The second direction D**2** may be perpendicular to the first direction D**1**. In an embodiment, each of the shield lines SHL and each of the bit lines BL may be alternately arranged in the first direction D**1**.
[0075] A bit-line contact plug BLC may penetrate a portion of the cell interlayer dielectric layer IL to contact the bit line BL. A shield-line contact plug SHC may penetrate a portion of the cell interlayer dielectric layer IL to contact the shield line SHL. A word-line contact plug WLC may penetrate a portion of the cell interlayer dielectric layer IL to contact the word line WL. A back gate contact plug BGC may penetrate a portion of the cell interlayer dielectric layer IL to come into connection with the back gate line BGL. The term “contact,” as used herein, refers to a direct connection (i.e., physical touching) unless the context indicates otherwise.
[0076] FIG. **5**A illustrates a simplified enlarged view inversely showing section P**1** of FIG. **3**.
[0077] Referring to FIGS. **2** to **5**A, the cell transistors CTR may be disposed on each of the first to eighth memory blocks BLK(**1**) to BLK(**8**). The cell transistors CTR may correspond to the selection element TR of FIG. **1**B. The cell transistors CTR may correspondingly include active patterns AP. In this description, the term “active pattern AP” may be called a cell active pattern to

distinguish from a peripheral active pattern PAP of FIG. **6**. The active patterns AP may include a pair of first and second active patterns AP(**1**) and AP(**2**) that are adjacent to each other in the second direction D**2**. Each of the pair of active patterns AP(**1**) and AP(**2**) may include a channel region CH and first and second impurity regions IM**1** and IM**2**. The first impurity regions IM**1** of the active patterns AP may be in contact with the bit lines BL. The second impurity regions IM**2** of the active patterns AP may be in contact with storage node contacts BC. For example, the first impurity region IM**1**, the channel region CH, and the second impurity region IM**2** may be arranged in the third direction D**3**. The first and second impurity regions IM**1** and IM**2** may be disposed at a lower surface of the channel region CH and an upper surface of the channel region CH, respectively.

[0078] The word lines WL may include a pair of first and second word lines WL(**1**) and WL(**2**) that are adjacent to each other in the second direction D**2**. The first word line WL(**1**) may be adjacent to the channel region CH of the first active pattern AP(**1**). The second word line WL(**2**) may be adjacent to the channel region CH of the second active pattern AP(**2**). In an embodiment, the pair of active patterns AP(**1**) and AP(**2**) may be disposed in a space between the first word line WL(**1**) and the second word line WL(**2**). The configuration of the pair of word lines WL(**1**) and WL(**2**) and the pair of active patterns AP(**1**) and AP(**2**) may be repeatedly arranged along the second direction D**2** to form each of the first to eighth memory blocks BLK(**1**) to BLK(**8**).

[0079] First gate dielectric layers Gox**1** may be disposed between the first and second word lines WL(**1**) and WL(**2**) and the first and second active patterns AP(**1**) and AP(**2**), respectively. The first gate dielectric layers Gox**1** may extend lengthwise in the first direction D**1** parallel to the first and second word lines WL(**1**) and WL(**2**).

[0080] The back gate line BGL may be interposed between a pair of first and second active patterns AP(**1**) and AP(**2**). The word lines WL and the back gate lines BGL may extend lengthwise along the first direction D**1** as shown in FIG. **4**. A second gate dielectric layer Gox**2** may be disposed between the back gate line BGL and each of the first and second active patterns AP(**1**) and AP(**2**). The first gate dielectric layers Gox**1** and the second gate dielectric layer Gox**2** may each be formed of, for example, a single layer or multiple layers including at least one selected from a silicon oxide layer, a silicon oxynitride layer, and a high-k dielectric layer whose a dielectric constant is greater than a dielectric constant of a silicon oxide layer. The high-k dielectric layer may be formed of metal oxide or metal oxynitride. For example, the high-k dielectric layer used as the first and second gate dielectric layers Gox**1** and Gox**2** may be formed of HfO.sub.2, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, ZrO.sub.2, Al.sub.2O.sub.3, or a combination thereof, but the present inventive concepts are not limited thereto. According to some embodiments, the second gate dielectric layer Gox**2** may be formed of a single layer or multiple layers including a dielectric material whose a dielectric constant is less than a dielectric contestant of a silicon oxide layer. For example, the second gate dielectric layer Gox**2** may include SiOCH or an air gap. In some embodiments, the dielectric constant of the second gate dielectric layer Gox**2** may be smaller than the dielectric constant of the first gate dielectric layer Gox**1**. In some embodiments, the back gate line BGL may be disposed in a space between the pair of active patterns AP(**1**) and AP(**2**) which are repeatedly disposed in each of the first to eighth memory blocks BLK(**1**) to BLK(**8**). No back gate line may be present in a space between two pairs of active patterns AP(**1**) and AP(**2**) which are repeatedly disposed in each of the first to eighth memory blocks BLK(**1**) to BLK(**8**), and no active pattern may be present in a space between two pairs of word lines WL(**1**) and WL(**2**) which are repeatedly disposed in each of the first to eighth memory blocks BLK(**1**) to BLK(**8**). The term “air” as discussed herein, may refer to atmospheric air, or other gases that may be present during the manufacturing process.

[0081] The first gate dielectric layers Gox**1** may have a first thickness T**1**. The second gate dielectric layer Gox**2** may have a second thickness T**2**. The first thickness T**1** may be the same as or different from the second thickness T**2**. The second gate dielectric layer Gox**2** may be called a back

gate dielectric layer.
[0082] A portion of the first word line WL(**1**) and the first active pattern AP(**1**) adjacent thereto may constitute a left cell transistor CTR(L). A portion of the second word line WL(**2**) and the second active pattern AP(**2**) adjacent thereto may constitute a right cell transistor CTR(R). The left cell transistor CTR(L) and the right cell transistor CTR(R) may constitute a cell transistor structure CTS. In some embodiments, the portion of the first word line WL(**1**) may overlap the first active pattern AP(**1**) in the second direction D**2** to form the left cell transistor CTR(L), and the portion of the second word line WL(**2**) may overlap the second active pattern AP(**2**) in the second direction D**2**.
[0083] FIG. **5**B illustrates a detailed enlarged view inversely showing section P**1** of FIG. **3**.
[0084] Referring to FIG. **5**B, each of the bit lines BL may include a polysilicon pattern **161** and a metal pattern **163** that are sequentially stacked. Although not shown in FIG. **5**B, each of the shield lines SHL may have at least one of a poly silicon pattern corresponding to the polysilicon pattern **161** of each of the bit lines BL and a metal pattern corresponding to the metal pattern **163** of each of the bit lines BL. Each of the bit lines BL may have a top surface at a level which is the same as or different from a level of a top surface of each of the shield lines SHL. Each of the bit lines BL may have a bottom surface at a level which is the same as or different from a level of a bottom surface of each of the shield lines SHL. The metal pattern **163** may include or may be formed of one or more of conductive metal nitride (e.g., titanium nitride or tantalum nitride) and metal (e.g., tungsten, titanium, or tantalum). The metal pattern **163** may include or may be formed of metal silicide, such as titanium silicide, cobalt silicide, and nickel silicide.
[0085] Referring to FIGS. **5**A and **5**B, the active patterns AP may be formed of a monocrystalline semiconductor material, an oxide semiconductor material, or a two-dimensional semiconductor material. The oxide semiconductor material may be indium-gallium-zinc oxide. The two-dimensional semiconductor material may be MoS.sub.2, WS.sub.2, MoSe.sub.2, or WSe.sub.2. For example, the active patterns AP may be formed of single crystalline silicon.
[0086] Each of the first active pattern AP(**1**) and the second active pattern AP(**2**) may have a length in the first direction D**1** as shown in FIG. **4**, a width in the second direction D**2**, and a height in a third direction D**3** perpendicular to the first and second directions D**1** and D**2**. Each of the first active pattern AP(**1**) and the second active pattern AP(**2**) may have a substantially uniform width. Each of the first active pattern AP(**1**) and the second active pattern AP(**2**) may have a width of several nanometers to tens nanometers. For example, each of the first active pattern AP(**1**) and the second active pattern AP(**2**) may have a width of about 1 nm to about 30 nm, for example, about 1 nm to about 10 nm. Each of the first active pattern AP(**1**) and the second active pattern AP(**2**) may have a length greater than a line-width of the bit line BL.
[0087] Referring to FIG. **5**B, each of the first active pattern AP(**1**) and the second active pattern AP(**2**) may have a first surface S**1** and a second surface S**2** that are opposite to each other in the third direction D**3**. For example, the first surfaces S**1** of the first and second active patterns AP(**1**) and AP(**2**) may be in contact with the polysilicon pattern **161** of the bit line BL or with the metal pattern **163** when the polysilicon pattern **161** is omitted. The second surfaces S**2** of the first and second active patterns AP(**1**) and AP(**2**) may be in contact with the storage node contacts BC, respectively.
[0088] Each of the first active pattern AP(**1**) and the second active pattern AP(**2**) may have a first lateral surface SS**1** and a second lateral surface SS**2** that are opposite to each other in the second direction D**2**. The first lateral surface SS**1** of the first active pattern AP(**1**) may be adjacent to the first word line WL(**1**), and the second lateral surface SS**2** of the second active pattern AP(**2**) may be adjacent to the second word line WL(**2**). For example, the first lateral surface SS**1** of the first active pattern AP(**1**) may be adjacent to the first word line WL(**1**), and the second lateral surface SS**2** of the first active pattern AP(**1**) may be adjacent to the back gate line BGL. The first lateral surface SS**1** of the second active pattern AP(**2**) may be adjacent to the second word line WL(**2**), and the

second lateral surface SS**2** of the second active pattern AP(**2**) may be adjacent to the back gate line BGL.
[0089] The first and second impurity regions IM**1** and IM**2** may be regions doped with N-type or P-type impurities in each of the first and second active patterns AP(**1**) and AP(**2**). The channel region CH may not be doped with impurities or may be doped with impurities whose a conductivity type is different from a conductivity type of impurities doped in the first and second impurity regions IM**1** and IM**2**.
[0090] The channel regions CH of the first and second active patterns AP(**1**) and AP(**2**) may be controlled by the first and second word lines WL(**1**) and WL(**2**) and the back gate lines BGL when a semiconductor device is operated.
[0091] Referring to FIGS. **4** and **5**B, the back gate lines BGL may be disposed spaced apart at a certain interval from each other in the second direction D**2** on the bit lines BL. The back gate lines BGL may extend lengthwise in the first direction D**1** across the bit lines BL.
[0092] When viewed in a vertical direction, the back gate lines BGL may have a height less than that of the first active pattern AP(**1**) and the second active pattern AP(**2**). The back gate line BGL may have a first surface adjacent to the bit line BL and a second surface adjacent to the storage node contact BC. The first and second surfaces of the back gate line BGL may be vertically spaced apart from the first and second surfaces S**1** and S**2** of each of the first and second active patterns AP(**1**) and AP(**2**), respectively.
[0093] Each of the back gate lines BGL may have a top surface at a level which is the same as or different from a level of a top surface of each of the word lines WL. Each of the back gate lines BGL may have a bottom surface at a level which is the same as or different from that of a bottom surface of each of the word lines WL.
[0094] The first word line WL(**1**), the second word line WL(**2**), and the back gate line BGL may include or may be formed of, for example, doped polysilicon, conductive metal nitride (e.g., titanium nitride or tantalum nitride), metal (e.g., tungsten, titanium, or tantalum), conductive metal silicide, conductive metal oxide, or a combination thereof.
[0095] The back gate line BGL may be provided with a negative voltage when a semiconductor memory device is operated, and may increase a threshold voltage of a vertical channel transistor. For example, as the vertical channel transistor reduces in size, a threshold voltage of the vertical transistor may be lowered, thereby increasing a leakage current. With the back gate line BGL supplied with a negative voltage, the reduction of the threshold voltage in the vertical channel transistor may be compensated, thereby preventing the increase of a leakage current.
[0096] A portion of the cell interlayer dielectric layer IL may include layers **111**, **115**, Gox**1**, Gox**2**, **131**, **141**, **143**, **153**, **155**, **210**, **231**, and **245** each of which is formed of a dielectric material. A first dielectric pattern **111** may be disposed between the first active pattern AP(**1**) and the second active pattern AP(**2**) that are adjacent to each other in the second direction D**2**. The first dielectric pattern **111** may be disposed between the second impurity regions IM**2** of the first and second active patterns AP(**1**) and AP(**2**). The first dielectric pattern **111** may include or may be formed of, for example, a silicon oxide layer, a silicon nitride layer, or a silicon oxynitride layer.
[0097] The second gate dielectric layer Gox**2** may be disposed between the back gate line BGL and each of the first and second active patterns AP(**1**) and AP(**2**) and between the back gate line BGL and the first dielectric pattern **111**. The second gate dielectric layer Gox**2** may include vertical parts that cover opposite lateral surfaces of the back gate line BGL and a horizontal part that connects the vertical parts to each other. The horizontal part of the second gate dielectric layer Gox**2** may be closer to the storage node contact BC than the bit line BL, and may cover the second surface of the back gate line BGL. The horizontal part of the second gate dielectric layer Gox**2** may be disposed between the back gate line BGL and the first dielectric pattern **111**.
[0098] A back gate capping pattern **115** may be disposed between the back gate line BGL and the bit line BL. The back gate capping pattern **115** may be formed of a dielectric material, and may

have a bottom surface in contact with the polysilicon pattern **161** of the bit line BL. The back gate capping pattern **115** may be disposed between the vertical parts of the second gate dielectric layer Gox**2**. In some embodiments, the back gate capping pattern **115** may extend in the first direction D**1** along the first surface, adjacent to the bit line BL, of the back gate line BGL. A thickness of a portion of the back gate capping pattern **115** between the bit lines BL may be different from a thickness of a portion of the back gate capping pattern **115** on the bit lines BL.

[0099] The first gate dielectric layer Gox**1** may cover the first lateral surface SS**1** of the first active pattern AP(**1**) and the second lateral surfaces SS**2** of the second active pattern AP(**2**). The first gate dielectric layer Gox**1** may have a substantially uniform thickness. Each of the first gate dielectric layers Gox**1** may include a vertical part VP adjacent to the first and second active patterns AP(**1**) and AP(**2**) and a horizontal part HP that protrudes in the second direction D**2** from the vertical part VP. For example, the vertical part VP may extend in the third direction D**3** along the first lateral surface SS**1** of each of the first and second active patterns AP(**1**) and AP(**2**). The horizontal part HP may be connected to an upper end of the vertical part VP and expend in the second direction D**2** and away from a corresponding one of the first and second active patterns AP(**1**) and AP(**2**).

[0100] For example, a pair of first and second word lines WL(**1**) and WL(**2**) may be disposed on the horizontal part HP of each of the first gate dielectric layers Gox**1**. The first gate dielectric layers Gox**1** may be disposed spaced apart from each other, and may be mirror-symmetric with each other.

[0101] A second dielectric pattern **143** may be disposed between the storage node contact BC and the horizontal part HP of the first gate dielectric layer Gox**1**. For example, the second dielectric pattern **143** may include or may be formed of silicon oxide. First and second etch stop layers **131** and **141** may be disposed between the second dielectric pattern **143** and the second impurity regions IM**2** of the first and second active patterns AP(**1**) and AP(**2**).

[0102] On the first gate dielectric layer Gox**1**, a third dielectric pattern **155** may separate the first and second word lines WL(**1**) and WL(**2**) from each other. The third dielectric pattern **155** may extend in the first direction D**1** between the first and second word lines WL(**1**) and WL(**2**). A first capping layer **153** may be disposed between the third dielectric pattern **155** and the first and second word lines WL(**1**) and WL(**2**). The first capping layer **153** may have a substantially uniform thickness.

[0103] The storage node contacts BC may penetrate an interlayer dielectric layer **231**, an upper dielectric layer **245**, and an etch stop layer **210** to be correspondingly coupled to the first and second active patterns AP(**1**) and AP(**2**). The storage node contacts BC may have a lower width greater than an upper width. The upper dielectric layer **245** may separate neighboring storage node contacts BC from each other. When viewed in a plan view, each of the storage node contacts BC may have a circular shape, an oval shape, a rectangular shape, a square shape, a rhombic shape, a hexagonal shape, or any other suitable shape. The storage node contacts BC may be arranged in a matrix shape along the first direction D**1** and the second direction D**2**. The storage node contacts BC may be formed of doped polysilicon, Al, Cu, Ti, Ta, Ru, W, Mo, Pt, Ni, Co, TiN, TaN, WN, NON, TiAl, TiAlN, TiSi, TiSiN, TaSi, TaSiN, Ru, TiN, NiSi, CoSi, IrOx, RuOx, or a combination thereof, but the present inventive concepts are not limited thereto.

[0104] Referring to FIG. **3**, landing pads LP may be disposed underneath the storage node contacts BC. When viewed in a plan view, each of the landing pads LP may have a circular shape, an oval shape, a rectangular shape, a square shape, a rhombic shape, a hexagonal shape, or any other suitable shape. The landing pads LP may completely or partially vertically overlap the storage node contacts BC. When viewed in a plan view, the landing pads LP may be arranged in a matrix shape along the first direction D**1** and the second direction D**2**. In some embodiments, the landing pads LP may be arranged in a honeycomb shape when viewed in a plan view. The landing pads LP may be formed of doped polysilicon, Al, Cu, Ti, Ta, Ru, W, Mo, Pt, Ni, Co, TiN, TaN, WN, NbN, TiAl, TiAlN, TiSi, TiSiN, TaSi, TaSiN, RuTiN, NiSi, CoSi, IrOx, RuOx, or a combination thereof, but the

present inventive concepts are not limited thereto.
[0105] The cell capacitors CAP**1** may be correspondingly connected to the landing pads LP. The cell capacitors CAP**1** may have an inverse structure. For example, bottom electrodes BE may be positioned above a top electrode UE.
[0106] The bottom electrodes BE may be correspondingly disposed underneath the landing pads LP. The bottom electrodes BE may be correspondingly electrically connected to the first and second active patterns AP(**1**) and AP(**2**). Each of the bottom electrodes BE may have a pillar shape or a hollow cup shape.
[0107] The bottom electrodes BE may be disposed in a honeycomb shape or a matrix shape along the first direction D**1** and the second direction D**2**. The bottom electrodes BE may completely or partially overlap the landing pads LP. The bottom electrodes BE may be entirely or partially in contact with bottom surfaces of the landing pads LP, respectively. There may be a constant interval between the bottom electrodes BE. The bottom electrodes BE may include at least one selected from impurity-doped silicon, metal, metal oxide, and metal nitride. For example, the bottom electrodes BE may include a titanium nitride layer.
[0108] The bottom electrodes BE may have their lower sidewalls in partial contact with support patterns SSP. The support patterns SSP may prevent collapse of the bottom electrodes BE. When viewed in a plan view, the support patterns SSP may have a mesh shape or a plate shape in which a plurality of apertures are formed. The support patterns SSP may be formed of either one layer or two or more layers. The support patterns SSP may be formed of, for example, a single layer or multiple layers including at least one of a silicon nitride (SiN) layer, a silicon boronitride (SiBN) layer, and a silicon carbonitride (SiCN) layer.
[0109] A dielectric layer DL may conformally cover the bottom electrodes BE and the support patterns SSP. The dielectric layer DL may be formed of a single or multiple layers including at least one of, for example, a silicon oxide layer and a metal oxide layer such as an aluminum oxide layer having a material whose a dielectric constant is greater than a dielectric constant of a silicon oxide layer. The dielectric layer DL may have a single-layered or a multi-layered structure of at least one of a ferroelectric layer and an antiferroelectric layer. The dielectric layer DL may have a bottom surface covered with the top electrode UE. The top electrode UE may be formed to have a single-layered or a multi-layered structure including at least one of a titanium nitride layer, a tungsten layer, an impurity-doped polysilicon layer, and an impurity-doped silicon-germanium layer. The top electrode UE may have a sidewall aligned with that of the dielectric layer DL.
[0110] The bottom electrodes BE, the dielectric layer DL, and the top electrode UE may constitute the cell capacitors CAP**1**. The cell capacitors CAP**1** may correspond to the data storage element DS of FIG. **1**B.
[0111] In the present inventive concepts, as shown in FIGS. **1**A to **3**, each of the memory cells MC of the cell structure CS is illustrated to have a 1T1C (1-transistor, 1-capacitor) structure in which one VCT structured cell transistor CTR is connected to one cell capacitor CAP**1**, but the present inventive concepts are not limited thereto. The dielectric layer DL may be formed of a ferroelectric material, and in this case, each of the memory cells MC may have a 1T1F (1-transistor, 1-ferroelectric capacitor) structure. In some embodiments, one cell transistor CTR may be connected to n numbers of cell capacitors CAP**1** (where, n is a natural number equal to or greater than 2), and in this case, each of the memory cells MC may have a 1TnC (1-transistor, n-capacitor) structure. Each of the memory cells MC may have a vertically stacked dynamic random access memory (VS-DRAM) structure in which the active patterns AP are horizontally elongated and vertically stacked and in which the bottom electrode BE is positioned on sides of the active patterns AP. In some embodiments, each of the memory cells MC may have a 1T (1-transistor) DRAM structure formed of the cell transistors CTR without the cell capacitor CAP**1**.
[0112] The following description will focus on the first peripheral circuit section PE(**1**) and the second peripheral circuit section PE(**2**).

[0113] Referring to FIG. **3**, the peripheral structure PS may include first and second peripheral transistors PTR**1** and PTR**2**, first to fourth peripheral contact plugs PC**1** to PC**4**, first to third peripheral wiring lines PI**1** to PI**3**, a peripheral interlayer dielectric layer PL, and peripheral connection pads CP**1**.
[0114] There are no limitations to those shown in figures, but there may be various changes in terms of the number, height, thickness, and stacking numbers of the first and second peripheral transistors PTR**1** and PTR**2**, the first to fourth peripheral contact plugs PC**1** to PC**4**, the first to third peripheral wiring lines PI**1** to PI**3**, the peripheral interlayer dielectric layer PL, and the peripheral connection pads CP**1**.
[0115] Each of the first and second peripheral transistors PTR**1** and PTR**2** may have a VCT shape. Each of the first and second peripheral transistors PTR**1** and PTR**2** may be connected to the first and second peripheral wiring lines PI**1** and PI**2**. The first peripheral contact plug PC**1** may connect the first and second peripheral wiring lines PI**1** and PI**2** with each other. Each of the first, second, and third peripheral wiring lines PI**1**, PI**2**, and PI**3** may be formed of multi-layers. The peripheral interlayer dielectric layer PL may cover the peripheral contact plugs PC**1**, PC**2**, PC**3**, and PC**4** and the peripheral wiring lines PI**1**, PI**2**, and PI**3**. The third peripheral wiring line PI**3** may have a thickness greater than thicknesses of the first and second peripheral wiring lines PI**1** and PI**2**. The second peripheral contact plugs PC**2** may be connected to the second peripheral wiring lines PI**2**. The third peripheral contact plugs PC**3** may be connected to the third peripheral wiring lines PI**3**. The peripheral connection pads CP**1** may be disposed on a bottom end of the peripheral interlayer dielectric layer PL. The fourth peripheral contact plugs PC**4** may connect the peripheral connection pads CP**1** to the first peripheral wiring lines PI**1**, respectively.
[0116] The peripheral connection pads CP**1**, the peripheral contact plugs PC**1**, PC**2**, PC**3**, and PC**4**, and the peripheral wiring lines PI**1**, PI**2**, and PI**3** may each include metal, such as copper, aluminum, tungsten, titanium, tantalum, titanium nitride, and tantalum nitride. The peripheral interlayer dielectric layer PL may have a single-layered or a multi-layered structure of at least one of silicon oxide, silicon nitride, silicon oxynitride, SiCN, and porous dielectrics.
[0117] On each of the core circuit sections COR(**1**) to COR(**8**), the first peripheral transistors PTR**1**, the first to fourth peripheral contact plugs PC**1** to PC**4**, and the first to third peripheral wiring lines PI**1** to PI**3** may constitute the sense amplifiers **24** and the sub-word line drivers **22**.
[0118] On the first peripheral circuit section PE(**1**), the second peripheral transistors PTR**2**, the first to fourth peripheral contact plugs PC**1** to PC**4**, and the first to third peripheral wiring lines PI**1** to PI**3** may constitute portions of the row decoders **32**, the column decoders **34**, and the control logics **36**.
[0119] FIG. **6** illustrates an enlarged view showing section P**2** of FIG. **3**. FIG. **6** depicts a cross-section of the first peripheral transistor PTR**1**.
[0120] Referring to FIGS. **3** and **6**, the first peripheral transistors PTR**1** may include peripheral active patterns PAP and a peripheral gate electrode GE adjacent thereto. The peripheral active patterns PAP may include a pair of first and second peripheral active patterns PAP(**1**) and PAP(**2**) that are adjacent to each other.
[0121] The peripheral active patterns PAP may be formed of a monocrystalline semiconductor material, an oxide semiconductor material, or a two-dimensional semiconductor material. The oxide semiconductor material may be indium-gallium-zinc oxide. The two-dimensional semiconductor material may be MoS.sub.2, WS.sub.2, MoSe.sub.2, or WSe.sub.2. For example, the peripheral active patterns PAP may be formed of single crystalline silicon.
[0122] A channel region CH and first and second impurity regions IM**1** and IM**2** may be disposed on each of the peripheral active patterns PAP. The first impurity regions IM**1** of the peripheral active patterns PAP may be in contact with the first peripheral wiring line PI**1**. The second impurity regions IM**2** of the peripheral active patterns PAP may be in contact with conductive patterns BP. The conductive patterns BP may include or may be formed of the same material as a material of the

storage node contacts BC. The conductive patterns BP may be formed of metal, impurity-doped silicon, SiGe, or SiC. Impurities doped in the conductive patterns BP and impurities doped in the first and second impurity regions IM**1** and IM**2** may have the same conductivity type.

[0123] The conductivity type of impurities doped in the first and second impurity regions IM**1** and IM**2** of the first peripheral transistors PTR**1** of FIG. **6** may be the same as or different from the conductivity type of impurities doped in the first and second impurity regions IM**1** and IM**2** of the cell transistors CTR of FIG. **5**A. The first and second impurity regions IM**1** and IM**2** of the first peripheral transistors PTR**1** of FIG. **6** may be doped with first impurities at a first concentration, and the first and second impurity regions IM**1** and IM**2** of the cell transistors CTR of FIG. **5**A may be doped with the first impurities at a second concentration. The second concentration may be less than the first concentration.

[0124] A first peripheral gate electrode GE(**1**) may be adjacent to the channel region CH of the first peripheral active pattern PAP(**1**). A second peripheral gate electrode GE(**2**) may be adjacent to the channel region CH of the second peripheral active pattern PAP(**2**). The first gate dielectric layer Gox**1** may be disposed between the peripheral gate electrodes GE and the peripheral active pattern PAP. A peripheral back gate electrode BG may be interposed between a pair of first and second peripheral active patterns PAP(**1**) and PAP(**2**). The second gate dielectric layer Gox**2** may be disposed between the peripheral back gate electrodes BG and the peripheral active pattern PAP.

[0125] The first peripheral gate electrode GE(**1**) and the first peripheral active pattern PAP(**1**) adjacent thereto may constitute a first left peripheral transistor PTR**1**(L). The second peripheral gate electrode GE(**2**) and the second peripheral active pattern PAP(**2**) adjacent thereto may constitute a first right peripheral transistor PTR**1**(R). The first left peripheral transistor PTR**1**(L) and the first right peripheral transistor PTR**1**(R) may constitute a first pair transistor structure PTS**1**.

[0126] A material included in each of the first and second gate dielectric layers Gox**1** and Gox**2** of the first pair transistor structure PTS**1** of FIG. **6** may be the same as or different from a material included in each of the first and second gate dielectric layers Gox**1** and Gox**2** of the cell transistor structure CTS of FIG. **5**A. The first gate dielectric layers Gox**1** of the first pair transistor structure PTS**1** may have a third thickness T**3**. The second gate dielectric layers Gox**2** of the first pair transistor structure PTS**1** may have a fourth thickness T**4**. The third thickness T**3** of FIG. **6** may be the same as or different from the first thickness T**1** of the cell transistor structure CTS of FIG. **5**A, and for example, the third thickness T**3** may be greater than the first thickness T**1**. The fourth thickness T**4** of FIG. **6** may be the same as or different from the second thickness T**2** of FIG. **5**A, and for example, the fourth thickness T**4** may be greater than the second thickness T**2**.

[0127] The second peripheral transistors PTR**2** may have a cross-section which is the same as or similar to the cross-section of the first peripheral transistors PTR**1**. In some embodiments, the second peripheral transistors PTR**2** may have a fin field effect transistor (FinFET) structure.

[0128] FIG. **7**A illustrates an enlarged view showing section P**3** of FIG. **3**. FIG. **7**B illustrates an enlarged view inversely showing section P**4** of FIG. **7**A.

[0129] Referring to FIG. **7**A, on the first peripheral circuit section PE(**1**), some of the second peripheral wiring lines PI**2** positioned on the second peripheral transistor PTR**2** may be a signal wiring layer SIG. On the second peripheral circuit section PE(**2**) positioned below the second peripheral transistor PTR**2**, portions of the fourth cell wiring lines IT**4** may constitute a backside power delivery network layer PDN. An interval between the fourth cell wiring lines IT**4** on the backside power delivery network layer PDN may be greater than an interval between the second peripheral wiring lines PI**2** on the signal wiring layer SIG.

[0130] Referring to FIGS. **7**A and **7**B, the third peripheral transistors PTR**3** may be disposed on the second peripheral circuit section PE(**2**). The third peripheral transistors PTR**3** may have a structure which is the same as or similar to a structure of the first peripheral transistors PTR**1** of FIG. **6**. The third peripheral transistors PTR**3** may include peripheral active patterns PAP and peripheral gate

electrodes GE adjacent thereto. The peripheral active patterns PAP may include a pair of first and second peripheral active patterns PAP(**1**) and PAP(**2**) that are adjacent to each other. Each of the peripheral active patterns PAP may include a channel region CH and first and second impurity regions IM**1** and IM**2**. The first impurity regions IM**1** of the peripheral active patterns PAP may be in contact with the first cell wiring line IT**1**. The second impurity regions IM**2** of the peripheral active patterns PAP may be in contact with conductive patterns BP.

[0131] The third peripheral transistors PTR**3** may include a third left peripheral transistor PTR**3**(L) and a third right peripheral transistor PTR**3**(R). The third left peripheral transistor PTR**3**(L) and the third right peripheral transistor PTR**3**(R) may constitute a third pair transistor structure PTS**3**.

[0132] A material included in each of the first and second gate dielectric layers Gox**1** and Gox**2** of the third pair transistor structure PTS**3** of FIG. **7**B may be the same as or different from a material included in each of the first and second gate dielectric layers Gox**1** and Gox**2** of the cell transistor structure CTS of FIG. **5**A. The first gate dielectric layers Gox**1** of the third pair transistor structure PTS**3** may have a fifth thickness T**5**. The second gate dielectric layers Gox**2** of the third pair transistor structure PTS**3** may have a sixth thickness T**6**. The fifth thickness T**5** of FIG. **7**B may be the same as or different from the third thickness T**3** of FIG. **6** and the first thickness T**1** of FIG. **5**A, for example, the fifth thickness T**5** may be the same as the first thickness T**1**. The sixth thickness T**6** of FIG. **7**B may be the same as or different from the fourth thickness T**4** of FIG. **6** and the second thickness T**2** of FIG. **5**A, for example, the sixth thickness T**6** may be the same as the second thickness T**2**.

[0133] To distinguish the first and second gate dielectric layers Gox**1** and Gox**2** of FIG. **5**A from the first and second gate dielectric layers Gox**1** and Gox**2** of FIGS. **6** and **7**B, the first and second gate dielectric layers Gox**1** and Gox**2** of FIG. **5**A may be called first and second cell gate dielectric layers Gox**1**(C) and Gox**2**(C), and the first and second gate dielectric layers Gox**1** and Gox**2** of FIGS. **6** and **7**B may be called first and second peripheral gate dielectric layers Gox**1**(P) and Gox**2**(P).

[0134] Referring to FIG. **7**A, the second peripheral circuit section PE(**2**) may include the peripheral capacitor CAP**2** connected to one of the third peripheral transistors PTR**3**. The peripheral capacitor CAP**2** may be called a power capacitor. The peripheral capacitor CAP**2** may include an electrode pad EP, bottom electrodes BE, a dielectric layer DL, and a top electrode UE. The peripheral capacitor CAP**2** may also have an inverse structure. For example, the bottom electrodes BE may be positioned above the top electrode UE. The electrode pad EP may connect all of top surfaces of the bottom electrodes BE. The electrode pad EP and the bottom electrodes BE connected thereto may serve as a single electrode of the peripheral capacitor CAP**2**. With the electrode pad EP, sub-capacitors formed between the top electrode UE and each of the bottom electrodes BE may be connected with each other in parallel.

[0135] In a semiconductor device according to the present embodiment, as the peripheral transistors PTR**1** to PTR**3** have their VCT structure, the peripheral transistors PTR**1** to PTR**3** may decrease in horizontal size. Thus, the peripheral structure PS may have a reduced horizontal area. In addition, the VCT structure of the peripheral transistors PTR**1** to PTR**3** may facilitate wiring routing and may reduce a connection distance between the cell structure CS and the peripheral structure PS.

[0136] A planar transistor may require a semiconductor substrate, but a VCT structured peripheral transistor may not need a semiconductor substrate. Thus, the peripheral structure PS may have a reduced vertical size. Moreover, a through via penetrating a semiconductor substrate may not be included, and thus a semiconductor device may have a reduced horizontal size. Accordingly, a semiconductor device may become highly integrated.

[0137] In this description, the cell transistors CTR are illustrated to have their VCT structure, but the present inventive concepts are not limited thereto. The cell transistors CTR may have their buried channel array transistor (BCAT) structure.

[0138] FIG. **7**C illustrates an enlarged view showing section P**3** of FIG. **3** according to an embodiment of the present disclosure.
[0139] Referring to FIG. **7**C, the second peripheral circuit section PE(**2**) may not include but exclude the third peripheral transistors PTR**3**. One of the third cell contact plugs CT**3** may connect the electrode pad EP to one of the first cell wiring lines IT**1**. Other configurations may be identical or similar to those discussed above.
[0140] FIGS. **8**A to **8**J illustrate cross-sectional views showing a method of fabricating a semiconductor device of FIG. **3**.
[0141] Referring to FIG. **8**A, a first peripheral interlayer dielectric layer PL**1** may be formed on a first carrier substrate CB**1**. First peripheral wiring lines PI**1**, first and second peripheral transistors PTR**1** and PTR**2**, first peripheral contact plugs PC**1**, and a second peripheral interlayer dielectric layer PL**2** may be formed on the first peripheral interlayer dielectric layer PL**1**.
[0142] Referring to FIG. **8**B, second peripheral contact plugs PC**2**, second peripheral wiring lines PI**2**, and a third peripheral interlayer dielectric layer PL**3** may be formed on the second peripheral interlayer dielectric layer PL**2**. Third peripheral contact plugs PC**3**, third peripheral wiring lines PI**3**, and a fourth peripheral interlayer dielectric layer PL**4** may be formed on the third peripheral interlayer dielectric layer PL**3**.
[0143] Referring to FIG. **8**C, a second carrier substrate CB**2** may be bonded to the fourth peripheral interlayer dielectric layer PL**4**.
[0144] Referring to FIG. **8**D, the first carrier substrate CB**1** of FIG. **8**C may be removed to expose a bottom surface of the first peripheral interlayer dielectric layer PL**1**. A resultant structure may be turned upside down to allow the bottom surface of the first peripheral interlayer dielectric layer PL**1** to face upwards.
[0145] Referring to FIG. **8**E, fourth peripheral contact plugs PC**4** may be formed in the first peripheral interlayer dielectric layer PL**1**. A fifth peripheral interlayer dielectric layer PL**5** may be formed on the first peripheral interlayer dielectric layer PL**1**. Peripheral connection pads CP**1** may be formed in the fifth peripheral interlayer dielectric layer PL**5**. Thus, a peripheral structure PS may be manufactured on the second carrier substrate CB**2**.
[0146] Referring to FIG. **8**F, a first cell interlayer dielectric layer IL**1** may be formed on a third carrier substrate CB**3**. Bit lines BL, first cell wiring lines IT**1**, active patterns AP, cell transistors CTR, third peripheral transistors PTR**3**, and a second cell interlayer dielectric layer IL**2** may be formed on the first cell interlayer dielectric layer IL**1**.
[0147] Referring to FIG. **8**G, a third cell interlayer dielectric layer IL**3** may be formed on the second cell interlayer dielectric layer IL**2**. Storage node contacts BC and conductive patterns BP may be formed in the third cell interlayer dielectric layer IL**3**. A fourth cell interlayer dielectric layer IL**4**, landing pads LP, second cell wiring lines IT**2**, and an electrode pad EP may be formed on the third cell interlayer dielectric layer IL**3**. Cell capacitors CAP**1** and a peripheral capacitor CAP**2** may be formed on the fourth cell interlayer dielectric layer IL**4**. A fifth cell interlayer dielectric layer IL**5** may be formed to cover the cell capacitors CAP**1** and the peripheral capacitor CAP**2**. First cell contact plugs CT**1** may be formed to penetrate the fifth cell interlayer dielectric layer IL**5**. Second cell contact plugs CT**2**, third cell wiring lines IT**3**, and a sixth cell interlayer dielectric layer IL**6** may be formed on the fifth cell interlayer dielectric layer IL**5**.
[0148] Referring to FIG. **8**H, a fourth carrier substrate CB**4** may be bonded to the sixth cell interlayer dielectric layer IL**6** in a state depicted in FIG. **8**G. A resultant structure may be turned upside down to allow the third carrier substrate CB**3** to face upwards.
[0149] Referring to FIG. **8**I, the third carrier substrate CB**3** of FIG. **8**H may be removed to expose a top surface of the first cell interlayer dielectric layer IL**1**. Bit-line contact plugs BLC, word-line contact plugs WLC, and back gate contact plugs BGC may be formed to penetrate the first cell interlayer dielectric layer IL**1**. Fourth cell wiring lines IT**4**, a seventh cell interlayer dielectric layer IL**7**, and cell connection pads CP**2** may be formed on the first cell interlayer dielectric layer IL**1**.

Thus, a cell structure CS may be manufactured on the fourth carrier substrate CB**4**.
[0150] Referring to FIG. **8**J, the peripheral structure PS of FIG. **8**E may be flipped and placed on the cell structure CS of FIG. **8**I. A thermocompression process may be performed to bond the peripheral structure PS to the cell structure CS. For simplification of drawings, the first to fifth peripheral interlayer dielectric layers PL**1** to PL**5** of FIG. **8**E may be integrated and represented as a peripheral interlayer dielectric layer PL in FIG. **8**J. Likewise, for simplification of drawings, the first to seventh cell interlayer dielectric layers IL**1** to IL**7** of FIG. **8**I may be integrated and represented as a cell interlayer dielectric layer IL in FIG. **8**J.
[0151] Referring to FIG. **3**, after the bonding of the peripheral structure PS to the cell structure CS, the second carrier substrate CB**2** of FIG. **8**J may be removed. The fourth carrier substrate CB**4** of FIG. **8**J may become a substrate **100** of FIG. **3**. A semiconductor device may thus be fabricated as shown in FIG. **3**.
[0152] FIGS. **9** and **10** illustrate cross-sectional views showing a semiconductor device according to some embodiments of the present inventive concepts.
[0153] A semiconductor device of FIG. **9** may include a peripheral structure PS and a cell structure CS that are sequentially stacked on a substrate **100**. The peripheral structure PS and the cell structure CS of FIG. **9** may have configurations obtained by flipping those of the peripheral structure PS and the cell structures CS of FIG. **3** on the substrate **100**. Other configurations may be identical to those of FIG. **3**. The semiconductor device of FIG. **9** may be fabricated by employing a thermocompression process to bond the peripheral structure PS and the cell structure CS with each other as shown in FIG. **8**J, removing the fourth carrier substrate CB**4**, and then flipping a resultant structure. The second carrier substrate CB**2** of FIG. **8**J may become a substrate **100** of FIG. **3**.
[0154] A semiconductor device of FIG. **10** may not include a substrate **100**, and may include a cell structure CS and a peripheral structure PS that are sequentially stacked. Other configurations may be identical to those of FIG. **3**. The semiconductor device of FIG. **10** may be fabricated by employing a thermocompression process to bond the peripheral structure PS and the cell structure CS with each other as shown in FIG. **8**J, and then removing both of the second carrier substrate CB**2** and the fourth carrier substrate CB**4**.
[0155] FIG. **11** illustrates a cross-sectional view taken along line A-A′ of FIG. **2** according to an embodiment of the present disclosure.
[0156] Referring to FIG. **11**, a semiconductor device according to the present embodiment may not include but exclude the peripheral connection pads CP**1** and the cell connection pads CP**2** of FIG. **3**. The cell interlayer dielectric layer IL may have a top surface in direct contact with a bottom surface of a peripheral interlayer dielectric layer PL. The first peripheral contact plug PC**1** may penetrate portions of the cell interlayer dielectric layer IL and the peripheral interlayer dielectric layer PL to connect the second peripheral wiring line PI**2** to the fourth cell wiring line IT**4**. Other configurations may be identical or similar to those discussed with reference to FIGS. **3** to **7**B.
[0157] FIGS. **12**A to **12**E illustrate cross-sectional views showing a method of fabricating the semiconductor device of FIG. **11** according to an embodiment of the present disclosure.
[0158] Referring to FIG. **12**A, the third carrier substrate CB**3** of FIG. **8**H may be removed to expose the first cell interlayer dielectric layer IL**1**. A bit-line contact plug BLC, a back gate contact plug BGC, and a word-line contact plug WLC may be formed in the first cell interlayer dielectric layer IL**1**. A seventh cell interlayer dielectric layer IL**7**, a fourth cell wiring line IT**4**, and third cell contact plugs CT**3** may be formed on the first cell interlayer dielectric layer IL**1**. An eighth cell interlayer dielectric layer IL**8** may be formed on the seventh cell interlayer dielectric layer IL**7**. Thus, a cell structure CS may be manufactured on the fourth carrier substrate CB**4**.
[0159] Referring to FIG. **12**B, a first peripheral interlayer dielectric layer PL**1** may be formed on the first carrier substrate CB**1**. A second peripheral interlayer dielectric layer PL**2**, peripheral active patterns PAP, first peripheral wiring lines PI**1**, and first and second peripheral transistors PTR**1** and PTR**2** may be formed on the first peripheral interlayer dielectric layer PL**1**. A third peripheral

interlayer dielectric layer PL**3** may be formed on the second peripheral interlayer dielectric layer PL**2**.
[0160] Referring to FIGS. **12**C and **12**D, a structure of FIG. **12**B may be flipped and placed on the cell structure CS of FIG. **12**A. Thus, the third peripheral interlayer dielectric layer PL**3** may be in contact with the eighth cell interlayer dielectric layer IL**8** of the cell structure CS. A thermocompression process may be performed to bond the third peripheral interlayer dielectric layer PL**3** to the eighth cell interlayer dielectric layer IL**8**.
[0161] Referring to FIG. **12**E, the first carrier substrate CB**1** and the first peripheral interlayer dielectric layer PL**1** on the second peripheral interlayer dielectric layer PL**2** may be removed to expose the peripheral active patterns PAP. First peripheral contact plugs PC**1** may be formed to penetrate the second peripheral interlayer dielectric layer PL**2**, the third peripheral interlayer dielectric layer PL**3**, and the eighth cell interlayer dielectric layer IL**8**, thereby being in contact with the fourth cell wiring lines IT**4**.
[0162] Referring to FIG. **11**, second peripheral wiring lines PI**2**, the second peripheral contact plugs PC**2**, third peripheral wiring lines PI**3**, third peripheral contact plugs PC**3**, and additional peripheral interlayer dielectric layers may be formed on the second peripheral interlayer dielectric layer PL**2**. A semiconductor device may thus be fabricated as shown in FIG. **11**. For simplification of drawings, the first to third peripheral interlayer dielectric layers PL**1** to PL**3** of FIG. **12**E may be integrated and represented as a peripheral interlayer dielectric layer PL in FIG. **11**. Likewise, for simplification of drawings, the first to eighth cell interlayer dielectric layers IL**1** to IL**8** of FIG. **12**E may be integrated and represented as a cell interlayer dielectric layer IL in FIG. **11**.
[0163] The following description will focus on various configurations of a pair of transistor structures including peripheral transistors according to the present inventive concepts. A pair of transistor structures PTS according to the present inventive concepts may be used as a basic unit to constitute various circuits.
[0164] FIG. **13**A illustrates a cross-sectional view showing a semiconductor device according to some embodiments of the present inventive concepts. FIGS. **13**B to **13**D illustrate circuit diagrams showing a semiconductor device that has a structure of FIG. **13**A.
[0165] Referring to FIG. **13**A, a pair of N-type transistor structure PTS(N) (i.e., the N-type pair transistor structure PTS(N)) and a pair of P-type transistor structure PTS(P) (i.e., P-type pair transistor structure PTS(P)) may be disposed on a lower structure **200**. The lower structure **200** may be a semiconductor substrate, a dielectric substrate, a conductive layer, or a dielectric layer. The N-type pair transistor structure PTS(N) and the P-type pair transistor structure PTS(P) may each include a pair of left and right peripheral transistors PTR(L) and PTR(R) that are adjacent to each other. Each of the left peripheral transistor PTR(L) and the right peripheral transistor PTR(R) may include a peripheral active pattern PAP and a peripheral gate electrode GE. The peripheral active pattern PAP may include a channel region CH and first and second impurity regions IM**1** and IM**2**.
[0166] In this description, the first impurity region IM**1** may correspond to a drain or a source of one of the left peripheral transistor PTR(L) and the right peripheral transistor PTR(R), and may be called a first terminal. The second impurity region IM**2** may correspond to a source or a drain of one of the left peripheral transistor PTR(L) and the right peripheral transistor PTR(R), and may be called a second terminal.
[0167] N-type impurities may be doped in the first and second impurity regions IM**1** and IM**2** included in the N-type pair transistor structure PTS(N). No impurities or P-type impurities may be doped in the channel region CH included in the N-type pair transistor structure PTS(N). P-type impurities may be doped in the first and second impurity regions IM**1** and IM**2** included in the P-type pair transistor structure PTS(P). No impurities or N-type impurities may be doped in the channel region CH included in the P-type pair transistor structure PTS(P).
[0168] First and second peripheral gate electrodes GE(**1**) and GE(**2**) of each of the N-type pair transistor structure PTS(N) and the P-type pair transistor structure PTS(P) may include metal, such

as tungsten, aluminum, and copper. The first and second peripheral gate electrodes GE(**1**) and GE(**2**) of each of the N-type pair transistor structure PTS(N) and the P-type pair transistor structure PTS(P) may further include a work-function pattern suitable to each characteristics. In some embodiments, the work-function pattern may be included to control a threshold voltage of a transistor.

[0169] The first and second peripheral gate electrodes GE(**1**) and GE(**2**) included in the N-type pair transistor structure PTS(N) may include or may be formed of the same material and structure as those of the first and second peripheral gate electrodes GE(**1**) and GE(**2**) included in the P-type pair transistor structure PTS(P). In some embodiments, the first and second peripheral gate electrodes GE(**1**) and GE(**2**) included in the N-type pair transistor structure PTS(N) may include or may include different material and structure from those of the first and second peripheral gate electrodes GE(**1**) and GE(**2**) included in the P-type pair transistor structure PTS(P).

[0170] A conductive pattern BP may be disposed on the second impurity region IM**2** of the peripheral active pattern PAP. The conductive pattern BP may include or may be formed of metal. In some embodiments, the conductive pattern BP may be formed of impurity-doped silicon, SiGe, or SiC. Impurities doped in the conductive pattern BP may have the same conductivity type as that of impurities doped in the second impurity region IM**2** adjacent to the conductive pattern BP.

[0171] A source/drain connection line SDL**1** may be disposed underneath the first impurity regions IM**1** of the peripheral active patterns PAP that are adjacent to each other, and may connect the first impurity regions IM**1** connected with each other. Each of the N-type pair transistor structure PTS(N) and the P-type pair transistor structure PTS(P) may further include a peripheral back gate electrode BG interposed between the peripheral active patterns PAP that are adjacent to each other.

[0172] Referring to FIGS. **13**A and **13**B, the N-type pair transistor structure PTS(N) may have a structure including two neighboring N-type metal oxide semiconductor (NMOS) transistors which have a VCT structure and share one back gate electrode. The P-type pair transistor structure PTS(P) may have a structure including two neighboring P-type metal oxide semiconductor (PMOS) transistors which have a VCT structure and share one back gate electrode. A semiconductor device of FIG. **13**A may have a complementary metal oxide semiconductor (CMOS) transistor structure.

[0173] Referring to FIGS. **13**A and **13**C, the first and the second peripheral gate electrodes GE(**1**) and GE(**2**) and the peripheral back gate electrode BG of the N-type pair transistor structure PTS(N) may be connected to each other and provided with the same first input voltage Vin**1**. The first and the second peripheral gate electrodes GE(**1**) and GE(**2**) and the peripheral back gate electrode BG of the P-type pair transistor structure PTS(P) may be connected to each other and provided with the same second input voltage Vin**2**. In this case, each of the N-type pair transistor structure PTS(N) and the P-type pair transistor structure PTS(P) may have a double gate structure or a gate-all-around structure.

[0174] Referring to FIGS. **13**A and **13**D, the first and the second peripheral gate electrodes GE(**1**) and GE(**2**) and the peripheral back gate electrode BG of the N-type pair transistor structure PTS(N) may be provided with input voltages Vin**1**, Vin**2**, and Vin**3** that are different from each other. The first and the second peripheral gate electrodes GE(**1**) and GE(**2**) and the peripheral back gate electrode BG of the P-type pair transistor structure PTS(P) may be provided with input voltages Vin**4**, Vin**5**, and Vin**6** that are different from each other. In this case, each of the N-type pair transistor structure PTS(N) and the P-type pair transistor structure PTS(P) may have an independent double gate structure.

[0175] FIGS. **14**A to **14**D illustrate cross-sectional views showing a semiconductor device according to some embodiments of the present inventive concepts.

[0176] Referring to FIG. **14**A, in the structure of FIG. **13**A, the conductive pattern BP may be connected to each of the second impurity regions IM**2** of the peripheral active patterns PAP that are adjacent to each other. Other configurations and circuitry may be identical or similar to those discussed with reference to FIGS. **13**A to **13**D.

[0177] Referring to FIG. **14**B, in the structure of FIG. **13**A, the peripheral back gate electrode BG and the second gate dielectric layer Gox**2** may be omitted.
[0178] Referring to FIG. **14**C, a first pair transistor structure PTS(n**1**) and a second pair transistor structure PTS(n**2**) may be disposed on the lower structure **200**. Each of the first pair transistor structure PTS(n**1**) and the second pair transistor structure PTS(n**2**) may include a pair of left and right peripheral transistors PTR(L) and PTR(R) that are adjacent to each other. Each of the left peripheral transistor PTR(L) and the right peripheral transistor PTR(R) may include a peripheral active pattern PAP and a peripheral gate electrode GE. The peripheral active pattern PAP may include a channel region CH and first and second impurity regions IM**1** and IM**2**.
[0179] First impurities having a first conductivity type may be doped in the first and second impurity regions IM**1** and IM**2** of each of the first pair transistor structure PTS(n**1**) and the second pair transistor structure PTS(n**2**). The first conductivity type may be N-type or P-type. The first and second impurity regions IM**1** and IM**2** of the first pair transistor structure PTS(n**1**) may be doped with the first impurities at a first concentration. The first and second impurity regions IM**1** and IM**2** of the second pair transistor structure PTS(n**2**) may be doped with the first impurities at a second concentration. The second concentration may be greater than the first concentration.
[0180] Referring to FIG. **14**D, a first pair transistor structure PTS**1** and a second pair transistor structure PTS**2** may be disposed on the lower structure **200**. The peripheral transistors PTR included in the first pair transistor structure PTS**1** may have a first gate length GL**1**. The peripheral transistors PTR included in the second pair transistor structure PTS**2** may have a second gate length GL**2**. The second gate length GL**2** may be different from the first gate length GL**1**, and for example, the second gate length GL**2** may be greater than the first gate length GL**1**. In this description, the term “gate length” may be defined to refer to a vertical length of a portion where the peripheral gate electrode GE and the channel region CH overlap each other horizontally.
[0181] FIGS. **15**A to **15**E illustrate cross-sectional views showing a semiconductor device according to some embodiments of the present inventive concepts.
[0182] Referring to FIG. **15**A, in a pair transistor structure PTS according to the present embodiment, the first and second peripheral gate electrodes GE(**1**) and GE(**2**) and the peripheral back gate electrodes BG may have a vertical length less than a vertical length of the channel region CH. Thus, the first and second impurity regions IM**1** and IM**2** may not horizontally overlap the peripheral back gate electrode BG and the first and second peripheral gate electrodes GE(**1**) and GE(**2**).
[0183] Referring to FIG. **15**B, in a pair transistor structure PTS according to the present embodiment, the first and second peripheral gate electrodes GE(**1**) and GE(**2**) and the peripheral back gate electrodes BG may have a vertical length greater than a vertical length of the channel region CH. Thus, the first and second peripheral gate electrodes GE(**1**) and GE(**2**) and the peripheral back gate electrodes BG may horizontally overlap the first and second impurity regions IM**1** and IM**2**.
[0184] Referring to FIG. **15**C, in a pair transistor structure PTS according to the present embodiment, the third thickness T**3** of the first gate dielectric layer Gox**1** may be less than the fourth thickness T**4** of the second gate dielectric layer Gox**2**.
[0185] Referring to FIG. **15**D, in a pair transistor structure PTS according to the present embodiment, the third thickness T**3** of the first gate dielectric layer Gox**1** may be greater than the fourth thickness T**4** of the second gate dielectric layer Gox**2**.
[0186] Referring to FIG. **15**E, in a pair transistor structure PTS according to the present embodiment, the first gate dielectric layer Gox**1** may be formed of a double layer including a silicon oxide layer SO and a high-k dielectric layer HK. The high-k dielectric layer HK may include a material, such as metal oxide, whose a dielectric constant is greater than a dielectric constant of the silicon oxide layer SO. The high-k dielectric layer HK may be interposed between the silicon oxide layer SO and the peripheral gate electrode GE. Other configurations may be

identical or similar to those discussed above with reference to FIG. **15**D.
[0187] In some embodiments, the first gate dielectric layer Gox**1** may be formed of a single layer including the silicon oxide layer SO, and the second gate dielectric layer Gox**2** may be formed of a double layer including the silicon oxide layer SO and the high-k dielectric layer HK.
[0188] Based on connection structures or operations of circuit, the peripheral back gate electrode BG may become a gate electrode, and each of the first and second peripheral gate electrodes GE(**1**) and GE(**2**) may become a back gate electrode. According to an embodiment, the first peripheral gate electrode GE(**1**), the peripheral back gate electrode BG, and the second peripheral gate electrode GE(**2**) may be called a first gate electrode, a second gate electrode, and a third gate electrode, respectively, according to the described order.
[0189] FIG. **16**A illustrates a cross-sectional view showing a semiconductor device according to some embodiments of the present inventive concepts. FIG. **16**B illustrates a circuit diagram showing a semiconductor device of FIG. **16**A.
[0190] Referring to FIGS. **16**A and **16**B, an N-type pair transistor structure PTS(N) and a P-type pair transistor structure PTS(P) may be disposed on a lower structure **200**. The N-type pair transistor structure PTS(N) and the P-type pair transistor structure PTS(P) may each include a pair of left and right peripheral transistors PTR(L) and PTR(R) that are adjacent to each other. Each of the left peripheral transistor PTR(L) and the right peripheral transistor PTR(R) may include a peripheral active pattern PAP. A peripheral gate electrode GE may be interposed between first and second peripheral active patterns PAP(**1**) and PAP(**2**) that are adjacent to each other. A first peripheral back gate electrode BG**1** may be disposed on a left side of the first peripheral active pattern PAP(**1**). A second peripheral back gate electrode BG**2** may be disposed on a right side of the second peripheral active pattern PAP(**2**). The left peripheral transistor PTR(L) and the right peripheral transistor PTR(R) may share the peripheral gate electrode GE. A threshold voltage of the left peripheral transistor PTR(L) may be adjusted by the first peripheral back gate electrode BG**1**. A threshold voltage of the right peripheral transistor PTR(R) may be adjusted by the second peripheral back gate electrode BG**2**.
[0191] N-type impurities may be doped in the first and second impurity regions IM**1** and IM**2** included in the N-type pair transistor structure PTS(N). No impurities or P-type impurities may be doped in the channel region CH included in the N-type pair transistor structure PTS(N). P-type impurities may be doped in the first and second impurity regions IM**1** and IM**2** included in the P-type pair transistor structure PTS(P). No impurities or N-type impurities may be doped in the channel region CH included in the P-type pair transistor structure PTS(P).
[0192] The N-type pair transistor structure PTS(N) may have a structure including two neighboring N-type metal oxide semiconductor (NMOS) transistors which have a VCT structure and share one peripheral gate electrode GE. The P-type pair transistor structure PTS(P) may have a structure including two neighboring P-type metal oxide semiconductor (PMOS) transistors which have a VCT structure and share one peripheral gate electrode GE.
[0193] FIG. **17**A illustrates a cross-sectional view showing a semiconductor device according to some embodiments of the present inventive concepts. FIGS. **17**B and **17**C illustrate circuit diagrams showing a semiconductor device of FIG. **17**A.
[0194] Referring to FIGS. **17**A and **17**B, a pair transistor structure PTS according to the present embodiment may include a pair of left and right peripheral transistors PTR(L) and PTR(R) that are adjacent to each other. N-type impurities may be doped in a conductive pattern BP and first and second impurity regions IM**1**(*n*) and IM**2**(*n*) of the left peripheral transistor PTR(L). P-type impurities may be doped in a conductive pattern BP and first and second impurity regions IM**1**(*p*) and IM**2**(*p*) of the right peripheral transistor PTR(R). The left peripheral transistor PTR(L) may be a VCT structured NMOS transistor. The right peripheral transistor PTR(R) may be a VCT structured PMOS transistor. The left peripheral transistor PTR(L) and the right peripheral transistor PTR(R) may share one peripheral back gate electrode BG. The pair transistor structure PTS may

have a CMOS transistor structure that shares a back gate electrode.
[0195] In FIG. **17**C, the peripheral back gate electrode BG may be electrically grounded. In this case, a CMOS transistor structure may include a PMOS transistor and an NMOS transistor whose threshold voltages are low.
[0196] FIG. **18**A illustrates a cross-sectional view showing a semiconductor device according to some embodiments of the present inventive concepts. FIGS. **18**B and **18**C illustrate circuit diagrams showing a semiconductor device of FIG. **18**A.
[0197] Referring to FIGS. **18**A and **18**B, a pair transistor structure PTS according to the present embodiment may include a pair of left and right peripheral transistors PTR(L) and PTR(R) that are adjacent to each other. N-type impurities may be doped in a conductive pattern BP and first and second impurity regions IM**1**(*n*) and IM**2**(*n*) of the left peripheral transistor PTR(L). P-type impurities may be doped in a conductive pattern BP and first and second impurity regions IM**1**(*p*) and IM**2**(*p*) of the right peripheral transistor PTR(R). The left peripheral transistor PTR(L) may be a VCT structured NMOS transistor. The right peripheral transistor PTR(R) may be a VCT structured PMOS transistor. The pair transistor structure PTS may have a CMOS transistor structure that shares a peripheral gate electrode GE.
[0198] Each of the left peripheral transistor PTR(L) and the right peripheral transistor PTR(R) may include a peripheral active pattern PAP. The peripheral gate electrode GE may be interposed between the first and second peripheral active patterns PAP(**1**) and PAP(**2**) that are adjacent to each other. A first peripheral back gate electrode BG**1** may be disposed on a left side of the first peripheral active pattern PAP(**1**). A second peripheral back gate electrode BG**2** may be disposed on a right side of the second peripheral active pattern PAP(**2**). The left peripheral transistor PTR(L) and the right peripheral transistor PTR(R) may share the peripheral gate electrode GE. A threshold voltage of the left peripheral transistor PTR(L) may be adjusted by the first peripheral back gate electrode BG**1**. A threshold voltage of the right peripheral transistor PTR(R) may be adjusted by the second peripheral back gate electrode BG**2**.
[0199] Referring to FIGS. **18**A and **18**C, an input voltage Vin may be applied to the peripheral gate electrode GE. The second impurity region IM**2** of the left peripheral transistor PTR(L) may be electrically grounded. A power voltage Vdd may be applied to the second impurity region IM**2** of the right peripheral transistor PTR(R). A first back gate voltage Vbgn may be applied to the first peripheral back gate electrode BG**1**, and a second back gate voltage Vbgp may be applied to the second peripheral back gate electrode BG**2**. The first impurity regions IM**1** of the left peripheral transistor PTR(L) and the right peripheral transistor PTR(R) may be connected through a first source/drain connection line SDL**1**, and through this configuration, an output voltage Vout may be readout. A semiconductor device of FIG. **18**A having a circuit of FIG. **18**C may correspond to an inverter that shares a gate electrode. For example, when the input voltage Vin has a high level, the output voltage Vout has a low level. In a case where the input voltage Vin has a low level, the output voltage Vout has a high level.
[0200] FIG. **19**A illustrates a plan view showing a semiconductor device according to some embodiments of the present inventive concepts. FIG. **19**B illustrates a cross-sectional view taken along line B-B′ of FIG. **19**A.
[0201] Referring to FIGS. **19**A and **19**B, a semiconductor device according to the present embodiment may correspond to an example of a standard cell STC of a logic circuit. A first peripheral wiring line PI**1** may be disposed on the lower structure **200**. The first peripheral wiring line PI**1** may be provided thereon with a first source/drain connection line SDL**1** and a second source/drain connection line SDL**2** that are spaced apart from each other in a second direction D**2**. An N-type pair transistor structure PTS(N) may be disposed on the first source/drain connection line SDL**1**. A P-type pair transistor structure PTS(P) may be disposed on the second source/drain connection line SDL**2**. A first peripheral gate electrode GE(**1**) of the N-type pair transistor structure PTS(N) may extend in the second direction D**2** to serve as a first peripheral gate electrode GE(**1**) of

the P-type pair transistor structure PTS(P). A second peripheral gate electrode GE(**2**) of the N-type pair transistor structure PTS(N) may extend in the second direction D**2** to serve as a second peripheral gate electrode GE(**2**) of the P-type pair transistor structure PTS(P). A peripheral back gate electrode BG of the N-type pair transistor structure PTS(N) may extend in the second direction D**2** to become a peripheral back gate electrode BG of the P-type pair transistor structure PTS(P). A second peripheral wiring line PI**2** may be disposed on the N-type pair transistor structure PTS(N). A third peripheral wiring line PI**3** may be disposed on the P-type pair transistor structure PTS(P).
[0202] A ground voltage GND may be applied to the second peripheral wiring line PI**2**. A power voltage Vdd may be applied to the third peripheral wiring line PI**3**. An input voltage Vin may be applied to the first peripheral gate electrode GE(**1**) and the second peripheral gate electrode GE(**2**). The output voltage Vout may be readout through the first peripheral wiring line PI**1**.
[0203] FIG. **20** illustrates a circuit diagram showing a logic transistor according to some embodiments of the present inventive concepts.
[0204] Referring to FIG. **20**, a logic transistor LTR according to the present embodiment may include pair transistor structures PTS arranged in M rows and N columns that are connected with each other and two-dimensionally arranged along a first direction D**1** and a second direction D**2**. The M and N may each be a natural number of equal to or greater than 2. Each of the pair transistor structures PTS may include a pair of left and right peripheral transistors PTR(L) and PTR(R) that are adjacent to each other as discussed with reference to FIGS. **13**A to **18**C. Each of the left peripheral transistor PTR(L) and the right peripheral transistor PTR(R) may be called a unit transistor.
[0205] A first source/drain connection line SDL**1** may connect first impurity regions IM**1** of each of the pair transistor structures PTS with each other. A second source/drain connection line SDL**2** may connect second impurity regions IM**2** of each of the pair transistor structures PTS with each other. A gate connection line GCL may connect peripheral gate electrodes GE of each of the pair transistor structures PTS with each other.
[0206] An output value of the logic transistor LTR according to the present inventive concepts may be the same as a sum of output values of the unit transistors. As the logic transistor LTR is formed of a plurality of unit transistors each having a VCT structure.
[0207] FIG. **21**A illustrates a plan view showing a logic transistor according to some embodiments of the present inventive concepts. FIG. **21**B illustrates a cross-sectional view taken along line C-C′ of FIG. **21**A.
[0208] Referring to FIGS. **21**A and **21**B, a logic transistor LTR according to the present embodiment may have a circuit discussed with reference to FIG. **20**. The logic transistor LTR may include a plurality of pair transistor structures PTS on the lower structure **200** that are two-dimensionally arranged along a first direction D**1** and a second direction D**2**. The first source/drain connection lines SDL**1** that connect the first impurity regions IM**1** of the pair transistor structures PTS with each other may have a linear shape that extends along the first direction D**1** and may be spaced apart from each other in the second direction D**2**. On each of the pair transistor structures PTS, first peripheral gate electrodes GE(**1**), peripheral back gate electrodes BG, and second peripheral gate electrodes GE(**2**) may each have a linear shape that extends along the second direction D**2** and may be spaced apart from each other in the first direction D**1**. Peripheral active patterns PAP may have island shapes that are two-dimensionally arranged along the first and second directions D**1** and D**2** and are spaced apart from each other. Conductive patterns BP may correspondingly overlap the peripheral active patterns PAP. The conductive patterns BP may have island shapes that are two-dimensionally arranged along the first and second directions D**1** and D**2** and are spaced apart from each other. The second source/drain connection lines SDL**2** may connect the conductive patterns BP with each other. Other configurations may be identical or similar to those discussed above.
[0209] FIG. **22**A illustrates a plan view showing a logic transistor according to some embodiments

of the present inventive concepts. FIG. **22**B illustrates a cross-sectional view taken along line C-C′ of FIG. **22**A.
[0210] Referring to FIGS. **22**A and **22**B, in a logic transistor LTR according to the present embodiment, the conductive patterns BP may have linear shapes that extend along the first direction D**1** and may be spaced apart from each other in the second direction D**2**. Other configurations may be identical or similar to those discussed with reference to FIGS. **21**A and **21**B.
[0211] FIG. **23** illustrates a plan view showing a logic transistor according to some embodiments of the present inventive concepts. A cross-section obtained by cutting FIG. **23** along line C-C′ may correspond to FIG. **21**B.
[0212] Referring to FIG. **23**, the first source/drain connection lines SDL**1** may be connected with each other to have a plate shape. Other configurations may be identical or similar to those discussed with reference to FIGS. **21**A and **21**B.
[0213] FIG. **24**A illustrates a plan view showing a logic transistor according to some embodiments of the present inventive concepts. FIG. **24**B illustrates a cross-sectional view taken along line C-C′ of FIG. **24**A.
[0214] Referring to FIGS. **24**A and **24**B, one conductive pattern BP may overlap four neighboring peripheral active patterns PAP. The conductive pattern BP may be provided in plural, and the plurality of conductive patterns BP may have island shapes that are two-dimensionally arranged in the first and second directions D**1** and D**2** and are spaced apart from each other. Other configurations may be identical or similar to those discussed with reference to FIGS. **21**A and **21**B.
[0215] FIG. **25** illustrates a plan view showing a logic transistor according to some embodiments of the present inventive concepts. A cross-section obtained by cutting FIG. **25** along line C-C′ may correspond to FIG. **21**B.
[0216] Referring to FIG. **25**, the conductive patterns BP of FIG. **23** may extend in the second direction D**2** to be connected with each other, thereby having a linear shape extending in the second direction D**2**. The conductive patterns BP may be spaced apart from each other in the first direction D**1**. Other configurations may be identical or similar to those discussed with reference to FIGS. **21**A and **21**B.
[0217] FIG. **26**A illustrates a plan view showing a logic transistor according to some embodiments of the present inventive concepts. FIG. **26**B illustrates a cross-sectional view taken along line C-C′ of FIG. **26**A.
[0218] Referring to FIGS. **26**A and **26**B, the first source/drain connection lines SDL**1** may have a linear shape that extends in the second direction D**2** and may be spaced apart from each other in the first direction D**1**. Other configurations may be identical or similar to those discussed with reference to FIGS. **21**A and **21**B.
[0219] The logic transistor LTR of FIGS. **20** to **26**B may correspond to at least one of the first to third peripheral transistors PTR**1** to PTR**3** discussed with reference to FIGS. **2** to **11**.
[0220] A semiconductor device according to the present inventive concepts may include a cell structure and a peripheral structure that are stacked, and peripheral transistors included in the cell structure and/or the peripheral structure may have a vertical channel transistor (VCT) structure. In addition, a logic transistor may be formed of VCT structured unit transistors. It may thus be possible to reduce a horizontal area of the peripheral structure, to decrease a connection distance between the cell structure and the peripheral structure, and to facilitate wiring routing. Moreover, no through via may be included, and thus the semiconductor device may have a reduced horizontal size. Accordingly, the semiconductor device may become highly integrated.
[0221] Although the present invention has been described in connection with some embodiments of the present inventive concepts illustrated in the accompanying drawings, it will be understood to those skilled in the art that various changes and modifications may be made without departing from the technical spirit and essential feature of the present inventive concepts. It will be apparent to those skilled in the art that various substitution, modifications, and changes may be thereto without

departing from the scope and spirit of the present inventive concepts. The embodiments of FIG. **1**A to **26**B may be combined with each other.

Claims

1. A semiconductor device comprising: a cell structure; and a peripheral structure disposed on the cell structure, wherein the cell structure includes a first memory block and a second memory block that are side by side in a first horizontal direction, wherein the peripheral structure includes: a first core circuit section on the first memory block; and a second core circuit section on the second memory block, wherein each of the first and second memory blocks includes a plurality of cell transistors, wherein each of the plurality of first and second core circuit sections includes a plurality of first peripheral transistors, wherein each of the first peripheral transistors includes: a first peripheral active pattern extending in a second horizontal direction perpendicular to the first horizontal direction; a first peripheral gate electrode adjacent to one sidewall of the first peripheral active pattern; and a first peripheral impurity region and a second peripheral impurity region on a lower portion and an upper portion of the first peripheral active pattern, respectively, and wherein, in each of the plurality of first peripheral transistors, the first and second peripheral impurity regions are spaced apart from each other in a third direction perpendicular to the first and second horizontal directions.

2. The semiconductor device of claim 1, wherein the peripheral structure further includes a first peripheral circuit section between the first core circuit section and the second core circuit section, wherein the first peripheral circuit section includes a plurality of second peripheral transistors, and wherein each of the second peripheral transistors includes: a second peripheral active pattern extending in the second horizontal direction; and a second peripheral gate electrode adjacent to one sidewall of the second peripheral active pattern.

3. The semiconductor device of claim 2, wherein the cell structure further includes a second peripheral circuit section between the first memory block and the second memory block, wherein the second peripheral circuit section includes a plurality of third peripheral transistors, and wherein each of the third peripheral transistors includes: a third peripheral active pattern extending in the second horizontal direction; and a third peripheral gate electrode adjacent to one sidewall of the third peripheral active pattern.

4. The semiconductor device of claim 3, wherein each of the first and second memory blocks further includes a plurality of cell capacitors that are connected to the plurality of cell transistors, respectively, wherein the second peripheral circuit section further includes a peripheral capacitor connected to one of the third peripheral transistors, and wherein the peripheral capacitor includes: a plurality of bottom electrodes, an electrode pad that connects the bottom electrodes with each other, a dielectric layer covering the electrode pad and each of the plurality of bottom electrodes, and a top electrode on the dielectric layer.

5. The semiconductor device of claim 3, wherein the second peripheral circuit section further includes a backside power delivery network layer.

6. The semiconductor device of claim 1, wherein each of the cell transistors includes: a cell active pattern extending in the second horizontal direction; a word line adjacent to a lateral surface of the cell active pattern; and a first cell impurity region and a second cell impurity region on a lower portion and an upper portion of the cell active pattern, respectively, wherein, in each of the cell transistors, the first and second cell impurity regions are spaced apart from each other in the third direction perpendicular to the first and second horizontal directions, and wherein a conductivity type of impurities doped in the first and second cell impurity regions is different from a conductivity type of impurities doped in the first and second peripheral impurity regions.

7. The semiconductor device of claim 1, wherein each of the cell transistors includes: a cell active pattern extending in the second horizontal direction; a word line adjacent to a lateral surface of the

cell active pattern; and a first cell impurity region and a second cell impurity region on a lower portion and an upper portion of the cell active pattern, respectively, wherein, in each of the cell transistors, the first and second cell impurity regions are spaced apart from each other in the third direction perpendicular to the first and second horizontal directions, wherein first impurities are doped in the first and second cell impurity regions and the first and second peripheral impurity regions, and wherein a concentration of the first impurities doped in the first and second cell impurity regions is less than a concentration of the first impurities doped in the first and second peripheral impurity regions.

8. The semiconductor device of claim 1, wherein at least one of the first and second core circuit sections further includes: a first wiring line that connects first peripheral impurity regions of some of the plurality of first peripheral transistors with each other; a second wiring line that connects second peripheral impurity regions of the some of the plurality of first peripheral transistors with each other; and a third wiring line that connects first peripheral gate electrodes of the some of the first peripheral transistors with each other.

9. The semiconductor device of claim 8, wherein at least one of the first and second core circuit sections further includes: a plurality of first conductive patterns between the first wiring line and the first peripheral impurity regions of the some of the first peripheral transistors; and a plurality of second conductive patterns between the second wiring line and the second peripheral impurity regions of the some of the first peripheral transistors, and wherein, when viewed in a plan view, each of the first and second conductive patterns has an island shape, a linear shape, or a plate shape.

10. The semiconductor device of claim 1, wherein a pair of neighboring ones of the first peripheral transistors constitute a pair transistor structure, wherein the pair transistor structure includes a left peripheral transistor and a right peripheral transistor that are adjacent to and are symmetric with each other in configuration, each of the left and right peripheral transistors including the first peripheral active pattern, the first peripheral gate electrode, and the first and second peripheral impurity regions, wherein the first and second peripheral impurity regions of the left peripheral transistor are doped with N-type impurities, and wherein the first and second peripheral impurity regions of the right peripheral transistor are doped with P-type impurities.

11. The semiconductor device of claim 10, wherein the pair transistor structure further includes a second peripheral gate electrode between the first peripheral active pattern of the left peripheral transistor and the first peripheral active pattern of the right peripheral transistor.

12. The semiconductor device of claim 11, wherein a first peripheral gate electrode of the left peripheral transistor, a first peripheral gate electrode of the right peripheral transistor, and the second peripheral gate electrode are provided with voltages that are different from each other.

13. The semiconductor device of claim 1, wherein the cell structure includes a plurality of cell connection pads on a top end of the cell structure, and wherein the peripheral structure includes a plurality of peripheral connection pads on a bottom end of the peripheral structure, the peripheral connection pads contacting the cell connection pads, respectively.

14. The semiconductor device of claim 1, wherein the cell structure further includes a cell interlayer dielectric layer on a top end of the cell structure, and wherein the peripheral structure further includes: a peripheral interlayer dielectric layer on a bottom end of the peripheral structure and contacting the cell interlayer dielectric layer; and a contact plug that penetrates the peripheral interlayer dielectric layer and the cell interlayer dielectric layer to connect one of the first peripheral transistors to one of the plurality of cell transistors.

15. A semiconductor device comprising: a substrate; and a pair transistor structure on the substrate, wherein the pair transistor structure includes: first, second, and third gate electrodes that are sequentially disposed in a first horizontal direction; a first active pattern between the first and second gate electrodes and extending in a vertical direction perpendicular to a top surface of the substrate; a second active pattern between the second and third gate electrodes and extending in the

vertical direction perpendicular to the top surface of the substrate; a pair of first impurity regions on lower portions of the first and second active patterns, respectively; and a pair of second impurity regions on upper portions of the first and second active patterns, respectively, wherein the pair of first impurity regions are spaced apart from the pair of second impurity regions, respectively, in the vertical direction, wherein the first and second impurity regions, among the pair of first and second impurity regions, of the first active pattern are doped with N-type impurities, and wherein the first and second impurity regions, among the pair of first and second impurity regions, of the second active pattern are doped with P-type impurities.

16. The semiconductor device of claim 15, wherein the first, second, and third gate electrodes are provided with voltages that are different from each other.

17. The semiconductor device of claim 15, further comprising: a first wiring line that connects the first impurity regions of the first and second active patterns with each other, wherein a second impurity region of the first active pattern is grounded, and wherein a second impurity region of the second active pattern is provided with a power voltage.

18. The semiconductor device of claim 15, wherein the substrate includes a first source/drain connection line and a second source/drain connection line that are side by side in the first horizontal direction, wherein the first, second, and third gate electrodes extend in the first horizontal direction to extend across the first source/drain connection line and the second source/drain connection line, wherein the first active pattern is on the first source/drain connection line, and wherein the second active pattern is on the second source/drain connection line.

19. A semiconductor device comprising: a substrate; a plurality of pair transistor structures arranged in M rows and N columns on the substrate; and a plurality of wiring lines that connect the pair transistor structures with each other, wherein M and N are each a natural number of equal to or greater than 2, wherein each of the pair transistor structures includes a left transistor and a right transistor that are symmetric with each other, wherein each of the left transistor and the right transistor includes: an active pattern extending in a vertical direction perpendicular to a top surface of the substrate; a gate electrode adjacent to one side of the active pattern; a first impurity region on a lower portion of the active pattern; and a second impurity region on an upper portion of the active pattern, wherein, in each of the left transistor and the right transistor, the first impurity region and the second impurity region are spaced apart from each other in the vertical direction, and wherein the plurality of wiring lines include: a first wiring line that connects the first impurity regions of the pair transistor structures with each other; a second wiring line that connects the second impurity regions of the pair transistor structures with each other; and a third wiring line that connects the gate electrodes of the pair transistor structures with each other.

20. The semiconductor device of claim 19, further comprising: a plurality of first conductive patterns between the first wiring line and the first impurity region of each of the left and right transistors; and a plurality of second conductive patterns between the second wiring line and the second impurity region of each of the left and right transistors, wherein, when viewed in a plan view, each of the plurality of first and second conductive patterns has an island shape, a linear shape, or a plate shape.