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(54) **SYSTEMS AND METHODS FOR PARALLEL ELECTRICAL ENDURANCE TESTING OF CONTACTS**

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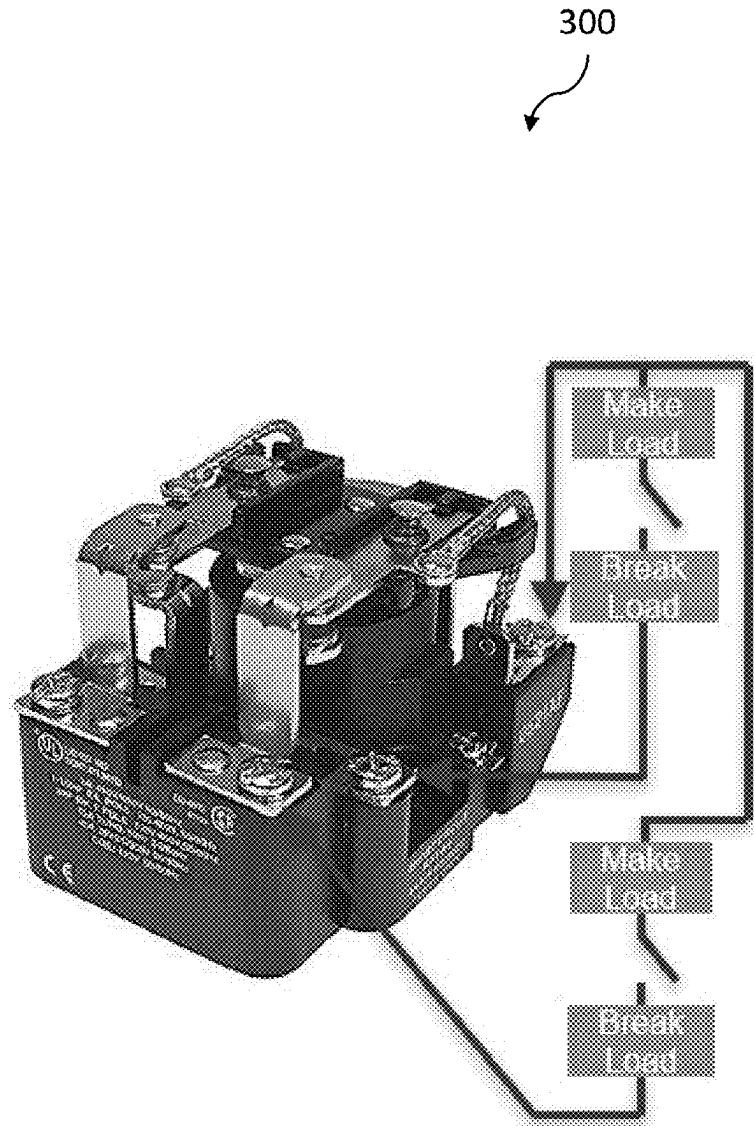
(52) **U.S. Cl.**

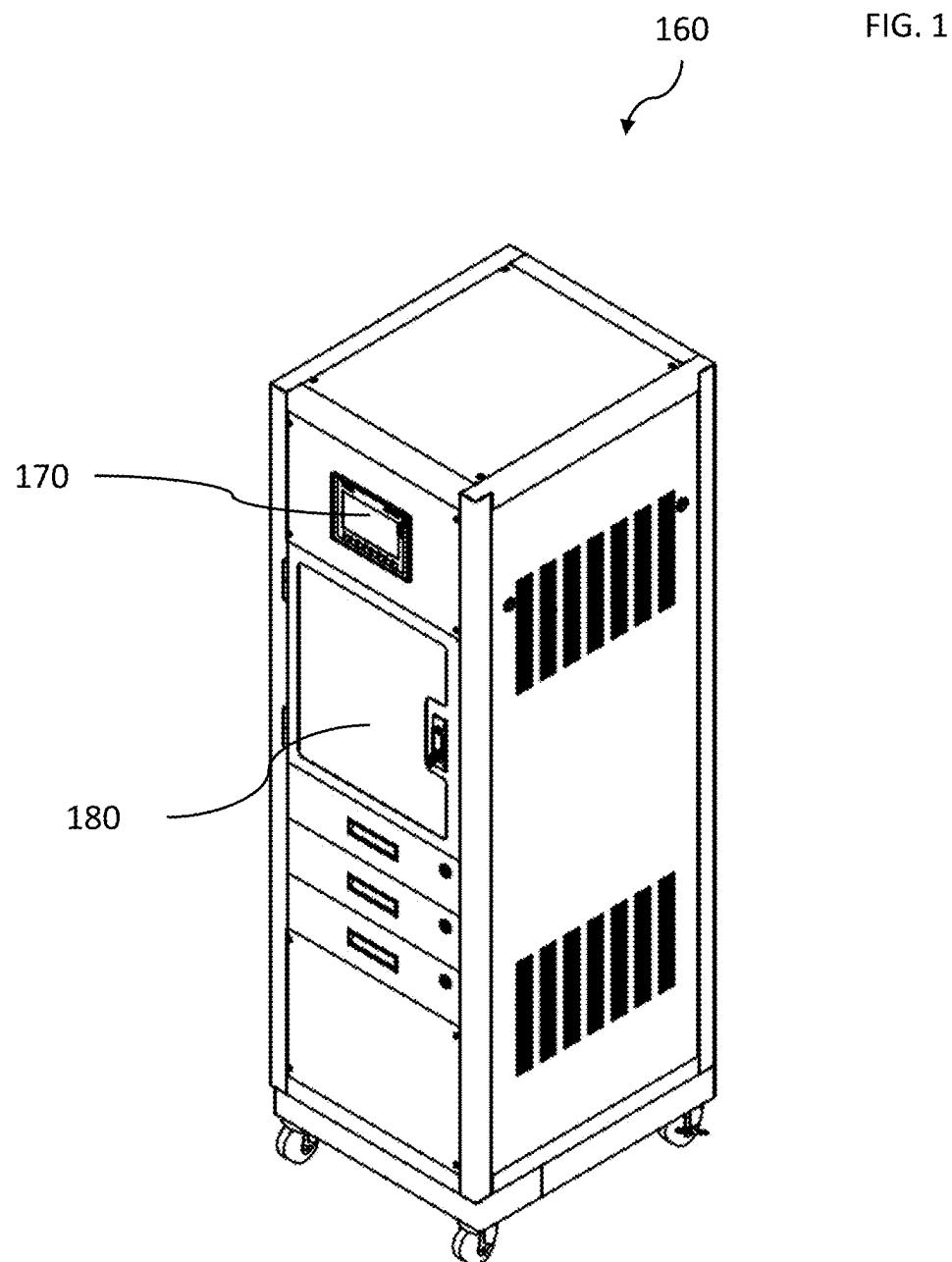
CPC **G01R 31/327** (2013.01)

(57) **ABSTRACT**

An apparatus for testing a plurality of electrical switches including contacts to connect multiple sample switches to an input and an output. A power source is connected to the inputs of the sample switches, and other switches are connected to the outputs of the sample switches so that the sample switches may be selectively connected to either a make load or a break load to perform testing on the sample switches. The sample switches may further be made of silicon carbide MOSFETs that shutoff using a zero-crossing current sensing logic. The voltage at the sample switches may further be monitored by a universal voltage board configured to sense various alternating and direct current (AC or DC) voltages so that various types of sample switches may be tested.

FIG. 3





200

FIG. 2

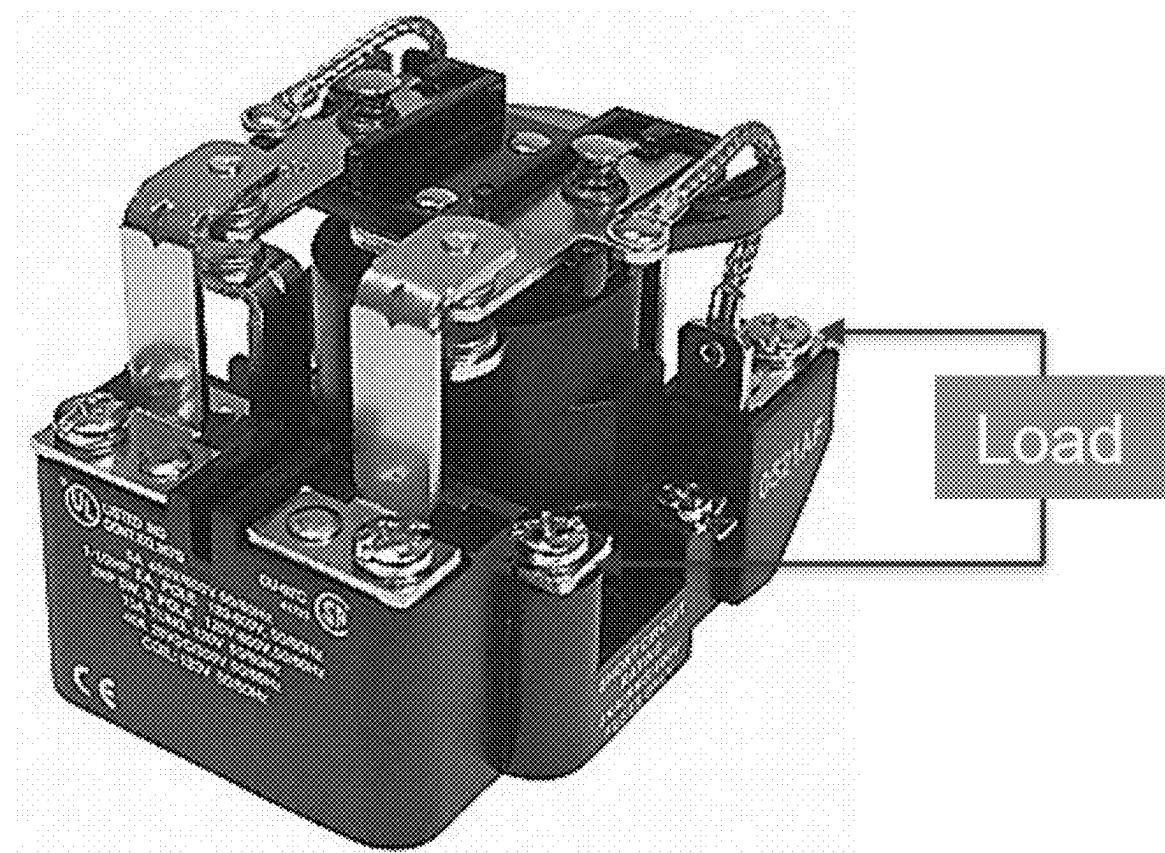


FIG. 3

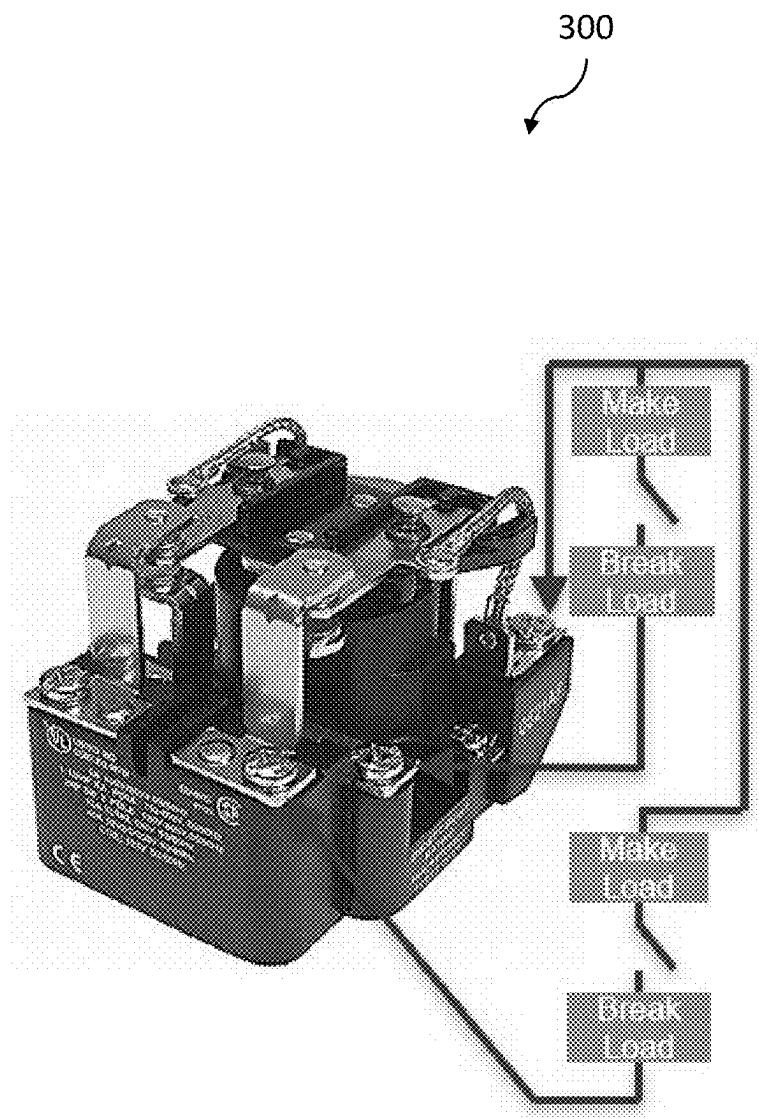


FIG. 4

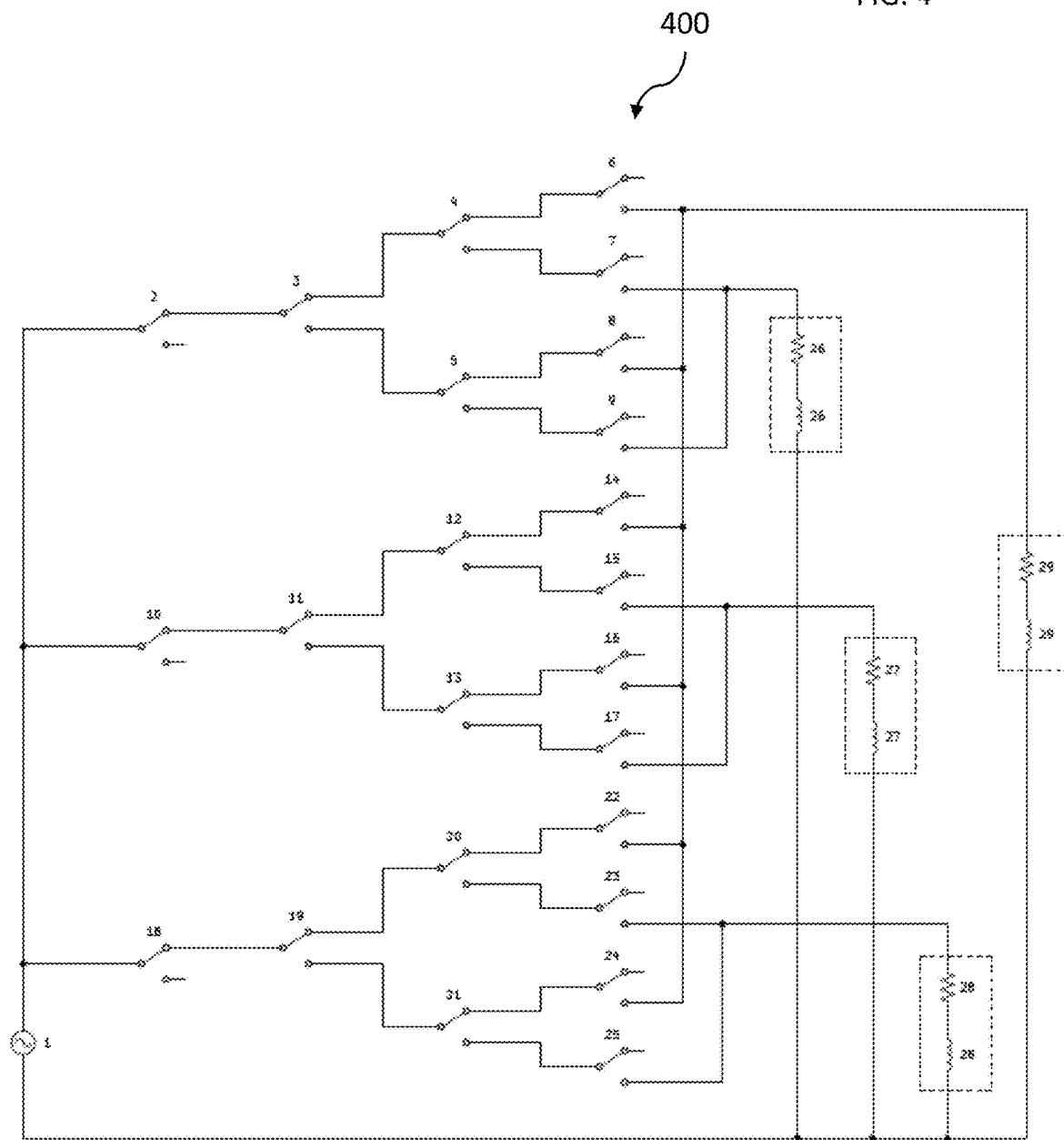


FIG. 5

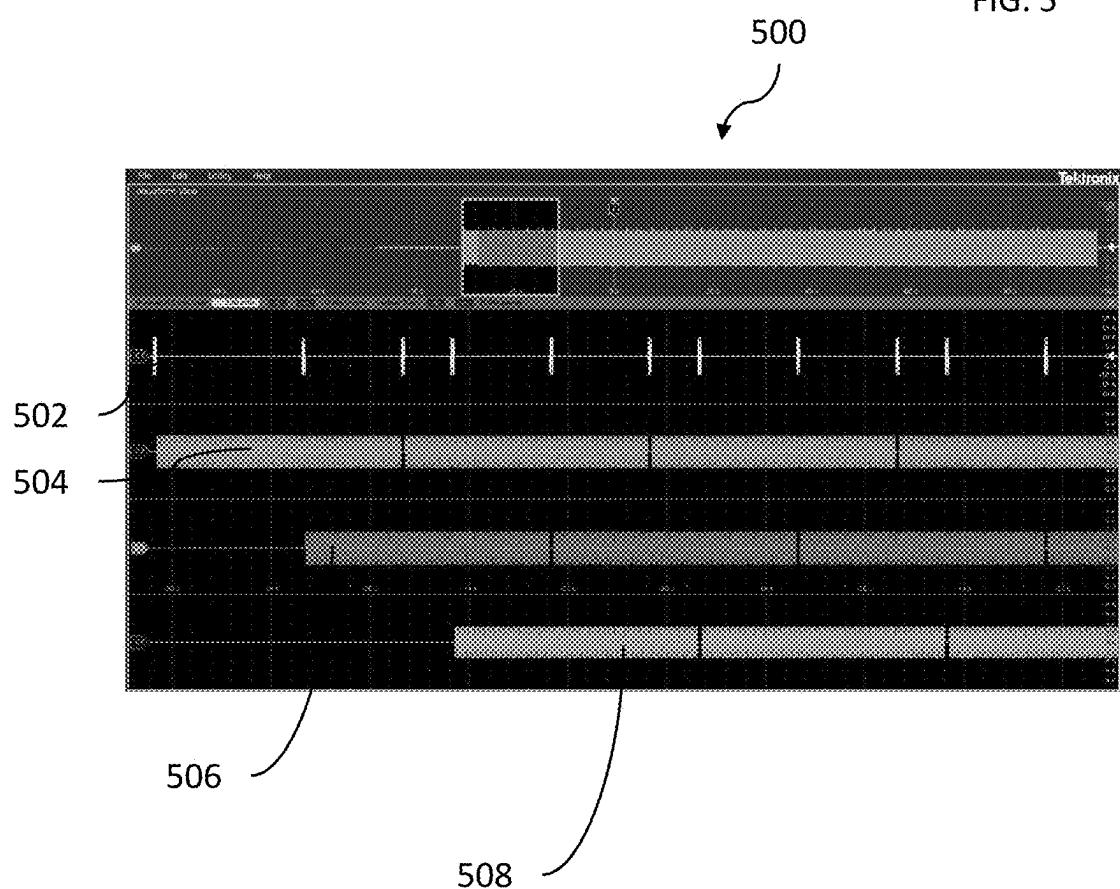


FIG. 6

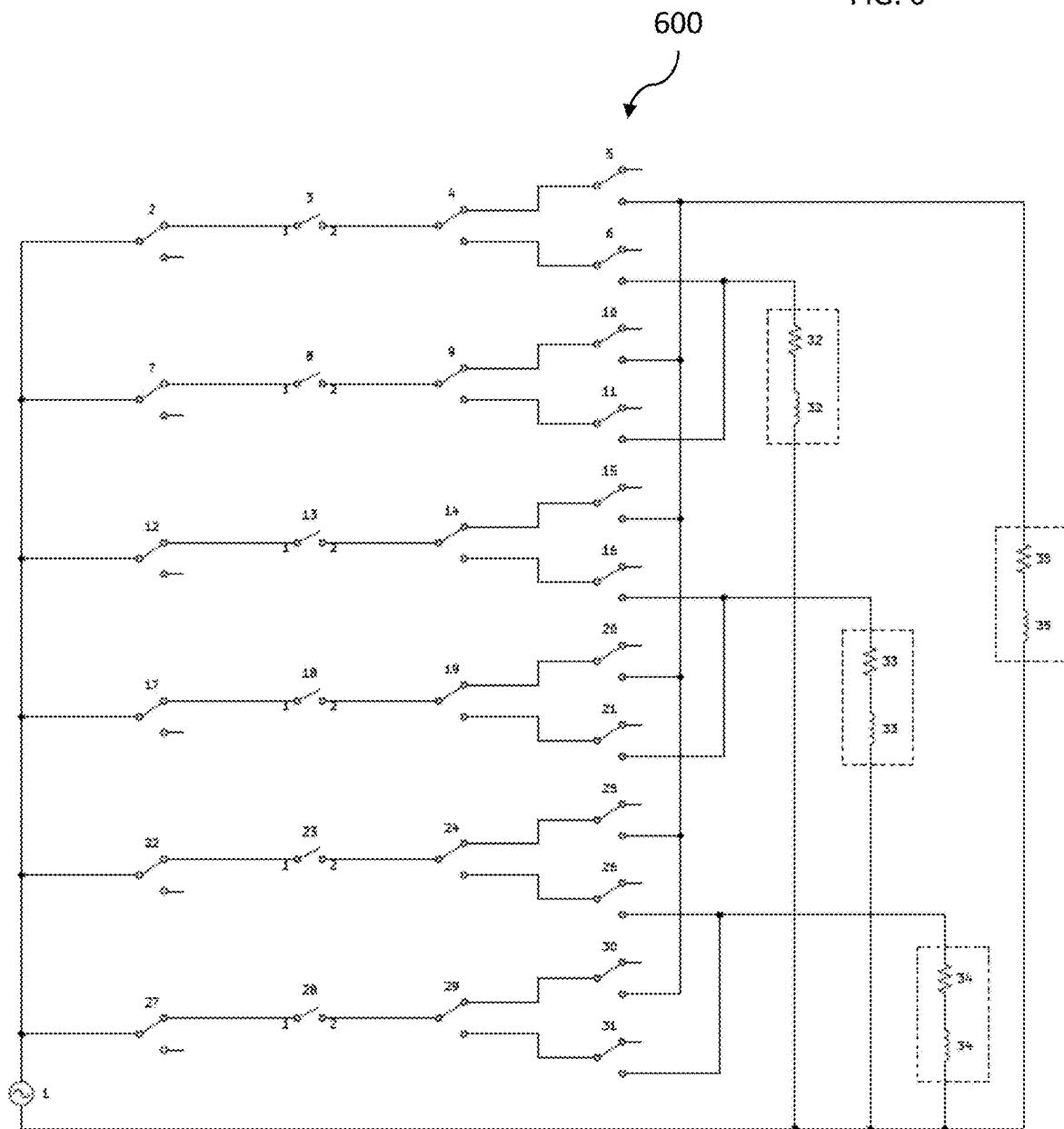


FIG. 7

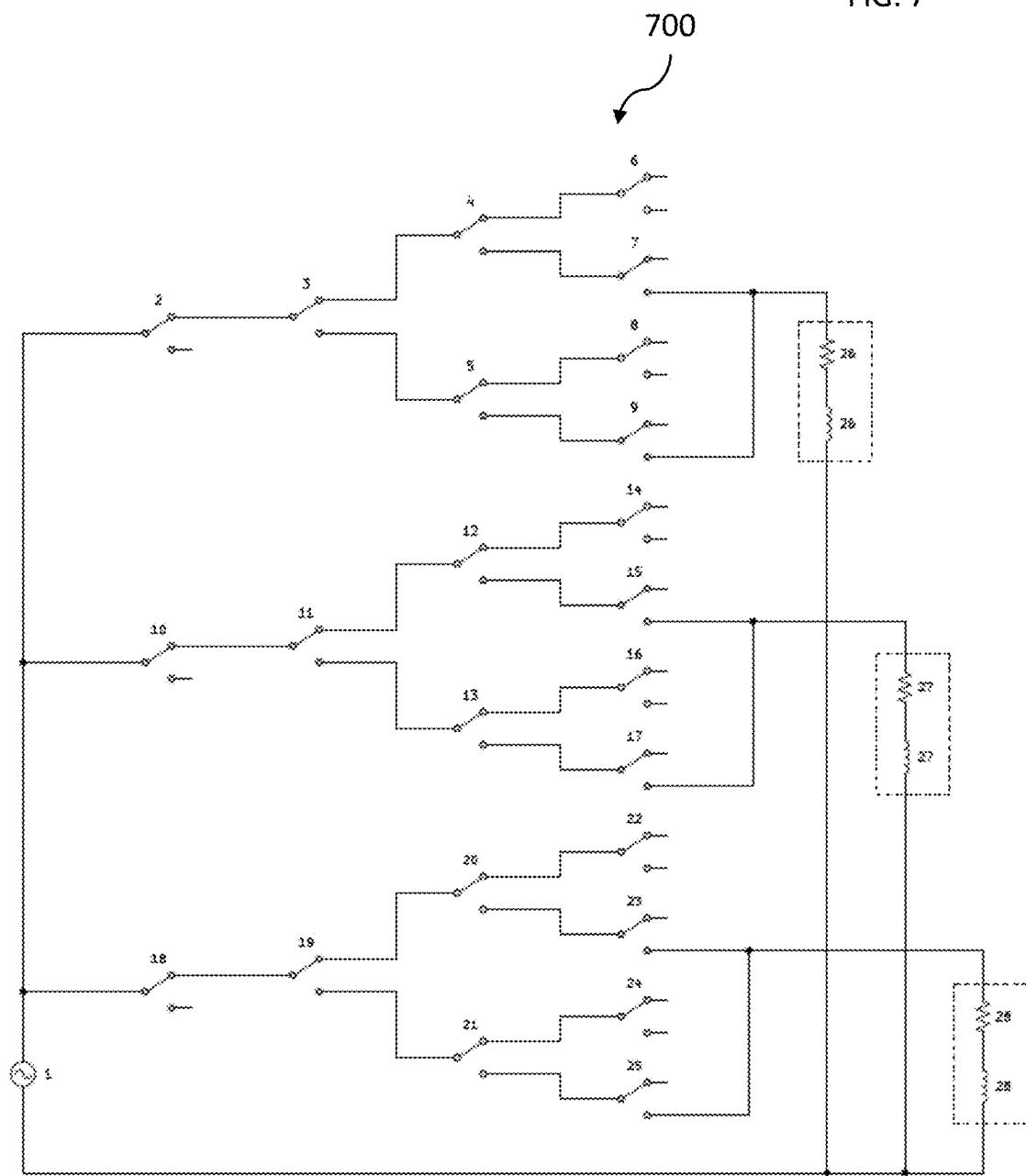


FIG. 8

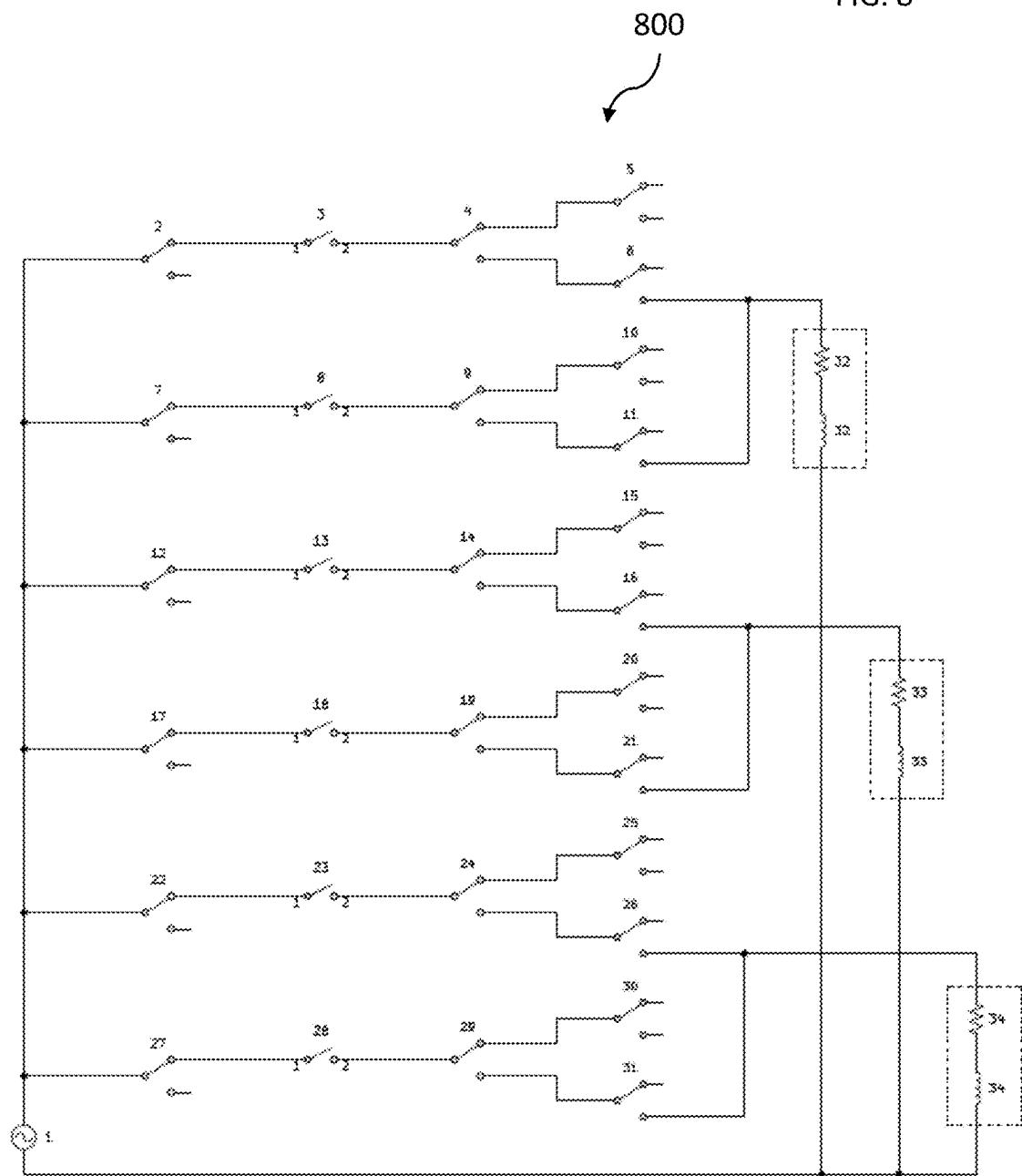


FIG. 9

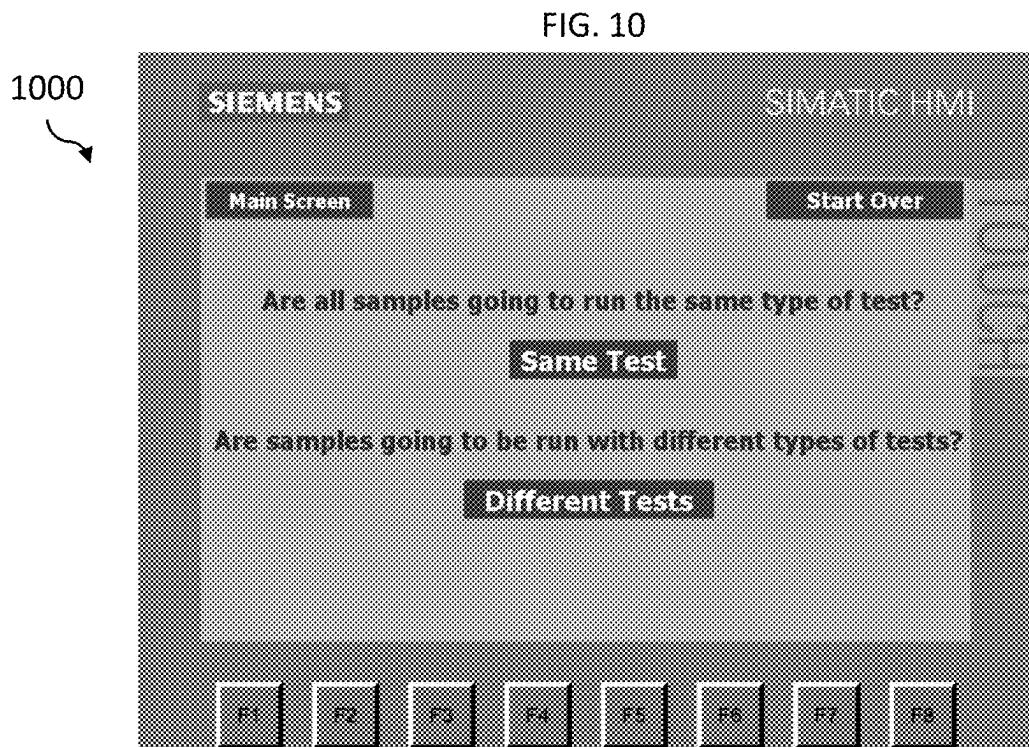
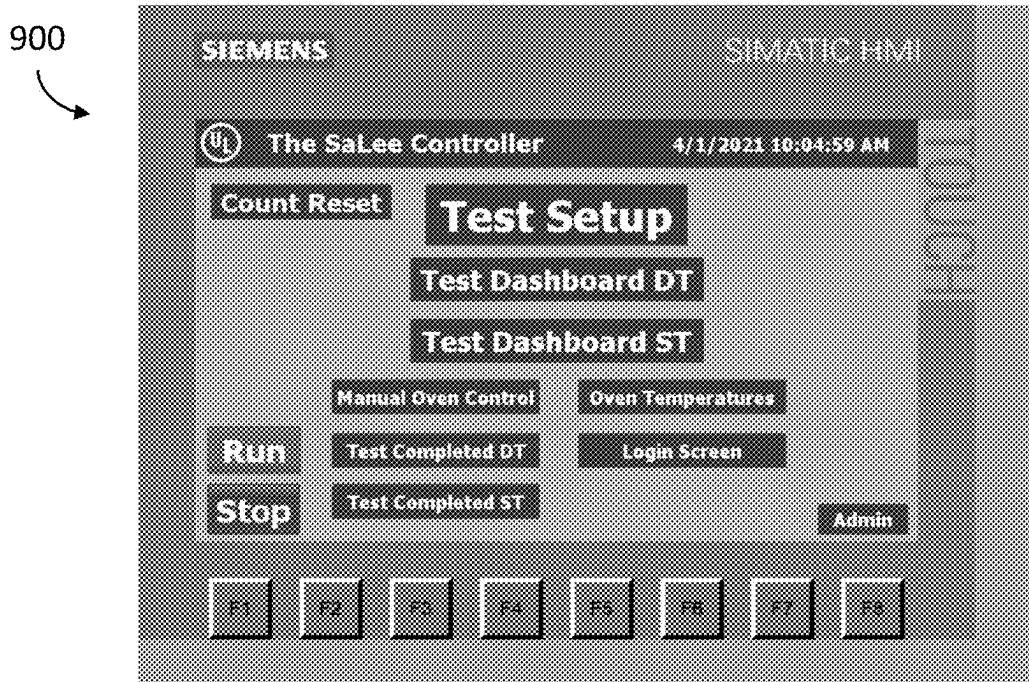
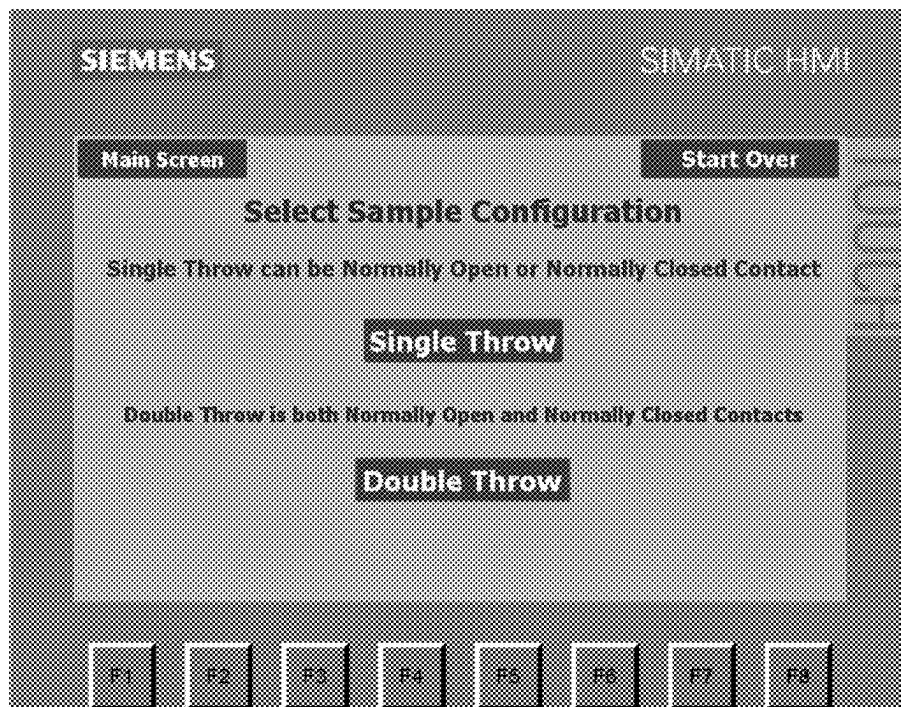


FIG. 11

1100



1200

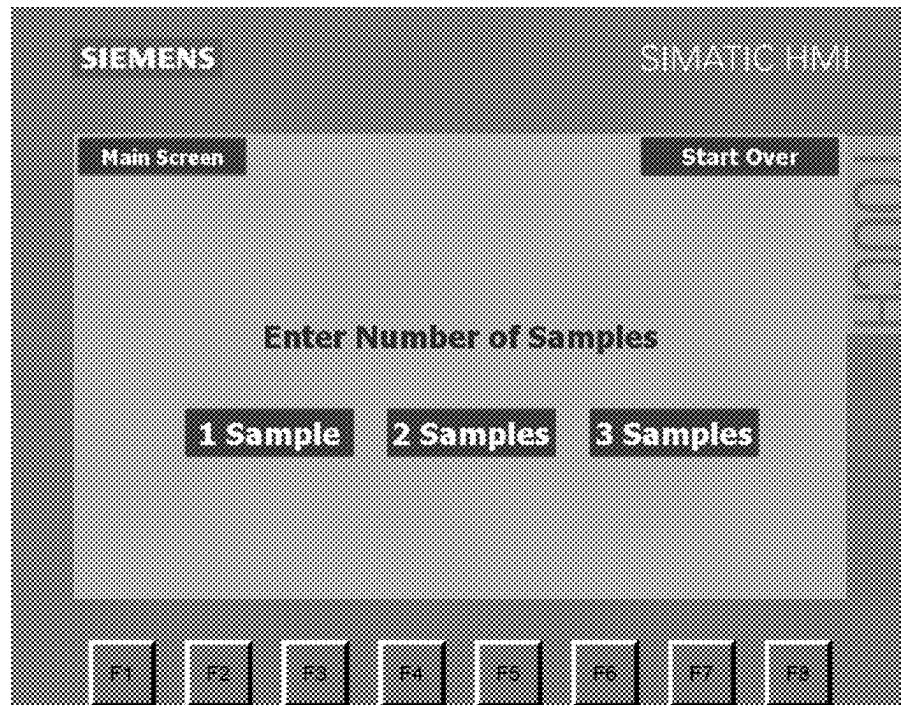


FIG. 13

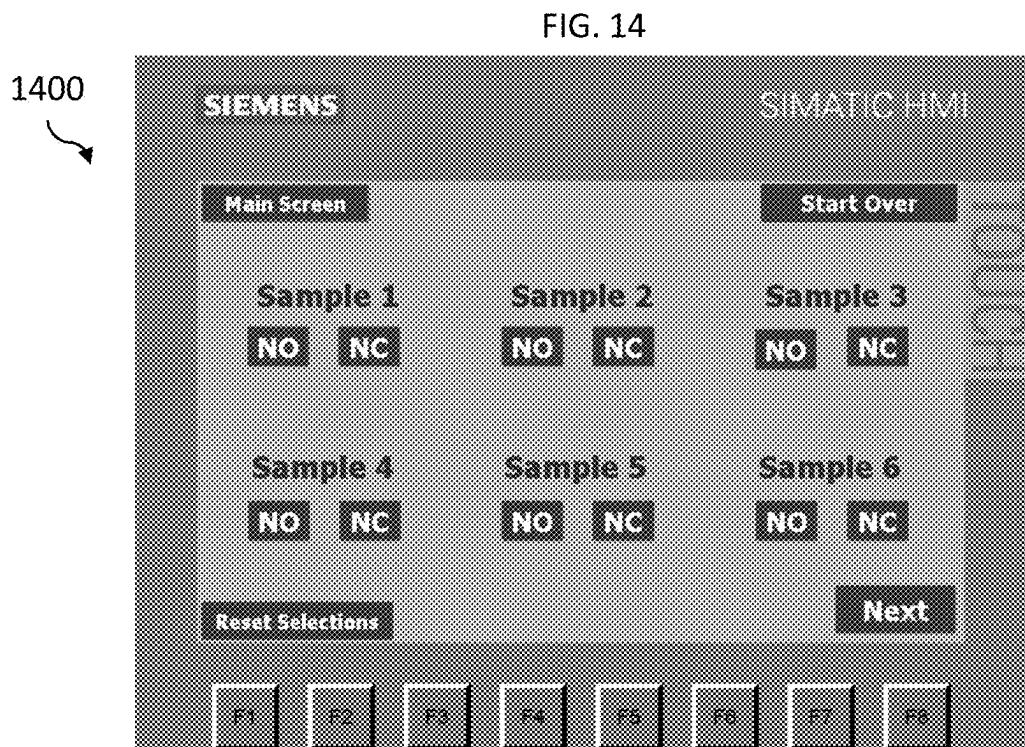
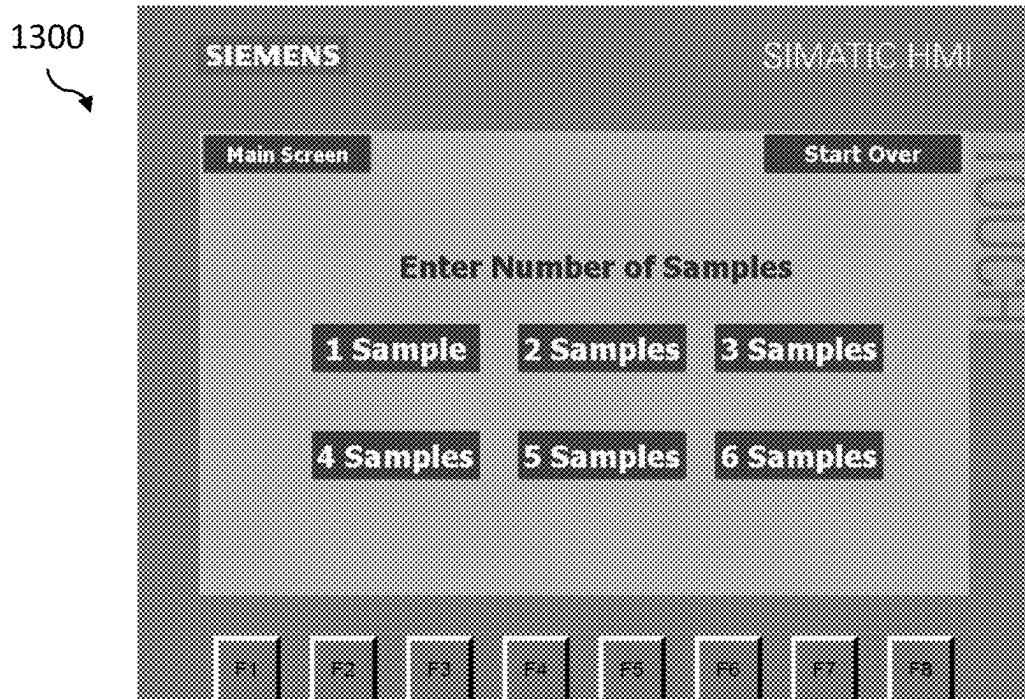


FIG. 15

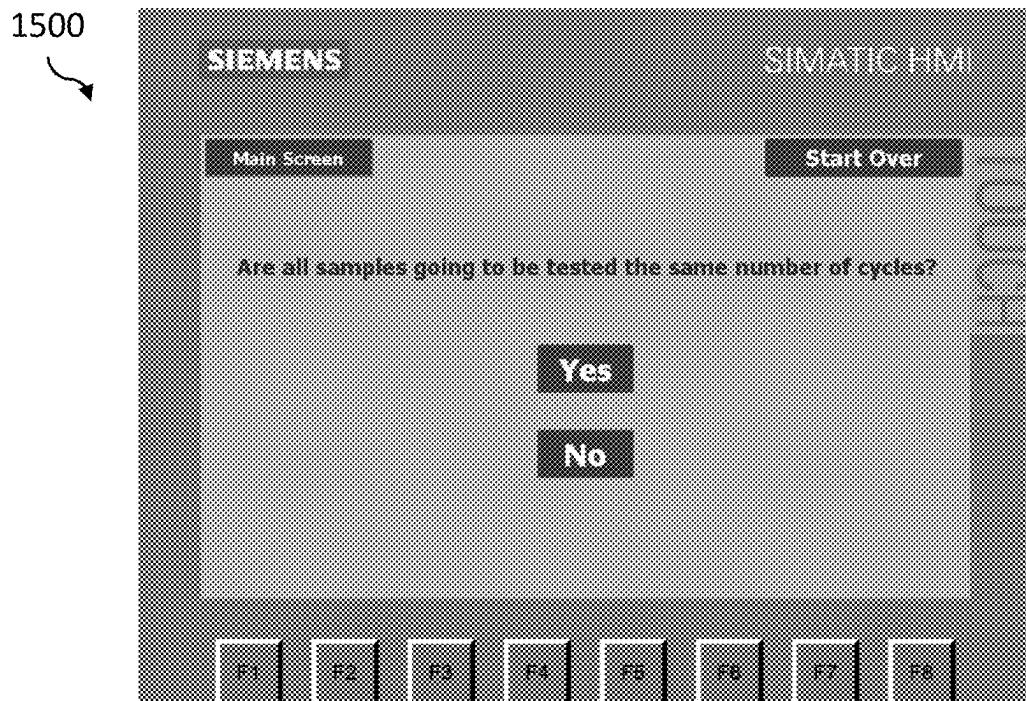


FIG. 16

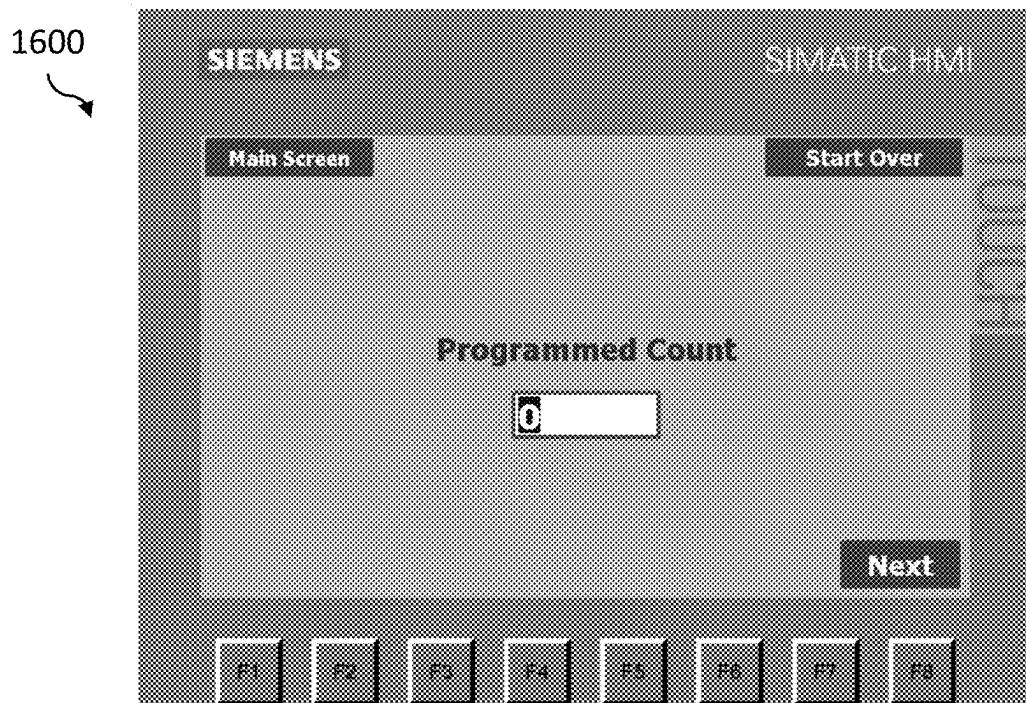


FIG. 17

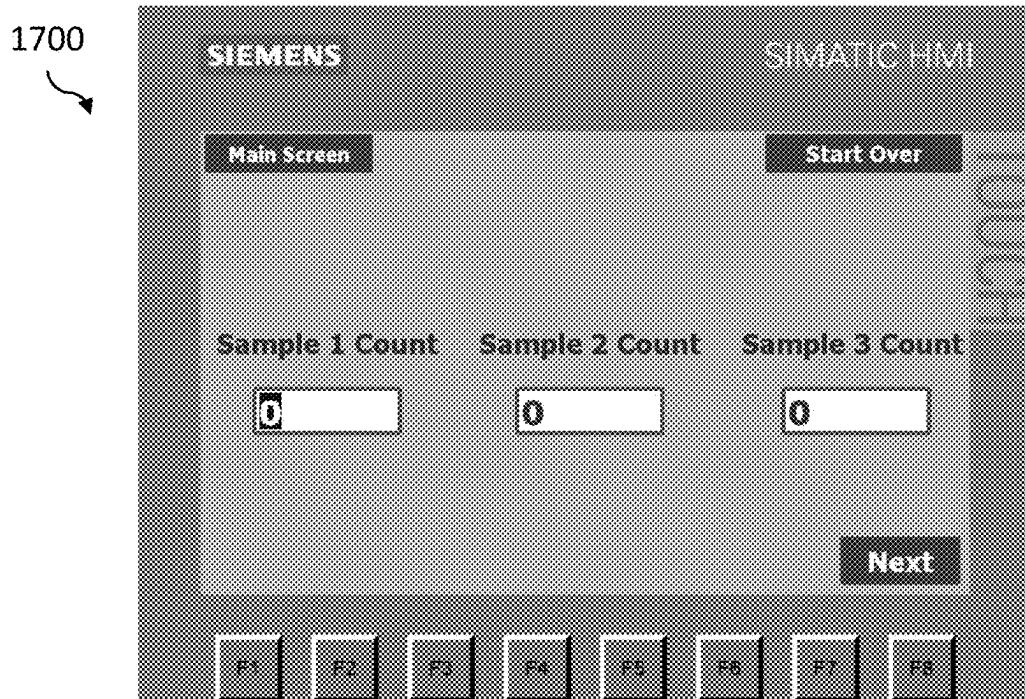


FIG. 18

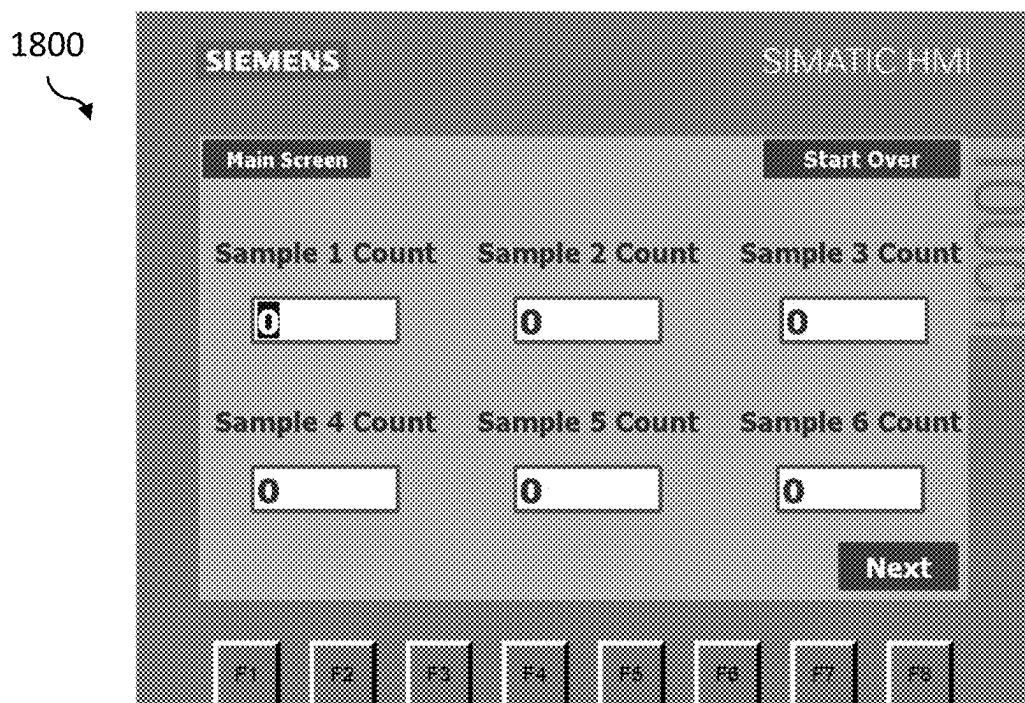


FIG. 19

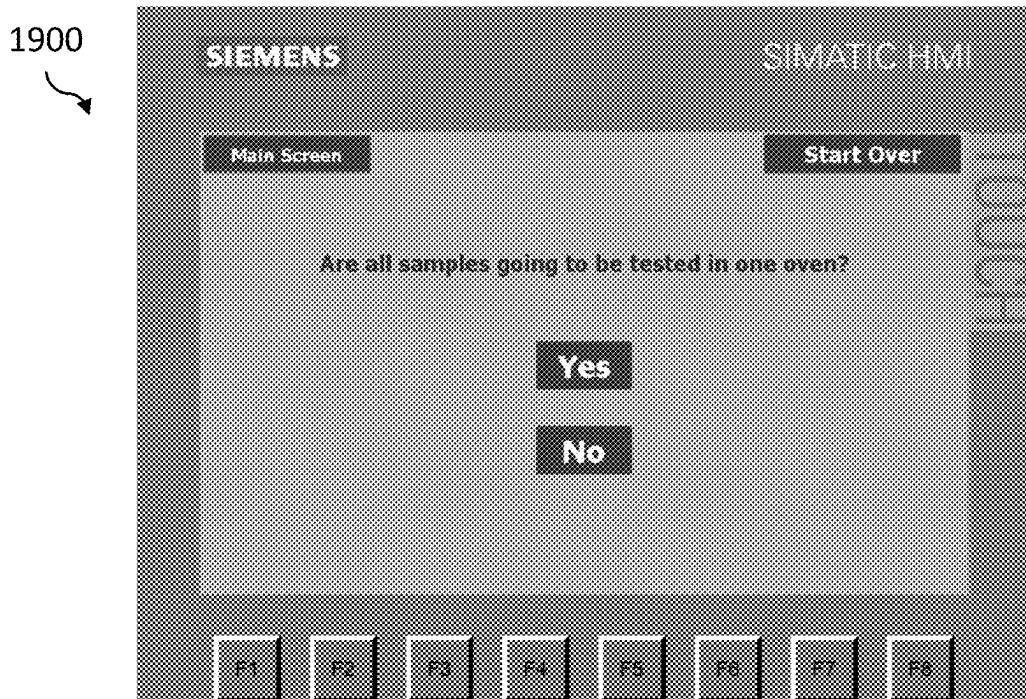


FIG. 20

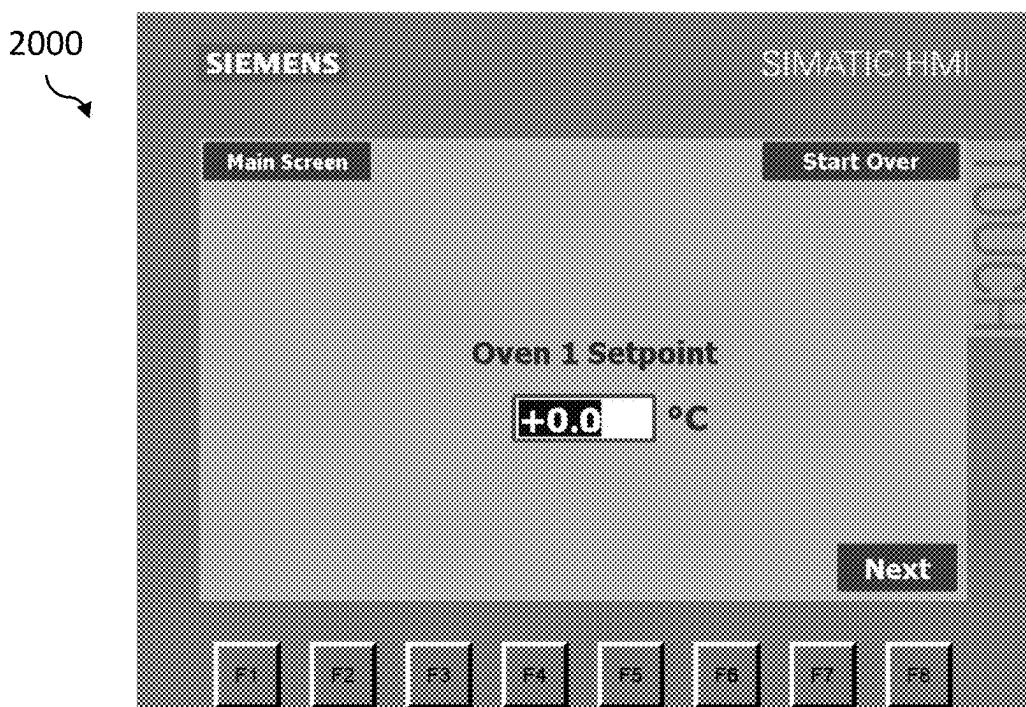


FIG. 21

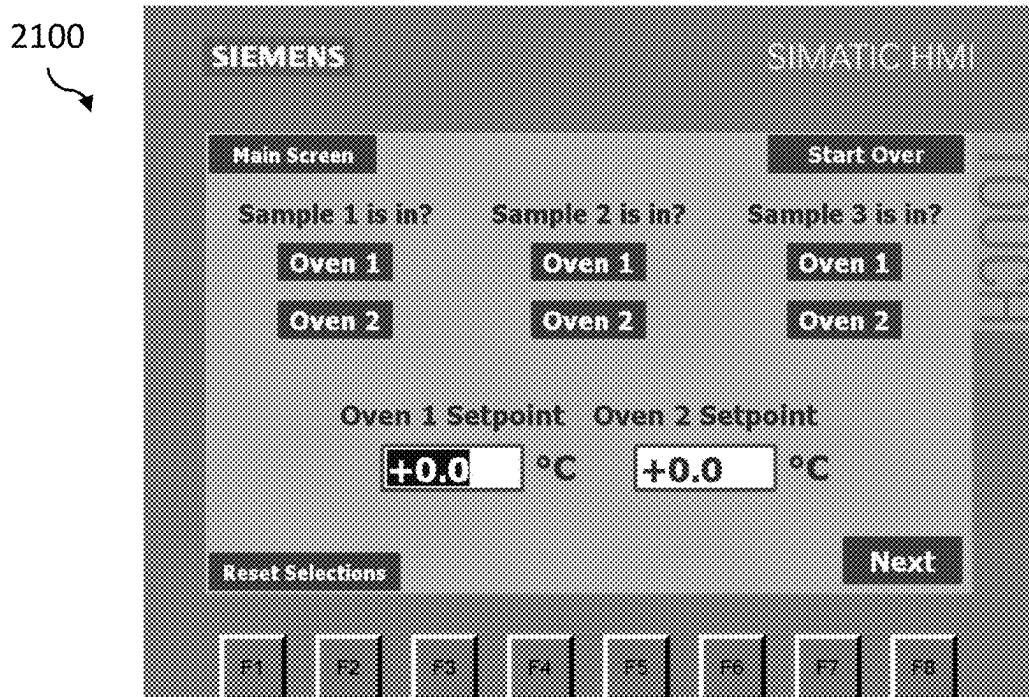


FIG. 22

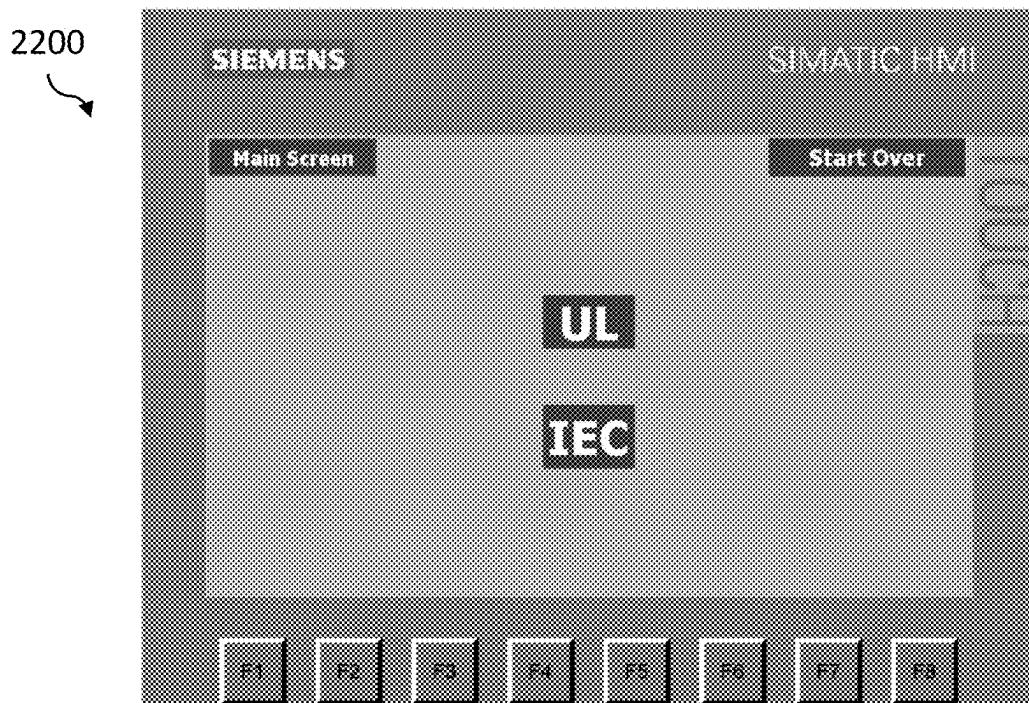


FIG. 23

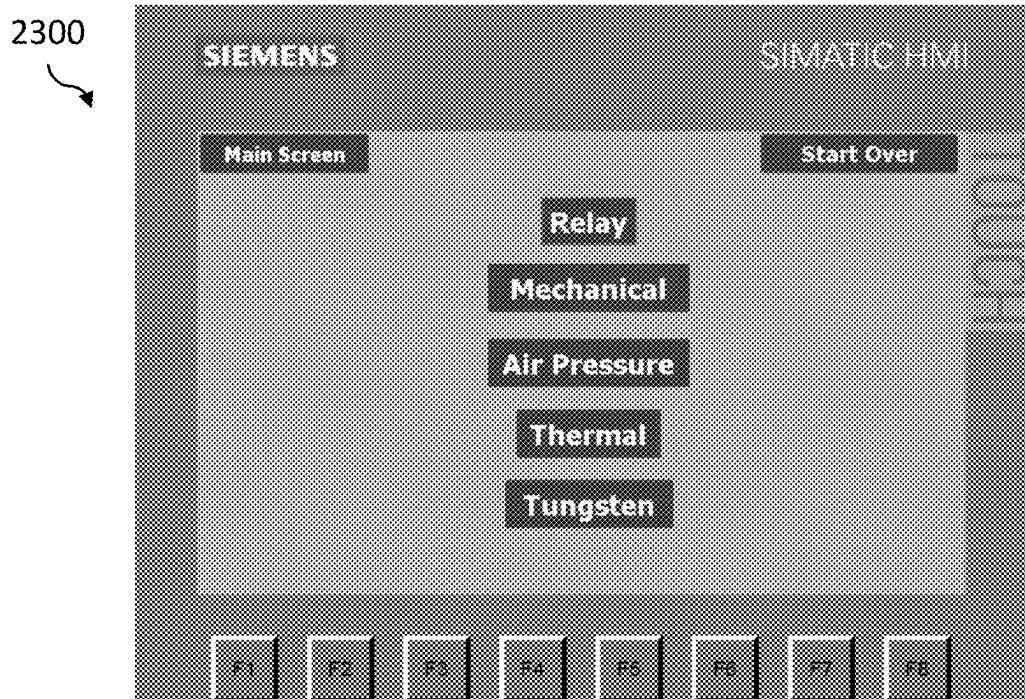


FIG. 24

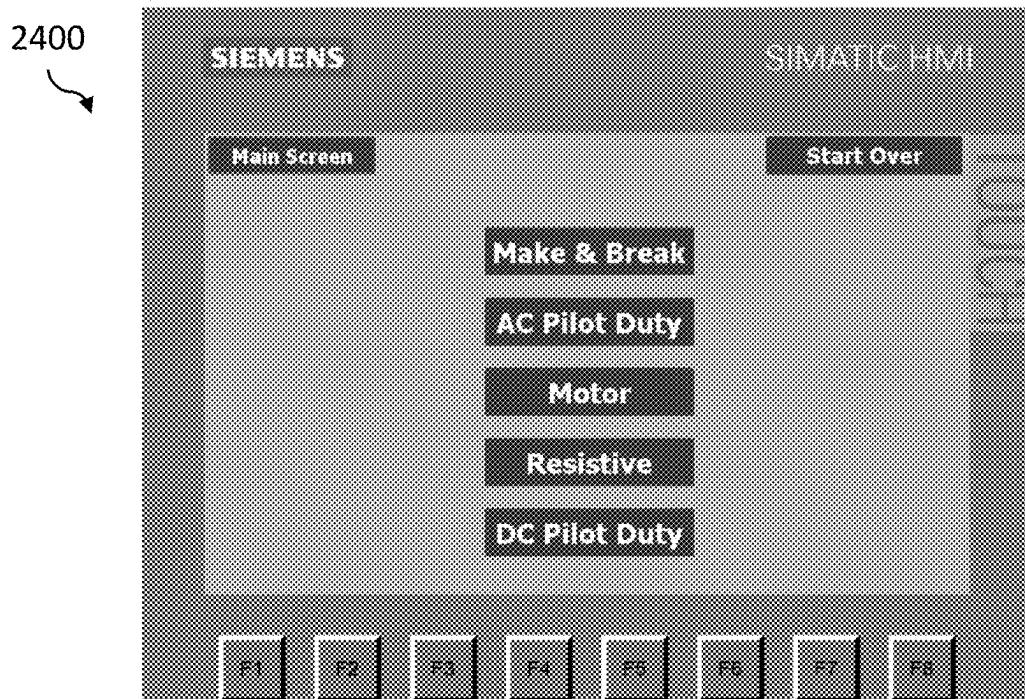


FIG. 25

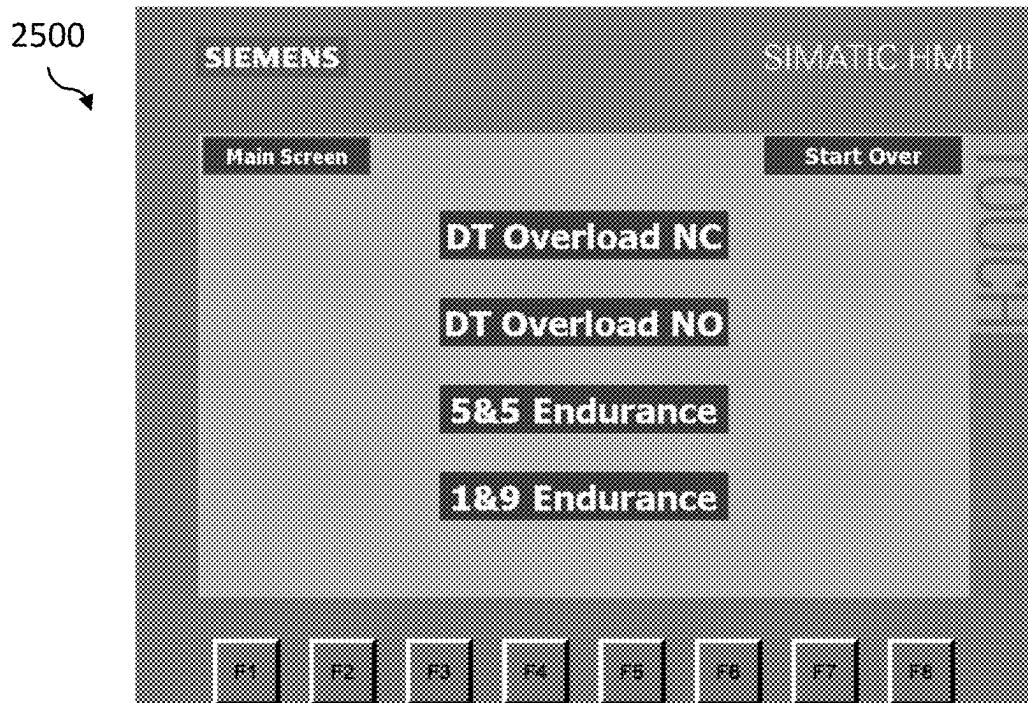


FIG. 26

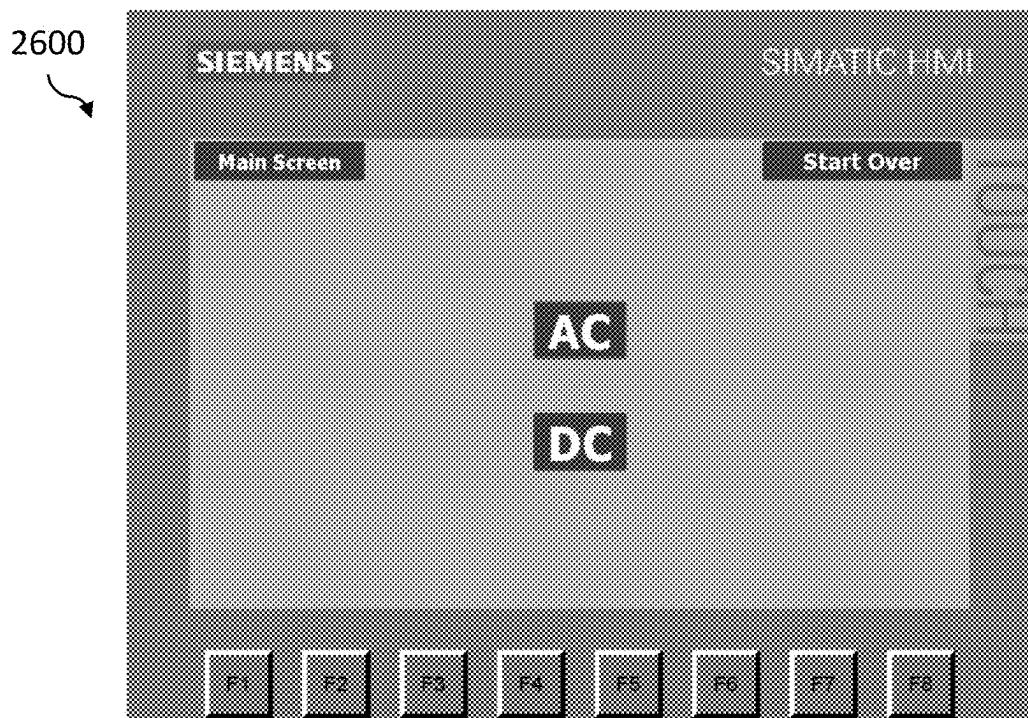


FIG. 27

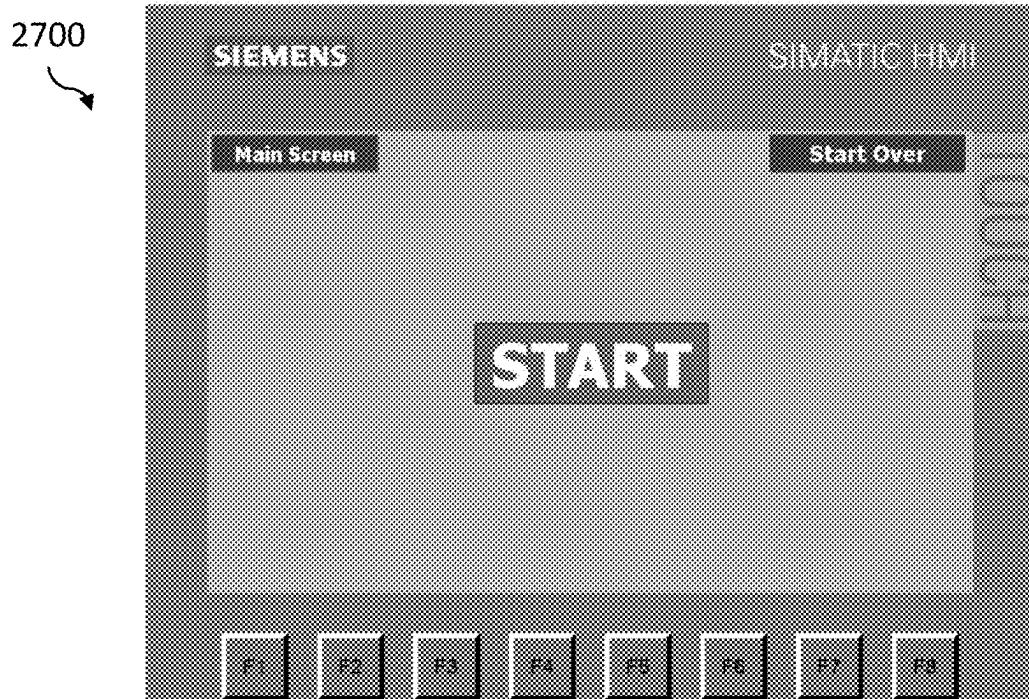


FIG. 28

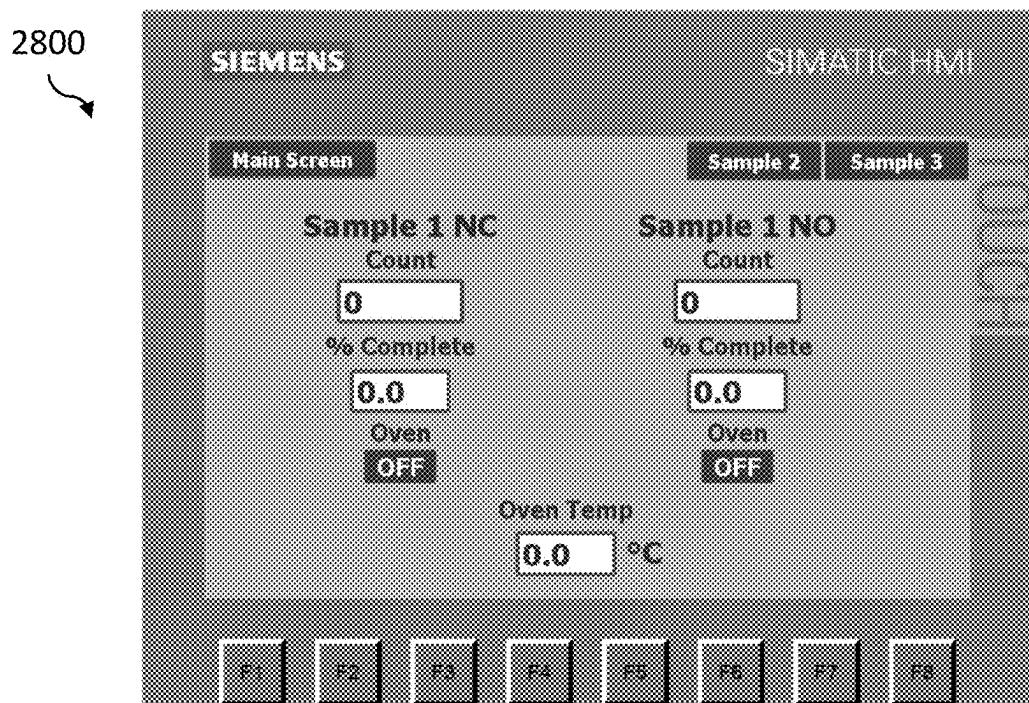


FIG. 29

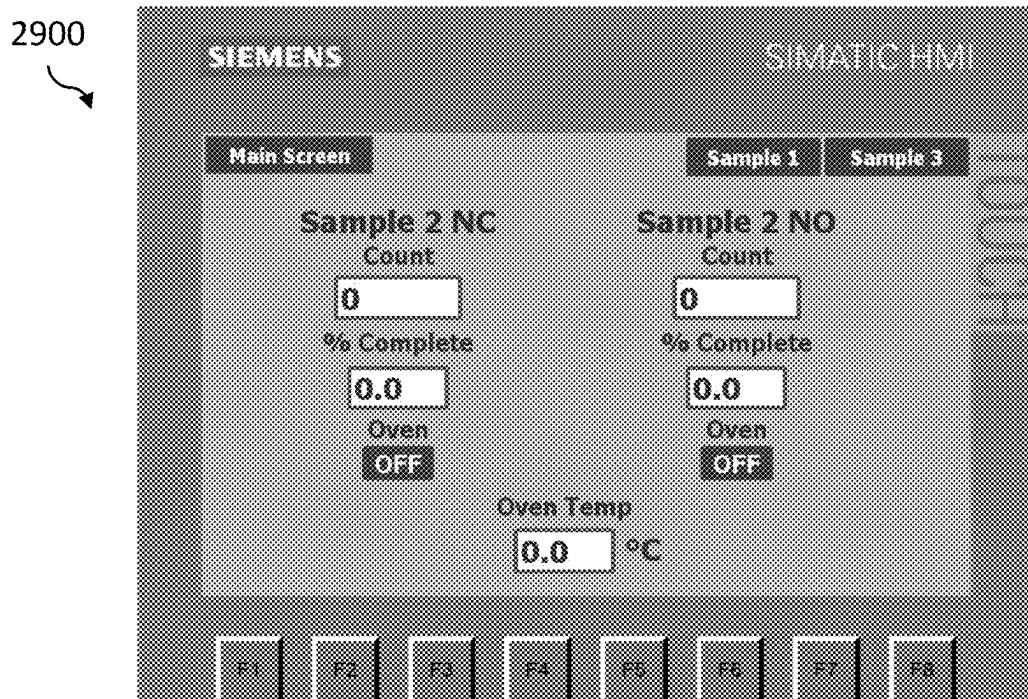


FIG. 30

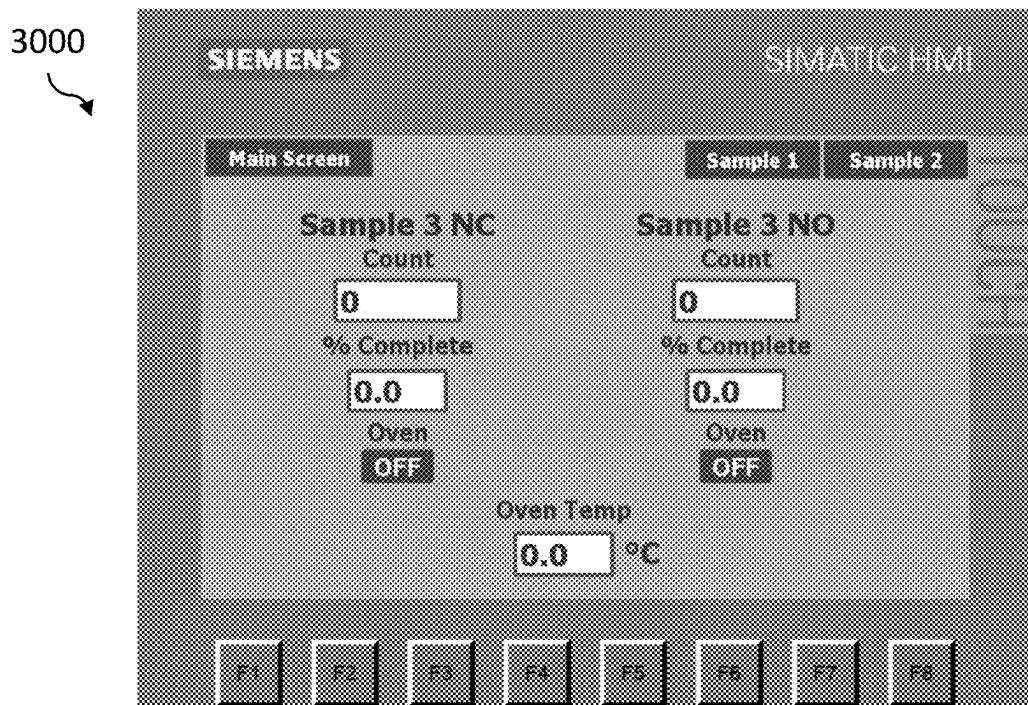


FIG. 31

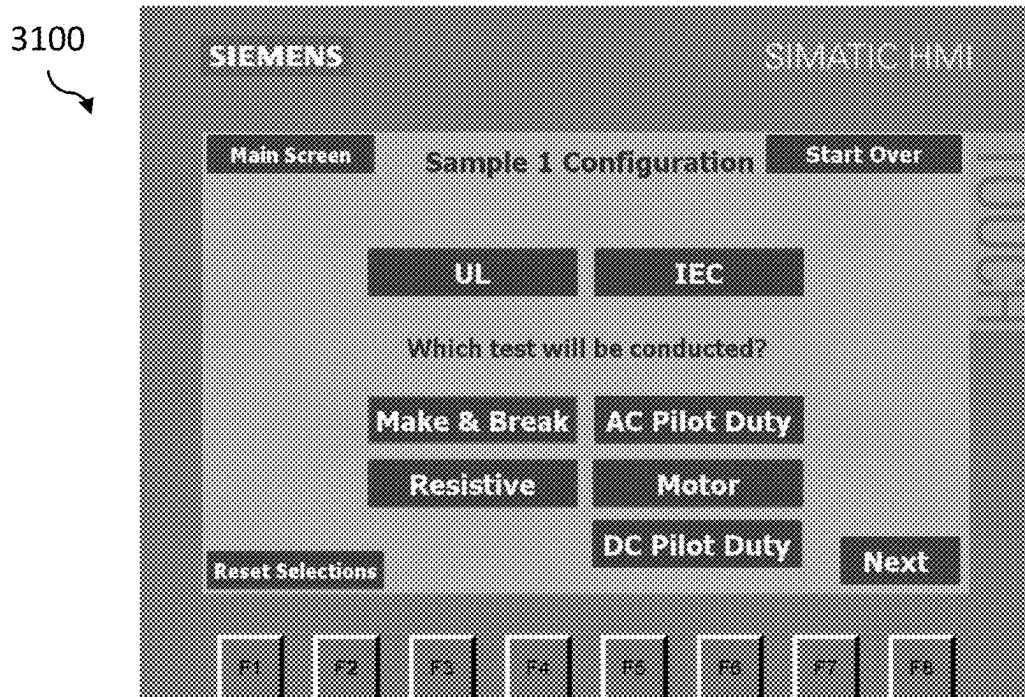


FIG. 32

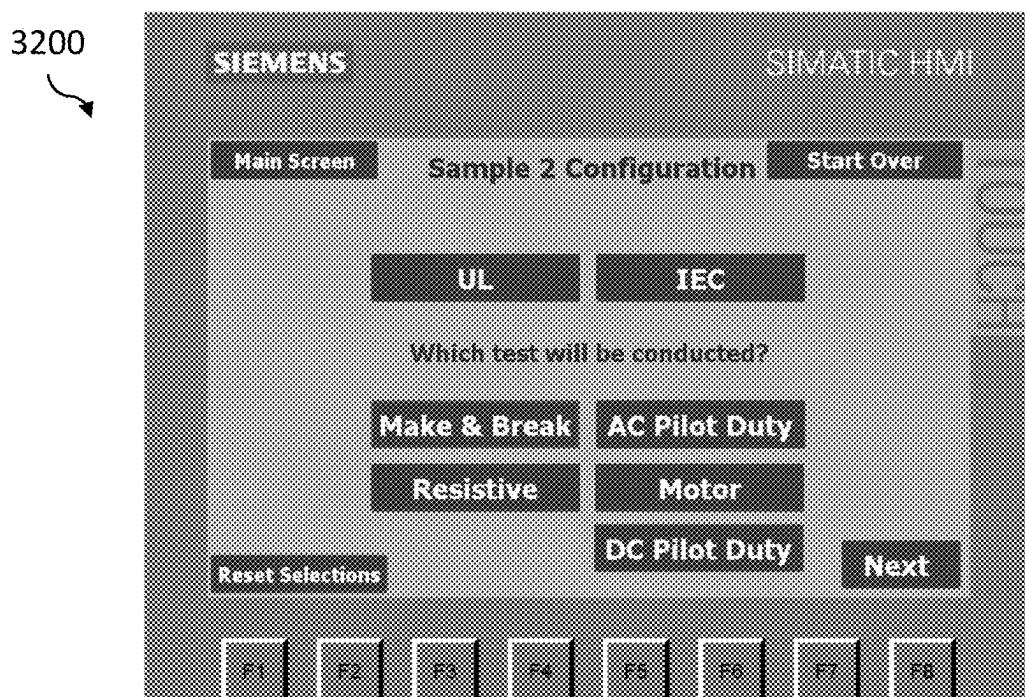
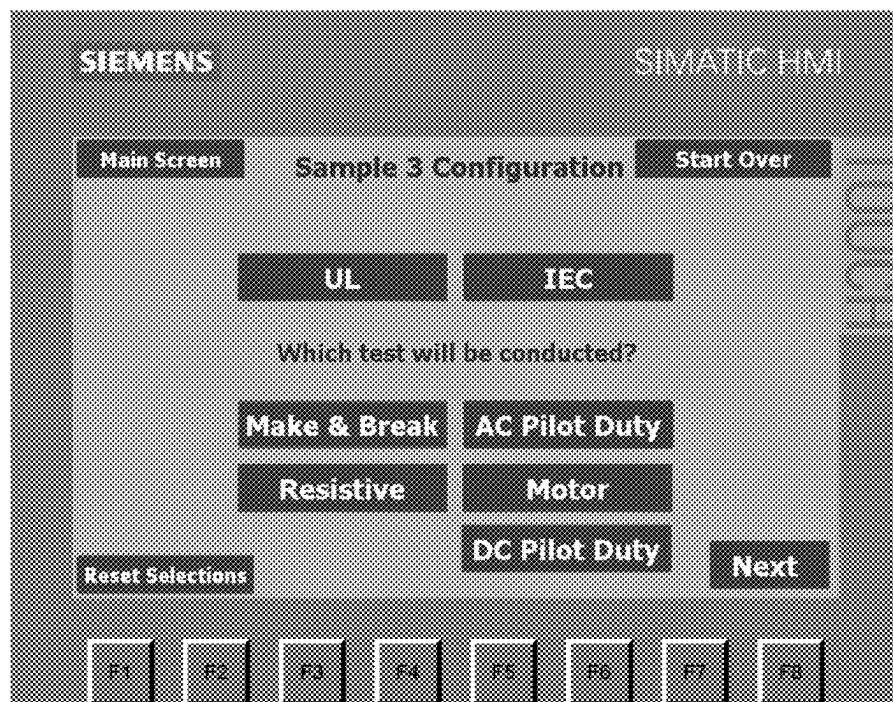


FIG. 33

3300



3400

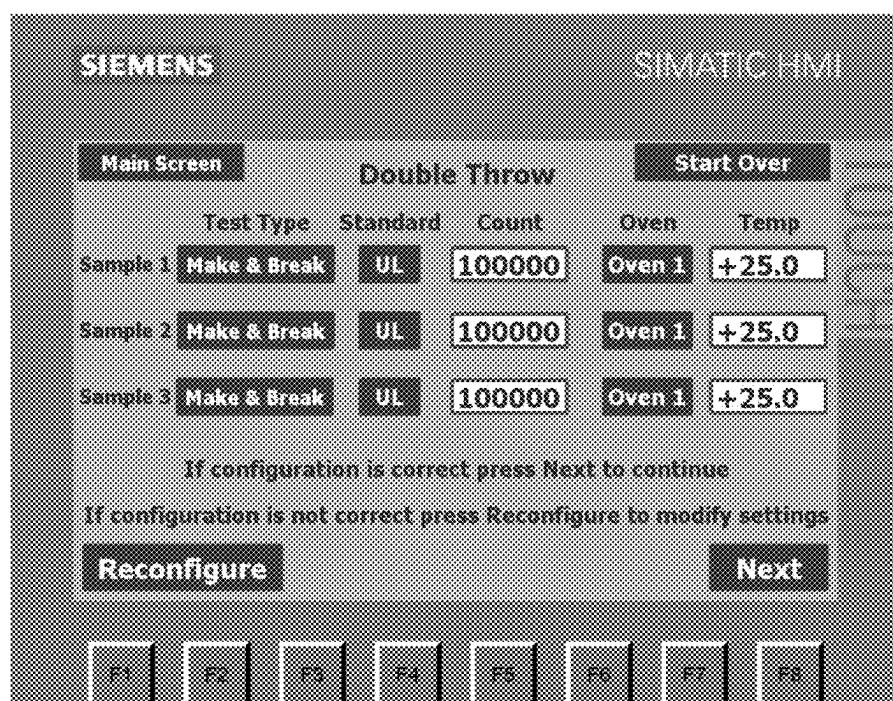


FIG. 35

3500

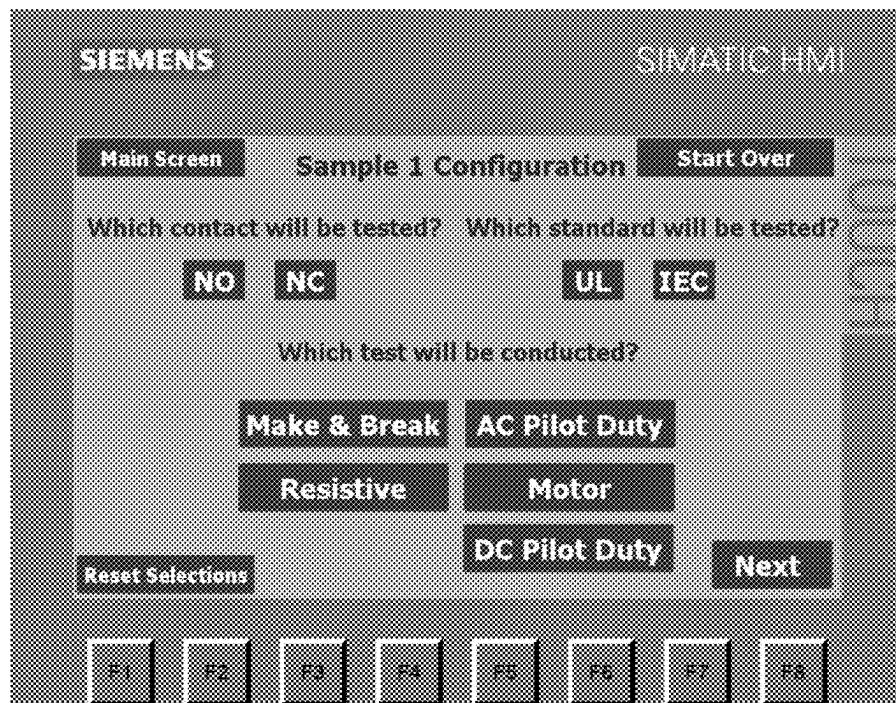


FIG. 36

3600

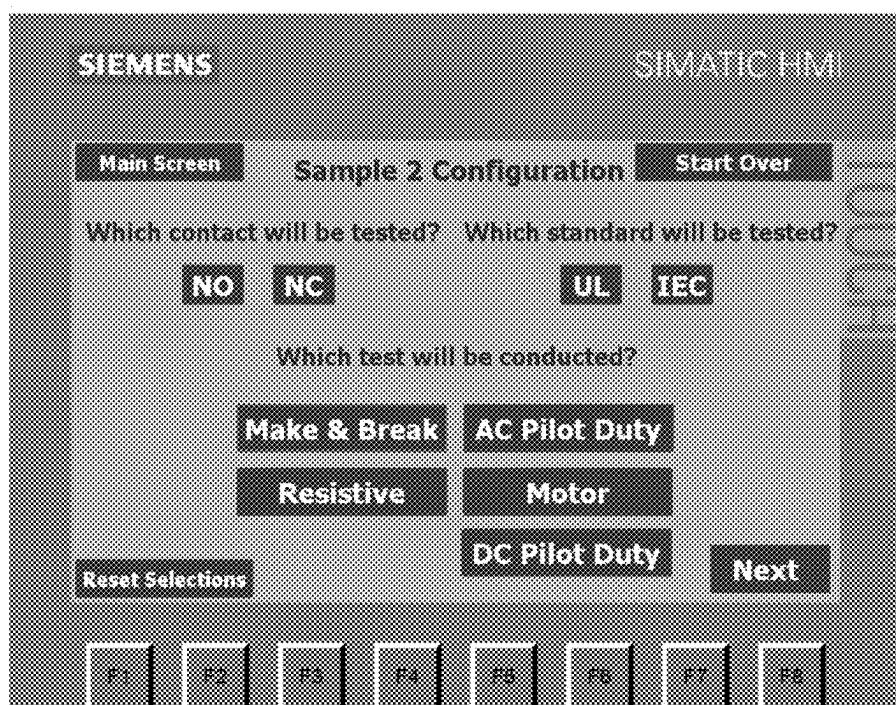


FIG. 37

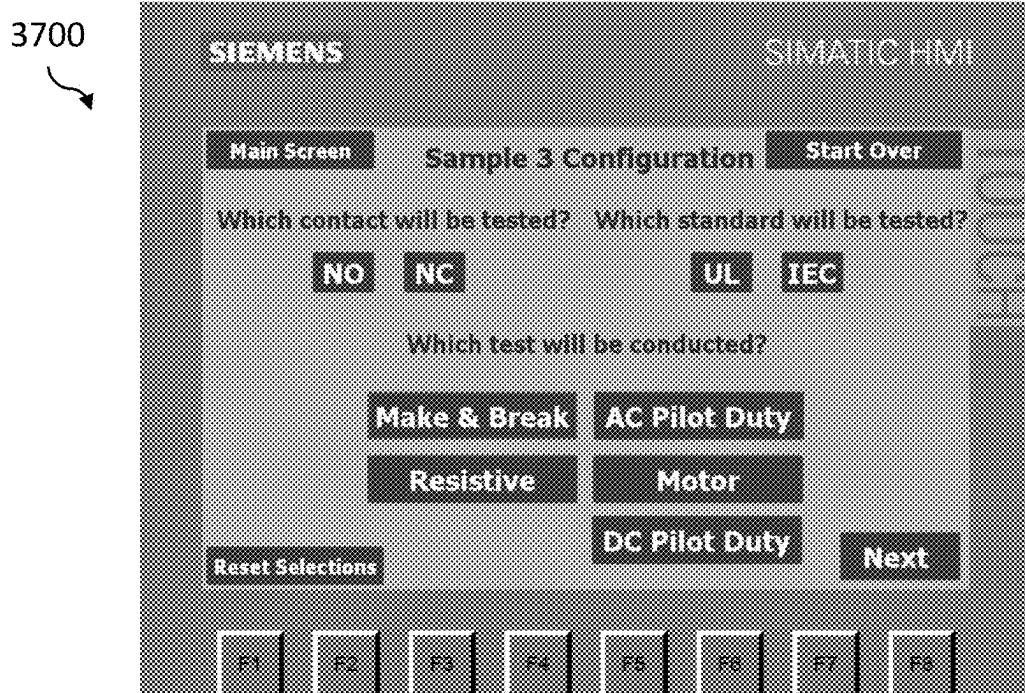


FIG. 38

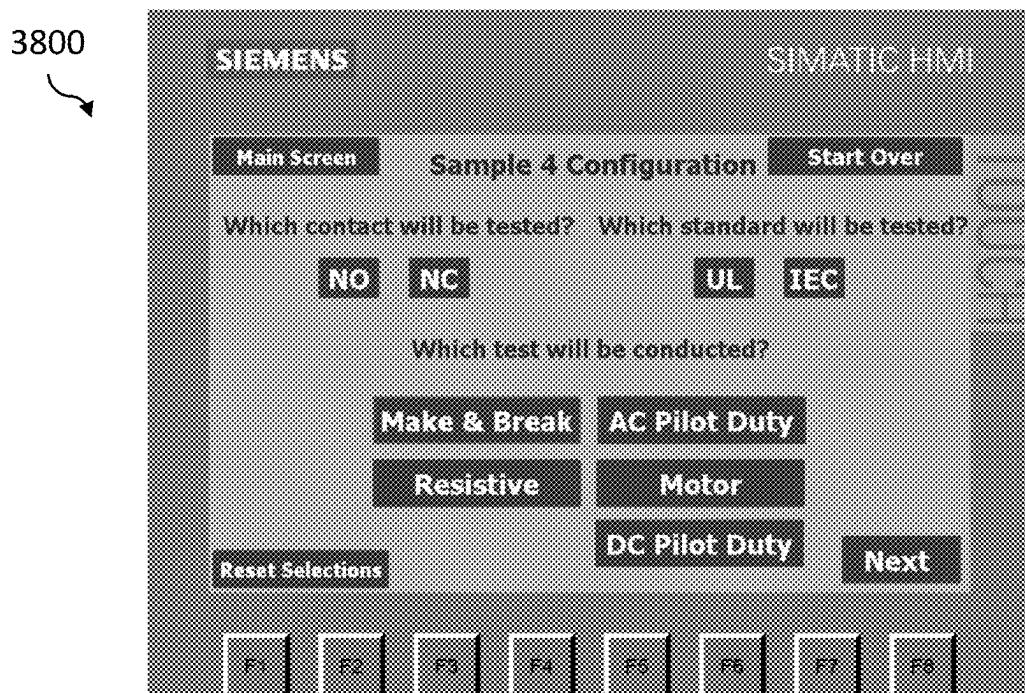


FIG. 39

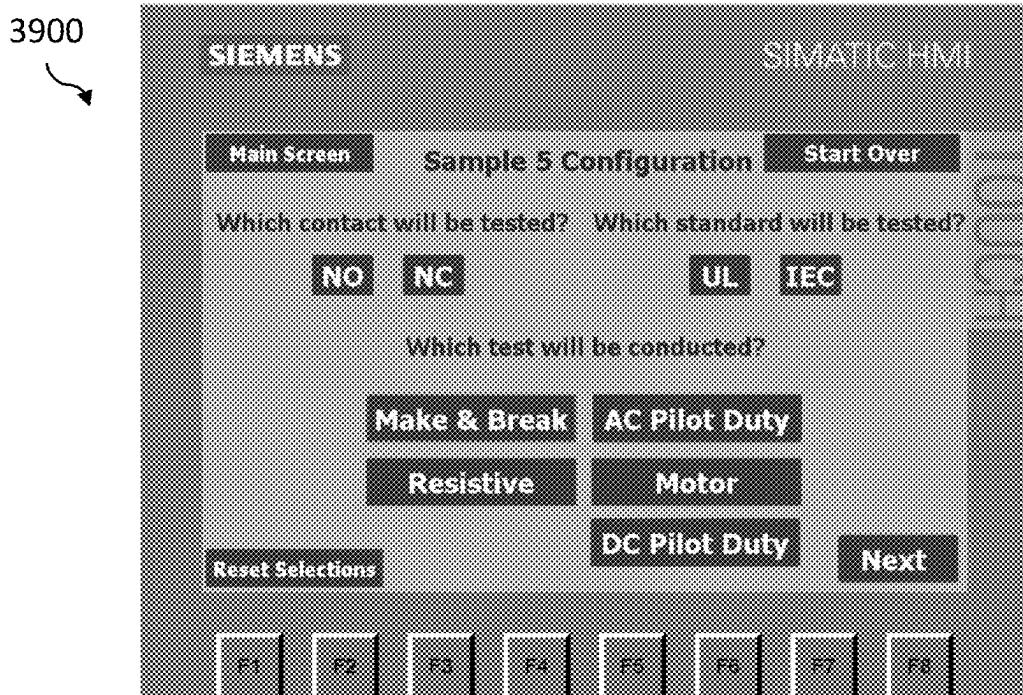


FIG. 40

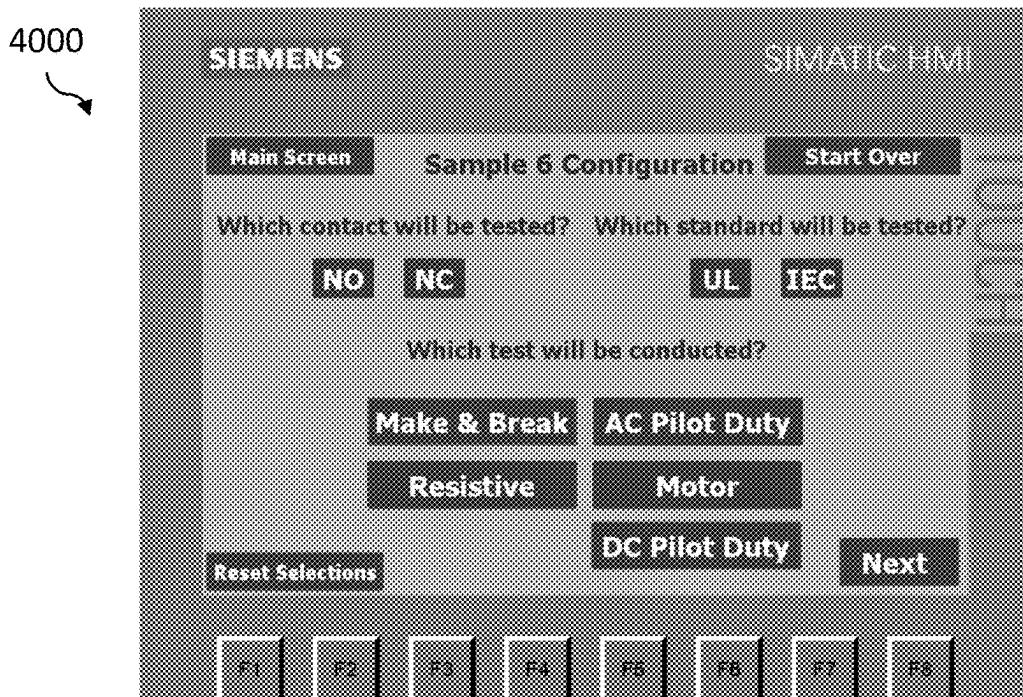


FIG. 41

4100

Sample	Test Type	Single Throw		Start Over		
		STD	NC/NO	Count	Oven	Temp
Sample 1	Make & Break	UL	NO	100000	Oven 1	+0.0
Sample 2	AC Pilot Duty	UL	NO	100000	Oven 1	+0.0
Sample 3	Resistive	UL	NC	100000	Oven 1	+0.0
Sample 4	Meter	UL	NC	100000	Oven 1	+0.0
Sample 5	AC Pilot Duty	UL	NC	100000	Oven 1	+0.0
Sample 6	Resistive	UL	NO	100000	Oven 1	+0.0

If configuration is correct press Next to continue
If configuration is not correct press Reconfigure to modify settings

Reconfigure **Next**

Function keys: F1, F2, F3, F4, F5, F6, F7, F8

FIG. 42

4200

Main Screen		Samples 4-6	
Sample 1	Count	Sample 2	Count
0		0	
% Complete		% Complete	
0.0		0.0	
Oven	OFF	Oven	OFF
Oven Temp	0.0	Oven Temp	0.0

Function keys: F1, F2, F3, F4, F5, F6, F7, F8

FIG. 43

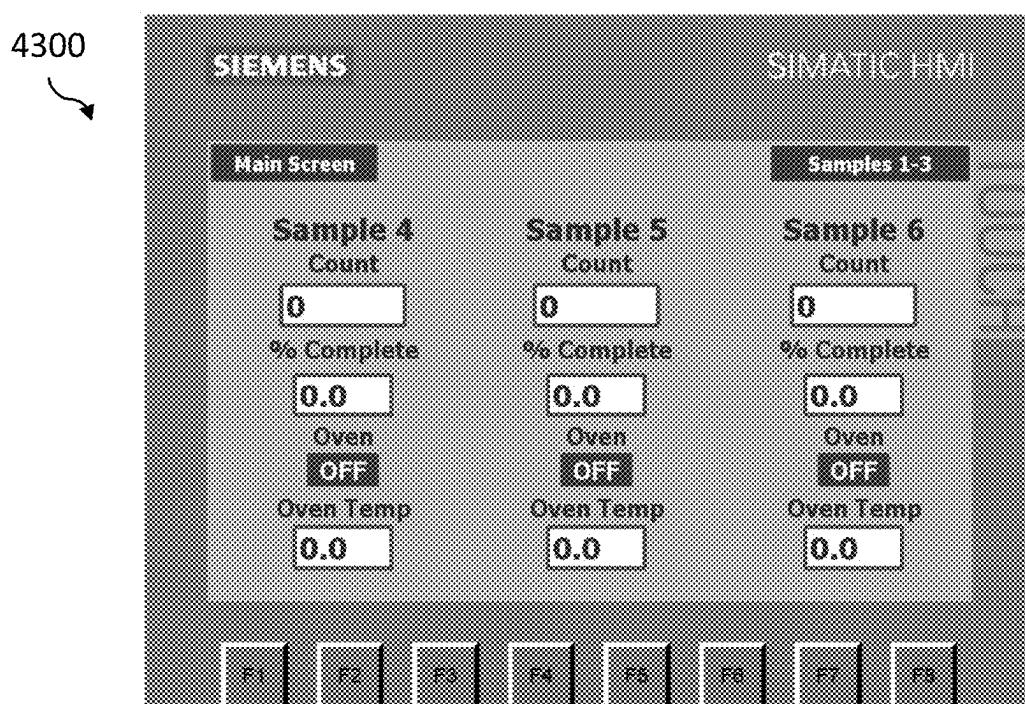


FIG. 44

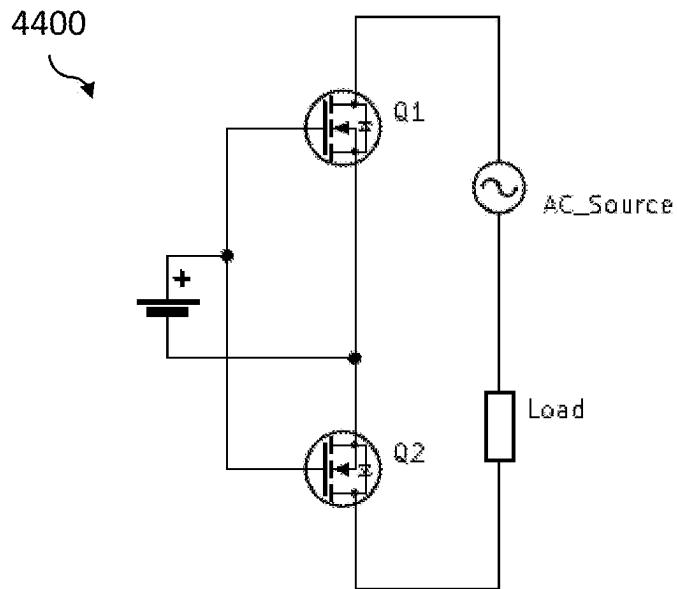


FIG. 45

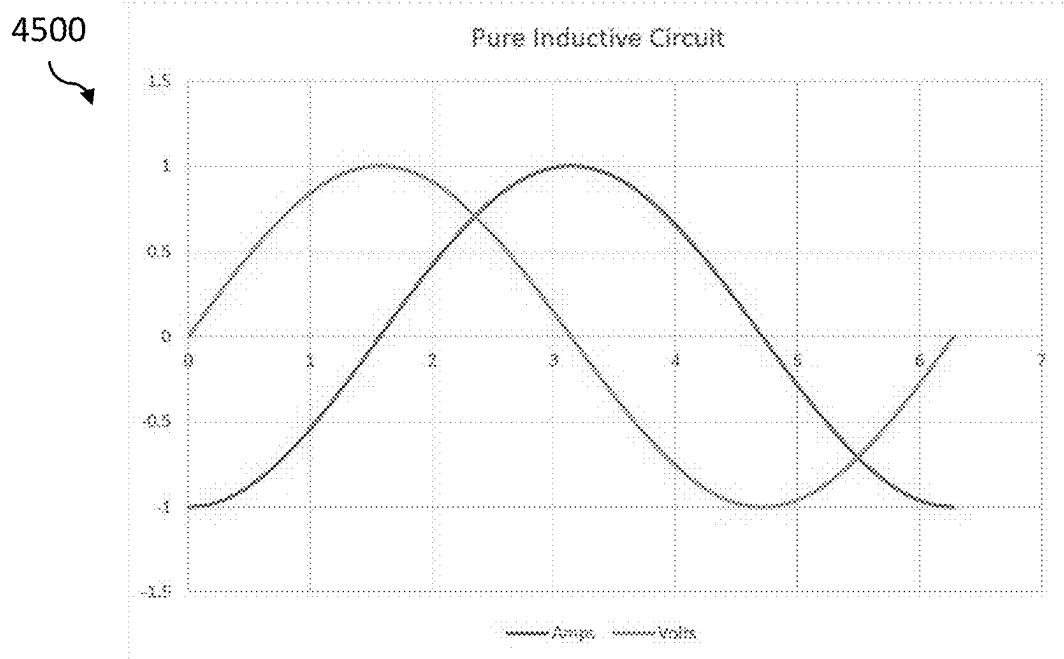
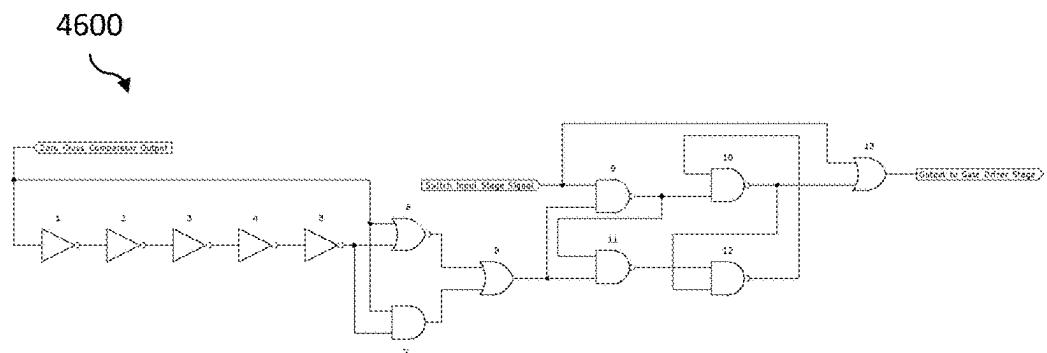


FIG. 46



4700

FIG. 47

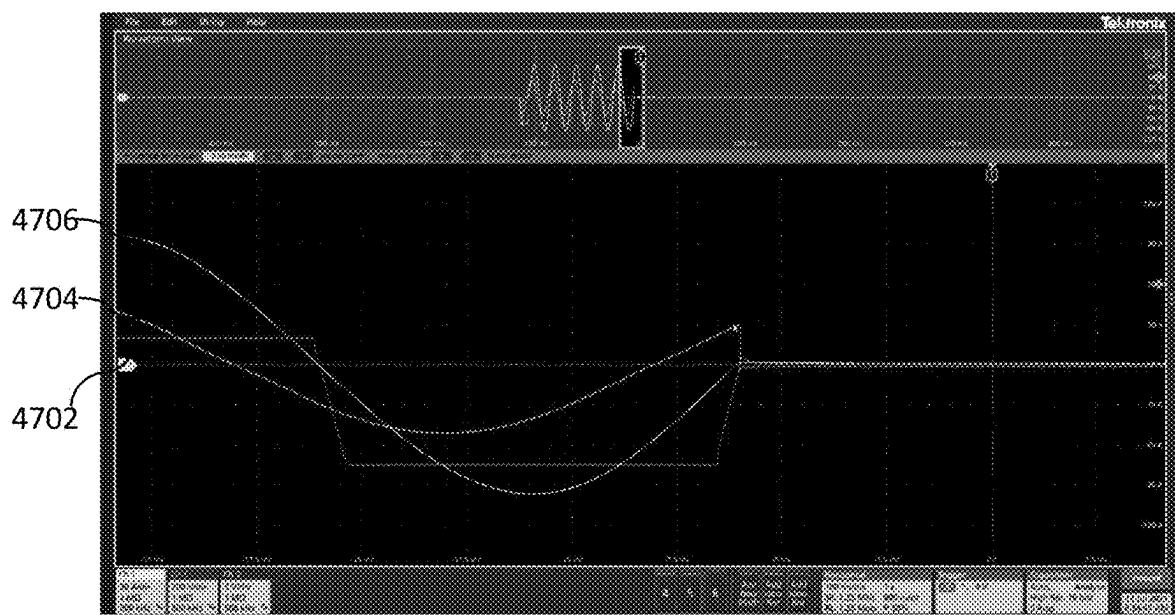


FIG. 48

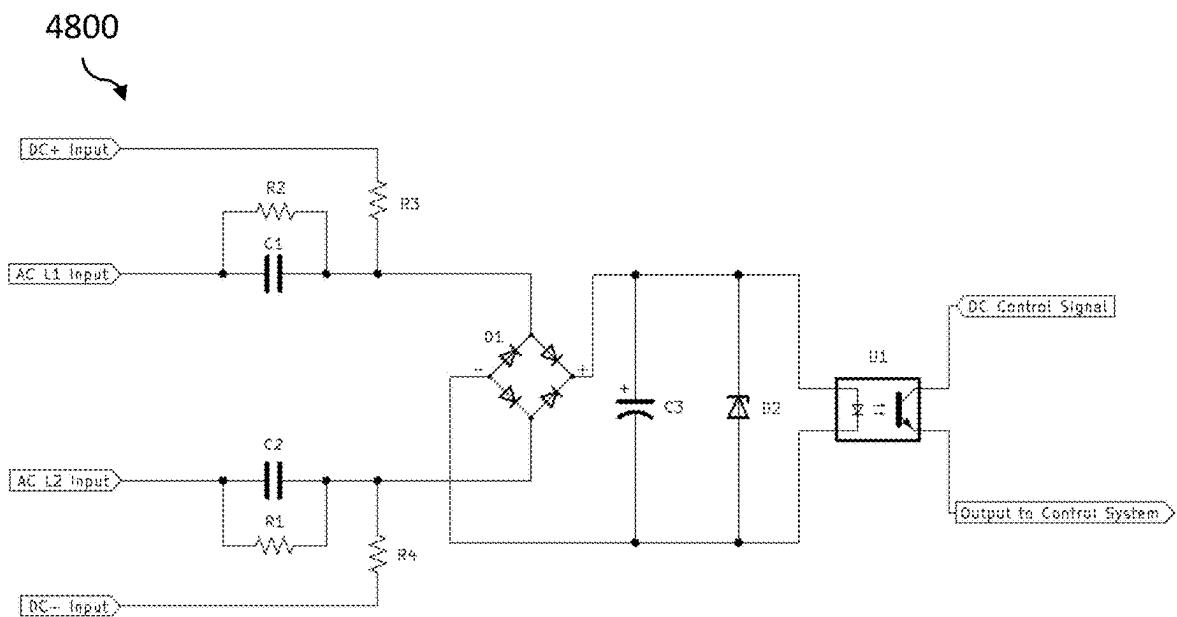
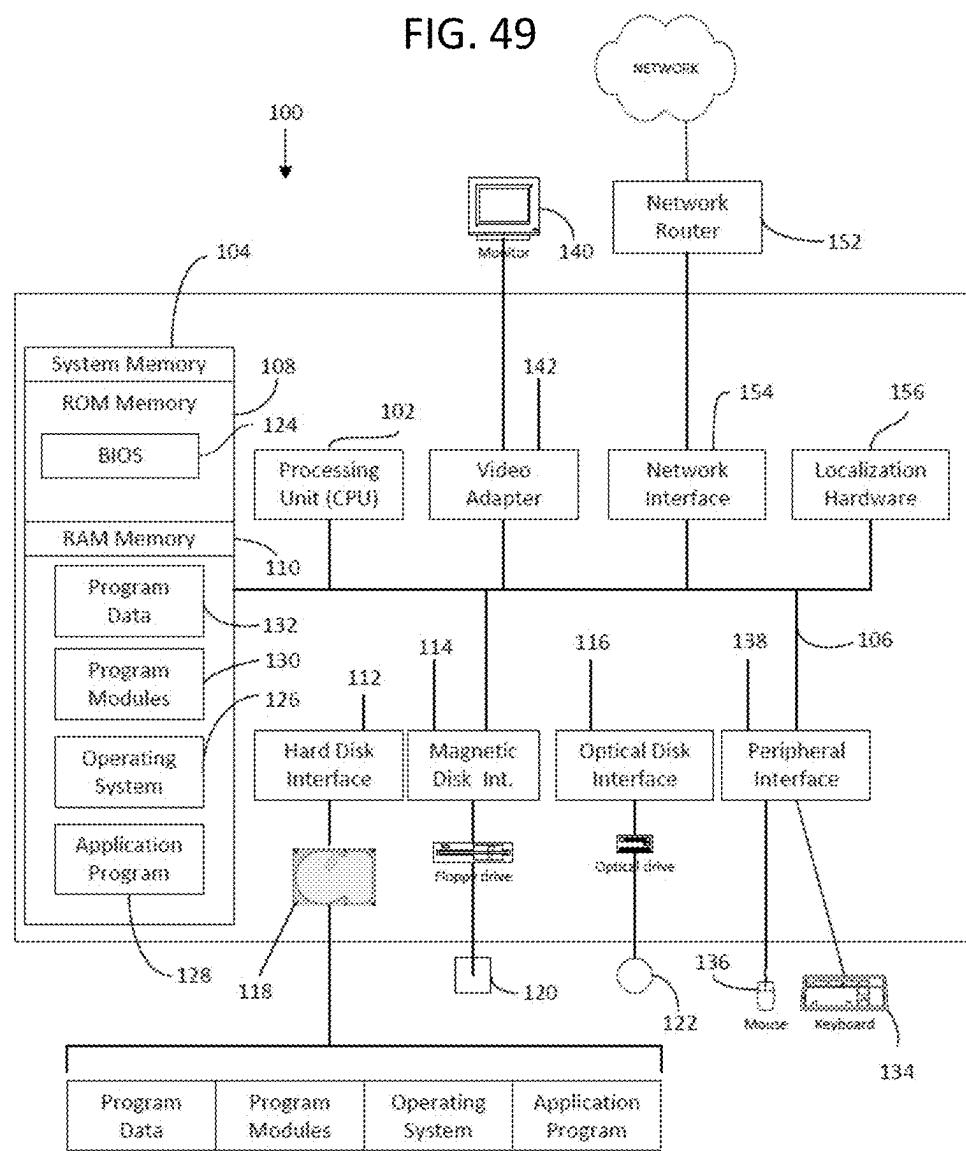


FIG. 49



SYSTEMS AND METHODS FOR PARALLEL ELECTRICAL ENDURANCE TESTING OF CONTACTS

BACKGROUND

[0001] As a part of product safety testing and certification, electrical relays and switches may be evaluated to prove their performance safely in normal use through endurance testing. Such electrical endurance testing may be used to stress a given product to its maximum rated electrical, thermal, and/or mechanical limits through, for example, on-off cycling.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] FIG. 1 is a diagrammatic view of an example enclosure in which an electrical device may be tested, in embodiments.

[0003] FIG. 2 is a diagrammatic view of an electrical component that may be tested, in embodiments.

[0004] FIG. 3 is a diagrammatic view of another electrical component that may be tested, in embodiments.

[0005] FIGS. 4 and 6-8 are schematic wiring diagrams of example testing apparatuses in various states, in embodiments.

[0006] FIGS. 9-43 are diagrammatic views of example graphical user interfaces for using an example testing apparatus, in embodiments.

[0007] FIG. 44 is a schematic view of a SiC switch having two MOSFETs with a common source connection, in embodiments.

[0008] FIG. 45 is a diagrammatic view of a voltage and current waveform for an example SiC switch, in embodiments.

[0009] FIG. 46 is a schematic view of digital logic for implementing a zero-crossing current circuit, in embodiments.

[0010] FIG. 47 is a diagrammatic view of waveforms demonstrating implementation of a zero-crossing current circuit, in embodiments.

[0011] FIG. 48 is a schematic view of a universal voltage board for sensing both alternating current (AC) and direct current (DC) voltages, in embodiments.

[0012] FIG. 49 is a diagrammatic view of an example of a computing environment, in embodiments.

DETAILED DESCRIPTION

[0013] The following disclosure of example apparatuses, methods, and computer-readable media is not intended to limit the scope of the detailed description to the precise form or forms detailed herein. Instead, the disclosure herein is intended to be illustrative so that others may follow its teachings.

[0014] As a part of product safety testing and certification, relays and switches may be evaluated to prove their performance safely in normal use through endurance testing. Such electrical endurance testing may be designed to stress the product to its maximum rated electrical, thermal, and mechanical limits through on-off cycling of the relays and/or switches. For example, testing may be performed according to Underwriters Laboratories (UL) or International Electrotechnical Commission (IEC) standard 60730-1. However, the various embodiments described herein may be used in conjunction with or for other types of tests or test standards.

The testing may be broken down into two electrical tests: an overload test and an endurance test. The overload test may run the product through a certain percentage over a maximum rating for a short period of time. The endurance test may run the product through its maximum rating for a long period of time. Previous tests of a single switch or relay may take, for example, over one month to complete.

[0015] As such, this type of testing may use a large amount of lab equipment and lab footprint to accomplish. As the testing required increases with more ratings, models, samples, etc. the testing time can further increase significantly. Various embodiments described herein are configured to mitigate/eliminate these problems and provide a reduction in testing time per sample, laboratory footprint, equipment used, etc., all while providing more flexibility for testing more samples than previous test equipment, testing different types of samples at the same time, and/or the ability to perform different types of tests using the same test equipment as described herein in various embodiments.

[0016] Using the apparatuses, methods, and computer-readable media described herein, one example embodiment may be used to perform an overload test on a relay or switch with 50 cycles of overload at a rate of 1 second on and 9 seconds off and perform an endurance test on a relay or switch with 100,000 cycles of endurance load at a rate of 5 seconds on 5 seconds off. Given such an example cycle rate, testing using the embodiments herein may, for example, take approximately 12 days to complete testing on a relay/switch samples.

[0017] As such, described herein are various apparatuses, methods, and computer-readable media for reducing the amount of time it takes to test such relays or switches by, for example, testing multiple (e.g., 3, 6) relays/switches at the same time with a single device. The apparatuses, methods, and computer-readable media described herein may also reduce the overall electric loads used to test the relays/switches, thereby reducing the cost and amount of electricity needed to run the tests. The various embodiments herein may also advantageously be used to test multiple different samples (sample relays or switches may be referred to herein merely as a sample or samples) that are tested to different ratings at the same time. That is, different types of samples that may be different and therefore are subject to different tests, may also be simultaneously tested using the embodiments described herein.

[0018] Components used to conduct this testing may include a control system, controller, or processor to turn the sample(s) on and off (e.g., a small programmable logic controller or PLC); an oven or other heat source for providing a desired or predetermined amount of heat in which to test the samples; electrical loads capable of providing the required or desired predetermined power levels for long durations; a transformer or variable autotransformer (e.g., Variac™ transformers) to adjust electrical mains voltage; and a mains power configured to provide a desired or predetermined amount of power sufficient to run desired tests for the samples.

[0019] The various embodiments described herein therefore provide for test fixtures capable of various methods of parallel electrical endurance testing of relays and/or switch contacts. A section of sequencing relays in the various test fixtures described herein may advantageously allow electrical power to be multiplexed to the appropriate loads for a given sample. The multiplexing may be achieved using

relays, which may also be referred to herein as backfeeds. These backfeed relays may prevent current from flowing in an unwanted direction (e.g., back to a power source of a test fixture through another test sample). For example, the backfeed relays may prevent current from flowing in an unwanted direction as the load current is connected through a normally open contact of a backfeed relay. In various embodiments the backfeed relays may be used for current carrying and not used for breaking any load. The multiplexing may also provide a way to reduce a total number of loads used to test multiple samples through load sharing, as further discussed herein.

[0020] FIG. 1 illustrates an example enclosure 160 in which an electrical device (e.g., sample, device under test (DUT)) may be tested. The example enclosure may include a user interface 170, which may also be referred to herein as a human machine interface (HMI). A door 180 may open so that the inside may be accessed for servicing. The enclosure 160 may further include electrical equipment, such as that shown in any one of or any combination of FIGS. 4 and 5-8. FIG. 2 illustrates an electrical component 200 (e.g., sample, device under test (DUT)) that may be tested in an external oven/environmental chamber. The electrical component 200 is a switch and demonstrates how the switch may be connected to a load when in a typical use. FIG. 3 illustrates another electrical component 300 similar to that of FIG. 2, and shows a typical setup of how that switch may be tested in various embodiments with Make and Break loads.

[0021] In an example embodiment, the sequencing of testing multiple DUTs in various embodiments described herein is divided up into six identical sections that may be configured in multiple ways to accommodate different sample configurations and test types to perform. This allows the flexibility of testing multiple samples to the same electrical rating, or multiple samples to different electrical ratings. Connections may be made with terminal block jumpers on the rear panel. This example test fixture may therefore advantageously perform testing on the following contact configurations at the same time, and may be either the same type or combinations of different types at once:

- [0022] 1. One, two, or three double throw switches
- [0023] 2. One, two, three, four, five, or six single throw switches of either normally open (NO)
- [0024] or normally closed (NC)
- [0025] 3. One double pole double throw switch
- [0026] 4. Two double pole single throw switches of either NO or NC
- [0027] 5. One three phase double throw switch
- [0028] 6. Two three phase single throw switches of either NO or NC

Input Sensing

[0029] The input sensing to a controller such as a PLC may be accomplished through specially designed universal voltage sensing circuit boards. These boards may sense a wide range of alternating current (AC) and direct current (DC) voltages and provide a constant 24 volts DC (VDC) output to digital inputs of a controller or PLC. The response time of these boards may be on the order of microseconds (μs). This may provide a controller with a very fast response to a closure of a contact/sample under test. The controller may therefore be used to set test sequence control, counting, on time duration, and/or off time duration. A separate

universal voltage board may be used to measure the make inrush current time of each contact.

[0030] In various embodiments, there may be current sensing switches that are on each break line. These provide the ability to count when load sharing with a resistive or motor test as the load voltage may never drop low enough to indicate a change in state.

Timing

[0031] For accurate timing throughout the duration of the test a special watchdog timer may be used. This prevents timing drift in the controller or PLC scan rate. This timer may be driven from a PLC internal 10 Hertz (Hz) asynchronous clock. Every positive rising edge of the 10 Hz clock increases a counter block up by one count. The programmed value of the counter may be set to 100 counts. Given the period of a 10 Hz signal is 100 milliseconds (ms) multiplied by the 100 counts gives a total duration of ten seconds with 100 ms steps. Once the counter reaches 100 counts the output changes states and uses an internal memory bit to reset the counter back to zero. Due to the asynchronous nature of the 10 Hz clock this timing may not be affected by the PLC scan rate. The output count may then be used in the test sequence program blocks. Where count 1=100 ms, count 2=200 ms, etc., for example. The PLC outputs may then be set and reset in sequence with an equals comparator statement.

[0032] To adequately catch the short duration of the make load a PLC pulse train output (PTO) and high-speed counter input may be used. This provides accurate timing of the make load duration to conform with standard requirements. This may be handled through a PTO to DC circuit board. This board may include six DC to DC solid state relays (one for each contact and/or sample). The output of each make universal voltage input board may be connected to the DC input of a solid state relay (SSR). A SSR DC transistor output may be connected to a 10 kilohertz (kHz) 50% duty cycle pulse train output from the PLC. This may then be connected to a special high-speed counter input on the PLC. This may provide a tighter tolerance of time when the digital input is “on” or high. The high-speed counter PLC block may then convert the pulse counts to a time in milliseconds. This time may then be compared to check to make sure the value is within a predetermined or standard requirement.

Error Handling and Safety Shutdown

[0033] The PLC may also provide for supervisory control over process errors and safety shutdown errors. The PLC may be configured to monitor the on-time of each contact and/or sample. If this on-time exceeds a predetermined time an alarm may be triggered and output via a user interface. This alarm may also trigger integrated shutdown relays (e.g., relays 2, 10, and 18 of FIGS. 4 and 7 while testing double throws samples; relays 2, 7, 12, 17, 22, and 27 of FIGS. 6 and 8 while testing single throw samples). Each contact may be independently controlled so the shutdown of one sample does not affect the others while they continue to run.

Oven Control

[0034] For International Electrotechnical Commission (IEC) testing requirements, for example, the first 50% of test cycles are to be performed at room temperature, and the second 50% of test cycles are to be performed at a maximum

or minimum rated temperature. An integrated contactor and thermocouple PLC module may provide control over an external oven or environmental chamber. If more than one sample is being tested to the same temperature the PLC may control the system such that all samples have achieved the required 50% of test cycles before powering the oven (or before powering down the oven if heated cycles are performed first). If a sample has fallen behind (e.g., due to error) the PLC may stop testing the other samples at the 50% point and wait until the other sample(s) have caught up. Testing may also be halted while the oven/chamber reaches its set point (or cools down to a room temperature), and the temperature stabilizes. Then the PLC will restart the test to complete the remaining 50% of test cycles on all samples.

Test Background

[0035] In overload and/or endurance testing there may be four basic types of tests:

- [0036] 1. Make & Break
- [0037] 2. Pilot Duty AC or DC
- [0038] 3. Motor (locking rotor amps (LRA)/full load amps (FLA))
- [0039] 4. Resistive AC or DC

[0040] Each type of overload and/or endurance testing may have its own specific load ratings and requirements.

[0041] A Make & Break test is intended to simulate an AC motor load. The test starts with a “make” load current inrush for a time between 50 ms to 100 ms (standard requirement), then change-over to a “break” load. This is intended to simulate the contact under test to “make” the current inrush to start a motor, and “break” the steady state or running current of a motor. This make to break change-over is performed every contact cycle during a Make & Break test.

[0042] A Pilot Duty test is intended to simulate a moving armature load (e.g., a solenoid, a contactor). There is a 10x (ten times) current inrush and then change to a steady state current like a make & break test.

[0043] A Motor load test is intended to simulate a locked rotor amps (LRA) rating of a motor, and a full load amps (FLA) rating of a motor. The overload will be at the LRA current, and the endurance will be at the FLA current.

[0044] A Resistive test is intended to simulate a predominately resistive load like a heating element.

[0045] In various embodiments described herein, fixture sequencing for Make & Break and Pilot Duty testing may be grouped together in a same test block as they behave the same despite their rating differences. The same applies for Motor and Resistive tests, which may also be grouped together. As such, the embodiments described herein may be advantageously used and programmed to reduce the complexity of a system for performing these various tests on samples and may significantly simplify programming of a system for performing these various tests.

[0046] In addition, the Motor and Resistive test sequence may be or may utilize a same or similar logic as that used for testing a DC Resistive or Pilot Duty test.

Program Sequence Background

[0047] In various embodiments, non-transitory computer readable instructions stored on a memory and executed by a processor may be used to set up and control a testing apparatus. For example, where a PLC is used, its PLC program may be configured to have separate test sequence

blocks, and these blocks may be selected by a user making user selections during test setup on a human-machine interface (HMI) (e.g., a touchscreen or other display/interface in communication with a PLC or other controller/processor). In these blocks, control of the PLC outputs may be based on a mix of fixed timings and physical inputs. The fixed timings keep the sequencing synced between samples, and the physical inputs react to sample contact changes of state.

[0048] For double throw samples, for example, the normally closed (NC) contacts are already closed so the normally open (NO) contacts may be tested first on each sample. On the first cycle the sequence staggers the starting of each relay sample under test by three seconds. The staggering allows only one make current to happen at a time, thus allowing the use of only one make load instead of three separate loads. Because only one contact is carrying current at one time with a double throw sample this allows the break loads to be shared as one load. For example, Sample 1 is at time zero seconds, sample 2 is at time three seconds, and sample 3 is at time six seconds. FIG. 5 demonstrates oscilloscope waveforms that outlines this time sequence, the individual make events are shown as waveform 502 (channel 1). Sample 1 break current is shown as waveform 504 (channel 2), Sample 2 break current is shown as waveform 506 (channel 3), and Sample 3 break current is shown as waveform 508 (channel 4).

[0049] For Make & Break and Pilot Duty tests on a double throw sample when the DUT contact closes multiple things happen. First, the NO Break Backfeed turns on to provide a complete path to the Break load. At the rising edge of the DUT voltage input of the NO contact a timer in the PLC program is started to allow a delay from sample contact closure to the NO Make/Break relay turning on. In this example, the timer is programmed for 32 ms. This delay combined with the propagation delay within the PLC system as well as the propagation delay in the Make/Break relay itself to provide a make load duration of approximately 70 ms to 80 ms. This allows deviation plus or minus and still stay within standard requirements. On the falling edge of the DUT voltage input of the NC contact from the previous cycle both the NC Break Backfeed relay and NC Make/Break relay are reset. This is to make sure that the DUT contact breaks the load circuit and not a relay inside the test fixture.

[0050] For overload tests on double throw samples the contacts are tested separately with the NO contacts first, then the NC contacts are tested. There is logic in the PLC program (or other instructions executed by a processor) to automatically make this switch from NO contact testing to NC contact testing.

[0051] For overload and endurance tests on single throw samples the contacts are tested all at once. During test setup the user tells the program which samples are normally open and which samples are normally closed on the HMI screen. This adjusts which sequence the PLC uses to activate the samples.

Program Sequences

[0052] FIGS. 4 and 6-8 show different configurations of a test apparatus that may be used to test various types of DUTs/samples/switches as described herein. Although FIGS. 4 and 6-8 vary somewhat from one another, each of the setups shown in FIGS. 4 and 6-8 may be advantageously implemented using the same test apparatus. For example,

1 DUT (relay 3) is turned on to open the NC contact. This completes the contacts one second on time. On the falling edge of the contact DUT voltage input both Sample 1 Break Backfeed (relay 6) and Sample 1 Make/Break (relay 4) are turned off.

[0073] If Sample 2 is a NC contact at time 1500 ms Sample 2 DUT (relay 8) is turned on to open the NC contact. This is done before the device under test activates the load to allow a complete path to the Make load (load 35). At time 1600 ms Sample 2 Make Backfeed (relay 10) is turned on. At time 1700 ms one of two actions can happen depending on if the sample is NO or NC. If the sample is NO Sample 2 DUT (relay 8) turns on to close the NO contact. If the sample is NC, then Sample 2 DUT (relay 8) is turned off to close the NC contact. On the rising edge of the DUT contact voltage input Sample 2 Break Backfeed (relay 11) turns on. After the 32 ms delay from DUT contact voltage input Sample 2 Make/Break (relay 9) turns on to change-over from the Make load (load 35) to the Break load (load 32). To allow sufficient time for the make current duration Sample 2 Make Backfeed (relay 10) is turned off at time 2100 ms. At 2700 ms if the sample is NO then Sample 2 DUT (relay 8) is turned off to open the NO contact. If the sample is NC, then Sample 2 DUT (relay 8) is turned on to open the NC contact. This completes the contacts one second on time. On the falling edge of the contact DUT voltage input both Sample 2 Break Backfeed (relay 11) and Sample 2 Make/Break (relay 9) are turned off.

[0074] If Sample 3 is a NC contact at time 3000 ms Sample 3 DUT (relay 13) is turned on to open the NC contact. This is done before the device under test activates the load to allow a complete path to the Make load (load 35). At time 3100 ms Sample 3 Make Backfeed (relay 15) is turned on. At time 3200 ms one of two actions can happen depending on if the sample is NO or NC. If the sample is NO Sample 3 DUT (relay 13) turns on to close the NO contact. If the sample is NC, then Sample 3 DUT (relay 13) is turned off to close the NC contact. On the rising edge of the DUT contact voltage input Sample 3 Break Backfeed (relay 16) turns on. After the 32 ms delay from DUT contact voltage input Sample 3 Make/Break (relay 14) turns on to change-over from the Make load (load 35) to the Break load (load 33). To allow sufficient time for the make current duration Sample 3 Make Backfeed (relay 15) is turned off at time 3600 ms. At 4200 ms if the sample is NO then Sample 3 DUT (relay 13) is turned off to open the NO contact. If the sample is NC, then Sample 3 DUT (relay 13) is turned on to open the NC contact. This completes the contacts one second on time. On the falling edge of the contact DUT voltage input both Sample 3 Break Backfeed (relay 16) and Sample 3 Make/Break (relay 14) are turned off.

[0075] If Sample 4 is a NC contact at time 4500 ms Sample 4 DUT (relay 18) is turned on to open the NC contact. This is done before the device under test activates the load to allow a complete path to the Make load (load 35). At time 4600 ms Sample 4 Make Backfeed (relay 20) is turned on. At time 4700 ms one of two actions can happen depending on if the sample is NO or NC. If the sample is NO Sample 4 DUT (relay 18) turns on to close the NO contact. If the sample is NC, then Sample 4 DUT (relay 18) is turned off to close the NC contact. On the rising edge of the DUT contact voltage input Sample 4 Break Backfeed (relay 21) turns on. After the 32 ms delay from DUT contact voltage input Sample 4 Make/Break (relay 19) turns on to change-

over from the Make load (load 35) to the Break load (load 33). To allow sufficient time for the make current duration Sample 4 Make Backfeed (relay 20) is turned off at time 5100 ms. At 5700 ms if the sample is NO then Sample 4 DUT (relay 18) is turned off to open the NO contact. If the sample is NC, then Sample 4 DUT (relay 18) is turned on to open the NC contact. This completes the contacts one second on time. On the falling edge of the contact DUT voltage input both Sample 4 Break Backfeed (relay 21) and Sample 4 Make/Break (relay 19) are turned off.

[0076] If Sample 5 is a NC contact at time 6000 ms Sample 5 DUT (relay 23) is turned on to open the NC contact. This is done before the device under test activates the load to allow a complete path to the Make load (load 35). At time 6100 ms Sample 5 Make Backfeed (relay 25) is turned on. At time 6200 ms one of two actions can happen depending on if the sample is NO or NC. If the sample is NO Sample 5 DUT (relay 23) turns on to close the NO contact. If the sample is NC, then Sample 5 DUT (relay 23) is turned off to close the NC contact. On the rising edge of the DUT contact voltage input Sample 5 Break Backfeed (relay 26) turns on. After the 32 ms delay from DUT contact voltage input Sample 5 Make/Break (relay 24) turns on to change-over from the Make load (load 35) to the Break load (load 34). To allow sufficient time for the make current duration Sample 5 Make Backfeed (relay 25) is turned off at time 6600 ms. At 7200 ms if the sample is NO then Sample 5 DUT (relay 23) is turned off to open the NO contact. If the sample is NC, then Sample 5 DUT (relay 23) is turned on to open the NC contact. This completes the contacts one second on time. On the falling edge of the contact DUT voltage input both Sample 5 Break Backfeed (relay 26) and Sample 5 Make/Break (relay 24) are turned off.

[0077] If Sample 6 is a NC contact at time 7500 ms Sample 6 DUT (relay 28) is turned on to open the NC contact. This is done before the device under test activates the load to allow a complete path to the Make load (load 35). At time 7600 ms Sample 6 Make Backfeed (relay 30) is turned on. At time 7700 ms one of two actions can happen depending on if the sample is NO or NC. If the sample is NO Sample 6 DUT (relay 28) turns on to close the NO contact. If the sample is NC, then Sample 6 DUT (relay 28) is turned off to close the NC contact. On the rising edge of the DUT contact voltage input Sample 6 Break Backfeed (relay 31) turns on. After the 32 ms delay from DUT contact voltage input Sample 6 Make/Break (relay 29) turns on to change-over from the Make load (load 35) to the Break load (load 34). To allow sufficient time for the make current duration Sample 6 Make Backfeed (relay 30) is turned off at time 8100 ms. At 8700 ms if the sample is NO then Sample 6 DUT (relay 28) is turned off to open the NO contact. If the sample is NC, then Sample 6 DUT (relay 28) is turned on to open the NC contact. This completes the contacts one second on time. On the falling edge of the contact DUT voltage input both Sample 6 Break Backfeed (relay 31) and Sample 6 Make/Break (relay 29) are turned off.

[0078] The chronological order of operations for an AC Make & Break or Pilot Duty overload test on six single throw relay samples using the test apparatus of FIG. 6 is outlined below in Table 4. This sequence may be repeated as many times as desired or as called for to complete standard tests for given DUTs.

using an asynchronous timer that is not part of the ladder scanning of a PLC. Such an asynchronous timer may operate as a master clock signal that is used to control timing of the various switches described herein instead of timers built into the rungs of a PLC controller. For example, embodiments herein may use a timer that has a 10 Hz on/off cycle and any logic present in the rungs built using a PLC controller just refers back to that 10 Hz timer and count cycles to measure time instead of using logic that may use or operate separate timers.

[0155] In various embodiments, the systems and methods herein may also be implemented to test single and double throw switches at the same time. For example, the apparatus described above with respect to FIGS. 4 and 6-8 may be used to test one double throw and up to four single throw switches at the same time, up to two double throw switches and up to two single throw switches at the same time, etc. Various embodiments may also be capable of testing different numbers of switches, such as an embodiment that can test up to 6 double throw switches or up to 12 single throw switches, or an embodiment that can test up to 9 double throw switches or up to 18 single throw switches.

Example Computing Environment

[0156] FIG. 49 is a diagrammatic view of an example of a computing environment that includes a general-purpose computing system environment 100, such as a desktop computer, laptop, smartphone, tablet, or any other such device having the ability to execute instructions, such as those stored within a non-transient, computer-readable medium. Various computing devices as disclosed herein (e.g., a processor, controller, PLC, or any other computing device used to control or communicate with components of a test apparatus) may be similar to the computing system 100 or may include some components of the computing system 100. Furthermore, while described and illustrated in the context of a single computing system 100, those skilled in the art will also appreciate that the various tasks described hereinafter may be practiced in a distributed environment having multiple computing systems 100 linked via a local or wide-area network in which the executable instructions may be associated with and/or executed by one or more of multiple computing systems 100.

[0157] In its most basic configuration, computing system environment 100 typically includes at least one processing unit 102 and at least one memory 104, which may be linked via a bus 106. Depending on the exact configuration and type of computing system environment, memory 104 may be volatile (such as RAM 110), non-volatile (such as ROM 108, flash memory, etc.) or some combination of the two. Computing system environment 100 may have additional features and/or functionality. For example, computing system environment 100 may also include additional storage (removable and/or non-removable) including, but not limited to, magnetic or optical disks, tape drives and/or flash drives. Such additional memory devices may be made accessible to the computing system environment 100 by means of, for example, a hard disk drive interface 112, a magnetic disk drive interface 114, and/or an optical disk drive interface 116. As will be understood, these devices, which would be linked to the system bus 306, respectively, allow for reading from and writing to a hard disk 118, reading from or writing to a removable magnetic disk 120, and/or for reading from or writing to a removable optical

disk 122, such as a CD/DVD ROM or other optical media. The drive interfaces and their associated computer-readable media allow for the nonvolatile storage of computer readable instructions, data structures, program modules and other data for the computing system environment 100. Those skilled in the art will further appreciate that other types of computer readable media that can store data may be used for this same purpose. Examples of such media devices include, but are not limited to, magnetic cassettes, flash memory cards, digital videodisks, Bernoulli cartridges, random access memories, nano-drives, memory sticks, other read/write and/or read-only memories and/or any other method or technology for storage of information such as computer readable instructions, data structures, program modules or other data. Any such computer storage media may be part of computing system environment 100.

[0158] A number of program modules may be stored in one or more of the memory/media devices. For example, a basic input/output system (BIOS) 124, containing the basic routines that help to transfer information between elements within the computing system environment 100, such as during start-up, may be stored in ROM 108. Similarly, RAM 110, hard drive 118, and/or peripheral memory devices may be used to store computer executable instructions comprising an operating system 126, one or more applications programs 128 (which may include the functionality disclosed herein, for example), other program modules 130, and/or program data 122. Still further, computer-executable instructions may be downloaded to the computing environment 100 as needed, for example, via a network connection.

[0159] An end-user may enter commands and information into the computing system environment 100 through input devices such as a keyboard 134 and/or a pointing device 136. While not illustrated, other input devices may include a microphone, a joystick, a game pad, a scanner, etc. These and other input devices would typically be connected to the processing unit 102 by means of a peripheral interface 138 which, in turn, would be coupled to bus 106. Input devices may be directly or indirectly connected to processor 102 via interfaces such as, for example, a parallel port, game port, firewire, or a universal serial bus (USB). To view information from the computing system environment 100, a monitor 140 or other type of display device may also be connected to bus 106 via an interface, such as via video adapter 132. In addition to the monitor 140, the computing system environment 100 may also include other peripheral output devices, not shown, such as speakers and printers.

[0160] The computing system environment 100 may also utilize logical connections to one or more computing system environments. Communications between the computing system environment 100 and the remote computing system environment may be exchanged via a further processing device, such a network router 152, that is responsible for network routing. Communications with the network router 152 may be performed via a network interface component 154. Thus, within such a networked environment, e.g., the Internet, World Wide Web, LAN, or other like type of wired or wireless network, it will be appreciated that program modules depicted relative to the computing system environment 100, or portions thereof, may be stored in the memory storage device(s) of the computing system environment 100.

[0161] The computing system environment 100 may also include localization hardware 186 for determining a location of the computing system environment 100. In some

instances, the localization hardware 156 may include, for example only, a GPS antenna, an RFID chip or reader, a WiFi antenna, or other computing hardware that may be used to capture or transmit signals that may be used to determine the location of the computing system environment 100.

[0162] While this disclosure has described certain embodiments, it will be understood that the claims are not intended to be limited to these embodiments except as explicitly recited in the claims. On the contrary, the instant disclosure is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the disclosure. Furthermore, in the detailed description of the present disclosure, numerous specific details are set forth in order to provide a thorough understanding of the disclosed embodiments. However, it will be obvious to one of ordinary skill in the art that systems and methods consistent with this disclosure may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure various aspects of the present disclosure.

[0163] Some portions of the detailed descriptions of this disclosure have been presented in terms of procedures, logic blocks, processing, and other symbolic representations of operations on data bits within a computer or digital system memory. These descriptions and representations are the means used by those skilled in the data processing arts to most effectively convey the substance of their work to others skilled in the art. A procedure, logic block, process, etc., is herein, and generally, conceived to be a self-consistent sequence of steps or instructions leading to a desired result. The steps are those requiring physical manipulations of physical quantities. Usually, though not necessarily, these physical manipulations take the form of electrical or magnetic data capable of being stored, transferred, combined, compared, and otherwise manipulated in a computer system or similar electronic computing device. For reasons of convenience, and with reference to common usage, such data is referred to as bits, values, elements, symbols, characters, terms, numbers, or the like, with reference to various presently disclosed embodiments.

[0164] It should be borne in mind, however, that these terms are to be interpreted as referencing physical manipulations and quantities and are merely convenient labels that should be interpreted further in view of terms commonly used in the art. Unless specifically stated otherwise, as apparent from the discussion herein, it is understood that throughout discussions of the present embodiment, discussions utilizing terms such as "determining" or "outputting" or "transmitting" or "recording" or "locating" or "storing" or "displaying" or "receiving" or "recognizing" or "utilizing" or "generating" or "providing" or "accessing" or "checking" or "notifying" or "delivering" or the like, refer to the action and processes of a computer system, or similar electronic computing device, that manipulates and transforms data. The data is represented as physical (electronic) quantities within the computer system's registers and memories and is transformed into other data similarly represented as physical quantities within the computer system memories or registers, or other such information storage, transmission, or display devices as described herein or otherwise understood to one of ordinary skill in the art.

[0165] Although certain example methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus, and articles of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.

What is claimed is:

1. An apparatus for testing a plurality of electrical switches comprising:
 - first contacts configured to connect to a first sample switch of the plurality of electrical switches, wherein the first contacts comprise at least a first input contact and a first output contact;
 - second contacts configured to connect to a second sample switch of the plurality of electrical switches, wherein the second contacts comprise at least a second input contact and a second output contact;
 - a power source connected to the first input contact and the second input contact;
 - at least one first switch connected to the first output contact, the at least one first switch configured to selectively connect the first sample switch to a first make load;
 - at least one second switch connected to the first output contact, the at least one second switch configured to selectively connect the first sample switch to a first break load;
 - at least one third switch connected to the second output contact, the at least one third switch configured to selectively connect the second sample switch to a second make load; and
 - at least one fourth switch connected to the second output contact, the at least one fourth switch configured to selectively connect the second sample switch to a second break load.
2. The apparatus of claim 1, wherein the first make load and the second make load are a same make load.
3. The apparatus of claim 1, wherein the first break load and the second break load are a same break load.
4. The apparatus of claim 1, wherein the first sample switch and the second sample switch are each a double throw switch.
5. The apparatus of claim 1, wherein the first sample switch and the second sample switch are each a single throw switch.
 6. The apparatus of claim 5, wherein:
 - the first sample switch and the second sample switch are each a single throw normally open switch;
 - the first sample switch and the second sample switch are each a single throw normally closed switch;
 - the first sample switch is a single throw normally open switch and the second sample switch is a single throw normally closed switch; or
 - the first sample switch is a single throw normally closed switch and the second sample switch is a single throw normally open switch.
 7. The apparatus of claim 1, further comprising third contacts configured to connect to a third sample switch of the plurality of electrical switches.
 8. The apparatus of claim 1, further comprising a safety switch connected between the power source and the first input contact.
 9. The apparatus of claim 1, wherein the at least one first switch comprises two MOSFETs configured to have a

common source, wherein the at least one first switch allows current to flow in two directions in an on state and blocks current in both positive and negative directions in an off state.

10. The apparatus of claim **9**, wherein the two MOSFETs are comprised of silicon carbide.

11. The apparatus of claim **9**, wherein the at least one first switch further comprises a zero-crossing current sensor, wherein the at least one first switch is turned off only when the current output by the at least one first switch is at or near zero current.

12. The apparatus of claim **1**, further comprising a universal voltage sensing circuit configured to sense alternating current (AC) voltage or direct current (DC) voltage, wherein the universal voltage sensing circuit is connected to the first output contact of the first sample switch.

13. The apparatus of claim **12**, wherein an output of the universal voltage sensing circuit is connected to a controller of the apparatus, wherein the controller is configured to determine a cycle of a test of the first sample switch based on the output of the universal voltage sensing circuit.

14. A method for testing a plurality of electrical switches comprising:

connecting, by a controller of an electrical switch testing apparatus, a first sample switch of the plurality of electrical switches to a make load;

disconnecting, by the controller at a first predetermined time after the first sample switch is connected to the make load, the first sample switch from the make load;

connecting, by the controller at a second predetermined time after the first sample switch is connected to the make load, the first sample switch to a break load; and

connecting, by the controller at a third predetermined time after the first sample switch is connected to the make load, a second switch of the plurality of electrical switches to the make load.

15. The method of claim **14**, further comprising disconnecting, by the controller at a fourth predetermined time after the first sample switch is connected to the make load, the second sample switch from the make load.

16. The method of claim **15**, further comprising connecting, by the controller at a fifth predetermined time after the first sample switch is connected to the make load, the second sample switch to the break load.

17. The method of claim **16**, further comprising connecting, by the controller at a sixth predetermined time after the first sample switch is connected to the make load, a third sample switch of the plurality of electrical switches to the make load.

18. The method of claim **17**, further comprising: disconnecting, by the controller at a seventh predetermined time after the first sample switch is connected to the make load, the third sample switch from the make load; and

connecting, by the controller at an eighth predetermined time after the first sample switch is connected to the make load, the third sample switch to the break load.

19. The method of claim **14**, further comprising determining, by the controller, that the first predetermined time after the first sample switch is connected to the make load has elapsed based a timer count based on an internal asynchronous clock signal of the controller.

20. An apparatus for testing a plurality of electrical switches comprising:

first contacts configured to connect to a first sample switch of the plurality of electrical switches, wherein the first contacts comprise at least a first input contact and a first output contact, and wherein the first sample switch is one of a double throw switch, a single throw normally open switch, or a single throw normally closed switch;

second contacts configured to connect to a second sample switch of the plurality of electrical switches, wherein the second contacts comprise at least a second input contact and a second output contact, and wherein the second sample switch is one of a double throw switch, a single throw normally open switch, or a single throw normally closed switch;

at least one first switch connected to the first output contact, the at least one first switch configured to selectively connect the first sample switch to a first make load;

at least one second switch connected to the first output contact, the at least one second switch configured to selectively connect the first sample switch to a first break load;

at least one third switch connected to the second output contact, the at least one third switch configured to selectively connect the second sample switch to a second make load; and

at least one fourth switch connected to the second output contact, the at least one fourth switch configured to selectively connect the second sample switch to a second break load.

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