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(54) **STRUCTURE AND METHOD FOR A LOW-K DIELECTRIC WITH PILLAR-TYPE AIR-GAPS**

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(21) Appl. No.: **19/086,402**

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Related U.S. Application Data

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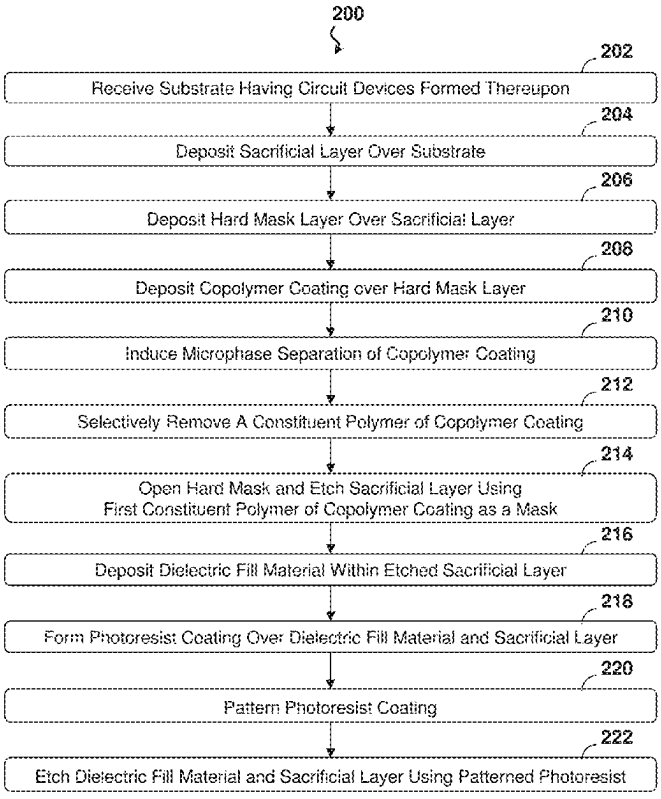
H01L 23/522	(2006.01)
H01L 23/528	(2006.01)
H01L 23/532	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 23/535*** (2013.01); ***H01L 21/31144*** (2013.01); ***H01L 21/7682*** (2013.01); ***H01L 23/5222*** (2013.01); ***H01L 23/528*** (2013.01); ***H01L 23/5329*** (2013.01); ***H01L 23/53295*** (2013.01); *H01L 21/76807* (2013.01); *H01L 21/76885* (2013.01); *H01L 23/485* (2013.01); *H01L 2924/0002* (2013.01)

(57) **ABSTRACT**

A circuit device having an interlayer dielectric with pillar-type air gaps and a method of forming the circuit device are disclosed. In an exemplary embodiment, the method comprises receiving a substrate and depositing a first layer over the substrate. A copolymer layer that includes a first constituent polymer and a second constituent polymer is formed over the first layer. The first constituent polymer is selectively removed from the copolymer layer. A first region of the first layer corresponding to the selectively removed first constituent polymer is etched. The etching leaves a second region of the first layer underlying the second constituent polymer unetched. A metallization process is performed on the etched substrate, and the first layer is removed from the second region to form an air gap. The method may further comprise depositing a dielectric material within the etched first region.



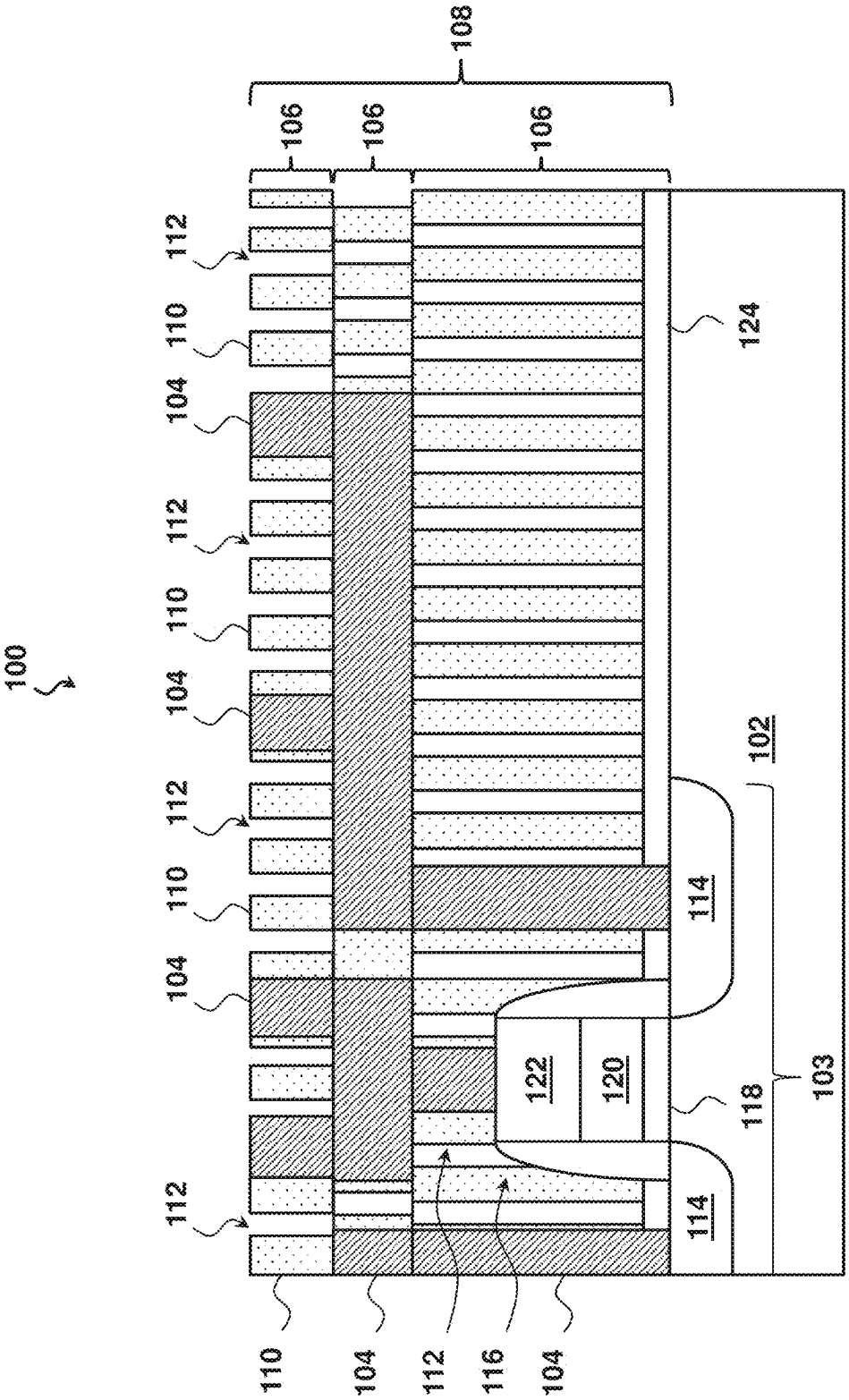

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Fig. 1

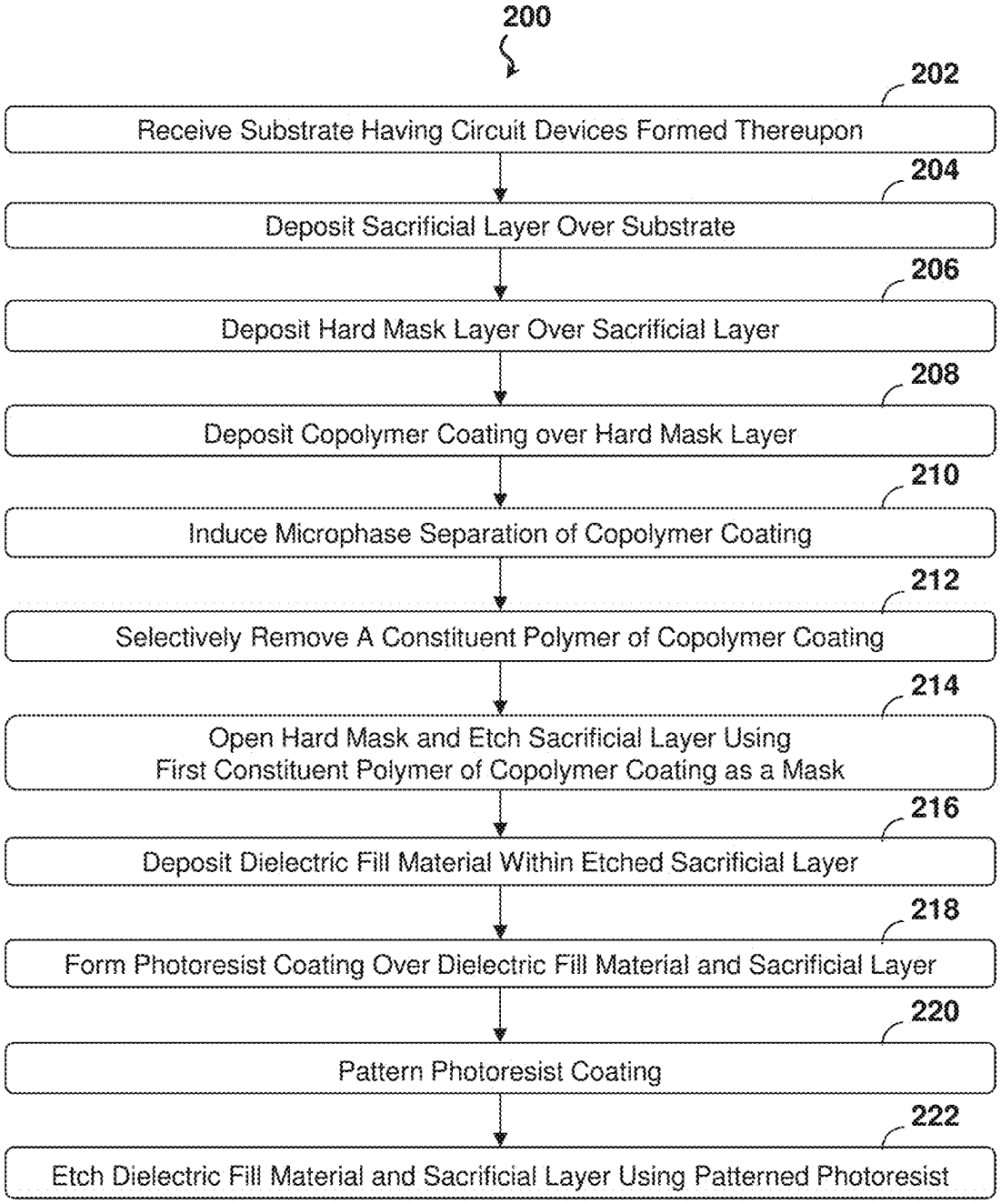

200
202
Receive Substrate Having Circuit Devices Formed Thereupon
204
Deposit Sacrificial Layer Over Substrate
206
Deposit Hard Mask Layer Over Sacrificial Layer
208
Deposit Copolymer Coating over Hard Mask Layer
210
Induce Microphase Separation of Copolymer Coating
212
Selectively Remove A Constituent Polymer of Copolymer Coating
214
Open Hard Mask and Etch Sacrificial Layer Using First Constituent Polymer of Copolymer Coating as a Mask
216
Deposit Dielectric Fill Material Within Etched Sacrificial Layer
218
Form Photoresist Coating Over Dielectric Fill Material and Sacrificial Layer
220
Pattern Photoresist Coating
222
Etch Dielectric Fill Material and Sacrificial Layer Using Patterned Photoresist

Fig. 2A

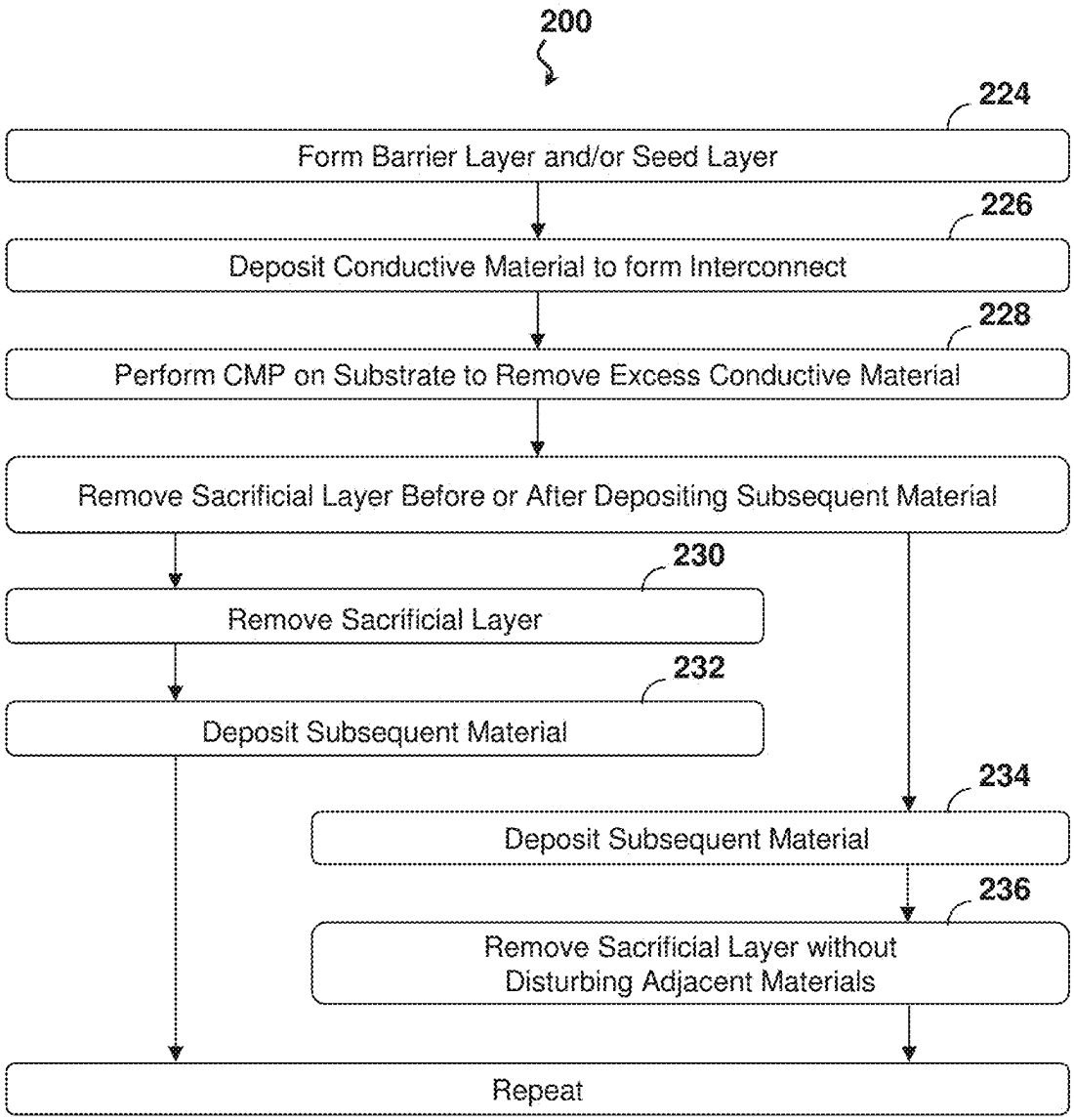

200
224
Form Barrier Layer and/or Seed Layer
226
Deposit Conductive Material to form Interconnect
228
Perform CMP on Substrate to Remove Excess Conductive Material
Remove Sacrificial Layer Before or After Depositing Subsequent Material
230
Remove Sacrificial Layer
232
Deposit Subsequent Material
234
Deposit Subsequent Material
236
Remove Sacrificial Layer without Disturbing Adjacent Materials
Repeat

Fig. 2B

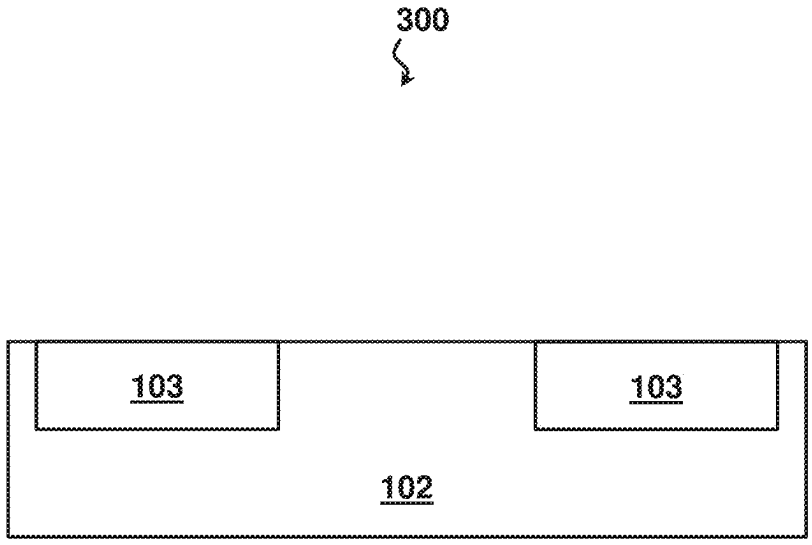
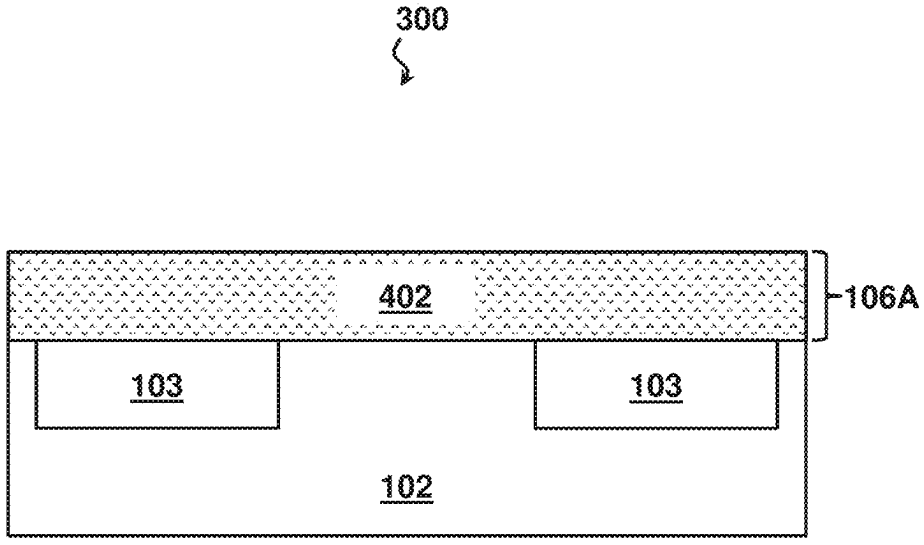


Fig. 3



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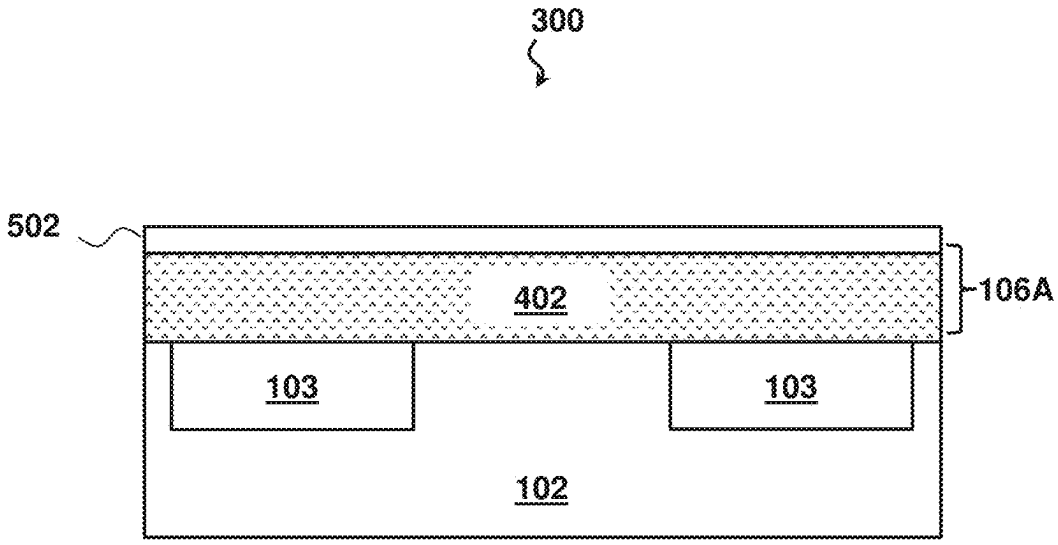

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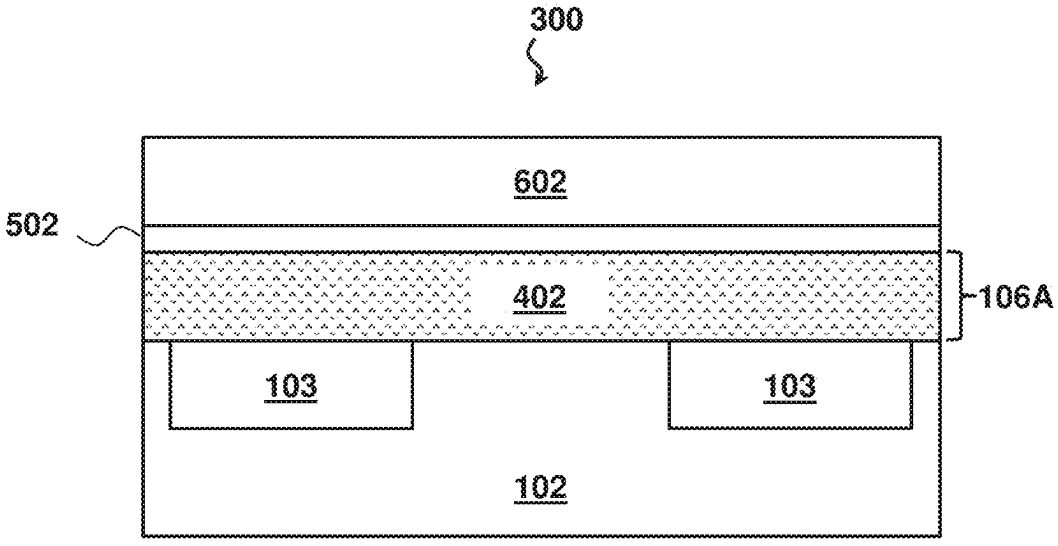
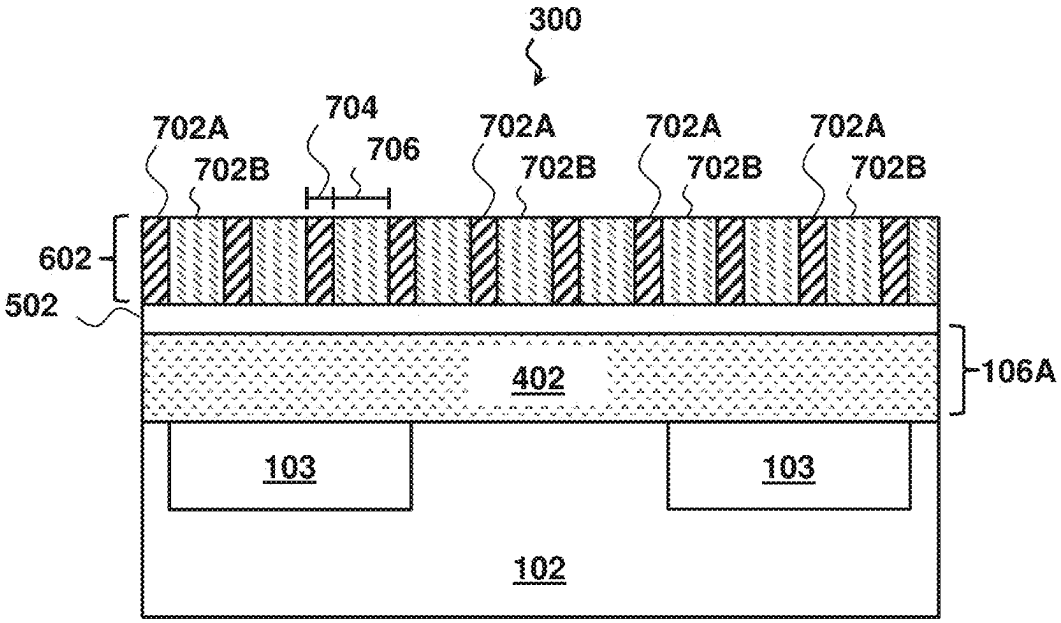


Fig. 6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702B
702B
702B
602
502
402
106A
103
103
102

Fig. 7

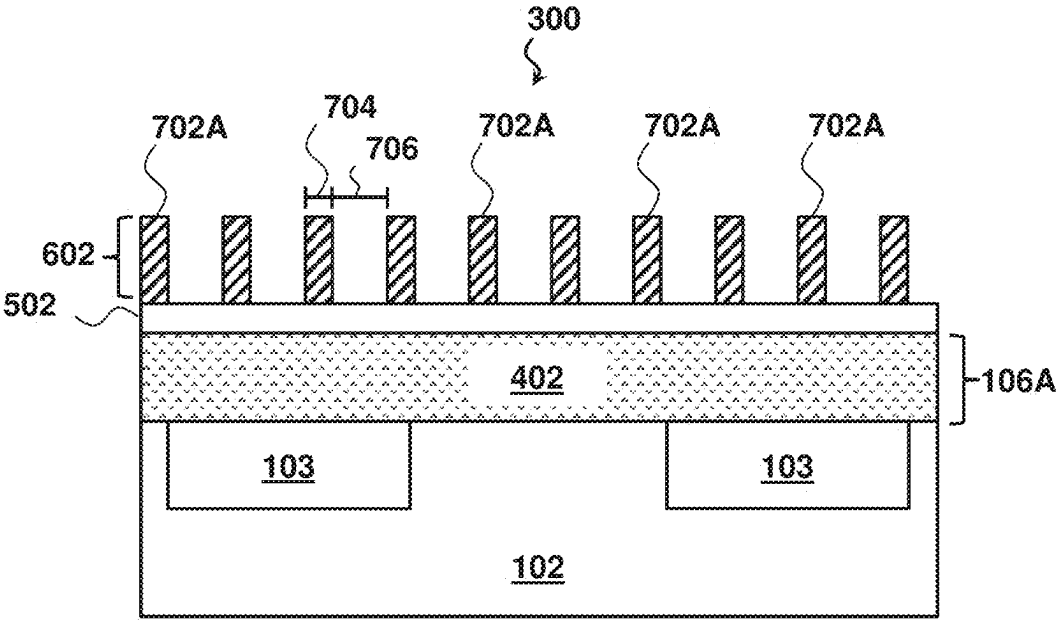
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Fig. 8

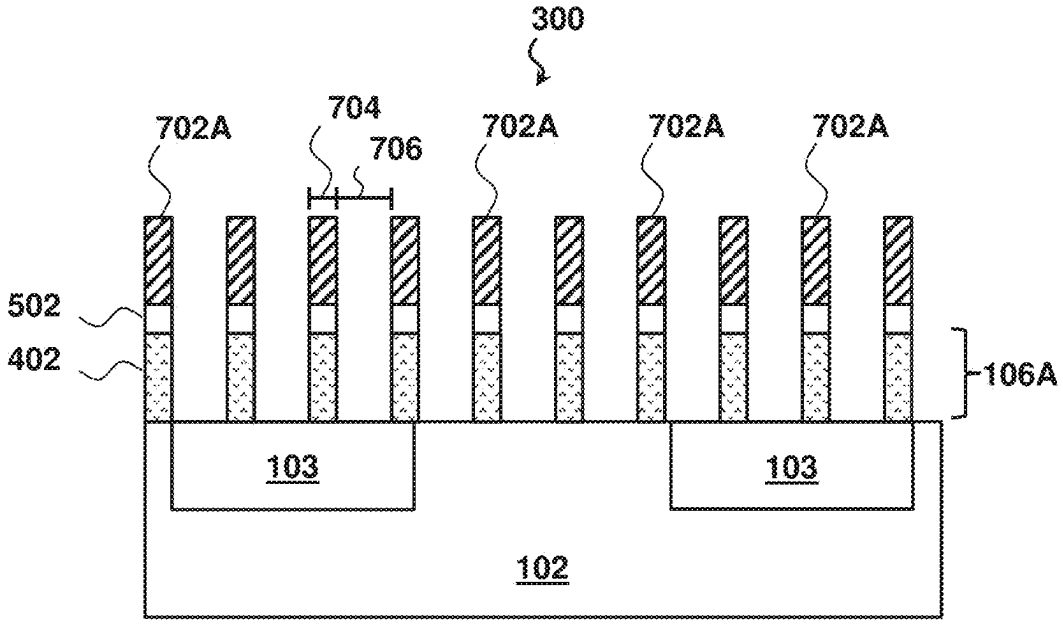
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Fig. 9

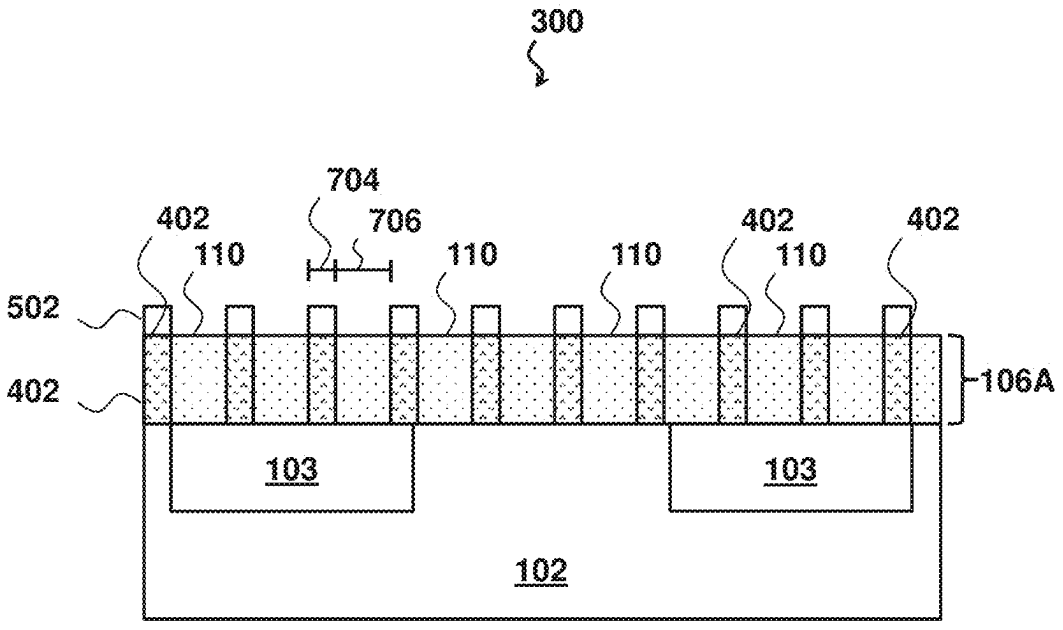
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Fig. 10

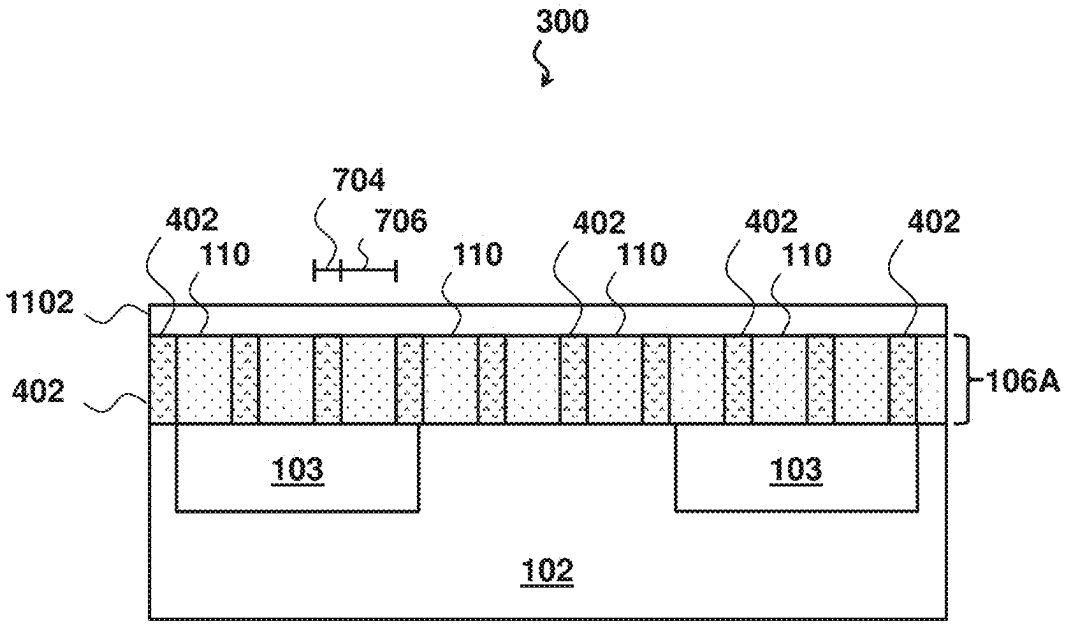
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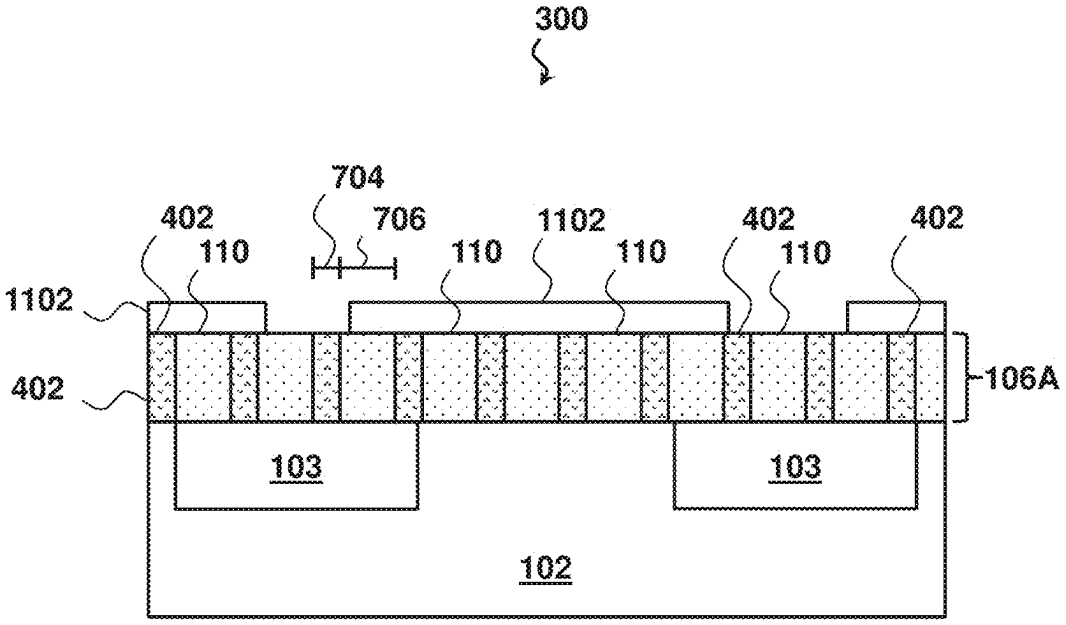
Fig. 11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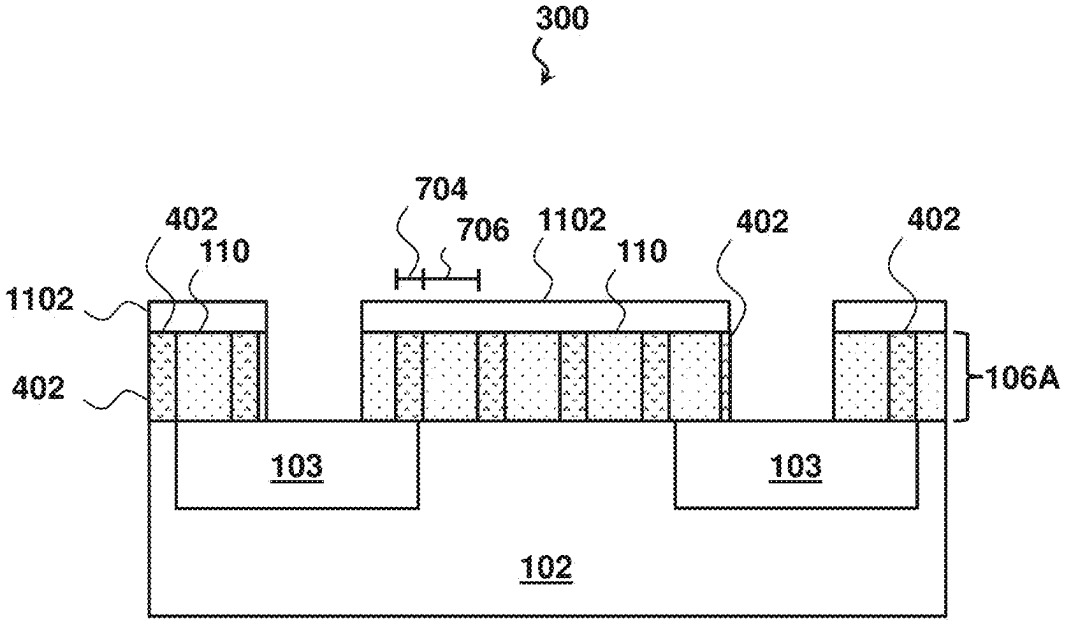
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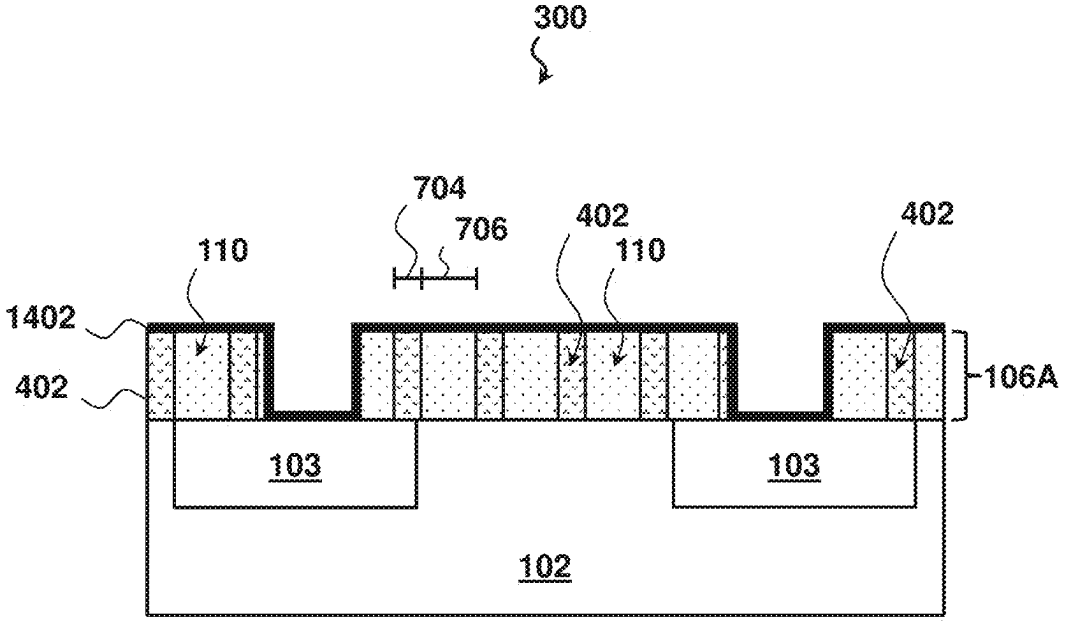
Fig. 13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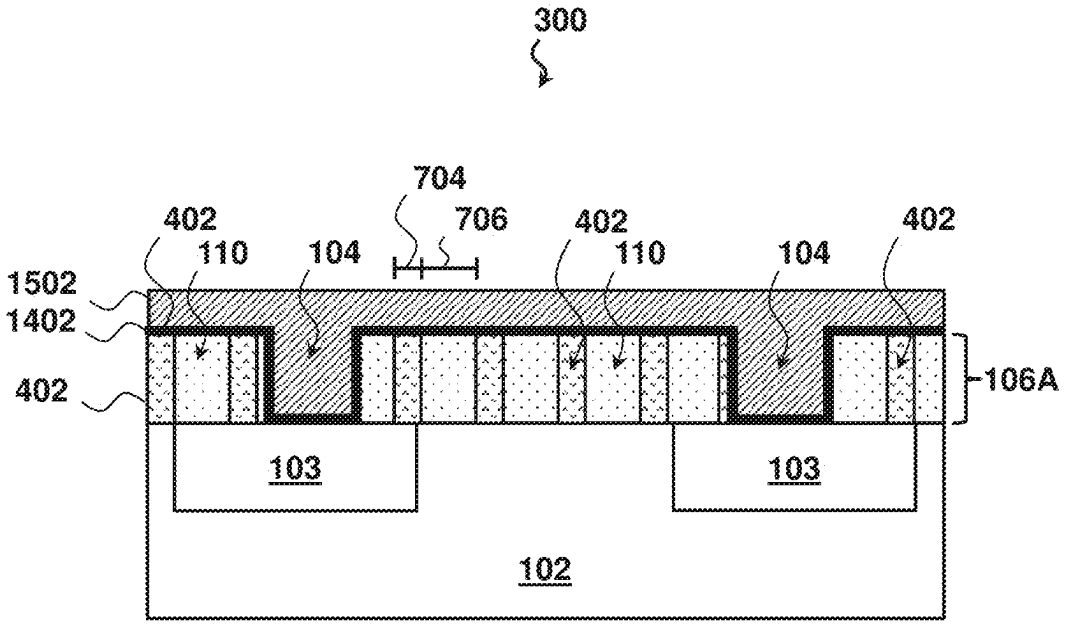
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Fig. 15

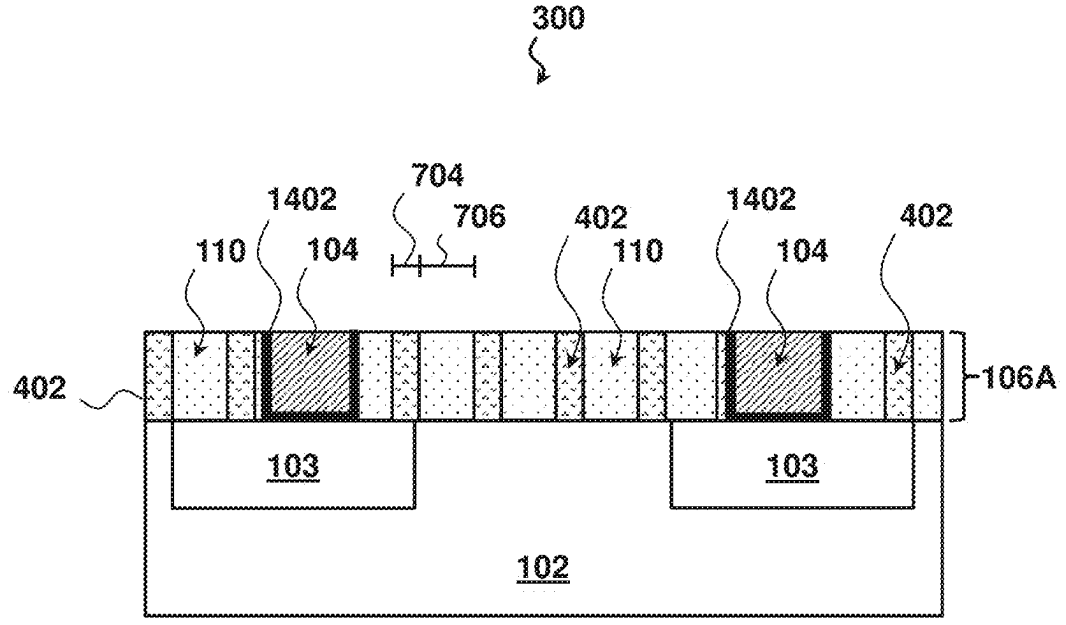
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Fig. 16

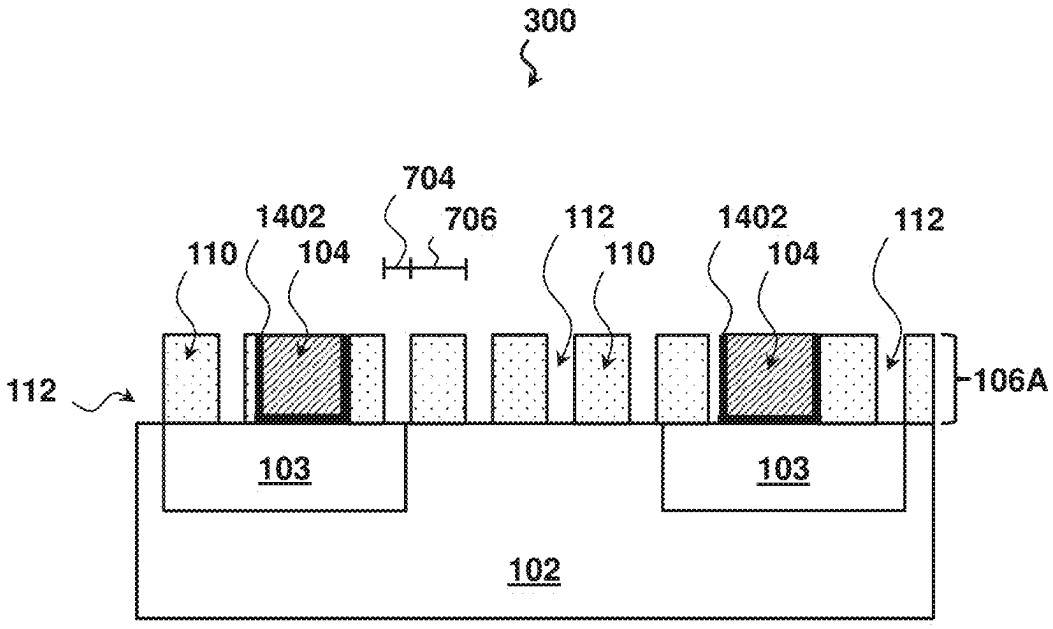
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Fig. 17

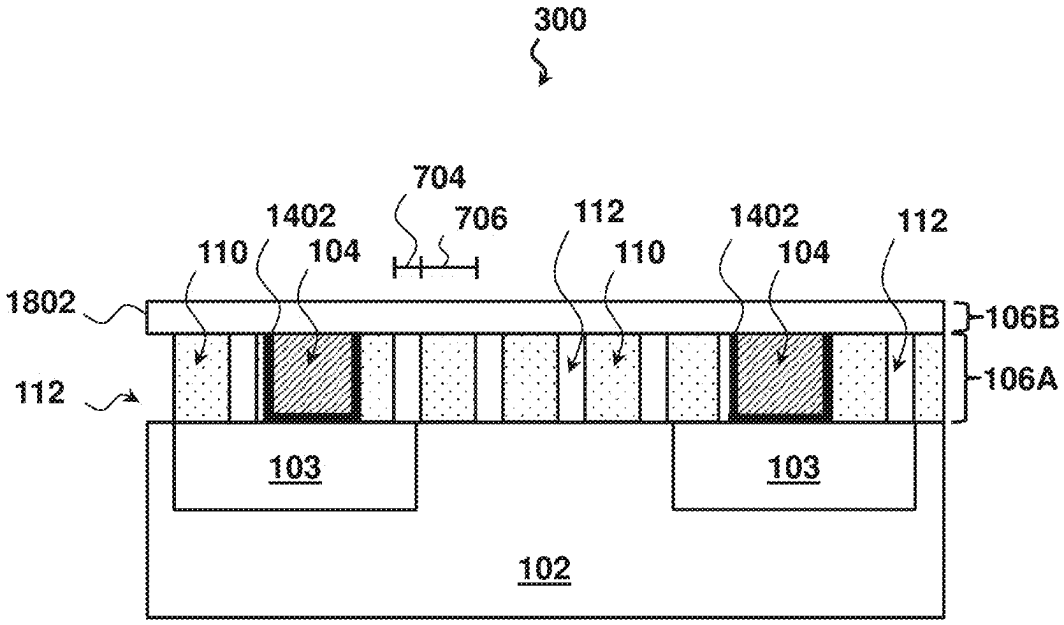
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Fig. 18

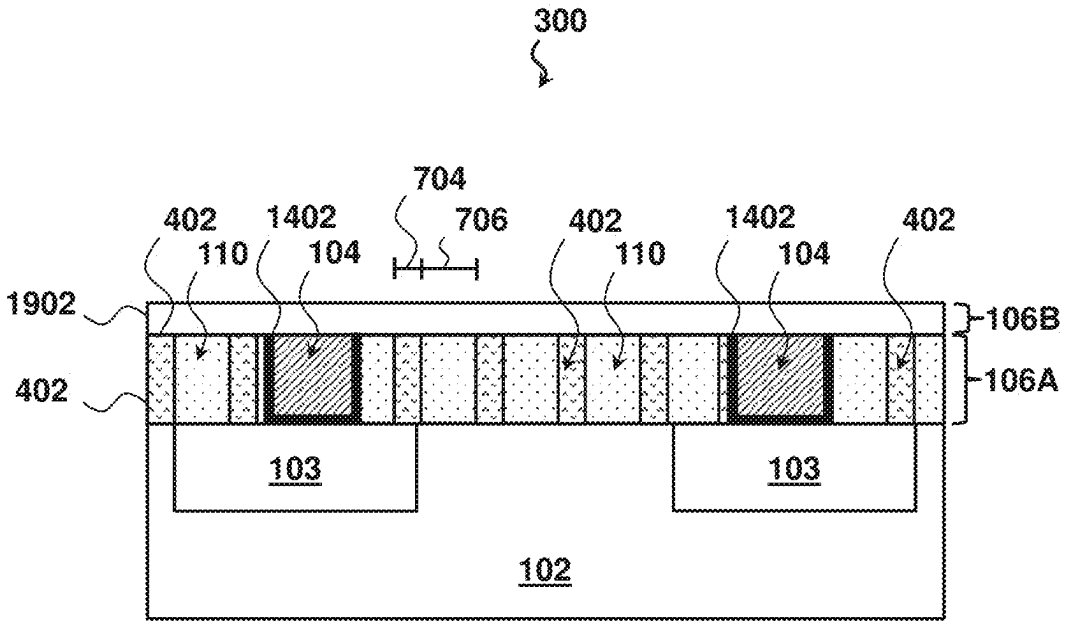
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Fig. 19

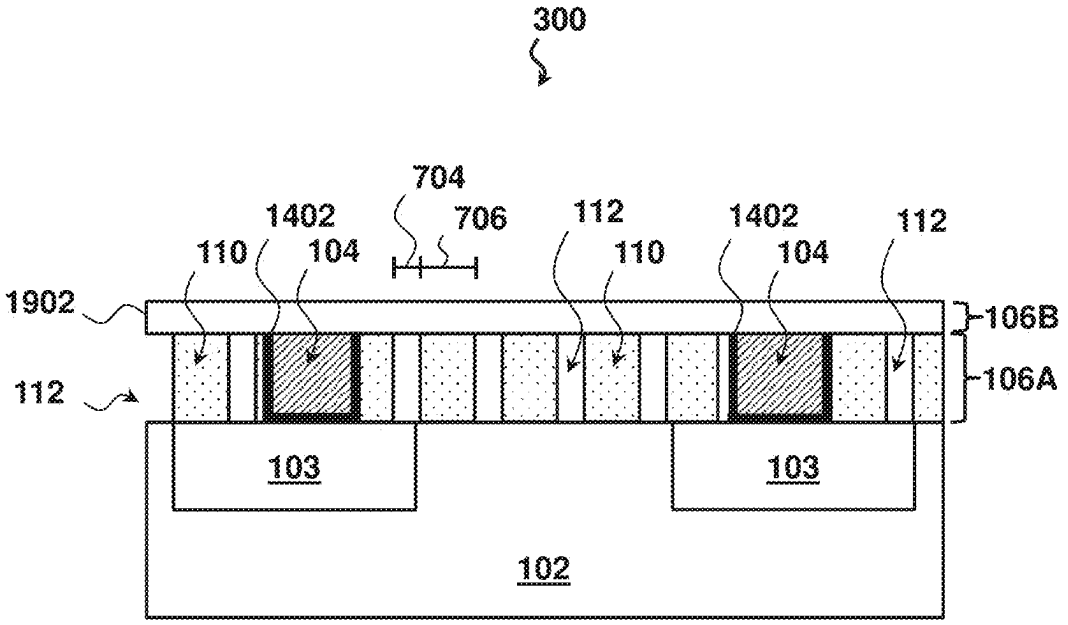
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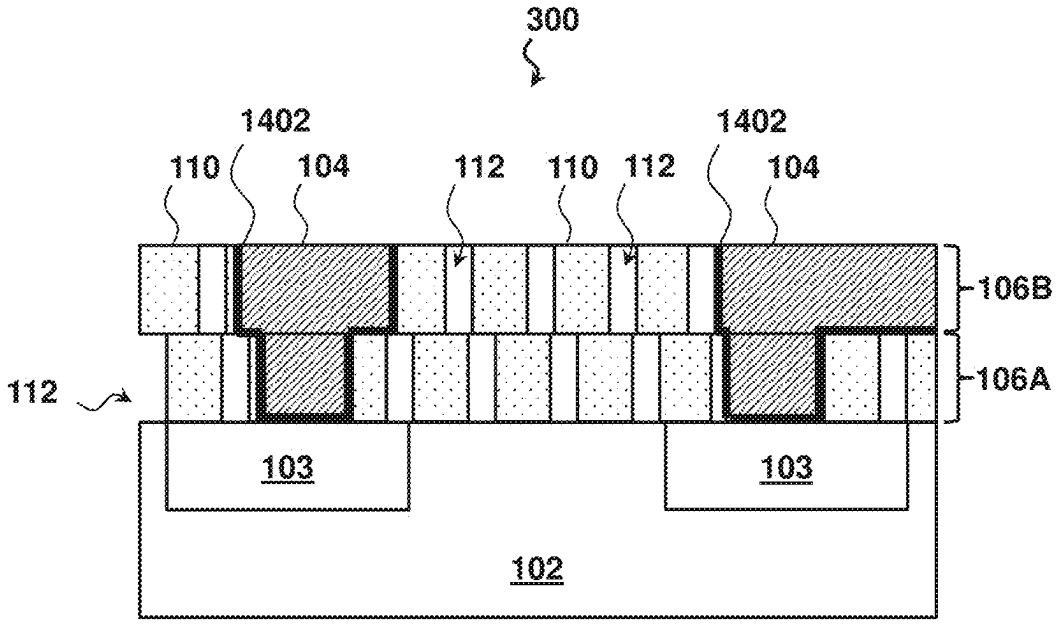
Fig. 20



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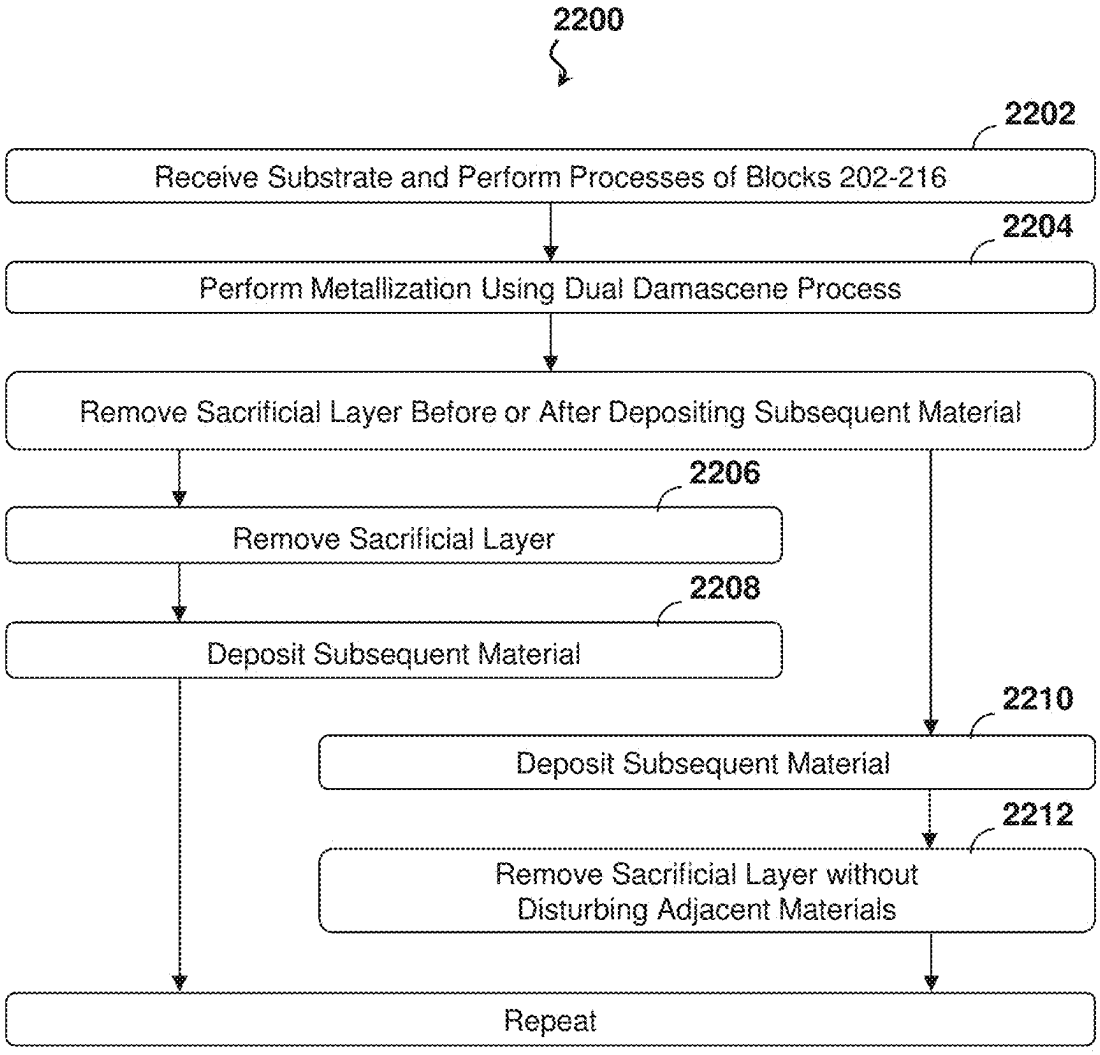
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2202
Receive Substrate and Perform Processes of Blocks 202-216
2204
Perform Metallization Using Dual Damascene Process
Remove Sacrificial Layer Before or After Depositing Subsequent Material
2206
Remove Sacrificial Layer
2208
Deposit Subsequent Material
2210
Deposit Subsequent Material
2212
Remove Sacrificial Layer without Disturbing Adjacent Materials
Repeat

Fig. 22

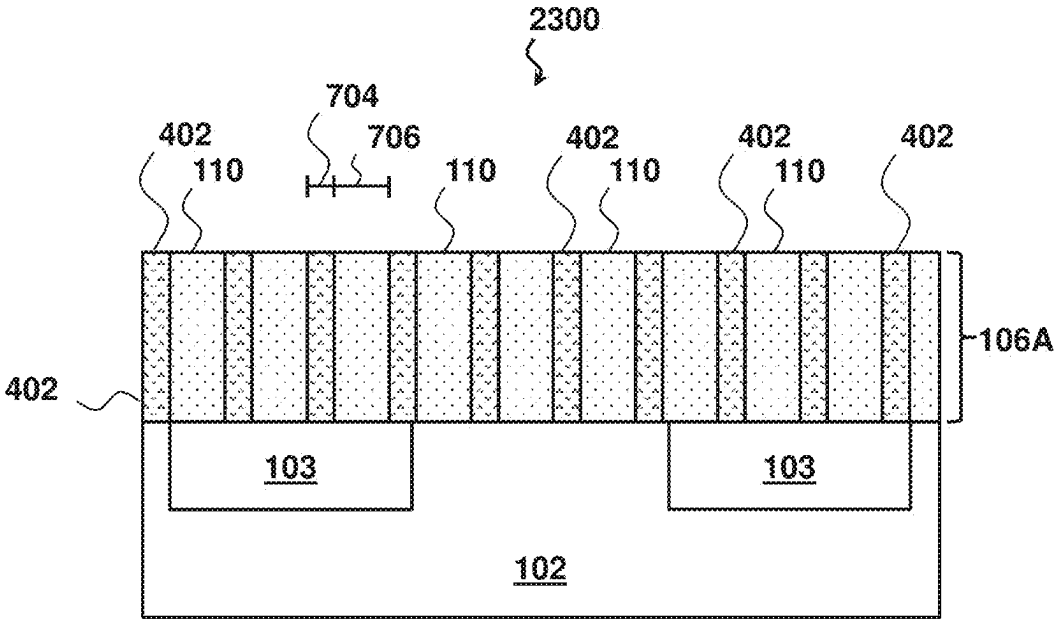
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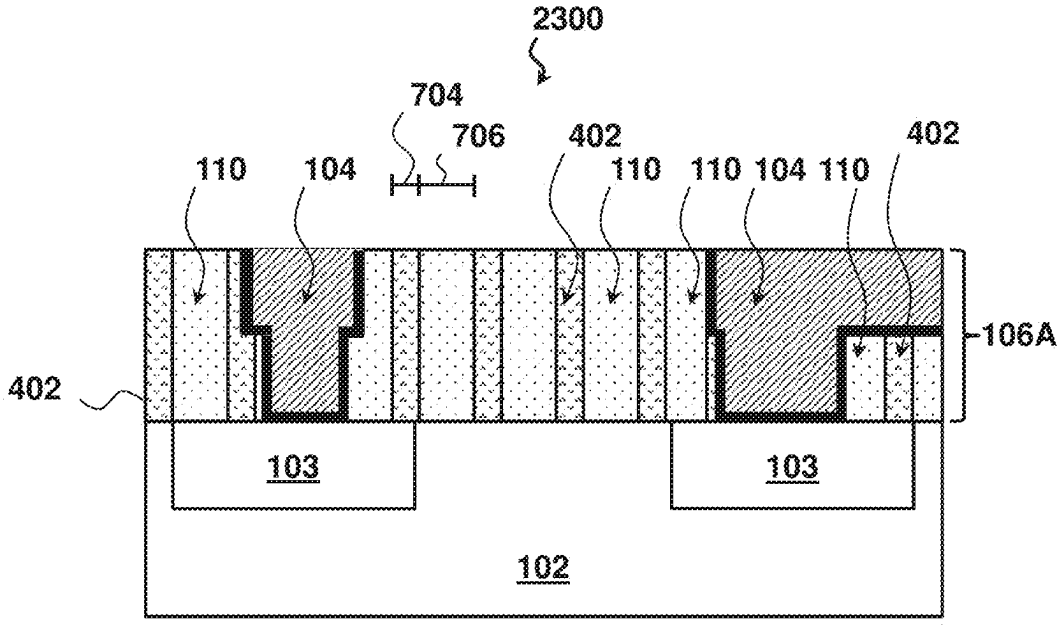
Fig. 23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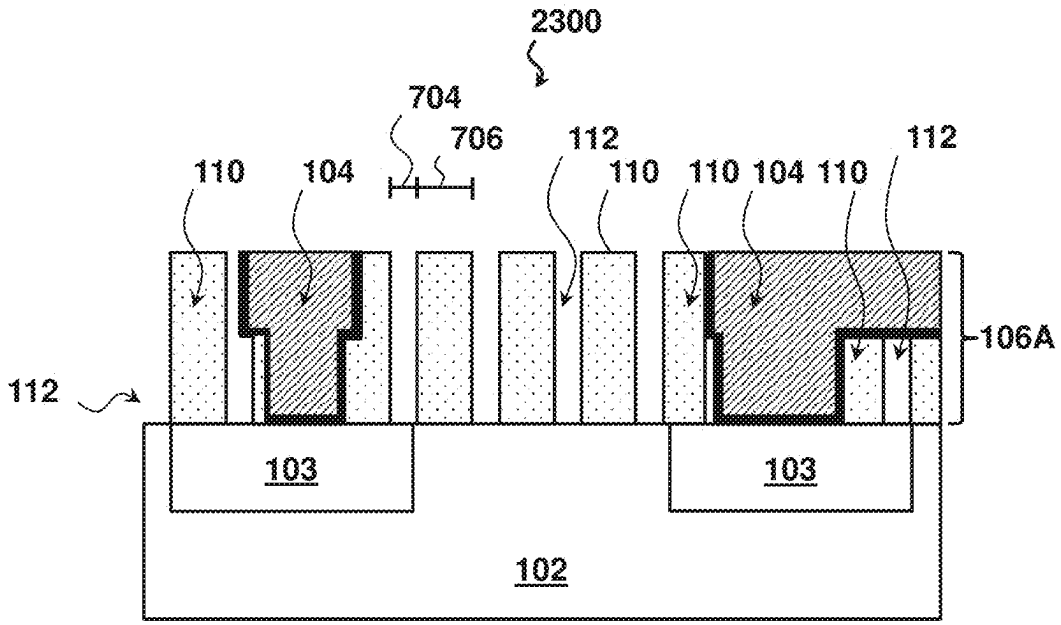
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Fig. 25

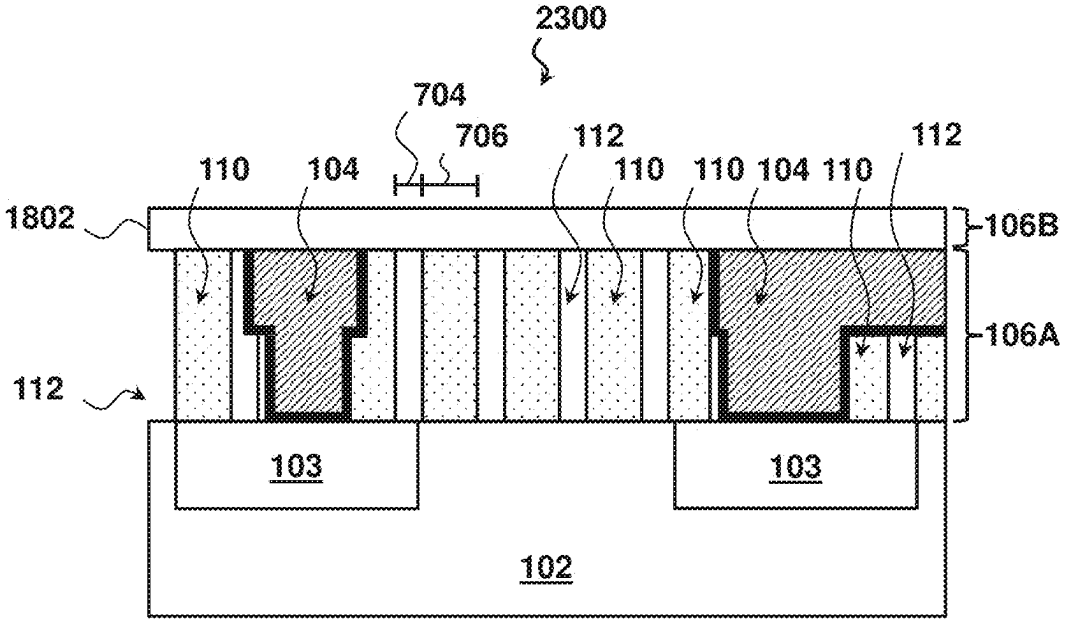
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Fig. 26

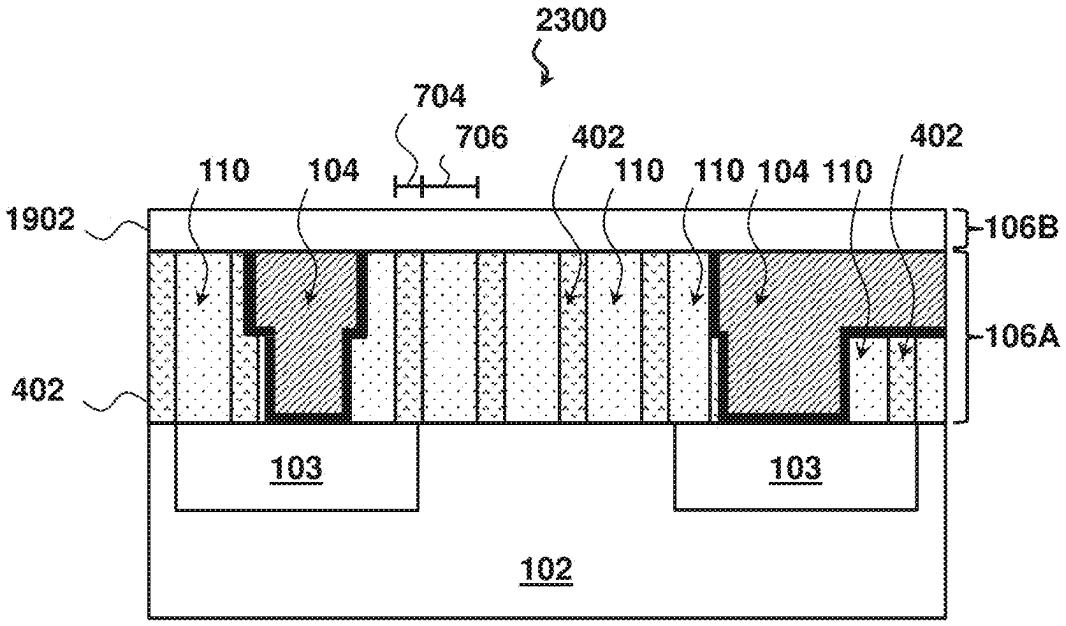
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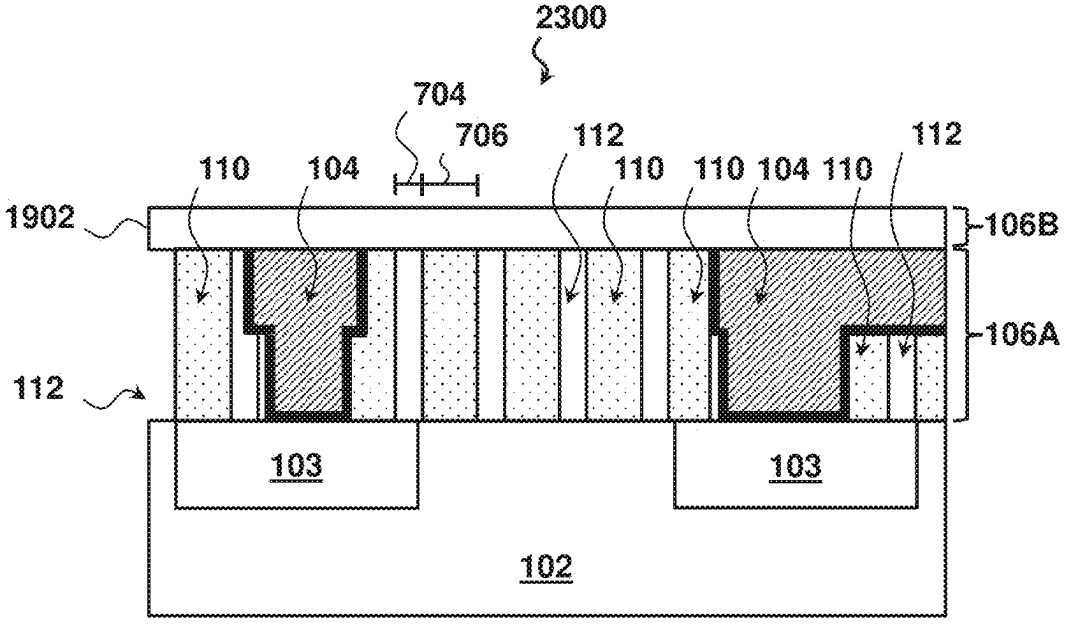
Fig. 27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1902
106B
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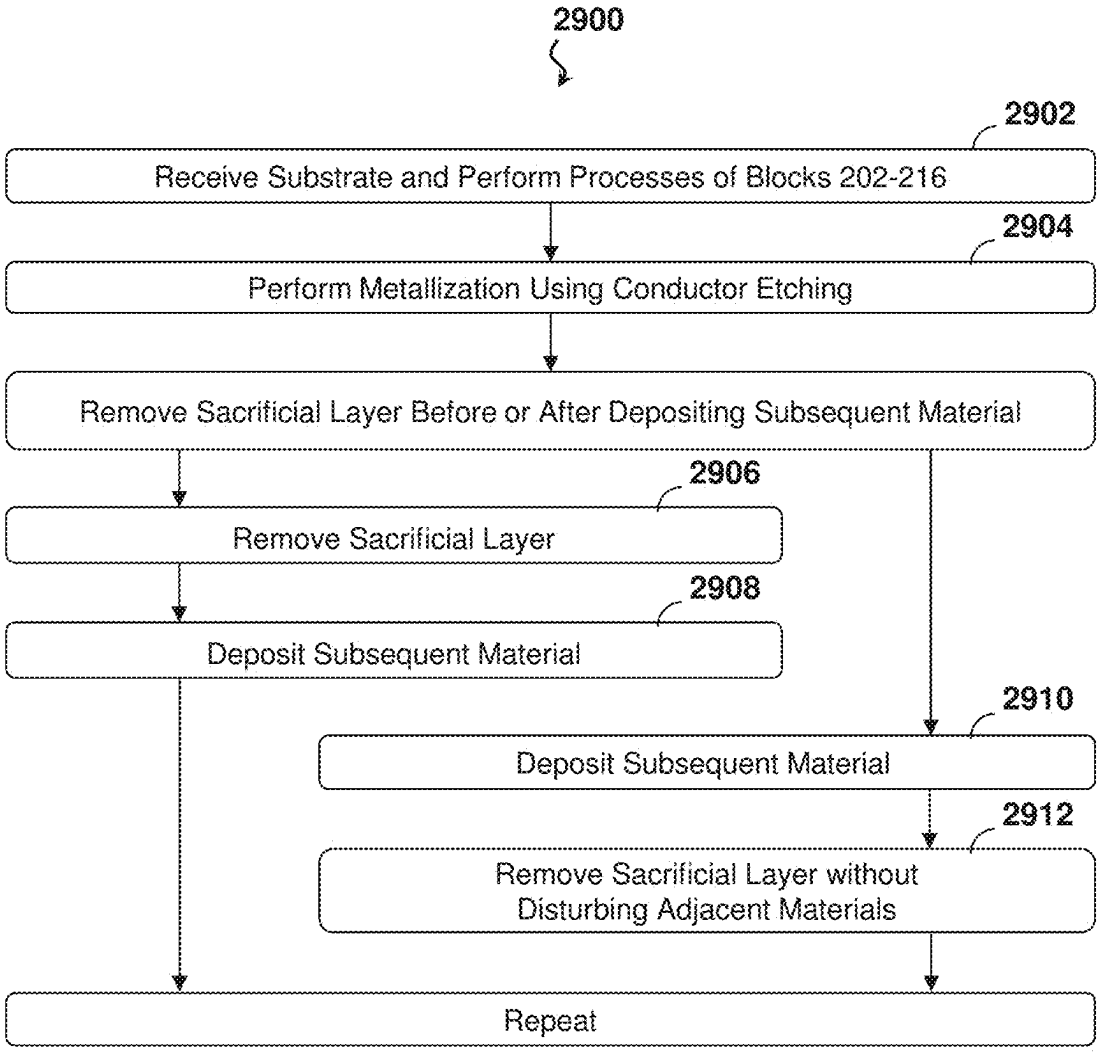
Fig. 28


2900
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Receive Substrate and Perform Processes of Blocks 202-216
2904
Perform Metallization Using Conductor Etching
Remove Sacrificial Layer Before or After Depositing Subsequent Material
2906
Remove Sacrificial Layer
2908
Deposit Subsequent Material
2910
Deposit Subsequent Material
2912
Remove Sacrificial Layer without Disturbing Adjacent Materials
Repeat

Fig. 29

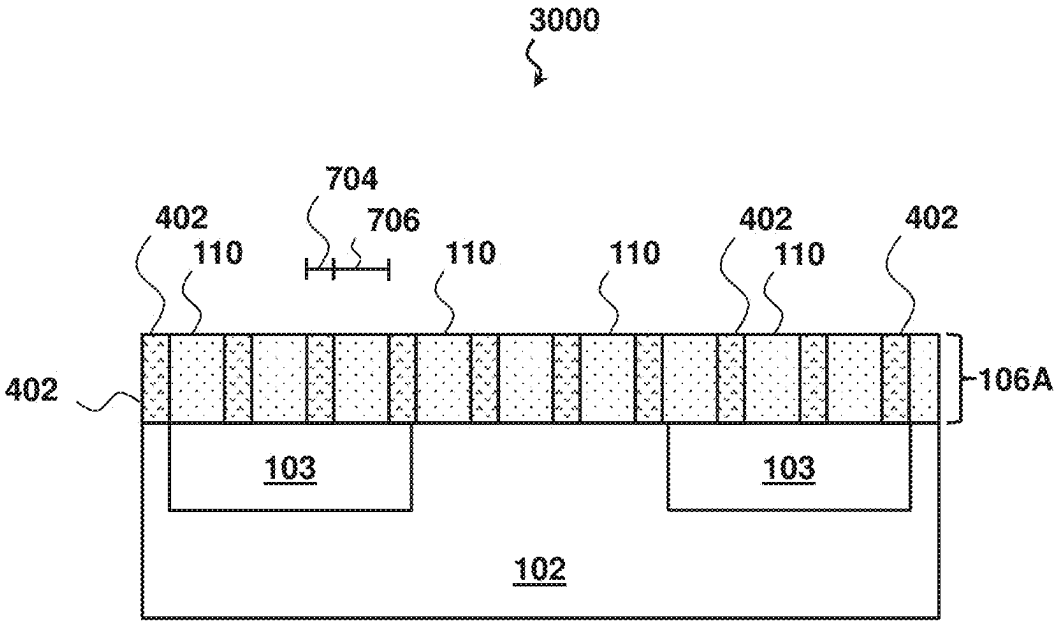
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Fig. 30

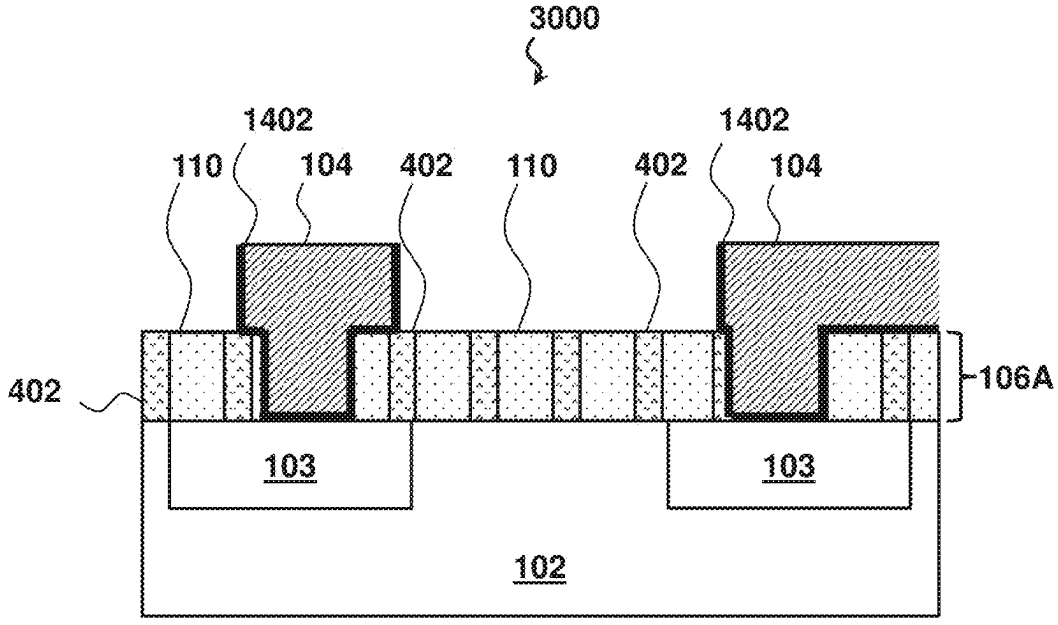
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Fig. 31

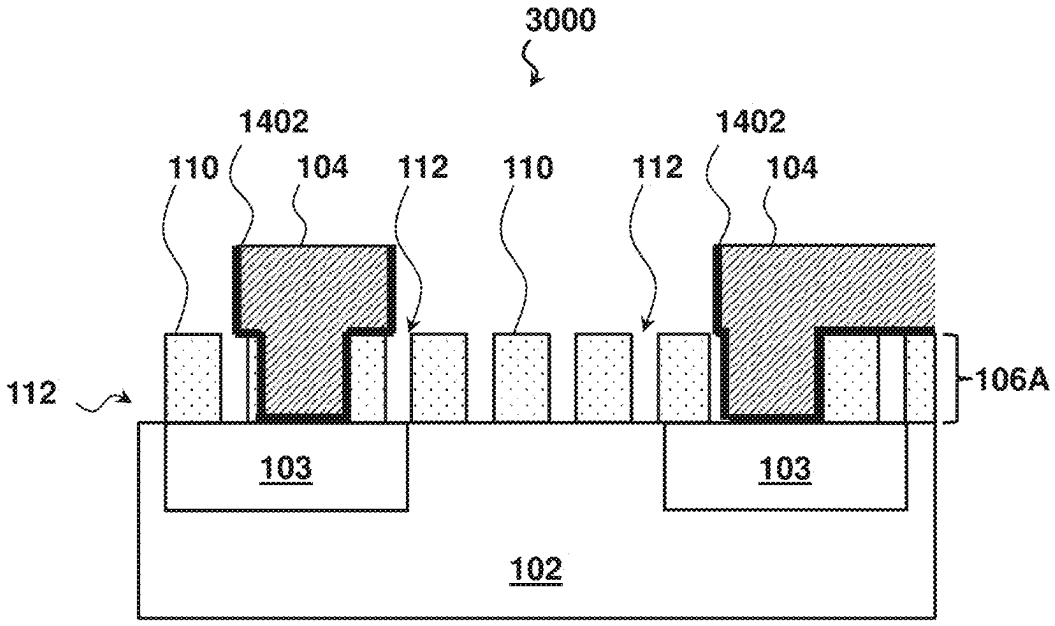
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Fig. 32

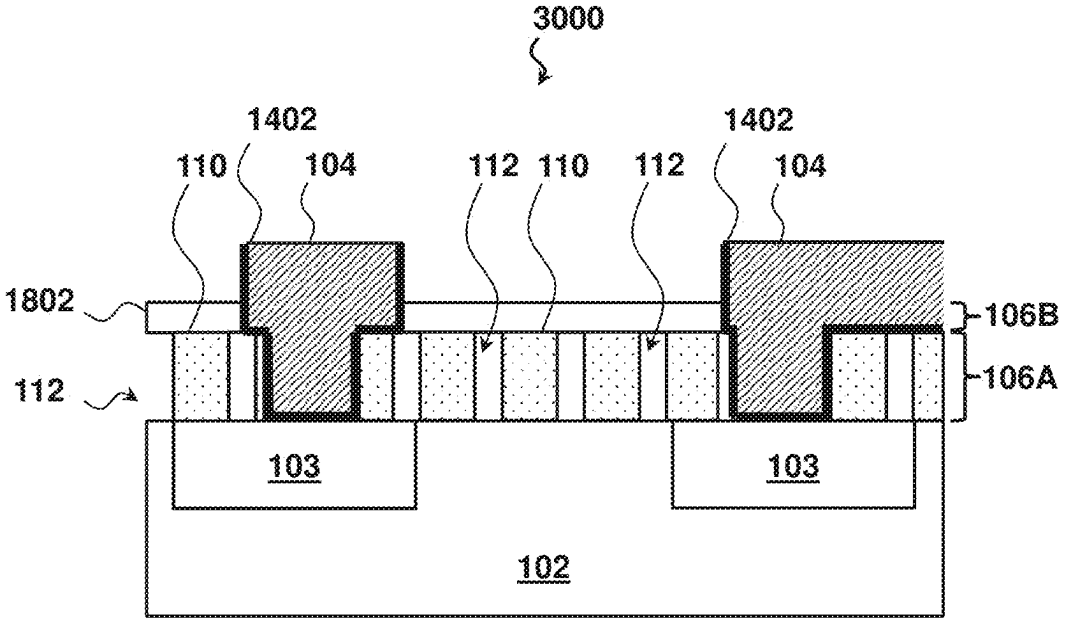
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Fig. 33

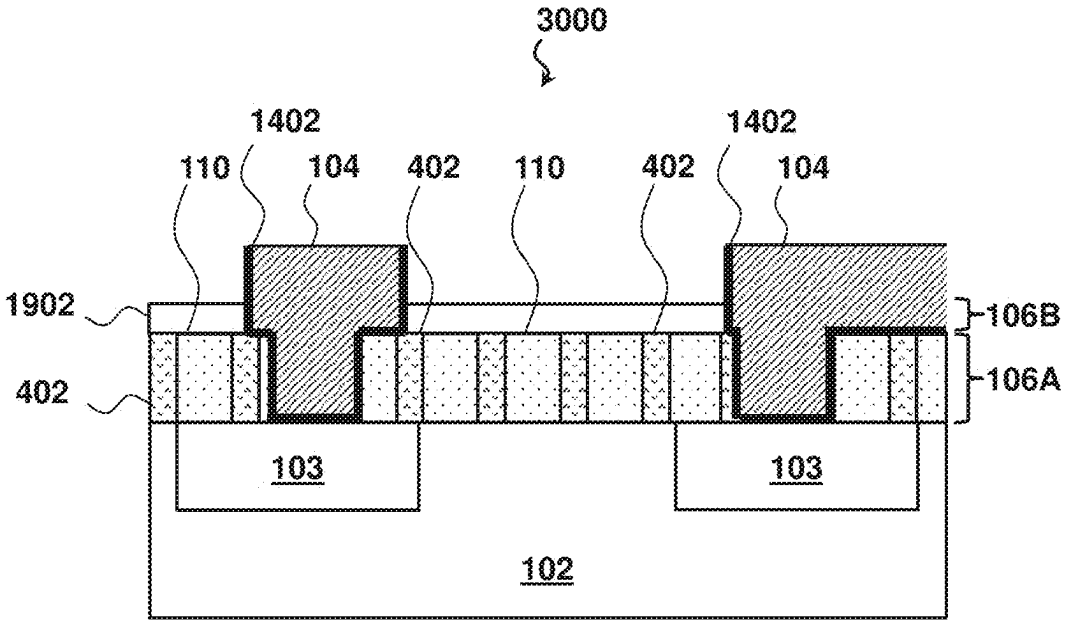
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Fig. 34

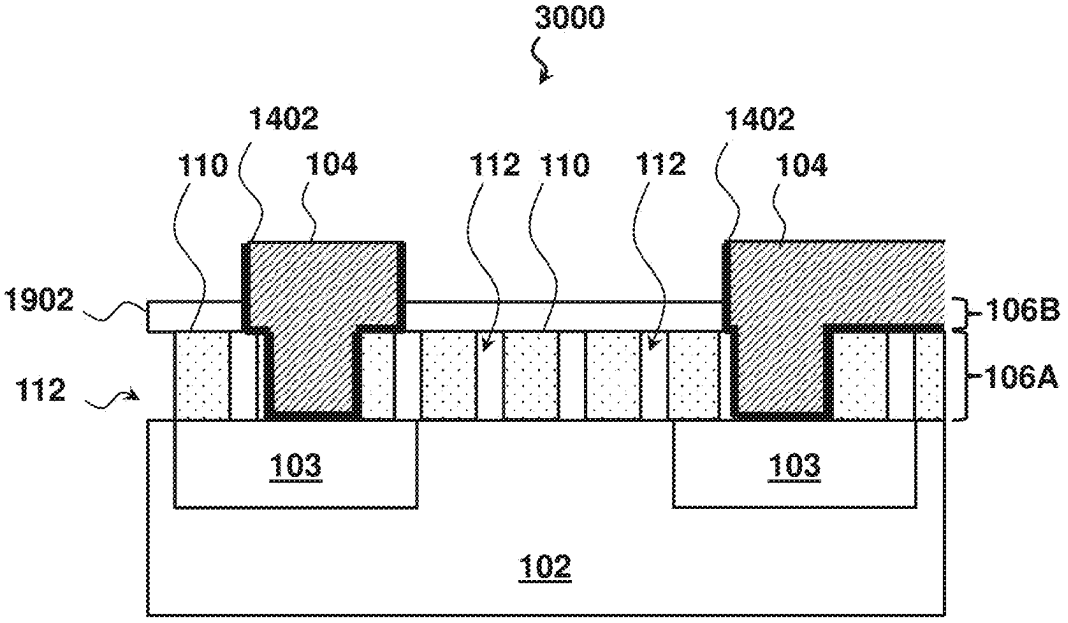
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Fig. 35

STRUCTURE AND METHOD FOR A LOW-K DIELECTRIC WITH PILLAR-TYPE AIR-GAPS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. patent application Ser. No. 18/361,088, filed Jul. 28, 2023, which is a divisional of U.S. patent application Ser. No. 17/080,051, filed Oct. 26, 2020, issued as U.S. Pat. No. 11,728,271, which is a continuation of U.S. patent application Ser. No. 15/096,703, filed Apr. 12, 2016, issued as U.S. Pat. No. 10,818,600, which is a divisional of U.S. patent application Ser. No. 13/925,457, filed Jun. 24, 2013, issued as U.S. Pat. No. 9,312,220, which claims priority to U.S. Provisional Patent Application Ser. No. 61/778,198, filed Mar. 12, 2013, the entire disclosures of which are incorporated herein by reference.

BACKGROUND

[0002] The semiconductor interconnect structure (IC) industry has experienced rapid growth. In the course of IC evolution, functional density (i.e., the number of interconnected devices per chip area) has generally increased while geometry size (i.e., the smallest component (or line) that can be created using a fabrication process) has decreased. This scaling down process generally provides benefits by increasing production efficiency and lowering associated costs. Such scaling down has also increased the complexity of processing and manufacturing ICs, and, for these advances to be realized, similar developments in IC manufacturing are needed.

As merely one example, interconnects, the conductive traces used to carry electrical signals between the elements that make up the circuit, are typically insulated by a dielectric material. Historically, this insulating dielectric has been silicon dioxide. However, the relative permittivity (or dielectric constant) of silicon dioxide, a measure of the insulating properties, is relatively high. Replacing silicon dioxide with a dielectric material having a lower relative permittivity can reduce interference, noise, and parasitic coupling capacitance between the interconnects. Though the benefits are promising, these low-k dielectrics have proven challenging to manufacture. Some materials are brittle, difficult to deposit, sensitive to processes such as etching, annealing, and polishing processes, unstable, and/or otherwise difficult to fabricate. For these reasons and others, although existing interconnect dielectrics have been generally adequate, they have not proved entirely satisfactory in all respects.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0004] FIG. **1** is a cross-sectional view of an interconnect structure according to various aspects of the present disclosure.

[0005] FIGS. **2**A and **2**B are flow diagrams of a method for forming an MLI using a single damascene metallization according to various aspects of the present disclosure.

[0006] FIGS. **3-21** are cross-sectional views of an MLI undergoing a method for forming an MLI using a single damascene metallization according to various aspects of the present disclosure.

[0007] FIG. **22** is a flow diagram of a method for forming an MLI using a dual damascene process according to various aspects of the present disclosure.

[0008] FIGS. **23-28** are cross-sectional views of an MLI undergoing a method for forming an MLI using a dual damascene process according to various aspects of the present disclosure.

[0009] FIG. **29** is a flow diagram of a method for forming an MLI using conductor etching according to various aspects of the present disclosure.

[0010] FIGS. **30-35** are cross-sectional views of an MLI undergoing a method for forming an MLI using conductor etching according to various aspects of the present disclosure.

DETAILED DESCRIPTION

[0011] The present disclosure relates generally to IC device manufacturing and more particularly, to the forming of dielectric materials with pillar-type air gaps.

[0012] The following disclosure provides many different embodiments, or examples, for implementing different features of the disclosure. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0013] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as being "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" can encompass both an orientation of above and below. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0014] FIG. **1** is a cross-sectional view of an interconnect structure **100** according to various aspects of the present disclosure. FIG. **1** has been simplified for the sake of clarity to better illustrate the inventive concepts of the present disclosure. Additional features may be incorporated into the

interconnect structure **100**, and some of the features described below may be replaced or eliminated for other embodiments of the interconnect structure **100**.

[0015] The interconnect structure **100** includes a substrate **102**, which may have one or more circuit devices **103** formed upon it. The circuit devices **103** are electrically coupled to interconnects **104** disposed in one or more interlayer (or inter-level) dielectric structures (ILDs) **106**. Each ILD structure **106** includes conductive interconnects **104** disposed in an insulating dielectric material **110**. The one or more ILD structures **106** may be arranged in a vertical stack to form a multilayer interconnect (MLI) **108**.

[0016] Because the dielectric material **110** of the ILD structures **106** insulates the conductive interconnects **104**, the amount of insulation provided has a direct impact on the performance of the circuit devices **103**. One measure of insulation is the dielectric constant or relative permittivity of the dielectric material. A vacuum is an effective insulator and is often used as a benchmark for permittivity. For reference, the permittivity of a vacuum ε_0, is 8.854×10^{-12} F/m. Dielectric materials (including dielectric material **110**) are typically characterized by their permittivity relative to that of a vacuum expressed as a ratio, k. The relative permittivity, k, of silicon dioxide is 3.9. Dielectric materials with greater permittivity than silicon dioxide and that correspondingly provide reduced insulation are typically referred to as high-k materials and may be commonly used as a gate dielectric, for example. Exemplary high-k dielectric materials include HfO_2, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, other suitable high-k dielectric materials, and/or combinations thereof. Conversely, materials that provide greater insulation may be referred to as low-k materials. Low-k materials may be used in ILDs **106** and other insulating applications. Exemplary low-k dielectric materials include porous silicon dioxide, carbon doped silicon dioxide, low-k silicon nitride, low-k silicon oxynitride, polyimide, spin-on glass (SOG), fluoride-doped silicate glass (FSG), phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), Black Diamond® (Applied Materials of Santa Clara, California), Xerogel, Aerogel, amorphous fluorinated carbon, Parylene, BCB (bis-benzocyclobutenes), SiLK (Dow Chemical of Midland, Michigan), other suitable low-k dielectric materials, and/or combinations thereof.

[0017] Because the permittivity of air is less than that of even low-k dielectrics, efforts have been made to introduce air into the dielectric materials **110** to further reduce the relative permittivity in certain applications. However, air-laden porous materials often prove brittle, difficult to deposit, sensitive to processes such as etching, annealing, and polishing processes, unstable, and/or otherwise difficult to fabricate. For example, damage caused by etching interconnect trenches often damages the dielectric sidewall. This damage can be a significant cause of time-dependent dielectric breakdown (TDDB) which may eventually render the device nonfunctional. Accordingly, in some embodiments of the present disclosure a more stable dielectric material is formed in segments or blocks separated by air gaps **112**, as an alternative to depositing a porous dielectric. The air gaps **112** reduce the permittivity of the overall structure, and in some embodiments, do so without the use of fragile or sensitive dielectric materials. For example, in some embodiments, ultra-low-k (e.g., k less than about 2.5) dielectric structures can be fabricated using materials with a significantly higher k value (e.g., k greater than or equal to about 3.9). In further embodiments, a porous dielectric is formed separated by air gaps **112**, thus reducing the dielectric constant for the structure below even that of the porous dielectric.

[0018] By reducing the relative permittivity of the ILD **106**, in many embodiments, parasitic effects between interconnects **104** are reduced. Because an interconnect **104** can be modeled as a resistor (R) and a capacitor (C), these parasitic effects may be referred to as RC effects. Typically, an adjacent interconnect increases the effective capacitance of a victim. In some embodiments, decreasing the relative permittivity (and thereby improving the insulating qualities) of the dielectric material **110** separating the interconnects **104** reduces this effective capacitance. In some such embodiments, this is achieved by introducing air gaps **112** into the ILD structure **106**. Accordingly, in some such embodiments, the air gaps **112** reduce the effective capacitance and thereby the energy required to drive a signal through the interconnect **104**. This allows the use of lower powered devices. The advantages also extend beyond RC effects. In one example, by reducing permittivity, the air gaps **112** may also reduce parasitic noise that may cause signal errors. In further example, the increased permittivity due to air gaps **112** allows for closer interconnect **104** spacing and reduced overall circuit size. Of course, these advantages are merely exemplary, and one of skill in the art will recognize further advantages of the principles of the present disclosure. No particular advantage is necessary or required for any particular embodiment.

[0019] The structure of the interconnect structure **100** will now be disclosed in more detail. As disclosed above, the interconnect structure **100** is formed on a substrate **102**. In some embodiments, the substrate **102** includes an elementary semiconductor (e.g., silicon or germanium) and/or a compound semiconductor (e.g., silicon germanium, silicon carbide, gallium arsenic, indium arsenide, gallium nitride, and indium phosphide). Other exemplary substrate materials include alloy semiconductors, such as silicon germanium carbide, gallium arsenic phosphide, and gallium indium phosphide. The substrate **102** may also comprise non-semiconductor materials including soda-lime glass, fused silica, fused quartz, calcium fluoride (CaF_2), and/or other suitable materials. In some embodiments, the substrate **102** has one or more layers defined within it, such as an epitaxial layer. For example, in one such embodiment, the substrate **102** includes an epitaxial layer overlying a bulk semiconductor. Other layered substrates include semiconductor-on-insulator (SOI) substrates. In one such SOI substrate, the substrate **102** includes a buried oxide (BOX) layer formed by a process such as separation by implanted oxygen (SIMOX). In various embodiments, the substrate **102** may take the form of a planar substrate, a fin, a nanowire, and/or other forms known to one of skill in the art.

[0020] The substrate **102** may include one or more doped regions. For example, a region of the substrate **102** may be doped with a p-type dopant. Suitable p-type dopants include boron, gallium, indium, other suitable p-type dopants, and/or combinations thereof. The substrate may also include one or more regions doped with an n-type dopant such as phosphorus, arsenic, other suitable n-type dopants, and/or combinations thereof. Doping may be implemented using a process such as ion implantation or diffusion in various steps and techniques.

[0021] The substrate **102** may have one or more circuit devices **103** formed on the substrate **102**. These circuit devices **103** may include P-channel field effect transistors (PFETs), N-channel FETs (NFETs), metal-oxide semiconductor field effect transistors (MOSFETs), complementary metal-oxide semiconductor (CMOS) transistors, FinFETs, high voltage transistors, high frequency transistors, bipolar junction transistors, diodes, resistors, capacitors, inductors, varactors, other suitable devices, and/or combinations thereof.

[0022] In an exemplary embodiment, the circuit device **103** is a field effect transistor and includes doped source/drain regions **114** and a gate stack **116** disposed between the source/drain regions **114**. The source/drain regions **114** have a dopant implanted therein that is appropriate for the design requirements of the associated device. Suitable p-type dopants include boron, gallium, indium, other suitable p-type dopants, and/or combinations thereof. Suitable n-type dopants include phosphorus, arsenic, other suitable n-type dopants, and/or combinations thereof. Doping may be implemented using a process such as ion implantation or diffusion in various steps and techniques.

[0023] The gate stack **116** is disposed above and between the source/drain regions **114** and defines a channel region in the substrate **102**. The channel region is an active region in the substrate in which the majority carriers flow between the source and drain regions when the device is in a conduction mode and is controlled by the gate stack **116**. The gate stack **116** may include an interfacial layer **118**, a gate dielectric **120**, a gate electrode **122**, and/or other suitable layer. An exemplary interfacial layer **118** may include silicon dioxide, silicon nitride, silicon oxynitride, other semiconductor oxides, other suitable interfacial materials, and/or combinations thereof. The gate dielectric **120** may include a high-k dielectric material such as HfO_2, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, zirconium oxide, aluminum oxide, hafnium dioxide-alumina (HfO_2—Al_2O_3) alloy, other suitable high-k dielectric materials, and/or combinations thereof. Additionally or in the alternative, the gate dielectric **120** may include other dielectrics such as a silicon dioxide, silicon nitride, silicon oxynitride, silicon carbide, amorphous carbon, tetraethylorthosilicate (TEOS), other suitable dielectric material, and/or combinations thereof. The gate electrode **122** may be a polysilicon gate, a dummy gate, a metal gate, and/or other suitable gate electrode. In that regard, the gate electrode **122** may include any suitable material, such as polysilicon, aluminum, copper, titanium, tantalum, tungsten, molybdenum, tantalum nitride, nickel silicide, cobalt silicide, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, metal alloys, other suitable materials, and/or combinations thereof. The gate stack **116** may also include sidewall spacers formed on one or more lateral surfaces of the gate stack **116**.

[0024] The circuit device **103** is electrically coupled to other circuit devices via the multi-layer interconnect (MLI) structure **108**. The MLI **108** is a vertical stack of one or more ILD structures **106** formed above the substrate **102**. Each ILD structure **106** includes conductive interconnects **104** disposed in a dielectric material **110**. The interconnects **104** may contain copper, aluminum, aluminum/silicon/copper alloy, titanium, titanium nitride, tungsten nitride, metal silicide, non-metallic conductive material, and/or combinations thereof. As disclosed above, the ILD dielectric material **110** may be any suitable dielectric. In some embodiments, the material **110** includes a low-k dielectric such as porous silicon dioxide, carbon doped silicon dioxide, low-k silicon nitride, low-k silicon oxynitride, polyimide, SOG, FSG, PSG, BPSG, Black Diamond®, Xerogel, Aerogel, amorphous fluorinated carbon, Parylene, BCB, SILK, other suitable low-k dielectric materials, and/or combinations thereof. Additionally or in the alternative, the dielectric material **110** includes a traditional dielectric such as silicon dioxide, silicon nitride, silicon oxynitride, and/or combinations thereof. Each ILD **106** may, in itself, comprise several layers of disparate dielectric material **110**. Examples of ILD **106** sub-layers include etch stop layers and/or a contact etch stop layers (CESL) (e.g., CESL **124** of FIG. **1**).

[0025] In some embodiments, the dielectric material **110** of the ILD **106** is separated by one or more air gaps **112** that serve to lower the permittivity of the ILD **106**. Due in part to the orientation, these may be termed pillar-type air gaps **112**. In some embodiments, the air gaps **112** extend from a top surface of an ILD **106** to a bottom surface of the ILD **106**, thereby extending completely through the ILD **106**. In some embodiments, the air gaps **112** extend from a first surface of an ILD **106** to a sub-layer of the ILD **106**, thus extending completely through a first material of the ILD **106** but not extending through a second material of the ILD **106**. In some embodiments, the air gaps **112** extend longitudinally in a direction perpendicular to the surface of the substrate **102** and thus the interface between the substrate and the ILD **106**. The principles of the present disclosure apply equally to these orientations as well as others as recognized by one of skill in the art. Accordingly, further embodiments include air gaps **112** of varying depth, size, and orientation.

[0026] As disclosed above, air has a lower permittivity than most dielectric materials, and the air gaps **112** may reduce the permittivity of the ILD **106** without further changes to the dielectric material **110**. This provides benefits including reduced capacitive effects between interconnects **104** and reduced parasitic noise. In some embodiments, reduced permittivity allows for closer interconnect **104** spacing and reduced device size and strength. In various embodiments, the introduction of air gaps **112** allows the use of dielectric materials **110** that have a relatively higher permittivity but are more structurally sound, less sensitive, and/or easier to manufacture.

[0027] The principles and concepts of the present disclosure apply equally to a variety of processes for forming an ILD **106** and an associated MLI **108**. For brevity, only a selected set of examples are provided. One of skill in the art will recognize that these are not limiting and that the principles can be applied to further processes. In some exemplary embodiments, the process for forming air gaps is integrated with a single damascene metallization process. The process is disclosed with reference to FIGS. **2**A and **2**B and FIGS. **3**-**21**. FIGS. **2**A and **2**B are flow diagrams of the method **200** for forming an MLI using a single damascene metallization according to various aspects of the present disclosure. It is understood that additional steps can be provided before, during, and after the method **200** and that some of the steps described can be replaced or eliminated for other embodiments of the method **200**. FIGS. **3**-**21** are cross-sectional views of an MLI **300** undergoing the method **200** for forming the MLI **300** using a single damascene metallization according to various aspects of the present

disclosure. FIGS. **3-21** have been simplified for the sake of clarity and to better illustrate the inventive concepts of the present disclosure.

[0028] Referring to block **202** of FIG. **2**A and to FIG. **3**, a substrate **102** is received. The substrate **102** may be substantially similar to the substrate **102** disclosed with respect to FIG. **1** and includes circuit devices **103** substantially similar to the circuit device **103** of FIG. **1** formed upon the substrate **102**. Referring to block **204** of FIG. **2**A and to FIG. **4**, a sacrificial layer **402** is formed over the substrate **102**. In an exemplary embodiment, the sacrificial layer **402** includes polyimide, although any suitable resist material with good mechanical and thermal stability may be used. The sacrificial layer **402** may be formed using any suitable deposition method, including atomic layer deposition (ALD), chemical vapor deposition (CVD), high-density plasma CVD (HDP-CVD), plasma enhanced CVD (PECVD), physical vapor deposition (PVD), spin-on deposition, and/or other suitable deposition processes, and may be formed to any suitable thickness. The sacrificial layer **402** defines a first ILD structure **106**A.

[0029] Referring to block **206** of FIG. **2**A and to FIG. **5**, a hard mask layer **502** is formed over the sacrificial layer **402** and protects the sacrificial layer **402** during processing. In some embodiments, the hard mask layer **502** includes a dielectric material such as silicon dioxide, silicon nitride, silicon oxynitride, silicon carbide, and/or other suitable materials. The hard mask layer **502** may be formed using any suitable deposition method and may be formed to any suitable thickness. In an exemplary embodiment, a hard mask layer **502** containing nitrogen-doped silicon carbide is formed via CVD. In a further exemplary embodiment, a hard mask layer **502** containing silicon nitride is formed via PECVD.

[0030] Referring to block **208** of FIG. **2**A and to FIG. **6**, a copolymer coating **602** is formed over the hard mask layer **502**. The copolymer coating **602** is used to form a mask for defining air gaps of the ILD **106**A. In some embodiments, the copolymer coating **602** includes a directed self-assembly (DSA) material. DSA materials take advantage of the tendency of some copolymer materials to align in regular, repeating patterns, such as spherical, cylindrical, lamellar (layered), and/or bicontinuous gyroid arrangements, in what is termed microphase separation. The morphology of the microphase separated copolymer may depend on the polymers used, the relative amounts of the constituent polymers, process variables including temperature, and other factors. Once a desired morphology is obtained, subsequent fabrication processes may transfer the pattern to an underlayer such as the sacrificial layer **402**. In some embodiments, constituent polymers of the copolymer coating **602** have different sensitivities to particular etchants. Individual constituent polymers may be removed, and the remaining polymers may be used as a mask to pattern underlying layers.

[0031] In an exemplary embodiment, in block **208**, a copolymer coating **602** including polystyrene and polymethyl methacrylate (PMMA) is formed to a thickness of between about 1 nm and about **100** nm using a spin-coating process. Polystyrene is hydrophobic, whereas PMMA is slightly less so. Further embodiments also utilize a copolymer coating **602** with a hydrophobic first constituent and a hydrophilic second constituent as this facilitates segregation of the constituent polymers.

[0032] Referring to block **210** of FIG. **2**A and to FIG. **7**, one or more processes may be performed on the copolymer coating **602** to induce microphase separation. The particular processes may depend on the constituent polymers of the copolymer coating **602** and may include heating, cooling, introduction of a solvent, application of a magnetic field, and/or other techniques known to one of skill in the art. In an exemplary embodiment, a copolymer coating **602** containing polystyrene and PMMA is annealed at a temperature of between about 100° C. and about 400° C. in order to induce microphase separation. This causes the constituent polymer blocks to segregate and align. In the illustrated embodiment, the microphase separation forms blocks of a first constituent polymer **702**A and blocks of a second constituent polymer **702**B. The constituent polymer blocks **702**A and **702**B are exaggerated for clarity. In various embodiments, polymer blocks **702**A have a width **704** of between about 2 nm and about 50 nm and polymer blocks **702**B have a width **706** of between about 2 nm and about 50 nm. It is understood that the width **704** of the polymer blocks **702**A and the width **706** of the polymer blocks **702**B are not necessarily equivalent and may vary independently. Block widths may be controlled during the deposition of the copolymer coating **602** of block **208** and may depend on deposition parameters such as the selected constituent polymers, the relative concentration of constituent polymers, the use of a solvent, and/or other deposition parameters and techniques known to one of skill in the art. In particular, block sizes may depend on the molecular weights of the constituent polymers and/or the relative molecular weights of the constituent polymers. Block sizes may also be controlled during the microphase separation of block **210** via processing parameters such as temperature, use of a solvent, application of a magnetic field, the ambient gas atmosphere, and/or other suitable parameters.

[0033] Referring to block **212** of FIG. **2**A and to FIG. **8**, blocks of a constituent polymer (e.g., the second constituent polymer **702**B) are selectively removed. The selective removal process does not remove blocks of the first constituent polymer **702**A. The removal process may include any suitable etching process such as dry etching, wet etching, ashing, and/or other etching methods (e.g., reactive ion etching). In some embodiments, the removal process includes the use of a solvent such as acetone, benzene, chloroform, methylene chloride, and/or other suitable solvent. In an exemplary embodiment, PMMA is more sensitive to O_2 plasma etching than polystyrene. Accordingly O_2 plasma etching is used with a PMMA/polystyrene copolymer coating **602** to remove the PMMA and leave the polystyrene behind as a mask.

[0034] Referring to block **214** of FIG. **2**A and to FIG. **9**, the hard mask **502** is opened and the sacrificial layer **402** is etched. The etchings of the hard mask **502** and the sacrificial layer **402** use the remaining blocks of the first constituent polymer **702**A as a mask to prevent etching regions of the hard mask **502** and the sacrificial layer **402** underlying the blocks **702**A. The etching of block **214** may include any suitable etching process such as dry etching, wet etching, ashing, and/or other etching methods (e.g., reactive ion etching). In some embodiments, the etching includes multiple etching steps with different etching chemistries each targeting a particular material of the hard mask **502** and the sacrificial layer **402**. In an embodiment, a silicon carbide hard mask **502** is etched using dry etching with a chlorine-

based etchant chemistry, and a polyimide sacrificial layer **402** is etched using dry etching with an oxygen-based etchant chemistry. In some embodiments, the etching process removes the remaining copolymer blocks **702**A.

[0035] Referring to block **216** of FIG. **2**A and to FIG. **10**, a dielectric material **110** is deposited above the substrate **102** and within the etched sacrificial layer **402** to further define the ILD structure **106**A. The deposition of the dielectric material **110** may include any suitable process including ALD, CVD, HDP-CVD, PVD, spin-on deposition, and/or other suitable deposition processes. In some embodiments, the dielectric material **110** includes a low-k dielectric such as porous silicon dioxide, carbon doped silicon dioxide, low-k silicon nitride, low-k silicon oxynitride, SOG, FSG, PSG, BPSG, Black Diamond®, Xerogel, Aerogel, amorphous fluorinated carbon, Parylene, BCB, SiLK, other suitable low-k dielectric materials, and/or combinations thereof. In one such embodiment, a low-k silicon dioxide material is deposited via a PECVD process. In further embodiments, the air gaps **112** formed by the method **200** allow the use of traditional dielectrics (e.g., silicon dioxide, silicon nitride, silicon oxynitride, etc.) to produce a low-k ILD structure **106**A. In one such embodiment, a conventional silicon dioxide material is deposited via a CVD process. These traditional dielectrics may have better material properties and may be easier to fabricate than their low-k counterparts. A chemical-mechanical polishing (CMP) process may follow the deposition. In some embodiments, the CMP process removes the remaining copolymer blocks **702**A. The CMP process may also remove the hard mask layer **502**.

[0036] Referring to block **218** of FIG. **2**A and to FIG. **11**, a photoresist coating **1102** is formed above the dielectric material **110** and the etched sacrificial layer **402**. Referring to block **220** of FIG. **2**A and to FIG. **12**, the photoresist coating **1102** is patterned to define an interconnect trench. The patterning of block **220** may include soft baking, mask aligning, exposure, post-exposure baking, developing the photoresist, rinsing, and drying (e.g., hard baking). Alternatively, the photolithographic process may be implemented, supplemented, or replaced by other methods such as maskless photolithography, electron-beam writing, and ion-beam writing. Referring to block **222** of FIG. **2**A and to FIG. **13**, the dielectric material **110** and/or the sacrificial layer **402** is etched using the remaining photoresist coating **1102** as a mask. The etching of block **222** may include any suitable etching process such as dry etching, wet etching, ashing, and/or other etching methods (e.g., reactive ion etching). In an embodiment, a silicon dioxide-containing dielectric material **110** is etched using buffered hydrofluoric acid. Remaining photoresist coating **1102** may be removed following the etching of block **222**.

[0037] Referring to block **224** of FIG. **2**B and to FIG. **14**, a barrier layer **1402** and/or a seed layer (not shown) may be formed above the substrate. A barrier layer **1402** is used in some metallization processes to prevent conductive material from diffusing into surrounding structures. In some embodiments, the barrier layer **1402** includes a non-oxide dielectric, such as silicon nitride or a polymer dielectric. In further embodiments, the barrier layer **1402** includes a metal or metal compound, such as aluminum, titanium, tantalum, tungsten, molybdenum, tantalum nitride, nickel silicide, cobalt silicide, TIN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, metal alloys, other suitable materials, and/or combinations thereof. The deposition of the barrier layer **1402** may include any suitable process including ALD, CVD, HDP-CVD, PVD, spin-on deposition, and/or other suitable deposition processes. In an embodiment, a barrier layer **1402** containing TiN is deposited using PVD. In another exemplary embodiment, a barrier layer **1402** containing WN is deposited using ALD.

[0038] In some embodiments, a seed layer is used to promote growth of a conductive material. The deposition may include any suitable process including ALD, CVD, HDP-CVD, PVD, spin-on deposition, and/or other suitable deposition processes. In an embodiment, a copper seed layer is deposited above a barrier layer **1402** using a PVD process.

[0039] Referring to block **226** of FIG. **2**B and to FIG. **15**, interconnects **104** are formed by depositing a conductive material **1502**. Interconnects **104** are broad examples of conductive structures and in various embodiments take the form of conductive traces, vias, bonding pads, and/or other conductive structures. Interconnects **104** may contain copper, aluminum, aluminum/silicon/copper alloy, titanium, titanium nitride, tungsten nitride, metal silicide, non-metallic conductive material, other suitable conductive materials, and/or combinations thereof. In some embodiments, interconnects **104** are formed via electroless plating, electroplating, CVD, ALD, PVD, sputtering, and/or other suitable deposition processes. In one such embodiment a copper-containing interconnect **104** is formed via electroless plating. Referring to block **228** of FIG. **2**B and to FIG. **16**, a CMP process may follow the formation of the interconnects **104**.

[0040] Following the metallization of blocks **224**-**228**, the remaining portions of sacrificial layer **402** may be removed (to create air gaps **112**) either before or after forming another ILD layer over the sacrificial layer **402** and the dielectric material **110**. Blocks **230** and **232** disclose examples of removing the sacrificial layer **402** before forming the other ILD layer, whereas blocks **234** and **236** disclose examples of removing the sacrificial layer **402** after forming the other ILD layer.

[0041] Referring first to block **230** of FIG. **2**B and to FIG. **17**, the sacrificial layer **402** is removed. In some embodiments, an anneal process is used to break down the sacrificial layer **402**. In one such embodiment, the anneal process is performed at between about 200° C. and about 450° C. Other suitable methods of removing the sacrificial layer **402** include heating, UV exposure, ashing, etching, application of a solvent, and/or other methods known to one of skill in the art. The removing of the sacrificial layer **402** leaves air gaps **112** within the dielectric material **110**.

[0042] Referring to block **232** of FIG. **2**B and to FIG. **18**, a subsequent ILD material **1802** such as an etch stop layer is deposited above the dielectric material **110**. In some embodiments, the subsequent ILD material **1802** is part of a second ILD structure **106**B to be formed above the first ILD structure **106**A. The subsequent ILD material **1802** may include any suitable material including silicon dioxide, carbon-doped silicon dioxide, low-k silicon nitride, low-k silicon oxynitride, SOG, FSG, PSG, BPSG, and Black Diamond® and may be deposited using any suitable process including ALD, CVD, PECVD, HDP-CVD, PVD, spin-on deposition, and/or other suitable deposition processes. In some embodiments, the deposition method is selected to have poor gap filling properties to avoid depositing material within the air gaps **112**. Such non-conformal deposition processes include CVD, PECVD, HDP-CVD, and spin-on

coating. In an embodiment, an ILD material **1802** containing silicon nitride is deposited via CVD. In another embodiment, an ILD material **1802** containing a polymer dielectric is deposited via spin-on deposition.

[0043] In contrast, blocks **234** and **236** disclose embodiments where the sacrificial layer **402** is removed after forming other layers. Referring first to block **234** of FIG. **2**B and to FIG. **19**, a subsequent ILD material **1902** is deposited above the dielectric material **110** and the sacrificial layer **402**. In some embodiments, the subsequent ILD material **1902** is part of a second ILD structure **106**B to be formed above the first ILD structure **106**A. In an exemplary embodiment, the subsequent ILD material **1902** includes a porous etch stop layer that, in turn, may include materials such as silicon nitride, silicon oxynitride, and silicon carbide nitride. Additionally or in the alternative, the porous etch stop layer may include a low-k dielectric material such as a porous silicon dioxide, carbon doped silicon dioxide, low-k silicon nitride, low-k silicon oxynitride, SOG, FSG, PSG, BPSG, Black Diamond®, Xerogel, Aerogel, amorphous fluorinated carbon, Parylene, BCB, SiLK, other suitable low-k dielectric materials, and/or combinations thereof. The ILD material **1902** may be deposited via any suitable deposition process including CVD and/or PECVD processes.

[0044] Referring to block **236** of FIG. **2**B and to FIG. **20**, the remaining sacrificial layer **402** is removed. In some embodiments, due in part to the porosity of the subsequent ILD material **1902** and/or the dielectric material **110**, the sacrificial layer **402** material is removed without disturbing the surrounding layers. In some such embodiments, an anneal process is used to break down the sacrificial layer **402** so that it can penetrate the porous surrounding layers. In one such embodiment, the anneal process is performed at between about 200° C. and about 450° C. Other suitable methods of removing the sacrificial layer **402** include heating, UV exposure, application of a solvent, and/or other methods known to one of skill in the art. The removing of the sacrificial layer **402** leaves air gaps **112** within the dielectric material **110**.

[0045] Referring to FIG. **21**, the processes of blocks **202** through **236** may be repeated to form the second ILD structure **106**B and other subsequent ILD layers.

[0046] As disclosed above, the principles of the present disclosure can be extended to any other suitable metallization process. A further exemplary method in which the metallization includes a dual damascene process is disclosed with reference to FIG. **22** and FIGS. **23-28**. FIG. **22** is a flow diagram of the method **2200** for forming an MLI using a dual damascene process according to various aspects of the present disclosure. It is understood that additional steps can be provided before, during, and after the method **2200** and that some of the steps described can be replaced or eliminated for other embodiments of the method **2200**. FIGS. **23-28** are cross-sectional views of the MLI **2300** undergoing the method **2200** for forming the MLI **2300** using a dual damascene process according to various aspects of the present disclosure. FIGS. **23-28** have been simplified for the sake of clarity and to better illustrate the inventive concepts of the present disclosure.

[0047] Referring to block **2202** of FIG. **22** and to FIG. **23**, a substrate **102** including circuit devices **103** is received and the processes of blocks **202-216** of FIG. **2**A are performed upon the substrate **102**. Following the processes of blocks **202-216**, the substrate **102** includes an ILD structure **106**A comprising regions of dielectric material **110** separated by regions of a sacrificial layer **402**. Each element may be substantially similar to those disclosed with respect to FIGS. **1-10**. Referring to block **2204** of FIG. **22** and to FIG. **24**, a dual damascene metallization is performed on the substrate **102**.

[0048] One of skill in the art will recognize that the principles of the present disclosure apply to any suitable dual damascene metallization process. However, an exemplary process includes forming a photoresist over the dielectric material **110** and the sacrificial layer **402**. The photoresist coating is patterned to define via-type interconnects, and a via-etching process is performed. The photoresist coating may be removed following the via-etching process. A second photoresist coating is then deposited and patterned, and the dielectric material **110** and the sacrificial layer **402** are patterned to define trenches for trace-type interconnects. This may be referred to as a trench patterning. In some such processes, a barrier layer **1402** and/or seed layer each substantially similar to those disclosed with respect to FIG. **14** may be formed. A conductive material is then deposited. A CMP process may follow the deposition of the conductive material.

[0049] Following the metallization of block **2204**, the sacrificial layer **402** may be removed (to create air gaps **112**) either before or after forming another ILD layer over the sacrificial layer **402** and the dielectric material **110**. Blocks **2206** and **2208** disclose examples of removing the sacrificial layer **402** before forming the other ILD layer, whereas blocks **2208** and **2210** disclose examples of removing the sacrificial layer **402** after forming the other ILD layer.

[0050] Referring first to block **2206** of FIG. **22** and to FIG. **25**, the sacrificial layer **402** is removed. In some embodiments, an anneal process is used to break down the sacrificial layer **402**. In one such embodiment, the anneal process is performed at between about 200° C. and about 450° C. Other suitable methods of removing the sacrificial layer **402** include heating, UV exposure, ashing, etching, application of a solvent, and/or other methods known to one of skill in the art. The removing of the sacrificial layer **402** leaves air gaps **112** within the dielectric material **110**.

[0051] Referring to block **2208** of FIG. **22** and to FIG. **26**, a subsequent ILD material **1802** such as an etch stop layer is deposited above the dielectric material **110**. In some embodiments, the subsequent ILD material **1802** is part of a second ILD structure **106**B to be formed above the first ILD structure **106**A. The subsequent ILD material **1802** may be substantially similar to ILD material **1802** of FIG. **18** and may include any suitable material including silicon dioxide, carbon doped silicon dioxide, low-k silicon nitride, low-k silicon oxynitride, SOG, FSG, PSG, BPSG, and/or Black Diamond®. ILD material **1802** may be deposited using any suitable process including ALD, CVD, HDP-CVD, PVD, spin-on deposition, and/or other suitable deposition processes. In some embodiments, the deposition method is selected to have poor gap filling properties to avoid depositing material within the air gaps **112**. Such non-conformal deposition processes include CVD, PECVD, HDP-CVD, and spin-on coating. In an embodiment, an ILD material **1802** containing silicon nitride is deposited via CVD. In another embodiment, an ILD material **1802** containing a polymer dielectric is deposited via spin-on deposition.

[0052] In contrast, blocks **2210** and **2212** of FIG. **22** disclose embodiments where the sacrificial layer **402** is

removed after forming other layers. Referring first to block **2210** of FIG. **22** and to FIG. **27**, a subsequent ILD material **1902** is deposited above the dielectric material **110** and the sacrificial layer **402**. In some embodiments, the subsequent ILD material **1902** is part of a second ILD structure **106**B to be formed above the first ILD structure **106**A. The subsequent ILD material **1902** may be substantially similar to ILD material **1902** of FIG. **19**. In an exemplary embodiment, the subsequent ILD material **1902** includes a porous etch stop layer and is deposited via a suitable deposition process such as CVD and/or PECVD.

[0053] Referring to block **2212** of FIG. **22** and to FIG. **28**, the remaining sacrificial layer **402** is removed. In some embodiments, due in part to the porosity of the subsequent ILD material **1902** and/or the dielectric material **110**, the sacrificial layer **402** material is removed without disturbing the surrounding layers. In some such embodiments, an anneal process is used to break down the sacrificial layer **402** so that it can penetrate the porous surrounding layers. In one such embodiment, the anneal process is performed at between about 200° C. and about 450° C. Other suitable methods of removing the sacrificial layer **402** include heating, UV exposure, application of a solvent, and/or other methods known to one of skill in the art. The removing of the sacrificial layer **402** leaves air gaps **112** within the dielectric material **110**.

[0054] The processes of blocks **2202** through **2212** may be repeated to form the second ILD structure **106**B and other subsequent ILD layers.

[0055] A further exemplary process where metallization includes depositing and etching a conductive material to form interconnects **104** is disclosed with reference to FIG. **29** and FIGS. **30-35**. FIG. **29** is a flow diagram of the method **2900** for forming an MLI using conductor etching according to various aspects of the present disclosure. It is understood that additional steps can be provided before, during, and after the method **2900** and that some of the steps described can be replaced or eliminated for other embodiments of the method **2900**. FIGS. **30-35** are cross-sectional views of an MLI **3000** undergoing the method **2900** for forming the MLI **3000** using conductor etching according to various aspects of the present disclosure. FIGS. **30-35** have been simplified for the sake of clarity and to better illustrate the inventive concepts of the present disclosure.

[0056] Referring to block **2902** of FIG. **29** and to FIG. **30**, a substrate **102** including circuit devices **103** is received and the processes of blocks **202-216** of FIG. **2**A are performed upon the substrate **102**. Following the processes of blocks **202-216**, the substrate **102** includes an ILD structure **106**A comprising regions of dielectric material **110** separated by regions of a sacrificial layer **402**. Each element may be substantially similar to those disclosed with respect to FIGS. **1-10**. Referring to block **2904** of FIG. **29** and to FIG. **31**, a metallization process is performed on the substrate **102**.

[0057] An exemplary metallization process that incorporates conductor etching includes forming a photoresist over the dielectric material **110** and the sacrificial layer **402**. The photoresist coating is patterned to define interconnects **104** such as conductive traces, vias, bonding pads, and/or other conductive structures. An etching is performed using the patterned photoresist, which may be removed following the etching process. In some such processes, a barrier layer **1402** and/or seed layer each substantially similar to those disclosed with respect to FIG. **14** may be formed. A conductive material is then deposited. The conductive material may fill the etched trenches and may extend above an upper surface of the ILD structure **106**A. A second photoresist is formed on the conductive material and patterned to further define the interconnects **104**. A second etching process using the patterned second photoresist is performed to etch the conductive material including the portions formed above the upper surface of the ILD **106**A. This etching separates and further defines the interconnects **104**.

[0058] Following the metallization of block **2904**, the sacrificial layer **402** may be removed (to create air gaps **112**) either before or after forming another ILD layer over the sacrificial layer **402** and the dielectric material **110**. Blocks **2906** and **2908** disclose examples of removing the sacrificial layer **402** before forming the other ILD layer, whereas blocks **2908** and **2910** disclose examples of removing the sacrificial layer **402** after forming the other ILD layer.

[0059] Referring first to block **2906** of FIG. **29** and to FIG. **32**, the sacrificial layer **402** is removed. In some embodiments, an anneal process is used to break down the sacrificial layer **402**. In one such embodiment, the anneal process is performed at between about 200° C. and about 450° C. Other suitable methods of removing the sacrificial layer **402** include heating, UV exposure, ashing, etching, application of a solvent, and/or other methods known to one of skill in the art. The removing of the sacrificial layer **402** leaves air gaps **112** within the dielectric material **110**.

[0060] Referring to block **2908** of FIG. **29** and to FIG. **33**, a subsequent ILD material **1802** such as an etch stop layer is deposited above the dielectric material **110**. In some embodiments, the subsequent ILD material **1802** is part of a second ILD structure **106**B to be formed above the first ILD structure **106**A. The subsequent ILD material **1802** may be substantially similar to ILD material **1802** of FIG. **18** and may include any suitable material including silicon dioxide, carbon doped silicon dioxide, low-k silicon nitride, low-k silicon oxynitride, SOG, FSG, PSG, BPSG, and/or Black Diamond®. ILD material **1802** may be deposited using any suitable process including ALD, CVD, HDP-CVD, PVD, spin-on deposition, and/or other suitable deposition processes. In some embodiments, the deposition method is selected to have poor gap filling properties to avoid depositing material within the air gaps **112**. Such non-conformal deposition processes include CVD, PECVD, HDP-CVD, and spin-on coating. In an embodiment, an ILD material **1802** containing silicon nitride is deposited via CVD. In another embodiment, an ILD material **1802** containing a polymer dielectric is deposited via spin-on deposition.

[0061] In contrast, blocks **2910** and **2912** of FIG. **29** disclose embodiments where the sacrificial layer **402** is removed after forming other layers. Referring first to block **2910** of FIG. **29** and to FIG. **34**, a subsequent ILD material **1902** is deposited above the dielectric material **110** and the sacrificial layer **402**. In some embodiments, the subsequent ILD material **1902** is part of a second ILD structure **106**B to be formed above the first ILD structure **106**A. The subsequent ILD material **1902** may be substantially similar to ILD material **1902** of FIG. **19**. In an exemplary embodiment, the subsequent ILD material **1902** includes a porous etch stop layer and is deposited via any suitable deposition process including CVD and/or PECVD.

[0062] Referring to block **2912** of FIG. **29** and to FIG. **35**, the remaining sacrificial layer **402** is removed. In some embodiments, due in part to the porosity of the subsequent

ILD material **1902** and/or the dielectric material **110**, the sacrificial layer **402** material is removed without disturbing the surrounding layers. In some such embodiments, an anneal process is used to break down the sacrificial layer **402** so that it can penetrate the porous surrounding layers. In one such embodiment, the anneal process is performed at between about 200° C. and about 450° C. Other suitable methods of removing the sacrificial layer **402** include heating, UV exposure, application of a solvent, and/or other methods known to one of skill in the art. The removing of the sacrificial layer **402** leaves air gaps **112** within the dielectric material **110**.

[0063] The processes of blocks **2902** through **2912** may be repeated to form the second ILD structure **106**B and other subsequent ILD layers.

[0064] Thus, the present disclosure provides a circuit device having an interlayer dielectric with pillar-type air gaps and a method of forming the circuit device. In some embodiments, a method for forming an interconnect structure device is provided. The method comprises: receiving a substrate; depositing a first layer over the substrate; forming a copolymer layer over the first layer, wherein the copolymer layer includes a first constituent polymer and a second constituent polymer; selectively removing the first constituent polymer from the copolymer layer; etching a first region of the first layer corresponding to the selectively removed first constituent polymer, wherein the etching leaves a second region of the first layer underlying the second constituent polymer unetched; performing a metallization process on the etched substrate; and removing the first layer from the second region to form an air gap.

[0065] In further embodiments, a method of fabricating an interconnect structure is provided. The method comprises: receiving a substrate; depositing a sacrificial layer over the substrate; depositing a copolymer material over the sacrificial layer, wherein the copolymer material is directed self-assembling; inducing microphase separation within the copolymer material, wherein the inducing of the microphase separation defines a first region and a second region; selectively etching the sacrificial layer within the first region; depositing a dielectric material within the first region to define an interlayer dielectric structure; and removing the sacrificial layer from the second region to form an air gap within the interlayer dielectric structure.

[0066] In yet further embodiments, an interconnect structure is provided. The interconnect structure comprises: a substrate having a circuit device formed thereupon; and an interlayer dielectric structure formed over the substrate, the interlayer dielectric structure including an interlayer dielectric and an interconnect electrically coupled to the circuit device, wherein the interlayer dielectric structure further includes a pillar-type air gap formed therein.

[0067] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method of forming an interconnect structure, the method comprising:

forming a sacrificial layer;

forming a directed self-assembly (DSA) material layer over the sacrificial layer, wherein the DSA material layer includes first DSA material portions having a first composition and second DSA material portions having a second composition, wherein the first composition is different than the second composition;

selectively removing the second DSA material portions with respect to the first DSA material portions to form a etch mask;

etching the sacrificial layer using the etch mask, wherein the etching forms openings within the sacrificial layer that expose an underlying layer;

filling the openings within the sacrificial layer with a dielectric material, wherein the dielectric material and the etched sacrificial layer form an interconnect dielectric layer; and

after forming an interconnect in the interconnect dielectric layer, removing the etched sacrificial layer to form air gaps, wherein the interconnect dielectric layer includes the dielectric material and the air gaps within the dielectric material.

2. The method of claim **1**, wherein the forming the DSA material layer includes:

forming a copolymer layer that includes polystyrene and polymethyl methacrylate (PMMA) over the sacrificial layer; and

annealing the copolymer layer to cause segregation of polystyrene and PMMA, wherein the first DSA material portions having the first composition are polystyrene portions and the second DSA material portions having the second composition are PMMA portions.

3. The method of claim **2**, wherein the selectively removing the second DSA material portions with respect to the first DSA material portions includes performing an O_2 plasma etch to selectively remove the PMMA portions.

4. The method of claim **2**, wherein the forming the copolymer layer that includes polystyrene and PMMA includes performing a spin-coating process.

5. The method of claim **1**, further comprising performing an annealing to remove the etched sacrificial layer to form the air gaps of the interconnect dielectric layer.

6. The method of claim **1**, wherein the sacrificial layer is a first sacrificial layer, the DSA material layer is a first DSA material layer, the etch mask is a first etch mask, the openings are first openings, the dielectric material is a first dielectric material, the interconnect dielectric layer is a first interconnect dielectric layer, the interconnect is a first interconnect, the air gaps are first air gaps, and the method further includes:

forming a second sacrificial layer over the first interconnect dielectric layer;

forming a second DSA material layer over the second sacrificial layer, wherein the second DSA material layer includes third DSA material portions having a third composition and fourth DSA material portions having a fourth composition, wherein the third composition is different than the fourth composition;

selectively removing the fourth DSA material portions with respect to the third DSA material portions to form a second etch mask and etching the second sacrificial layer using the second etch mask, wherein the etching forms second openings within the second sacrificial layer that expose the first interconnect dielectric layer;

filling the second openings within the second sacrificial layer with a second dielectric material, wherein the second dielectric material and the etched second sacrificial layer form a second interconnect dielectric layer; and

after forming a second interconnect in the second interconnect dielectric layer, removing the etched second sacrificial layer to form second air gaps, wherein the second interconnect dielectric layer includes the second dielectric material and the second air gaps within the second dielectric material and the second interconnect is disposed on the first interconnect.

7. The method of claim **6**, wherein at least one of the second air gaps at least partially overlaps a respective one of the first air gaps.

8. The method of claim **1**, wherein:

the forming the interconnect in the interconnect dielectric layer includes forming a first portion of the interconnect and a second portion of the interconnect in the interconnect dielectric layer, wherein the first portion has a first width, the second portion has a second width, and the second width is greater than the first width; and

the method further includes forming a dielectric layer over the interconnect dielectric layer after forming the interconnect in the interconnect dielectric layer.

9. The method of claim **1**, wherein:

the forming the interconnect in the interconnect dielectric layer includes forming a first portion of the interconnect in the interconnect dielectric layer and a second portion of the interconnect over the interconnect dielectric layer, wherein the first portion has a first width, the second portion has a second width, and the second width is greater than the first width; and

the method further includes forming a dielectric layer over the interconnect dielectric layer after forming the interconnect in the interconnect dielectric layer.

10. The method of claim **1**, wherein the underlying layer is a device layer, the interconnect is a connected to a device of the device layer, and at least a substrate of the device layer is exposed by the openings within the sacrificial layer.

11. The method of claim **10**, wherein a portion of the device of the device layer is exposed by the openings within the sacrificial layer.

12. A method of forming an interconnect structure, the method comprising:

forming a sacrificial layer;

forming a hard mask layer over the sacrificial layer;

forming a directed self-assembly (DSA) material layer over the hard mask layer, wherein the DSA material layer includes first DSA material portions and second DSA material portions;

selectively removing the second DSA material portions with respect to the first DSA material portions to form a patterned DSA material layer;

etching the hard mask layer using the patterned DSA material layer, wherein the etching forms a patterned hard mask layer over the sacrificial layer;

etching the sacrificial layer using the patterned hard mask layer, wherein the etching forms a patterned sacrificial layer having first openings therein that expose an underlying layer;

filling the first openings of the patterned sacrificial layer with a dielectric material, wherein the dielectric material filling the first openings forms a patterned dielectric layer;

after removing the patterned DSA material layer and the patterned hard mask layer, forming a patterned mask layer over the patterned sacrificial layer and the patterned dielectric layer, wherein the patterned mask layer has at least one second opening that exposes a portion of the patterned sacrificial layer and a portion of the patterned dielectric layer;

etching the exposed portion of the patterned sacrificial layer and the exposed portion of the patterned dielectric layer using the patterned mask layer to form an interconnect opening; and

after forming an electrically conductive material in the interconnect opening, selectively removing the patterned sacrificial layer to form air gaps within the patterned dielectric layer.

13. The method of claim **12**, further comprising forming an etch stop layer over the electrically conductive material, the patterned sacrificial layer, and the patterned dielectric layer before selectively removing the patterned sacrificial layer.

14. The method of claim **12**, wherein the filling the first openings of the patterned sacrificial layer with the dielectric material includes:

depositing the dielectric material over a top of the patterned sacrificial layer and within the first openings of the patterned sacrificial layer; and

performing a planarization process that removes the dielectric material from over the top of the patterned sacrificial layer, wherein the planarization process further removes the patterned hard mask layer.

15. The method of claim **12**, wherein the selectively removing the patterned sacrificial layer to form air gaps within the patterned dielectric layer includes annealing.

16. The method of claim **12**, wherein the selectively removing the patterned sacrificial layer to form air gaps within the patterned dielectric layer includes UV treatment.

17. The method of claim **12**, wherein the interconnect opening is a single damascene opening, and the electrically conductive material provides a single damascene interconnect.

18. The method of claim **12**, wherein the interconnect opening is a dual damascene opening, and the electrically conductive material provides a dual damascene interconnect.

19. A method of forming an interconnect structure, the method comprising:

forming a sacrificial layer having a first thickness;

forming a directed self-assembly (DSA) material layer over the sacrificial layer, wherein the DSA material layer includes first DSA material portions and second DSA material portions;

selectively removing the second DSA material portions with respect to the first DSA material portions to form a patterned DSA material layer;

selectively removing a portion of the sacrificial layer using the patterned DSA material layer to form a

patterned sacrificial layer, wherein the patterned sacrificial layer has openings therein having a first height that is equal to the first thickness;

filling the openings within the patterned sacrificial layer with a dielectric material, wherein the dielectric material filling the openings within the patterned sacrificial layer forms a patterned dielectric layer having a second thickness equal to the first thickness; and

after replacing a portion of the patterned sacrificial layer and a portion of the patterned dielectric layer with an interconnect, selectively removing a remaining portion of the patterned sacrificial layer to form air gaps, wherein the interconnect is disposed in a remaining portion of the patterned dielectric layer.

20. The method of claim **19**, further comprising forming a dielectric cap over the air gaps, the patterned dielectric layer, and the interconnect, wherein a composition of the dielectric cap is different than a composition of the patterned dielectric layer.

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