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(54) **SEMICONDUCTOR DEVICES INCLUDING GATE SPACER**

Publication Classification

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(63) Continuation of application No. 18/483,413, filed on Oct. 9, 2023, now Pat. No. 12,310,079, which is a continuation of application No. 17/060,193, filed on Oct. 1, 2020, now Pat. No. 11,810,964.

Foreign Application Priority Data

Apr. 7, 2020 (KR) 10-2020-0042140

(57)

ABSTRACT

A semiconductor device includes a first active region defined on a substrate, a first gate electrode across the first active region, a first drain region in the first active region at a position adjacent to the first gate electrode, an undercut region between the first active region and the first gate electrode, and a first gate spacer on a side surface of the first gate electrode and extending into the undercut region.

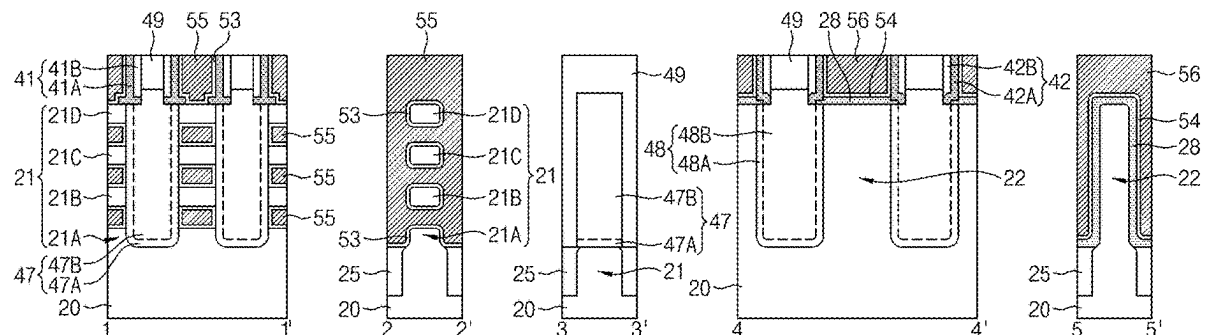


FIG. 1

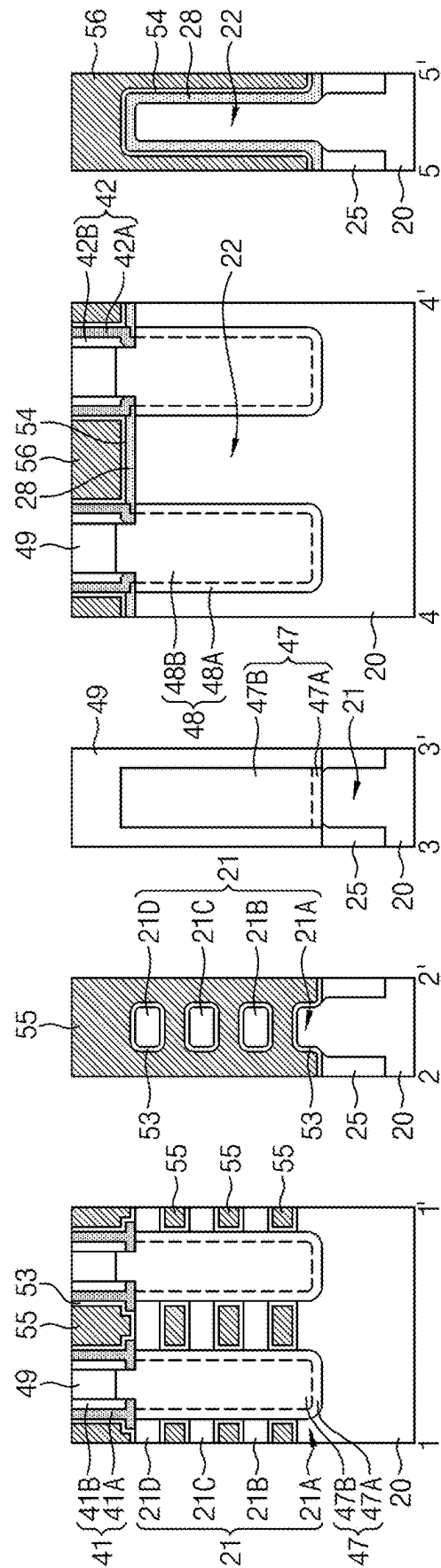


FIG. 2

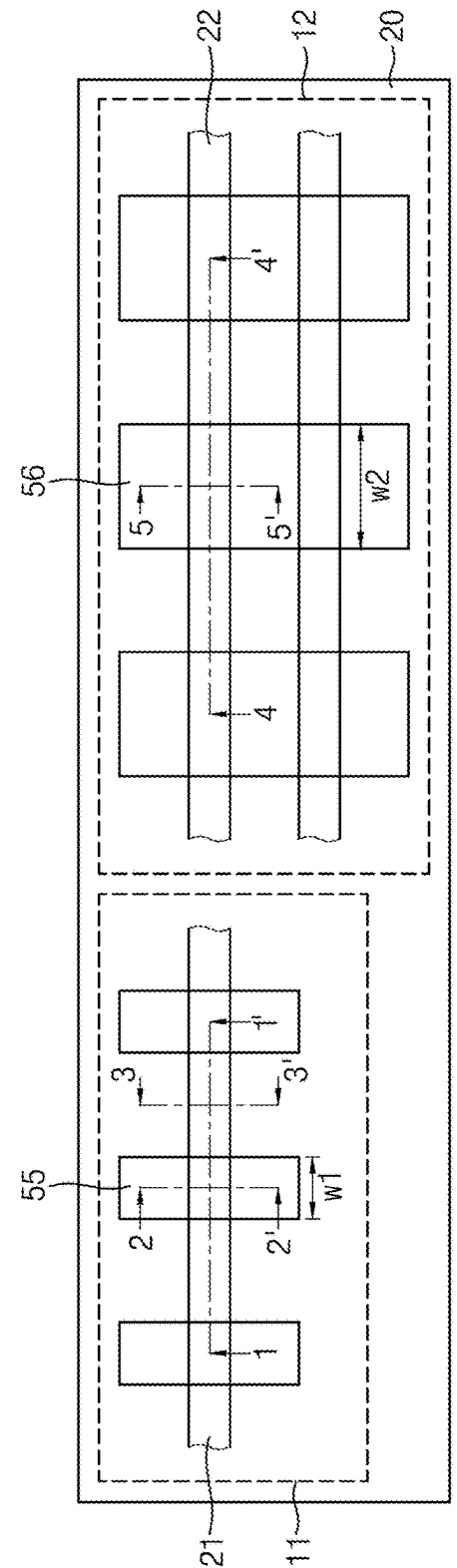


FIG. 3

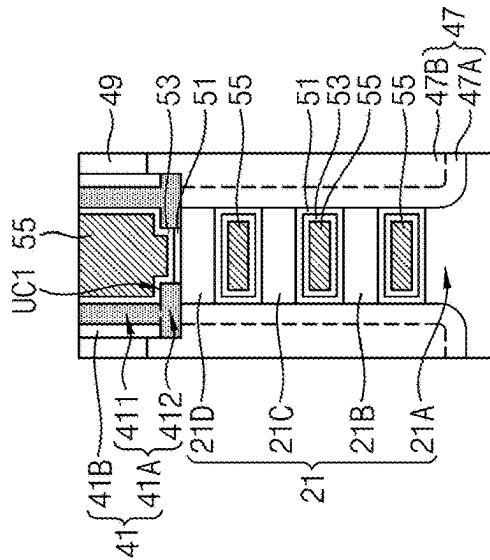


FIG. 4

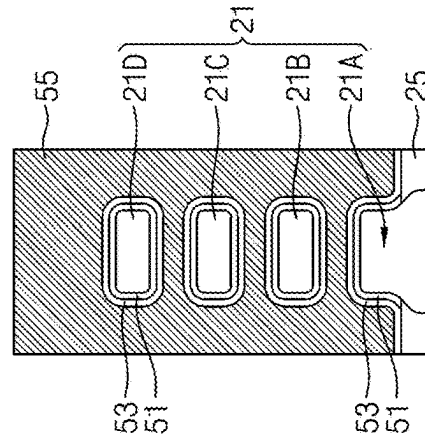


FIG. 5

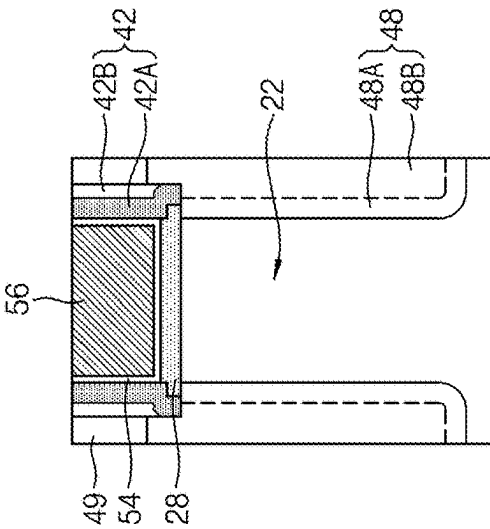


FIG. 6

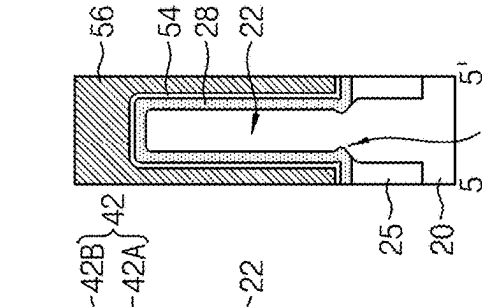
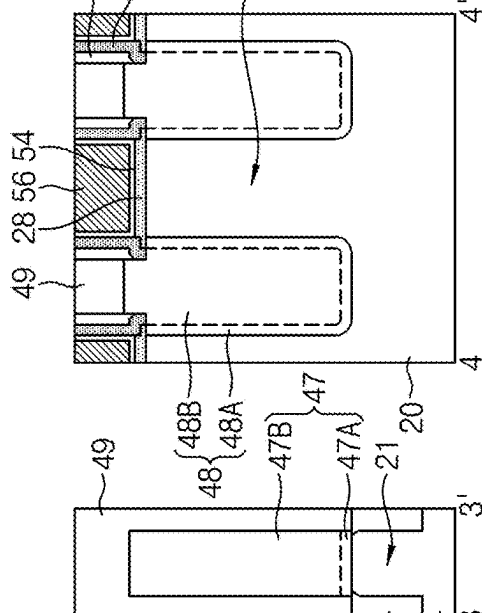
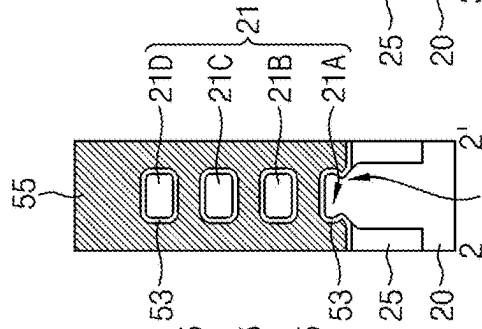
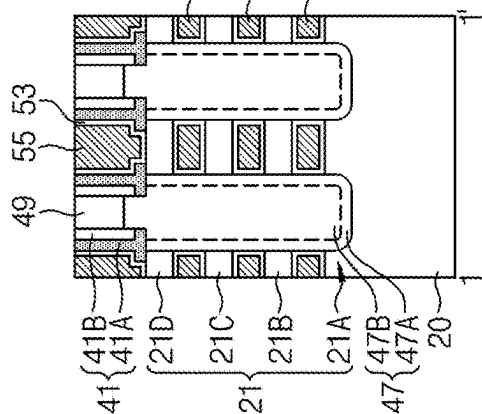
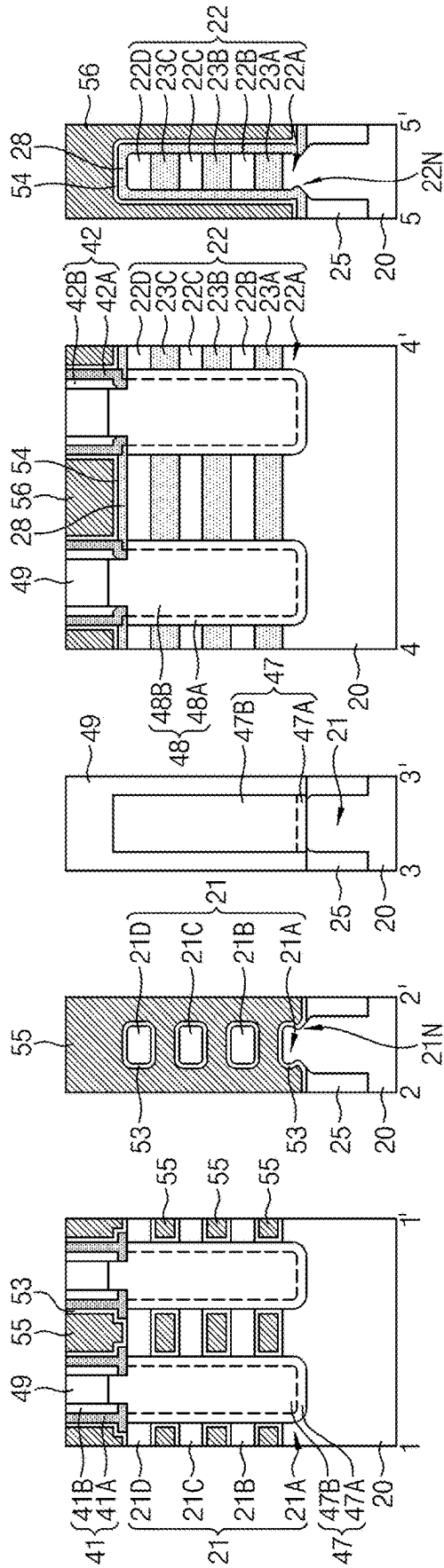


FIG. 7



854

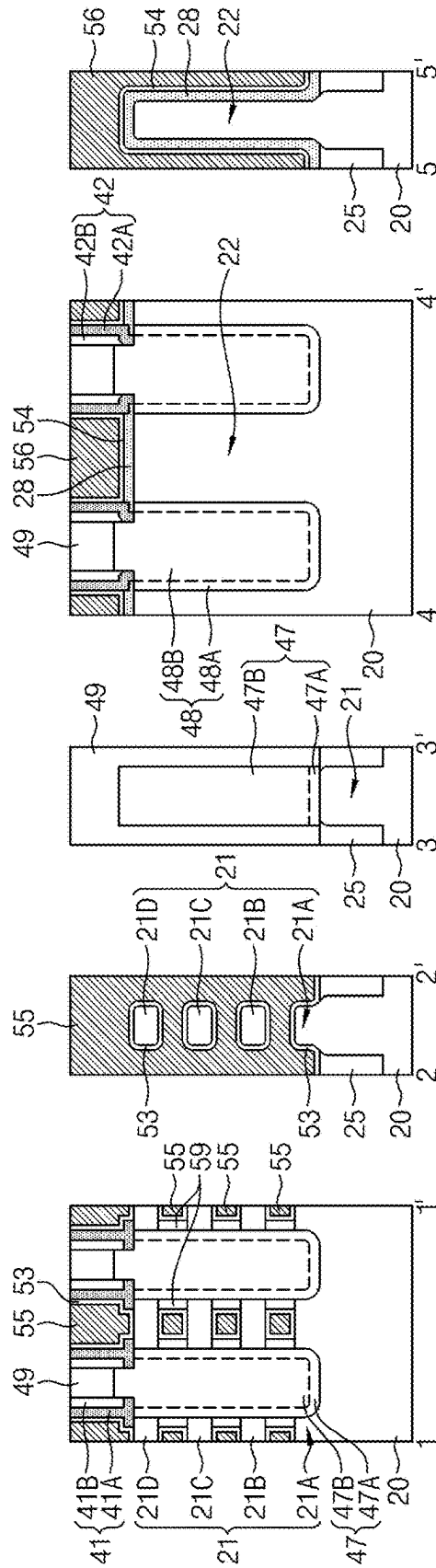


FIG. 9

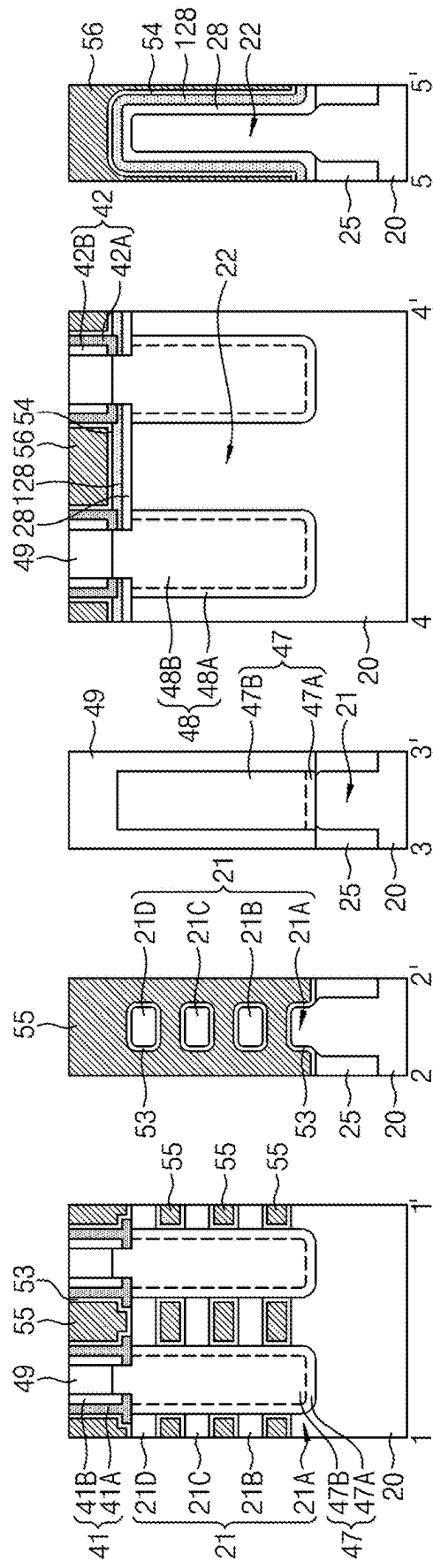


FIG. 10

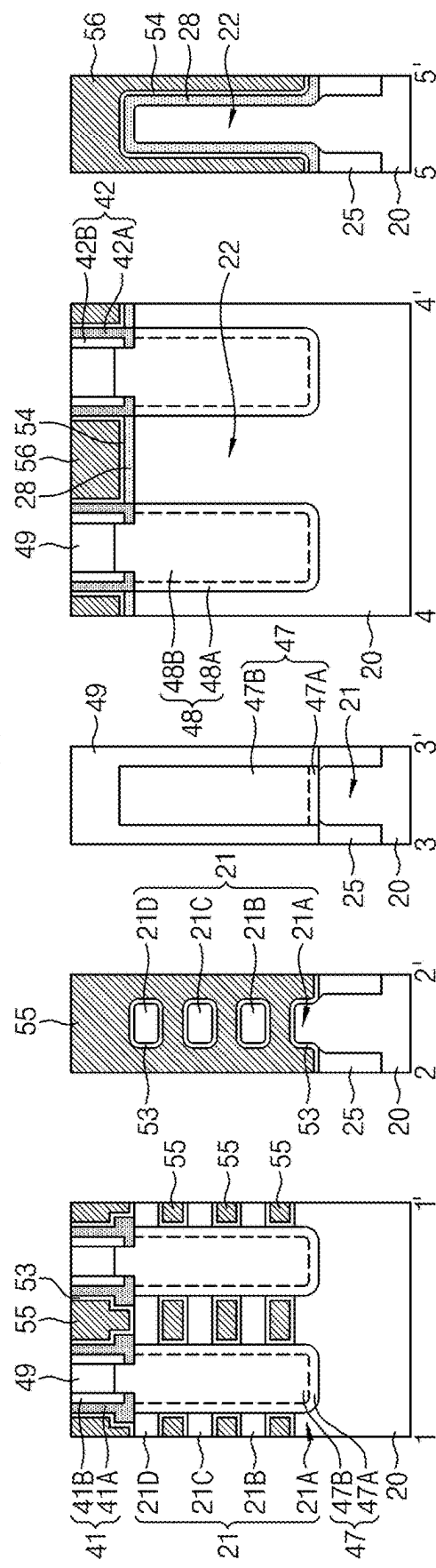


FIG. 11

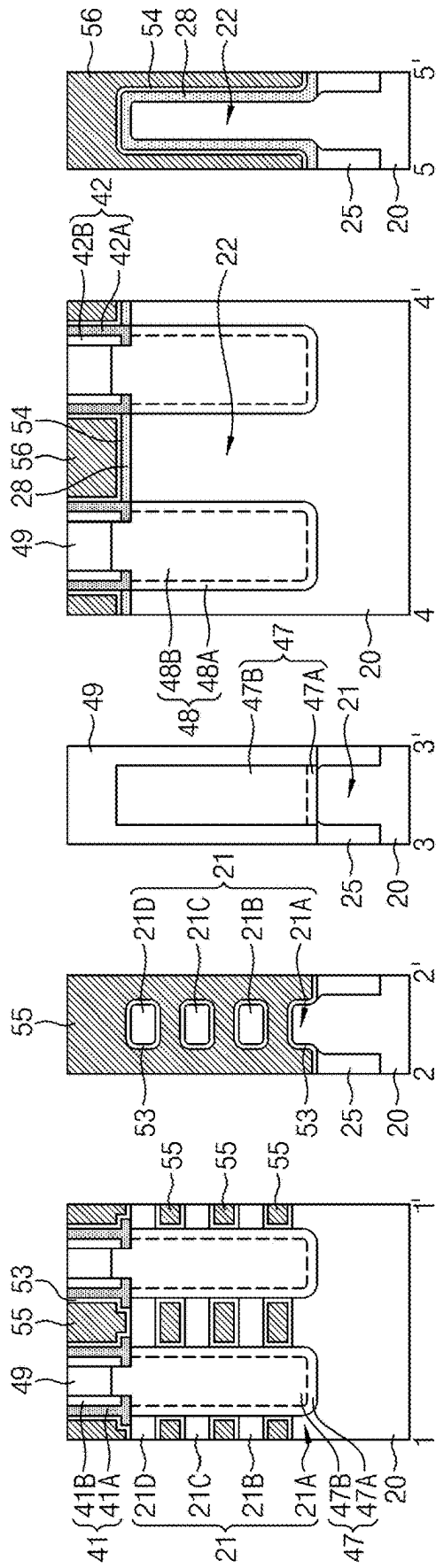


FIG. 12

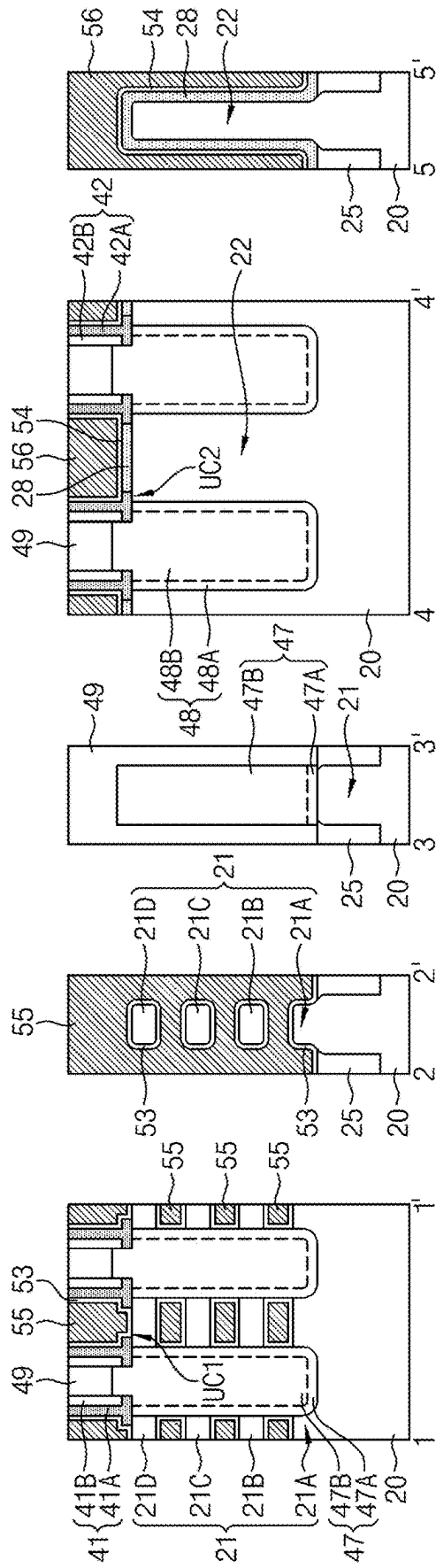


FIG. 13

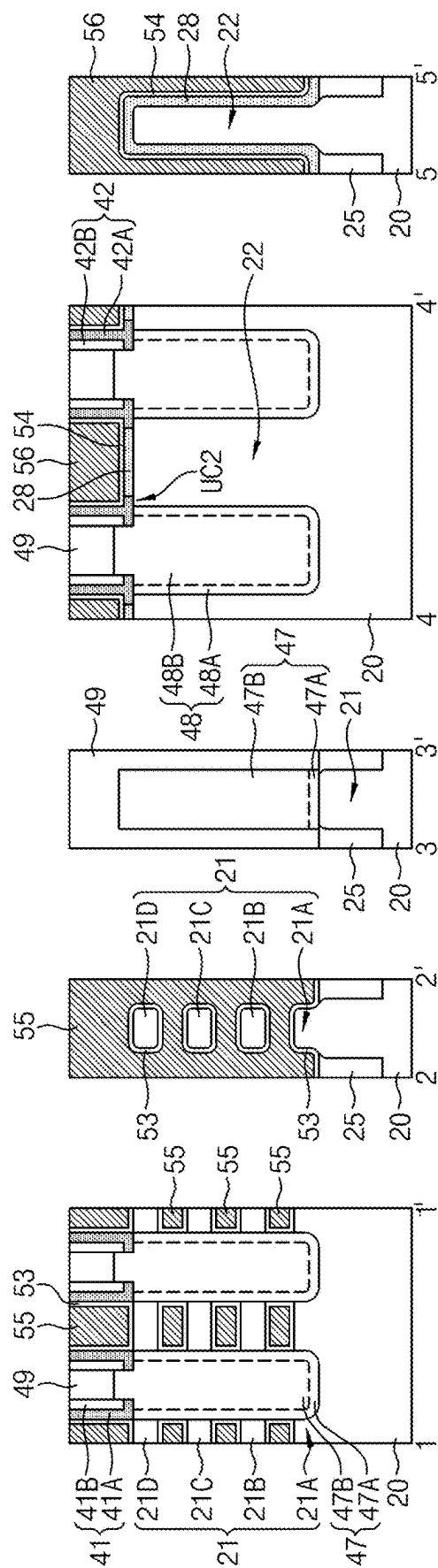


FIG. 14

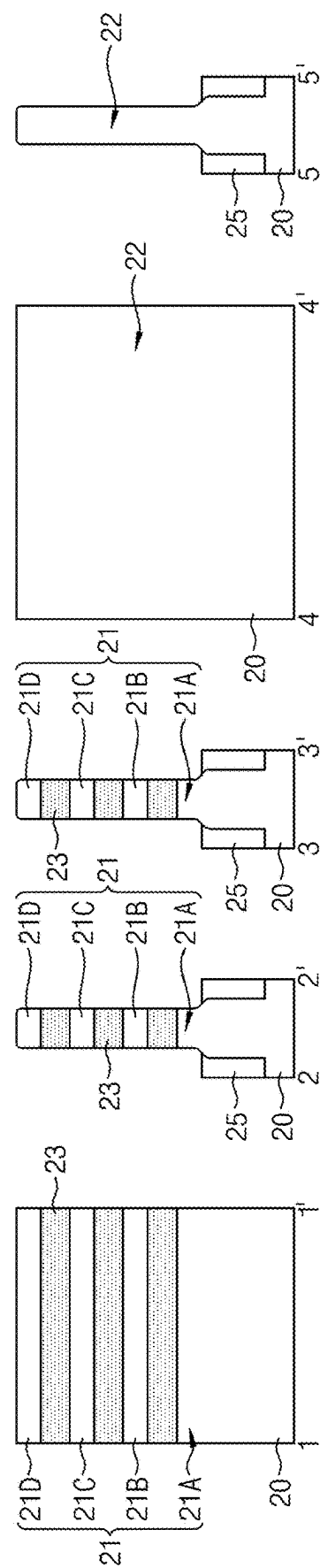


FIG. 15

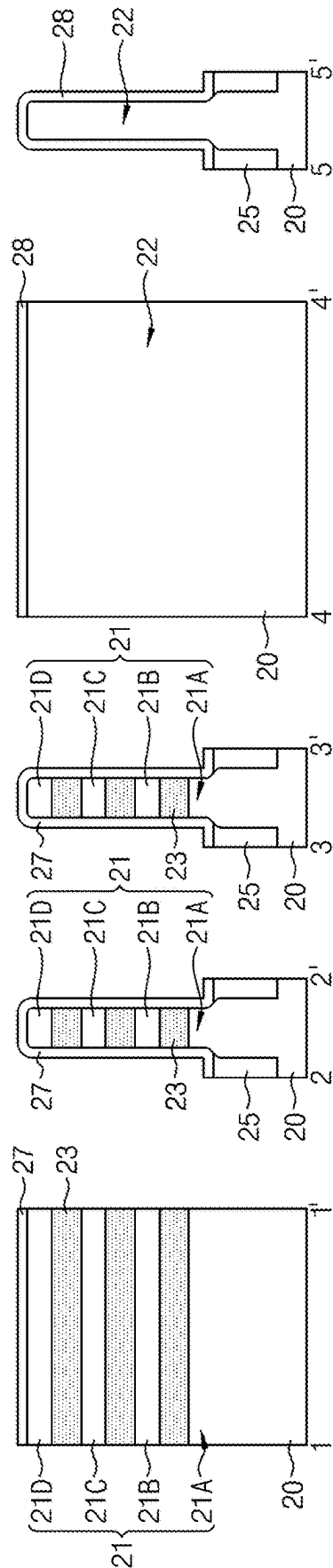


FIG. 16

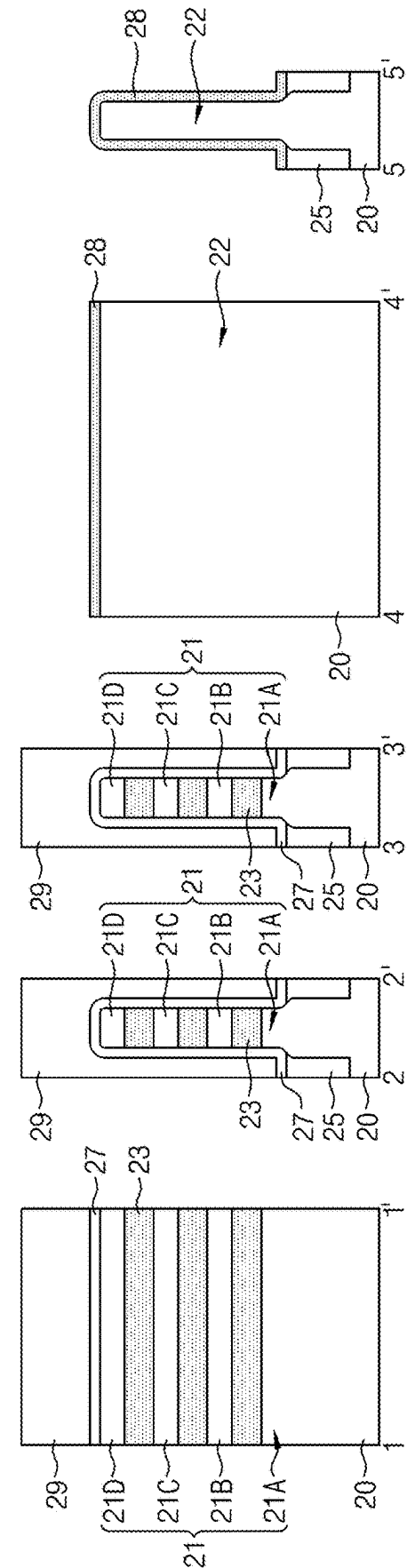


FIG. 17

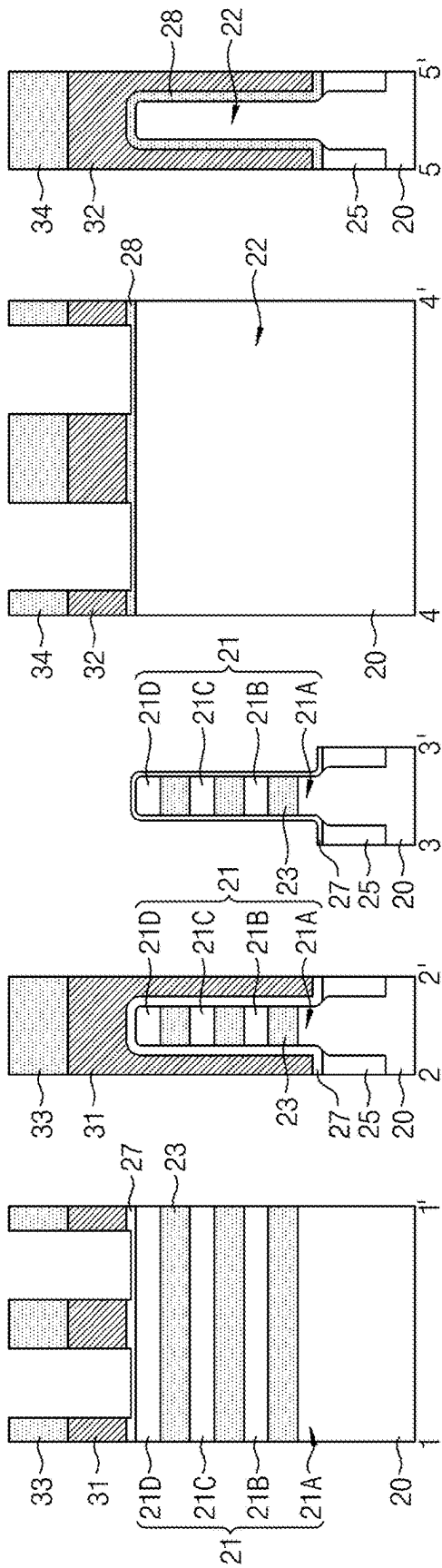
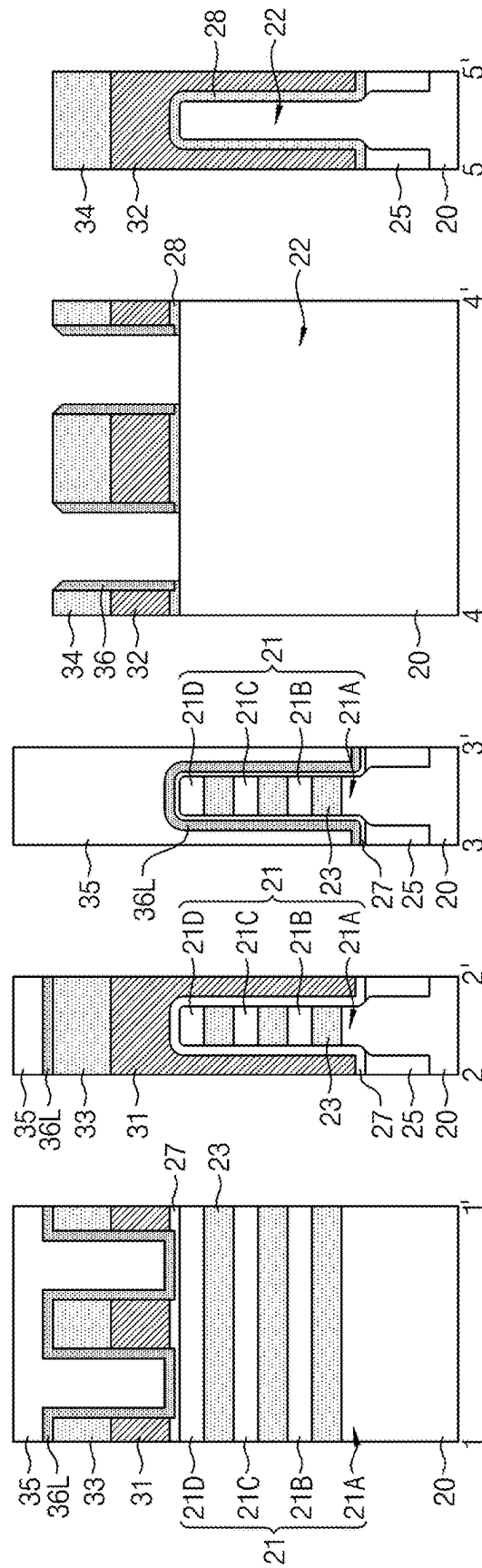


FIG. 18



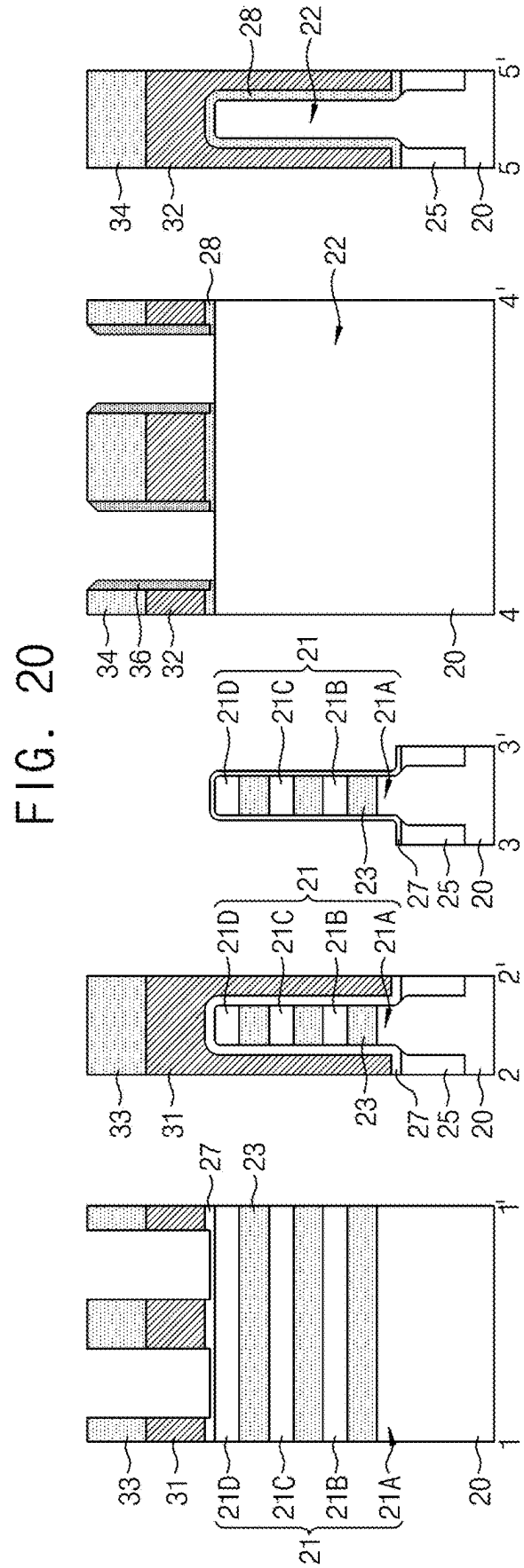
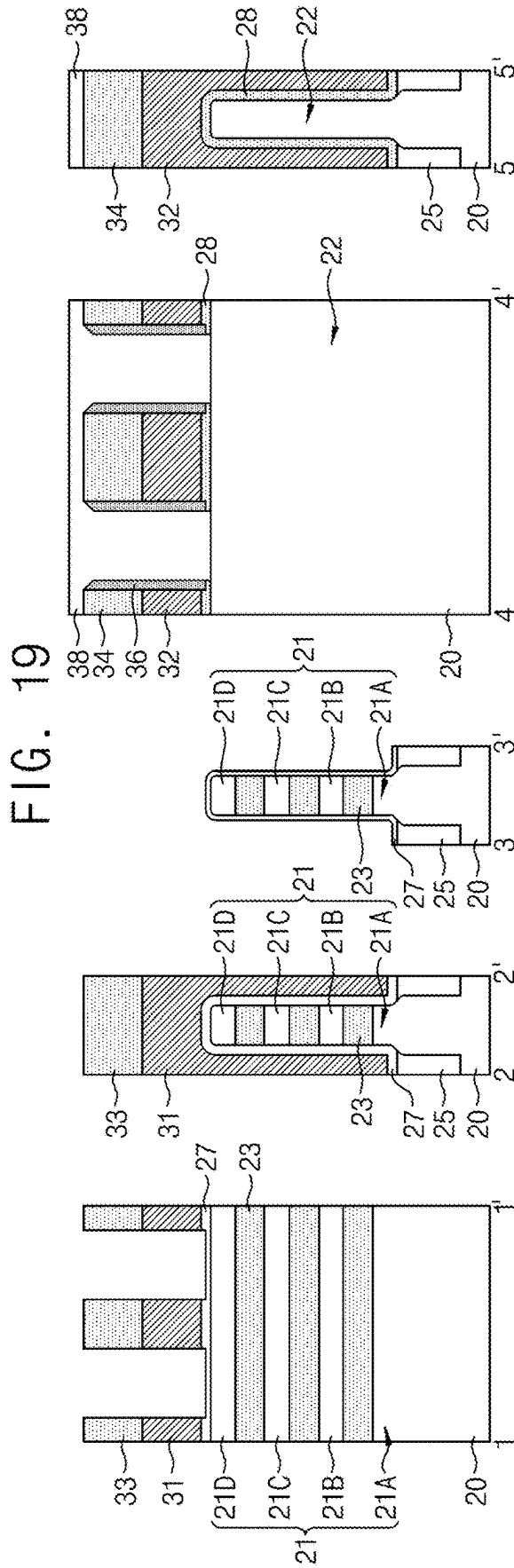


FIG. 21

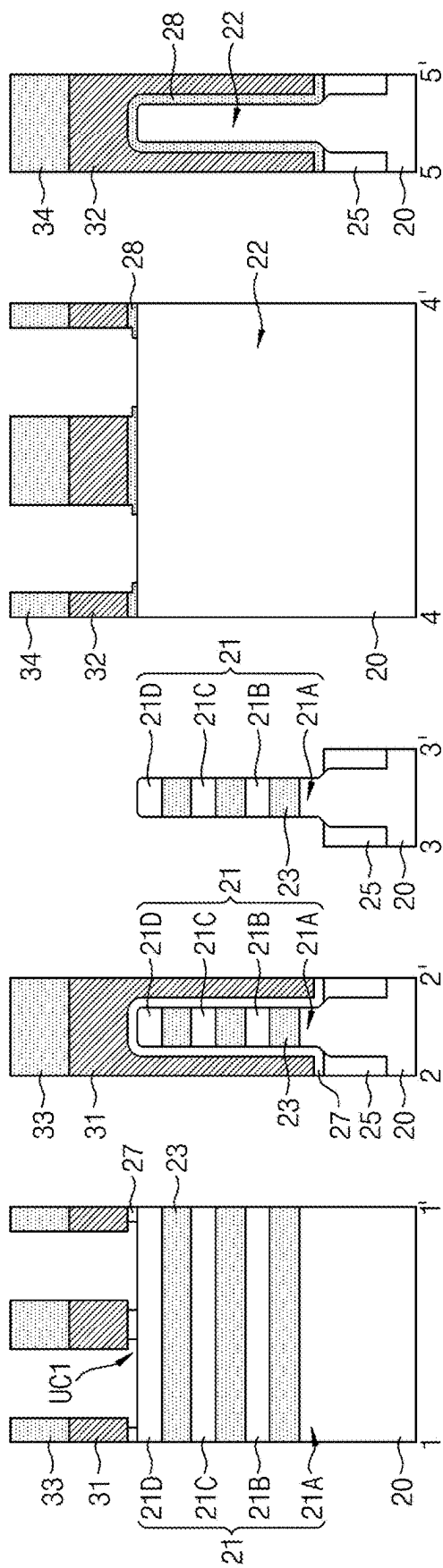


FIG. 22

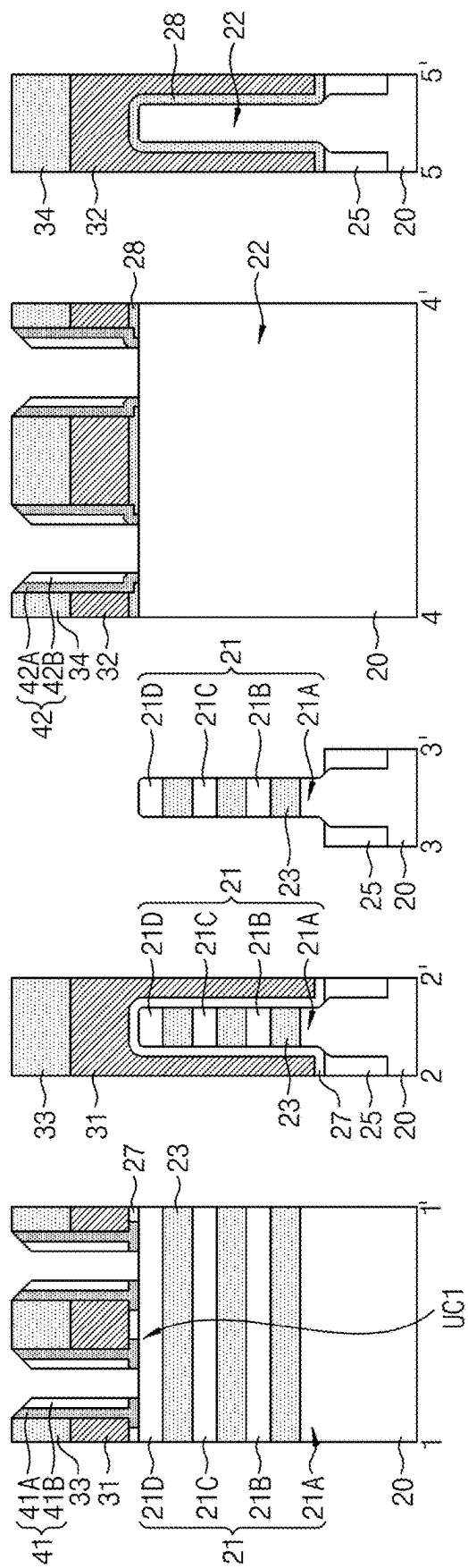


FIG. 23

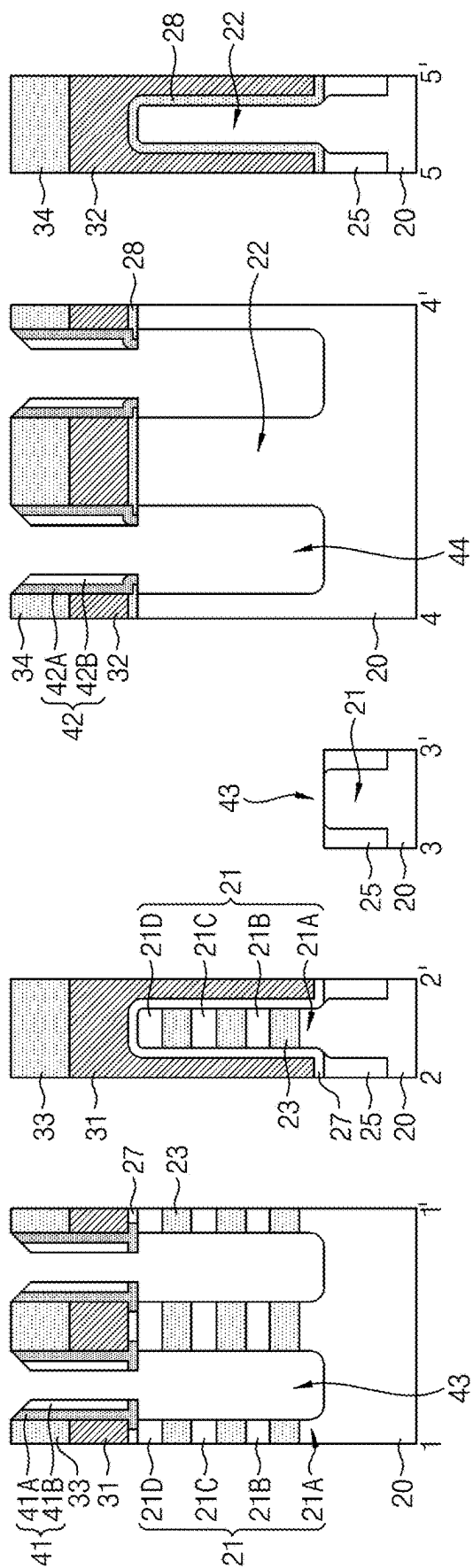


FIG. 24

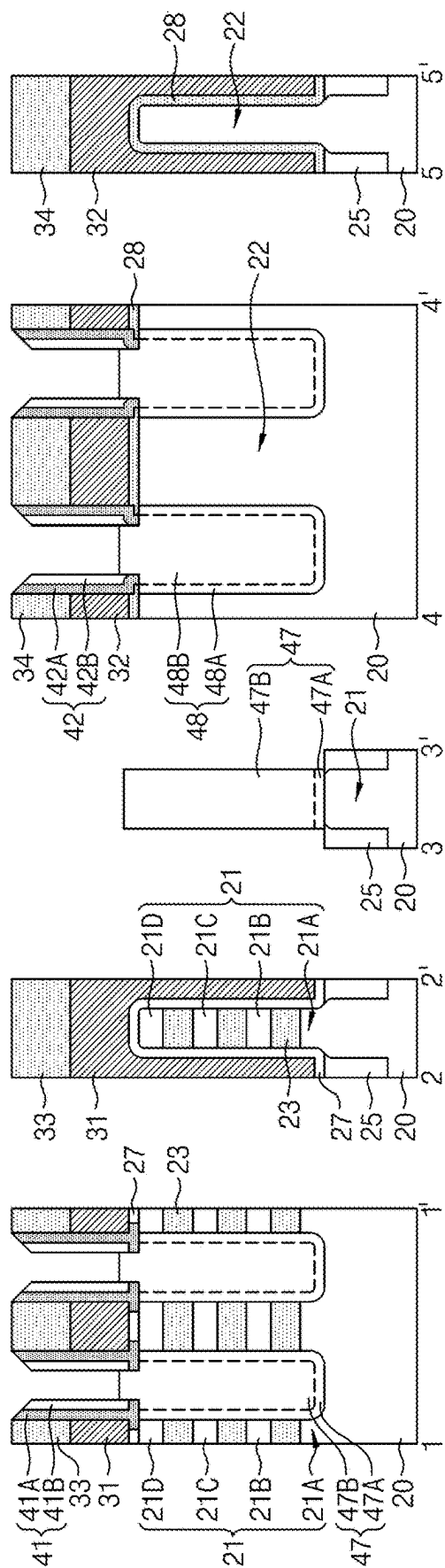


FIG. 25

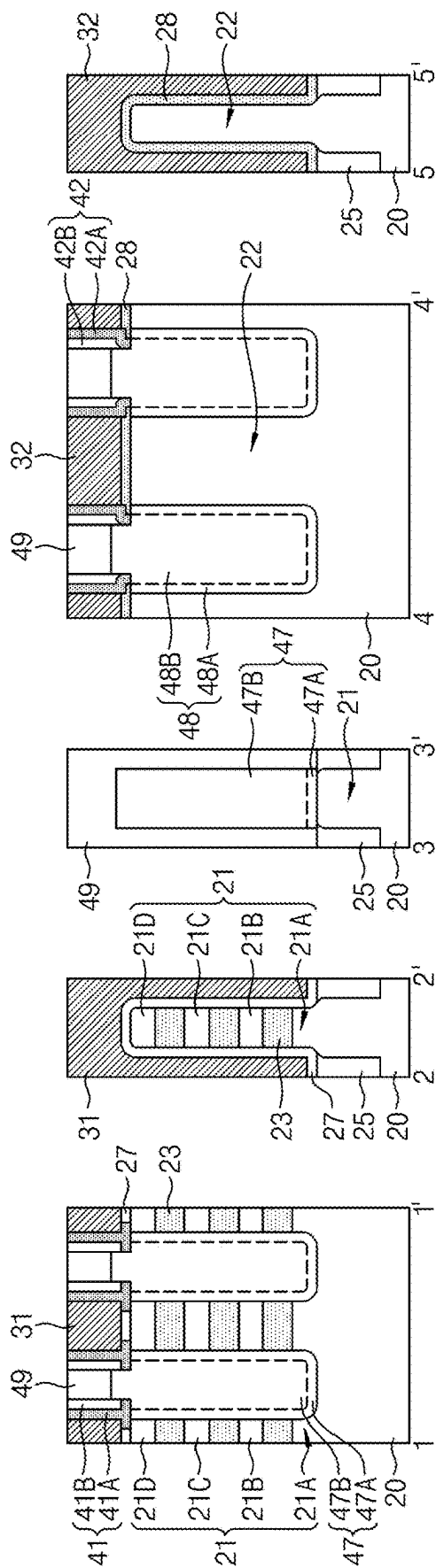


FIG. 26

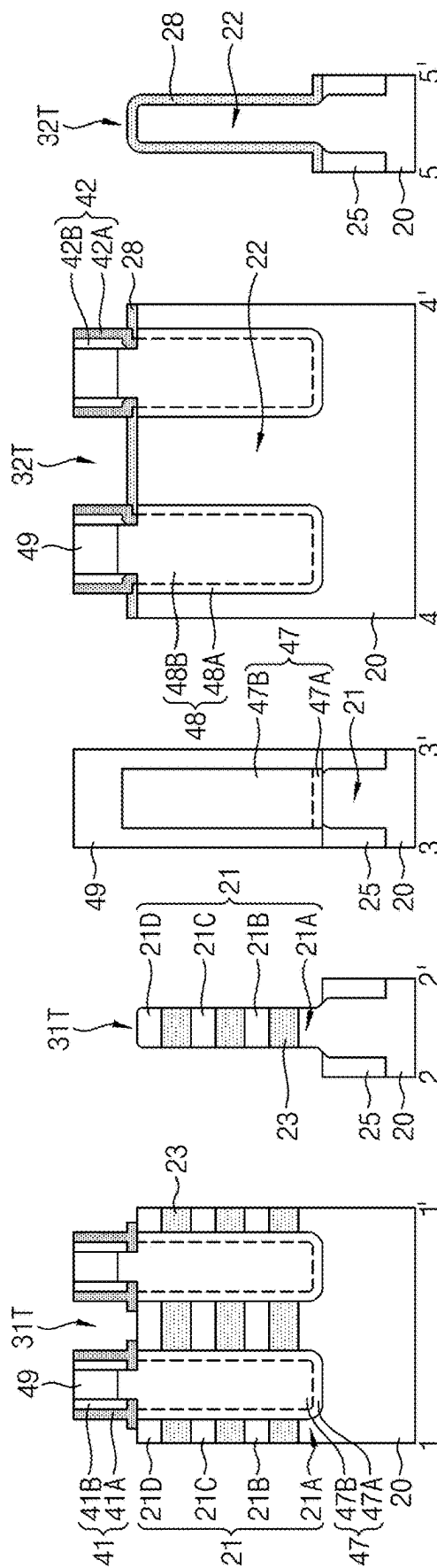


FIG. 27

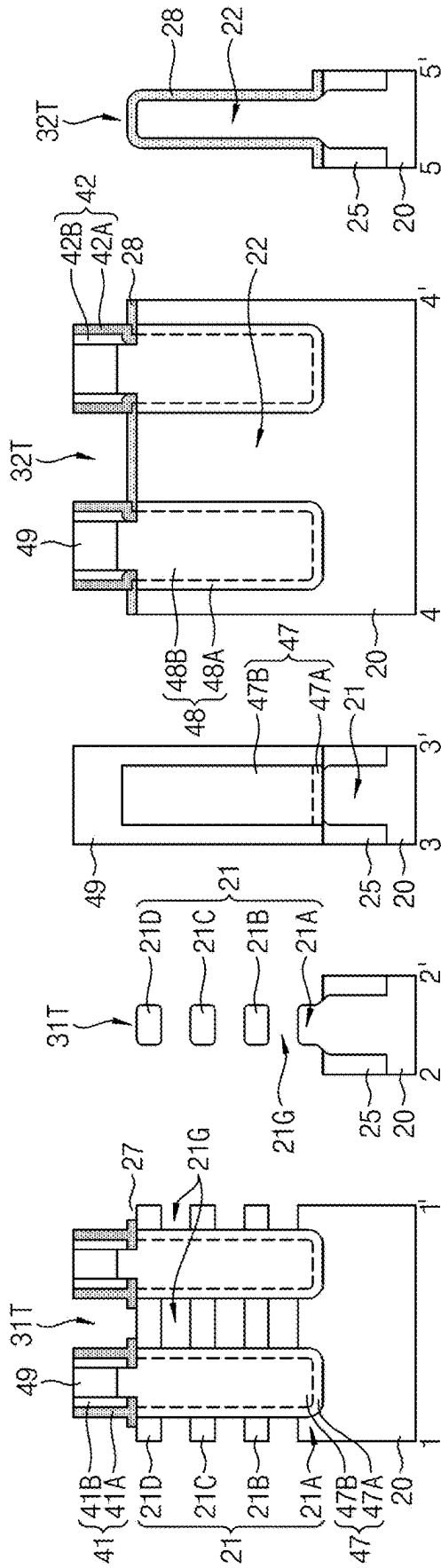


FIG. 28

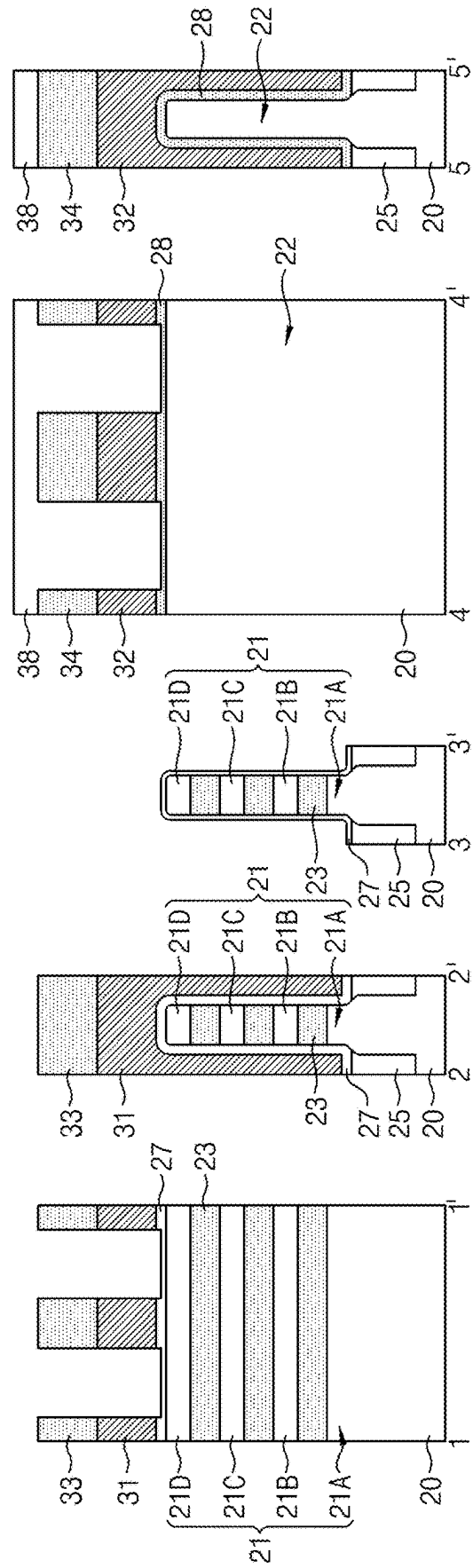


FIG. 29

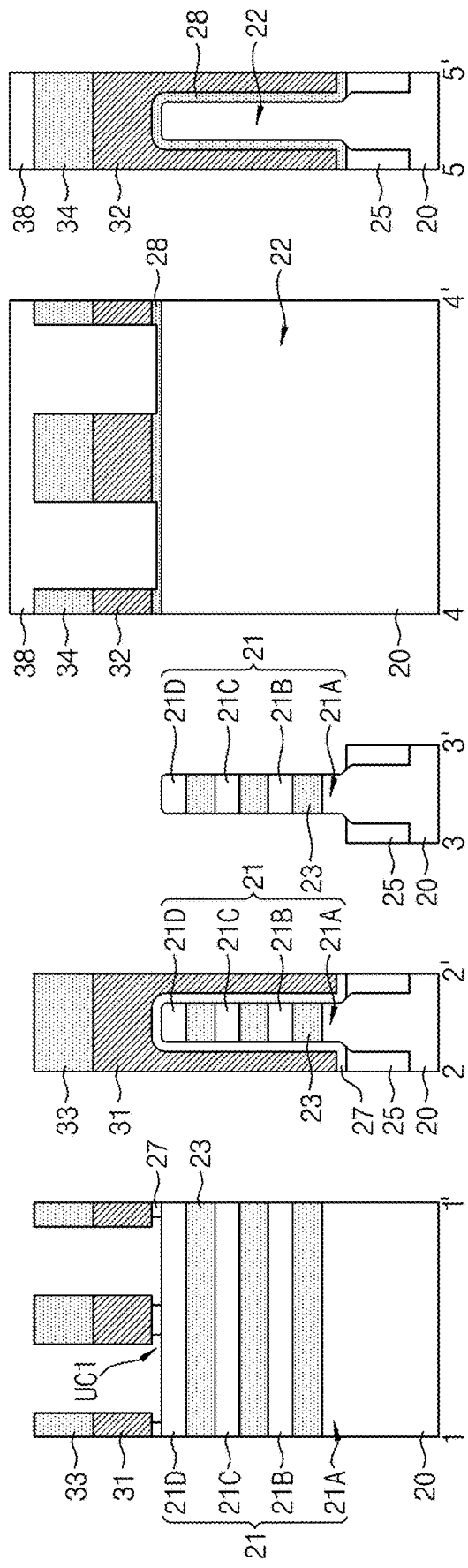


FIG. 30

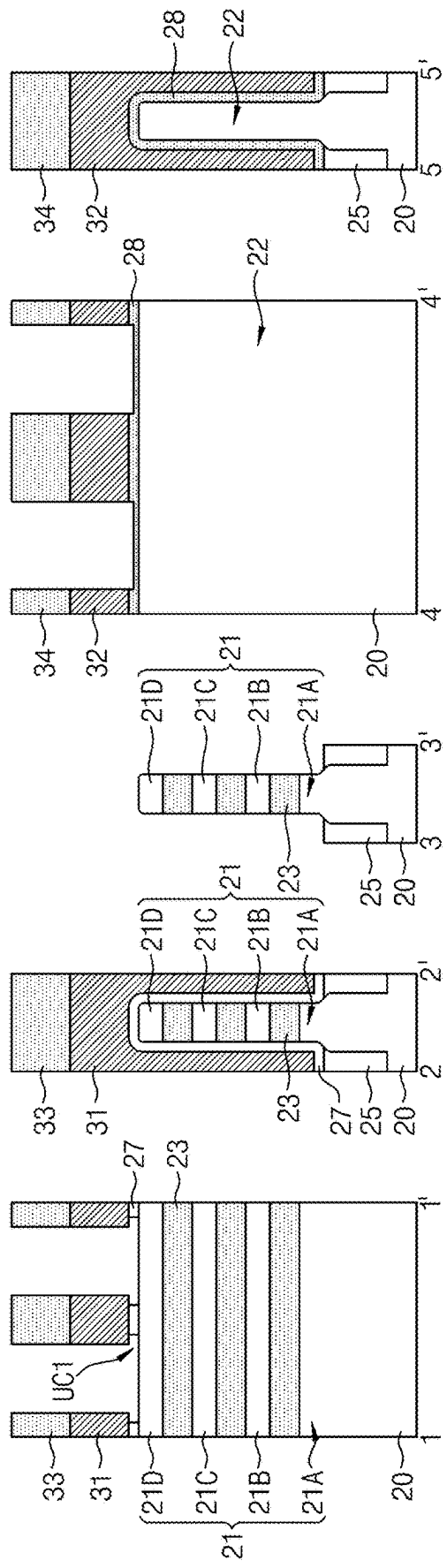


FIG. 31

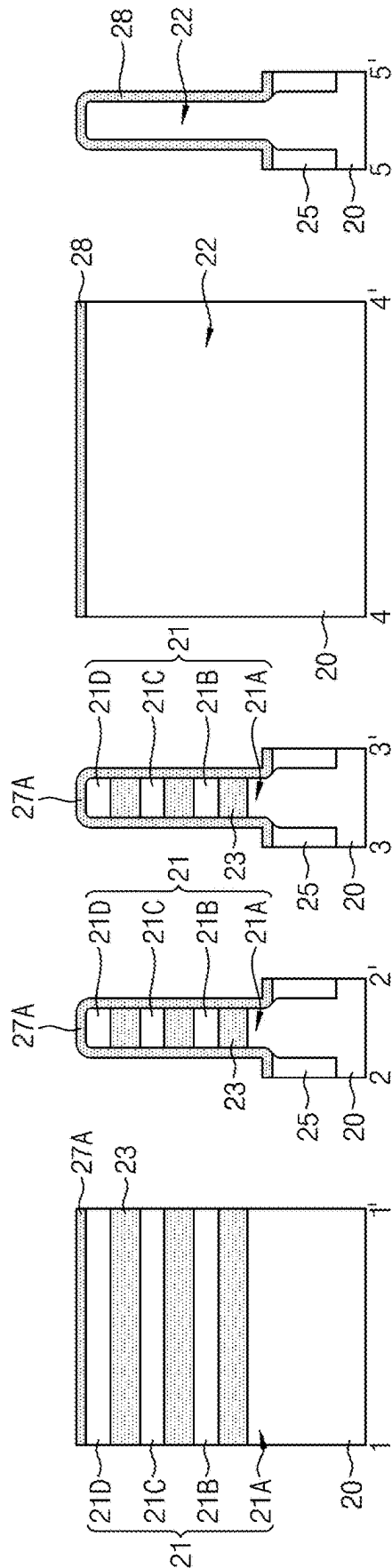
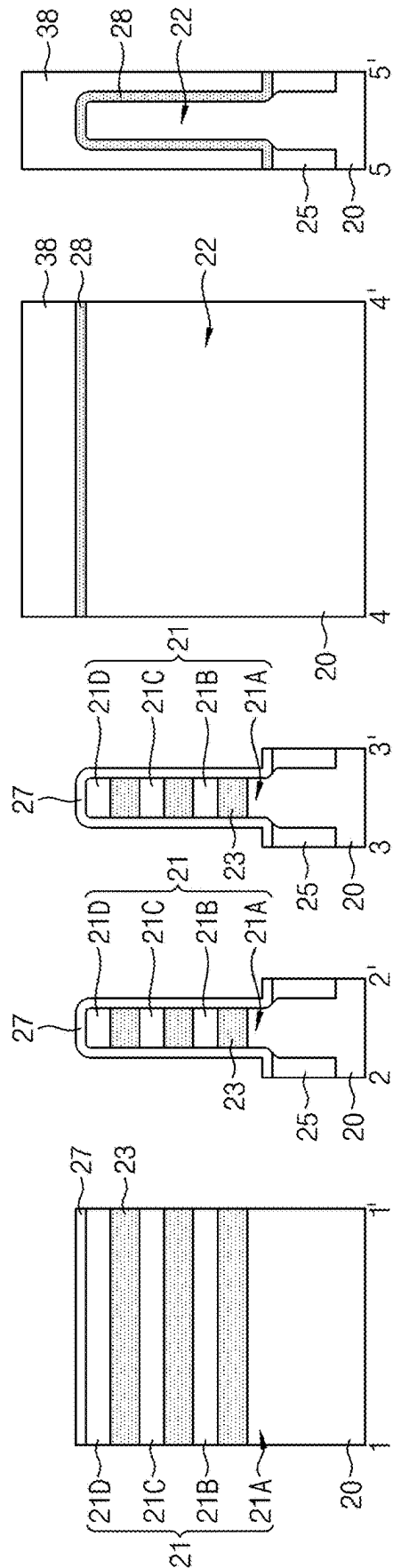


FIG. 32



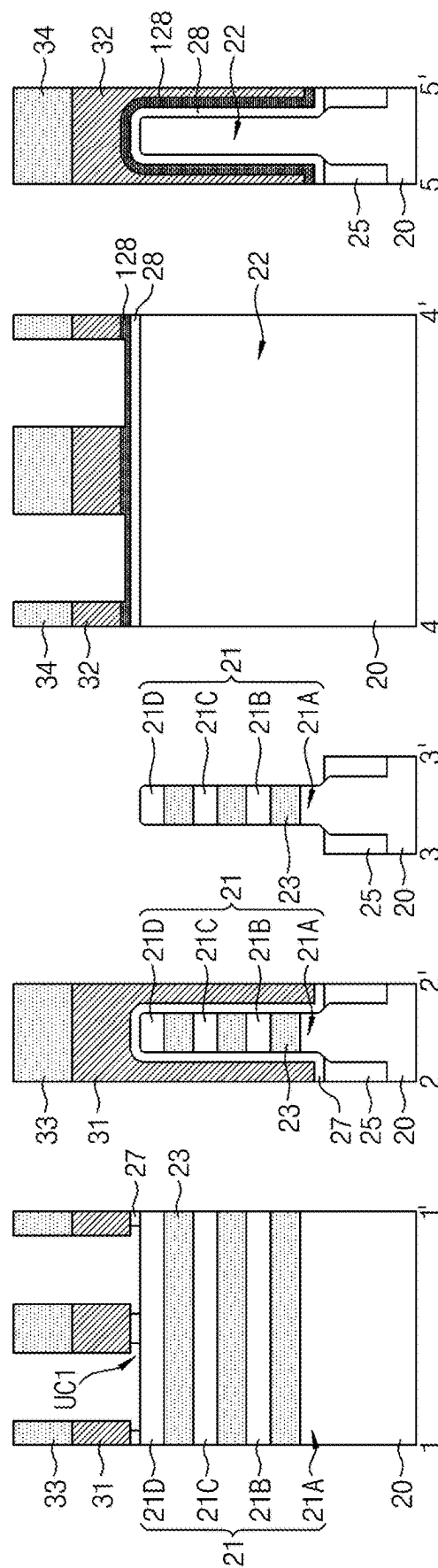
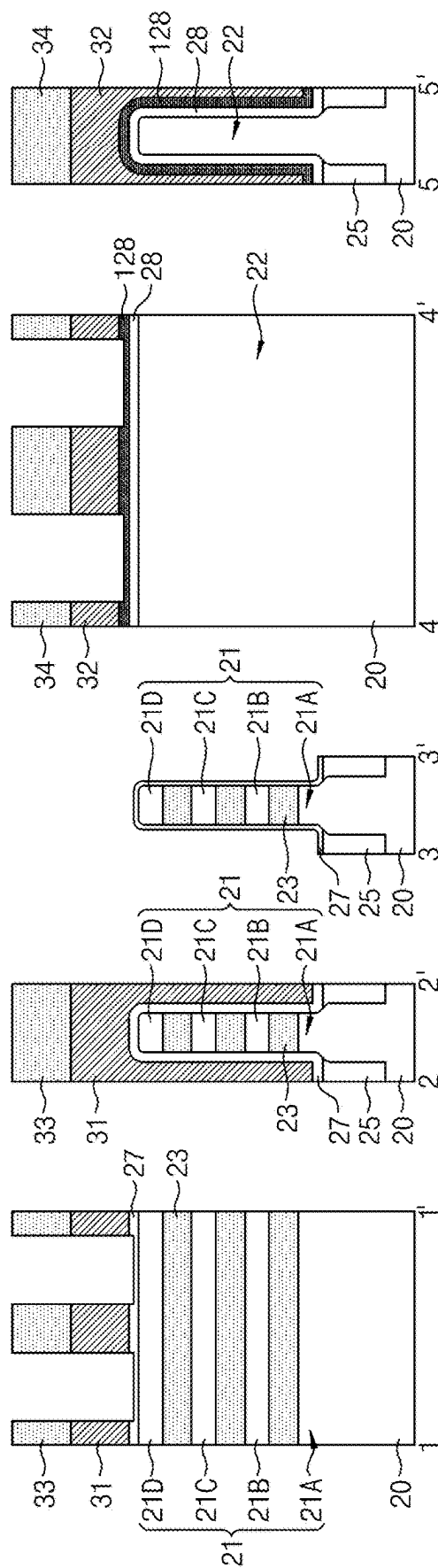
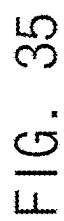


FIG. 37

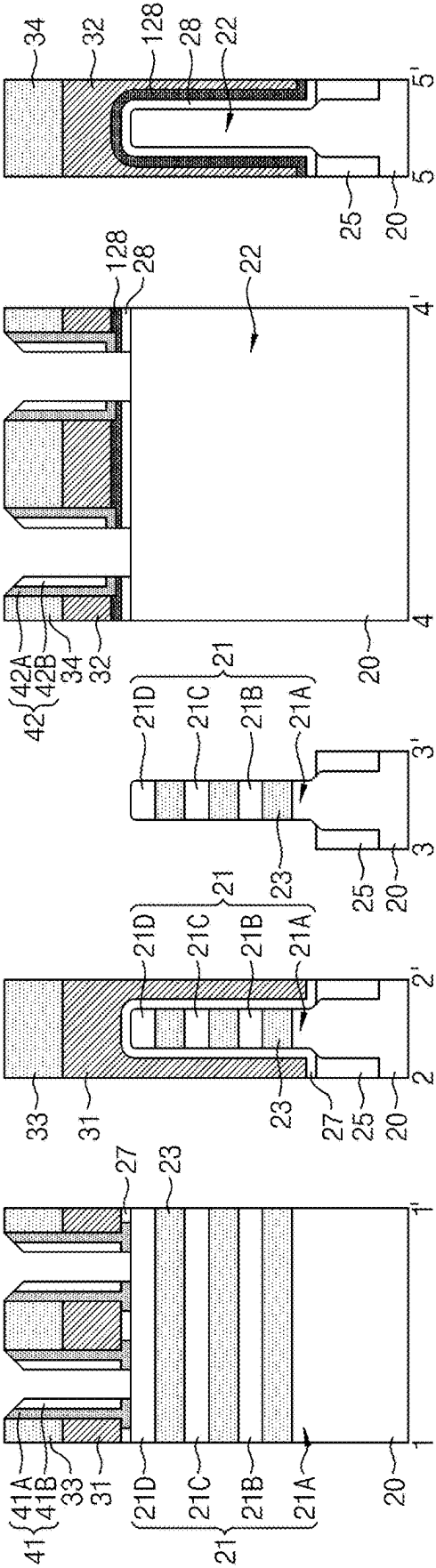


FIG. 38

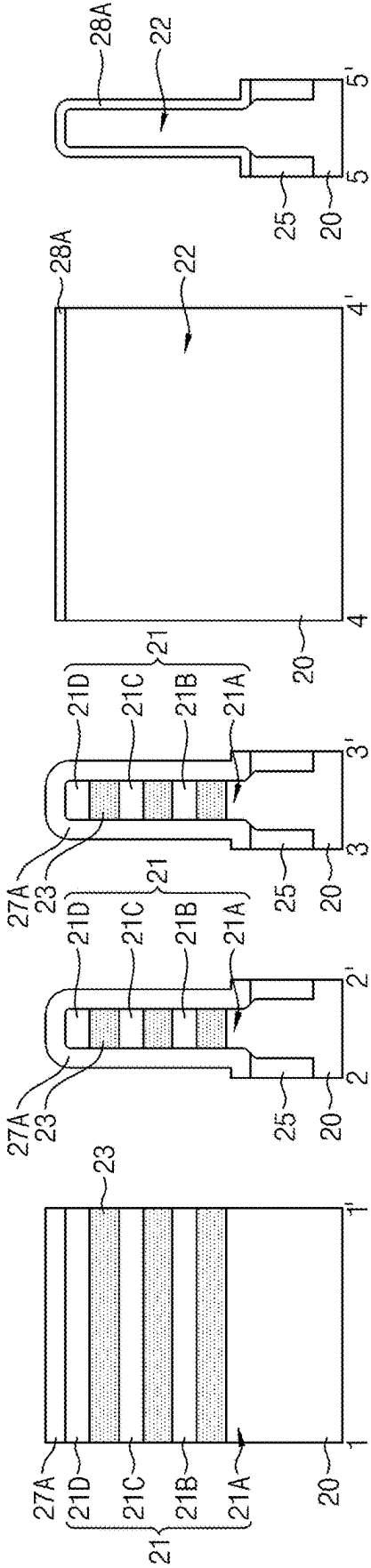


FIG. 39

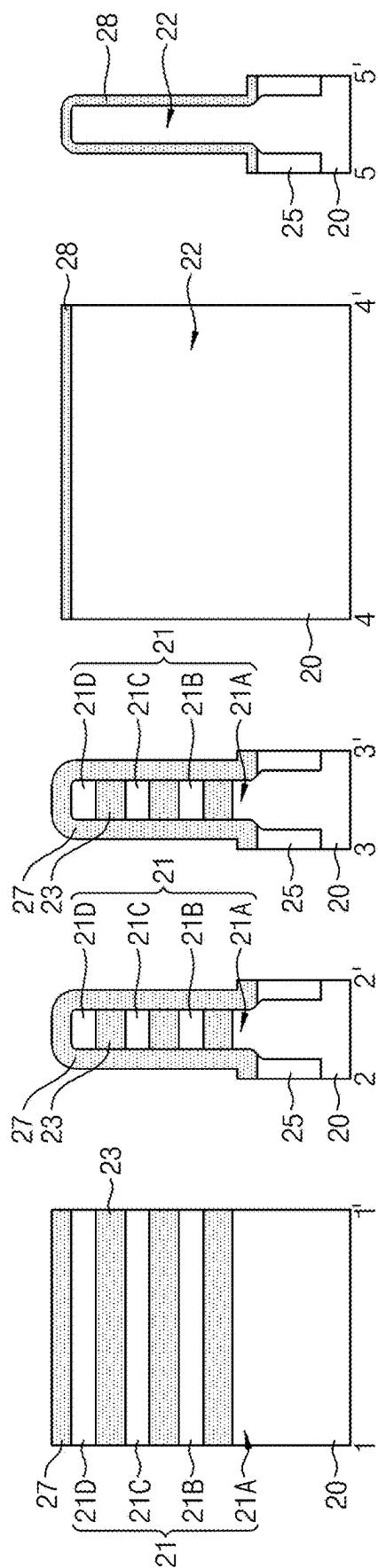
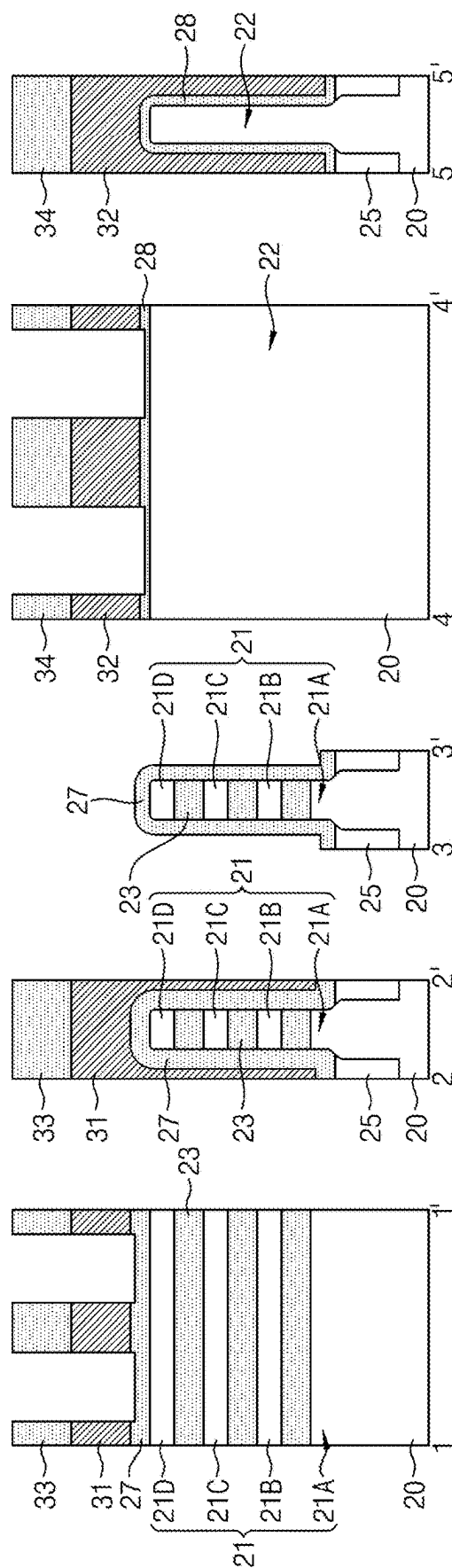


FIG. 40



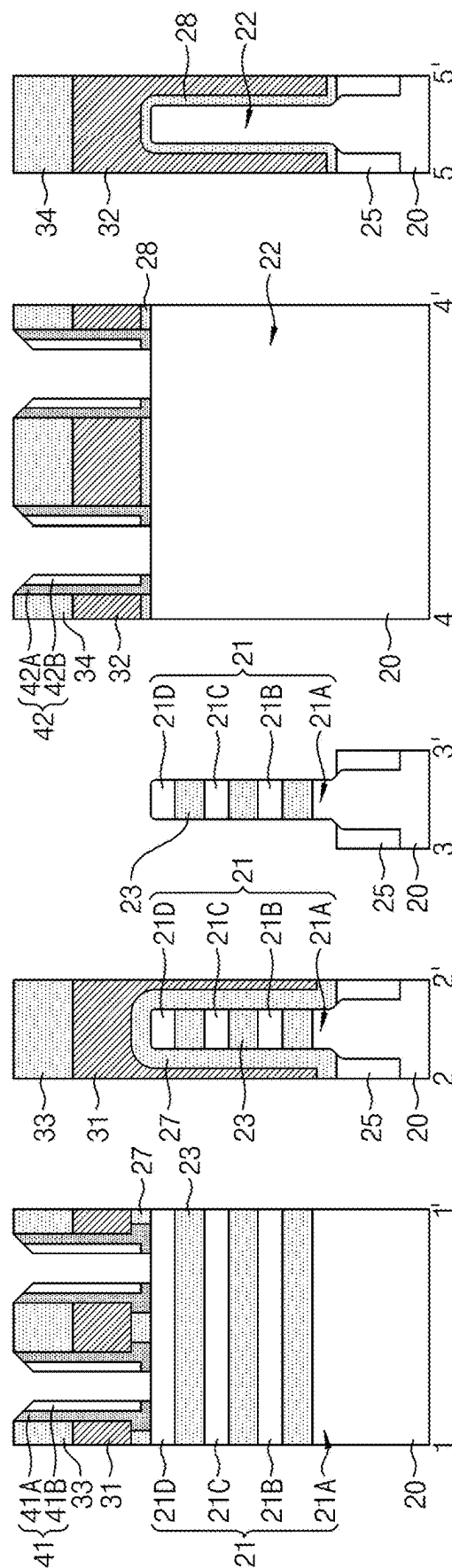
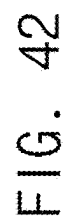
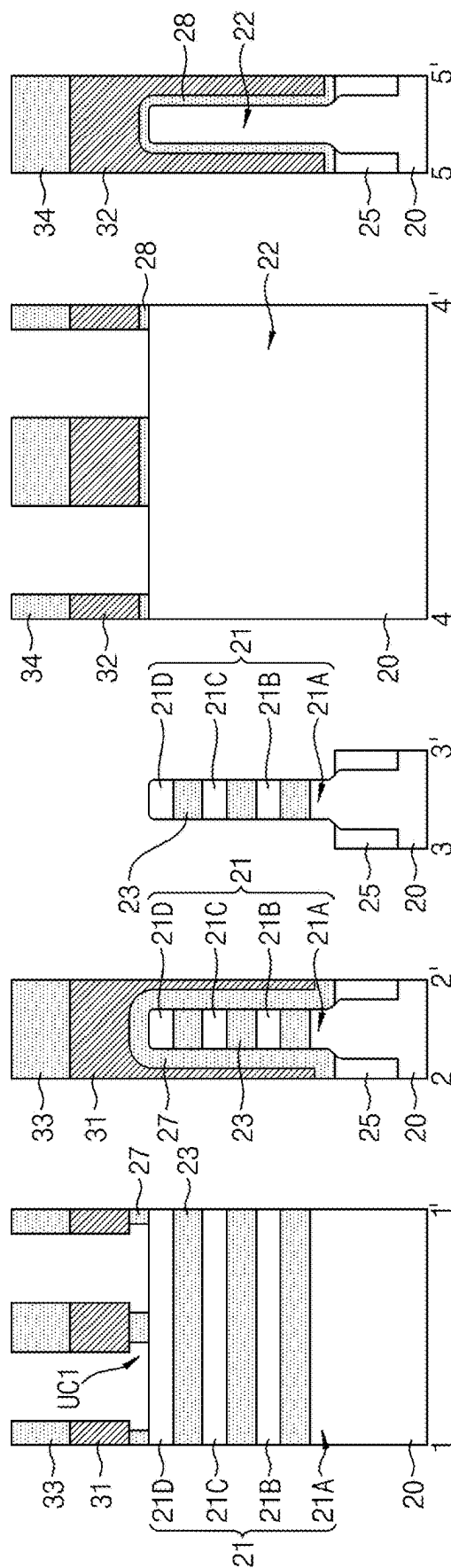


FIG. 43

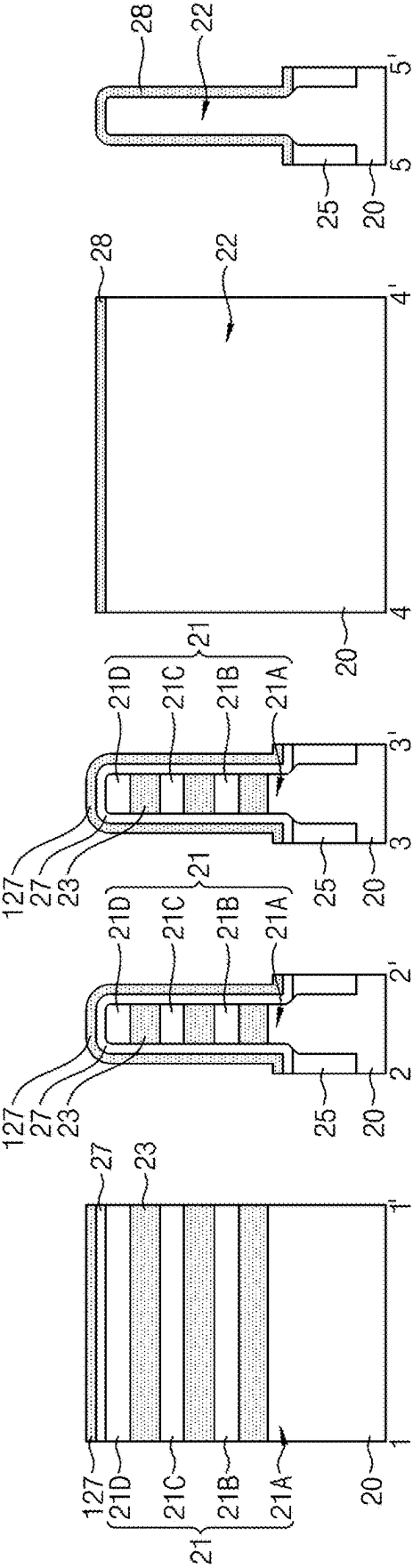
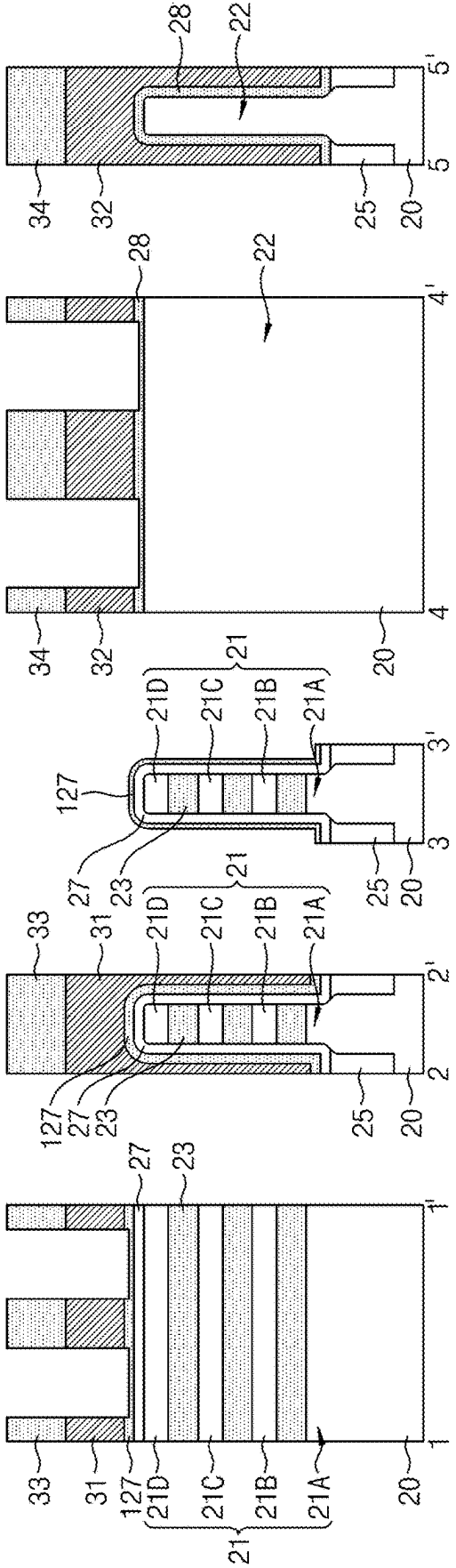


FIG. 44



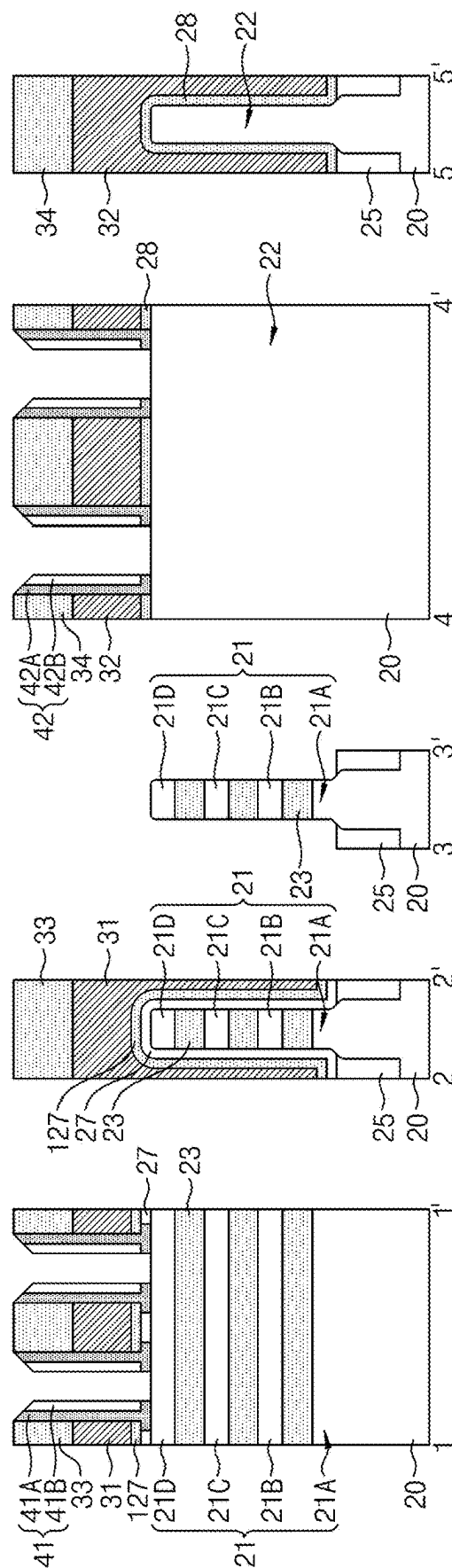
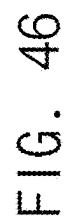
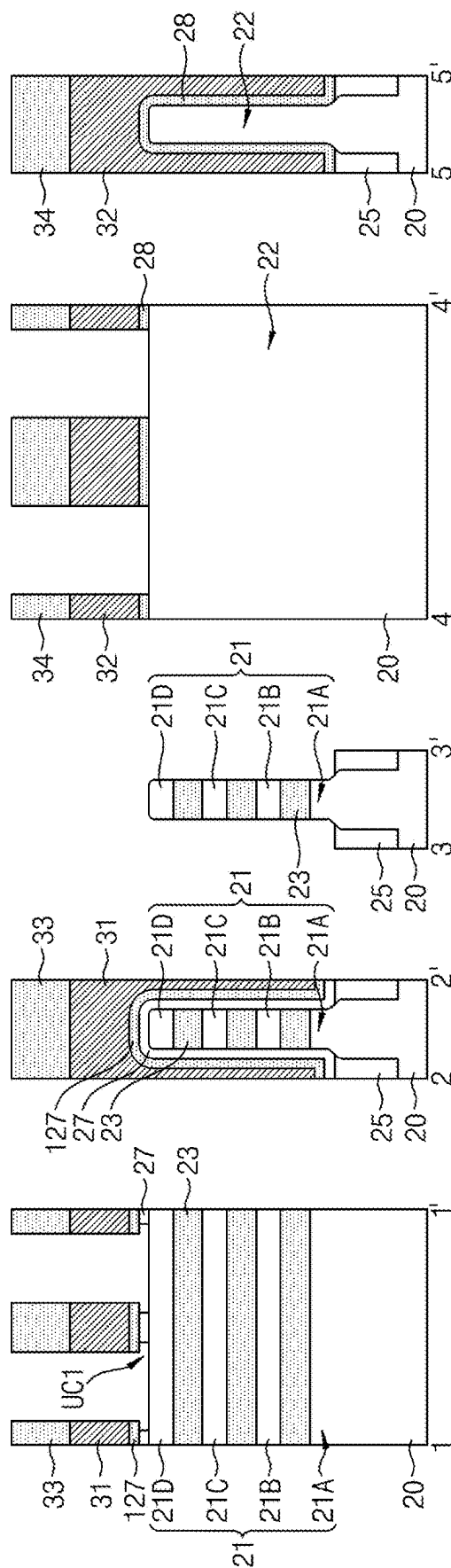
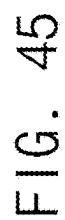


FIG. 47

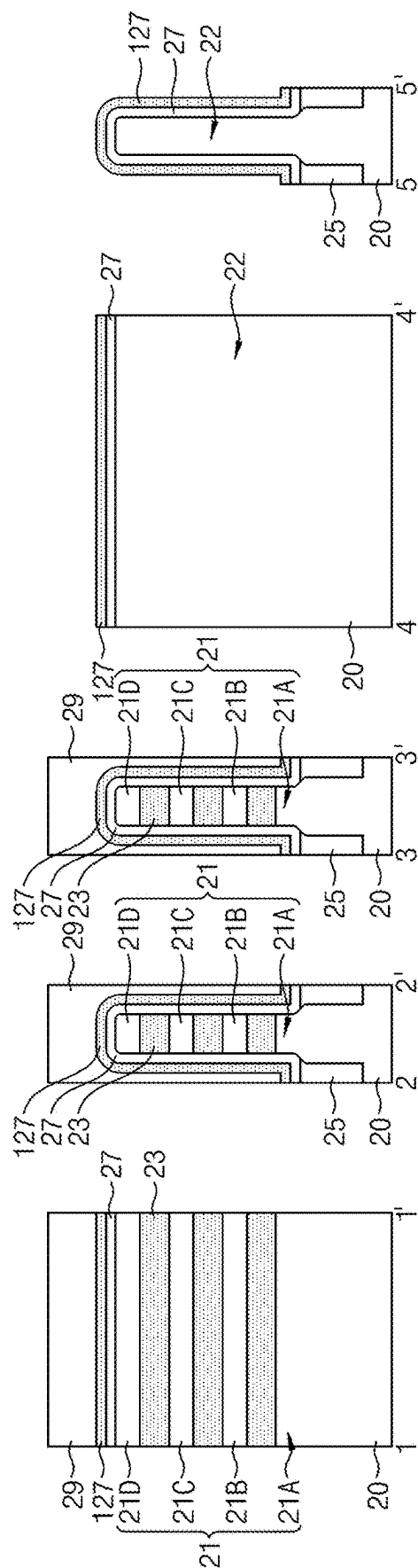


FIG. 48

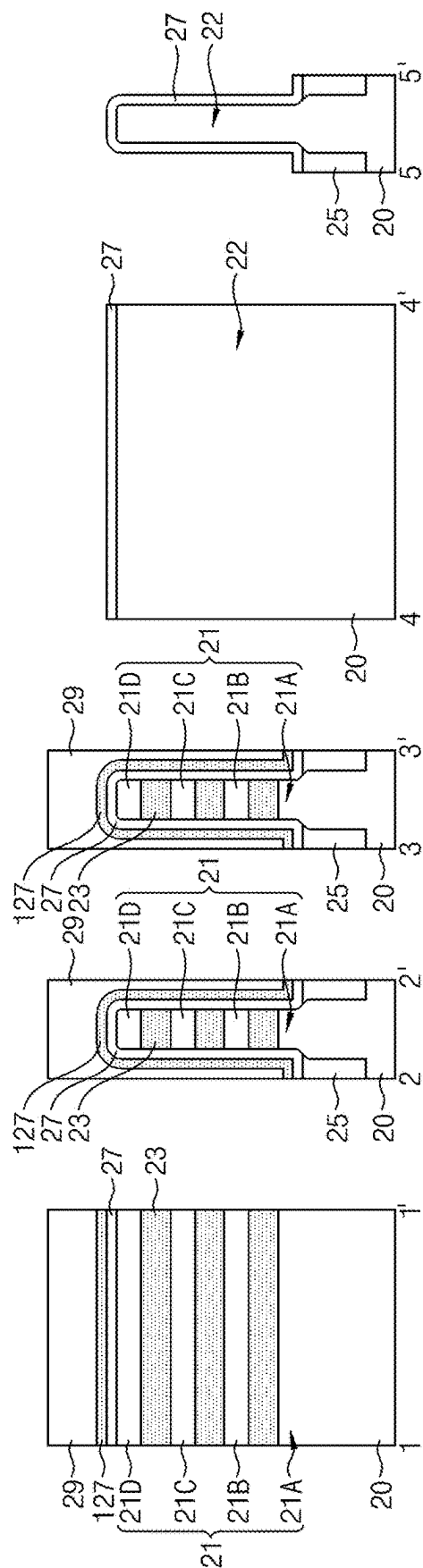


FIG. 49

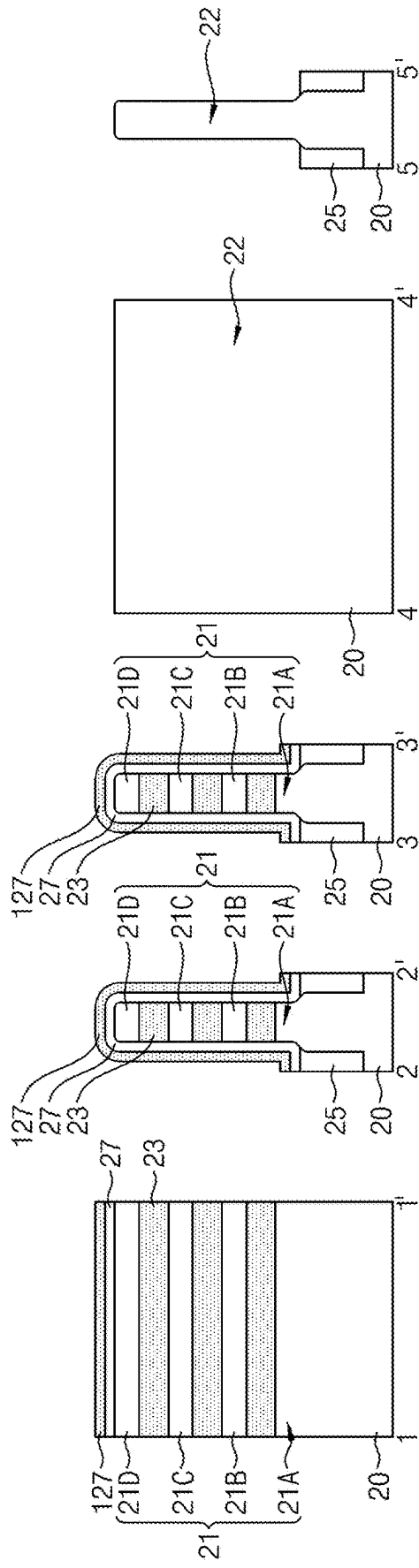


FIG. 50

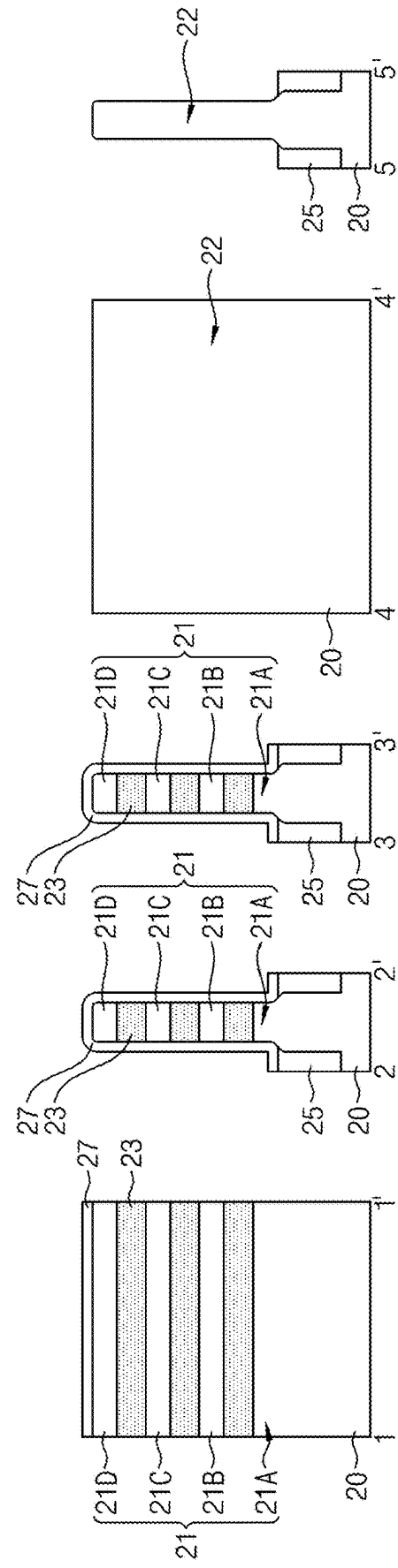


FIG. 51

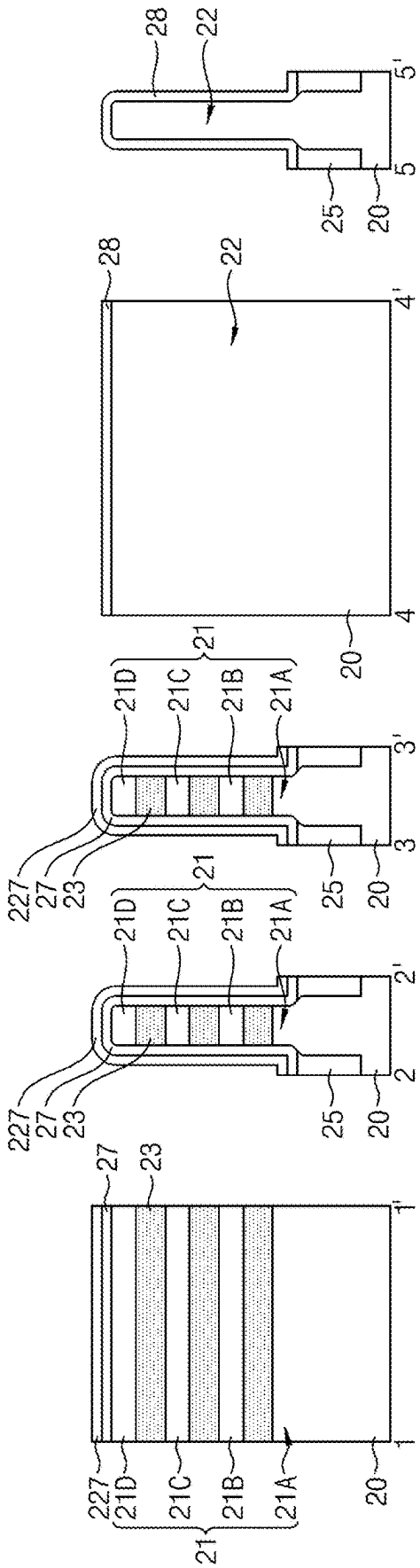


FIG. 52

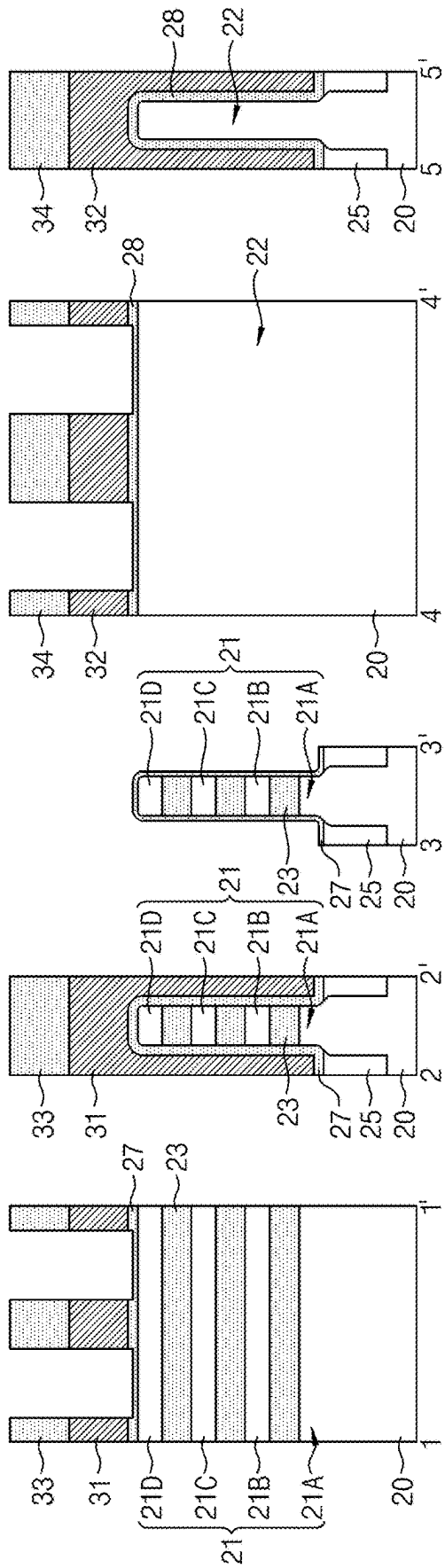


FIG. 53

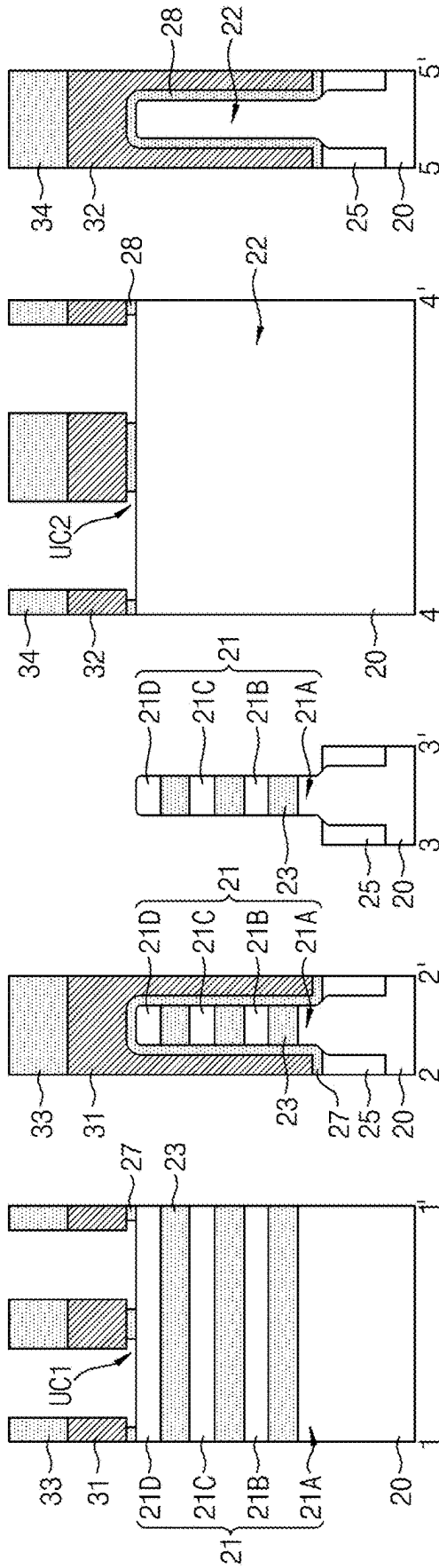


FIG. 54.

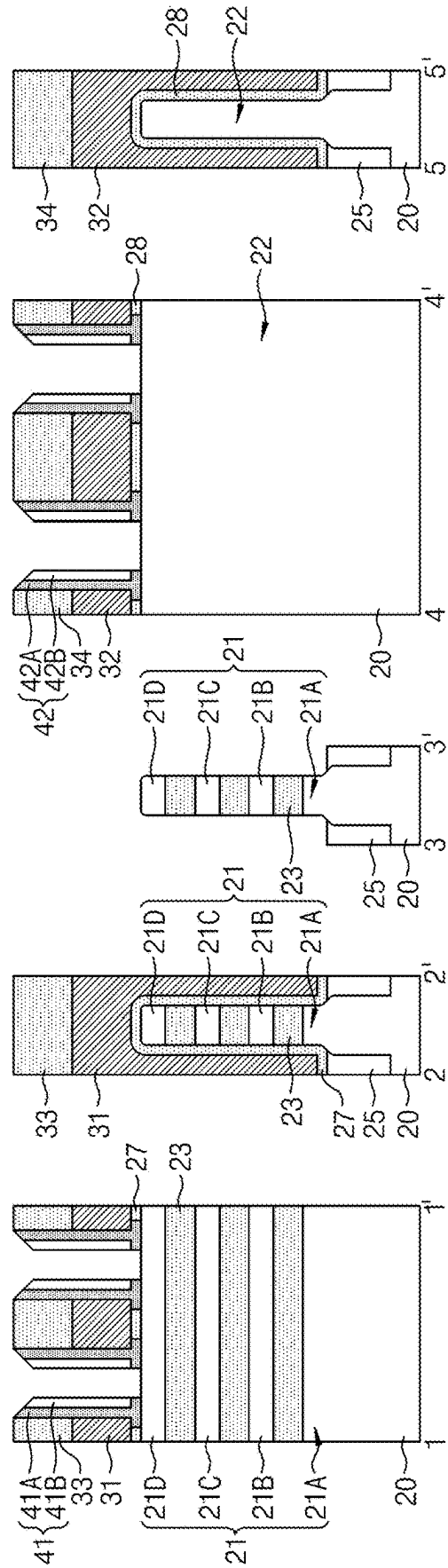


FIG. 55

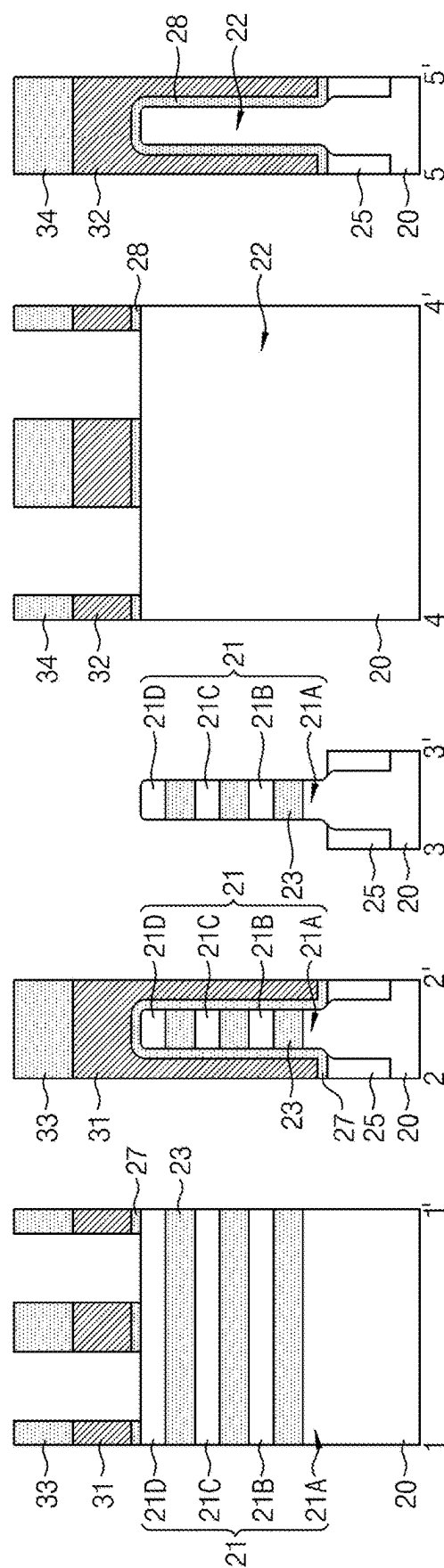


FIG. 56

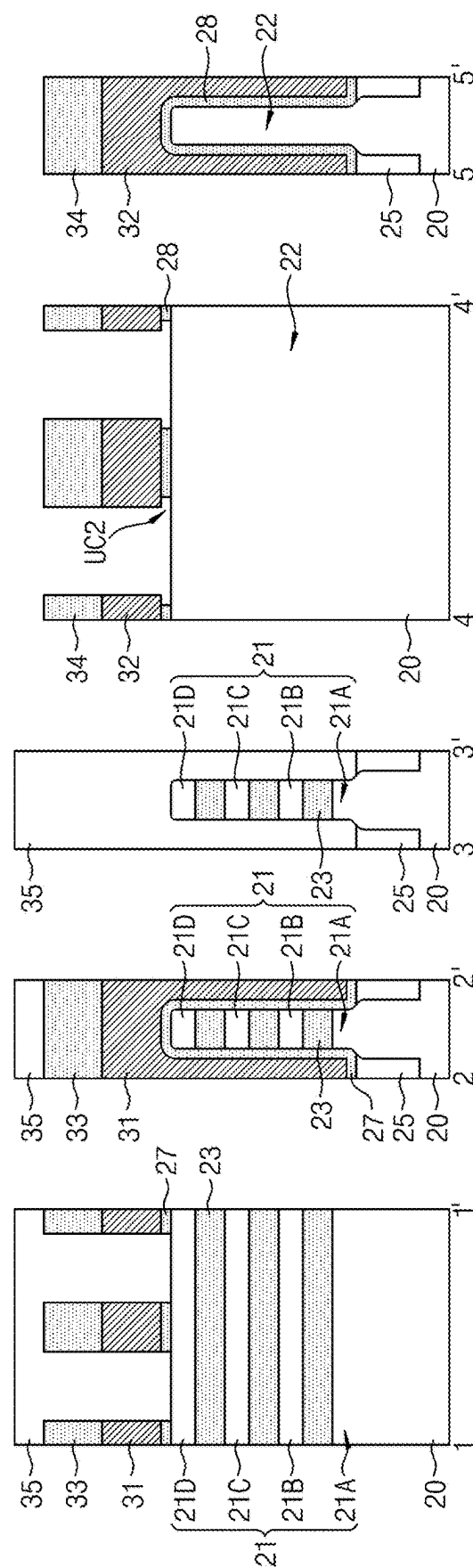
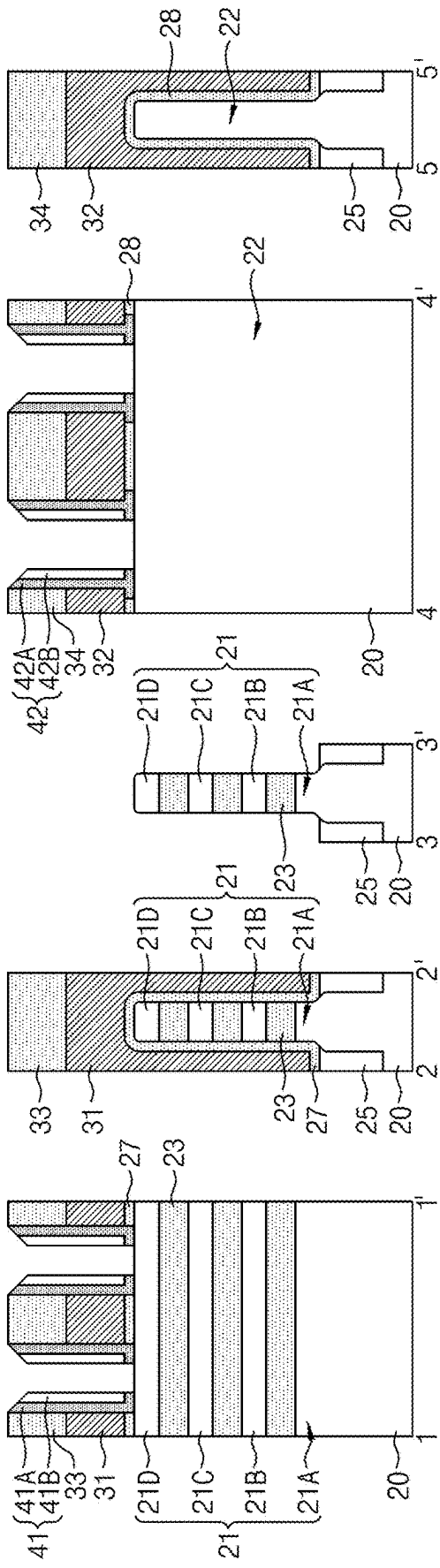


FIG. 57



SEMICONDUCTOR DEVICES INCLUDING GATE SPACER

CROSS-REFERENCE TO THE RELATED APPLICATION

[0001] This application is a continuation of U.S. application Ser. No. 18/483,413, filed Oct. 9, 2023, which is a continuation of U.S. application Ser. No. 17/060,193, filed Oct. 1, 2020, now U.S. Pat. No. 11,810,964, which claims priority to Korean Patent Application No. 10-2020-0042140, filed on Apr. 7, 2020, in the Korean Intellectual Property Office, and entitled: “Semiconductor Devices Including Gate Spacer,” is incorporated by reference herein in their entireties.

BACKGROUND

1. Field

[0002] The disclosure relates to semiconductor devices including a gate spacer and a method of forming the same.

2. Description of the Related Art

[0003] With the trend of high integration of semiconductor devices, technology using a gate spacer and a replacement gate electrode has been developed. The shape of the gate spacer has a great influence on the process of forming the replacement gate electrode.

SUMMARY

[0004] A semiconductor device in accordance with an exemplary embodiment of the disclosure may include a first active region defined on a substrate. A first gate electrode may be disposed across the first active region thereon. A first drain region may be disposed in the first active region at a position adjacent to the first gate electrode. An undercut region may be disposed between the first active region and the first gate electrode. A first gate spacer may be disposed on a side surface of the first gate electrode, and may extend in the undercut region.

[0005] A semiconductor device in accordance with an exemplary embodiment of the disclosure may include a first active region defined in a first region on a substrate. A first gate electrode may be disposed across the first active region thereon. A first drain region may be disposed in the first active region at a position adjacent to the first gate electrode. A first gate spacer may be disposed on a side surface of the first gate electrode. A second active region may be defined in a second region on the substrate. A second gate electrode may be disposed across the second active region thereon, and may have a different horizontal width from the first gate electrode. A second drain region may be disposed in the second active region at a position adjacent to the second gate electrode. A lower gate dielectric layer may be disposed between the second active region and the second gate electrode, and may have a smaller width than the second gate electrode. A second gate spacer may be disposed on a side surface of the second gate electrode, and may extend in an undercut region between the second active region and the second gate electrode. The second gate spacer may be in contact with a side surface of the lower gate dielectric layer.

[0006] A semiconductor device in accordance with an exemplary embodiment of the disclosure may include a first active region defined in a first region on a substrate. A first

gate electrode may be disposed across the first active region thereon. A first gate dielectric layer may be disposed between the first active region and the first gate electrode. A pair of first drain regions may be disposed in the first active region at positions adjacent to opposite sides of the first gate electrodes, and may be spaced apart from each other. An undercut region may be disposed between the first active region and the first gate electrode. A first gate spacer may be disposed on a side surface of the first gate electrode, and may extend in the undercut region. A second active region may be defined in the second region on the substrate. A second gate electrode may be disposed across the second active region thereon, and may have a larger horizontal width than the first gate electrode. A second gate dielectric layer may be disposed between the second active region and the second gate electrode. A pair of second drain regions may be disposed in the second active region at positions adjacent to opposite sides of the second gate electrodes, and may be spaced apart from each other. A lower gate dielectric layer may be disposed between the second active region and the second gate dielectric layer, and may have a larger horizontal width than the second gate electrode. A second gate spacer may be disposed on a side surface of the second gate electrode. The first active region may include a plurality of channel regions. Each of the plurality of channel regions may be in contact with the pair of first drain regions. The first gate electrode may surround a top surface, a side surface, and a bottom surface of at least one of the plurality of channel regions. The second gate electrode may be disposed on a top surface and a side surface of the second active region. The lower end of the second gate electrode may be disposed at a lower level than the upper end of the second active region.

[0007] A method of forming a semiconductor device in accordance with an exemplary embodiment of the disclosure may include defining a first active region and a second active region on a substrate. A first gate electrode may be formed across the first active region thereon, and a second gate electrode may be formed across the second active region thereon. A first drain region may be formed in the first active region at a position adjacent to the first gate electrode, and a second drain region may be formed in the second active region at a position adjacent to the second gate electrode. A first gate spacer may be formed on a side surface of the first gate electrode. A lower gate dielectric layer may be formed between the second active region and the second gate electrode. A second gate spacer may be formed on a side surface of the second gate electrode. The first gate spacer may extend in an undercut region between the first active region and the first gate electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Features will become apparent to those of skill in the art by describing in detail exemplary embodiments with reference to the attached drawings, in which:

[0009] FIG. 1 is a cross-sectional view illustrating semiconductor devices according to exemplary embodiments of the disclosure.

[0010] FIG. 2 is a layout illustrating semiconductor devices according to exemplary embodiments of the disclosure.

[0011] FIGS. 3 to 5 are enlarged views of parts shown in FIG. 1.

[0012] FIGS. 6 to 13 are cross-sectional views illustrating semiconductor devices according to exemplary embodiments of the disclosure.

[0013] FIGS. 14 to 57 are cross-sectional views of stages in methods of forming semiconductor devices according to exemplary embodiments of the disclosure.

DETAILED DESCRIPTION

[0014] FIG. 1 is a cross-sectional view illustrating semiconductor devices according to exemplary embodiments of the disclosure, and FIG. 2 is a layout illustrating semiconductor devices according to exemplary embodiments of the disclosure. FIGS. 3 to 5 are enlarged views of parts shown in FIG. 1. FIG. 1 illustrates cross-sectional views taken along lines 1-1', 2-2', 3-3', 4-4' and 5-5' in FIG. 2. Semiconductor devices according to exemplary embodiments of the disclosure may include MBCFET®, finFET, or a combination thereof.

[0015] Referring to FIG. 1, semiconductor devices according to exemplary embodiments of the disclosure may include a substrate 20, a first active region 21, a second active region 22, a device isolation layer 25, a lower gate dielectric layer 28, a first gate spacer 41, a second gate spacer 42, a plurality of first drain regions 47, a plurality of second drain regions 48, an interlayer insulating layer 49, a first gate dielectric layer 53, a second gate dielectric layer 54, a plurality of first gate electrodes 55, and a plurality of second gate electrodes 56.

[0016] The first active region 21 may include a plurality of channel regions 21A, 21B, 21C and 21D. The plurality of channel regions 21A, 21B, 21C and 21D may include a first channel region 21A, a second channel region 21B, a third channel region 21C, and a fourth channel region 21D. The first gate spacer 41 may include a first inner spacer 41A and a first outer spacer 41B. The second gate spacer 42 may include a second inner spacer 42A and a second outer spacer 42B. Each of the plurality of first drain regions 47 may include a first layer 47A and a second layer 47B. Each of the plurality of second drain regions 48 may include a third layer 48A and a fourth layer 48B.

[0017] Referring to FIG. 2, the substrate 20 may be provided to have a first region 11 and a second region 12 that is adjacent to the first region 11. The first active region 21 may be disposed in the first region 11 on the substrate 20. The second active region 22 may be disposed in the second region 12 on the substrate 20. The plurality of first gate electrodes 55 may be disposed across the first active region 21 in the first region 11. The plurality of second gate electrodes 56 may be disposed across the second active region 22 in the second region 12.

[0018] Each of the plurality of second gate electrodes 56 may have a different horizontal width from each of the plurality of first gate electrodes 55. Each of the plurality of second gate electrodes 56 may have a larger horizontal width than each of the plurality of first gate electrodes 55. Each of the plurality of first gate electrodes 55 may have a first width W1. Each of the plurality of second gate electrodes 56 may have a second width W2. The second width W2 may be larger than the first width W1.

[0019] Referring to FIG. 3, which illustrates an enlarged portion of FIG. 1 along line 1-1', the first gate dielectric layer 53 may be disposed between the first gate electrode 55 and the plurality of channel regions 21A, 21B, 21C and 21D. The first gate dielectric layer 53 may extend between the first

gate electrode 55 and the first gate spacer 41. An interfacial dielectric layer 51 may be disposed between the first gate dielectric layer 53 and the plurality of channel regions 21A, 21B, 21C and 21D. The interfacial dielectric layer 51 may include silicon oxide formed through a thermal oxidation process or a cleaning process. The interfacial dielectric layer 51 may be omitted. In an exemplary embodiment, the first gate dielectric layer 53 may be interposed between the first gate electrode 55 and the interfacial dielectric layer 51.

[0020] A pair of first drain regions 47 may be disposed in the first active region 21 at positions adjacent to opposite sides of the first gate electrode 55. The pair of first drain regions 47 may be spaced apart from each other. Each of the plurality of channel regions 21A, 21B, 21C and 21D may be in contact with the pair of first drain regions 47.

[0021] A first undercut region UC1 may be disposed between the first active region 21 and the first gate electrode 55. For example, as illustrated in FIG. 3, a bottom of the first gate electrode 55 may have a stair profile at bottom corners thereof, e.g., a center portion of the bottom of the first gate electrode 55 may extend deeper than edge portions of the bottom of the first gate electrode 55 to define the stair profile, such that the undercut region UC1 may be defined under the edge portions of the bottom of the first gate electrode 55.

[0022] The first gate spacer 41 may include the first inner spacer 41A and the first outer spacer 41B. The first inner spacer 41A may include an upper portion 411, which is disposed on the side surface of the first gate electrode 55, and a lower portion 412, which extends, e.g., continuously, from the lower end of the first upper portion 411 into the first undercut region UC1. The lower portion 412 may extend between the first active region 21 and the first gate electrode 55, e.g., between the first active region 21 and the edge portion of the bottom of the first gate electrode 55. A straight line, e.g., an imaginary straight line, that extends along the outermost side surface of the first gate electrode 55 and is perpendicular to the surface of the substrate 20 may intersect the lower portion 412. The upper portion 411 may have a height greater than the horizontal width thereof. The lower portion 412 may have a horizontal width greater than the height thereof, e.g., the upper and lower portions 411 and 412 may have a combined cross-section of an inverted "T" that extends along the outermost side surface of the first gate electrode 55 and protrudes into the first undercut region UC1 to partially overlap the edge portion of the bottom of the first gate electrode 55.

[0023] The first gate dielectric layer 53 may be interposed between the first gate electrode 55 and the upper portion 411 and between the first gate electrode 55 and the lower portion 412. The first gate dielectric layer 53 may be in contact with the side and top surfaces of the lower portion 412. The first gate dielectric layer 53 may be in contact with the side surface of the upper portion 411, e.g., the first gate dielectric layer 53 may be conformal on outer surfaces of the first gate electrode 55.

[0024] Referring to FIG. 4, which illustrates an enlarged portion of FIG. 1 along line 2-2', the interfacial dielectric layer 51 may cover the top and side surfaces of the first channel region 21A. The interfacial dielectric layer 51 may surround the top, bottom and side surfaces of the second channel region 21B, the third channel region 21C, and the fourth channel region 21D. The first gate electrode 55 may surround the top, bottom and side surfaces of the second channel region 21B, the third channel region 21C, and the

fourth channel region 21D. The first gate electrode 55 may cover the top and side surfaces of the first channel region 21A. The first gate dielectric layer 53 may be disposed between the first gate electrode 55 and the interfacial dielectric layer 51. The interfacial dielectric layer 51 may be omitted.

[0025] Referring to FIG. 5, which illustrates an enlarged portion of FIG. 1 along line 4-4', a pair of second drain regions 48 may be disposed in the second active region 22 at positions adjacent to the second gate electrode 56. The pair of second drain regions 48 may be spaced apart from each other. The second gate dielectric layer 54 may be disposed between the second gate electrode 56 and the second active region 22. The lower gate dielectric layer 28 may be disposed between the second gate dielectric layer 54 and the second active region 22. The second gate spacer 42 may be disposed on the side surface of the second gate electrode 56. The second gate dielectric layer 54 may extend between the second gate electrode 56 and the second gate spacer 42.

[0026] The lower gate dielectric layer 28 may have a larger horizontal width than the second gate electrode 56. The lower gate dielectric layer 28 may protrude, e.g., along the horizontal direction, beyond the second gate electrode 56. The second gate spacer 42 may be in contact with the top and side surfaces of the lower gate dielectric layer 28. The second gate spacer 42 may include the second inner spacer 42A and the second outer spacer 42B. The second inner spacer 42A may be in contact with the top and side surfaces of the lower gate dielectric layer 28. In an exemplary embodiment, the second gate dielectric layer 54 may be disposed on the lower gate dielectric layer 28.

[0027] Referring again to FIGS. 1 to 5, the first active region 21 and the second active region 22 may be defined on the substrate 20. The first gate electrode 55 may be disposed across the first active region 21. The first drain region 47 may be disposed in the first active region 21 at a position adjacent to the first gate electrode 55. The first undercut region UC1 may be disposed between the first active region 21 and the first gate electrode 55. The first gate spacer 41 may be disposed on the side surface of the first gate electrode 55, and may extend into the first undercut region UC1. The first gate spacer 41 may have, e.g., an inverted T shape or an L shape.

[0028] The second gate electrode 56 may be disposed across the second active region 22. The second drain region 48 may be disposed in the second active region 22 at a position adjacent to the second gate electrode 56. The lower gate dielectric layer 28 may be disposed between the second active region 22 and the second gate electrode 56. The second gate spacer 42 may be disposed on the side surface of the second gate electrode 56. The second gate electrode 56 may be disposed on the top and side surfaces of the second active region 22. The lower end of the second gate electrode 56 may be disposed at a lower level than the upper end of the second active region 22. The second gate electrode 56 may have a larger horizontal width than the first gate electrode 55. In an exemplary embodiment, the lower portion 412 of the first inner spacer 41A may have substantially the same thickness, e.g., along a vertical direction, as the lower gate dielectric layer 28.

[0029] FIGS. 6 to 13 are cross-sectional views illustrating semiconductor devices according to exemplary embodi-

ments of the disclosure. FIGS. 6 to 13 are cross-sectional views taken along lines 1-1', 2-2', 3-3', 4-4' and 5-5' in FIG. 2.

[0030] Referring to FIG. 6, the first active region 21 may include a first notch 21N, which is disposed adjacent to the top surface of the device isolation layer 25. The second active region 22 may include a second notch 22N, which is disposed adjacent to the top surface of the device isolation layer 25.

[0031] Referring to FIG. 7, the second active region 22 may include a plurality of semiconductor layers 22A, 23A, 22B, 23B, 22C, 23C and 22D. The plurality of semiconductor layers 22A, 23A, 22B, 23B, 22C, 23C and 22D may include a first semiconductor layer 22A, a second semiconductor layer 23A, a third semiconductor layer 22B, a fourth semiconductor layer 23B, a fifth semiconductor layer 22C, a sixth semiconductor layer 23C, and a seventh semiconductor layer 22D, which are sequentially stacked. The first semiconductor layer 22A may be defined in the second active region 22. The first semiconductor layer 22A may include a semiconductor layer such as a single-crystal silicon layer.

[0032] Each of the second semiconductor layer 23A, the third semiconductor layer 22B, the fourth semiconductor layer 23B, the fifth semiconductor layer 22C, the sixth semiconductor layer 23C, and the seventh semiconductor layer 22D may include a single-crystal semiconductor layer that is formed through an epitaxial growth method. In an exemplary embodiment, each of the third semiconductor layer 22B, the fifth semiconductor layer 22C, and the seventh semiconductor layer 22D may include a single-crystal silicon layer. Each of the second semiconductor layer 23A, the fourth semiconductor layer 23B, and the sixth semiconductor layer 23C may include a single-crystal SiGe layer.

[0033] Referring to FIG. 8, a plurality of blocking patterns 59 may be disposed between the plurality of first drain regions 47 and the plurality of first gate electrodes 55. The plurality of blocking patterns 59 may include, e.g., silicon oxide, silicon nitride, silicon oxynitride, or combinations thereof. In an exemplary embodiment, the plurality of blocking patterns 59 may include silicon nitride. The plurality of blocking patterns 59 may be disposed between the plurality of channel regions 21A, 21B, 21C and 21D. The plurality of blocking patterns 59 may be interposed between the first layer 47A and the first gate dielectric layer 53.

[0034] Referring to FIG. 9, an intermediate gate dielectric layer 128 may be disposed on the lower gate dielectric layer 28. The second gate dielectric layer 54 may be disposed on the intermediate gate dielectric layer 128. The intermediate gate dielectric layer 128 may include a material having etch selectivity with respect to the lower gate dielectric layer 28. The intermediate gate dielectric layer 128 may include a different material from the lower gate dielectric layer 28. The intermediate gate dielectric layer 128 may have a larger horizontal width than the second gate electrode 56. The intermediate gate dielectric layer 128 may protrude beyond the second gate electrode 56. The second inner spacer 42A may be in contact with the top surface of the intermediate gate dielectric layer 128.

[0035] Referring to FIG. 10, the first gate spacer 41 may have various thicknesses and shapes. In an exemplary embodiment, the portion of the first gate spacer 41 that is located between the first gate electrode 55 and the first active

region 21 may be thicker than the lower gate dielectric layer 28. The outermost portion of the lower gate dielectric layer 28 may be aligned between the second gate spacer 42 and the second gate electrode 56.

[0036] Referring to FIG. 11, the portion of the first gate spacer 41 that is located between the first gate electrode 55 and the first active region 21 may have substantially the same thickness as the lower gate dielectric layer 28. The outermost portion of the lower gate dielectric layer 28 may be aligned between the second gate spacer 42 and the second gate electrode 56.

[0037] Referring to FIG. 12, the lower gate dielectric layer 28 may have a smaller horizontal width than the second gate electrode 56. The second gate spacer 42 may extend in a second undercut region UC2 between the second active region 22 and the second gate electrode 56. The second gate spacer 42 may have an L shape. In an exemplary embodiment, the second inner spacer 42A may extend in the second undercut region UC2. The second inner spacer 42A may have an L shape. The second inner spacer 42A may be in contact with the side surface of the lower gate dielectric layer 28.

[0038] Referring to FIG. 13, the first gate spacer 41 may be disposed on the side surface of the first gate electrode 55. The first gate dielectric layer 53 may be disposed between the first gate electrode 55 and the first active region 21 and between the first gate electrode 55 and the first gate spacer 41. The first undercut region (UC1 in FIG. 3) may be omitted.

[0039] The lower gate dielectric layer 28 may have a smaller horizontal width than the second gate electrode 56. The second gate spacer 42 may extend in the second undercut region UC2 between the second active region 22 and the second gate electrode 56. The second gate spacer 42 may have an L shape. The second gate spacer 42 may be in contact with the side surface of the lower gate dielectric layer 28.

[0040] FIGS. 14 to 27 are cross-sectional views of stages in methods of forming semiconductor devices according to exemplary embodiments of the disclosure. FIGS. 14 to 27 are cross-sectional views along lines 1-1', 2-2', 3-3', 4-4' and 5-5' in FIG. 2.

[0041] Referring to FIGS. 2 and 14, a device isolation layer 25 may be formed on the substrate 20 to define the first active region 21 and the second active region 22. The first active region 21 may be formed in the first region 11 on the substrate 20. The second active region 22 may be formed in the second region 12 on the substrate 20. The first active region 21 may include the plurality of channel regions 21A, 21B, 21C and 21D. A plurality of sacrificial layers 23 may be formed between the plurality of channel regions 21A, 21B, 21C and 21D. The plurality of channel regions 21A, 21B, 21C and 21D and the plurality of sacrificial layers 23 may be stacked alternately and repeatedly. The plurality of channel regions 21A, 21B, 21C and 21D may include the first channel region 21A, the second channel region 21B, the third channel region 21C, and the fourth channel region 21D.

[0042] The substrate 20 may include a semiconductor substrate, e.g., a silicon wafer or a silicon-on-insulator (SOI) wafer. Each of the first active region 21 and the second active region 22 may have a height, e.g., along the vertical direction, greater than the horizontal width thereof. Formation of the plurality of channel regions 21A, 21B, 21C and

21D and the plurality of sacrificial layers 23 may include an epitaxial growth process. In an exemplary embodiment, the plurality of sacrificial layers 23 may include a SiGe layer, formed through an epitaxial growth method. Each of the second channel region 21B, the third channel region 21C, and the fourth channel region 21D may include a Si layer, formed through an epitaxial growth method. The first channel region 21A may be defined in the substrate 20. The first channel region 21A may include a single-crystal Si layer. The second active region 22 may be defined in the substrate 20. The second active region 22 may include a single-crystal Si layer.

[0043] The device isolation layer 25 may include, e.g., silicon oxide, silicon nitride, silicon oxynitride, low-k dielectrics, high-k dielectrics, or combinations thereof. The top surface of the device isolation layer 25 may be formed at a lower level than the top surfaces of the first active region 21 and the second active region 22. The upper ends of the first active region 21 and the second active region 22 may protrude to a higher level than the top surface of the device isolation layer 25. The upper corners of the first active region 21 and the second active region 22 may be formed to be rounded.

[0044] Referring to FIGS. 2 and 15, a buffer layer 27 and the lower gate dielectric layer 28 may be formed on the substrate 20. In an exemplary embodiment, the buffer layer 27 and the lower gate dielectric layer 28 may be formed simultaneously. The buffer layer 27 and the lower gate dielectric layer 28 may be substantially the same thickness. The buffer layer 27 and the lower gate dielectric layer 28 may include an insulating material, e.g., silicon oxide. The buffer layer 27 may cover the first active region 21. The lower gate dielectric layer 28 may cover the second active region 22.

[0045] Referring to FIGS. 2 and 16, a first mask pattern 29 may be formed to cover the buffer layer 27 and expose the lower gate dielectric layer 28. Nitrogen may be injected into the lower gate dielectric layer 28. In an exemplary embodiment, the injecting nitrogen into the lower gate dielectric layer 28 may include a decoupled plasma nitridation (DPN) process, a post-nitridation annealing (PNA) process, or a combination thereof. The first mask pattern 29 may serve to prevent nitrogen from being injected into the buffer layer 27 during the process of injecting nitrogen into the lower gate dielectric layer 28.

[0046] Referring to FIGS. 2 and 17, the buffer layer 27 may be exposed by removing the first mask pattern 29. A plurality of first temporary gate electrodes 31 may be formed across the first active region 21 on the buffer layer 27. A second mask pattern 33 may be formed on the plurality of first temporary gate electrodes 31. A plurality of second temporary gate electrodes 32 may be formed across the second active region 22 on the lower gate dielectric layer 28. A third mask pattern 34 may be formed on the plurality of second temporary gate electrodes 32.

[0047] In an exemplary embodiment, the plurality of first temporary gate electrodes 31 and the plurality of second temporary gate electrodes 32 may include a polysilicon layer. The second mask pattern 33 and the third mask pattern 34 may include silicon nitride. Formation of the plurality of first temporary gate electrodes 31 and the plurality of second temporary gate electrodes 32 may include an anisotropic etching process using the second mask pattern 33 and the third mask pattern 34 as an etching mask. The buffer layer

27 between the plurality of first temporary gate electrodes 31 may be partially etched, and may be reduced in thickness. The lower gate dielectric layer 28 between the plurality of second temporary gate electrodes 32 may be partially etched, and may be reduced in thickness.

[0048] Referring to FIGS. 2 and 18, a spacer layer 36L may be formed on the top and side surfaces of the buffer layer 27, the lower gate dielectric layer 28, the plurality of first temporary gate electrodes 31, the plurality of second temporary gate electrodes 32, the second mask pattern 33, and the third mask pattern 34. A fourth mask pattern 35 may be formed on the spacer layer 36L to cover the first region 11 and expose the second region 12.

[0049] A sacrificial spacer 36 may be formed on the sidewalls of the plurality of second temporary gate electrodes 32 and the third mask pattern 34 by anisotropically etching the spacer layer 36L. The sacrificial spacer 36 may include silicon nitride. The second active region 22 may be exposed to the outside of the sacrificial spacer 36. The bottom of the sacrificial spacer 36 may be in contact with the top surface of the lower gate dielectric layer 28. The sacrificial spacer 36 may be in contact with the side surfaces of the plurality of second temporary gate electrodes 32 and the third mask pattern 34.

[0050] Referring to FIGS. 2 and 19, the spacer layer 36L may be exposed by removing the fourth mask pattern 35. A fifth mask pattern 38 may be formed to cover the second region 12 and expose the first region 11. The spacer layer 36L may be removed.

[0051] Referring to FIGS. 2 and 20, the fifth mask pattern 38 may be removed.

[0052] Referring to FIGS. 2 and 21, the first active region 21 may be exposed between the plurality of first temporary gate electrodes 31 by partially removing the buffer layer 27. The buffer layer 27 may be preserved between the plurality of first temporary gate electrodes 31 and the first active region 21. The buffer layer 27 may have a smaller horizontal width than each of the plurality of first temporary gate electrodes 31. A first undercut region UC1 may be formed under the plurality of first temporary gate electrodes 31. In an exemplary embodiment, the first undercut region UC1 may be formed between the plurality of first temporary gate electrodes 31 and the first active region 21.

[0053] The sidewalls of the plurality of second temporary gate electrodes 32 and the third mask pattern 34 may be exposed by removing the sacrificial spacer 36. The lower gate dielectric layer 28 may have a larger horizontal width than a corresponding one of the plurality of second temporary gate electrodes 32. The lower gate dielectric layer 28 may protrude beyond a corresponding one of the plurality of second temporary gate electrodes 32.

[0054] Referring to FIGS. 2 and 22, the first gate spacer 41 may be formed on the sidewalls of the plurality of first temporary gate electrodes 31 and the second mask pattern 33. The second gate spacer 42 may be formed on the sidewalls of the plurality of second temporary gate electrodes 32 and the third mask pattern 34. The first gate spacer 41 may include the first inner spacer 41A and the first outer spacer 41B. The second gate spacer 42 may include the second inner spacer 42A and the second outer spacer 42B. In an exemplary embodiment, the first inner spacer 41A and the second inner spacer 42A may include silicon nitride. The first outer spacer 41B and the second outer spacer 42B may include silicon oxide or silicon oxynitride.

[0055] The first inner spacer 41A may be formed on the sidewalls of the plurality of first temporary gate electrodes 31 and the second mask pattern 33. The first inner spacer 41A may extend in the first undercut region UC1. The first inner spacer 41A may be in contact with the bottom surfaces of the plurality of first temporary gate electrodes 31 and with the first active region 21. The first inner spacer 41A may be in contact with the side surface of the buffer layer 27. The first outer spacer 41B may be formed on the outer side surface of the first inner spacer 41A.

[0056] The second inner spacer 42A may be formed on the sidewalls of the plurality of second temporary gate electrodes 32 and the third mask pattern 34. The second inner spacer 42A may be in contact with the side and top surfaces of the lower gate dielectric layer 28. The second outer spacer 42B may be formed on the outer side surface of the second inner spacer 42A.

[0057] Referring to FIGS. 2 and 23, a plurality of first trenches 43 may be formed in the first active region 21 between the plurality of first temporary gate electrodes 31. A plurality of second trenches 44 may be formed in the second active region 22 between the plurality of second temporary gate electrodes 32.

[0058] Referring to FIGS. 2 and 24, a plurality of first drain regions 47 may be formed in the plurality of first trenches 43, and a plurality of second drain regions 48 may be formed in the plurality of second trenches 44. Each of the plurality of first drain regions 47 may include a first layer 47A and a second layer 47B disposed on the first layer 47A. Each of the plurality of second drain regions 48 may include a third layer 48A and a fourth layer 48B disposed on the third layer 48A. The upper ends of the plurality of first drain regions 47 may protrude to a higher level than the upper end of the first active region 21. The upper ends of the plurality of second drain regions 48 may protrude to a higher level than the upper end of the second active region 22.

[0059] Each of the plurality of first drain regions 47 and the plurality of second drain regions 48 may be formed through a selective epitaxial growth (SEG) method. Each of the plurality of first drain regions 47 and the plurality of second drain regions 48 may include SiGe, Si, SiC, or combinations thereof. In an exemplary embodiment, each of the first layer 47A and the third layer 48A may include a Si layer, and each of the second layer 47B and the fourth layer 48B may include a SiGe layer. In an exemplary embodiment, the first layer 47A may include a SiGe layer having a lower Ge density than the second layer 47B. The third layer 48A may include a SiGe layer having a lower Ge density than the fourth layer 48B.

[0060] Referring to FIGS. 2 and 25, an interlayer insulating layer 49 may be formed on the plurality of first drain regions 47 and the plurality of second drain regions 48. The interlayer insulating layer 49 may include, e.g., silicon oxide, silicon nitride, silicon oxynitride, low-k dielectrics, high-k dielectrics, or combinations thereof. In an exemplary embodiment, the interlayer insulating layer 49 may include silicon oxide.

[0061] The top surfaces of the plurality of first temporary gate electrodes 31 and the plurality of second temporary gate electrodes 32 may be exposed by removing the second mask pattern 33 and the third mask pattern 34 through a planarization process. The planarization process may include a chemical mechanical polishing (CMP) process.

[0062] Referring to FIGS. 2 and 26, a first gate trench 31T may be formed by removing the plurality of first temporary gate electrodes 31 and the buffer layer 27. A second gate trench 32T may be formed by removing the plurality of second temporary gate electrodes 32.

[0063] Referring to FIGS. 2 and 27, a plurality of gap regions 21G may be formed by removing the plurality of sacrificial layers 23. The plurality of gap regions 21G may communicate with the first gate trench 31T. The plurality of first drain regions 47 may be exposed in the plurality of gap regions 21G.

[0064] The first inner spacer 41A may serve to prevent damage to the plurality of first drain regions 47 during the process of removing the plurality of sacrificial layers 23. The second inner spacer 42A and the lower gate dielectric layer 28 may serve to prevent damage to the plurality of second drain regions 48 and the second active region 22 during the process of removing the plurality of sacrificial layers 23.

[0065] Referring again to FIGS. 1 and 2, the first gate dielectric layer 53 may be formed on the inner walls of the first gate trench 31T and the plurality of gap regions 21G. The second gate dielectric layer 54 may be formed on the inner walls of the second gate trench 32T. The first gate electrode 55 may be formed on the first gate dielectric layer 53 to fill the first gate trench 31T. The second gate electrode 56 may be formed on the second gate dielectric layer 54 to fill the second gate trench 32T.

[0066] Each of the first gate dielectric layer 53 and the second gate dielectric layer 54 may include, e.g., silicon oxide, silicon nitride, silicon oxynitride, high-k dielectrics, or combinations thereof. In an exemplary embodiment, each of the first gate dielectric layer 53 and the second gate dielectric layer 54 may include high-k dielectrics, e.g., metal oxide. Each of the first gate electrode 55 and the second gate electrode 56 may include, e.g., metal, metal silicide, metal nitride, metal oxide, polysilicon, conductive carbon, or combinations thereof. In an exemplary embodiment, each of the first gate electrode 55 and the second gate electrode 56 may include, e.g., work function metal.

[0067] FIGS. 28 to 30 are cross-sectional views illustrating stages in methods of forming semiconductor devices according to exemplary embodiments of the disclosure. FIGS. 28 to 30 are cross-sectional views along lines 1-1', 2-2', 3-3', 4-4' and 5-5' in FIG. 2. Hereinafter, only the differences will be briefly described.

[0068] Referring to FIGS. 2 and 28, a fifth mask pattern 38 may be formed to cover the second region 12 and expose the first region 11.

[0069] Referring to FIGS. 2 and 29, the first undercut region UC1 may be formed under the plurality of first temporary gate electrodes 31 by partially removing the buffer layer 27.

[0070] Referring to FIGS. 2 and 30, the fifth mask pattern 38 may be removed. Subsequently, semiconductor devices may be formed in a manner similar to that described with reference to FIGS. 22 to 27.

[0071] FIGS. 31 and 32 are cross-sectional views illustrating stages in methods of forming semiconductor devices according to exemplary embodiments of the disclosure. FIGS. 31 and 32 are cross-sectional views along lines 1-1', 2-2', 3-3', 4-4' and 5-5' in FIG. 2.

[0072] Referring to FIGS. 2 and 31, a temporary buffer layer 27A and a lower gate dielectric layer 28 may be formed. In an exemplary embodiment, the temporary buffer

layer 27A may be formed through the same process as the lower gate dielectric layer 28 simultaneously therewith, and may include substantially the same material as the lower gate dielectric layer 28. The temporary buffer layer 27A and the lower gate dielectric layer 28 may include, e.g., silicon oxynitride or silicon nitride.

[0073] Referring to FIGS. 2 and 32, a fifth mask pattern 38 may be formed to cover the lower gate dielectric layer 28 and expose the temporary buffer layer 27A. The buffer layer 27 may be formed by removing nitrogen in the temporary buffer layer 27A through a surface modification process, e.g., a descum process. The nitrogen concentration in the buffer layer 27 may be lower than that in the lower gate dielectric layer 28. The buffer layer 27 may have etch selectivity with respect to the lower gate dielectric layer 28. The buffer layer 27 may have a higher etching rate than the lower gate dielectric layer 28. The fifth mask pattern 38 may be removed. Subsequently, semiconductor devices may be formed in a manner similar to that described with reference to FIGS. 17 to 29.

[0074] FIGS. 33 to 37 are cross-sectional views illustrating stages in methods of forming semiconductor devices according to exemplary embodiments of the disclosure. FIGS. 33 to 37 are cross-sectional views along lines 1-1', 2-2', 3-3', 4-4' and 5-5' in FIG. 2.

[0075] Referring to FIGS. 2 and 33, a sacrificial buffer layer 127 may be formed on the buffer layer 27. An intermediate gate dielectric layer 128 may be formed on the lower gate dielectric layer 28. The buffer layer 27 may be formed through the same process as the lower gate dielectric layer 28 simultaneously therewith, and may include substantially the same material as the lower gate dielectric layer 28. The sacrificial buffer layer 127 may be formed through the same process as the intermediate gate dielectric layer 128 simultaneously therewith, and may include substantially the same material as the intermediate gate dielectric layer 128.

[0076] In an exemplary embodiment, each of the buffer layer 27 and the lower gate dielectric layer 28 may include, e.g., silicon oxide or silicon oxynitride. The sacrificial buffer layer 127 and the intermediate gate dielectric layer 128 may include different materials from the buffer layer 27 and the lower gate dielectric layer 28. The sacrificial buffer layer 127 and the intermediate gate dielectric layer 128 may include silicon oxynitride or silicon nitride.

[0077] Referring to FIGS. 2 and 34, a sixth mask pattern 138 may be formed to cover the intermediate gate dielectric layer 128. The sacrificial buffer layer 127 may be removed through an isotropic etching process to expose the buffer layer 27. The sixth mask pattern 138 may be removed.

[0078] Referring to FIGS. 2 and 35, a plurality of first temporary gate electrodes 31, a plurality of second temporary gate electrodes 32, a second mask pattern 33, and a third mask pattern 34 may be formed.

[0079] Referring to FIGS. 2 and 36, the first active region 21 may be exposed between the plurality of first temporary gate electrodes 31 by partially removing the buffer layer 27. The buffer layer 27 may be preserved between the plurality of first temporary gate electrodes 31 and the first active region 21. The buffer layer 27 may have a smaller horizontal width than each of the plurality of first temporary gate electrodes 31. A first undercut region UC1 may be formed under the plurality of first temporary gate electrodes 31. In an exemplary embodiment, the first undercut region UC1

may be formed between the plurality of first temporary gate electrodes 31 and the first active region 21. The intermediate gate dielectric layer 128 may serve to prevent etching damage to the lower gate dielectric layer 28 during the process of forming the first undercut region UC1.

[0080] Referring to FIGS. 2 and 37, the first gate spacer 41 may be formed on the sidewalls of the plurality of first temporary gate electrodes 31 and the second mask pattern 33. The second gate spacer 42 may be formed on the sidewalls of the plurality of second temporary gate electrodes 32 and the third mask pattern 34. The first gate spacer 41 may include the first inner spacer 41A and the first outer spacer 41B. The second gate spacer 42 may include the second inner spacer 42A and the second outer spacer 42B.

[0081] The first inner spacer 41A may extend in the first undercut region UC1. The second inner spacer 42A may be formed on the sidewalls of the plurality of second temporary gate electrodes 32 and the third mask pattern 34. The lower end of the second inner spacer 42A may be in contact with the top surface of the intermediate gate dielectric layer 128.

[0082] Referring again to FIGS. 2 and 9, the intermediate gate dielectric layer 128 may be preserved on the lower gate dielectric layer 28. The second gate dielectric layer 54 may be formed on the intermediate gate dielectric layer 128. The intermediate gate dielectric layer 128 may have a larger horizontal width than the second gate electrode 56. The intermediate gate dielectric layer 128 may protrude beyond the second gate electrode 56.

[0083] FIGS. 38 to 42 are cross-sectional views illustrating stages in methods of forming semiconductor devices according to exemplary embodiments of the disclosure. FIGS. 38 to 42 are cross-sectional views along lines 1-1', 2-2', 3-3', 4-4' and 5-5' in FIG. 2.

[0084] Referring to FIGS. 2 and 38, the temporary buffer layer 27A and a temporary lower gate dielectric layer 28A may be formed. The temporary buffer layer 27A may be thicker than the temporary lower gate dielectric layer 28A. In an exemplary embodiment, the temporary buffer layer 27A and the temporary lower gate dielectric layer 28A may include the same material. The temporary buffer layer 27A and the temporary lower gate dielectric layer 28A may include silicon oxide.

[0085] Referring to FIGS. 2 and 39, the buffer layer 27 and a lower gate dielectric layer 28 may be formed by injecting nitrogen into the temporary buffer layer 27A and the temporary lower gate dielectric layer 28A. In an exemplary embodiment, the injecting nitrogen into the temporary buffer layer 27A and the temporary lower gate dielectric layer 28A may include a decoupled plasma nitridation (DPN) process, a post-nitridation annealing (PNA) process, or a combination thereof.

[0086] Referring to FIGS. 2 and 40, a plurality of first temporary gate electrodes 31, a plurality of second temporary gate electrodes 32, a second mask pattern 33, and a third mask pattern 34 may be formed.

[0087] Referring to FIGS. 2 and 41, the first active region 21 may be exposed between the plurality of first temporary gate electrodes 31 by partially removing the buffer layer 27. The buffer layer 27 may be preserved between the plurality of first temporary gate electrodes 31 and the first active region 21. A first undercut region UC1 may be formed under the plurality of first temporary gate electrodes 31.

[0088] The lower gate dielectric layer 28 may be partially removed during the process of forming the first undercut

region UC1. The lower gate dielectric layer 28 may be preserved between the plurality of second temporary gate electrodes 32 and the second active region 22. Since the lower gate dielectric layer 28 is thinner than the buffer layer 27, the rate at which the lower gate dielectric layer 28 is etched between the plurality of second temporary gate electrodes 32 and the second active region 22 may be reduced during the process of forming the first undercut region UC1. In an exemplary embodiment, the horizontal width of the lower gate dielectric layer 28 may be substantially the same as that of a neighboring one of the plurality of second temporary gate electrodes 32, or may be larger than that of a neighboring one of the plurality of second temporary gate electrodes 32.

[0089] Referring to FIGS. 2 and 42, the first gate spacer 41 may be formed on the sidewalls of the plurality of first temporary gate electrodes 31 and the second mask pattern 33. The second gate spacer 42 may be formed on the sidewalls of the plurality of second temporary gate electrodes 32 and the third mask pattern 34. The first gate spacer 41 may have various thicknesses and shapes. In an exemplary embodiment, the portion of the first gate spacer 41 that is located between the plurality of first temporary gate electrodes 31 and the first active region 21 may be thicker than the lower gate dielectric layer 28. The outermost portion of the lower gate dielectric layer 28 may be aligned with the side surfaces of the plurality of second temporary gate electrodes 32. In an exemplary embodiment, the side surface of the lower gate dielectric layer 28 and the side surfaces of the plurality of second temporary gate electrodes 32 may form substantially the same plane.

[0090] Referring again to FIGS. 2 and 10, the portion of the first gate spacer 41 that is located between the first gate electrode 55 and the first active region 21 may be thicker than the lower gate dielectric layer 28. The outermost portion of the lower gate dielectric layer 28 may be aligned between the second gate spacer 42 and the second gate electrode 56.

[0091] FIGS. 43 to 46 are cross-sectional views illustrating stages in methods of forming semiconductor devices according to exemplary embodiments of the disclosure. FIGS. 43 to 46 are cross-sectional views along lines 1-1', 2-2', 3-3', 4-4' and 5-5' in FIG. 2.

[0092] Referring to FIGS. 2 and 43, the sacrificial buffer layer 127 may be formed on the buffer layer 27. A lower gate dielectric layer 28 may be formed on the second active region 22. In an exemplary embodiment, the sacrificial buffer layer 127 may include a material having etch selectivity with respect to the buffer layer 27. The lower gate dielectric layer 28 may be formed through the same process as the sacrificial buffer layer 127 simultaneously therewith, and may include substantially the same material as the sacrificial buffer layer 127. The buffer layer 27 may include silicon oxide or silicon oxynitride. The lower gate dielectric layer 28 and the sacrificial buffer layer 127 may include silicon oxynitride or silicon nitride.

[0093] Referring to FIGS. 2 and 44, a plurality of first temporary gate electrodes 31, a plurality of second temporary gate electrodes 32, a second mask pattern 33, and a third mask pattern 34 may be formed.

[0094] Referring to FIGS. 2 and 45, the first active region 21 may be exposed by partially removing the sacrificial buffer layer 127 and the buffer layer 27. The sacrificial buffer layer 127 may be preserved under the plurality of first

temporary gate electrodes 31. The sacrificial buffer layer 127 may have substantially the same horizontal width as a neighboring one of the plurality of first temporary gate electrodes 31. A first undercut region UC1 may be formed under the sacrificial buffer layer 127. The lower gate dielectric layer 28 may be partially removed to expose the second active region 22 during the process of removing the sacrificial buffer layer 127. The lower gate dielectric layer 28 may have substantially the same horizontal width as a neighboring one of the plurality of second temporary gate electrodes 32.

[0095] Referring to FIGS. 2 and 46, the first gate spacer 41 may be formed on the sidewalls of the plurality of first temporary gate electrodes 31 and the second mask pattern 33. The second gate spacer 42 may be formed on the sidewalls of the plurality of second temporary gate electrodes 32 and the third mask pattern 34.

[0096] Referring again to FIGS. 2 and 11, the outermost portion of the lower gate dielectric layer 28 may be aligned between the second gate spacer 42 and the second gate electrode 56.

[0097] FIGS. 47 to 51 are cross-sectional views illustrating stages in methods of forming semiconductor devices according to exemplary embodiments of the disclosure. FIGS. 47 to 51 are cross-sectional views along lines 1-1', 2-2', 3-3', 4-4' and 5-5' in FIG. 2.

[0098] Referring to FIGS. 2 and 47, the buffer layer 27 and the sacrificial buffer layer 127 may be sequentially stacked on the first region 11 and the second region 12. The buffer layer 27 and the sacrificial buffer layer 127 may cover the first active region 21 and the second active region 22. In an exemplary embodiment, the sacrificial buffer layer 127 may include a material having etch selectivity with respect to the buffer layer 27. The buffer layer 27 may include silicon oxide or silicon oxynitride. The sacrificial buffer layer 127 may include silicon oxynitride or silicon nitride. A first mask pattern 29 may be formed to cover the first region 11 and expose the second region 12.

[0099] Referring to FIGS. 2 and 48, the buffer layer 27 may be exposed by removing the sacrificial buffer layer 127 in the second region 12.

[0100] Referring to FIGS. 2 and 49, the sacrificial buffer layer 127 in the first region 11 may be exposed by removing the first mask pattern 29. The second active region 22 may be exposed by removing the buffer layer 27 in the second region 12.

[0101] Referring to FIGS. 2 and 50, the buffer layer 27 may be exposed by removing the sacrificial buffer layer 127 in the first region 11. The buffer layer 27 may cover the first active region 21.

[0102] Referring to FIGS. 2 and 51, an upper buffer layer 227 may be formed on the buffer layer 27 in the first region 11. A lower gate dielectric layer 28 may be formed on the second active region 22. The lower gate dielectric layer 28 may be formed through the same process as the upper buffer layer 227 simultaneously therewith, and may include substantially the same material as the upper buffer layer 227.

[0103] Subsequently, semiconductor devices may be formed in a manner similar to that described with reference to FIGS. 38 to 46.

[0104] FIGS. 52 to 54 are cross-sectional views illustrating stages in methods of forming semiconductor devices according to exemplary embodiments of the disclosure.

FIGS. 52 to 54 are cross-sectional views along lines 1-1', 2-2', 3-3', 4-4' and 5-5' in FIG. 2.

[0105] Referring to FIGS. 2 and 52, a buffer layer 27, a lower gate dielectric layer 28, a plurality of first temporary gate electrodes 31, a plurality of second temporary gate electrodes 32, a second mask pattern 33, and a third mask pattern 34 may be formed. The lower gate dielectric layer 28 may be formed through the same process as the buffer layer 27 simultaneously therewith, and may include substantially the same material as the buffer layer 27.

[0106] Referring to FIGS. 2 and 53, the first active region 21 may be exposed between the plurality of first temporary gate electrodes 31 by partially removing the buffer layer 27. The buffer layer 27 may have a smaller horizontal width than each of the plurality of first temporary gate electrodes 31. A first undercut region UC1 may be formed under the plurality of first temporary gate electrodes 31.

[0107] The second active region 22 may be exposed between the plurality of second temporary gate electrodes 32 by partially removing the lower gate dielectric layer 28. The lower gate dielectric layer 28 may be preserved between the plurality of second temporary gate electrodes 32 and the second active region 22. The lower gate dielectric layer 28 may have a smaller horizontal width than each of the plurality of second temporary gate electrodes 32. A second undercut region UC2 may be formed under the plurality of second temporary gate electrodes 32. In an exemplary embodiment, the second undercut region UC2 may be formed between the plurality of second temporary gate electrodes 32 and the second active region 22. Formation of the first undercut region UC1 and formation of the second undercut region UC2 may be performed simultaneously through the same process.

[0108] Referring to FIGS. 2 and 54, the first gate spacer 41 may be formed on the sidewalls of the plurality of first temporary gate electrodes 31 and the second mask pattern 33. The second gate spacer 42 may be formed on the sidewalls of the plurality of second temporary gate electrodes 32 and the third mask pattern 34. The first gate spacer 41 may include the first inner spacer 41A and the first outer spacer 41B. The second gate spacer 42 may include the second inner spacer 42A and the second outer spacer 42B. In an exemplary embodiment, the second gate spacer 42 may have a shape similar to that of the first gate spacer 41.

[0109] The second inner spacer 42A may be formed on the sidewalls of the plurality of second temporary gate electrodes 32 and the third mask pattern 34. The second inner spacer 42A may extend in the second undercut region UC2. The second inner spacer 42A may be in contact with the bottom surfaces of the plurality of second temporary gate electrodes 32 and with the second active region 22. The second inner spacer 42A may be in contact with the side surface of the lower gate dielectric layer 28.

[0110] Referring again to FIGS. 2 and 12, the first gate spacer 41 may extend in the first undercut region UC1 between the first active region 21 and the first gate electrode 55. The lower gate dielectric layer 28 may have a smaller horizontal width than the second gate electrode 56. The second gate spacer 42 may extend in the second undercut region UC2 between the second active region 22 and the second gate electrode 56.

[0111] FIGS. 55 to 57 are cross-sectional views illustrating stages in methods of forming semiconductor devices accord-

ing to exemplary embodiments of the disclosure. FIGS. 55 to 57 are cross-sectional views along lines 1-1', 2-2', 3-3', 4-4' and 5-5' in FIG. 2.

[0112] Referring to FIGS. 2 and 55, a buffer layer 27, a lower gate dielectric layer 28, a plurality of first temporary gate electrodes 31, a plurality of second temporary gate electrodes 32, a second mask pattern 33, and a third mask pattern 34 may be formed.

[0113] A first active region 21 may be exposed between the plurality of first temporary gate electrodes 31. The buffer layer 27 may be preserved between the plurality of first temporary gate electrodes 31 and the first active region 21. The buffer layer 27 may have substantially the same horizontal width as a neighboring one of the plurality of first temporary gate electrodes 31. The side surface of the buffer layer 27 and the side surfaces of the plurality of first temporary gate electrodes 31 may form substantially the same plane.

[0114] A second active region 22 may be exposed between the plurality of second temporary gate electrodes 32. The lower gate dielectric layer 28 may be preserved between the plurality of second temporary gate electrodes 32 and the second active region 22. The lower gate dielectric layer 28 may have substantially the same horizontal width as a neighboring one of the plurality of second temporary gate electrodes 32. The side surface of the lower gate dielectric layer 28 and the side surfaces of the plurality of second temporary gate electrodes 32 may form substantially the same plane.

[0115] Referring to FIGS. 2 and 56, the fourth mask pattern 35 may be formed to cover the first region 11. A second undercut region UC2 may be formed under the plurality of second temporary gate electrodes 32 by partially removing the lower gate dielectric layer 28. The lower gate dielectric layer 28 may have a smaller horizontal width than each of the plurality of second temporary gate electrodes 32. In an exemplary embodiment, the second undercut region UC2 may be formed between the plurality of second temporary gate electrodes 32 and the second active region 22.

[0116] Referring to FIGS. 2 and 57, the fourth mask pattern 35 may be removed. A first gate spacer 41 may be formed on the sidewalls of the plurality of first temporary gate electrodes 31 and the second mask pattern 33. A second gate spacer 42 may be formed on the sidewalls of the plurality of second temporary gate electrodes 32 and the third mask pattern 34.

[0117] The first inner spacer 41A may be formed on the sidewalls of the plurality of first temporary gate electrodes 31 and the second mask pattern 33. The first inner spacer 41A may be in contact with the side surface of the buffer layer 27. The first inner spacer 41A may be aligned outside the plurality of first temporary gate electrodes 31. The second inner spacer 42A may be formed on the sidewalls of the plurality of second temporary gate electrodes 32 and the third mask pattern 34. The second inner spacer 42A may extend in the second undercut region UC2. The second inner spacer 42A may be in contact with the bottom surfaces of the plurality of second temporary gate electrodes 32 and with the second active region 22. The second inner spacer 42A may be in contact with the side surface of the lower gate dielectric layer 28.

[0118] Referring again to FIGS. 2 and 13, the first gate spacer 41 may be formed on the side surface of the first gate electrode 55. The first gate dielectric layer 53 may be formed

between the first gate electrode 55 and the first active region 21 and between the first gate electrode 55 and the first gate spacer 41. The lower gate dielectric layer 28 may have a smaller horizontal width than the second gate electrode 56. The second gate spacer 42 may extend in the second undercut region UC2 between the second active region 22 and the second gate electrode 56.

[0119] By way of summation and review, optimized shapes of gate spacers and replacement gate electrodes are required. Therefore, exemplary embodiments provide semiconductor devices with optimized gate spacer shapes, thereby improving electrical properties of the semiconductor devices and methods of forming the same.

[0120] That is, according to the exemplary embodiments, a semiconductor device includes a gate spacer on a side surface of a gate electrode, such that the gate spacer extends into an undercut region between the gate electrode and an active region. Due to the gate spacer, defects in the process of forming the gate electrode may be greatly reduced, and therefore, semiconductor devices having excellent electrical properties may be realized.

[0121] Example embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.

What is claimed is:

1. A method of forming a semiconductor device, the method comprising:

- defining a first active region and a second active region on a substrate;
- forming a buffer layer on the first active region;
- forming a lower gate dielectric layer on the second active region;
- forming a first temporary gate electrode on the buffer layer and a second temporary gate electrode on the lower gate dielectric layer;
- partially removing the buffer layer to form an undercut region between the first active region and the first temporary gate electrode;
- forming a first gate spacer on a side surface of the first temporary gate electrode and extending in the undercut region and a second gate spacer on a side surface of the second temporary gate electrode;
- forming a first drain region in the first active region at a position adjacent to the first temporary gate electrode and a second drain region in the second active region at a position adjacent to the second temporary gate electrode;
- removing the first temporary gate electrode and the buffer layer;
- forming a first gate electrode in a region from which the first temporary gate electrode and the buffer layer are removed;
- removing the second temporary gate electrode; and

forming a second gate electrode in a region from which the second temporary gate electrode is removed.

2. The method as claimed in claim 1, wherein forming the undercut region further includes, before the partially removing the buffer layer, forming a sacrificial spacer on a side surface of the second temporary gate electrode.

3. The method as claimed in claim 2, wherein the sacrificial spacer is in contact with a top surface of the lower gate dielectric layer and a side surface of the second temporary gate electrode.

4. The method as claimed in claim 1, wherein the first gate spacer includes:

- an upper portion disposed on a side surface of the first gate electrode; and
- a lower portion extending from the upper portion into the undercut region.

5. The method as claimed in claim 4, wherein the lower portion extends between the first active region and the first gate electrode.

6. The method as claimed in claim 4, wherein:
the first active region includes a plurality of channel regions, each of the plurality of channel regions being in contact with the first drain region, and
the first gate electrode surrounding a top surface, a side surface, and a bottom surface of at least one of the plurality of channel regions.

7. The method as claimed in claim 6, further comprising forming a first gate dielectric layer between the first gate electrode and the plurality of channel regions, such that the first gate dielectric layer extends between the first gate electrode and the first gate spacer, and the first gate dielectric layer is in contact with a side surface and a top surface of the lower portion.

8. The method as claimed in claim 1, further comprising forming a second gate dielectric layer between the lower gate dielectric layer and the second gate electrode, such that the second gate dielectric layer extends between the second gate spacer and the second gate electrode.

9. The method as claimed in claim 1, wherein the second gate electrode has a larger horizontal width than the first gate electrode, and the lower gate dielectric layer has a larger horizontal width than the second gate electrode.

10. The method as claimed in claim 1, wherein the lower gate dielectric layer protrudes beyond the second gate electrode.

11. The method as claimed in claim 1, wherein the second gate spacer is in contact with a top surface and a side surface of the lower gate dielectric layer.

12. The method as claimed in claim 1, wherein the lower gate dielectric layer has a smaller horizontal width than the second gate electrode, and the second gate spacer extends between the second active region and the second gate electrode.

13. A method of forming a semiconductor device, the method comprising:

- defining a first active region and a second active region on a substrate;
- forming a buffer layer on the first active region and a lower gate dielectric layer on the second active region;
- forming a first temporary gate electrode on the buffer layer and a second temporary gate electrode on the lower gate dielectric layer;
- forming a sacrificial spacer on a side surface of the second temporary gate electrode;

partially removing the buffer layer to form an undercut region between the first active region and the first temporary gate electrode;

removing the sacrificial spacer;

forming a first gate spacer on a side surface of the first temporary gate electrode and a second gate spacer on a side surface of the second temporary gate electrode;

removing the first temporary gate electrode and the buffer layer to form a first gate electrode; and

removing the second temporary gate electrode to form a second gate electrode.

14. The method as claimed in claim 13, wherein the buffer layer and the lower gate dielectric layer are formed simultaneously.

15. The method as claimed in claim 13, wherein in the forming of the first temporary gate electrode and the second temporary gate electrode, the buffer layer and the lower gate dielectric layer are partially etched and are reduced in thickness outside the first temporary gate electrode and the second temporary gate electrode.

16. The method as claimed in claim 13, wherein a bottom surface of the sacrificial spacer is in contact with a top surface of the lower gate dielectric layer outside the second temporary gate electrode.

17. The method as claimed in claim 13, wherein the lower gate dielectric layer has a larger horizontal width than the second gate electrode.

18. A method of forming a semiconductor device, the method comprising:

- defining a first active region on a substrate;
- forming a buffer layer on the first active region;
- forming a first temporary gate electrode on the buffer layer;

partially removing the buffer layer to form an undercut region between the first active region and the first temporary gate electrode;

forming a first gate spacer on a side surface of the first temporary gate electrode;

forming a first drain region in the first active region at a position adjacent to the first temporary gate electrode;

removing the first temporary gate electrode and the buffer layer; and

forming a first gate dielectric layer and a first gate electrode in a region from which the first temporary gate electrode and the buffer layer are removed,

wherein:

the first active region includes a plurality of channel regions, each of the plurality of channel regions being in contact with the first drain region,

the first gate electrode surrounds a top surface, a side surface, and a bottom surface of at least one of the plurality of channel regions,

wherein the first gate spacer includes:

- an upper portion disposed on a side surface of the first gate electrode; and

- a lower portion extending from the upper portion into the undercut region, and

wherein the first gate dielectric layer extends between the first gate electrode and the first gate spacer and is in contact with a side surface and a portion of a top surface of the lower portion.

19. The method as claimed in claim 18, wherein the first gate spacer has a shape of L or inverted T.

20. The method as claimed in claim **18**, wherein the lower portion extends between the first active region and the first gate electrode.

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