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(54) **VARIABLE OUTPUT IMPEDANCE RF GENERATOR**

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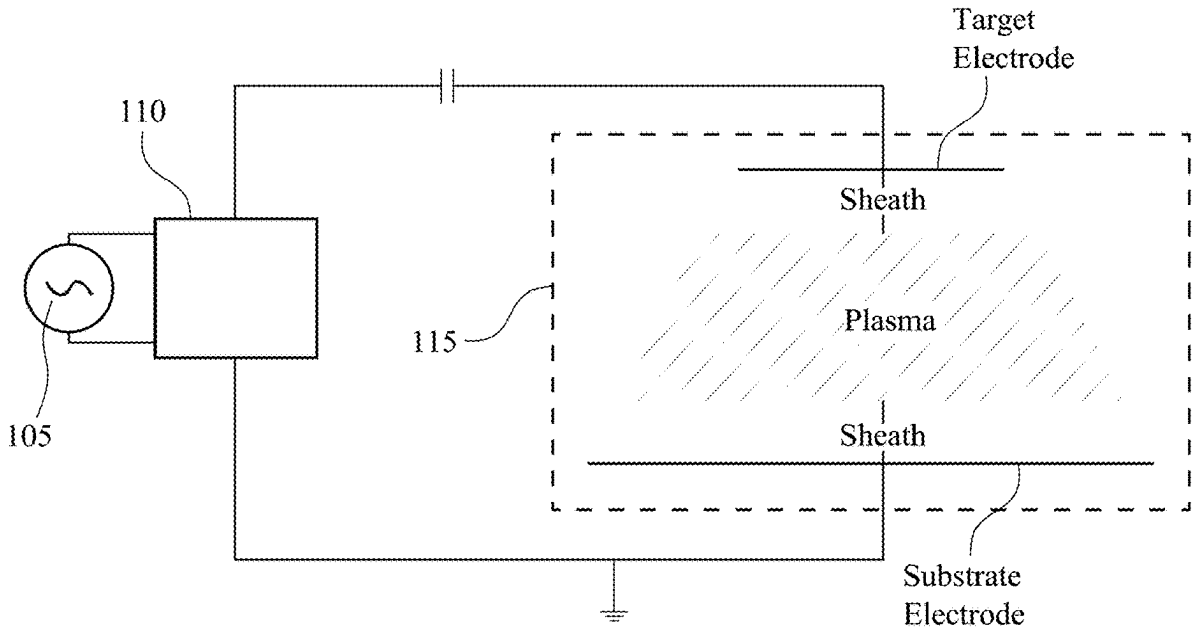
(57) **ABSTRACT**

Various RF plasma systems are disclosed that do not require a matching network. In some embodiments, the RF plasma system includes an energy storage capacitor; a switching circuit coupled with the energy storage capacitor, the switching circuit producing a plurality of pulses with a pulse amplitude and a pulse frequency, the pulse amplitude being greater than 100 volts; a resonant circuit coupled with the switching circuit. In some embodiments, the resonant circuit includes: a transformer having a primary side and a secondary side; and at least one of a capacitor, an inductor, and a resistor. In some embodiments, the resonant circuit having a resonant frequency substantially equal to the pulse frequency, and the resonant circuit increases the pulse amplitude to a voltage greater than 2 kV.



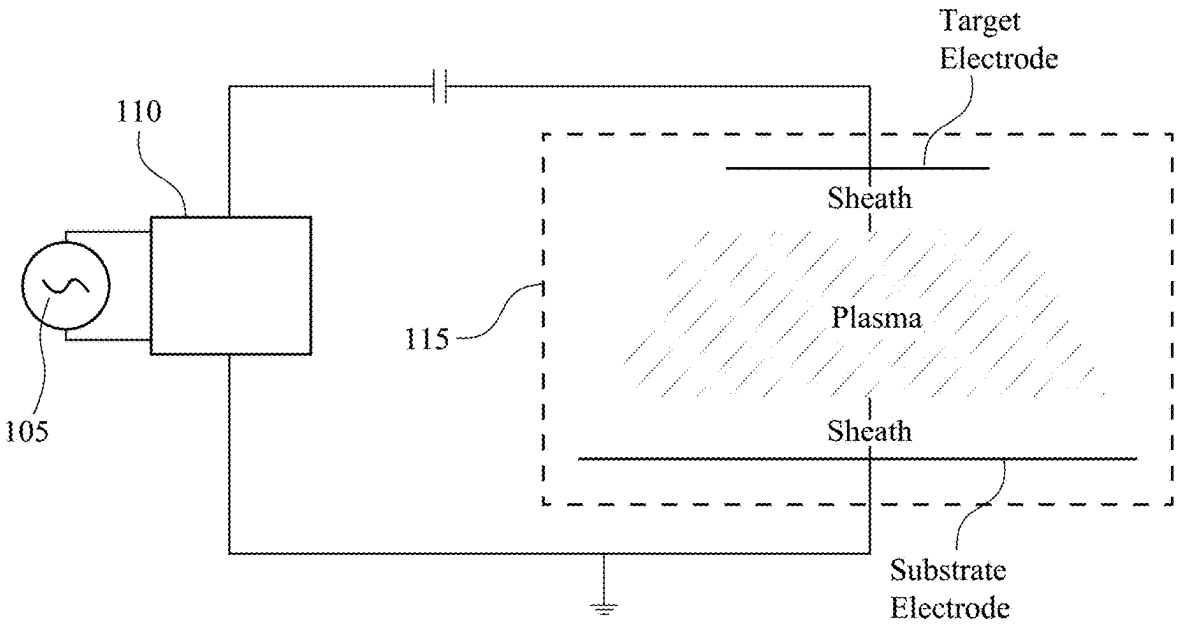

Target
Electrode
110
Sheath
115
Plasma
105
Sheath
Substrate
Electrode

FIG. 1

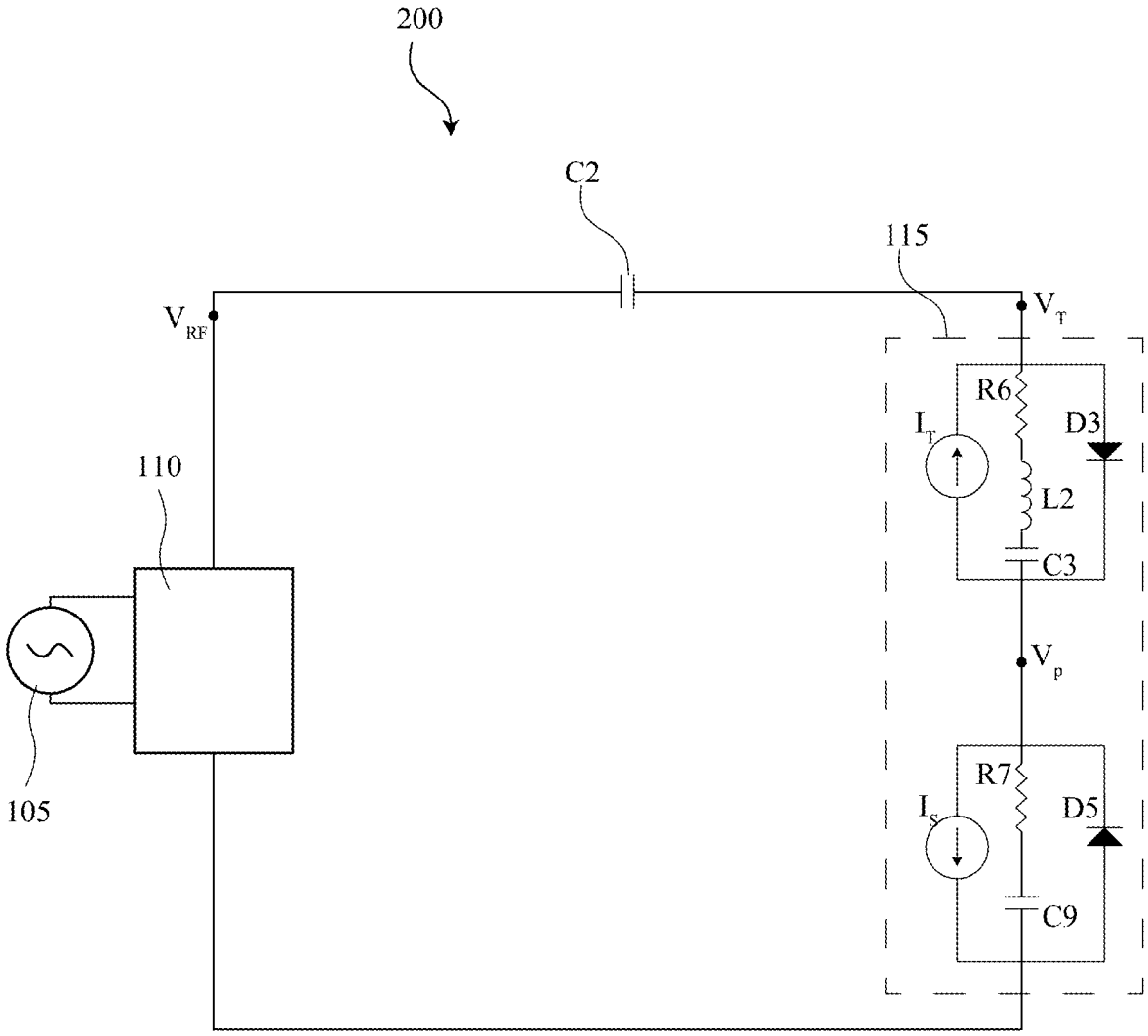


FIG. 2

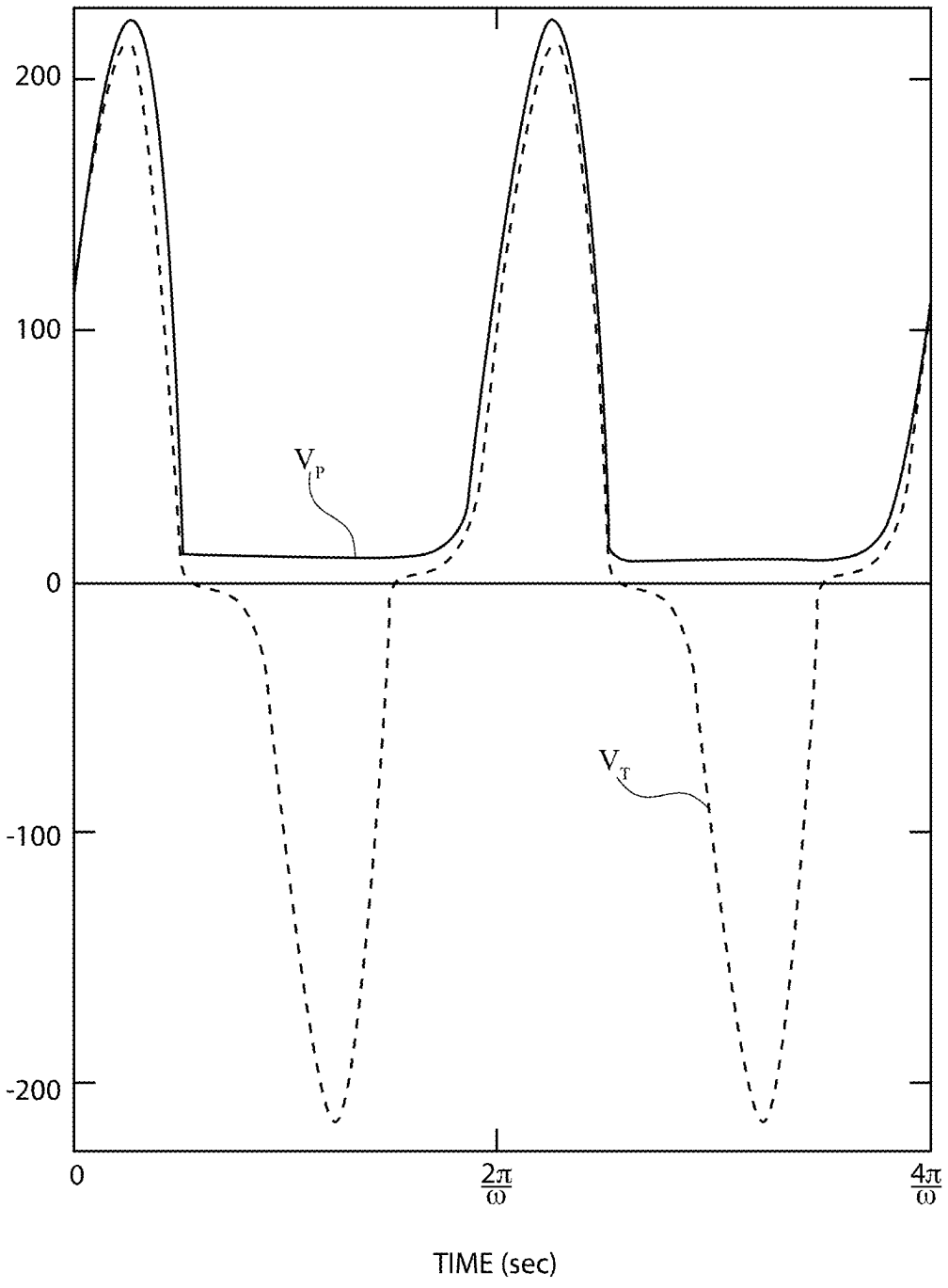


FIG. 3

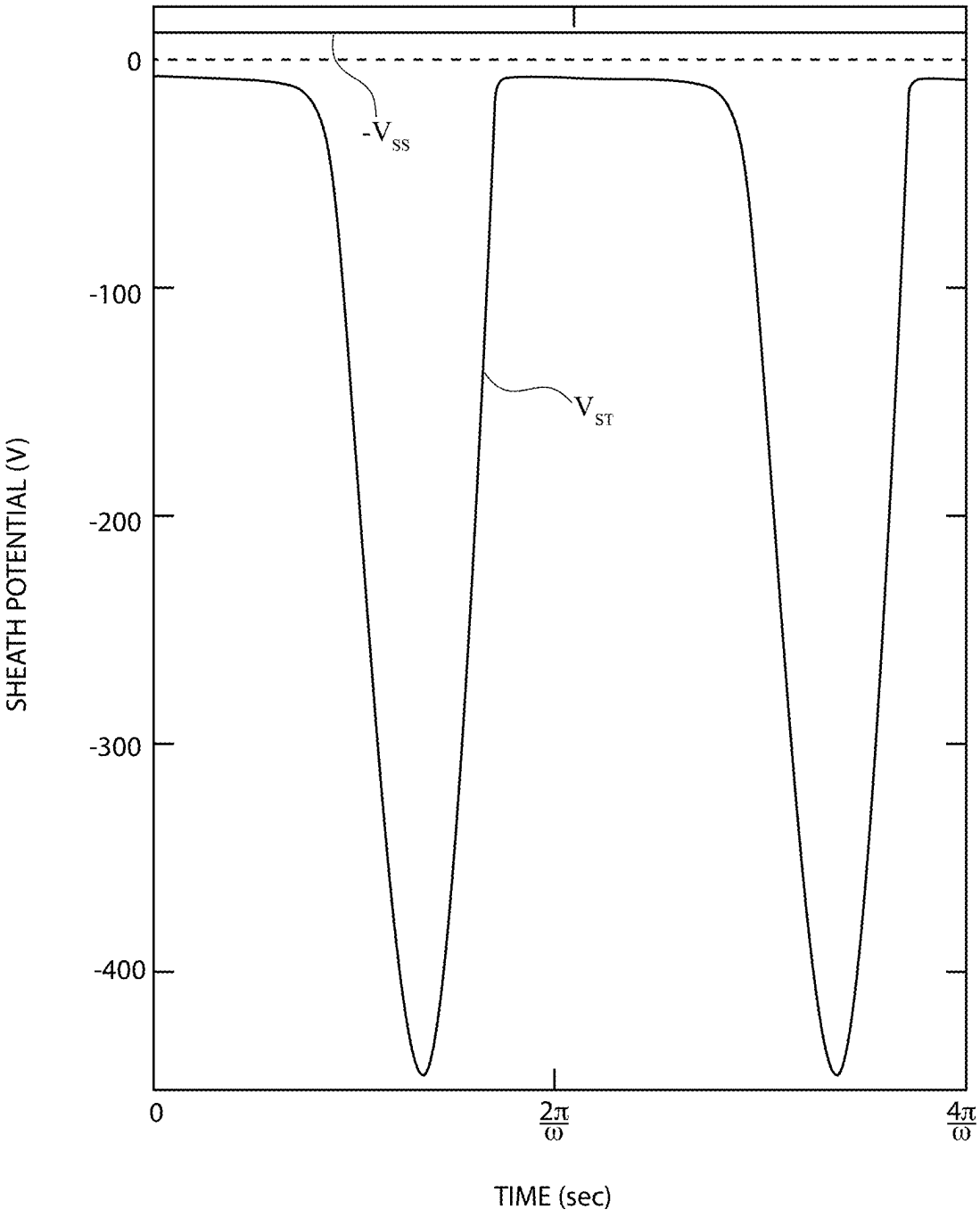

0
-100
-200
-300
-400
SHEATH POTENTIAL (V)
$-V_{SS}$
V_{ST}
0
$\frac{2\pi}{\omega}$
$\frac{4\pi}{\omega}$
TIME (sec)

FIG. 4

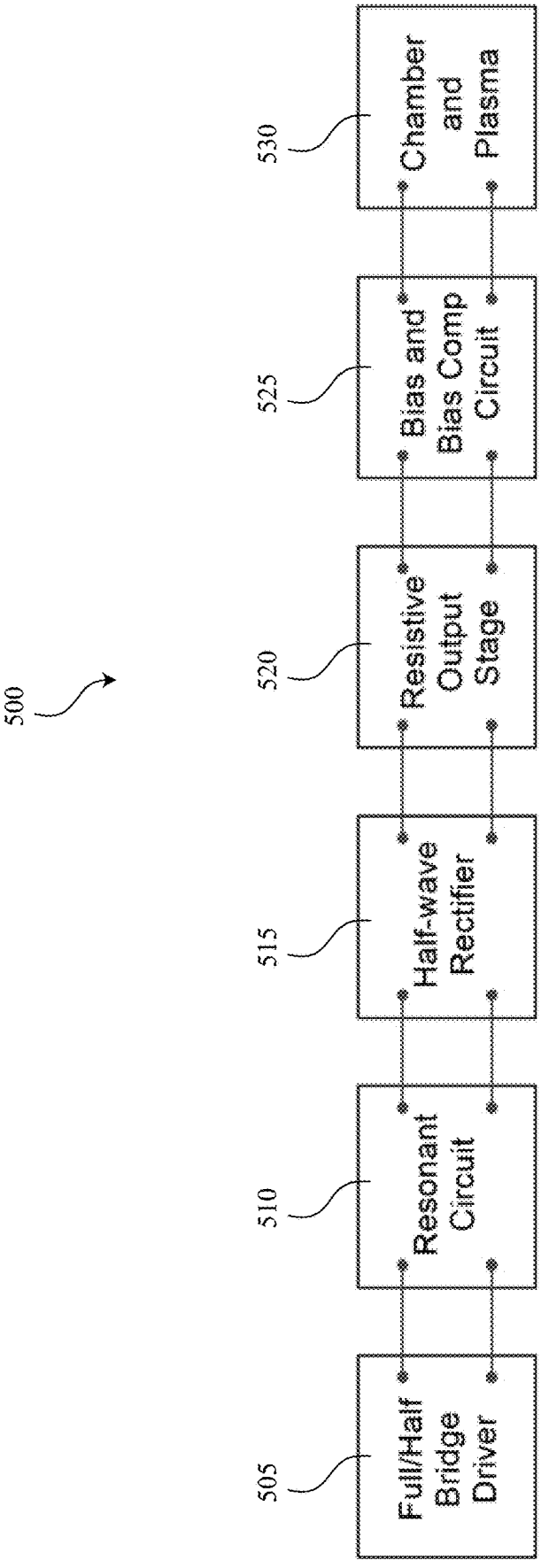

500
505
Full/Half Bridge Driver
510
Resonant Circuit
515
Half-wave Rectifier
520
Resistive Output Stage
525
Bias and Bias Comp Circuit
530
Chamber and Plasma

FIG. 5

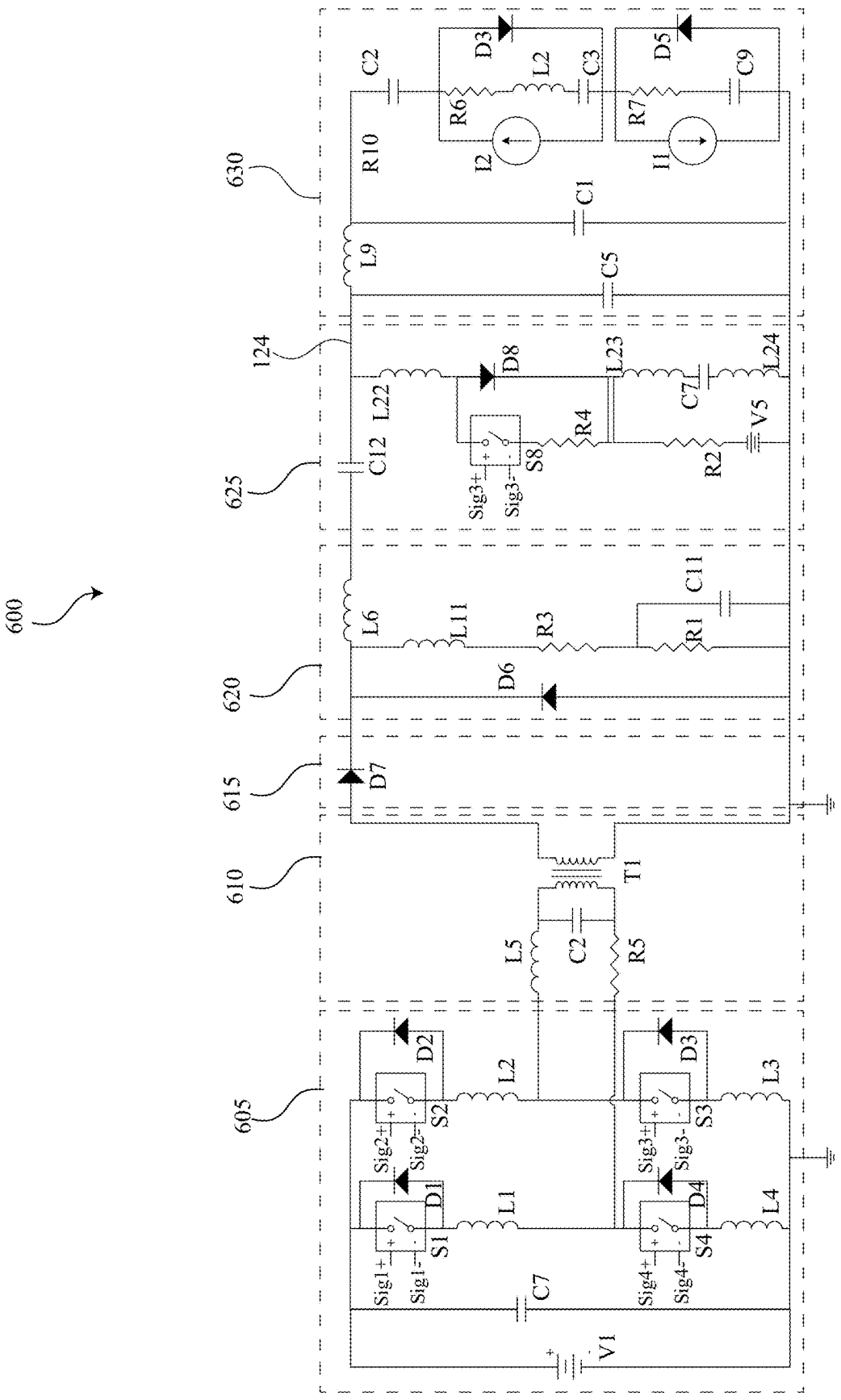

600
605
610
615
620
625
630
124
C2
D3
L2
C3
D5
C9
R6
R7
I2
I1
R10
C1
L9
C5
D8
L23
L24
C7
L22
C12
R4
V5
S8
R2
Sig3+
Sig3-
L6
L11
R3
C11
R1
D6
D7
T1
L5
C2
R5
D2
L2
D3
L3
S2
S3
Sig2+
Sig2-
Sig3+
Sig3-
D1
D4
L1
L4
S1
S4
Sig1+
Sig1-
Sig4+
Sig4-
C7
V1

FIG. 6

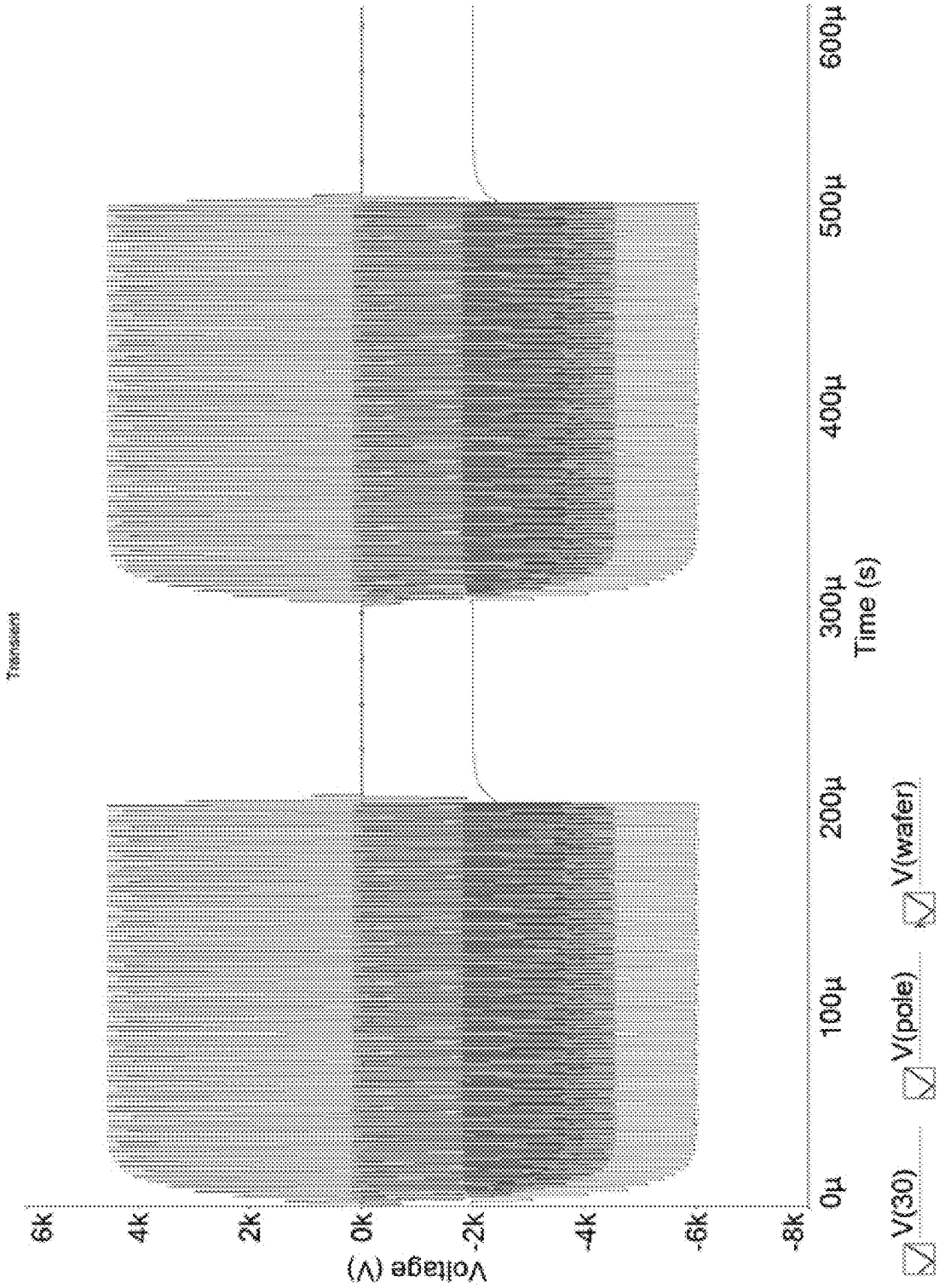

Transient
6k
4k
2k
0k
-2k
-4k
-6k
-8k
Voltage (V)
0µ
100µ
200µ
300µ
400µ
500µ
600µ
Time (s)
V(30)
V(pole)
V(wafer)

FIG. 7

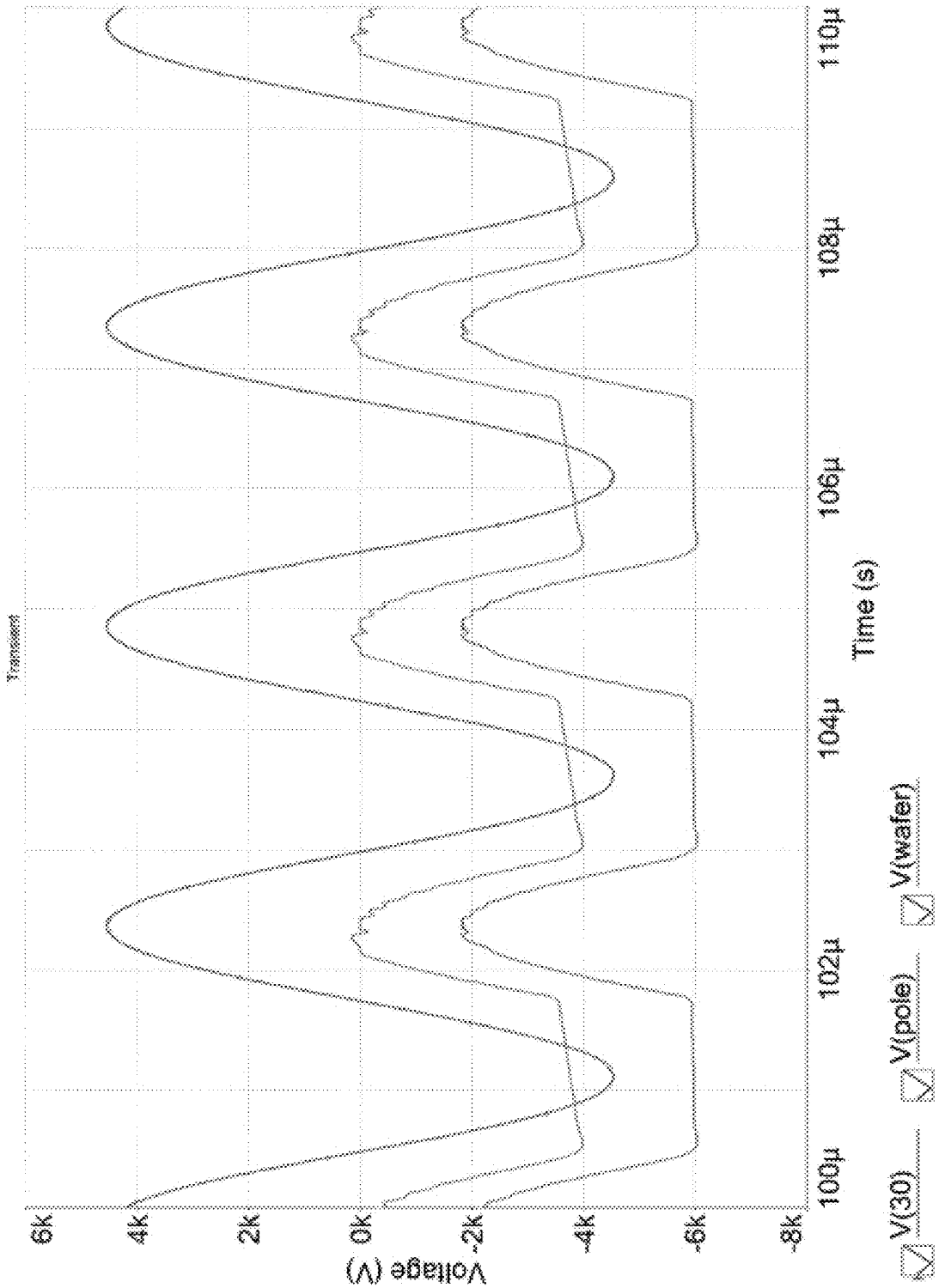

Transient
Voltage (V)
6k
4k
2k
0k
-2k
-4k
-6k
-8k
100µ
102µ
104µ
106µ
108µ
110µ
Time (s)
V(30)
V(pole)
V(wafer)

FIG. 8

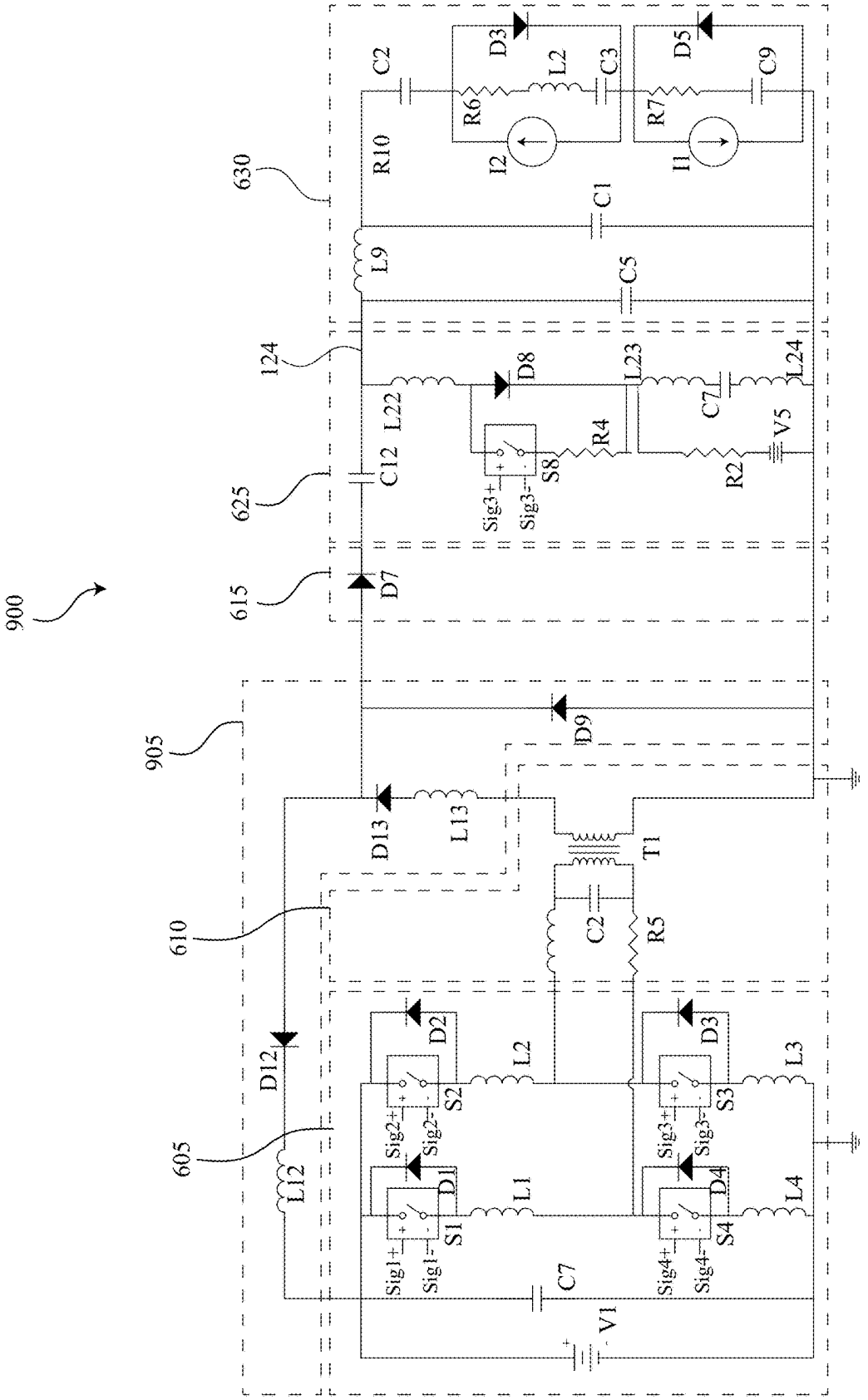

900
905
610
605
630
625
615
124
C2
D3
L2
C3
D5
C9
R6
R7
R10
I2
I1
C1
L9
C5
D8
L23
L24
L22
C7
V5
C12
R4
R2
S8
Sig3+
Sig3-
D7
D9
D13
L13
T1
C2
R5
D12
D2
D3
L2
L3
S2
S3
Sig2+
Sig2-
Sig3+
Sig3-
L12
D1
D4
L1
L4
S1
S4
Sig1+
Sig1-
Sig4+
Sig4-
C7
V1

FIG. 9

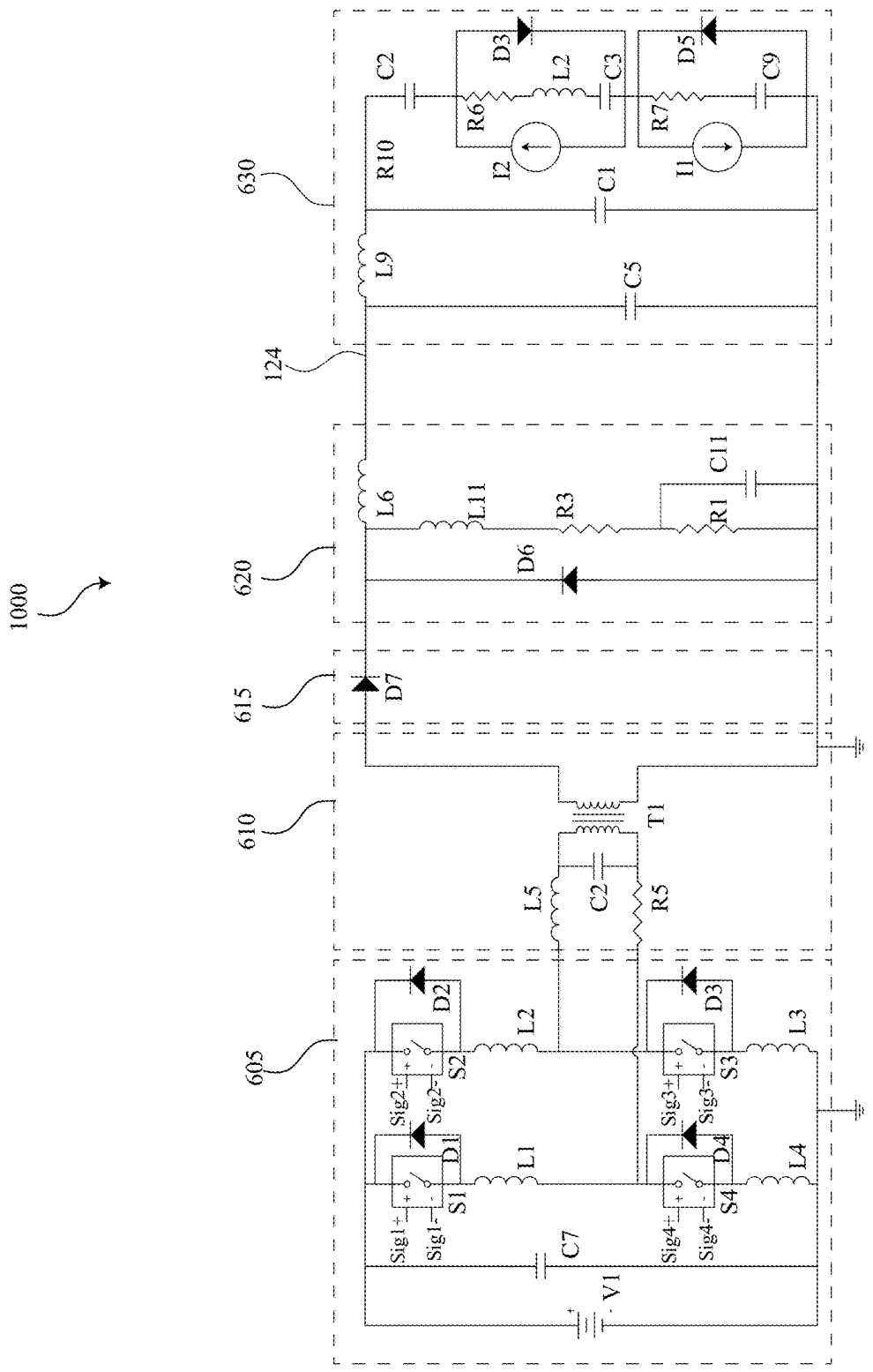

1000
630
620
615
610
605
124
C2
D3
L2
C3
D5
C9
R6
R7
R10
I2
I1
C1
L9
C5
L6
L11
R3
C11
R1
D6
D7
T1
L5
C2
R5
D2
D3
L2
L3
S2
S3
Sig2+
Sig2-
Sig3+
Sig3-
D1
D4
L1
L4
S1
S4
Sig1+
Sig1-
Sig4+
Sig4-
C7
V1

FIG. 10

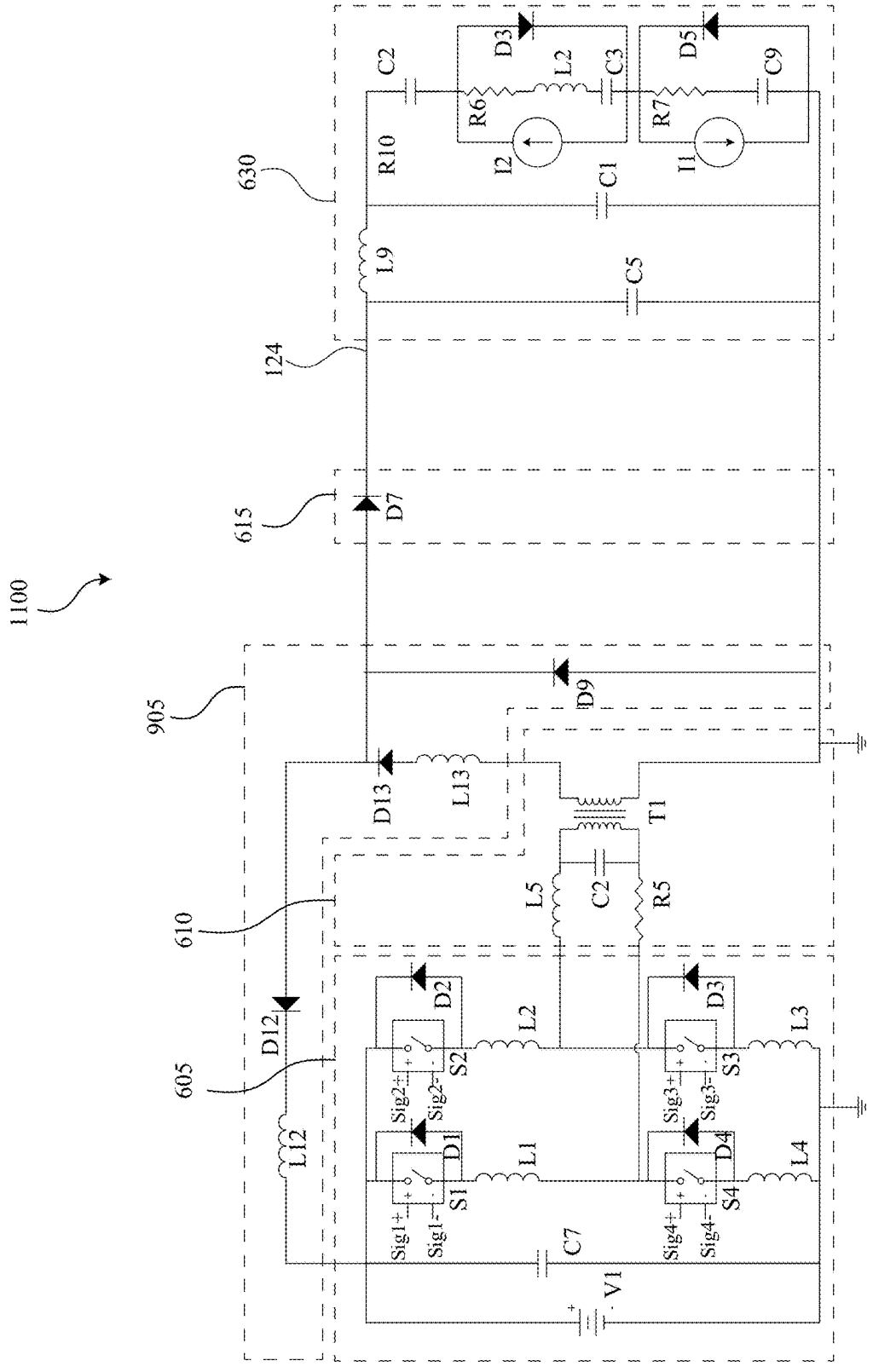

1100
905
610
605
615
630
124
D12
L12
D13
L13
D7
D9
T1
L5
C2
R5
D1
D2
D3
D4
L1
L2
L3
L4
S1
S2
S3
S4
Sig1+
Sig1-
Sig2+
Sig2-
Sig3+
Sig3-
Sig4+
Sig4-
C7
V1
C2
R10
D3
L2
C3
R6
I2
C1
D5
C9
R7
I1
L9
C5

FIG. 11

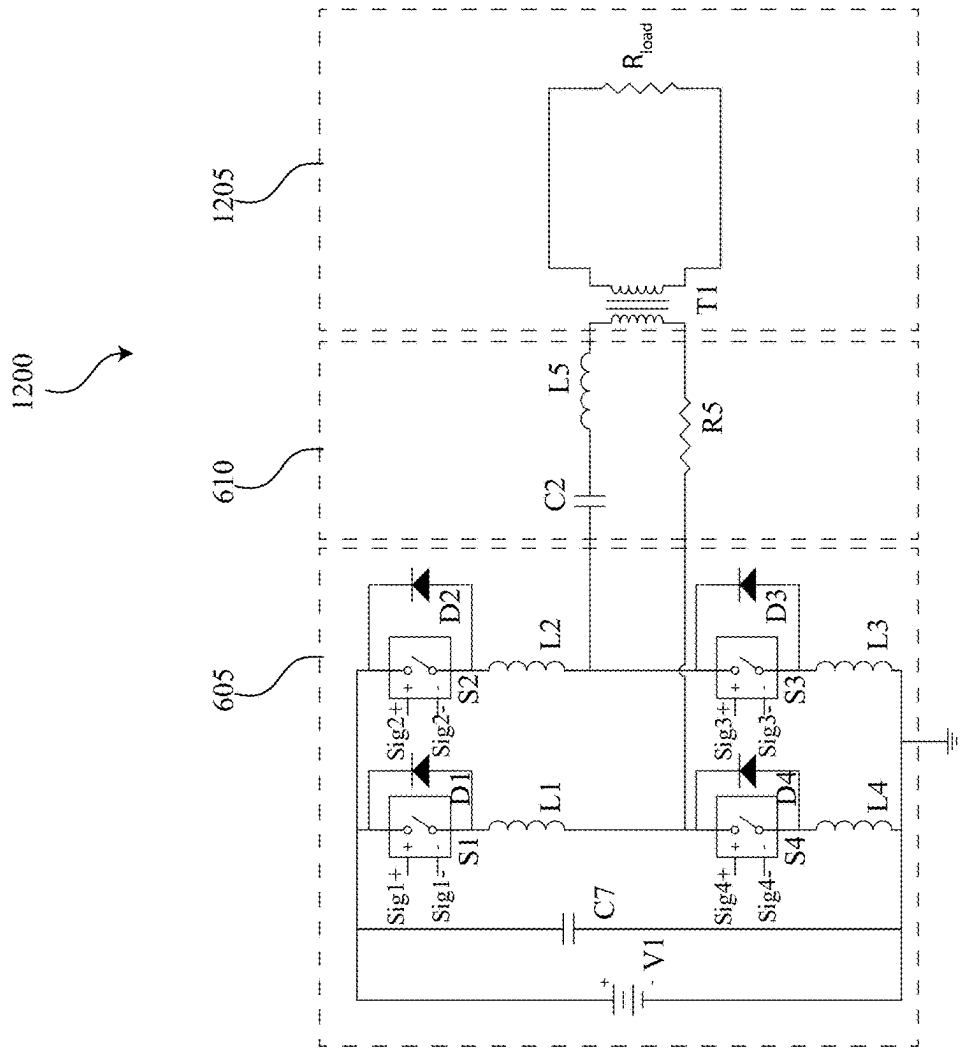

1200
1205
610
605
R_{load}
T1
L5
R5
C2
D2
D3
L2
L3
S2
S3
Sig2+
Sig2-
Sig3+
Sig3-
D1
D4
L1
L4
S1
S4
Sig1+
Sig1-
Sig4+
Sig4-
C7
V1

FIG. 12

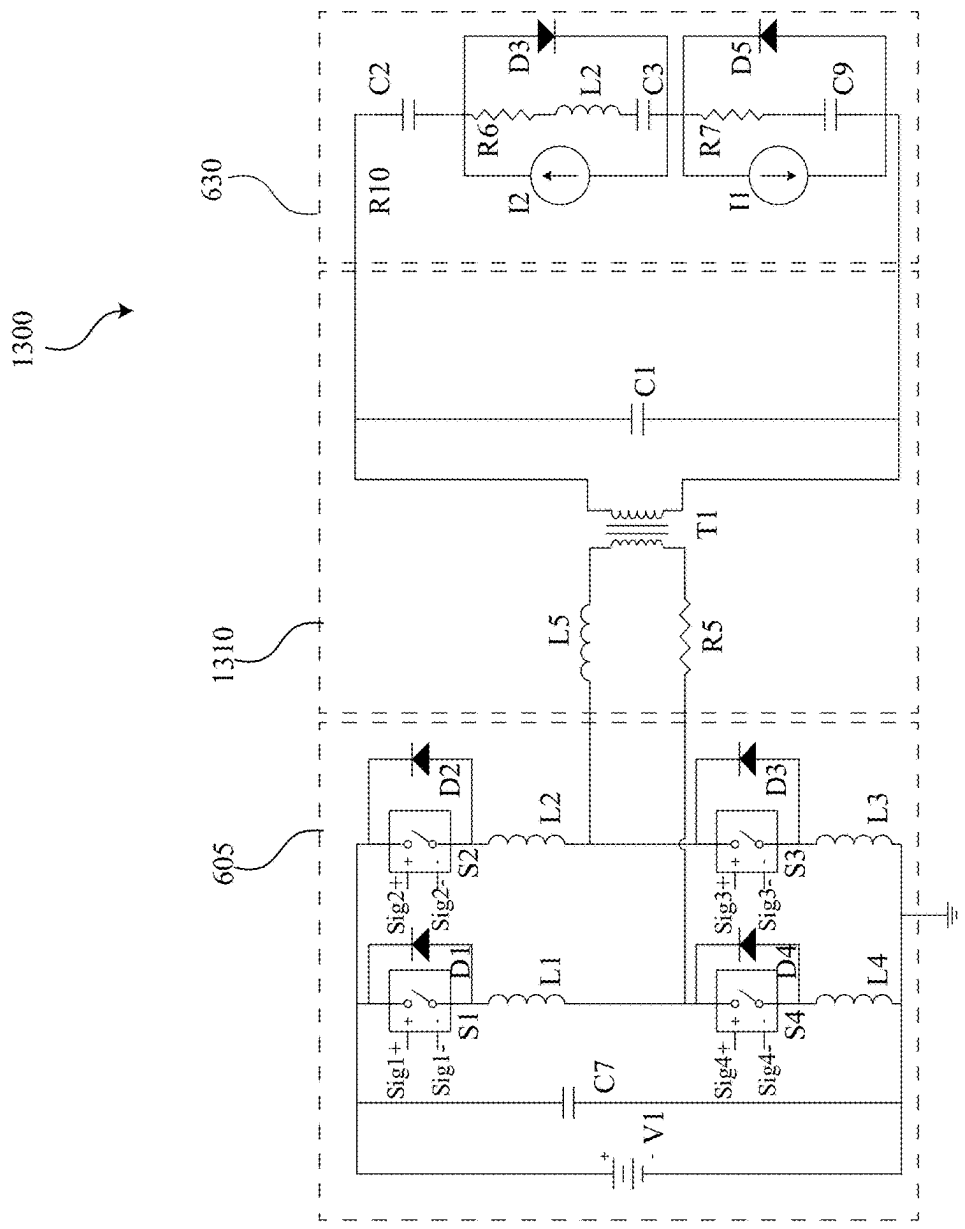

1300
630
1310
605
C2
D3
L2
C3
D5
C9
R6
R7
R10
I2
I1
C1
T1
L5
R5
D2
L2
D3
L3
S2
S3
Sig2+
Sig2-
Sig3+
Sig3-
D1
D4
L1
L4
S1
S4
Sig1+
Sig1-
Sig4+
Sig4-
C7
V1

FIG. 13

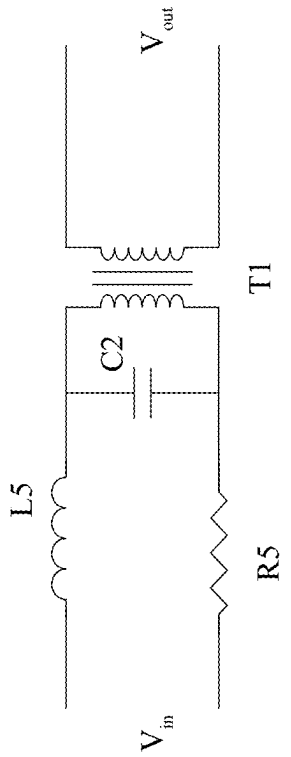


FIG. 14A

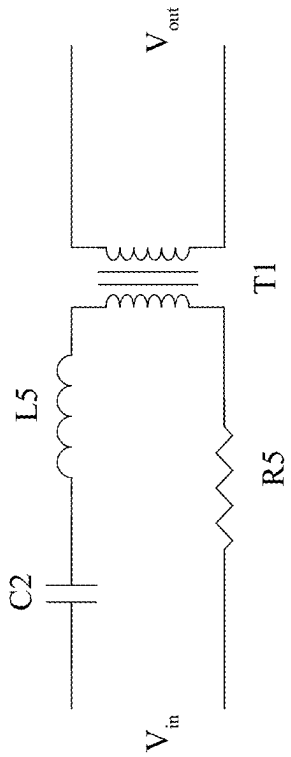


FIG. 14B

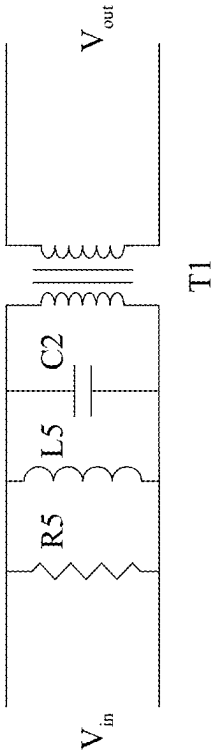


FIG. 15A

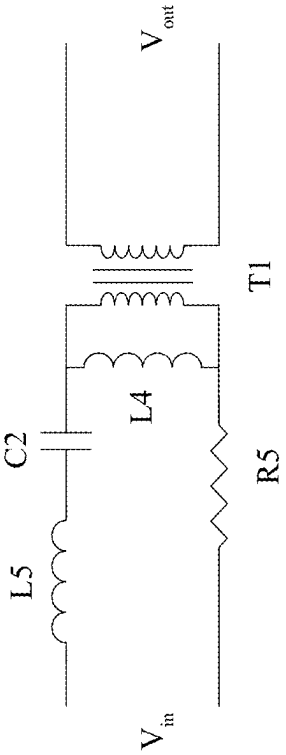


FIG. 15B

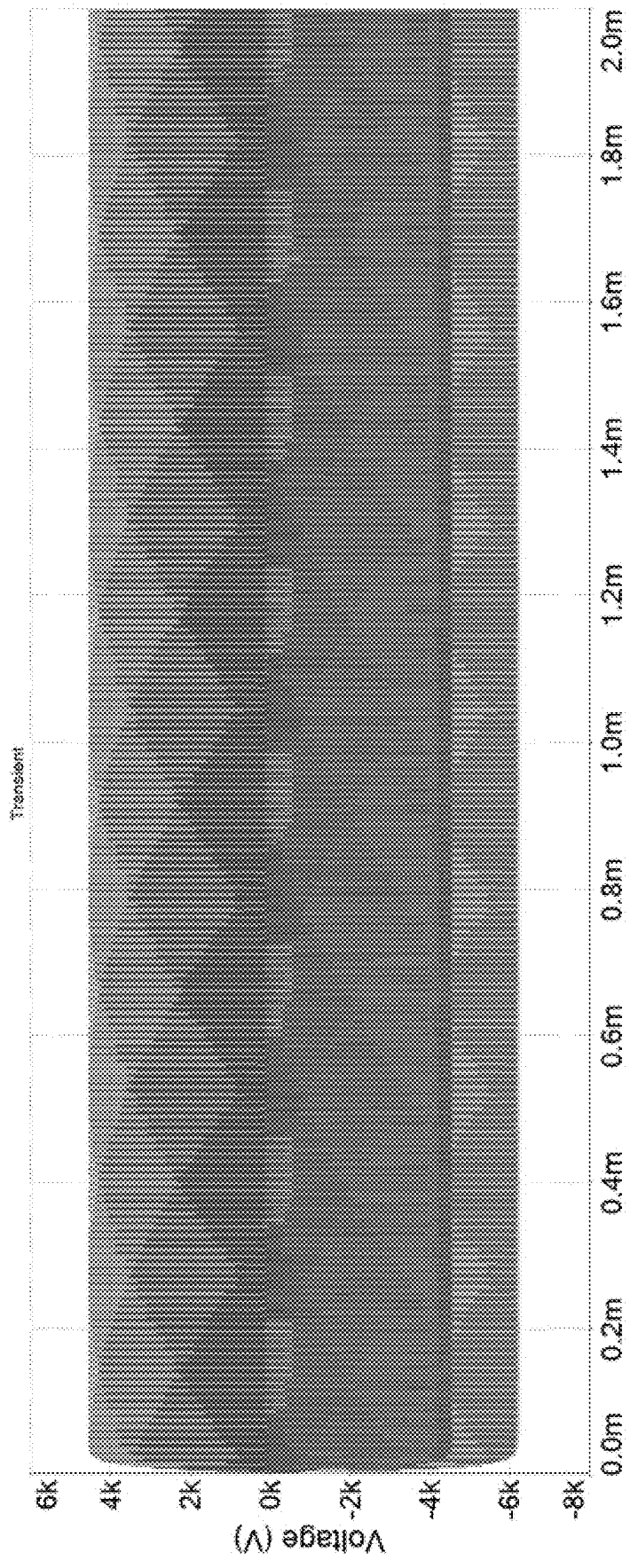

Transient
Voltage (V)
6k
4k
2k
0k
-2k
-4k
-6k
-8k
0.0m
0.2m
0.4m
0.6m
0.8m
1.0m
1.2m
1.4m
1.6m
1.8m
2.0m
Time (s)
V(30)
V(pole)
V(wafer)

FIG. 16

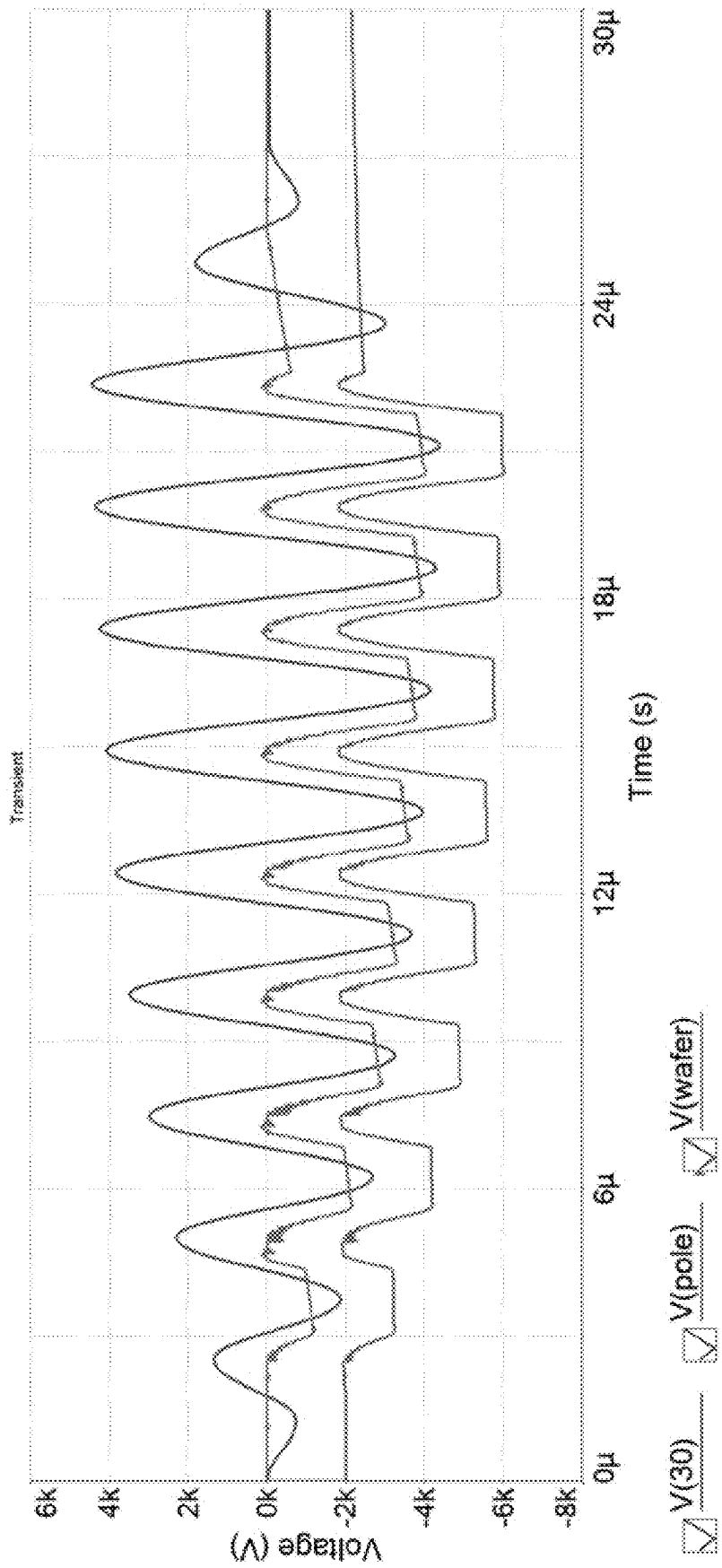

Transient
Voltage (V)
6k
4k
2k
0k
-2k
-4k
-6k
-8k
0µ
6µ
12µ
18µ
24µ
30µ
Time (s)
V(30)
V(pole)
V(wafer)

FIG. 17

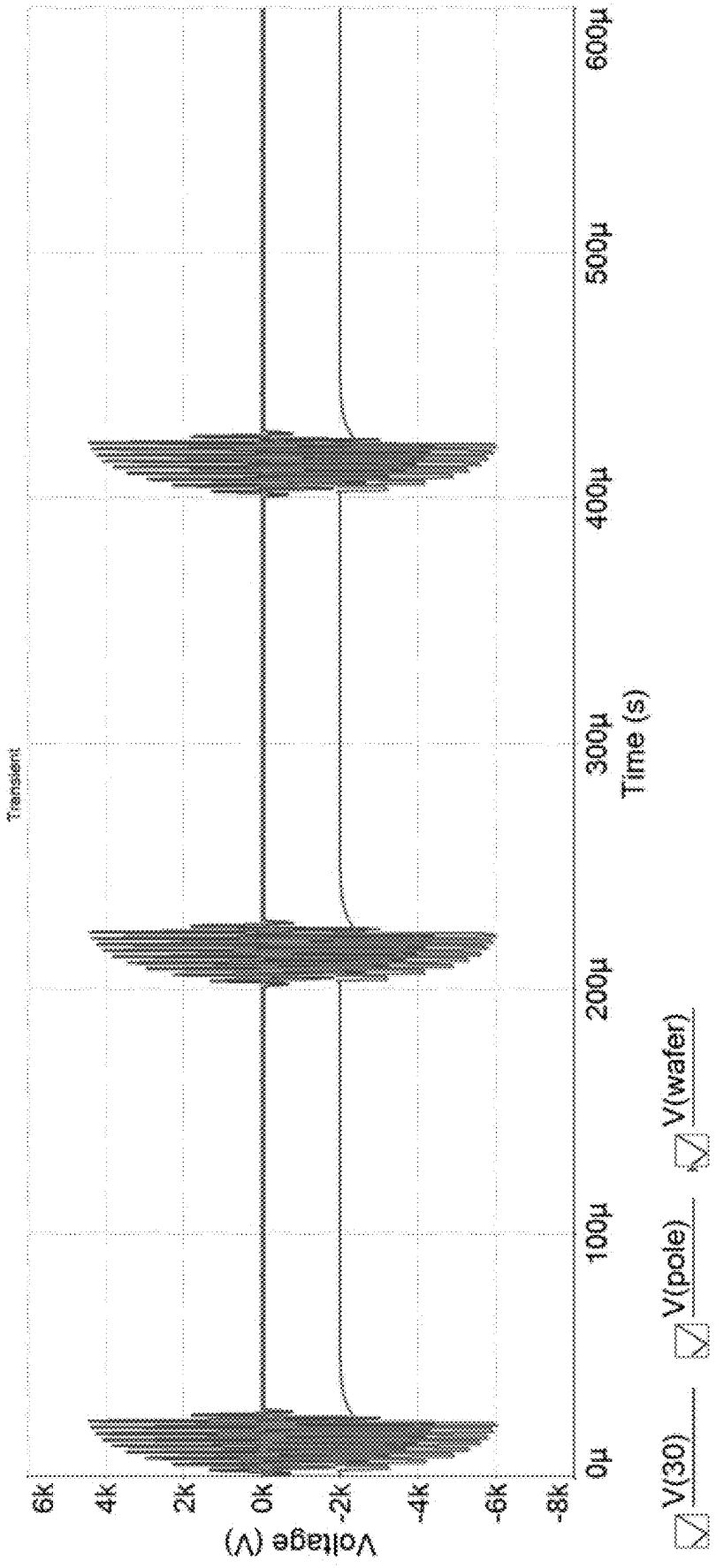

Transient
Voltage (V)
6k
4k
2k
0k
-2k
-4k
-6k
-8k
0µ
100µ
200µ
300µ
400µ
500µ
600µ
Time (s)
V(30)
V(pole)
V(wafer)

FIG. 18

VARIABLE OUTPUT IMPEDANCE RF GENERATOR

BACKGROUND

[0001] The application of RF-excited gaseous discharges in thin film fabrication technology has become standard. The simplest geometry most commonly used is that of two planar electrodes between which a voltage is applied. A schematic representation of such a planar RF plasma reactor is shown in FIG. **1**. The plasma is separated from each electrode by a plasma sheath.

[0002] Positive ions produced in the plasma volume are accelerated across the plasma sheaths and arrive at the electrodes with an Ion Energy Distribution Function (IEDF) which is determined by the magnitude and the waveform of the time dependent potential difference across the sheaths, the gas pressure, the physical geometry of the reactor, and/or other factors. This ion bombardment energy distribution may determine the degree of anisotropy in thin-film etching amount of ion impact induced damage to surfaces, etc.

SUMMARY

[0003] Some embodiments include an RF system that includes an energy storage capacitor, a switching circuit, a resonant circuit, and an energy recovery circuit. In some embodiments, the switching circuit may be coupled with the energy storage capacitor. In some embodiments, the switching circuit producing a plurality of pulses with a pulse amplitude and a pulse frequency where the pulse amplitude may be greater than 100 volts. In some embodiments, the resonant circuit may be coupled with the switching circuit and may include a transformer having a primary side and a secondary side; and at least one of a capacitor, an inductor, and a resistor. In some embodiments, the resonant circuit has a resonant frequency substantially equal to the pulse frequency, and the resonant circuit increases the pulse amplitude to a voltage greater than 2 kV. In some embodiments, the energy recovery circuit may be coupled with the energy storage capacitor and the secondary side of the transformer and the energy recovery circuit comprising a diode and an inductor.

[0004] In some embodiments, the RF system includes a plasma chamber coupled with the resonant circuit. In some embodiments, the switching circuit comprises either a full-bridge driver or a half-bridge driver.

[0005] In some embodiments, the resonant circuit comprises an inductor, and the resonant frequency comprises

$$f_{resonant} \approx \frac{1}{2\pi\sqrt{(L)(C)}},$$

where the inductance L includes any stray inductance of the transformer and the inductance of the inductor, and the capacitance C includes any stray capacitance of the transformer.

[0006] In some embodiments, the resonant circuit comprises a capacitor, and the resonant frequency comprises

$$f_{resonant} \approx \frac{1}{2\pi\sqrt{(L)(C)}},$$

where the inductance L includes any stray inductance of the transformer, and the capacitance C includes any stray capacitance of the transformer and the capacitance of the capacitor.

[0007] Some embodiments include an RF system that includes an energy storage capacitor, a switching circuit, a resonant circuit, and a plasma chamber. In some embodiments, the switching circuit may be coupled with the energy storage capacitor. In some embodiments, the switching circuit producing a plurality of pulses with a pulse amplitude and a pulse frequency where the pulse amplitude may be greater than 100 volts. In some embodiments, the resonant circuit may be coupled with the switching circuit and may include a transformer having a primary side and a secondary side; and at least one of a capacitor, an inductor, and a resistor. In some embodiments, the resonant circuit has a resonant frequency substantially equal to the pulse frequency, and the resonant circuit increases the pulse amplitude to a voltage greater than 2 kV. In some embodiments, the plasma chamber coupled with the resonant circuit.

[0008] In some embodiments, the RF plasma system may include a transformer coupled with the resonant circuit. In some embodiments, the RF plasma system may include a resistive output stage. In some embodiments, the RF plasma system may include an energy recovery stage. In some embodiments, the RF plasma system may include a bias compensation circuit.

[0009] In some embodiments, either or both the inductance (L) and/or the capacitance (C) of the transformer determine the resonant frequency according to:

$$f_{resonant} \approx \frac{1}{2\pi\sqrt{(L)(C)}}.$$

[0010] In some embodiments, the resonant frequency comprises

$$f_{resonant} \approx \frac{1}{2\pi\sqrt{(L)(C)}},$$

where the inductance L includes any stray inductance of the transformer and the capacitance C includes any stray capacitance of the transformer.

[0011] In some embodiments, the high voltage switching power supply comprises either a full-bridge driver or a half-bridge driver.

[0012] In some embodiments, the switching power supply is driven with a frequency selected from the group consisting of 400 kHz, 0.5 MHz, 2.0 MHz, 4.0 MHz, 13.56 MHz, 27.12 MHz, 40.68 MHz, and 50 MHz.

[0013] Some embodiments include an RF system that includes a high voltage switching power supply, an inductively coupled plasma source, and a capacitor. In some embodiments, the high voltage switching power supply producing a plurality of pulses with a pulse amplitude and a pulse frequency, the pulse amplitude being greater than 100 volts. In some embodiments, the inductively coupled plasma source comprising a coil that is electrically coupled with the high voltage switching power supply. In some embodiments, the capacitor and the inductance of the inductively coupled

plasma source resonate with a resonant frequency substantially equal to the pulse frequency.

[0014] In some embodiments, the resonant frequency comprises

$$f_{resonant} \approx \frac{1}{2\pi\sqrt{(L)(C)}},$$

where the inductance L includes the inductance of the inductively coupled plasma source and the capacitance C includes the capacitance of the capacitor. In some embodiments, the high voltage switching power supply comprises either a full-bridge driver or a half-bridge driver.

[0015] Some embodiments include an RF system that includes a high voltage switching power supply, a capacitively coupled plasma, and an inductor. In some embodiments, the high voltage switching power supply producing a plurality of pulses with a pulse amplitude and a pulse frequency, the pulse amplitude being greater than 100 volts. In some embodiments, the inductor and the capacitance of the capacitively coupled plasma form a resonant circuit with a resonant frequency substantially equal to the pulse frequency.

[0016] In some embodiments, the resonant frequency comprises

$$f_{resonant} \approx \frac{1}{2\pi\sqrt{(L)(C)}},$$

where the inductance L includes the inductance of the inductor and the capacitance C includes the capacitance of the capacitively coupled plasma. In some embodiments, the high voltage switching power supply comprises either a full-bridge driver or a half-bridge driver.

[0017] These illustrative embodiments are mentioned not to limit or define the disclosure, but to provide examples to aid understanding thereof. Additional embodiments are discussed in the Detailed Description, and further description is provided there. Advantages offered by one or more of the various embodiments may be further understood by examining this specification or by practicing one or more embodiments presented.

BRIEF DESCRIPTION OF THE FIGURES

[0018] These and other features, aspects, and advantages of the present disclosure are better understood when the following Detailed Description is read with reference to the accompanying drawings.

[0019] FIG. **1** is a schematic representation of a planar RF plasma reactor according to some embodiments.

[0020] FIG. **2** is schematic of the equivalent electric circuit model of an RF plasma reactor according to some embodiments.

[0021] FIG. **3**. illustrates calculated waveforms of the voltage V_r across the plasma reactor and the plasma potential V_P for equal areas of the target and substrate electrodes.

[0022] FIG. **4** Illustrates calculated waveforms of the potential V_{ST} across the plasma sheath adjacent to the target electrode and that of the potential V_{ss} across the sub-strate electrode.

[0023] FIG. **5** is a block diagram of an RF Driver according to some embodiments.

[0024] FIG. **6** is a circuit diagram of an RF Driver according to some embodiments.

[0025] FIG. **7** is a waveform of the voltage across the transformer T**1** (red), at the Pole (green), and at the wafer (blue) for a time frame of 600 μs.

[0026] FIG. **8** is a zoomed view of the waveform over a time frame of 10 μs.

[0027] FIG. **9** is a circuit diagram of an RF Driver according to some embodiments.

[0028] FIG. **10** is a circuit diagram of an RF Driver according to some embodiments.

[0029] FIG. **11** is a circuit diagram of an RF Driver according to some embodiments.

[0030] FIG. **12** is a circuit diagram of an RF Driver according to some embodiments.

[0031] FIG. **13** is a circuit diagram of an RF Driver according to some embodiments.

[0032] FIGS. **14**A, **14**B, **15**A, and **15**B are circuit diagrams of example resonant circuits.

[0033] FIG. **16** is a continuous waveform of the voltage across the transformer T**1** (red), at the Pole (green), and at the wafer (blue).

[0034] FIG. **17** is a short burst waveform of the voltage across the transformer T**1** (red), at the Pole (green), and at the wafer (blue).

[0035] FIG. **18** is a waveform showing a series of short bursts across the transformer T**1** (red), at the Pole (green), and at the wafer (blue).

DESCRIPTION OF THE DISCLOSURE

[0036] In some embodiments, systems and methods are disclosed to provide switching power to a plasma chamber without the use of a matching network. As shown in FIG. **1**, a typical RF driver **105** requires a matching network **110**, for example, to ensure the impedance of the RF driver **105** matches the impedance of the plasma chamber **115**. To accomplish this, a matching network **110** can include any combinations of transformers, resistors, inductors, capacitors, and/or transmission lines. Often the matching network **110** may need to be tuned to ensure that the impedance of the RF driver **105** and the impedance of the plasma chamber **115** match. This tuning may be required during plasma processing. Matching networks, however, can be relatively slow at tuning (e.g., requiring at best lest than around tens or hundreds of milliseconds to tune), which may not allow real time tuning.

[0037] Embodiments described in this disclosure include circuits and processes for driving switching power to a plasma chamber without a matching network. In some embodiments, a full (or half) bridge circuit may be used to drive a resonant circuit at its resonant frequency. Because the resonant circuit is being driven at its resonant frequency, the output voltage of the resonant circuit may be higher than the input voltage. In some embodiments, this resonant condition may allow for a drive voltage of a few hundred volts to generate about 4 kV or more of output voltage at a transformer.

[0038] As used throughout this disclosure, the term "high voltage" may include a voltage greater than 500 V, 1 kV, 10 kV, 20 kV, 50 kV, 100 kV, etc.; the term "high frequency" may be a frequency greater than 100 Hz, 250 Hz, 500 Hz, 750 Hz, 1 kHz, 10 KHz, 100 kHz, 200 kHz, 500 KHz, 1

MHz, 10 MHz, 50 MHz, 100 MHz, etc., the term "fast rise time" may include a rise time less than about 1 ns, 10 ns, 50 ns, 100 ns, 250 ns, 500 ns, 1,000 ns, etc.; the term "fast fall time" may include a fall time less than about 1 ns, 10 ns, 50 ns, 100 ns, 250 ns, 500 ns, 1,000 ns, etc.); and the term short pulse width may include pulse widths less than about 1 ns, 10 ns, 50 ns, 100 ns, 250 ns, 500 ns, 1,000 ns, etc.).

[0039] FIG. **2** is schematic of an equivalent electric circuit model **200** for an RF driver **105**, which may be an RF power supply, and an equivalent circuit of a plasma chamber **115**. In this example, V_{RF} is the voltage of the applied RF signal from a RF driver **105** with a matching network **110**. V_T and V_P are the potentials of the target electrode and the plasma, respectively. In addition, $V_{SS}=V_P$ and $V_{ST}=V_T-V_P$ are the voltages across the substrate or chamber wall plasma sheath (V_{SS}) and the target plasma sheath (V_{ST}), respectively. The blocking capacitor is represented by C**2**; C**3** and I_T represent the capacitance and the conduction current through the sheath adjacent to the target electrode, respectively, while C**9** and I_S represent the corresponding values of the capacitance and current for the sheath adjacent to the substrate electrode.

[0040] In some embodiments, the electrical resistance of the plasma may be small with respect to the sheath resistance for the plasma electron densities and voltage frequencies described in this disclosure. However, inclusion of the plasma resistance does not introduce any complications for the circuit model.

[0041] FIG. **3**. Illustrates waveforms of the voltage V_T across a plasma reactor such as, for example, those shown in FIG. **1** and FIG. **2**, and the plasma potential V_P for equal areas of the target and substrate electrodes. FIG. **4** Illustrates calculated waveforms of the potential V_{ST} across the plasma sheath adjacent to the target electrode shown in FIG. **1** and that of the potential V_{ss} across the sub-strate electrode sheath for $A_T/A_S=0.2$, where A_T and A_S are the areas of the target electrode and the substrate electrode respectively. FIG. **4** shows the half sine wave of the sheath potential going from 0 to −450V.

[0042] FIG. **5** is a block diagram of a driver and chamber circuit **500** without a matching network according to some embodiments. The driver and chamber circuit **500** may include an RF driver **505** that may include a voltage source and either a full-bridge driver or a half bridge driver or an equivalent driver. The driver and chamber circuit **500** may include a resonant circuit **510** having a transformer and resonant elements. The driver and chamber circuit **500** may include may also include a half-wave rectifier **515** electrically coupled with the resonant circuit **510**. A resistive output stage **520** (or an energy recovery circuit) may be coupled with the half-wave rectifier. A bias compensation circuit **525** may be coupled with the resistive output stage **520**. The plasma and chamber **530** and a plasma may be coupled with the bias compensation circuit **525**.

[0043] FIG. **6** is a circuit diagram of a driver and chamber circuit **600** according to some embodiments.

[0044] In this example, the driver and chamber circuit **600** may include an RF driver **605**. The RF driver **605**, for example, may be a half-bridge driver or a full-bridge driver as shown in FIG. **6**. The RF driver **605** may include an input voltage source V**1** that may be a DC voltage source (e.g., a capacitive source, AC-DC converter, etc.). In some embodiments, the RF driver **605** may include four switches S**1**, S**2**, S**3**, and S**4**. In some embodiments, the RF driver **605** may include a plurality of switches S**1**, S**2**, S**3**, and S**4** in series or in parallel. These switches S**1**, S**2**, S**3**, and S**4**, for example, may include any type of solid-state switch such as, for example, IGBTs, a MOSFETs, a SiC MOSFETs, SiC junction transistors, FETs, SiC switches, GaN switches, photoconductive switches, etc. These switches S**1**, S**2**, S**3**, and S**4** may be switched at high frequencies and/or may produce a high voltage pulses. These frequencies may, for example, include frequencies of about 400 kHz, 0.5 MHz, 2.0 MHz, 4.0 MHz, 13.56 MHz, 27.12 MHz, 40.68 MHz, 50 MHz, etc.

[0045] Each switch of switches S**1**, S**2**, S**3**, and S**4** may be coupled in parallel with a respective diode D**1**, D**2**, D**3**, and D**4** and may include stray inductance represented by inductor L**1**, L**2**, L**3**, and L**4**. In some embodiments, the inductances of inductor L**1**, L**2**, L**3**, and L**4** may be equal. In some embodiments, the inductances of inductor L**1**, L**2**, L**3**, and L**4** may be less than about 50 nH, 100 nH, 150 nH, 500 nH, 1,000 nH, etc. The combination of a switch (S**1**, S**2**, S**3**, or S**4**) and a respective diode (D**1**, D**2**, D**3**, or D**4**) may be coupled in series with a respective inductor (L**1**, L**2**, L**3**, or L**4**). Inductors L**3** and L**4** are connected with ground. Inductor L**1** is connected with switch S**4** and the resonant circuit **610**. And inductor L**2** is connected with switch S**3** and the opposite side of the resonant circuit **610**.

[0046] In some embodiments, the RF driver **605** may be coupled with a resonant circuit **610**. The resonant circuit **610** may include a resonant inductor L**5** and/or a resonant capacitor C**2** coupled with a transformer T**1**. The resonant circuit **610** may include a resonant resistance R**5**, for example, that may include the stray resistance of any leads between the RF driver **605** and the resonant circuit **610** and/or any component within the resonant circuit **610** such as, for example, the transformer T**1**, the capacitor C**2**, and/or the inductor L**5**. In some embodiments, the resonant resistance R**5** comprises only stray resistances of wires, traces, or circuit elements. While the inductance and/or capacitance of other circuit elements may affect the driving frequency, the driving frequency can be set largely by choice of the resonant inductor L**5** and/or the resonant capacitor C**2**. Further refinements and/or tuning may be required to create the proper driving frequency in light of stray inductance or stray capacitance. In addition, the rise time across the transformer T**1** can be adjusted by changing L**5** and/or C**2**, provided that:

$$f_{resonant} = \frac{1}{2\pi\sqrt{(L5)(C2)}} = \text{constant.}$$

In some embodiments, large inductance values for L**5** can result in slower or shorter rise times. These values may also affect the burst envelope. As shown in FIG. **17**, each burst can include transient and steady state pulses. The transient pulses within each burst may be set by L**5** and/or the Q of the system until full voltage is reached during the steady state pulses.

If the switches in the RF driver **605** are switched at the resonant frequency, $f_{resonant}$, then the output voltage at the transformer T**1** will be amplified. In some embodiments, the resonant frequency may be about 400 kHz, 0.5 MHz, 2.0 MHz, 4.0 MHz, 13.56 MHz, 27.12 MHz, 40.68 MHz, 50 MHz, etc.

[0047] In some embodiments, the resonant capacitor C**2** may include the stray capacitance of the transformer T**1** and/or a physical capacitor. In some embodiments, the resonant capacitor C**2** may have a capacitance of about 10 μF, 1 μF, 100 nF, 10 nF, etc. In some embodiments, the resonant inductor L**5** may include the stray inductance of the transformer T**1** and/or a physical inductor. In some embodiments, the resonant inductor L**5** may have an inductance of about 50 nH, 100 nH, 150 nH, 500 nH, 1,000 nH, etc. In some embodiments, the resonant resistor R**5** may have a resistance of about 10 ohms, 25 ohms, 50 ohms, 100 ohms, 150 ohms, 500 ohms, etc.

[0048] In some embodiments, the resonant resistor R**5** may represent the stray resistance of wires, traces, and/or the transformer windings within the physical circuit. In some embodiments, the resonant resistor R**5** may have a resistance of about 10 mohms, 50 mohms, 100 mohms, 200 mohms, 500 mohms, etc.

[0049] In some embodiments, the transformer T**1** may comprise a transformer as disclosed in U.S. patent application Ser. No. 15/365,094, titled "High Voltage Transformer," which is incorporated into this document for all purposes. In some embodiments, the output voltage of the resonant circuit **610** can be changed by changing the duty cycle (e.g., the switch "on" time or the time a switch is conducting) of switches S**1**, S**2**, S**3**, and/or S**4**. For example, the longer the duty cycle, the higher the output voltage; and the shorter the duty cycle, the lower the output voltage. In some embodiments, the output voltage of the resonant circuit **610** can be changed or tuned by adjusting the duty cycle of the switching in the RF driver **605**.

[0050] For example, the duty cycle of the switches can be adjusted by changing the duty cycle of signal Sig**1**, which opens and closes switch S**1**; changing the duty cycle of signal Sig**2**, which opens and closes switch S**2**; changing the duty cycle of signal Sig**3**, which opens and closes switch S**3**; and changing the duty cycle of signal Sig**4**, which opens and closes switch S**4**. By adjusting the duty cycle of the switches S**1**, S**2**, S**3**, or S**4**, for example, the output voltage of the resonant circuit **610** can be controlled.

[0051] In some embodiments, each switch S**1**, S**2**, S**3**, or S**4** in the resonant circuit **605** can be switched independently or in conjunction with one or more of the other switches. For example, the signal Sig**1** may be the same signal as signal Sig**3**. As another example, the signal Sig**2** may be the same signal as signal Sig**4**. As another example, each signal may be independent and may control each switch S**1**, S**2**, S**3**, or S**4** independently or separately.

[0052] In some embodiments, the resonant circuit **610** may be coupled with a half-wave rectifier **615** that may include a blocking diode D**7**.

[0053] In some embodiments, the half-wave rectifier **615** may be coupled with the resistive output stage **620**. The resistive output stage **620** may include any resistive output stage known in the art. For example, the resistive output stage **620** may include any resistive output stage described in U.S. patent application Ser. No. 16/178,538 titled "HIGH VOLTAGE RESISTIVE OUTPUT STAGE CIRCUIT," which is incorporated into this disclosure in its entirety for all purposes.

[0054] For example, the resistive output stage **620** may include an inductor L**11**, resistor R**3**, resistor R**1**, and capacitor C**11**. In some embodiments, inductor L**11** may include an inductance of about 5 μH to about 25 μH. In some embodiments, the resistor R**1** may include a resistance of about 50 ohms to about 250 ohms. In some embodiments, the resistor R**3** may comprise the stray resistance in the resistive output stage **620**.

[0055] In some embodiments, the resistor R**1** may include a plurality of resistors arranged in series and/or parallel. The capacitor C**11** may represent the stray capacitance of the resistor R**1** including the capacitance of the arrangement series and/or parallel resistors. The capacitance of stray capacitance C**11**, for example, may be less than 500 pF, 250 pF, 100 pF, 50 pF, 10 pF, 1 pF, etc. The capacitance of stray capacitance C**11**, for example, may be less than the load capacitance such as, for example, less than the capacitance of C**2**, C**3**, and/or C**9**.

[0056] In some embodiments, the resistor R**1** may discharge the load (e.g., a plasma sheath capacitance). In some embodiments, the resistive output stage **620** may be configured to discharge over about 1 kilowatt of average power during each pulse cycle and/or a joule or less of energy in each pulse cycle. In some embodiments, the resistance of the resistor R**1** in the resistive output stage **620** may be less than 200 ohms. In some embodiments, the resistor R**1** may comprise a plurality of resistors arranged in series or parallel having a combined capacitance less than about 200 pF (e.g., C**11**).

[0057] In some embodiments, the resistive output stage **620** may include a collection of circuit elements that can be used to control the shape of a voltage waveform on a load. In some embodiments, the resistive output stage **620** may include passive elements only (e.g., resistors, capacitors, inductors, etc.). In some embodiments, the resistive output stage **620** may include active circuit elements (e.g., switches) as well as passive circuit elements. In some embodiments, the resistive output stage **620**, for example, can be used to control the voltage rise time of a waveform and/or the voltage fall time of waveform.

[0058] In some embodiments, the resistive output stage **620** can discharge capacitive loads (e.g., a wafer and/or a plasma). For example, these capacitive loads may have small capacitance (e.g., about 10 pF, 100 pF, 500 pF, 1 nF, 10 nF, 100 nF, etc.).

[0059] In some embodiments, a resistive output stage can be used in circuits with pulses having a high pulse voltage (e.g., voltages greater than 1 kV, 10 kV, 20 kV, 50 kV, 100 kV, etc.) and/or high frequencies (e.g., frequencies greater than 1 kHz, 10 kHz, 100 kHz, 200 kHz, 500 kHz, 1 MHz, etc.) and/or frequencies of about 400 KHz, 0.5 MHz, 2.0 MHz, 4.0 MHz, 13.56 MHz, 27.12 MHz, 40.68 MHz, 50 MHz, etc.

[0060] In some embodiments, the resistive output stage may be selected to handle high average power, high peak power, fast rise times and/or fast fall times. For example, the average power rating might be greater than about 0.5 kW, 1.0 KW, 10 KW, 25 KW, etc., and/or the peak power rating might be greater than about 1 kW, 10 KW, 100 KW, 1 MW, etc.

[0061] In some embodiments, the resistive output stage **620** may include a series or parallel network of passive components. For example, the resistive output stage **620** may include a series of a resistor, a capacitor, and an inductor. As another example, the resistive output stage **620** may include a capacitor in parallel with an inductor and the capacitor-inductor combination in series with a resistor. For example, L**11** can be chosen large enough so that there is no

significant energy injected into the resistive output stage when there is voltage out of the rectifier. The values of R3 and R1 can be chosen so that the L/R time can drain the appropriate capacitors in the load faster than the RF frequency

[0062] In some embodiments, the resistive output stage **620** may be coupled with the bias compensation circuit **625**. The bias compensation circuit **625** may include any bias and/or bias compensation circuit known in the art. For example, the bias compensation circuit **625** may include any bias and/or bias compensation circuit described in U.S. patent application Ser. No. 16/523,840 titled "NANOSECOND PULSER BIAS COMPENSATION," which is incorporated into this disclosure in its entirety for all purposes.

[0063] In some embodiments, the bias compensation circuit **625** may include a bias capacitor C7, blocking capacitor C12, a blocking diode D8, switch S8 (e.g., a high voltage switch), offset supply voltage V1, resistance R2, and/or resistance R4. In some embodiments, the switch S8 comprises a high voltage switch described in U.S. Patent Application No. 62/717,637, titled "HIGH VOLTAGE SWITCH FOR NANOSECOND PULSING," and/or in U.S. patent application Ser. No. 16/178,565, titled "HIGH VOLTAGE SWITCH FOR NANOSECOND PULSING," which is incorporated into this disclosure in its entirety for all purposes.

[0064] In some embodiments, the offset supply voltage V5 may include a DC voltage source that can bias the output voltage either positively or negatively. In some embodiments, the capacitor C12 may isolate/separate the offset supply voltage V5 from the resistive output stage **620** and/or other circuit elements. In some embodiments, the bias compensation circuit **625** may allow for a potential shift of power from one portion of the circuit to another. In some embodiments, the bias compensation circuit **625** may be used to hold a wafer in place as high voltage pulses are active within the chamber. Resistance R2 may protect/isolate the DC bias supply from the driver.

[0065] In some embodiments, the switch S8 may be open while the RF driver **605** is pulsing and closed when the RF driver **605** is not pulsing. While closed, the switch S8 may, for example, short current across the blocking diode D8. Shorting this current may allow the bias between the wafer and the chuck to be less than 2 kV, which may be within acceptable tolerances.

[0066] In some embodiments, the plasma and chamber **630** may be coupled with the bias compensation circuit **625**. The plasma and chamber **630**, for example, may be represented by the various circuit elements shown in FIG. **6**.

[0067] FIG. **6** does not include a traditional matching network such as, for example, a 50 ohm matching network or an external matching network or standalone matching network. Indeed, the embodiments described within this document do not require a 50 ohm matching network to tune the switching power applied to the wafer chamber. In addition, embodiments described within this document provide a variable output impedance RF generator without a traditional matching network. This can allow for rapid changes to the power drawn by the plasma chamber. Typically, this tuning of the matching network can take at least 100 μs-200 μs. In some embodiments, power changes can occur within one or two RF cycles, for example, 2.5 μs-5.0 μs at 400 KHz.

[0068] FIG. **7** is a waveform of the voltage across the transformer T1 (red), at the Pole (green), and at the wafer (blue) for a time frame of 600 μs. FIG. **8** is a zoomed view of the waveform over a time frame of 10 μs.

[0069] FIG. **9** is a circuit diagram of an RF Driver **900** according to some embodiments. The RF Driver **900**, for example, may include the RF driver **605**, the resonant circuit **610**, the bias compensation circuit **625**, and the plasma and chamber **630**. The RF Driver **900** is similar to the driver and chamber circuit **600** but without the resistive output stage **620** and includes an energy recovery circuit **905**.

[0070] In this example, the energy recovery circuit **905** may be positioned on or electrically coupled with the secondary side of the transformer T1. The energy recovery circuit **905**, for example, may include a diode D9 (e.g., a crowbar diode) across the secondary side of the transformer T1. The energy recovery circuit **905**, for example, may include diode D10 and inductor L12 (arranged in series), which can allow current to flow from the secondary side of the transformer T1 to charge the power supply C15 and current to flow to the plasma and chamber **630**. The diode D12 and the inductor L12 may be electrically connected with the secondary side of the transformer T1 and coupled with the power supply C15. In some embodiments, the energy recovery circuit **905** may include diode D13 and/or inductor L13 electrically coupled with the secondary of the transformer T1. The inductor L12 may represent the stray inductance and/or may include the stray inductance of the transformer T1.

[0071] When the nanosecond pulser is turned on, current may charge the plasma and chamber **630** (e.g., charge the capacitor C3, capacitor C2, or capacitor C9). Some current, for example, may flow through inductor L12 when the voltage on the secondary side of the transformer T1 rises above the charge voltage on the power supply C15. When the nanosecond pulser is turned off, current may flow from the capacitors within the plasma and chamber **630** through the inductor L12 to charge the power supply C15 until the voltage across the inductor L12 is zero. The diode D9 may prevent the capacitors within the plasma and chamber **630** from ringing with the inductance in the plasma and chamber **630** or the bias compensation circuit **625**.

[0072] The diode D12 may, for example, prevent charge from flowing from the power supply C15 to the capacitors within the plasma and chamber **630**.

[0073] The value of inductor L12 can be selected to control the current fall time. In some embodiments, the inductor L12 can have an inductance value between 1 μH-500 μH.

[0074] In some embodiments, the energy recovery circuit **905** may include a switch that can be used to control the flow of current through the inductor L12. The switch, for example, may be placed in series with the inductor L12. In some embodiments, the switch may be closed when the switch S1 is open and/or no longer pulsing to allow current to flow from the plasma and chamber **630** back to the power supply C15.

[0075] A switch in the energy recovery circuit **905**, for example, may include a high voltage switch such as, for example, the high voltage switch disclosed in U.S. patent application Ser. No. 16/178,565 filed Nov. 1, 2018, titled "HIGH VOLTAGE SWITCH WITH ISOLATED POWER," which claims priority to U.S. Provisional Patent Application No. 62/717,637 filed Aug. 10, 2018, both of which are

incorporated by reference in the entirety. In some embodiments, the RF driver **605** may include a high voltage switch in place of or in addition to the various components shown in RF driver **605**. In some embodiments, using a high voltage switch may allow for removal of at least the transformer T**1** and the switch S**1**.

[0076] FIG. **10** is a circuit diagram of a driver and chamber circuit **1000** according to some embodiments. The driver and chamber circuit **1000**, for example, may include the RF driver **605**, the resonant circuit **610**, the resistive output stage **620**, and the plasma and chamber **630**. Thus, driver and chamber circuit **1000** is similar to the driver and chamber circuit **600** without the bias compensation circuit **625**.

[0077] FIG. **11** is a circuit diagram of a driver and chamber circuit **1100** according to some embodiments. The driver and chamber circuit **1100**, for example, may include the RF driver **605**, the resonant circuit **610**, the energy recovery circuit **905**, and the plasma and chamber **630**. Thus, driver and chamber circuit **1100** is similar to the driver and chamber circuit **900** without the bias compensation circuit **625**.

[0078] FIG. **12** is a circuit diagram of a driver and a inductive discharge plasma **1200** according to some embodiments. The driver and a inductive discharge plasma **1200**, for example, may include the RF driver **605**, the resonant circuit **610**, and an inductively discharged plasma **1205**. In this example, the inductor L**5** may include the antenna that is coupled with the inductively discharged plasma **1205**. The transformer T**1** may represent how the inductively discharged plasma **1205** couples with the antenna, which is represented at least in part by the inductor L**5**. The capacitor C**2** may resonate with the inductor L**5** to determine the resonate frequency. The RF driver **605** may produce pulses that are driven with this resonant frequency.

[0079] FIG. **13** is a circuit diagram of a driver and a capacitive discharge plasma **1300** according to some embodiments. The driver and a capacitive discharge plasma **1300**, for example, may include the RF driver **605**, the resonant circuit **1310**, which may include the transformer, and the chamber **630**. The capacitor C**1** may represent the capacitance of the discharge geometry, any stray capacitance in the circuit, or the capacitance of any capacitors in the circuit. L**5** may represent the inductance of any stray inductance in the circuit or the inductance of any inductance in the circuit. The RF driver **605** may drive the resonant circuit **1310** with a pulse frequency that is substantially equal to the resonate frequency of the resonant circuit.

[0080] In some embodiments, each switch S**1**, S**2**, S**3**, or S**4** in the resonant circuit **605** can be switched independently or in conjunction with one or more of the other switches. For example, the signal Sig**1** may be the same signal as signal Sig**3**. As another example, the signal Sig**2** may be the same signal as signal Sig**4**. As another example, each signal may be independent and may control each switch S**1**, S**2**, S**3**, or S**4** independently or separately.

[0081] In some embodiments, the transformer T**1** may or may not be included in the driver and a capacitive discharge plasma **1300**.

[0082] FIGS. **14**A, **14**B, **15**A, and **15**B are circuit diagrams of example resonant circuits that may be used in place of resonant circuit **610** in FIG. **6**. These circuits may or may not include the transformer shown in each figure.

[0083] FIG. **16** is a continuous waveform of the voltage across the transformer T**1** (red), at the Pole (green), and at the wafer (blue).

[0084] FIG. **17** is a short burst waveform of the voltage across the transformer T**1** (red), at the Pole (green), and at the wafer (blue). This waveform shows a 22.5 μs long burst.

[0085] FIG. **18** is a waveform showing a series of short bursts across the transformer T**1** (red), at the Pole (green), and at the wafer (blue). This waveform shows repeated 22.5 μs long bursts. Embodiments described within this document provide a system whose timing can be adjusted. For example, the number of pulses in a burst, the frequency, the number of bursts, and/or the duty cycle of bursts can all be adjusted by changing the drive signal(s) (Sig**1**, Sig**2**, Sig**3**, or Sig**4**) to the switches S**1**, S**2**, S**3**, or S**4**.

[0086] In some embodiments, the diode D**8** and the capacitor C**7** in the bias compensation circuit **625** shown in any circuit can be arranged in a stripline such that the current flows in a U-shaped path. A stripline, for example, may be a transmission line trace surrounded by dielectric material suspended between two ground planes on internal layers of a PCB. In some embodiments, the separation between the diode D**8** and the capacitor C**7** can be maximized. In some embodiments, the diode D**8** and the capacitor C**7** stripline as wide as possible such as, for example, 10, 8, 6, 4, 3, 2, 1, ½ inches.

[0087] In some embodiments, the lead inductance L**22** can be minimized or eliminated by connecting the point **124** to the input of the diode D**8** (e.g., at the stray inductance L**22**). In some embodiments, the lead inductance L**24** can be minimized or eliminated by connecting the low side of the capacitor C**7** (e.g., at the stray inductance L**24**) directly to ground.

[0088] In this example, the bias compensation circuit **625** includes stray inductance L**22** between diode D**8** and the position labeled **124**, stray inductance L**23** between diode D**8** and capacitor C**7**, or stray inductance L**24** between capacitor C**7** and ground. The circuit **500** includes plasma side inductance L_p and switch side inductance L_s. The plasma side stray inductance L_p, for example, may include all the inductance whether stray, parasitic, or from any element between the bias compensation circuit **625** and the chamber **630** such as, for example, L**9** and any other stray inductance on this side of the circuit. The switch side inductance L_s, for example, may include all the inductance whether stray, parasitic, or from any element between the bias compensation circuit **625** and the switch S**1** such as, for example, L**11**, L**5**, L**1**, L**2**, L**3**, and/or L**4**, and any other stray inductance on this side of the circuit.

[0089] In some embodiments, the switch side inductance L_s should be greater than the plasma side stray inductance L_p. In some embodiments, the plasma side stray inductance L_p is 20% of the switch side inductance L_s. In some embodiments, the plasma side stray inductance L_p is less than about 1 nH, 10 nH, 100 nH, 1 uH, etc.

[0090] In some embodiments, the stray inductance L**22** has an inductance less than about 1 nH, 10 nH, 100 nH, 1 uH, etc. In some embodiments, the stray inductance L**23** has an inductance less than about 1 nH, 10 nH, 100 nH, 1 uH, etc. In some embodiments, the stray inductance L**24** has an inductance less than about 1 nH, 10 nH, 100 nH, 1 uH, etc. In some embodiments the sum of the stray inductance of L**22**, L**23**, and L**24** is less than about 1 nH, 10 nH, 100 nH, 1 uH, etc.

[0091] In some embodiments, the stray inductance L**22**, L**23**, or L**24** can be minimized In a variety of ways. For example, the conductor along stray inductance L**22**, L**23**, or L**24** can be broader than industry standard such as, for example, greater than ⅛, ¼, ⅜, ½, 1, 2.5, 5 inches etc. As another example, various circuit elements, such as, for example, diode D**8** or capacitor C**7** may include a plurality of diodes or capacitors in parallel or series.

[0092] In some embodiments, the distance between elements may be minimized to reduce stray inductance. For example, the top conductor and the bottom conductor between which the various bias compensation circuit elements may be separated by less than about 1, 2, 5, 15, 20, 25, 30, 35, 40 cm. As another example, the discrete elements comprising diode D**8** may be disposed within less than 10, 8, 6, 4, 3, 2, 1, ½ inches from the position labeled **124** or ground. As another example, the discrete elements comprising capacitor C**7** may be disposed within less than 10, 8, 6, 4, 3, 2, 1, ½ inches from the position labeled **124** or ground.

[0093] In some embodiments, the volume of the discrete elements comprising either or both the diode D**8** and/or capacitor C**7** may be less than 1200, 1000, 750, 500 cubic centimeters.

[0094] In some embodiments, a resistor R**4** may be included across diode D**8**. In some embodiments, the resistor R**4** may have resistance values of less than about 1 kΩ to 1 MΩ such as, for example, less than about 100 kΩ.

[0095] In some embodiments, the capacitor C**7** may have a capacitance less than about 1 μF or less than about 1 mF. The capacitor C**7** may have a stray inductance less than about 1 nH, 10 nH, 100 nH, 1 uH, etc.

[0096] The term "or" is inclusive.

[0097] Unless otherwise specified, the term "substantially" means within 5% or 10% of the value referred to or within manufacturing tolerances. Unless otherwise specified, the term "about" means within 5% or 10% of the value referred to or within manufacturing tolerances.

[0098] Numerous specific details are set forth herein to provide a thorough understanding of the claimed subject matter. However, those skilled in the art will understand that the claimed subject matter may be practiced without these specific details. In other instances, methods, apparatuses or systems that would be known by one of ordinary skill have not been described in detail so as not to obscure claimed subject matter.

[0099] Some portions are presented in terms of algorithms or symbolic representations of operations on data bits or binary digital signals stored within a computing system memory, such as a computer memory. These algorithmic descriptions or representations are examples of techniques used by those of ordinary skill in the data processing arts to convey the substance of their work to others skilled in the art. An algorithm is a self-consistent sequence of operations or similar processing leading to a desired result. In this context, operations or processing involves physical manipulation of physical quantities. Typically, although not necessarily, such quantities may take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared or otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to such signals as bits, data, values, elements, symbols, characters, terms, numbers, numerals or the like. It should be understood, however, that all of these and similar terms are to be associated with appropriate physical quantities and are merely convenient labels. Unless specifically stated otherwise, it is appreciated that throughout this specification discussions utilizing terms such as "processing," "computing," "calculating," "determining," and "identifying" or the like refer to actions or processes of a computing device, such as one or more computers or a similar electronic computing device or devices, that manipulate or transform data represented as physical electronic or magnetic quantities within memories, registers, or other information storage devices, transmission devices, or display devices of the computing platform.

[0100] The system or systems discussed herein are not limited to any particular hardware architecture or configuration. A computing device can include any suitable arrangement of components that provides a result conditioned on one or more inputs. Suitable computing devices include multipurpose microprocessor-based computer systems accessing stored software that programs or configures the computing system from a general-purpose computing apparatus to a specialized computing apparatus implementing one or more embodiments of the present subject matter. Any suitable programming, scripting, or other type of language or combinations of languages may be used to implement the teachings contained herein in software to be used in programming or configuring a computing device.

[0101] Embodiments of the methods disclosed herein may be performed in the operation of such computing devices. The order of the blocks presented in the examples above can be varied for example, blocks can be re-ordered, combined, and/or broken into sub-blocks. Certain blocks or processes can be performed in parallel.

[0102] The use of "adapted to" or "configured to" herein is meant as open and inclusive language that does not foreclose devices adapted to or configured to perform additional tasks or steps. Additionally, the use of "based on" is meant to be open and inclusive, in that a process, step, calculation, or other action "based on" one or more recited conditions or values may, in practice, be based on additional conditions or values beyond those recited. Headings, lists, and numbering included herein are for ease of explanation only and are not meant to be limiting.

[0103] While the present subject matter has been described in detail with respect to specific embodiments thereof, it will be appreciated that those skilled in the art, upon attaining an understanding of the foregoing, may readily produce alterations to, variations of, and equivalents to such embodiments. Accordingly, it should be understood that the present disclosure has been presented for purposes of example rather than limitation, and does not preclude inclusion of such modifications, variations and/or additions to the present subject matter as would be readily apparent to one of ordinary skill in the art.

That which is claimed:

1. A bias supply to apply a periodic voltage comprising:

an output node;

a return node;

a resonant switch section comprising:

a first node, a second node, and a third node;

a first current pathway between the first node and the second node, the first current pathway comprising a series combination of a switch and a diode;

a second current pathway between the second node and the third node comprising a diode and an inductive element; and

a power section comprising:

a first voltage source coupled between the third node and the first node; and

a second voltage source coupled to the return node;

wherein closing the switch causes unidirectional current in the first and second current pathways to cause an application of the periodic voltage between the output node and the return node.

1. The bias supply of claim **1**, wherein the first current pathway is configured so the unidirectional current in the first pathway increases from zero current at a time t**0** when the switch is closed to a peak value and then decreases back to zero at a time t**1** when the switch is opened and a voltage between the output node and return node increases from a negative voltage at the time t**0** to a peak value at the time t**1**.

2. The bias supply of claim **1**, wherein the first current pathway comprises a series combination of the switch, inductive element, and the diode coupled between the first node and the second node.

3. The bias supply of claim **1**, wherein the first current pathway comprises two inductive elements that are coupled together at the second node.

4. The bias supply of claim **1**, wherein the power section comprises a series combination of the second voltage source and an inductive element coupled between the output node and the return node.

6. The bias supply of claim **1**, wherein the second voltage source is coupled between the second node and the return node.

5. The bias supply of claim **1**, wherein a negative terminal of the second voltage source is coupled to a negative terminal of the first voltage source.

6. The bias supply of claim **1**, comprising a third voltage source coupled between the third node and the return node.

8. An apparatus to apply a periodic voltage comprising:

an output node;

a return node;

a switch and a first diode arranged in series within a first current pathway between a first node and a second node;

a second current pathway between the second node and a third node comprising a second diode; and

a first voltage source coupled between the first node and the third node; and a second voltage source coupled to the return node;

wherein closing the switch causes unidirectional current in the first and second current pathways to cause an application of the periodic voltage between the output node and the return node.

9. The method of claim **8**, wherein the connecting and disconnecting causes unidirectional current through the current pathway between the first node and the second node.

7. The method of claim **9**, wherein the connecting and disconnecting causes unidirectional current through a second current pathway between the second node and the third node.

8. The apparatus of claim **8**, wherein the first current pathway comprises two inductive elements that are coupled together at the second node.

9. The apparatus of claim **8**, wherein a series combination of the second voltage source and an inductive element coupled between the output node and the return node.

13. The apparatus of claim **8**, wherein the second voltage source is coupled between the second node and the return node.

10. The apparatus of claim **8**, wherein a negative terminal of the second voltage source is coupled to a negative terminal of the first voltage source.

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