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Inventor(s)

LAI; Wei-An et al.

LAYOUT DESIGNS OF INTEGRATED CIRCUITS HAVING BACKSIDE ROUTING TRACKS

Abstract

An integrated circuit includes a horizontal routing track in a first metal layer, and a backside routing track in a backside metal layer. The backside metal layer and the first metal layer are formed at opposite sides of a semiconductor substrate. The horizontal routing track is conductively connected to a first terminal of a first transistor without passing through a routing track in another metal layer. The backside routing track is conductively connected to a second terminal of the first transistor without passing through a routing track in another metal layer.

Inventors: LAI; Wei-An (Hsinchu, TW), PENG; Shih-Wei (Hsinchu, TW), LIN; Wei-Cheng (Hsinchu, TW), TZENG; Jiann-Tyng (Hsinchu, TW)

Applicant: TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
(Hsinchu, TW)

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Background/Summary

PRIORITY CLAIM [0001] The present application is a continuation of U.S. application Ser. No. 18/429,926, filed Feb. 1, 2024, now U.S. Pat. No. 12,288,785, issued on Apr. 29, 2025, which is a continuation of U.S. application Ser. No. 17/833,531, filed Jun. 6, 2022, and issued as U.S. Pat. No. 11,908,852 on Feb. 20, 2024, which is a continuation of U.S. application Ser. No. 16/933,570, filed Jul. 20, 2020 and issued as U.S. Pat. No. 11,355,487 on Jun. 7, 2022, each of which is incorporated herein by reference in its entirety.

BACKGROUND

[0002] The recent trend in miniaturizing integrated circuits (ICs) has resulted in smaller devices which consume less power yet provide more functionality at higher speeds. The miniaturization process has also resulted in stricter design and manufacturing specifications as well as reliability challenges. Various electronic design automation (EDA) tools generate, optimize and verify standard cell layout designs for integrated circuits while ensuring that the standard cell layout design and manufacturing specifications are met.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0004] FIGS. 1A-1B are partial layout diagrams of a buffer logic gate, in accordance with some embodiments.

[0005] FIG. 1C is a stick diagram of the layout diagrams in FIGS. 1A-1B, in accordance with some embodiments.

[0006] FIG. 1D is an equivalent circuit of the buffer logic gate of FIG. 1C, in accordance with some embodiments.

[0007] FIG. 1E is a circuit diagram of the logic gates formed from the transistors in FIG. 1D, in accordance with some embodiments.

[0008] FIG. 1F is a stick diagram of the buffer logic gate of FIGS. 1A-1B, in accordance with some embodiments.

[0009] FIGS. 2A-2D are cross-sectional views of the buffer logic gate along selected cutting planes of FIGS. 1A-1B, in accordance with some embodiments.

[0010] FIGS. 3A-3B are partial layout diagrams of an And-Or-Invertor (“AOI”) logic circuit having two backside routing tracks, in accordance with some embodiments.

[0011] FIG. 3C is a stick diagram of the AOI logic circuit of FIGS. 3A-3B, in accordance with some embodiments.

[0012] FIG. 3D is an equivalent circuit of the AOI logic circuit of FIG. 3C, in accordance with

some embodiments.

[0013] FIG. 3E is a stick diagram of the AOI logic circuit of FIGS. 3A-3B, in accordance with some embodiments.

[0014] FIGS. 4A-4C are partial layout diagrams of an AOI logic circuit having one backside routing track, in accordance with some embodiments.

[0015] FIG. 4D is a stick diagram of the AOI logic circuit of FIGS. 4A-4C, in accordance with some embodiments.

[0016] FIG. 4E is an equivalent circuit of the AOI logic circuit of FIG. 4D, in accordance with some embodiments.

[0017] FIG. 4F is a stick diagram of the AOI logic circuit of FIGS. 4A-4C, in accordance with some embodiments.

[0018] FIG. 5A is a circuit diagram of the AOI logic circuit, in accordance with some embodiments.

[0019] FIG. 5B is a logic symbol of the AOI logic circuit in FIG. 5A, in accordance with some embodiments.

[0020] FIGS. 6A-6C are partial layout diagrams of a multiplexer circuit, in accordance with some embodiments.

[0021] FIG. 6D is an equivalent circuit of the multiplexer circuit of FIGS. 6A-6C, in accordance with some embodiments.

[0022] FIG. 6E is an equivalent circuit of the multiplexer circuit of FIGS. 6A-6C, in accordance with some embodiments.

[0023] FIG. 6F is a circuit diagram of a four channel multiplexer circuit, in accordance with some embodiments.

[0024] FIG. 6G is a logic gate circuit diagram of a four channel multiplexer circuit, in accordance with some embodiments.

[0025] FIGS. 7A-7B are partial layout diagrams of a logic-gates combo circuit having a backside routing track, in accordance with some embodiments.

[0026] FIG. 7C is an equivalent circuit of the logic-gates combo circuit of FIGS. 7A-7B, in accordance with some embodiments.

[0027] FIG. 7D is a circuit diagram of the logic gates of FIG. 7C, in accordance with some embodiments.

[0028] FIGS. 8A-8B are partial layout diagrams of a Scan D Flip-flop (SDF) circuit, in accordance with some embodiments.

[0029] FIG. 8C is a circuit diagram of the SDF circuit in FIGS. 8A-8B, in accordance with some embodiments.

[0030] FIG. 8D is a partial layout diagram of a Scan D Flip-flop (SDF) circuit which has some of the signal phases identified, in accordance with some embodiments.

[0031] FIG. 9A is a circuit diagram of the SDF circuit in FIGS. 8A-8B, in accordance with some embodiments.

[0032] FIG. 9B is a circuit diagram of the SDF circuit represented in functional blocks, in accordance with some embodiments.

[0033] FIG. 10 is a flow chart of a method of fabricating the backside routing tracks and backside via connectors, in accordance with some embodiments.

[0034] FIGS. 11A-11E are top views and cross-sectional views of intermediate device structures during fabrication of the backside routing tracks and the backside via connector VBd for connecting a backside routing track with a source/drain terminal of a transistor, in accordance with some embodiments.

[0035] FIGS. 12A-12E are top views and cross-sectional views of intermediate device structures during fabrication of the backside routing tracks and the backside via connector VB for connecting a backside routing track with a gate terminal of a transistor, in accordance with some embodiments.

[0036] FIG. **13** is a flowchart of a method of generating a layout design of an integrated circuit in accordance with some embodiments.

[0037] FIG. **14** is a block diagram of an electronic design automation (EDA) system, in accordance with some embodiments.

[0038] FIG. **15** is a block diagram of an integrated circuit (IC) manufacturing system, and an IC manufacturing flow associated therewith, in accordance with some embodiments.

DETAILED DESCRIPTION

[0039] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components, materials, values, steps, operations, arrangements, or the like, are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. Other components, values, operations, materials, arrangements, or the like, are contemplated. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0040] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0041] The shrinking of integrated circuit (IC) devices, and the increasing density of integrated circuit devices on a substrate, produces increasing difficulty of designing and manufacturing interconnect structures between elements of individual devices and between devices of the integrated circuit. Interconnect structure complexity increases as devices shrink in successive generations of integrated circuits, and closer spacing between interconnects increases the likelihood of manufacturing defects causing device failure. As crowding between interconnect structure elements increases, parasitic capacitance increases, adversely impacting the performance of individual transistors of the integrated circuit.

[0042] Manufacturing an integrated circuit having backside routing tracks and backside via connectors reduces the overall complexity of the interconnect structure on the top side of the integrated circuit. Backside routing tracks and backside via connectors allow for more room between topside interconnects (e.g., lines traversing the circuit), reducing parasitic capacitance in the integrated circuit and providing greater manufacturing flexibility. In particular, when two adjacent routing tracks on a same metal layer carry signals with opposite phases, the parasitic capacitance coupling between the two adjacent routing tracks may adversely impact the speed and the power consumption of the integrated circuit. In accordance with at least one embodiment, when backside routing tracks are available for redesigning the layouts of integrated circuits, it is possible using one or more of the presently disclosed embodiments to reduce the number of unfavorable instances where two adjacent routing tracks on a same metal layer carry signals with opposite phases and to improve the speed and the power consumption of the integrated circuits.

[0043] FIGS. **1A-1B** are partial layout diagrams of a buffer logic gate **100**, in accordance with some embodiments. In FIG. **1A**, elements formed on the front side of the substrate are shown in corresponding layout patterns. The elements in FIG. **1A** include active zones, gate-strips, conductive segments, power rails, horizontal routing tracks in a first metal layer **M 0**, and via

connectors for connecting the horizontal routing tracks to the gate-strip and the conductive segment. In FIG. 1B, backside routing tracks and backside via connectors formed on the back side of the substrate are depicted with layout patterns superimposed on the layout patterns in FIG. 1A. FIG. 1C is a stick diagram of the layout diagrams in FIGS. 1A-1B, in accordance with some embodiments.

[0044] In the layout diagram of FIG. 1A, the buffer logic gate **100** includes two parallel power rails **122** and **124** extending in the X-direction. The power rail **122** is configured to have a first supply voltage VDD, and the power rail **124** is configured to have a second supply voltage VSS. The buffer logic gate **100** also includes a p-type active zone **80p** and an n-type active zone **80n** extending in the X-direction. The buffer logic gate **100** further includes multiple gate-strips **151**, **152**, **153**, **156**, and **158** extending in the Y-direction that is perpendicular to the X-direction. Each of the three gate-strips **151**, **152**, and **153** intersects both the p-type active zone **80p** and the n-type active zone **80n** and overlaps with the channel regions of corresponding p-type transistors and n-type transistors. Specifically, as shown in the stick diagram of FIG. 1C, the gate-strip **151** overlaps the channel region of a p-type transistor T1p and the channel region of an n-type transistor T1n. The gate-strip **152** overlaps the channel region of a p-type transistor T2p and the channel region of an n-type transistor T2n. The gate-strip **153** overlaps the channel region of a p-type transistor T3p and the channel region of an n-type transistor T3n. The channel regions of the p-type transistors T1p, T2p, and T3p are in the p-type active zone **80p**. The channel regions of the n-type transistors T1n, T2n, and T3n are in the n-type active zone **80n**. In some embodiments, the gate-strips **156** and **158** in FIG. 1A are dummy gate-strips which do not form gate terminals of functioning transistors connected in a circuit.

[0045] In the layout diagram of FIG. 1A, the buffer logic gate **100** includes multiple conductive segments **132**, **134p**, **134n**, **136**, **138p**, and **138n** extending in the Y-direction. Each of the conductive segments **132** and **136** intersects both the p-type active zone **80p** and the n-type active zone **80n**. Each of the conductive segments **134p** and **138p** intersects the p-type active zone **80p**. Each of the conductive segments **134n** and **138n** intersects the n-type active zone **80n**. Each of the multiple conductive segments **132**, **134p**, **134n**, **136**, **138p**, and **138n** overlap at least one source/drain region of a transistor. Specifically, in the stick diagram of FIG. 1C, the conductive segment **132** overlaps the source/drain regions of the p-type transistor T1p and the source/drain region of the n-type transistor T1n. The conductive segment **134p** overlaps the source/drain regions of the p-type transistors T1p and T2p, and the conductive segment **134n** overlaps the source/drain regions of the n-type transistors T1n and T2n. The conductive segment **136** overlaps the source/drain regions of two p-type transistors (T2p and T3p) and overlaps the source/drain regions of two n-type transistors (T2n and T3n). The conductive segment **138p** overlaps the source/drain region of the p-type transistors T3p, and the conductive segment **138n** overlaps the source/drain region of the n-type transistors T3n. Each of the conductive segments **134p** and **138p** is also conductively connected to the power rail **122**. Each of the conductive segments **134n** and **138n** is also conductively connected to the power rail **124**. The source/drain regions of the p-type transistors T1p, T2p, and T3p are in the p-type active zone **80p**. The source/drain regions of the n-type transistors T1n, T2n, and T3n are in the n-type active zone **80n**.

[0046] In the layout diagram of FIG. 1A, the buffer logic gate **100** includes horizontal routing tracks (e.g., **142**, **144**, and **146**) extending in the X-direction. As shown in the layout diagram of FIG. 1A and in the stick diagram of FIG. 1C, the horizontal routing track **144** is conductively connected to the gate-strip **151** through a via connector VG, and the horizontal routing track **146** is conductively connected to the conductive segment **136** through a via connector VD. In FIG. 1C, the horizontal routing track **142** is not used to carry electrical signals for the buffer logic gate **100**.

[0047] In the layout diagram of FIG. 1B, the buffer logic gate **100** includes a backside routing track **162** extending in the X-direction and backside via connectors VB and VBd for connecting the backside routing track **162** to other elements in the circuit. Specifically, as shown in the stick

diagram of FIG. 1C, the backside routing track **162** is conductively connected to each of the gate-strips **152** and **153** through a backside via connector VB. The backside routing track **162** is also conductively connected to the conductive segment **132** through a backside via connector VBd. In the layout diagram of FIG. 1B, the backside routing track **162** and the backside via connectors VBd and VB are depicted and superimposed on the layout patterns in FIG. 1A, while ignoring the depiction of the front side via connectors VG and VD, for better clarity.

[0048] In the layout diagram of FIG. 1B, some of the device elements are specified with layout patterns in abstract representations. For example, while each of the backside via connectors VB and VBd in FIG. 1B is represented by a triangle pattern, the physical shapes of the backside via connectors are not necessarily triangular in shape. In some embodiments, the triangle pattern generally specifies the location of a backside via connector that is needed for connecting an identified backside routing track with another identified conductive element (such as an identified gate-strip or an identified conductive segment which is a source/drain terminal of a transistor). In some embodiments, when the layout diagram is interpreted by a software interpreter program, the triangle pattern is translated into the corresponding mask patterns in a mask set for fabricating the backside via connector represented by the triangle pattern. In some embodiments, the shape and the dimensions of the mask patterns in the mask set for fabricating the backside via connector depend upon the technologies used for the fabrication. In some embodiments, each opening in the masks for fabricating the backside via connector is rectangular or square in shape, and consequently, the shape of the backside via connector in the top view at a selected plane is correspondingly rectangular shape or square shape. In some embodiments, the shape and the dimensions of the mask patterns in the mask set for fabricating the backside via connector are provided by a database or a technology file associated with the technologies used for the fabrication. Some example shapes of the backside via connectors VB and VBd are provided in the cross-sectional views of FIGS. 2A-2D.

[0049] Furthermore, in some embodiments, when a layout diagram is displayed in an editing mode on a display screen, the order of the layers of various layout patterns is not the same as the as-fabricated order of the layers containing the fabricated elements specified by the layout patterns. For example, in some embodiments, when the layout patterns for the backside via connectors VB and VBd are selected for editing in an editing mode, the layout patterns for the backside via connectors as shown in FIG. 1B is bring up to be in front of all other layout patterns. When another layout element (such as, a gate-strip or a conductive segment) is selected for editing, in some embodiments, the newly selected layout element is bring up to be in front of all other layout patterns.

[0050] FIGS. 2A-2D are cross-sectional views of the buffer logic gate **100** along selected cutting planes as specified by the layout diagrams in FIGS. 1A-1B, in accordance with some embodiments. In FIGS. 2A-2D, the power rails **122** and **124**, the horizontal routing tracks **142**, **144**, and **146**, the front side via connectors VG and VD, and the insulation layer **212** are formed at the front side of the substrate **210**, while the backside routing track **162** and the backside via connectors. VB and VBd are formed at the backside of the substrate **210**. The Z-direction, which is perpendicular to the Y-direction and the X-direction (which is not shown in FIGS. 2A-2D), points towards the front side of the substrate **210**.

[0051] FIG. 2A is a cross-sectional view of the buffer logic gate **100** along the cutting plane P1-P1' as shown in FIG. 1B, in accordance with some embodiments. In FIG. 2A, the channel region **282p** of the p-type transistor T2p, the channel region **282n** of the n-type transistor T2n, and the gate-strip **152** are also formed at the front side of the substrate **210**. The backside routing track **162** and the backside via connectors VB are formed at the backside of the substrate **210**. The channel region **282p** of the p-type transistor T2p and the channel region **282n** of the n-type transistor T2n are formed with nanosheet materials. Correspondingly, the p-type transistor T2p and the n-type transistor T2n are both nanosheet transistors. In other embodiments, the channel region **282p** of the

p-type transistor **T2p** and the channel region **282n** of the n-type transistor **T2n** are formed with nanowire materials, while the transistors **T2p** and **T2n** are nanowire transistors. In other embodiments, the channel region **282p** of the p-type transistor **T2p** and the channel region **282n** of the n-type transistor **T2n** are formed with fin structures, while the transistors **T2p** and **T2n** are fin transistors. In FIG. 2A, the gate-strip **152** is connected to the gate terminal of the p-type transistor **T2p** and the gate terminal of the n-type transistor **T2n**. The backside routing track **162** is conductively connected to the gate-strip **152** through the backside via connectors VB.

[0052] FIG. 2B is a cross-sectional view of the buffer logic gate **100** along the cutting plane P2-P2' as shown in FIG. 1B, in accordance with some embodiments. In FIG. 2B, the source/drain region **292p** of the p-type transistors **T1p**, the source/drain region **292n** of the n-type transistor **T1n**, and the conductive segments **132** are formed at the front side of the substrate **210**. The backside routing track **162** and the backside via connectors VBd are formed at the backside of the substrate **210**. The conductive segment **132** is connected to the drain terminal of the p-type transistor **T1p** and the drain terminal of the n-type transistor **T1n**. The backside routing track **162** is conductively connected to the conductive segment **132** through the backside via connectors VBd.

[0053] FIG. 2C is a cross-sectional view of the buffer logic gate **100** along the cutting plane P3-P3' as shown in FIG. 1A, in accordance with some embodiments. In FIG. 2C, the channel region **281p** of the p-type transistor **T1p**, the channel region **281n** of the n-type transistor **T2n**, the gate-strip **151**, and the via connector VG are formed at the front side of the substrate **210**. Examples of the p-type transistor **T1p** and the n-type transistor **T2n** include nanosheet transistors, nanowire transistors, and fin transistors. In FIG. 2C, the gate-strip **151** is connected to the gate terminal of the p-type transistor **T1p** and the gate terminal of the n-type transistor **T1n**. The horizontal routing track **144** is conductively connected to the gate-strip **151** through the via connector VG at the front side of the substrate **210**.

[0054] FIG. 2D is a cross-sectional view of the buffer logic gate **100** along the cutting plane P4-P4' as shown in FIG. 1A, in accordance with some embodiments. In FIG. 2D, the source/drain region **296p** of the p-type transistors **T2p** and **T3p**, the source/drain region **296n** of the n-type transistors **T2n** and **T3n**, the conductive segments **136**, and the via connector VD are formed at the front side of the substrate **210**. The source/drain terminal **296p** of the p-type transistors **T2p** and **T3p** are connected, through the conductive segment **136**, to the source/drain terminal **296n** of the n-type transistors **T2n** and **T3n**. The horizontal routing track **146** is conductively connected to the conductive segment **136** through the via connector VD at the front side of the substrate **210**.

[0055] The locations of the backside via connectors VB, the backside via connector VBd, the via connector VG, and the via connector VD as shown in FIGS. 2A-2D are also schematically depicted in the stick diagram of FIG. 1C. FIG. 1D is an equivalent circuit of the buffer logic gate **100** as specified by the stick diagram in FIG. 1C, in accordance with some embodiments. In FIG. 1C and FIG. 1D, the source terminals of the p-type transistors **T1p**, **T2p**, and **T3p** are connected to the first power supply VDD, and the drain terminals of the n-type transistors **T1n**, **T2n**, and **T3n** are connected to the second power supply VSS. The gate terminal of the p-type transistor **T1p** and the gate terminal of the n-type transistor **T1n** are connected together by the gate-strip **151**, the gate terminal of the p-type transistor **T2p** and the gate terminal of the n-type transistor **T2n** are connected together by the gate-strip **152**, and the gate terminal of the p-type transistor **T3p** and the gate terminal of the n-type transistor **T3n** are connected together by the gate-strip **153**. The drain terminal of the p-type transistor **T1p** and the drain terminal of the n-type transistor **T1n** are connected together by the conductive segment **132**. The drain terminals of the p-type transistors **T2p** and **T3p** are connected to the drain terminals of the n-type transistors **T2n** and **T3n** by the conductive segment **136**. The conductive segment **132** is conductively connected to the gate-strips **152** and **153** through the backside routing track **162**, after conductively passing through the backside via connectors VBd and VB. The horizontal routing track **144** is conductively connected to the gate-strip **151** through the front end via connectors VG and provides the input terminal "I"

for the buffer logic gate **100**. The horizontal routing track **146** is conductively connected to the conductive segment **136** through the front end via connectors VD and provides the output terminal “Z” for the buffer logic gate **100**.

[0056] FIG. **1E** is a circuit diagram of the logic gates formed from the transistors in FIG. **1D**, in accordance with some embodiments. The p-type transistor T_{1p} and the n-type transistor T_{1n} in FIG. **1D** are connected to form an inverter INV1. The p-type transistor T_{2p} and the n-type transistor T_{2n} in FIG. **1D** are connected to form an inverter INV2. The p-type transistor T_{3p} and the n-type transistor T_{3n} in FIG. **1D** are connected to form an inverter INV3. The inverter INV1 receives a first digital input signal from the input terminal “I” and generates a first digital output signal at the intermediate node “n1” between the output of the inverter INV1 and the inputs of the inverters INV2 and INV3. The inverters INV2 and INV3 receive the first digital output signal at the intermediate node “n1” and generates a second digital output signal at the output terminal “Z.” The buffer logic gate **100** is formed by the inverters INV1, INV2, and INV3.

[0057] In FIG. **1E**, the digital input signal received at the input terminal “I” has a first phase $\Phi_{\text{sub.}+}$, the intermediate output signal at the intermediate node “n1” has a second phase $\Phi_{\text{sub.}-}$, and the output signal generated at the output terminal “Z” has the first phase $\Phi_{\text{sub.}+}$. Because the phase of the intermediate output signal at the intermediate node “n1” is opposite to the phase of the input signal at the input terminal “I”, whenever the input signal changes from a first voltage level to a second voltage level, the intermediate output signal correspondingly changes from the second voltage level to the first voltage level. If the first voltage level is logic HIGH, the second voltage level is logic LOW. If the first voltage level is logic LOW, the second voltage level is logic HIGH. Similarly, because the phase of the output signal generated at the output terminal “Z” is opposite the phase of the intermediate output signal at the intermediate node “n1”, whenever the intermediate output signal changes from the second voltage level to the first voltage level, the output signal generated at the output terminal “Z” correspondingly changes from the first voltage level to the second voltage level.

[0058] FIG. **1F** is a stick diagram of the buffer logic gate **100** formed by the layout diagrams in FIGS. **1A-1B**, in accordance with some embodiments. The stick diagram in FIG. **1F** is a modification of the stick diagram in FIG. **1C**, by labeling the phases of various signals on the routing tracks. The input signal having the first phase $\Phi_{\text{sub.}+}$ is carried by the horizontal routing track **144**, and the output signal having the first phase $\Phi_{\text{sub.}+}$ is carried by the horizontal routing track **146**. The intermediate output signal having the second phase $\Phi_{\text{sub.}-}$ at the intermediate node “n1” is carried by the backside routing track **162**. When the routing track carrying the input signal with the first phase $\Phi_{\text{sub.}+}$ is adjacent to the routing track carrying the intermediate output signal with the second phase $\Phi_{\text{sub.}-}$ that is opposite to the first phase $\Phi_{\text{sub.}+}$, the capacitive coupling between the two adjacent routing tracks often reduces the speed performance and increases the power consumption of the logic circuit. In the layout of FIGS. **1A-1B**, the capacitive coupling between the backside routing track **162** and each of the horizontal routing tracks **144** and **146** is smaller than the capacitive coupling between two adjacent horizontal routing tracks **144** and **146**. When the intermediate node “n1” is placed on the backside routing track **162**, the speed and the power consumption of the buffer logic gate **100** are improved over some other approaches in which some signals of opposite phases are carried by two adjacent horizontal routing tracks.

[0059] FIGS. **3A-3B** are partial layout diagrams of an And-Or-Inverter (“AOI”) logic circuit **300** having two backside routing tracks, in accordance with some embodiments. In FIG. **3A**, elements formed on the front side of the substrate are shown in corresponding layout patterns. In FIG. **3B**, the backside routing track and the backside via connectors formed on the back side of the substrate are depicted with layout patterns superimposed on the layout patterns in FIG. **3A**, while ignoring the depiction of the front side via connectors VG and VD, for better clarity. FIG. **3C** is a stick diagram of the AOI logic circuit **300** formed by the layout diagrams in FIGS. **3A-3B**, in accordance with some embodiments. The AOI logic circuit **300** formed by the layout diagrams in FIGS. **3A-3B**

is an example of the 2-2AOI logic circuit in FIG. 5A. The logic symbol of the 2-2AOI logic circuit is shown in FIG. 5B. In FIGS. 5A-5B, the output ZN is related to the inputs A1, A2, B1, and B2 by the logic relationship $ZN=(A1.Math.A2+B1.Math.B2)$.

[0060] FIG. 5A is a circuit diagram of the AOI logic circuit, in accordance with some embodiments. In FIG. 5A, the source terminals of the p-type transistors having inputs B1 and B2 are connected to the power supply VDD. The drain terminals of the p-type transistors having inputs B1 and B2 are connected together as the node n01. The source terminals of the p-type transistors having inputs A1 and A2 are also connected to the node n01. The drain terminals of the p-type transistors having inputs A1 and A2 are connected together as the output terminal ZN. The drain terminals of the n-type transistors having inputs A1 and B1 are also connected to the output terminal ZN. The source terminal of the n-type transistor having inputs A1 is connected to the drain terminal of the n-type transistor having input A2, and the source terminal of the n-type transistor having inputs B1 is connected to the drain terminal of the n-type transistor having input B2. The source terminals of the n-type transistors having inputs A2 and B2 are connected to the power supply VSS.

[0061] In FIG. 5A, the voltage level change at the output terminal ZN induced by the voltage level change at an input terminal (such as A1, A2, B1, or B2) has the second phase $\Phi_{sub.-}$ that is opposite to the first phase $\Phi_{sub.+}$ of the input voltage level change. As an example, the voltage level change at the output terminal ZN induced by the voltage level change at the input A1 is depicted in the inset of FIG. 5A. When the signal at the input A1 changes from a first voltage level to a second voltage level, the signal at the output terminal ZN correspondingly changes from the second voltage level to the first voltage level. In the layout design of FIGS. 3A-3B, when two adjacent routing tracks on a same metal layer do not carry signals with opposite phases, both the speed and the power consumption of the AOI logic circuit 300 are improved, as compared with some other approaches in which some signals of opposite phases are placed on two adjacent horizontal routing tracks.

[0062] The elements formed on the front side of the substrate and specified by the layout patterns in FIG. 3A include the active zones, the gate-strips, the conductive segments, the horizontal routing tracks, the power rails, and the via connectors. In FIG. 3A, the p-type active zone 80p and the n-type active zone 80n are both extending in the X-direction. Each of the gate-strips gA1, gA2, gB1, gB2, extending in the Y-direction, overlaps the p-type active zone 80p and forms correspondingly the gate terminals of the p-type transistors pA1, pA2, pB1, and pB2 (as shown in FIGS. 3C-3D). Each of the gate-strips gA1, gA2, gB1, gB2 also overlaps the n-type active zone 80n and forms correspondingly the gate terminals of the n-type transistors nA1, nA2, nB1, and nB2 (as shown in FIGS. 3C-3D). The gate-strips 156 and 158 are dummy gate-strips.

[0063] In FIG. 3A and FIG. 3C, the conductive segments 332p, 334p, 335p, 336p, and 338p overlap the p-type active zone 80p and form the source/drain terminals of the p-type transistors. The conductive segments 332n, 334n, 335n, 336n, and 338n overlap the n-type active zone 80n and form the source/drain terminals of the n-type. The horizontal routing tracks A1, A2, B1, B2, and ZN extending in the X-direction are formed in a first metal layer M0 on the front side of the substrate. The horizontal routing tracks A1, A2, B1, B2 are correspondingly connected to the gate-strips gA1, gA2, gB1, gB2 through the via connector VG formed on the front side of the substrate. The horizontal routing track ZN is connected to the conductive segment 336p through the via connector VD. The conductive segment 336 is located between the gate-strips gA1 and gA2. The power rails 122 and 124 extending in the X-direction are configured to provide correspondingly the supply voltages VDD and VSS. The conductive segment 334p (located between the gate-strips gB1 and gB2) is connected to the power rail 122 for receiving the supply voltage VDD. The conductive segments 332p (located between the gate-strips gB2 and dummy gate-strip 156) and the conductive segments 332p (located between the gate-strips gA2 and dummy gate-strip 158) are both connected to the power rail 124 for receiving the supply voltage VSS.

[0064] The elements formed on the back side of the substrate and specified by the layout patterns in FIG. 3B include the backside routing tracks **362** and **364**, and the backside via connectors VBd. In FIG. 3B and FIG. 3C, the backside routing track **362** is connected to the conductive segments **332p**, **335p**, and **338p** through the backside via connectors VBd. The backside routing track **364** is connected to the conductive segments **335n** and **336p** through the backside via connectors VBd. [0065] FIG. 3D is an equivalent circuit of the AOI logic circuit **300** as specified by the stick diagram in FIG. 3C, in accordance with some embodiments. In FIGS. 3C and 3D, the gate terminals of the p-type transistor pB2 and the n-type transistor nB2 are connected together by the gate-strip gB2, the gate terminals of the p-type transistor pB1 and the n-type transistor nB1 are connected together by the gate-strip gB1, the gate terminals of the p-type transistor pA1 and the n-type transistor nA1 are connected together by the gate-strip gA1, and the gate terminals of the p-type transistor pA2 and the n-type transistor nA2 are connected together by the gate-strip gA2. The source terminals of the p-type transistors pB2 and pB1 are connected to the power supply VDD. The drain terminals of the p-type transistors pB2 and pB1 are connected to the source terminals of the p-type transistors pA1 and pA2 through the backside routing track **362**. The drain terminals (on the conductive segment **336p**) of the p-type transistors pA1 and pA2 are connected to the drain terminals (on the conductive segment **335n**) of the n-type transistors nB1 and nA1 through the backside routing track **364**. The source terminal of the n-type transistor nB1 and the source terminal of the n-type transistor nA1 are correspondingly connected to the drain terminal of the n-type transistor nB2 and the drain terminal of the n-type transistor nA2. The source terminals of the n-type transistors nB2 and nA2 are connected to the power supply VSS. The horizontal routing tracks A1, A2, B1, and B2 (which are correspondingly connected to the gate-strips gA1, gA2, gB1, and gB2) are configured to receive the input signals. The horizontal routing tracks ZN (which is connected to the conductive segment **336p**) is configured to transmit the output signal.

[0066] FIG. 3E is another stick diagram of the AOI logic circuit **300** formed by the layout diagrams in FIGS. 3A-3B, in accordance with some embodiments. The stick diagram in FIG. 3E is a modification of the stick diagram in FIG. 3C, by labeling the phases of various signals on the routing tracks. The input signals A1, A2, B1, and B2 of the AOI logic circuit **300** are correspondingly carried by the horizontal routing tracks A1, A2, B1, and B2. The output signal ZN of the AOI logic circuit **300** is carried by the horizontal routing track ZN and the backside routing track **364**. The intermediate signal at the node "n01" received from the drain terminals of the p-type transistors B1 and B2 is carried by the backside routing track **362**. In FIG. 3E, the horizontal routing tracks A1, A2, B1, and B2 carry signals with the first phase Φ_+ . The backside routing tracks **362** and **364** carry signals with the second phase Φ_{sub-} . The horizontal routing track ZN also carries signals with the second phase Φ_{sub-} . In the layout designs in FIGS. 3A-3B, adjacent routing tracks on a same metal layer do not carry signals with opposite phases, and the speed and the power consumption of the AOI logic circuit **300** are improved. In FIGS. 3A-3B, signals with the first phase Φ_{sub+} are carried by the horizontal routing tracks (e.g., A1, A2, B1, and B2) on the front side of the substrate, while signals with the second phase Φ_{sub-} are carried by the backside routing tracks (e.g., **362** and **364**) on the backside of the substrate.

[0067] Another example layout design of the 2-2 AOI logic circuit in FIGS. 5A-5B is the AOI logic circuit **400** formed by the layout diagrams in FIGS. 4A-4C. In FIGS. 5A-5B, the output ZN is related to the inputs A1, A2, B1, and B2 and expressed as the logic relationship $ZN = (A1 \cdot A2 + B1 \cdot B2)$. FIGS. 4A-4C are partial layout diagrams of an AOI logic circuit **400** having one backside routing track, in accordance with some embodiments. FIG. 4D is a stick diagram of the AOI logic circuit **400** formed by the layout diagrams in FIGS. 4A-4C, in accordance with some embodiments.

[0068] In FIG. 4A and FIG. 4C, elements formed on the front side of the substrate are selectively shown in corresponding layout patterns. The elements formed on the front side of the substrate and specified by the layout patterns in FIG. 4A include the active zones, the gate-strips, conductive

segments, the horizontal routing tracks, power rails, and the front side via connectors. Some of the elements in the layout of FIG. 4A are arranged identically as the corresponding elements in the layout of FIG. 3A. The identically arranged elements include the active zones **80p** and **80n**, the gate-strips **gA1**, **gA2**, **gB1**, and **gB2**, the power rails **122** and **124**, the conductive segments (**332p**, **334p**, **335p**, **336p**, **338p**, **332n**, **334n**, **335n**, **336n**, and **338n**), and some of the horizontal routing tracks **B1**, and **B2**. In comparison with the layout of FIG. 3A, some of the horizontal routing tracks **A1**, and **A2** in FIG. 4A are modified to shift in positions along the Y-direction. In both FIG. 4A and FIG. 3A, each of the horizontal routing tracks **A1**, **A2**, **B1**, and **B2** is correspondingly connected to one of the gate-strips **gA1**, **gA2**, **gB1**, and **gB2** through the via connectors **VG**. A comparison between the layouts of FIG. 4A and FIG. 3A indicates that the horizontal routing track **ZN** is substituted with the horizontal routing tracks **442** and **448**.

[0069] In FIG. 4B, the backside routing track **362** and the backside via connectors **VBd** formed on the back side of the substrate are depicted with layout patterns superimposed on the layout patterns in FIG. 4A, while ignoring the depiction of the front side via connectors **VG** and **VD**, for better clarity. The position of the backside routing track **362** is modified along the Y-direction, when the layout of FIG. 4B is compared with the layout of FIG. 3B. Similar to the layout in FIG. 3B, the backside routing track **362** in the layout of FIG. 4B is also connected to the conductive segments **332p**, **335p**, and **338p** through the backside via connectors **VBd**. A comparison between the layouts of FIG. 4B and FIG. 3B indicates that the backside routing track **364** is removed in the layout of FIG. 4B.

[0070] In FIG. 4C, the vertical routing track **472** and the via connectors **V0** are depicted with layout patterns superimposed on the layout patterns in FIG. 4A, while ignoring the depiction of the front side via connectors **VG** and **VD**, for better clarity. The vertical routing track **472** extending in the Y-direction is formed in a second metal layer **M1** on top of the interlayer dielectric overlying the first metal layer **M0**. The vertical routing track **472** is connected to the horizontal routing tracks **442** and **448** through the via connectors **V0** between the second metal layer **M1** and the first metal layer **M0**.

[0071] The stick diagram of the AOI logic circuit **400** in FIG. 4D is almost identical to the stick diagram of the AOI logic circuit **300** in FIG. 3C, other than the different routes of connections between the conductive segment **336p** and the conductive segments **335n**. In the stick diagram of FIG. 4D, the conductive segment **336p** is connected to the horizontal routing track **442** through the via connector **VD**, the horizontal routing track **442** is connected to the vertical routing track **472** through the via connector **V0**, the vertical routing track **472** is connected to the horizontal routing track **448** through the via connector **V0**, the horizontal routing track **448** is connected to the conductive segment **335n** through the via connector **VD**. As a comparison, in the stick diagram of FIG. 3C, the conductive segment **336p** is connected to the conductive segments **335n** through the backside routing track **364** and the backside via connectors **VBd**.

[0072] FIG. 4E is an equivalent circuit of the AOI logic circuit **400** as specified by the stick diagram in FIG. 4D, in accordance with some embodiments. With the exception of the conductive connection from the conductive segments **336p** to the conductive segments **335n**, the circuit connections in FIG. 4E and in FIG. 3D are identical. In FIG. 4E, the conductive segments **336p** is connected to the conductive segments **335n** through the horizontal routing track **442**, the vertical routing track **472**, and the horizontal routing track **448**. In FIG. 3D, the conductive segments **336p** is connected to the conductive segments **335n** through the backside routing track **364**.

[0073] FIG. 4F is another stick diagram of the AOI logic circuit **400** formed by the layout diagrams in FIGS. 4A-4C, in accordance with some embodiments. The stick diagram in FIG. 4F is a modification of the stick diagram in FIG. 4D, by labeling the phases of various signals on the routing tracks. The input signals **A1**, **A2**, **B1**, and **B2** of the AOI logic circuit **400** are correspondingly carried by the horizontal routing tracks **A1**, **A2**, **B1**, and **B2**. The output signal **ZN** of the AOI logic circuit **400** is carried by the horizontal routing tracks **442** and **448** and by the vertical routing track

472. The intermediate signal at the node “n01” received from the drain terminals of the p-type transistors B1 and B2 is carried by the backside routing track **362**.

[0074] In FIG. 4F, the horizontal routing tracks A1, A2, B1, and B2 carry input signals with the first phase $\Phi_{\text{sub.}+}$. The backside routing tracks **362** carry signals with the second phase $\Phi_{\text{sub.}-}$. The horizontal routing tracks **442** and **448** and the vertical routing track **472** carry the output signal ZN with the second phase $\Phi_{\text{sub.}-}$. In the layout designs of FIGS. 4A-4C, there are only three pairs of adjacent routing tracks that carry signals with opposite phases. The first pair is formed by the routing track A1 and the horizontal routing tracks **448**. The second pair is formed by the routing track A2 and the horizontal routing tracks **448**. The third pair is formed by the routing track A2 and the horizontal routing tracks **442**. In the layout designs of FIGS. 4A-4C, the sum of the capacitive couplings between the three pairs of adjacent routing tracks having signals with the opposite phases is reduced as compared with some of the alternative designs in which no backside routing track is available. The speed and the power consumption of the AOI logic circuit **400** are improved over some of the alternative designs which have no backside routing tracks. In addition, in embodiments in which the backside routing track **362** is not positioned near the edges of the cell of the AOI logic circuit **400**, it is possible to place the cell of the AOI logic circuit **400** vertically near another cell having backside routing tracks near the edges of the cell. In some embodiments, it is possible to achieve better cell density in a circuit designed with the AOI logic circuit **400** than that in a circuit designed with the AOI logic circuit **300**. Furthermore, the cell width of the AOI logic circuit **400** is only 5 CPP, whereas the cell width of an AOI logic circuit of another approach (which has no backside routing tracks) generally is larger than or equal to 7 CPP. Here, the unit of one CPP (Contacted Poly Pitch) is the pitch distance between the two adjacent gate-strips, such as the pitch distance between the gate-strips gB2 and gB1. In FIGS. 4A-4C, the cell width of the AOI logic circuit **400** is equal to the pitch distance between the dummy gate-strips **156** and **158**.

[0075] FIGS. 6A-6C are partial layout diagrams of a multiplexer circuit **600**, in accordance with some embodiments. FIG. 6D is an equivalent circuit of the multiplexer circuit **600** formed by the layout diagrams in FIGS. 6A-6C, in accordance with some embodiments. The multiplexer circuit **600** formed by the layout diagrams in FIGS. 6A-6C is an example of the four channel multiplexer circuit in FIG. 6F. An implementation of the four channel multiplexer circuit based logic gates is shown in FIG. 6G. In FIGS. 6F-6G, the output Z is related to the inputs I0, I1, I2, and I3 and the selection signals S0, S1, S2, and S3. The logic relationship for specifying the output Z is expressed as $Z = I0 \cdot \text{Math.S0} + I1 \cdot \text{Math.S1} + I2 \cdot \text{Math.S2} + I3 \cdot \text{Math.S3}$.

[0076] In FIG. 6A and FIG. 6D, elements formed on the front side of the substrate are shown in corresponding layout patterns. The elements formed on the front side of the substrate and specified by the layout patterns in FIG. 6A include the active zones, the gate-strips, the conductive segments, the horizontal routing tracks, the power rails, and the front side via connectors. The gate-strips gS1, gI1, gI0, and gS0 overlaps the p-type active zone **80p** and correspondingly form the gate terminals of the p-type transistors pS1, pI1, pI0, and pS0 (as shown in FIG. 6D). The gate-strips gS2, gI2, gI3, and gS3 overlaps the p-type active zone **80p** and correspondingly form the gate terminals of the p-type transistors pS2, pI2, pI3, and pS3 (as shown in FIG. 6D). The gate-strips gS1, gI1, gI0, and gS0 overlaps the n-type active zone **80n** and correspondingly form the gate terminals of the n-type transistors nS1, nI1, nI0, and nS0 (as shown in FIG. 6D). The gate-strips gS2, gI2, gI3, and gS3 overlaps the n-type active zone **80n** and correspondingly form the gate terminals of the n-type transistors nS2, nI2, nI3, and nS3 (as shown in FIG. 6D). The gate-strips g03 and g04 overlaps the p-type active zone **80p** and correspondingly form the gate terminals of the p-type transistors pT3 and pT4 (as shown in FIG. 6D). The gate-strips g03 and g04 overlaps the n-type active zone **80n** and correspondingly form the gate terminals of the n-type transistors nT3 and nT4 (as shown in FIG. 6D). Dummy gate-strips **156**, **656**, **658**, and **158** are not configured as gate terminals of transistors for using in the equivalent circuit of the multiplexer circuit **600** (as shown in FIG. 6D).

[0077] In FIG. 6A and FIG. 6D, the horizontal routing tracks S1, S0, S2, and S3 are

correspondingly connected to the gate-strips gS1, gS0, gS2, and gS3 through front end via connectors VG. The horizontal routing tracks I1, I0, I2, and I3 are correspondingly connected to the gate-strips gI1, gI0, gI2, and gI3 through front end via connectors VG. The horizontal routing track n01 is connected to the conductive segments cp_S1, cp_I1I0, and cp_S0 through front end via connectors VD. The horizontal routing track n02 is connected to the conductive segments cp_S2, cp_I2I3, and cp_S3 through front end via connectors VD. The horizontal routing track 642 is connected to the conductive segment cp_0304 through a front end via connector VD. The horizontal routing track 648 is connected to the conductive segment cn_03 through a front end via connector VD. The source terminals of the p-type transistors pS1, pI1, pI3, pS3, pT3, and pT4 are connected to the power supply VDD. The source terminals of the n-type transistors nS1, nS0, nS2, nS3, and nT4 are connected to the power supply VSS.

[0078] In FIG. 6C and FIG. 6D, the vertical routing track 672 extending in the Y-direction is depicted with layout patterns superimposed on the layout patterns in FIG. 6A, while ignoring the depiction of the front side via connectors VG and VD, for better clarity. The vertical routing track 672 extending in the Y-direction is formed in a second metal layer M1 on top of the interlayer dielectric overlying the first metal layer M0. The horizontal routing tracks 642 and 648 are connected by the vertical routing track 672 through the via connectors V0 between the second metal layer M1 and the first metal layer M0.

[0079] In FIG. 6B, the backside routing tracks and the backside via connectors formed on the back side of the substrate are depicted with layout patterns superimposed on the layout patterns in FIG. 6A, while ignoring the depiction of the front side via connectors VG and VD, for better clarity. The elements formed on the back side of the substrate and specified by the layout patterns in FIG. 6B include the backside routing tracks n03 and n04, and the backside via connectors VB and VBd. In FIG. 6B and FIG. 6D, the backside routing track n03 is connected to the conductive segments cn_I1I0 and cp_I0S0 through backside via connectors VBd. The backside routing track n03 is also connected to the gate-strip g03 through backside via connector VB. The backside routing track n04 is connected to the conductive segments cn_I2I3 and cp_S2I2 through backside via connectors VBd. The backside routing track n04 is also connected to the gate-strip g04 through backside via connector VB.

[0080] FIG. 6E is another stick diagram of the multiplexer circuit 600 formed by the layout diagrams in FIGS. 6A-6C, in accordance with some embodiments. The stick diagram in FIG. 6E is a modification of the stick diagram in FIG. 6D, by labeling the phases of various signals on the routing tracks. The horizontal routing tracks I0, I1, I2, I3, S0, S1, S2, S3, 642, and 648 carry signals with the first phase $\Phi_{\text{sub.}+}$. The vertical routing track 672 also carries signals with the first phase $\Phi_{\text{sub.}+}$. The horizontal routing tracks n01 and n02 and the backside routing tracks n03 and n04 carry signals with the second phase $\Phi_{\text{sub.}-}$ that is opposite to the first phase $\Phi_{\text{sub.}+}$. In FIGS. 6A-6C, adjacent routing tracks on a same metal layer (such as the metal layer M0) do not carry signals with the opposite phase. Consequently, the speed and the power consumption of the multiplexer circuit 600 are improved over some of the alternative designs which have capacitive couplings due to opposite phase signals carried by adjacent routing tracks on a same metal layer. In FIGS. 6A-6C, signals with the first phase $\Phi_{\text{sub.}+}$ are carried by the horizontal routing tracks on the front side of the substrate, while signals with the second phase $\Phi_{\text{sub.}-}$ are carried by the backside routing tracks (e.g., n01, n02, n03, and n04) on the backside of the substrate.

[0081] FIGS. 7A-7B are partial layout diagrams of a logic-gates combo circuit 700 having a backside routing track, in accordance with some embodiments. FIG. 7C is an equivalent circuit of the logic-gates combo circuit 700 formed by the layout diagrams in FIGS. 7A-7B, in accordance with some embodiments.

[0082] In FIG. 7A, elements formed on the front side of the substrate are shown in corresponding layout patterns. The elements formed on the front side of the substrate and specified by the layout patterns in FIG. 7A include the active zones, the gate-strips, the conductive segments, the

horizontal routing tracks, the power rails, and the via connectors. The p-type active zone **80p** and the n-type active zone **80n** are both extending in the X-direction. Each of the gate-strips **gA1**, **gA2**, **gZN**, **gA3**, and **gA4** extending in the Y-direction overlaps the p-type active zone **80p** and forms correspondingly the gate terminal of one of the p-type transistors **pA1**, **pA2**, **pZN**, **pA3**, and **pA4** (as shown in FIG. 7C). Each of the gate-strips **gA1**, **gA2**, **gZN**, **gA3**, and **gA4** also overlaps the n-type active zone **80n** and forms correspondingly the gate terminal of one of the n-type transistors **nA1**, **nA2**, **nZN**, **nA3**, and **nA4** (as shown in FIG. 7C). In FIG. 7A and FIG. 7C, the horizontal routing tracks **A1**, **A2**, **A3**, and **A4** are correspondingly connected to the gate-strips **gA1**, **gA2**, **gA3**, and **gA4** through the via connectors **VG** formed on the front side of the substrate. The horizontal routing track **742** is connected to the conductive segments **cn_ZNA3** and **c_A4** through the via connectors **VD**. The source terminals of the p-type transistors **pA1**, **pA2**, and **pZN** are connected to the power rail **122** for receiving the supply voltage **VDD**. The source terminals of the n-type transistors **nA2**, **nZN**, **nA3**, and **nA4** are connected to the power rail **124** for receiving the supply voltage **VSS**.

[0083] In FIG. 7B, the backside routing track and the backside via connectors formed on the back side of the substrate are depicted with layout patterns superimposed on the layout patterns in FIG. 7A, while ignoring the depiction of the front side via connectors **VG** and **VD**, for better clarity. The elements formed on the back side of the substrate and specified by the layout patterns in FIG. 7B include the backside routing track **762**, and the backside via connectors **VB** and **VBd**. In FIG. 7B and FIG. 7C, the backside routing track **762** is connected to the conductive segments **cn_A1** and **cp_A1A2** through backside via connectors **VBd**. The backside routing track **762** is also connected to the gate-strip **gZN** through backside via connector **VB**. In FIG. 7C, the horizontal routing tracks **A1**, **A2**, **A3**, and **A4** (which are correspondingly connected to the gate-strips **gA1**, **gA2**, **gA3**, and **gA4**) are configured as the input terminals for receiving the input signals. The horizontal routing track **742** is configured as the out terminal “OUT” for transmitting the output signal.

[0084] FIG. 7D is a circuit diagram of the logic gates formed from the transistors in FIG. 7C, in accordance with some embodiments. The circuit **700** in FIG. 7D includes a two-inputs NAND gate **710** and a three-inputs NOR gate **720**. The NAND gate **710** are formed from four transistors **pA1**, **nA1**, **pA2**, and **nA2** in FIG. 7C. The NOR gate **720** are formed from six transistors **pZN**, **nZN**, **pA3**, **nA3**, **pA4**, and **nA4** in FIG. 7C. The NAND gate **710** receives a digital signal at each of the two inputs **A1** and **A2**, and generates an output signal **ZN-A1**. The NOR gate **720** receives, at one of the three inputs, the output signal **ZN-A1** from the output terminal of the NAND gate **710**. The NOR gate **720** also receives additional digital signals at the other two inputs **A3** and **A4**.

[0085] In FIG. 7C, the horizontal routing tracks **A1**, **A2**, and **742** carry signals with the first phase $\Phi_{\text{sub.}+}$. The backside routing track **762** carry signals with the second phase $\Phi_{\text{sub.}-}$ that is opposite to the first phase $\Phi_{\text{sub.}-}$. In FIGS. 7A-7C, because the signal at the output of the NAND gate **710** with the second phase $\Phi_{\text{sub.}-}$ is carried by the backside routing track **762**, the capacitive coupling between the output of the NAND gate **710** and the inputs **A1** and **A2** of the NAND gate **710** reduced, as compared with some of the alternative designs in which some of the signals having opposite phase $\Phi_{\text{sub.}+}$ and $\Phi_{\text{sub.}-}$ are carried by adjacent routing tracks on a same metal layer. Consequently, the speed and the power consumption of the logic-gates combo circuit **700** are improved over some of the alternative designs.

[0086] FIGS. 8A-8B are partial layout diagrams of a Scan D Flip-flop (SDF) circuit **800**, in accordance with some embodiments. In FIG. 8A, elements formed on the front side of the substrate are shown in corresponding layout patterns. In FIG. 8B, the backside routing track and the backside via connectors formed on the back side of the substrate are depicted with layout patterns superimposed on the layout patterns in FIG. 8A. FIG. 8C and FIG. 9A are circuit diagrams of the SDF circuit **800** formed by the layout diagrams in FIGS. 8A-8B, in accordance with some embodiments. The circuit diagram in FIG. 8C closely tracks the physical locations of various elements (such as, the transistors, the routing tracks, and via connectors) in the layout diagrams in

FIGS. 8A-8B, while the circuit diagram in FIG. 9A groups the transistors in FIG. 8C into various functional blocks.

[0087] FIG. 9B is a circuit diagram of the SDF circuit **800** represented in functional blocks, in accordance with some embodiments. In FIG. 9B, the SDF circuit **800** includes a two-input multiplexer **910**, a master latch **920**, a transmission gate **930**, a slave latch **940**, and an inverter **950**. The two-input multiplexer **910** receives a data signal D at a first input **911** and a scan input signal SI at a second input **912**. Each of the two-input multiplexer **910**, the master latch **920**, and the slave latch **940** is clocked by clock signals synchronized to the clock signal CP. Depending upon the logical levels of the selection enable signal SE, either the data signal D or the scan input signal SI is generated as an inverted signal at the output **919** of the two-input multiplexer **910**. In some embodiments, the inverse of the data signal is generated at the output **919** when the selection enable signal SE is at the logic HIGH, and the inverse of the scan input signal SI is generated at the output **919** when the selection enable signal SE is at the logic LOW. The output **919** of the two-input multiplexer **910** is connected to the input of the master latch **920**. The transmission gate **930** is connected between the master latch **920** and the slave latch **940**. The output of the slave latch **940** is connected to the input of the inverter **950**. The output of the SDF circuit **800** is provided by the output of the inverter **950**.

[0088] In FIG. 8A, various elements for forming the SDF circuit **800** are specified by the corresponding layout patterns. The elements formed on the front side of the substrate and specified by the layout patterns include the active zones, the gate-strips, the conductive segments, the horizontal routing tracks, the power rails, and the via connectors. The gate-strips gSI, gSEB, gD, and gSE overlaps the p-type active zone **82p** and correspondingly form the gate terminals of the p-type transistors pSI, pSEB, pD, and pSE (as shown in FIG. 8C). The gate-strips gSI, gSEB, gD, and gSE overlaps the n-type active zone **82n** and correspondingly form the gate terminals of the n-type transistors nSI, nSEB, nD, and nSE (as shown in FIG. 8C). The gate-strips gQB, gSL_a, and gSE overlaps the p-type active zone **80p** and correspondingly form the gate terminals of the p-type transistors pQB, pSL_a, and pSE0 (as shown in FIG. 8C). The gate-strips gQB, gSL_a, and gSE overlaps the n-type active zone **80n** and correspondingly form the gate terminals of the n-type transistors nQB, nSL_a, and nSE0 (as shown in FIG. 8C). A poly-cut pattern **894** specifies a first disconnection gap between the gate-strips gSI and the gate-strips gQB and a second disconnection gap between the gate-strips gSEB and gSL_a. During device fabrication, in some embodiments, the gate-strips gSI and the gate-strips gQB are physically disconnected from each other by removing a gate-strip section as specified by the physical disconnection gap in the layout design, and the gate-strips gSI and the gate-strips gQB are similarly disconnected from each other. The poly-cut pattern **894** also specifies a third disconnection gap between the gate-strip gD and a vertically dummy gate-strip.

[0089] In FIG. 8A, the gate-strip gSL_bx overlaps the p-type active zone **80p** and the n-type active zone **80n**, forming correspondingly the gate terminals of the p-type transistors pSL_bx and the n-type transistors nSL_bx (as shown in FIG. 8C). A poly-cut pattern **895** specifies a disconnection gap between the gate-strip gSL_bx and a vertically dummy gate-strip.

[0090] In FIG. 8A, the gate-strips gpCK14, gpCK23, gML_b, and gCKb0 overlaps the p-type active zone **82p** and correspondingly form the gate terminals of the p-type transistors pCKbb1, pCKb2, pML_b, and pCKb0 (as shown in FIG. 8C). The gate-strips gnCKb1, gnCKbb2, gML_b, and gCKb0 overlaps the n-type active zone **82n** and correspondingly form the gate terminals of the n-type transistors nCKb1, nCKbb2, nML_b, and nCKb0 (as shown in FIG. 8C). The gate-strips gpCK14, gpCK23, gML_ax, and gCP overlaps the p-type active zone **80p** and correspondingly form the gate terminals of the p-type transistors pCKbb4, pCKb3, pML_ax, and pCP (as shown in FIG. 8C). The gate-strips gnCKb4, gnCKbb3, gML_ax, and gCP overlaps the n-type active zone **80n** and correspondingly form the gate terminals of the n-type transistors nCKb4, nCKbb3, nML_ax, and nCP (as shown in FIG. 8C). A poly-cut pattern **896** specifies a first disconnection gap between

the gate-strips gML_b and gML_ax and a second disconnection gap between the gate-strips gCKb0 and gCP. A poly-cut pattern **891** specifies a first disconnection gap between the gate-strips gnCKb1 and gpCK14 and a second disconnection gap between the gate-strips gnCKbb2 and gpCK23. A poly-cut pattern **892** specifies a first disconnection gap between the gate-strips gpCK14 and gnCKb4 and a second disconnection gap between the gate-strips gpCK23 and gnCKbb3.

[0091] In FIG. **8C** and FIG. **9A**, five p-type transistors (pSI, pSEB, pSE, pD, and pCKbb1) and five n-type transistors (nSI, nSE, nSEB, nD, and nCKb1) are used for forming the two-input multiplexer **910** (as shown in FIG. **9B**). The p-type transistor pML_ax and the n-type transistor nML_ax form an inverter **922** in the master latch **920**. Two p-type transistors (pL_b and pCKb2) and two n-type transistors (nML_b and nCKbb2) form a clocked inverter **924** in the master latch **920**. The p-type transistor pCKb3 and the n-type transistor nCKbb3 form the transmission gate **930**. The p-type transistor pSL_a and the n-type transistor nSL_a form an inverter **942** in the slave latch **920**. Two p-type transistors (pSL_bx and pCKbb4) and two n-type transistors (nSL_bx and nCKb4) form a clocked inverter **944** in the master latch **920**. The p-type transistor pQB and the n-type transistor nQB form the inverter **950**.

[0092] In FIG. **8C** and FIG. **9A**, the p-type transistor pSE0 and the n-type transistor nSE0 form an inverter **970** for generating an inverted selection enable signal SEB from the selection enable signal SE. The selection enable signal SE is coupled to the gate terminals of the p-type transistor pSE and the n-type transistor nSE. The p-type transistor pCP and the n-type transistor nCP form an inverter **980** for generating an inverted clock signal ckb from the clock signal CP. The p-type transistor pCKb0 and the n-type transistor nCK b0 form an inverter **990** for generating a clock signal ckbb from the inverted clock signal ckb. The inverted clock signal ckb is couple to the gate terminals of the p-type transistors pCKb2 and pCKb3 and the gate terminals of the n-type transistors nCKb1 and nCKb4. The clock signal ckbb is couple to the gate terminals of the p-type transistors pCKbb1 and pCKbb4 and the gate terminals of the n-type transistors nCKbb2 and nCKbb3.

[0093] In FIG. **8C**, various connections between the terminals of the transistors are formed from one or more of the horizontal routing tracks, the backside routing tracks, the via connectors, and/or the vertical routing tracks. The type of the via connectors include the front side via connectors VG and VD which connect the horizontal routing tracks with the terminals of the transistors, the backside via connectors VB and VBd which connect the backside routing tracks with the terminals of the transistors, and the front side via connectors V0 which connect the vertical routing tracks with the horizontal routing tracks.

[0094] The layout patterns of the horizontal routing tracks are depicted in FIG. **8A**. In FIG. **8A** and FIG. **8C**, the SDF circuit **800** includes horizontal routing tracks h_dSI, CKb1, CKbb2, CKb0, SI, ML_b, SEB, D, CKbb1, SE, CKb, Q, SL_a, hML_b, hSEB, CKb4, CKbb3, and CP. The layout positions of the front side via connectors VG and VD in FIG. **8A**, which are not explicitly shown, may be determined from the needed connections provided by the via connectors VG and VD in FIG. **8C**, because a connection between a chosen horizontal routing track and a chosen terminal of a transistor in FIG. **8C** implies a front side via connector VG or VD in FIG. **8A** at the intersection between the chosen horizontal routing track and the chosen terminal.

[0095] The layout patterns of the backside routing tracks are depicted in FIG. **8B**. In FIG. **8B** and FIG. **8C**, the SDF circuit **800** includes the backside routing tracks n01, n02, ML_ax, and SL_bx. The backside routing track n01 connects the source/drain terminals of the transistor nD and nSE with the source/drain terminal of the transistor nCKb1 through the backside via connectors VBd. The backside routing track n02 connects the source/drain terminals of the transistor pD and pSEB with the source/drain terminal of the transistor pCKbb1 through the backside via connectors VBd. The backside routing track ML_ax is connect to the gate terminals of the transistors pML_ax and nML_ax through the backside via connector VB. The backside routing track ML_ax is connect to the source/drain terminals of the transistors pCKbb1, nCKb1, pCKb2, and nCKbb2 through the backside via connectors VBd, The backside routing track SL_bx is connect to the gate terminals of

the transistors pSL_bx and nSL_bx through the backside via connector VB. The backside routing track SLbx is connect to the gate terminals of the transistors pQB and nQB through the backside via connector VB. The backside routing track SLbx is connect to the source/drain terminals of the transistors pSL_a and nSL_a through the backside via connectors VBd,

[0096] In FIG. 8C, the SDF circuit **800** includes the vertical routing tracks vSI, vQ, vSEB, vD, vCKb, vCKbb, vML_b, vCP, and vCKb0. The vertical routing track vSEB connects the horizontal routing tracks SEB and hSEB through the front side via connectors V0. The vertical routing track vCKb connects the horizontal routing tracks CKb1, CKb, and CKb4 through the front side via connectors V0. The vertical routing track vCKbb connects the horizontal routing tracks CKbb2, CKbb1 and CKbb3 through the front side via connectors V0. The vertical routing track vML_b connects the horizontal routing tracks ML_b and hML_b through the front side via connectors V0. [0097] In FIG. 8C, the vertical routing track vSI connects the horizontal routing track SI through the front side via connector V0. The vertical routing track vQ connects the horizontal routing track Q through the front side via connector V0. The vertical routing track vD connects the horizontal routing track D through the front side via connector V0. The vertical routing track vCP connects the horizontal routing track SI through the front side via connector CP. The vertical routing tracks vD, vQ, vSI, and vCP provides input pins correspondingly for the input data signal D, the output signal Q, the scan input signal SI, and the clock signal CP.

[0098] As shown in FIG. 9A, when the input data signal D has a first phase $\Phi+$, both the signal at the connection node n01 and the signal at the connection node n02 has a second phase $\Phi-$ that is opposite to the first phase $\Phi+$. The signal at the connection node m1_ax, which is between the output of the two-input multiplexer 910 and the input of the mater latch 920, has the second phase $\Phi-$. The signal at the connection node mI_b, which is between the output of the mater latch 920 and the input of the transmission gate 930, has the first phase $\Phi+$. The signal at the connection node sI_a, which is between the output of transmission gate 930 and the input of the slave latch 940, has the first phase $\Phi+$. The signal at the connection node sI_bx, which is between the output of the slave latch 940 and the input of the inverter 950, has the second phase $\Phi-$. The signal Q at the output of the inverter 950 has the first phase $\Phi+$.

[0099] In the layout design of the SDF circuit **800**, when adjacent routing tracks on a same metal layer (such as the metal layer M0) do not carry signals with the opposite phase, the speed and the power consumption of the SDF circuit **800** will be improved over some of the alternative designs which have capacitive couplings due to opposite phase signals carried by adjacent routing tracks on a same metal layer. A SDF circuit **800** based on the layout design of in FIGS. 8A-8B will have improved speed and the improved power consumption over some of the alternative designs. As shown in FIG. 8D, signals with the first phase $\Phi_{\text{sub.}+}$ are carried by the horizontal routing tracks D, MLb, hML_b, Q, and SL_a the front side of the substrate, while signals with the second phase $\Phi_{\text{sub.}-}$ are carried by the backside routing tracks n01, n02, ML_ax, and SL_bx on the backside of the substrate.

[0100] FIG. 10 is a flow chart showing a method **1000** of fabricating the backside routing tracks and backside via connectors, in accordance with some embodiments. Examples of the backside routing tracks and backside via connectors fabricated with the process **1000** include the backside routing track (e.g., 162) and the backside via connectors (e.g., VB and VBd) as shown in FIGS. 2A-2D. FIGS. 11A-11E are top views and cross-sectional views of intermediate device structures obtained when fabricating the backside routing tracks and the backside via connector VBd for connecting a backside routing track with a source/drain terminal of a transistor, in accordance with some embodiments. FIGS. 12A-12E are top views and cross-sectional views of intermediate device structures obtained when fabricating the backside routing tracks and the backside via connector VB for connecting a backside routing track with a gate terminal of a transistor, in accordance with some embodiments.

[0101] In the top views of FIGS. 11A-11E and FIGS. 12A-12E, the gate-strip 50p overlaps with the

p-type active zone **80p** and forms the gate terminal of a p-type transistor, and the gate-strip **50n** overlaps with the n-type active zone **80n** and forms the gate terminal of an n-type transistor. The device structures in FIGS. **11A-11E** when viewed along the cutting plan **Q1-Q1'** (as shown in the top view) are depicted correspondingly as the cross-sectional views in FIGS. **11A-11E**. The device structures in FIGS. **12A-12E** when viewed along the cutting plan **Q2-Q2'** (as shown in the top view) are depicted correspondingly as the cross-sectional views in FIGS. **12A-12E**.

[0102] In FIG. **10**, at process **1010**, the device structure for backside connections is prepared. At process **1010**, for preparing backside connections, active regions of the transistors in an integrated circuit, such as the channel regions and the source/drain regions, are isolated from each other by depositing dielectric materials onto the device structures from the backside of the integrated circuit. In some embodiments, the device structures prepared at the process **1010** includes the device structures of FIG. **11A** and FIG. **12A**.

[0103] In the cross-sectional view of FIG. **11A**, the source/drain region **60n** of the n-type transistor is isolated from the source/drain region **60p** of the p-type transistor by the isolation material **1110**. Dummy contact structures **1120n** and **1120p** contacting correspondingly the source/drain regions **60n** and **60p** are fabricated at the backside of the device structure. Dummy contact structures **1120n** and **1120p** are made of isolation materials. Hard masks **1130n** and **1130p** are fabricated covering correspondingly the dummy contact structures **1120n** and **1120p**. The isolation material **1110** in areas between the dummy contact structures **1120n** and **1120p** are recessed to a level as indicated by the surface **1112** of the isolation material **1110**.

[0104] In the cross-sectional view of FIG. **12A**, the channel region **70n** of the n-type transistor is isolated from the channel region **70p** of the p-type transistor by the isolation material **1215**. Dummy contact structures **1220n** and **1220p** contacting correspondingly the channel regions **70n** and **70p** are fabricated at the backside of the device structure. Dummy contact structures **1220n** and **1220p** are made of isolation materials. Hard masks **1230n** and **1230p** are fabricated covering correspondingly the dummy contact structures **1220n** and **1220p**. The isolation material **1215** in areas between the dummy contact structures **1220n** and **1220p** are recessed to a level as indicated by the surface **1212** of the isolation material **1215**.

[0105] In FIG. **10**, at process **1020**, conformal isolation material is deposited at the back of the device structure prepared at process **1010**. In FIG. **11B**, the conformal isolation material **1140** deposited at process **1020** covers the exposed surfaces of the hard masks **1130n** and **1130p**, the sidewalls of the dummy contact structures **1120n** and **1120p**, and the recessed surface **1112** of the isolation material **1110**. In FIG. **12B**, the conformal isolation material **1240** deposited at process **1020** covers the exposed surfaces of the hard masks **1230n** and **1230p**, the sidewalls of the dummy contact structures **1220n** and **1220p**, and the recessed surface **1212** of the isolation material **1215**.

[0106] After the process **1020**, a layer of isolation material is deposited at process **1030** and covers the surfaces of the conformal isolation material. In FIG. **11B**, the layer of isolation material **1172** covers the conformal isolation material **1140**. In FIG. **12B**, the layer of isolation material **1272** covers the conformal isolation material **1240**.

[0107] Then, at process **1040**, the conformal isolation material at selected locations is removed. The selected locations include portions of the sidewalls of the dummy contact structures. In FIG. **11C** and FIG. **12C**, the backside of the device structure is covered with a layer of photoresist (e.g., **1150** or **1250**), and the photoresist in a window area (e.g., **1155** or **1255**) as defined by a photomask is removed by photolithography techniques. In FIG. **11C**, the window area **1155** defines the location of a backside routing track for connecting with the source/drain region **60n** of the n-type transistor through a backside via connector. In FIG. **12C**, the window area **1155** defines the location of a backside routing track for connecting with the channel region **70n** of the n-type transistor through a backside via connector. During process **1040**, after the window areas in the photoresist layer for specifying the window area (e.g., **1155** or **1255**) are generated, materials exposed within the window areas of the photoresist layer are removed with etching processes. In FIG. **11C**, the

conformal isolation material at the selected portion **1122n** of a sidewall on the dummy contact structure **1120n** is removed by the etching processes. In FIG. **12C**, the conformal isolation material at the selected portion **1222n** of a sidewall on the dummy contact structure **1220n** is removed by the etching processes. In FIG. **11C** and FIG. **12C**, the layer of photoresist (e.g., **1150** or **1250**) is striped off after the conformal isolation material at the selected portions of the sidewalls of the dummy contact structures is removed.

[0108] Next, at process **1050**, backside routing tracks in a metal layer at the backside of the integrated circuit are fabricated. In FIG. **11D**, the metal layer **1175** is deposited overlying the isolation material **1172**, and the backside routing tracks (e.g., **1162**, **1164**, and **1166**) are formed. After the backside routing tracks are formed, another layer of isolation material **1174** is deposited covering the backside routing tracks (e.g., **1162**, **1164**, and **1166**). In FIG. **12D**, the metal layer **1275** is deposited overlying the isolation material **1272**, and the backside routing tracks (e.g., **1262**, **1264**, and **1266**) are formed. After the backside routing tracks are formed, another layer of isolation material **1274** is deposited covering the backside routing tracks (e.g., **1262**, **1264**, and **1266**).

[0109] Next, at process **1060**, backside via connectors are fabricated. In FIG. **11E**, the dummy structure **1120n** and the associated mask **1130n** are removed to expose a surface **62n** of the source/drain region **60n** of the n-type transistor. Then, conductive material such as metal is deposited to form the backside via connector **1180n**. The backside via connector **1180n** forms conductive contacts with both the backside routing track **1164** and the source/drain region **60n** of the n-type transistor. The backside via connector **1180n** is a backside via connector VBd for connecting a source/drain region of a transistor with a backside routing track. In FIG. **12E**, the dummy structure **1220n** and the associated mask **1230n** are removed to expose a surface **72n** of the channel region **70n** of the n-type transistor. Then, conductive material such as metal is deposited to form the backside via connector **1280n**. The backside via connector **1280n** forms conductive contacts with both the backside routing track **1264** and the channel region **70n** of the n-type transistor. The backside via connector **1280n** is a backside via connector VB for connecting a gate terminal of a transistor with a backside routing track. In FIG. **11E** and FIG. **12E**, after the backside via connectors (e.g., **1180n** or **1280n**) are formed, protective covers (e.g., **1132n** or **1232n**) are formed by depositing isolation materials over the backside via connectors.

[0110] In addition to the method **1000** in FIG. **10** for fabricating the backside routing tracks and backside via connectors. There are also other embodiments of the method for fabricating the backside routing tracks and backside via connectors.

[0111] FIG. **13** is a flowchart of a method **1300** of generating a layout design of an integrated circuit in accordance with some embodiments. It is understood that additional operations may be performed before, during, and/or after the method **1300** depicted in FIG. **13**, and that some other processes may only be briefly described herein. In some embodiments, the method **1300** is usable to generate one or more layout designs, such as the layout designs in FIGS. **1A-1B**, FIGS. **3A-3B**, FIGS. **4A-4C**, FIGS. **6A-6C**, FIGS. **7A-7B**, or FIGS. **8A-8B**. In some embodiments, the method **1300** is usable to form integrated circuits having similar structural relationships as one or more of the semiconductor structures formed based on the layout designs in FIGS. **1A-1B**, FIGS. **3A-3B**, FIGS. **4A-4C**, FIGS. **6A-6C**, FIGS. **7A-7B**, or FIGS. **8A-8B**. In some embodiments, the method **1300** is usable to form integrated circuits having similar structural relationships as one or more of the semiconductor structures in FIGS. **2A-2D**. In some embodiments, method **1300** is performed by a processing device (e.g., processor **1402** in FIG. **14**) configured to execute instructions for generating one or more layout designs, such as the layout designs in FIGS. **1A-1B**, FIGS. **3A-3B**, FIGS. **4A-4C**, FIGS. **6A-6C**, FIGS. **7A-7B**, or FIGS. **8A-8B**.

[0112] In operation **1310** of method **1300**, active zone patterns are generated. The active zone patterns generated include a first-type active zone pattern and a second-type active zone pattern. In the example layout designs of FIGS. **1A-1B**, FIGS. **3A-3B**, FIGS. **4A-4C**, FIGS. **6A-6C**, and FIGS. **7A-7B**, each of the p-type active zone **80p** and the n-type active zone **80n** is specified by a

corresponding p-type active zone pattern or a corresponding n-type active zone pattern. In the example layout design of FIGS. **8A-8B**, each of the p-type active zones **80p** and **82p** is specified by a corresponding p-type active zone pattern, and each of the n-type active zones **80n** and **82n** is specified by a corresponding n-type active zone pattern. The flow proceeds to operation **1320**.

[0113] In operation **1320** of method **1300**, gate-strip patterns are generated. In the example layout designs of FIGS. **1A-1B**, FIGS. **3A-3B**, and FIGS. **4A-4C**, each of the gate-strips **151**, **152**, **153**, **gB2**, **gB1**, **gA1**, and **gA2** is specified by a corresponding gate-strip pattern. In the example layout design of and FIGS. **6A-6C**, each of the gate-strips **gS1**, **gl1**, **gI0**, **gS0**, **656**, **g03**, **g04**, **gS2**, **gI2**, **gI3**, and **gS3** is specified by a corresponding gate-strip pattern. In the example layout design of and FIGS. **7A-7B**, each of the gate-strips pattern **gA1**, **gA2**, **g2N**, **gA3**, and **gA4** is specified by a corresponding gate-strip pattern. In the example layout design of FIGS. **8A-8B**, each of the gate-strips **gS1**, **gSEB**, **gD**, **gSE**, **gnCKb1**, **gnCKbb2**, **gML_b**, **gCKb0**, **gQB**, **gSL_a**, **gSE**, **gSL_bx**, **gnCKb4**, **gnCKbb3**, **gML_ax**, and **gCP** is specified by a corresponding gate-strip pattern. The flow proceeds to operation **1330**.

[0114] In operation **1330** of method **1300**, conductive segment patterns are generated. In the example layout design of FIGS. **1A-1B**, each of the conductive segments **132**, **134p**, **134n**, **136**, **138p**, and **138n** is specified by a corresponding conductive segment pattern. In the example layout designs of FIGS. **3A-3B** and FIGS. **4A-4C**, each of the conductive segments **332p**, **332n**, **334p**, **334n**, **335p**, **335n**, **336p**, **336n**, **338p**, and **338n** is specified by a corresponding conductive segment pattern. In the example layout designs of FIGS. **6A-6C**, FIGS. **7A-7B**, or FIGS. **8A-8B**, each of the conductive segments is similarly specified by a corresponding conductive segment pattern. The flow proceeds to operation **1340**.

[0115] In operation **1340** of method **1300**, horizontal routing track patterns are generated. In the example layout designs of FIGS. **1A-1B**, FIGS. **3A-3B** and FIGS. **4A-4C**, each of the horizontal routing tracks **142**, **144**, **146**, **B1**, **ZN**, **B2**, **A1**, **A2**, **442**, and **448** is specified by a corresponding horizontal routing track pattern. In the example layout design of FIGS. **6A-6C**, each of the horizontal routing tracks **n01**, **642**, **n02**, **S1**, **S0**, **S2**, **S3**, **11**, **10**, **648**, **12**, and **13** is specified by a corresponding horizontal routing track pattern. In the example layout design of FIGS. **7A-7B**, each of the horizontal routing tracks **A2**, **A3**, **A4**, **A1**, and **742** is specified by a corresponding horizontal routing track pattern. In the example layout design of FIGS. **8A-8B**, each of the horizontal routing tracks **h_dSI**, **CKb1**, **CKbb2**, **CKb0**, **SI**, **ML_b**, **SEB**, **D**, **CKbb1**, **SE**, **CKb**, **Q**, **SL_a**, **hML_b**, **hSEB**, **CKb4**, **CKbb3**, and **CP** is specified by a corresponding horizontal routing track pattern. In some embodiments, power rail patterns are also generated in operation **1340**. In the example layout designs of FIGS. **1A-1B**, FIGS. **3A-3B**, FIGS. **4A-4C**, FIGS. **6A-6C**, FIGS. **7A-7B**, and FIGS. **8A-8B**, each of the power rails **122** and **124** is specified by a corresponding power rail pattern. The flow proceeds to operation **1350**.

[0116] In operation **1350** of method **1300**, front side via connector patterns are generated. In the example layout designs of FIGS. **1A-1B**, FIGS. **3A-3B**, FIGS. **4A-4C**, FIGS. **6A-6C**, and FIGS. **7A-7B**, each of the side via connectors **VG** and **VD** is specified by a corresponding front side via connector pattern. In the example layout design of FIGS. **8A-8B**, the positions of the front side via connector pattern for specifying each of the front side via connectors that are needed in the layout design can be determined from the circuit diagram in FIG. **8C**. The flow proceeds to operation **1360**.

[0117] In operation **1360** of method **1300**, one or more backside routing track patterns are generated. In the example layout designs of FIGS. **1A-1B**, FIGS. **3A-3B**, FIGS. **4A-4C**, FIGS. **6A-6C**, FIGS. **7A-7B**, and FIGS. **8A-8B**, each of the backside routing tracks **162**, **362**, **364**, **n03**, **n04**, and **762** is specified by a corresponding backside routing track pattern. In the example layout design of FIGS. **8A-8B**, each of the backside routing tracks **n01**, **n02**, **ML_ax**, and **SL_bx** is specified by a corresponding backside routing track pattern. The flow proceeds to operation **1370**.

[0118] In operation **1370** of method **1300**, backside via connector patterns are generated. In the

example layout designs of FIGS. 1A-1B, FIGS. 3A-3B, FIGS. 4A-4C, FIGS. 6A-6C, FIGS. 7A-7B, and FIGS. 8A-8B, each of the backside via connectors VB and VBd is specified by a corresponding backside via connector pattern. The flow proceeds to operation **1380**.

[0119] In operation **1380** of method **1300**, vertical routing track patterns are generated. In the example layout designs of FIGS. 4A-4C and FIGS. 6A-6C, each of the vertical routing tracks **472** and **672** is specified by a corresponding vertical routing track pattern. In the example layout design of FIGS. 8A-8C, the positions of the vertical routing track patterns for specifying various vertical routing tracks that are needed in the layout design can be determined from the circuit diagram in FIG. 8C. When the vertical routing track patterns are included in the layout design of FIGS. 8A-8B, each of the vertical routing tracks vSI, vQ, vSEB, vD, vSE, vCKb, vCK bb, vML_b, vCP, and vCKb0 will be specified by a corresponding vertical routing track pattern. In some embodiments, the layout patterns for specifying the front side via connectors VO between the second metal layer M1 and the first metal layer M0 are also generated in operation **1380**. A front side via connector VO is a via connector that connects a vertical routing track in the second metal layer M1 with a horizontal routing track in the first metal layer M0.

[0120] FIG. 14 is a block diagram of an electronic design automation (EDA) system **1400** in accordance with some embodiments.

[0121] In some embodiments, EDA system **1400** is a general purpose computing device including a hardware processor **1402** and a non-transitory, computer-readable storage medium (storage medium **1404**). Storage medium **1404**, amongst other things, is encoded with, i.e., stores, computer program code **1406**, i.e., a set of computer-executable instructions (instructions). Execution of computer program code **1406** by hardware processor **1402** represents (at least in part) an EDA tool which implements a portion or all of, e.g., the methods described herein in accordance with one or more (hereinafter, the noted processes and/or methods).

[0122] Hardware processor **1402** is electrically coupled to computer-readable storage medium **1404** via a bus **1408**. Hardware processor **1402** is also electrically coupled to an I/O interface **1410** by bus **1408**. A network interface **1412** is also electrically connected to hardware processor **1402** via bus **1408**. Network interface **1412** is connected to a network **1414**, so that hardware processor **1402** and computer-readable storage medium **1404** are capable of connecting to external elements via network **1414**. Hardware processor **1402** is configured to execute computer program code **1406** encoded in computer-readable storage medium **1404** in order to cause EDA system **1400** to be usable for performing a portion or all of the noted processes and/or methods. In one or more embodiments, hardware processor **1402** is a central processing unit (CPU), a multi-processor, a distributed processing system, an application specific integrated circuit (ASIC), and/or a suitable processing unit.

[0123] In one or more embodiments, computer-readable storage medium **1404** is an electronic, magnetic, optical, electromagnetic, infrared, and/or a semiconductor system (or apparatus or device). For example, computer-readable storage medium **1404** includes a semiconductor or solid-state memory, a magnetic tape, a removable computer diskette, a random access memory (RAM), a read-only memory (ROM), a rigid magnetic disk, and/or an optical disk. In one or more embodiments using optical disks, computer-readable storage medium **1404** includes a compact disk-read only memory (CD-ROM), a compact disk-read/write (CD-R/W), and/or a digital video disc (DVD).

[0124] In one or more embodiments, storage medium **1404** stores computer program code **1406** configured to cause EDA system **1400** (where such execution represents (at least in part) the EDA tool) to be usable for performing a portion or all of the noted processes and/or methods. In one or more embodiments, storage medium **1404** also stores information which facilitates performing a portion or all of the noted processes and/or methods. In one or more embodiments, storage medium **1404** stores a library **1407** of standard cells including such standard cells as disclosed herein.

[0125] EDA system **1400** includes I/O interface **1410**. I/O interface **1410** is coupled to external

circuitry. In one or more embodiments, I/O interface **1410** includes a keyboard, keypad, mouse, trackball, trackpad, touchscreen, and/or cursor direction keys for communicating information and commands to hardware processor **1402**.

[0126] EDA system **1400** also includes network interface **1412** coupled to hardware processor **1402**. Network interface **1412** allows EDA system **1400** to communicate with network **1414**, to which one or more other computer systems are connected. Network interface **1412** includes wireless network interfaces such as BLUETOOTH, WIFI, WIMAX, GPRS, or WCDMA; or wired network interfaces such as ETHERNET, USB, or IEEE-1364. In one or more embodiments, a portion or all of noted processes and/or methods, is implemented in two or more EDA systems **1400**.

[0127] EDA system **1400** is configured to receive information through I/O interface **1410**. The information received through I/O interface **1410** includes one or more of instructions, data, design rules, libraries of standard cells, and/or other parameters for processing by hardware processor **1402**. The information is transferred to hardware processor **1402** via bus **1408**. EDA system **1400** is configured to receive information related to a UI through I/O interface **1410**. The information is stored in computer-readable medium **1404** as user interface (UI) **1452**.

[0128] In some embodiments, a portion or all of the noted processes and/or methods is implemented as a standalone software application for execution by a processor. In some embodiments, a portion or all of the noted processes and/or methods is implemented as a software application that is a part of an additional software application. In some embodiments, a portion or all of the noted processes and/or methods is implemented as a plug-in to a software application. In some embodiments, at least one of the noted processes and/or methods is implemented as a software application that is a portion of an EDA tool. In some embodiments, a portion or all of the noted processes and/or methods is implemented as a software application that is used by EDA system **1400**. In some embodiments, a layout diagram which includes standard cells is generated using a tool such as VIRTUOSO® available from CADENCE DESIGN SYSTEMS, Inc., or another suitable layout generating tool.

[0129] In some embodiments, the processes are realized as functions of a program stored in a non-transitory computer readable recording medium. Examples of a non-transitory computer readable recording medium include, but are not limited to, external/removable and/or internal/built-in storage or memory unit, e.g., one or more of an optical disk, such as a DVD, a magnetic disk, such as a hard disk, a semiconductor memory, such as a ROM, a RAM, a memory card, and the like.

[0130] FIG. **15** is a block diagram of an integrated circuit (IC) manufacturing system **1500**, and an IC manufacturing flow associated therewith, in accordance with some embodiments. In some embodiments, based on a layout diagram, at least one of (A) one or more semiconductor masks or (B) at least one component in a layer of a semiconductor integrated circuit is fabricated using IC manufacturing system **1500**.

[0131] In FIG. **15**, IC manufacturing system **1500** includes entities, such as a design house **1520**, a mask house **1530**, and an IC manufacturer/fabricator (“fab”) **1550**, that interact with one another in the design, development, and manufacturing cycles and/or services related to manufacturing an IC device **1560**. The entities in IC manufacturing system **1500** are connected by a communications network. In some embodiments, the communications network is a single network. In some embodiments, the communications network is a variety of different networks, such as an intranet and the Internet. The communications network includes wired and/or wireless communication channels. Each entity interacts with one or more of the other entities and provides services to and/or receives services from one or more of the other entities. In some embodiments, two or more of design house **1520**, mask house **1530**, and IC fab **1550** is owned by a single larger company. In some embodiments, two or more of design house **1520**, mask house **1530**, and IC fab **1550** coexist in a common facility and use common resources.

[0132] Design house (or design team) **1520** generates an IC design layout diagram **1522**. IC design

layout diagram **1522** includes various geometrical patterns designed for an IC device **1560**. The geometrical patterns correspond to patterns of metal, oxide, or semiconductor layers that make up the various components of IC device **1560** to be fabricated. The various layers combine to form various IC features. For example, a portion of IC design layout diagram **1522** includes various IC features, such as an active region, gate electrode, source and drain, metal lines or vias of an interlayer interconnection, and openings for bonding pads, to be formed in a semiconductor substrate (such as a silicon wafer) and various material layers disposed on the semiconductor substrate. Design house **1520** implements a proper design procedure to form IC design layout diagram **1522**. The design procedure includes one or more of logic design, physical design or place and route. IC design layout diagram **1522** is presented in one or more data files having information of the geometrical patterns. For example, IC design layout diagram **1522** can be expressed in a GDSII file format or DFII file format.

[0133] Mask house **1530** includes data preparation **1532** and mask fabrication **1544**. Mask house **1530** uses IC design layout diagram **1522** to manufacture one or more masks **1545** to be used for fabricating the various layers of IC device **1560** according to IC design layout diagram **1522**. Mask house **1530** performs mask data preparation **1532**, where IC design layout diagram **1522** is translated into a representative data file (“RDF”). Mask data preparation **1532** provides the RDF to mask fabrication **1544**. Mask fabrication **1544** includes a mask writer. A mask writer converts the RDF to an image on a substrate, such as a mask (reticle) **1545** or a semiconductor wafer **1553**. The design layout diagram **1522** is manipulated by mask data preparation **1532** to comply with particular characteristics of the mask writer and/or requirements of IC fab **1550**. In FIG. **15**, mask data preparation **1532** and mask fabrication **1544** are illustrated as separate elements. In some embodiments, mask data preparation **1532** and mask fabrication **1544** can be collectively referred to as mask data preparation.

[0134] In some embodiments, mask data preparation **1532** includes optical proximity correction (OPC) which uses lithography enhancement techniques to compensate for image errors, such as those that can arise from diffraction, interference, other process effects and the like. OPC adjusts IC design layout diagram **1522**. In some embodiments, mask data preparation **1532** includes further resolution enhancement techniques (RET), such as off-axis illumination, sub-resolution assist features, phase-shifting masks, other suitable techniques, and the like or combinations thereof. In some embodiments, inverse lithography technology (ILT) is also used, which treats OPC as an inverse imaging problem.

[0135] In some embodiments, mask data preparation **1532** includes a mask rule checker (MRC) that checks the IC design layout diagram **1522** that has undergone processes in OPC with a set of mask creation rules which contain certain geometric and/or connectivity restrictions to ensure sufficient margins, to account for variability in semiconductor manufacturing processes, and the like. In some embodiments, the MRC modifies the IC design layout diagram **1522** to compensate for limitations during mask fabrication **1544**, which may undo part of the modifications performed by OPC in order to meet mask creation rules.

[0136] In some embodiments, mask data preparation **1532** includes lithography process checking (LPC) that simulates processing that will be implemented by IC fab **1550** to fabricate IC device **1560**. LPC simulates this processing based on IC design layout diagram **1522** to create a simulated manufactured device, such as IC device **1560**. The processing parameters in LPC simulation can include parameters associated with various processes of the IC manufacturing cycle, parameters associated with tools used for manufacturing the IC, and/or other aspects of the manufacturing process. LPC takes into account various factors, such as aerial image contrast, depth of focus (“DOF”), mask error enhancement factor (“MEEF”), other suitable factors, and the like or combinations thereof. In some embodiments, after a simulated manufactured device has been created by LPC, if the simulated device is not close enough in shape to satisfy design rules, OPC and/or MRC are repeated to further refine IC design layout diagram **1522**.

[0137] It should be understood that the above description of mask data preparation **1532** has been simplified for the purposes of clarity. In some embodiments, data preparation **1532** includes additional features such as a logic operation (LOP) to modify the IC design layout diagram **1522** according to manufacturing rules. Additionally, the processes applied to IC design layout diagram **1522** during data preparation **1532** may be executed in a variety of different orders.

[0138] After mask data preparation **1532** and during mask fabrication **1544**, a mask **1545** or a group of masks **1545** are fabricated based on the modified IC design layout diagram **1522**. In some embodiments, mask fabrication **1544** includes performing one or more lithographic exposures based on IC design layout diagram **1522**. In some embodiments, an electron-beam (e-beam) or a mechanism of multiple e-beams is used to form a pattern on a mask (photomask or reticle) **1545** based on the modified IC design layout diagram **1522**. Mask **1545** can be formed in various technologies. In some embodiments, mask **1545** is formed using binary technology. In some embodiments, a mask pattern includes opaque regions and transparent regions. A radiation beam, such as an ultraviolet (UV) beam, used to expose the image sensitive material layer (e.g., photoresist) which has been coated on a wafer, is blocked by the opaque region and transmits through the transparent regions. In one example, a binary mask version of mask **1545** includes a transparent substrate (e.g., fused quartz) and an opaque material (e.g., chromium) coated in the opaque regions of the binary mask. In another example, mask **1545** is formed using a phase shift technology. In a phase shift mask (PSM) version of mask **1545**, various features in the pattern formed on the phase shift mask are configured to have proper phase difference to enhance the resolution and imaging quality. In various examples, the phase shift mask can be attenuated PSM or alternating PSM. The mask(s) generated by mask fabrication **1544** is used in a variety of processes. For example, such a mask(s) is used in an ion implantation process to form various doped regions in semiconductor wafer **1553**, in an etching process to form various etching regions in semiconductor wafer **1553**, and/or in other suitable processes.

[0139] IC fab **1550** includes wafer fabrication **1552**. IC fab **1550** is an IC fabrication business that includes one or more manufacturing facilities for the fabrication of a variety of different IC products. In some embodiments, IC fab **1550** is a semiconductor foundry. For example, there may be a manufacturing facility for the front end fabrication of a plurality of IC products (front-end-of-line (FEOL) fabrication), while a second manufacturing facility may provide the back end fabrication for the interconnection and packaging of the IC products (back-end-of-line (BEOL) fabrication), and a third manufacturing facility may provide other services for the foundry business.

[0140] IC fab **1550** uses mask(s) **1545** fabricated by mask house **1530** to fabricate IC device **1560**. Thus, IC fab **1550** at least indirectly uses IC design layout diagram **1522** to fabricate IC device **1560**. In some embodiments, semiconductor wafer **1553** is fabricated by IC fab **1550** using mask(s) **1545** to form IC device **1560**. In some embodiments, the IC fabrication includes performing one or more lithographic exposures based at least indirectly on IC design layout diagram **1522**.

Semiconductor wafer **1553** includes a silicon substrate or other proper substrate having material layers formed thereon. Semiconductor wafer **1553** further includes one or more of various doped regions, dielectric features, multilevel interconnects, and the like (formed at subsequent manufacturing steps).

[0141] Details regarding an integrated circuit (IC) manufacturing system (e.g., manufacturing system **1500** of FIG. **15**), and an IC manufacturing flow associated therewith are found, e.g., in U.S. Pat. No. 9,256,709, granted Feb. 9, 2016, U.S. Pre-Grant Publication No. 20150278429, published Oct. 1, 2015, U.S. Pre-Grant Publication No. 20140040838, published Feb. 6, 2014, and U.S. Pat. No. 7,260,442, granted Aug. 21, 2007, the entireties of each of which are hereby incorporated by reference.

[0142] An aspect of the present disclosure relates to an integrated circuit. The integrated circuit includes a horizontal routing track extending in a first direction as a one-dimensional horizontal routing track in a first metal layer, where the horizontal routing track is conductively connected to a

gate terminal of a first transistor without passing through a routing track in another metal layer. The circuit also includes a backside routing track extending in the first direction as a one-dimensional backside routing track in a backside metal layer, where the backside metal layer and the first metal layer are formed at opposite sides of a semiconductor substrate, where the backside routing track is conductively connected to either a source terminal or a drain terminal of the first transistor without passing through a routing track in another metal layer.

[0143] Another aspect of the present disclosure relates to an integrated circuit. The integrated circuit includes a horizontal routing track extending in a first direction as a one-dimensional horizontal routing track in a first metal layer, where the horizontal routing track is conductively connected to either a source terminal or a drain terminal of a first transistor without passing through a routing track in another metal layer. The circuit also includes a backside routing track extending in the first direction as a one-dimensional backside routing track in a backside metal layer, where the backside metal layer and the first metal layer are formed at opposite sides of a semiconductor substrate, where the backside routing track is conductively connected to a gate terminal of the first transistor without passing through a routing track in another metal layer.

[0144] Another aspect of the present disclosure relates to a method of fabricating an integrated circuit. The method includes fabricating a gate terminal of a first transistor. The method also includes fabricating a source terminal and a drain terminal of the first transistor, where each of the source terminal and the drain terminal is a channel connecting terminal. The method also includes fabricating a horizontal routing track conductively connected to a first one of the gate terminals or the channel connecting terminal of the first transistor through a front side via connector, where the horizontal routing track extends in a first direction in a first metal layer. The method also includes fabricating a backside routing track conductively connected to a second one of the gate terminals or the channel connecting terminal of the first transistor through a backside via connector, where the backside routing track extends in the first direction in a backside metal layer, and where the backside metal layer and the first metal layer are formed at opposite sides of a semiconductor substrate.

[0145] It will be readily seen by one of ordinary skill in the art that one or more of the disclosed embodiments fulfill one or more of the advantages set forth above. After reading the foregoing specification, one of ordinary skill will be able to affect various changes, substitutions of equivalents and various other embodiments as broadly disclosed herein. It is therefore intended that the protection granted hereon be limited only by the definition contained in the appended claims and equivalents thereof.

Claims

1. An integrated circuit comprising: a horizontal routing track extending in a first direction as a one-dimensional horizontal routing track in a first metal layer, wherein the horizontal routing track is conductively connected to a gate terminal of a first transistor without passing through a routing track in another metal layer; and a backside routing track extending in the first direction as a one-dimensional backside routing track in a backside metal layer, wherein the backside metal layer and the first metal layer are at opposite sides of a semiconductor substrate, wherein the backside routing track is conductively connected to either a source terminal or a drain terminal of the first transistor without passing through a routing track in another metal layer.
2. The integrated circuit of claim 1, wherein the first transistor has a channel region between the backside metal layer and the first metal layer.
3. The integrated circuit of claim 1, further comprising: a backside via connector passing through the semiconductor substrate and conductively connecting the backside routing track to the source terminal or the drain terminal of the first transistor.
4. The integrated circuit of claim 1, further comprising: a first gate-strip, extending in a second

direction perpendicular to the first direction, overlapping a channel region of the first transistor and forming the gate terminal of the first transistor; and a via connector connecting the horizontal routing track to the first gate-strip.

5. The integrated circuit of claim 1, further comprising: a conductive segment, extending in a second direction perpendicular to the first direction, overlapping a drain region of the first transistor and forming the drain terminal of the first transistor; and a backside via connector connecting the backside routing track to the conductive segment.

6. The integrated circuit of claim 1, wherein the first transistor, the horizontal routing track, and the backside routing track are within an AOI (“And-Or-Invertor”) logic cell, a multiplexer cell, a flip-flop cell, or a logic-gates combo cell.

7. The integrated circuit of claim 1, further comprising a second horizontal routing track adjacent to the horizontal routing track.

8. The integrated circuit of claim 7, and wherein the backside routing track is vertically between the horizontal routing track and the second horizontal routing track.

9. An integrated circuit comprising: a horizontal routing track extending in a first direction as a one-dimensional horizontal routing track in a first metal layer, wherein the horizontal routing track is conductively connected to either a source terminal or a drain terminal of a first transistor without passing through a routing track in another metal layer; and a backside routing track extending in the first direction as a one-dimensional backside routing track in a backside metal layer, wherein the backside metal layer and the first metal layer are formed at opposite sides of a semiconductor substrate, wherein the backside routing track is conductively connected to a gate terminal of the first transistor without passing through a routing track in another metal layer.

10. The integrated circuit of claim 9, wherein the first transistor has a channel region between the backside metal layer and the first metal layer.

11. The integrated circuit of claim 9, further comprising: a backside via connector passing through the semiconductor substrate and conductively connecting the backside routing track to the gate terminal of the first transistor.

12. The integrated circuit of claim 9, further comprising: a first gate-strip, extending in a second direction perpendicular to the first direction, overlapping a channel region of the first transistor and forming the gate terminal of the first transistor; and a backside via connector connecting the backside routing track to the first gate-strip.

13. The integrated circuit of claim 9, further comprising: a conductive segment, extending in a second direction perpendicular to the first direction, overlapping a drain region of the first transistor and forming the drain terminal of the first transistor; and a via connector connecting the horizontal routing track to the conductive segment.

14. The integrated circuit of claim 9, wherein the first transistor, the horizontal routing track, and the backside routing track are within an AOI logic cell, a multiplexer cell, a flip-flop cell, or a logic-gates combo cell.

15. The integrated circuit of claim 9, further comprising a second horizontal routing track adjacent to the horizontal routing track, wherein the backside routing track is vertically between the horizontal routing track and the second horizontal routing track.

16. A method of fabricating an integrated circuit, the method comprising: fabricating a gate terminal of a first transistor; fabricating a source terminal and a drain terminal of the first transistor, wherein each of the source terminal and the drain terminal is a channel connecting terminal; fabricating a horizontal routing track conductively connected to a first one of the gate terminal or the channel connecting terminal of the first transistor through a front side via connector, wherein the horizontal routing track extends in a first direction in a first metal layer; and fabricating a backside routing track conductively connected to a second one of the gate terminal or the channel connecting terminal of the first transistor through a backside via connector, wherein the backside routing track extends in the first direction in a backside metal layer, and wherein the backside metal

layer and the first metal layer are formed at opposite sides of a semiconductor substrate.

17. The method of claim 16, further comprising: forming a front side via connector connecting the horizontal routing track to the gate terminal of the first transistor; and forming a backside via connector connecting the backside routing track to the channel connecting terminal of the first transistor.

18. The method of claim 16, further comprising: fabricating the front side via connector connecting the horizontal routing track to the channel connecting terminal of the first transistor; and fabricating the backside via connector connecting the backside routing track to the gate terminal of the first transistor.

19. The method of claim 16, further comprising: fabricating gate-strips extending in a second direction perpendicular to a first direction, wherein a gate-strip overlaps an active zone extending in the first direction at a first intersection and forms a gate terminal of the first transistor; and fabricating the gate-strips in a layer between the backside metal layer and the first metal layer.

20. The method of claim 16, further comprising: fabricating the horizontal routing track, the backside routing track, a front side via connector, and a backside via connector as a part of a circuit including an AOI logic, a multiplexer, a flip-flop, or a logic-gates combo cell.
