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Zhao et al.

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(54) **ADAPTIVE OFF-TIME OR ON-TIME DC-DC CONVERTER**

(71) Applicant: **TEXAS INSTRUMENTS INCORPORATED**, Dallas, TX (US)

(72) Inventors: **Wei Zhao**, Shanghai (CN); **Jianzhang Xie**, Shanghai (CN)

(73) Assignee: **TEXAS INSTRUMENTS INCORPORATED**, Dallas, TX (US)

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H02M 3/158	(2006.01)
H02M 1/00	(2006.01)
H02M 1/08	(2006.01)

(52) **U.S. Cl.**

CPC ***H02M 1/08*** (2013.01); ***H02M 1/0003*** (2021.05); ***H02M 1/0041*** (2021.05); ***H02M 3/158*** (2013.01); *H02M 1/0025* (2021.05)

(58) **Field of Classification Search**

CPC H02M 3/156; H02M 3/157; H02M 3/158; H02M 1/08; H02M 1/0041; H02M 1/0003

See application file for complete search history.

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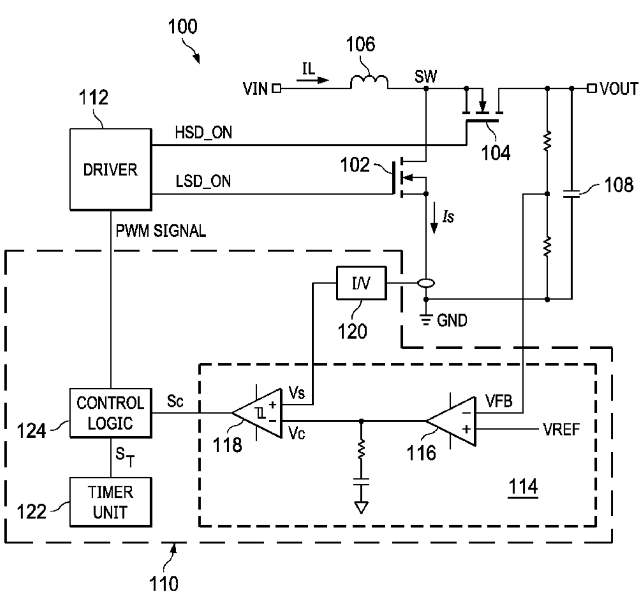
Primary Examiner — Alex Torres-Rivera
(74) *Attorney, Agent, or Firm* — Valerie M. Davis; Frank D. Cimino

(57) **ABSTRACT**

A converter system includes a first switch and a controller configured to switch the first switch between first and second states based on input and output voltages of the converter system. The controller includes: a timer unit including a first timer configured to determine a first duration based on a target switching frequency of the converter system; and a second timer configured to determine a second duration based on a predetermined duration equal to or greater than a minimum duration of the first state of the first switch and the input and output voltages; and a control logic unit configured to switch the first switch from the second state to the first state responsive to expiration of both the first and second durations.

17 Claims, 11 Drawing Sheets



Related U.S. Application Data

continuation of application No. PCT/CN2020/070110, filed on Jan. 2, 2020.

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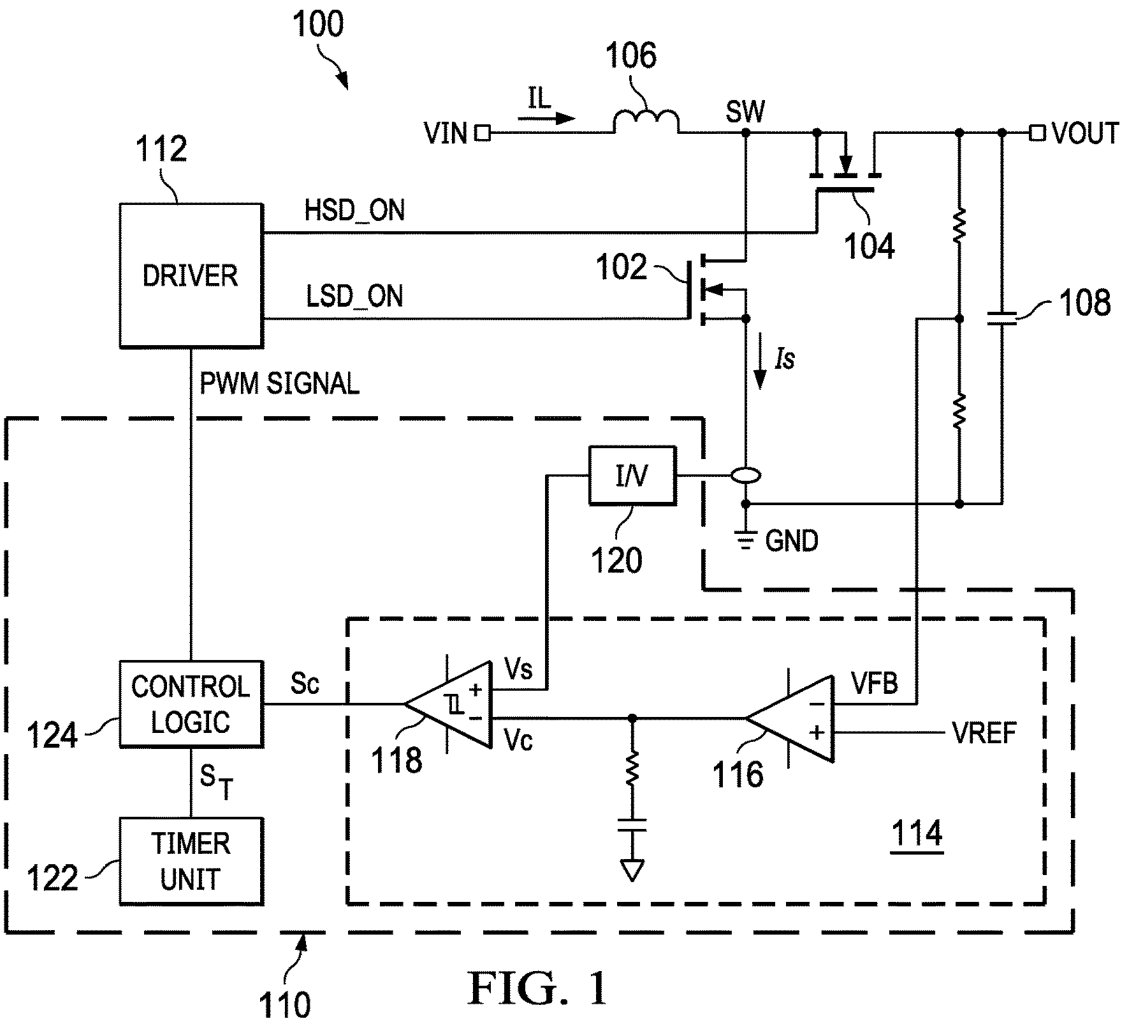


FIG. 1

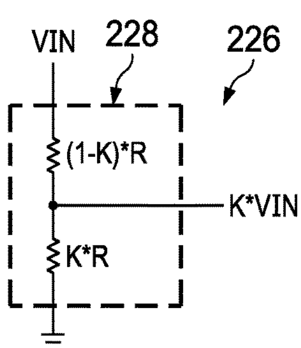


FIG. 2B

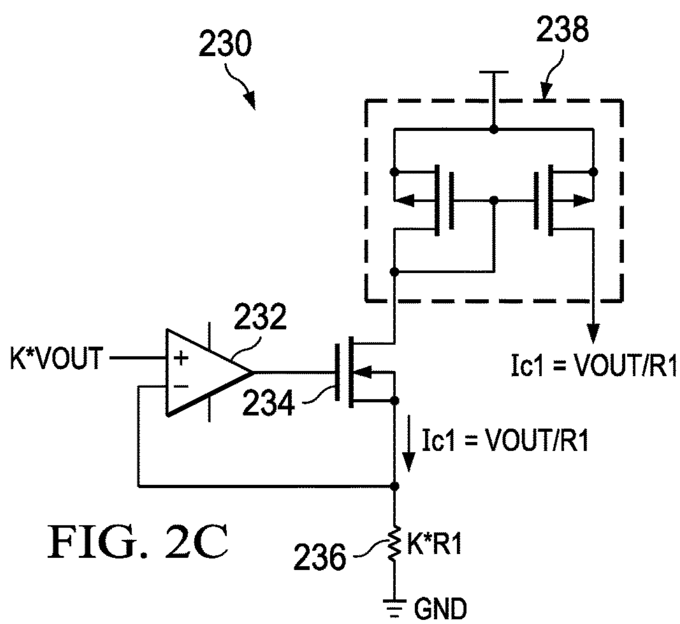


FIG. 2C

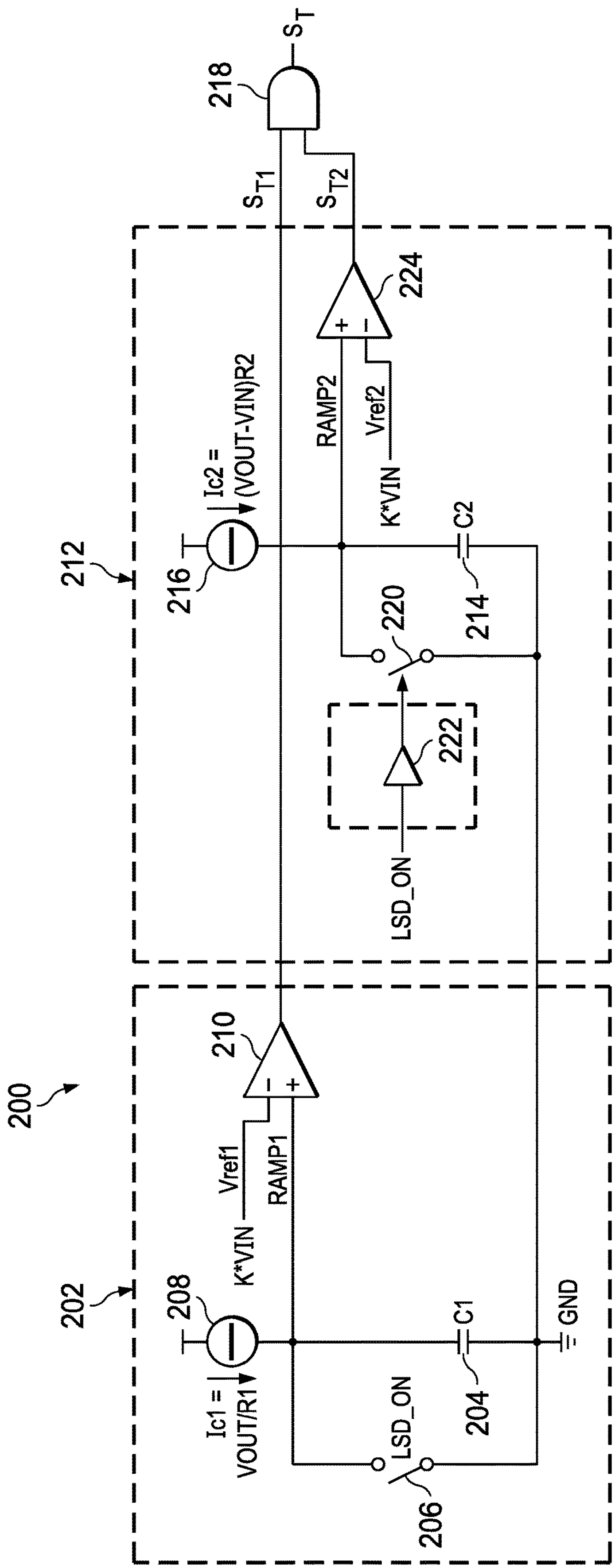

S_T
218
S_T1
S_T2
224
RAMP2
Vref2
K*VIN
Ic2 =
(VOUT-VIN)R2
216
212
C2
214
220
222
LSD_ON
210
200
Vref1
RAMP1
K*VIN
202
208
C1
GND
Ic1 =
VOUT/R1
LSD_ON
204
206

FIG. 2A

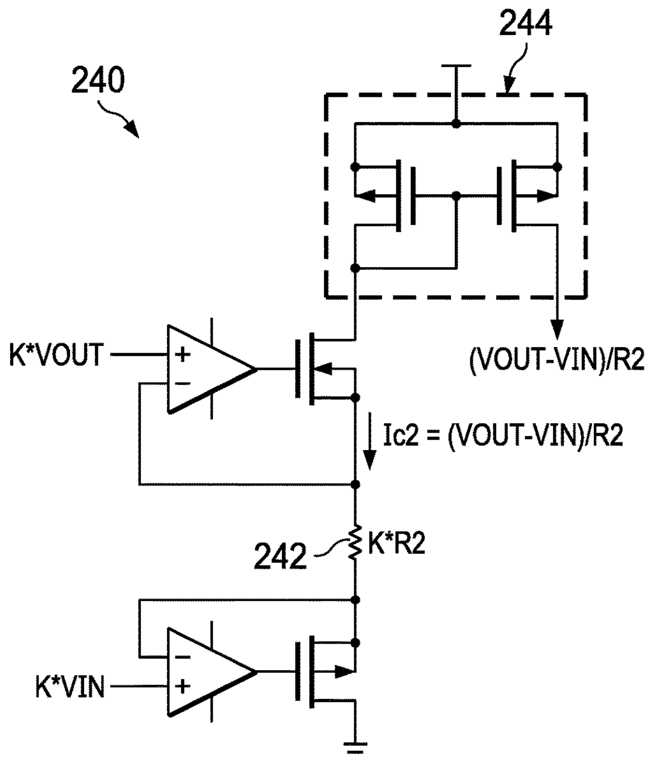

244
240
K*VOUT
(VOUT-VIN)/R2
Ic2 = (VOUT-VIN)/R2
242
K*R2
K*VIN

FIG. 2D

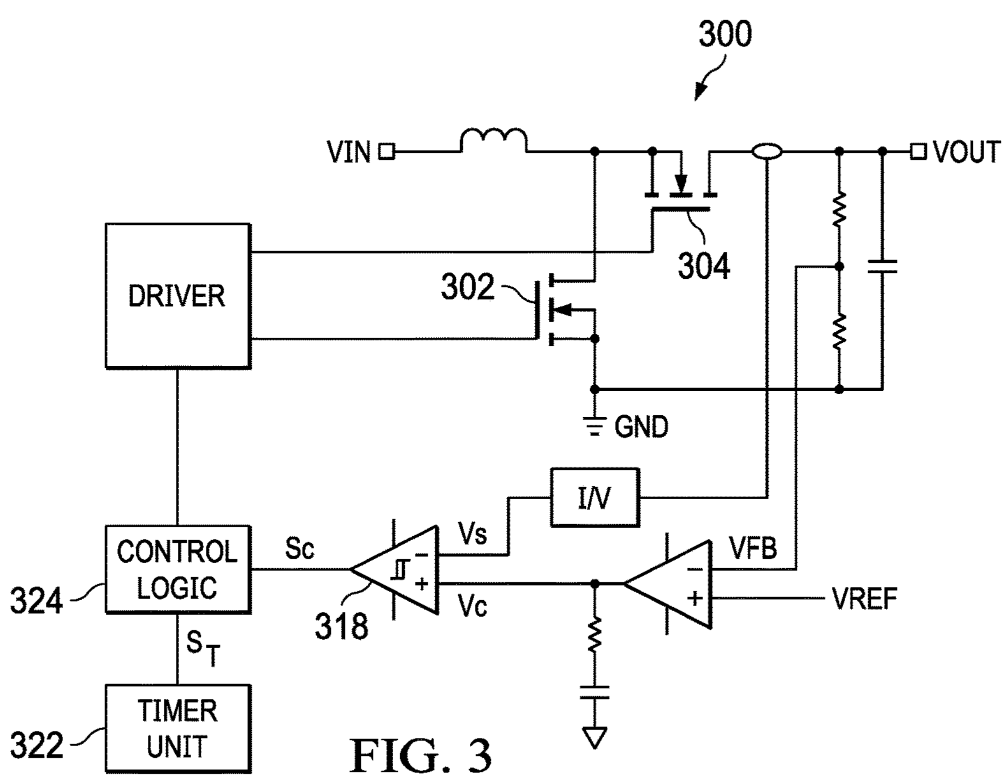
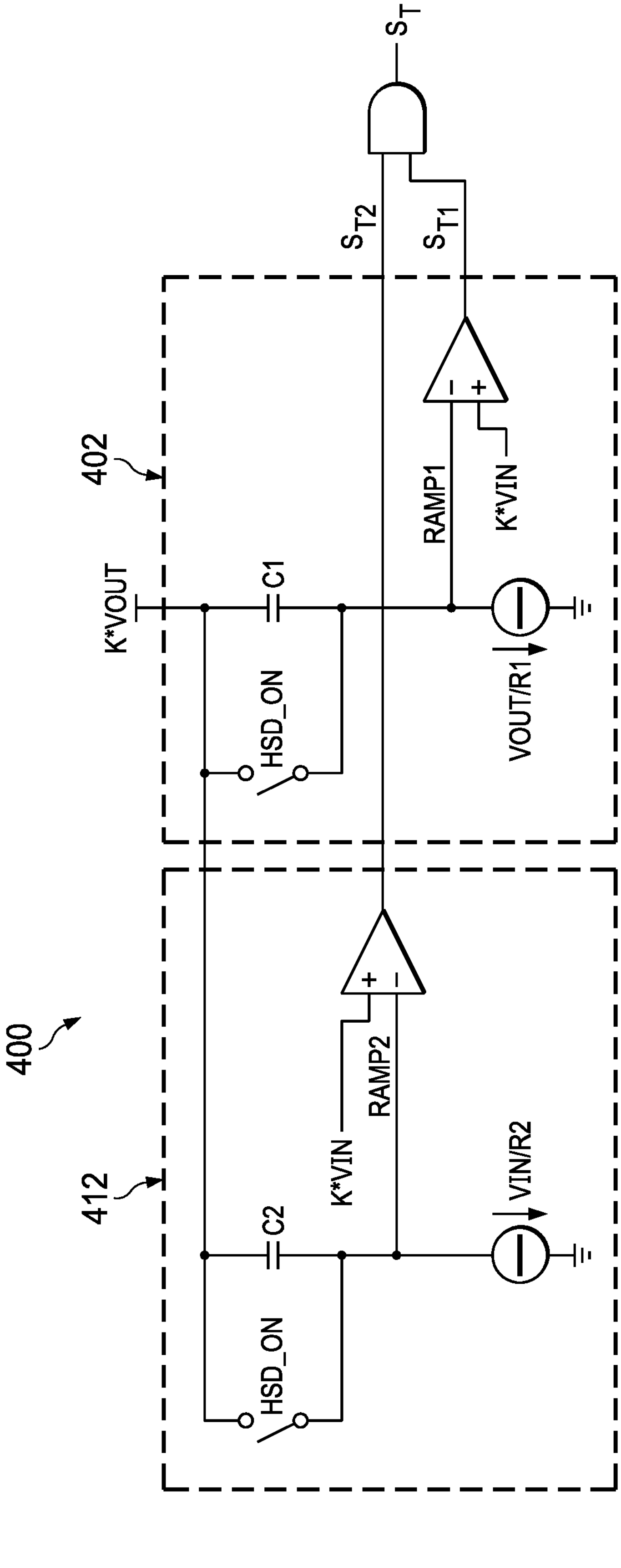

300
VIN
VOUT
DRIVER
302
304
GND
I/V
Vs
Sc
VFB
CONTROL LOGIC
324
318
Vc
VREF
ST
TIMER UNIT
322

FIG. 3



S_T
S_{T2}
S_{T1}
402
K*VOUT
C1
HSD_ON
RAMP1
K*VIN
VOUT/R1
400
412
C2
K*VIN
RAMP2
VIN/R2
HSD_ON

FIG. 4

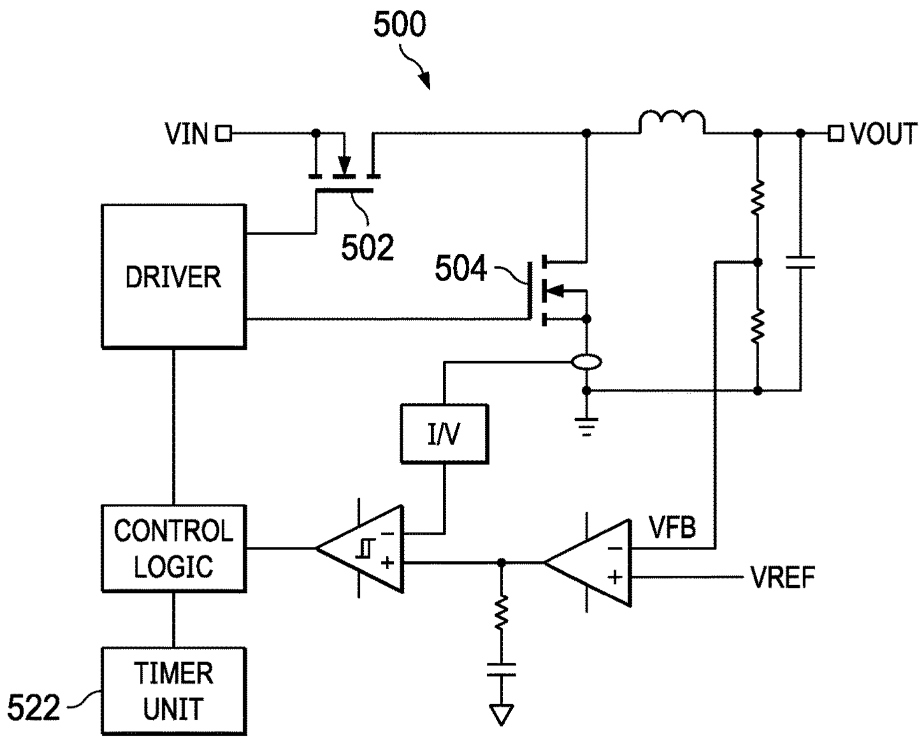

500
VIN
VOUT
502
504
DRIVER
I/V
CONTROL LOGIC
VFB
VREF
TIMER UNIT
522

FIG. 5

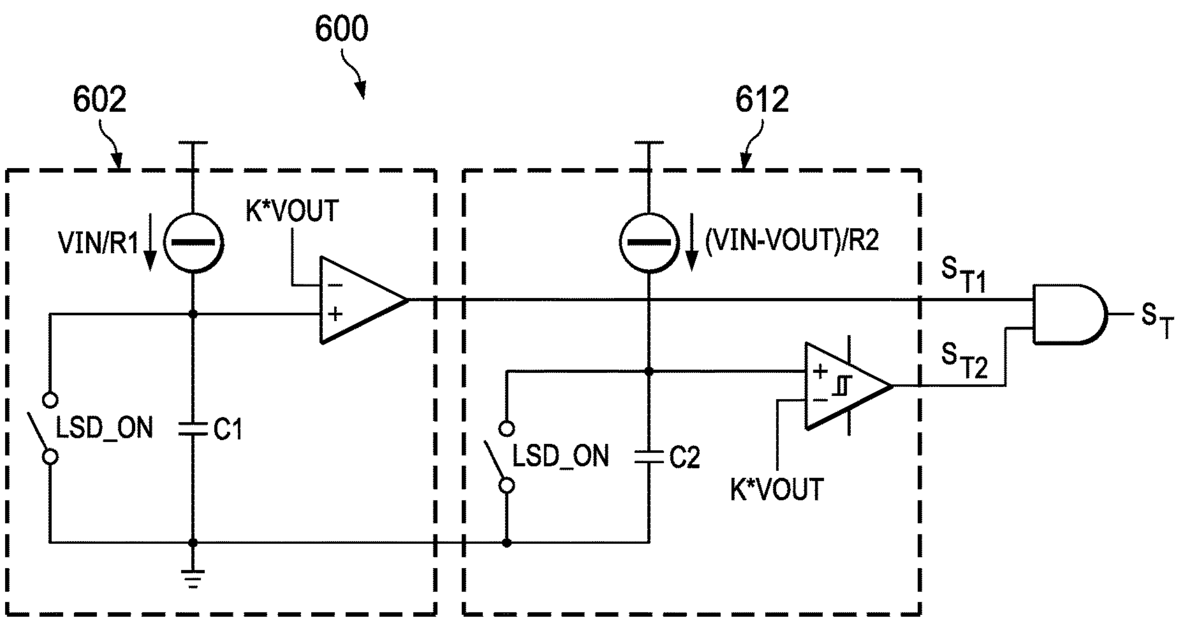

600
602
612
VIN/R1
K*VOUT
(VIN-VOUT)/R2
S_{T1}
S_T
S_{T2}
LSD_ON
C1
LSD_ON
C2
K*VOUT

FIG. 6

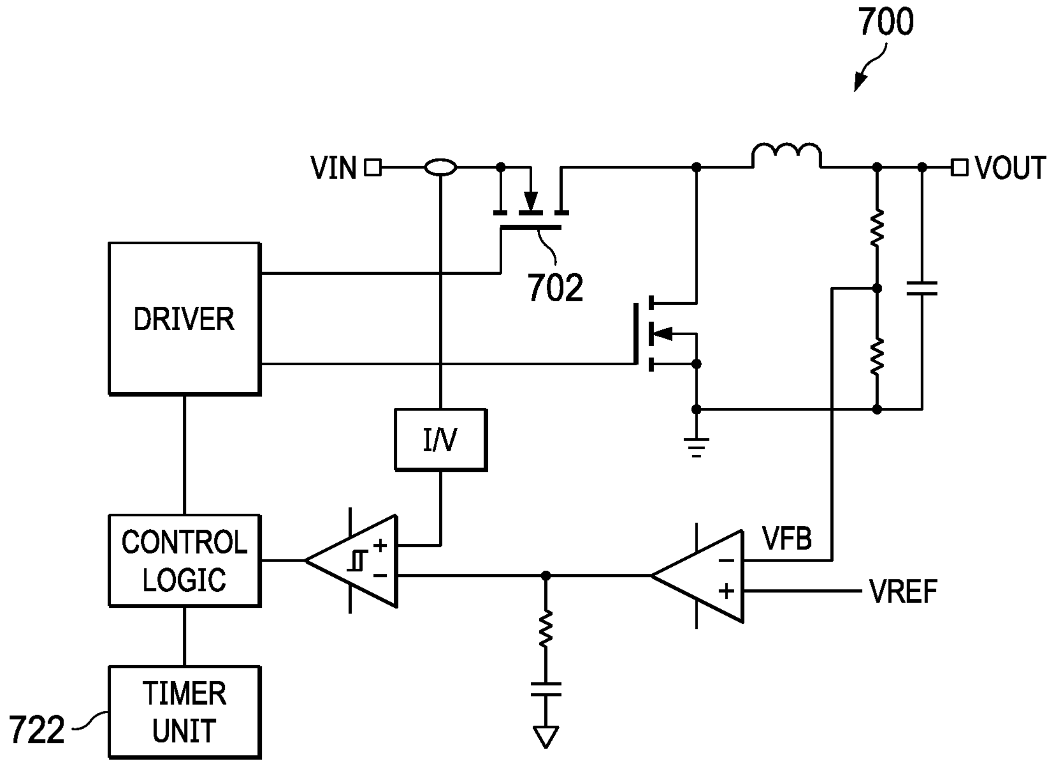

700
VIN
VOUT
702
DRIVER
I/V
CONTROL LOGIC
TIMER UNIT
722
VFB
VREF

FIG. 7

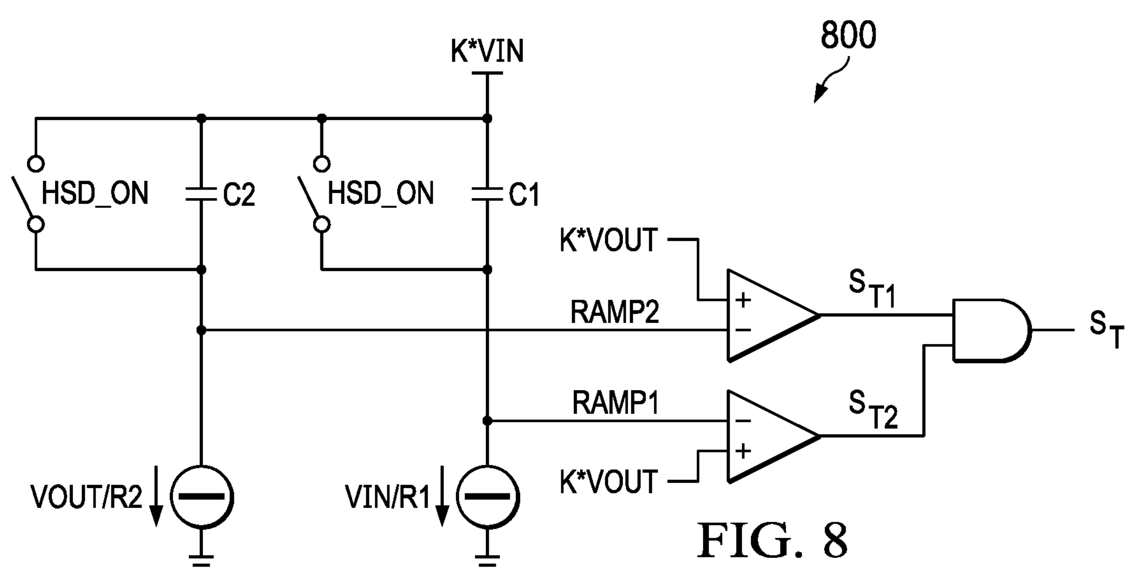

800
K*VIN
HSD_ON
C2
HSD_ON
C1
K*VOUT
RAMP2
S_T1
S_T
RAMP1
S_T2
K*VOUT
VOUT/R2
VIN/R1

FIG. 8

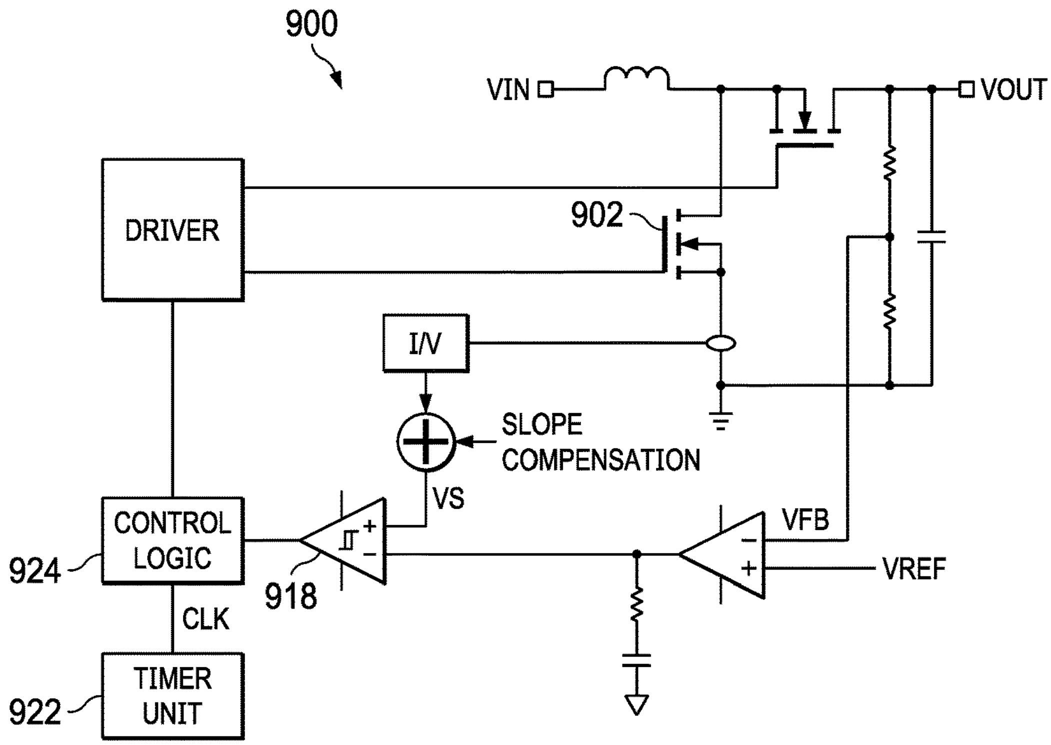

900
VIN
VOUT
DRIVER
902
I/V
SLOPE
COMPENSATION
VS
VFB
VREF
CONTROL
LOGIC
924
918
CLK
TIMER
UNIT
922

FIG. 9

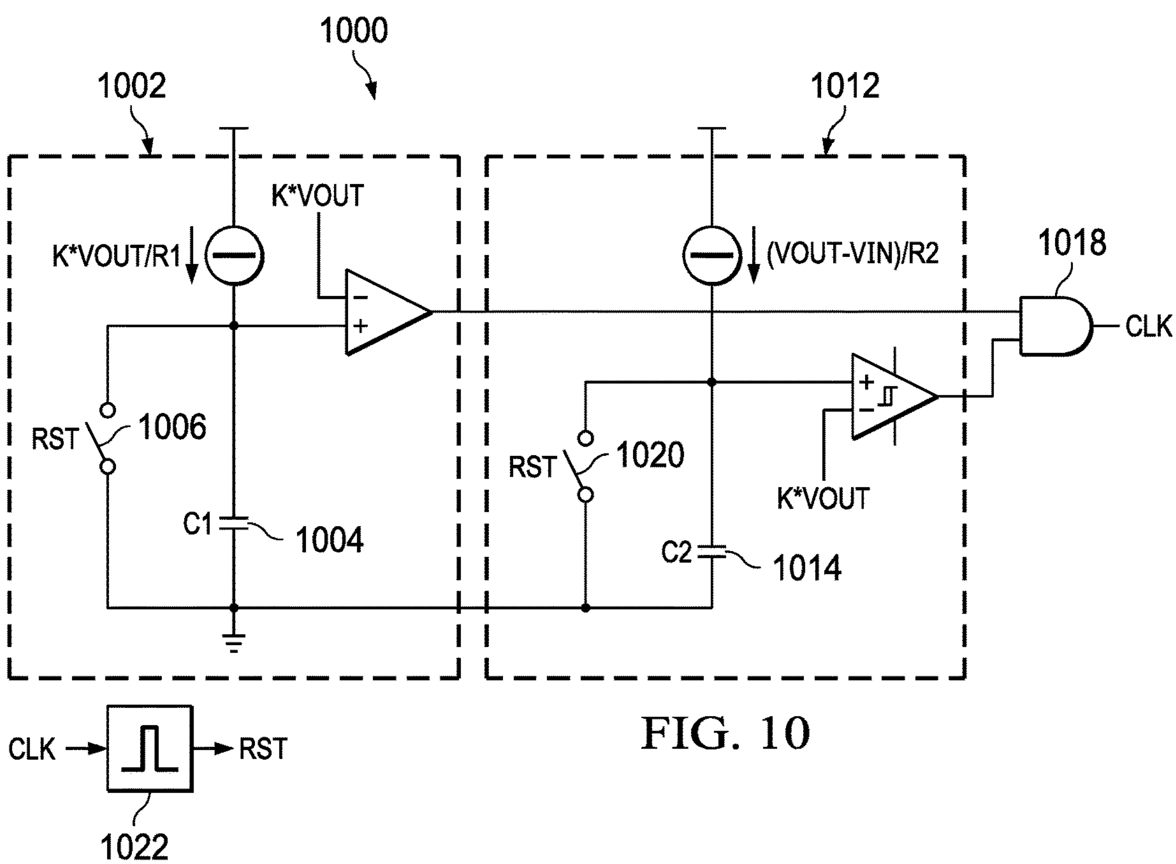

1000
1002
1012
K*VOUT
K*VOUT/R1
(VOUT-VIN)/R2
1018
CLK
RST
1006
RST
1020
K*VOUT
C1
1004
C2
1014
CLK
RST
1022

FIG. 10

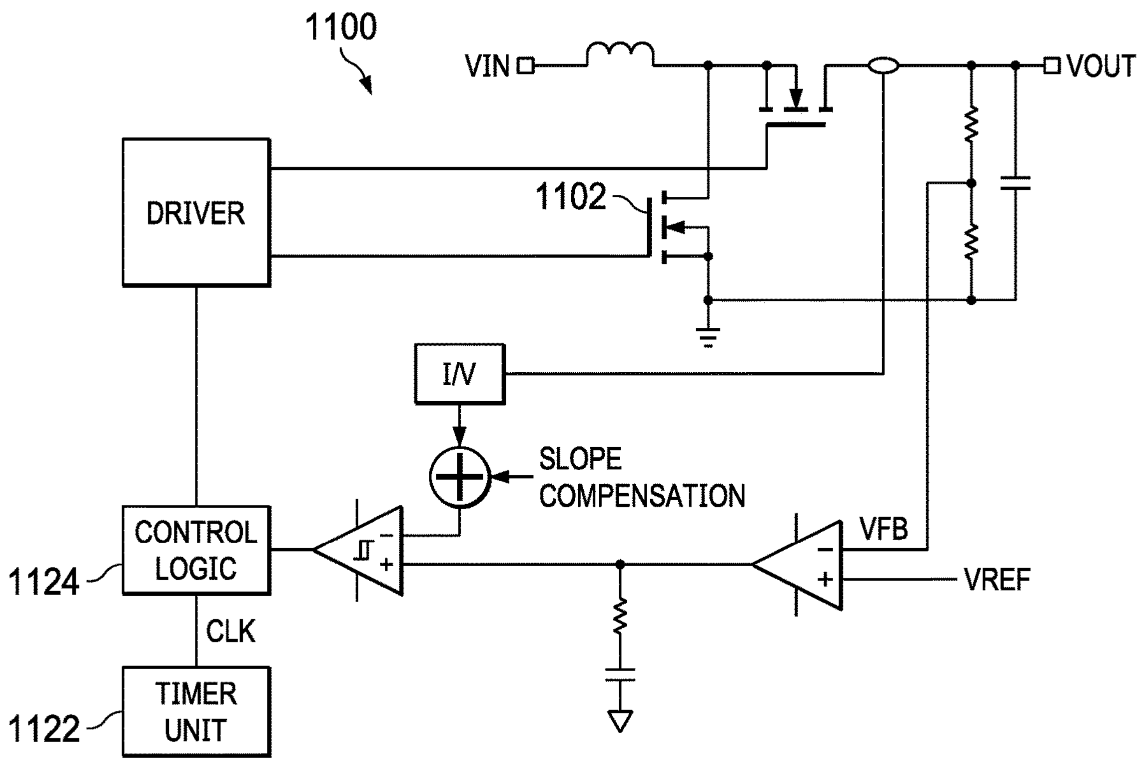

1100
VIN
VOUT
DRIVER
1102
I/V
SLOPE
COMPENSATION
CONTROL
LOGIC
1124
VFB
VREF
CLK
TIMER
UNIT
1122

FIG. 11

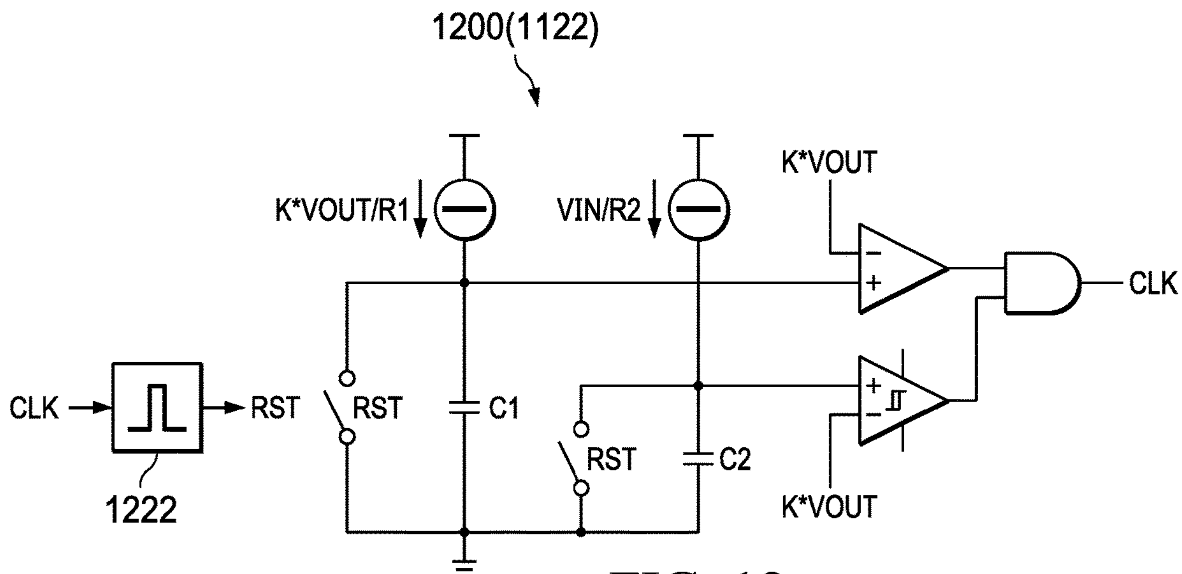

1200(1122)
K*VOUT/R1
VIN/R2
K*VOUT
CLK
RST
RST
C1
RST
C2
K*VOUT
1222
CLK

FIG. 12

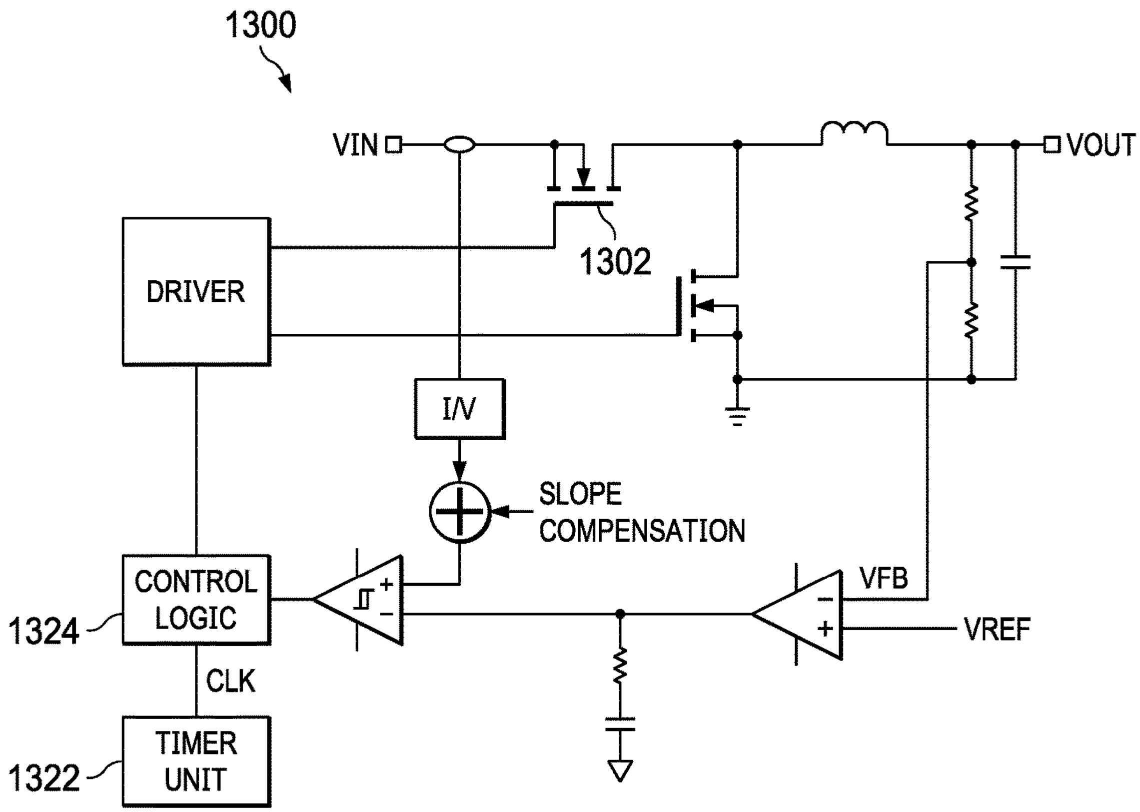

1300
VIN
VOUT
1302
DRIVER
I/V
SLOPE
COMPENSATION
VFB
VREF
CONTROL
LOGIC
1324
CLK
TIMER
UNIT
1322

FIG. 13

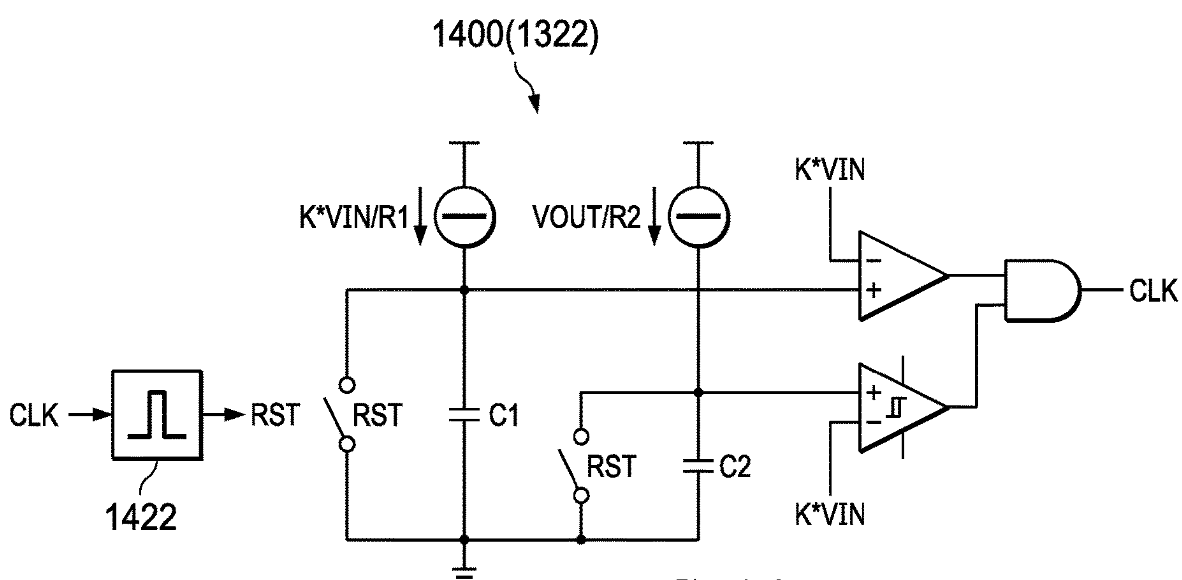

1400(1322)
K*VIN/R1
VOUT/R2
K*VIN
CLK
RST
RST
C1
RST
C2
1422
K*VIN
CLK

FIG. 14

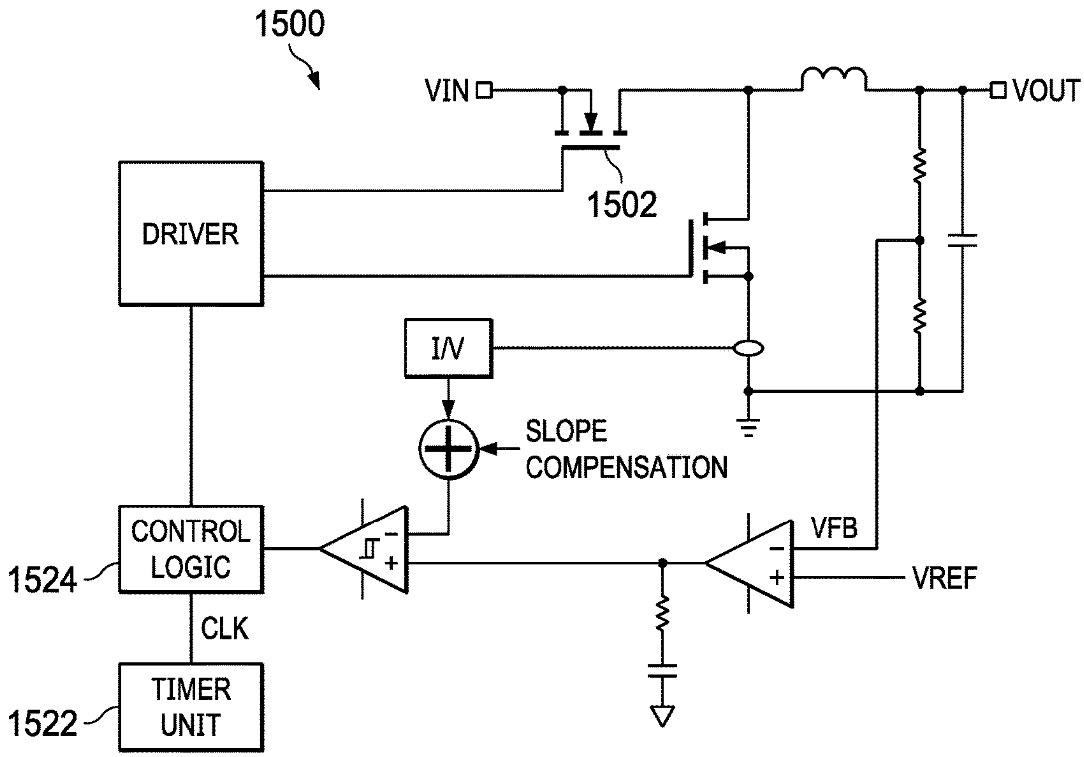

1500
VIN
VOUT
1502
DRIVER
I/V
SLOPE
COMPENSATION
CONTROL
LOGIC
1524
CLK
VFB
VREF
TIMER
UNIT
1522

FIG. 15

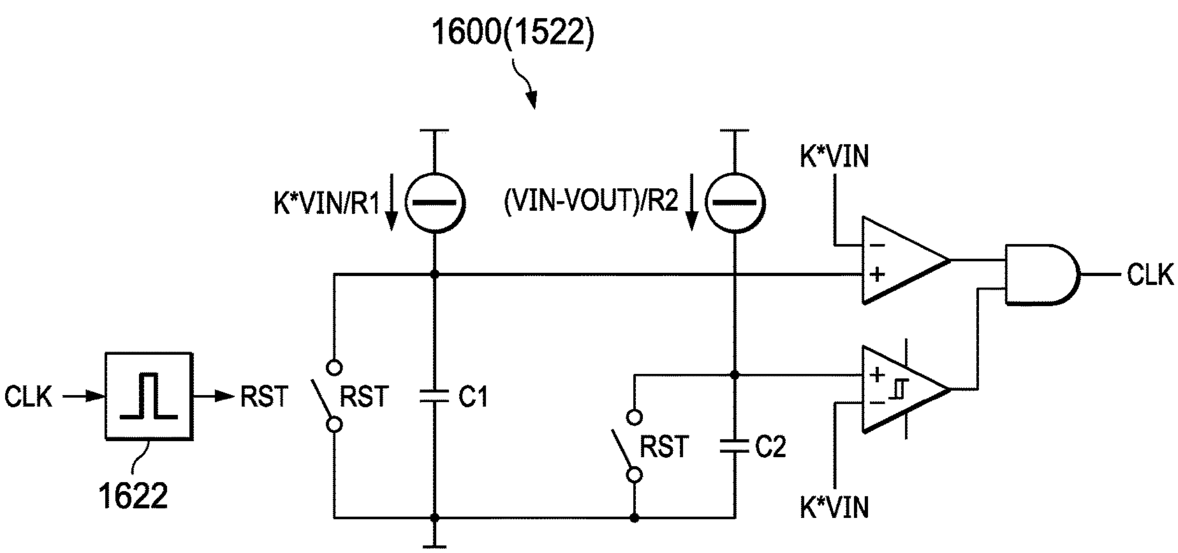

1600(1522)
K*VIN/R1
(VIN-VOUT)/R2
K*VIN
CLK
CLK
RST
RST
C1
RST
C2
1622
K*VIN

FIG. 16

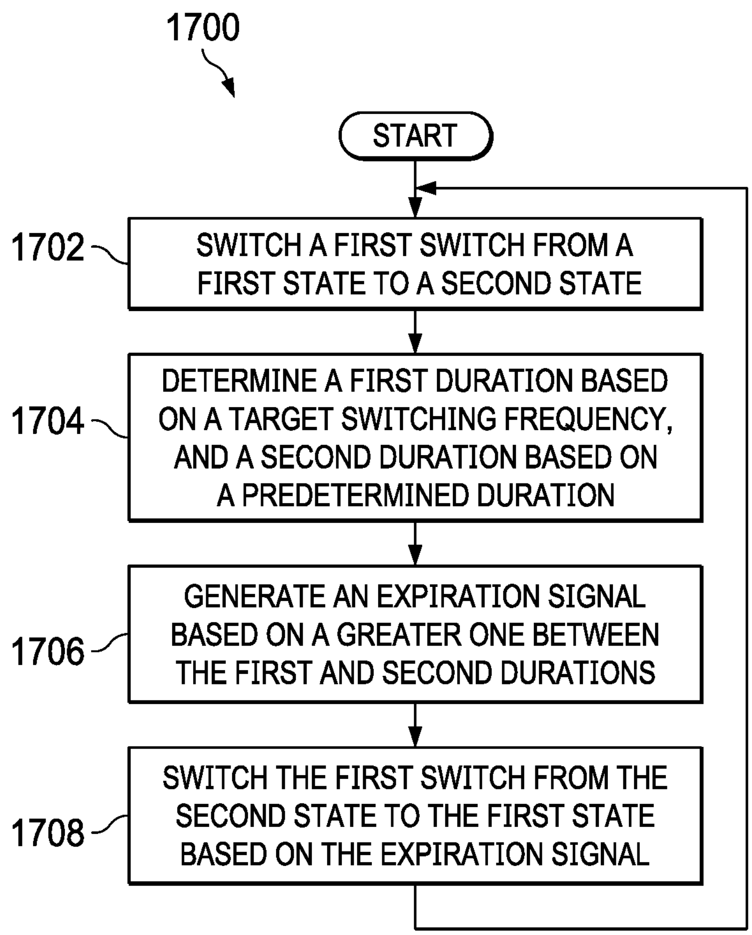

1700
START
1702
SWITCH A FIRST SWITCH FROM A FIRST STATE TO A SECOND STATE
1704
DETERMINE A FIRST DURATION BASED ON A TARGET SWITCHING FREQUENCY, AND A SECOND DURATION BASED ON A PREDETERMINED DURATION
1706
GENERATE AN EXPIRATION SIGNAL BASED ON A GREATER ONE BETWEEN THE FIRST AND SECOND DURATIONS
1708
SWITCH THE FIRST SWITCH FROM THE SECOND STATE TO THE FIRST STATE BASED ON THE EXPIRATION SIGNAL

FIG. 17

ADAPTIVE OFF-TIME OR ON-TIME DC-DC CONVERTER

This application is a divisional of U.S. patent application Ser. No. 16/876,897 filed May 18, 2020, which is a continuation of PCT Application No. PCT/CN2020/070110 filed Jan. 2, 2020, both of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

This relates generally to integrated circuits, and more particularly to a current mode DC-DC converter system.

BACKGROUND

DC-DC converters are widely used to convert an input DC voltage to a desired output DC voltage to drive a load. A current mode DC-DC converter may include a current loop that determines on or off time of a switch in each switching cycle by sensing an inductor current flowing through an inductor that is coupled to a switch node of the DC-DC converter, thereby regulating the inductor current. In a conventional adaptive on-time or off-time current mode DC-DC converter, a pulse-width-modulation (PWM) signal that controls the switch is regulated based on the sensed inductor current, the on-time or off-time determined based on input and output voltages of the DC-DC converter. In a conventional fixed frequency current mode DC-DC converter, the PWM signal is regulated based on the sensed inductor current, and a clock signal with a fixed target frequency.

SUMMARY

This description relates generally to integrated circuits, and more particularly to a DC-DC converter system with a wider range of duty cycle. A DC-DC converter system, such as a switch mode DC-DC converter, usually includes a switch configured to operate between on and off states based on a frequency signal, such as a pulse-width-modulation (PWM) signal, to generate an output DC voltage to a load by periodically storing energy from a source that provides an input DC voltage in a magnetic field of an inductor or a transformer and releasing the energy from the magnetic field. The ratio between the output DC voltage and the input DC voltage is proportional to a duty cycle of the PWM signal.

In one example, this description provides a DC-DC converter system including a first switch coupled to a switching node and operable between first and second states, and a controller, coupled to the first switch, and configured to switch the first switch between the first and second states based on an input voltage and an output voltage of the DC-DC converter system. The controller includes: a timer unit including a first timer configured to determine a first duration based on a target switching frequency of the DC-DC converter system, a second timer configured to determine a second duration based on a predetermined duration substantially equal to or greater than a minimum duration of the first state of the first switch and the input and output voltages, and logic circuitry coupled to the first and second timers and configured to generate an expiration signal responsive to expiration of both the first and second durations; and a control logic unit configured to switch the first switch from the second state to the first state based on the expiration signal.

In another example, this description provides a controller for switching a first switch of a DC-DC converter system. The controller includes: a timer unit including a first timer configured to determine a first duration based on a target switching frequency of the DC-DC converter system, a second timer configured to determine a second duration based on input and output voltages of the DC-DC converter system and a predetermined duration substantially equal to or greater than a minimum duration of a first state of the first switch, and logic circuitry coupled to the first and second timers and configured to generate an expiration signal responsive to expiration of both the first and second durations; and a control logic unit configured to switch the first switch from a second state to the first state based on the expiration signal.

In yet another example, this description provides a DC-DC converter system including: a first switch coupled to a switching node of the DC-DC converter system and a voltage supply node, and operable between first and second states; a first timer including a first capacitive element with a first capacitance, a first timing switching coupled in parallel with the first capacitive element, a first current source coupled in series with the first capacitive element and configured to source or sink a first current to or from the first capacitive element, and a first comparator with a first input terminal coupled to the first capacitive element, a second input terminal configured to receive a first reference voltage, and an output terminal configured to generate a first timer expired signal responsive to expiration of a first duration determined based on the first capacitance, the first current source and the first reference voltage; a second timer including a second capacitive element with a second capacitance, a second timing switching coupled in parallel with the second capacitive element; a second current source coupled in series with the second capacitive element and configured to source or sink a second current to or from the second capacitive element, and a second comparator with a first input terminal coupled to the second capacitive element, a second input terminal configured to receive a second reference voltage, and an output terminal configured to generate a second timer expired signal responsive to expiration of a second duration determined based on the second capacitance, the second current source and the second reference voltage; a logic gate coupled to outputs of the first and second comparators, and configured to generate an expiration signal based on expiration of both the first and second durations; and a control logic unit, coupled between the logic gate and a control terminal of the first switch, configured to switch the first switch from the second state to the first state based on the expiration signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic block diagram of a DC-DC converter system in accordance with a first implementation of this description.

FIGS. **2A-2D** show schematic circuit diagrams of a timer unit of the DC-DC converter system of FIG. **1**.

FIG. **3** is a schematic block diagram of a DC-DC converter system in accordance with a second implementation of this description.

FIG. **4** is a schematic circuit diagrams of a timer unit of the DC-DC converter system of FIG. **3**.

FIG. **5** is a schematic block diagram of a DC-DC converter system in accordance with a third implementation of this description.

FIG. **6** is a schematic circuit diagrams of a timer unit of the DC-DC converter system of FIG. **5**.

FIG. **7** is a schematic block diagram of a DC-DC converter system in accordance with a fourth implementation of this description.

FIG. **8** is a schematic circuit diagrams of a timer unit of the DC-DC converter system of FIG. **7**.

FIG. **9** is a schematic block diagram of a DC-DC converter system in accordance with a fifth implementation of this description.

FIG. **10** is a schematic circuit diagrams of a timer unit of the DC-DC converter system of FIG. **9**.

FIG. **11** is a schematic block diagram of a DC-DC converter system in accordance with a sixth implementation of this description.

FIG. **12** is a schematic circuit diagrams of a timer unit of the DC-DC converter system of FIG. **11**.

FIG. **13** is a schematic block diagram of a DC-DC converter system in accordance with a seventh implementation of this description.

FIG. **14** is a schematic circuit diagrams of a timer unit of the DC-DC converter system of FIG. **13**.

FIG. **15** is a schematic block diagram of a DC-DC converter system in accordance with an eighth implementation of this description.

FIG. **16** is a schematic circuit diagrams of a timer unit of the DC-DC converter system of FIG. **15**.

FIG. **17** is a flow chart of a method of operating a DC-DC converter system in accordance with an implementation of this description.

DETAILED DESCRIPTION

This description relates to current mode DC-DC converter systems.

Referring to FIG. **1**, a schematic block diagram of a DC-DC converter system **100** in accordance with a first implementation of this description is shown. More particularly, FIG. **1** shows an adaptive off-time current mode boost DC-DC converter system with peak current control topology.

The system **100** includes a first switch **102** coupled between a switch node SW and a voltage supply node, for example, a ground node GND, and a second switch **104** coupled between the switch node SW and an output node VOUT of the system **100**, thereby allowing a current flowing from the switch node SW to the output node VOUT. The first and second switches **102** and **104**, also named respectively as low side and high side switches, can be transistors, for example, N-channel MOSFETs that are respectively controlled by gate drive signals LSD_ON and HSD_ON to alternately operable between first and second states, e.g. on and off states, allowing a current to follow from the switch node SW towards the voltage supply node GND, and from the switch node SW towards the output node VOUT. In an alternate example, the second switch **104** can be replaced by a diode that allows current to flow from the switch node SW to the output node VOUT in a unidirectional manner. The system **100** also includes an input inductor **106** coupled between an input node VIN and the switch node SW, and an output capacitive element **108** coupled between the output node VOUT and the ground node GND.

The system **100** includes a controller **110** coupled to the first and second switches **102** and **104** to generate a PWM signal to alternately switch on and off the first and second switches **102** and **104** through a driver unit **112** which generates the gate drive signals LSD_ON and HSD_ON based on the PWM signal. In a preferred example, the driver unit **112** can be either a part of or separate from the controller **110**.

The controller **110** includes a sensing unit **114** configured to generate a control signal Sc based on a difference between a sensing voltage Vs proportional to an inductor current IL through the inductor **106** and a control voltage Vc proportional to a difference between a reference voltage VREF and a feedback voltage VFB proportional to the output voltage VOUT, generated by an amplifier **116**. In one example, the sensing unit **114** includes a comparator **118** configured to generate the control signal Sc to switch the first switch **102** from the on state to the off state if the sensing voltage Vs increases to the control voltage Vc. In one example, the sensing voltage Vs is proportional to a current Is flowing through the first switch **102** and obtained through a current-to-voltage (I/V) unit **120**, for example, by sensing a voltage across a sensing resistor (not shown) coupled between the first switch **102** and the ground node GND.

The controller **110** includes a control logic **124** configured to switch the first switch **102** from the on state to the off state through the driver unit **112**, based on the control signal Sc. However, a minimum duration of the on state, also known as a minimum on-time Ton_min, of the first switch is usually limited due to various factors of the DC-DC converter system **100**, such as blanking time of inductor current IL sensing, delay caused by the comparator **118**, the control logic **124** and/or the driver unit **112**. The minimum on-time of the first switch **102** limits the range of a ratio of output voltage VOUT to the input voltage VIN.

The controller **110** also includes a timer unit **122** configured to determine a preferred duration of the off state, also known as an off-time Toff, of the first switch **102** based on a target switching frequency fsw of the DC-DC converter system **100**, the minimum on-time Ton_min of the first switch, and the input and output voltages VIN and VOUT of the system **100**.

The timer unit **122** is further configured to generate an expiration signal S_T to switch the first switch **102** from the off state to the on state when the preferred off-time Toff expires. The control logic **124** is configured to generate the PWM signal based on the control signal Sc and the expiration signal S_T. For example, the control logic **124** can be an edge-triggered SR flip flop that asserts the PWM signal based on the expiration signal S_T and de-asserts the PWM signal based on the control signal Sc.

FIG. **2**A shows an example schematic circuit diagram of a timer unit **200**, such as the timer unit **122** of the DC-DC converter system **100** of FIG. **1**. The timer unit **200** includes a first timer **202** configured to generate a first timer expired signal S_{T1} based on a first duration **T1**. In one example, the first duration **T1** is a nominal duration of the second state, e.g. the off state, of the first switch **102** determined based on the target switching frequency fsw of the DC-DC converter system **100** and the input and output voltages VIN and VOUT, such that the DC-DC converter system operating at the target switching frequency fsw converts the input voltage VIN to the output voltage VOUT by keeping the first switch **102** at the off state for the nominal duration in each target switching cycle T. In the example of the adaptive off-time current mode boost DC-DC converter system with peak current control topology, the first duration **T1** is determined in accordance with the equation below:

$$T1 = T \cdot \frac{VIN}{VOUT} \tag{1}$$

where T is the target switching cycle, T=1/fsw.

In one example, the first timer **202** includes a first capacitive element **204** with a capacitance C**1**. The first capacitive element **204** is coupled in parallel with a first charging control switch **206** that is controlled by the gate drive signal LSD_ON, and in series with a first current source **208** configured to source a first charging current Ic**1** to the first capacitive element **204**. In the example of FIG. **2**, Ic**1**=VOUT/R**1**. Charging the first capacitive element **204** is triggered responsive to the first switch **102** being switched from the on state to the off state. The first timer **202** includes a first comparator **210** with an inverting input coupled to a reference voltage generator shown in FIG. **2**B to receive a reference voltage Vref**1**=K·VIN. The first capacitive element **204** is coupled between a non-inverting input of the first capacitive element **210** and the ground node GND. The first capacitive element **210** is configured to generate a first timer expired signal S_{T1} when a voltage across the first capacitive element **204** increased to the reference voltage K*VIN. Accordingly, the first duration T**1** is determined by the first timer **202** in accordance with the equation below:

$$T1 = K \cdot R1 \cdot C1 \cdot \frac{VIN}{VOUT} \tag{2}$$

where K is a number greater than 0, K·R**1** is resistance of a resistor **236** of a charging path of the first timer **202** shown in FIG. **2**C, and K·R**1**·C**1** is configured to be substantially equal to the target switching cycle T=1/fsw of the DC-DC converter system **100** within acceptable error range resulting from inherent errors of the first capacitive element **210** and the resistor **236**. However, the first charging current Ic**1** and the reference voltage Vref**1** can be other values as long as meeting the equation below:

$$T1 = \frac{\mathrm{V}ref2}{Ic1} \cdot C1 = T \cdot \frac{VIN}{VOUT} \tag{3}$$

The timer unit **200** also includes a second timer **212** with a structure similar to that of the first timer **202** except that a second capacitive element **214** of the second timer **212** has a capacitance C**2** and is charged by a second current source **216** with a second charging current Ic**2**, where Ic**2**=(VOUT−VIN)/R**2**. The second timer **212** is configured to be triggered substantially simultaneously with the first timer based on the gate drive signal LSD_ON, and to generate a second timer expired signal S_{T2} based on a second duration T**2** that is determined based on the minimum on-time Ton_min of the first switch **102** and the input and output voltages VIN and VOUT. The second duration T**2** is provided in accordance with the equations below:

$$T2 = K \cdot R2 \cdot C2 \cdot \frac{VIN}{VOUT - VIN} \tag{4}$$

where K·R**2** is resistance of a resistor **242** of a charging path of the second timer **212** shown in FIG. **2**D, and K·R**2**·C**2** is configured to be substantially equal to or slightly greater, e.g. 10 ns greater, than the minimum on-time Ton_min of the first switch **102**.

In one example, the second timer **212** includes a second charging switch **220** configured to be switched off simultaneously with switching off the first charging switch **206**, and K·R**2**·C**2** is configured to be substantially equal to the minimum on-time Ton_min of the first switch **102**, such that the second duration equals an off-time of the first switch **102** determined under the condition that the on-time of the first switch **102** is the minimum on-time Ton_min.

In another example, the second timer **212** includes a second charging switch **220** configured to be switched off simultaneously with switching off the first charging switch **206**, and K·R**2**·C**2** is configured to be slightly, e.g. 10 ns, greater, than the minimum on-time Ton_min of the first switch **102** to ensure the second duration longer than an off-time of the first switch **102** determined under the condition that the on-time of the first switch **102** is the minimum on-time Ton_min.

In yet another example, K·R**2**·C**2** is configured to be substantially equal to the minimum on-time Ton_min of the first switch **102**, and the second timer **212** further includes a delay unit **222** such that the second charging switch **220** is configured to be switched off slightly later, e.g. 50 ns or more, than switching off the first charging switch **206** to ensure the second duration longer than an off-time of the first switch **102** determined under the condition that the on-time of the first switch **102** is the minimum on-time Ton_min.

In one example, the second timer **212** further includes a second comparator **224** with an inverting input coupled to another reference voltage generator to receive another reference voltage Vref**2**. The second charging current Ic**2** and the reference voltage Vref**2** can be other values as long as meeting the equation below:

$$T2 = \frac{\mathrm{V}ref2}{ic2} \cdot C1 \geq \mathrm{Ton\_min} \cdot \frac{VIN}{VOUT - VIN} \tag{5}$$

The timer unit **200** also includes a logic gate **218** configured to generate the expiration signal S_T responsive to both the first and second timer expired signals S_{T1} and S_{T2} being asserted. In one example, when VOUT/(R**1**·C**1**)>(VOUT−VIN)/(R**2**·C**2**), the second duration T**2** is smaller than the first duration T**1**, the preferred duration of the off state of the first switch **102** is determined by the first duration T**1**, which is the nominal duration of the off state of the first switch **102** determined based on the target switching frequency fsw and the input and output voltages of the system **100**. In another example, when VOUT/(R**1**·C**1**)<(VOUT−VIN)/(R**2**·C**2**), the preferred duration of the off state of the first switch **102** is determined by the second duration T**2**, and the duration of the on state of the first switch **102** is regulated at (VOUT−VIN)/VIN*Toff=K*R**2***C**2**, which is substantially equal to or greater than the minimum on-time Ton_min of the first switch **102**, therefore the inductor current IL can still be regulated based on the sensing voltage Vs. In such situation, an actual switching cycle of the DC-DC converter system **100** is configured to be K·R**2**·C**2**·VOUT/(VOUT−VIN), with is greater than the target switching cycle of the DC-DC converter system **100**.

FIG. **2**B shows an example schematic circuit diagram of the reference voltage generator **226** that provides the reference voltage K·VIN. In one example, the reference voltage generator **226** includes a voltage divider **228** generating the reference voltage K·VIN proportional to the input voltage VIN.

FIG. **2**C shows an example schematic circuit diagram of a current source **230**, for example, the first current source **208** of the timer unit **200** of FIG. **2**. The first current source **230** includes an error amplifier **232** having an output terminal coupled to a gate node of a transistor **234**, a non-inverting input terminal configured to receive a reference voltage K·VOUT which can be provided in a similar manner as the reference voltage generator **220** shown in FIG. **2**B, and an inverting input terminal coupled to a source node of the transistor **234**. The first current source **230** also includes the resistor **236** coupled between the source node of the transistor **234** and the ground node GND and having a resistance of K·R**1**, and a current mirror **238** coupled to a drain node of the transistor **234** and configured to mirror a current flowing through the resistor **236**, which is provided as the first charging current Ic**1**=VOUT/R**1**.

FIG. **2**D shows an example schematic circuit diagram of another current source **240**, for example, the second current source **216** of the timer unit **200** of FIG. **2**. The second current source **240** has a structure similar to that of the first current source **230** except that a voltage difference across the resistor **242** is configured to be VOUT−VIN. The current mirror **244** is configured to mirror a current flowing through the resistor **242**, which is provided as the second charging current Ic**2**=(VOUT−VIN)/R**2**.

Referring back to FIG. **1**, the control logic unit **124** is configured to switch the first switch **102** from the off state to the on state based on the expiration signal S_T. Therefore, the duration of the off state, i.e., the off time Toff, of the first switch **102** is configured to be a greater one between the first and second duration T**1** and T**2**.

In a conventional adaptive off-time current mode boost DC-DC converter system, the off-time Toff of the first switch, e.g. the low side switch, is configured to be a nominal off-time Toff' determined in accordance with the equation below:

$$Toff' = T \cdot VIN/VOUT \quad (6)$$

Due to the limit of the minimum on-time Ton_min of the system, an on duty cycle range of the system is limited between Ton_min/T and 1, and thus a ratio of VOUT to VIN range is limited between T/(T−Ton_min) and ∞. Similarly, operation ranges of other conventional adaptive on-time/off-time current mode DC-DC converter systems with other topologies are also limited by the nominal off-time and minimum on-time of the system, or a nominal on-time and a minimum-off time of the system. Table 1 lists the operation ranges of conventional adaptive on-time/off-time current mode DC-DC converter systems with different topologies.

TABLE 1

Operation ranges of conventional adaptive on-time/off-time current mode DC-DC converter systems

Buck/Boost	Topology	Ton and Toff	On Duty Cycle Range	VOUT/VIN range
Boost	Peak Current + adaptive Toff	Current Regulated, Ton ≥ Ton_min Toff = T * VIN/VOUT	(Ton_min/T, 1)	(T/(T − Ton_min), ∞)
	Valley current + adaptive Ton	Ton = T * VOUT − VIN)/VOUT Current Regulated, Toff ≥ Toff_min	(0, 1 − Toff_min/T)	(1, T/Toff_min)
Buck	Peak Current + adaptive Toff	Current Regulated, Ton ≥ Ton_min Toff = T * (VIN − VOUT)/VIN	(Ton_min/T, 1)	(Ton_min/T, 1)
	Valley current + adaptive Ton	Ton = T * VOUT/VIN Current Regulated, Toff ≥ Toff_min	(0, 1 − Toff_min/T)	(0, 1 − Toff_min/T)

In this description, the proposed adaptive off-time current mode boost DC-DC converter system **100** dynamically extends the off-time Toff of the first switch **102** when the off-time determined based on the minimum on-time Ton_min and the input and output voltages VIN and VOUT is greater than the nominal off-time of the DC-DC converter system. As the off-time of the first switch **102** can be extended to Ton_min·VIN/(VOUT−VIN) when a target ratio of VOUT to VIN is less than T/(T−Ton_min), the range of on duty cycle can be extended between 0 and 1, and the range of VOUT/VIN can be extended between 1 and ∞.

FIG. **3** shows a schematic block diagram of a DC-DC converter system **300** in accordance with a second implementation of this description. More particularly, FIG. **3** shows an adaptive on-time current mode boost DC-DC converter system with valley current control topology.

The DC-DC converter system **300** is substantially similar to the DC-DC converter system **100** of FIG. **1** except that the sensing voltage Vs is generated proportional to a current flowing through the second switch **304**, i.e. the high side switch, the comparator **318** is configured to generate the control signal Sc when the sensing voltage Vs decreases to the control voltage Vc, and the control logic **324** is configured to switch on the first switch **302** based on the control signal Sc and to switch off the first switch **302** based on the expiration signal S_T generated by the timer unit **322**.

FIG. **4** shows an example schematic circuit diagram of a timer unit **400**, such as the timer unit **322** of the DC-DC converter system **300** of FIG. **3**. The timer unit **400** includes a first timer **402** configured to generate a first timer expired signal S_{T1} based on a first duration T**1**. In one example, the first duration T**1** is a nominal duration of the on state, i.e. a nominal on-time Ton, of the first switch **302** determined based on a target switching frequency fsw of the DC-DC converter system **300** and input and output voltages VIN and VOUT in accordance with the equation below:

$$T1 = T \cdot \frac{VOUT - VIN}{VOUT} \quad (6)$$

where T is the target switching cycle of the system **300**, T=1/fsw.

The first timer **402** is configured to determine the first duration T**1**, i.e., the nominal on-time of the first switch **302**, in accordance with the equation below:

$$T1 = K \cdot R1 \cdot C1 \cdot \frac{VOUT - VIN}{VOUT} \tag{7}$$

where K·R**1**·C**1** is configured to be substantially equal to a target switching cycle T=1/fsw of the DC-DC converter system **300**.

The timer unit **400** also includes a second timer **412** with a structure similar to that of the first timer **402** except that the second timer **412** is configured to generate a second timer expired signal ST**2** based on a second duration T**2** provided in accordance with the equations below:

$$T2 = K \cdot R2 \cdot C2 \cdot \frac{VOUT - VIN}{VOUT} \tag{8}$$

where K·R**2**·C**2** is configured to be substantially equal to or slightly greater, e.g. 10 ns greater, than a minimum duration of the off state, i.e., the minimum off-time Toff_min, of the first switch **302**.

The first and second timer **402** and **412** are configured to start timing responsive to the second switch **304** being switched from the on state to the off state, i.e., when the first switch **302** is switched from the off state to the on state. Similar to the timer unit **200** of FIG. **2**, the timer unit **400** is configured to generate an expiration signal S_T responsive to both of the first and second timer expired signals S_{T1} and S_{T2} being asserted.

Similar to the DC-DC converter system **100** of FIG. **1**, as the on-time of the first switch **302** can be extended to Toff_min·(VOUT−VIN)/VIN when a target ratio of VOUT to VIN is greater than T/Toff_min, the range of on duty cycle can be extended between 0 and 1, and the range of VOUT/VIN can be extended between 1 and ∞.

FIG. **5** in combination with FIG. **6** shows a schematic block diagram of a DC-DC converter system **500** in accordance with a third implementation of this description. More particularly, FIG. **5** shows an adaptive on-time current mode buck DC-DC converter system with valley current control topology. Similar to the adaptive on-time current mode boost DC-DC converter system **300** shown in FIG. **3** in combination with the timer unit **400** of FIG. **4**, the DC-DC converter system **500** is configured to switch off the first switch **502**, i.e. the high side switch, based on an expiration signal S_T generated by the timer unit **522**. The timer unit **522**, shown as the timer unit **600** of FIG. **6** in more detail, is configured to generate the expiration signal S_T to switch off the first switch **502** responsive to expiration of both of the first and second duration T**1** and T**2** respectively determined by the first and second timers. The first duration T**1** is determined based on a nominal duration of the on state, e.g. a nominal on-time Ton, of the first switch **602** determined based on the switching frequency fsw and the input and output voltages VIN and VOUT of the DC-DC converter system **500**, and the second duration T**2** is determined based on the input and output voltages VIN and VOUT and a predetermined duration substantially equal to greater than the minimum duration of the off state, also known as minimum off-time Toff_min, of the first switch **502**. Similar to the DC-DC converter system **300** of FIG. **3**, as the duration of the on state, i.e., the on-time, of the first switch **502** can be extended to Toff_min·VOUT/(VIN−VOUT) when a target ratio of VOUT to VIN is greater than 1−Toff_min/T, the range of on duty cycle can be extended between 0 and 1, and the range of VOUT/VIN can be extended between 0 and 1.

FIG. **7** in combination with FIG. **8** shows a schematic block diagram of a DC-DC converter system **700** in accordance with a fourth implementation of this description. More particularly, FIG. **7** shows an adaptive off-time current mode buck DC-DC converter system with peak current control topology. Similar to the adaptive on-time current mode buck DC-DC converter system **500** shown in FIG. **5** in combination with the timer unit **600** of FIG. **6**, the DC-DC converter system **700** is configured to switch on the first switch **702**, i.e. the high side switch, based on the expiration signal S_T generated by the timer unit **722**. The timer unit **722**, shown as the timer unit **800** of FIG. **8** in more detail, is configured to generate the expiration signal S_T to switch on the first switch **702** when both of the first and second duration T**1** and T**2** respectively determined by the first and second timers expire. The first duration T**1** is determined based on a nominal duration of the off state, i.e. a nominal off-time, of the first switch **702** which is determined based on the switching frequency fsw and the input and output voltages VIN and VOUT of the DC-DC converter system **700**, and the second duration T**2** is determined based on the input and output voltages VIN and VOUT and a predetermined duration substantially equal to greater than the minimum on-time Ton_min of the first switch **702**. Similar as the DC-DC converter system **500** of FIG. **5**, as the off-time of the first switch **702** can be extended to Ton_min·(VIN−VOUT)/VOUT when a target ratio of VOUT to VIN is less than Ton_min/T, the range of on duty cycle can be extended between 0 and 1, and the range of VOUT/VIN can be extended between 0 and 1.

Table 2 lists the operation ranges of adaptive on-time/off-time current mode DC-DC converter systems with different topologies in accordance with the first to fourth implementations of this description.

TABLE 2

Operation ranges of adaptive on-time/off-time current mode DC-DC converter systems in accordance with implementations of this description

Buck/ Boost	Topology	Ton and Toff	On Duty Cycle Range	VOUT/VIN range
Boost	Peak Current + adaptive Toff	Current Regulated, Ton ≥ Ton_min Toff = max{T * VIN/VOUT, Ton_min * VIN/(VOUT − VIN)}	(0, 1)	(1, ∞)
	Valley current + adaptive Ton	Ton = max{T * (VOUT − VIN)/VOUT, Toff _min * (VOUT − VIN)/VIN} Current Regulated, Toff ≥ Toff_min	(0, 1)	(1, ∞)

TABLE 2-continued

Operation ranges of adaptive on-time/off-time current mode DC-DC converter systems in accordance with implementations of this description				
Buck/ Boost	Topology	Ton and Toff	On Duty Cycle Range	VOUT/VIN range
Buck	Peak Current + adaptive Toff	Current Regulated, Ton ≥ Ton_min Toff = max{T * (VIN − VOUT)/VIN, Ton_min * (VIN − VOUT)/VOUT}	(0, 1)	(0, 1)
	Valley current + adaptive Ton	Ton = max{T * VOUT/VIN, Toff_min * VOUT/(VIN − VOUT)} Current Regulated, Toff ≥ Toff_min	(0, 1)	(0, 1)

Referring to FIG. **9**, a schematic block diagram of a DC-DC converter system **900** in accordance with a fifth implementation of this description is shown. More particularly, FIG. **9** shows a fixed frequency current mode boost DC-DC converter system with peak current control topology. The DC-DC converter system **900** is substantially similar to the DC-DC converter system **100** of FIG. **1** except that the sensing voltage Vs provided to the comparator **918** is proportional to a combination of the current flowing through the first switch **902** and a slope compensation signal, and the control logic **924** is configured to switch on the first switch **902** based on a clock signal CLK generated by the timer unit **922**, for example, a rising edge of the clock signal CLK.

FIG. **10** shows an example schematic circuit diagram of a timer unit **1000**, such as the timer unit **922** of the DC-DC converter system **900** of FIG. **9**. The timer unit **1000** is substantially similar to the timer unit **200** of FIG. **2**, except that the timer unit **922** further includes a one-shot signal generator **1022** coupled to the switches **1006** and **1020** to provide a one-shot signal RST based on the clock signal CLK, such that the first and second timers **1002** and **1012** start timing responsive to the first switch **902** being switched from the off state to the on state. The first timer **1002** is configured to generate a first timer expired signal S_{T1} based on a first duration T**1**. In one example, the first duration T**1** is a target switching cycle T=1/fsw, where fsw is a target switching frequency of the DC-DC converter system **900**. The first duration T**1** is provided in accordance with the equations below:

$$T1=K\cdot R1\cdot C1 \tag{9}$$

where K·R**1**·C**1** is configured to be substantially equal to the target switching cycle T=1/fsw of the DC-DC converter system **900**.

The timer unit **1000** also includes a second timer **1012** configured to generate a second timer expired signal S_{T2} based on a second duration T**2** that is determined based on a minimum duration of the on state, i.e., a minimum on-time Ton_min, of the first switch **902** and the input and output voltages VIN and VOUT. In one example, the second duration T**2** is determined based on the input and output voltages VIN and VOUT, and a predetermined duration substantially equal to greater than the minimum on-time Ton_min of the first switch **902**. The second duration T**2** is provided in accordance with the equations below:

$$T2 = K\cdot R2\cdot C2\cdot \frac{VOUT - VIN}{VOUT} \tag{10}$$

where K·R**2**·C**2** is configured to be substantially equal to or slightly greater, e.g. 10 ns greater, than the minimum on-time Ton_min of the first switch **902**.

The timer unit **1000** further includes a gate logic **1018** configured to generate, for example, a rising edge, of the clock signal CLK based on the first and second timer expired signals S_{T1} and S_{T2}, wherein the cycle of the clock signal CLK is configured to be the larger one of the first and second duration T**1** and T**2**.

In a conventional fixed frequency peak current control mode boost DC-DC converter system, a cycle of a clock signal CLK that periodically switches the first switch from a second state, e.g. the off state, to a first state, e.g. the on state, is fixed by the target switching frequency fsw of the conventional system.

Due to the minimum on-time Ton_min of the conventional system, the on duty cycle range of the system is limited between Ton_min/T and 1−Toff_min/T, and thus a range of a ratio of VOUT to VIN is limited between T/(T−Ton_min) and T/Toff_min. Similarly, operation ranges of other conventional fixed frequency current mode DC-DC converter systems with other topologies are also limited by the target switching cycle and minimum on or off time of the first switch of the system. Table 3 lists the operation ranges of conventional fixed frequency current mode DC-DC converter systems with different topologies.

TABLE 3

Operation ranges of conventional fixed frequency current mode DC-DC converter systems				
Buck/ Boost	Topology	Ton and Toff	On Duty Cycle Range	VOUT/VIN range
Boost	Fixed frequency + Peak Current	Current Regulated, Ton ≥ Ton_min Fixed period T	(Ton_min/T, 1 − Toff_min/T)	(T/(T − Ton_min), T/Toff_min)
	Fixed frequency + Valley Current	Current Regulated, Toff ≥ Toff_min Fixed Period T	(Ton_min/T, 1 − Toff_min/T)	(T/(T − Ton_min), T/Toff_min)

TABLE 3-continued

Operation ranges of conventional fixed frequency current mode DC-DC converter systems

Buck/ Boost	Topology	Ton and Toff	On Duty Cycle Range	VOUT/VIN range
Buck	Fixed frequency + Peak Current	Current Regulated, Ton ≥ Ton_min Fixed period T	(Ton_min/T, 1 − Toff_min/T)	(Ton_min/T, 1 − Toff_min/T)
	Fixed frequency + Valley Current	Current Regulated, Toff ≥ Toff_min Fixed Period T	(Ton_min/T, 1 − Toff_min/T)	(Ton_min/T, 1 − Toff_min/T)

In this description, the proposed fixed frequency current mode boost DC-DC converter system **900** dynamically extends the switching cycle when a switching cycle determined based on the minimum on-time Ton_min and the input and output voltages VIN and VOUT is greater than the target switching cycle of the DC-DC converter system. As the switching cycle can be extended to Ton_min·VOUT/(VOUT−VIN) when a target ratio of VOUT to VIN is less than T/(T−Ton_min), the range of on duty cycle can be extended between 0 and 1−Toff_min/T, and the range of VOUT/VIN can be extended between 1 and T/Toff_min.

FIG. **11** in combination with FIG. **12** shows a schematic block diagram of a DC-DC converter system **1100** in accordance with a sixth implementation of this description. More particularly, FIG. **11** shows a fixed current mode boost DC-DC converter system with valley current control topology. Similar to the timer unit **1000** of FIG. **10**, the timer unit **1200** is configured to generate a clock signal CLK with a cycle determined based on a larger one between the target switching cycle of the DC-DC converter system **1100** and an adjusted cycle determined based on the input and output voltages VIN and VOUT and a predetermined duration substantially equal to greater than the minimum off time Toff_min of the first switch **1102** of the DC-DC converter system **1100**. The control logic **1124** is configured to switch off the first switch **1102** responsive to, for example, a rising edge, of the clock signal CLK.

FIG. **13** in combination with FIG. **14** shows a schematic block diagram of a DC-DC converter system **1300** in accordance with a seventh implementation of this description. More particularly, FIG. **13** shows a fixed current mode buck DC-DC converter system with peak current control topology. Similar to the timer unit **1000** of FIG. **10**, the timer unit **1400** is configured to generate a clock signal CLK with a cycle determined based on a larger one between the target switching cycle of the DC-DC converter system **1300** and an adjusted cycle determined based on the input and output voltages VIN and VOUT and a predetermined duration substantially equal to greater than the minimum on time Ton_min of the first switch **1302** of the DC-DC converter system **1300**. The control logic **1324** is configured to switch on the first switch **1302** responsive to, for example, a rising edge, of the clock signal CLK.

FIG. **15** in combination with FIG. **16** shows a schematic block diagram of a DC-DC converter system **1500** in accordance with an eighth implementation of this description. More particularly, FIG. **15** shows a fixed current mode buck DC-DC converter system with valley current control topology. Similar to the timer unit **1200** of FIG. **12**, the timer unit **1200** is configured to generate a clock signal CLK with a cycle determined based on a larger one between the target switching cycle of the DC-DC converter system **1500** and an adjusted cycle determined based on the input and output voltages VIN and VOUT and a predetermined duration substantially equal to greater than the minimum on time Toff_min of the first switch **1502** of the DC-DC converter system **1500**. The control logic **1524** is configured to switch off the first switch **1502** responsive to, for example, a rising edge, of the clock signal CLK.

Table 4 lists the operation ranges of fixed frequency current mode DC-DC converter systems with different topologies in accordance with the fifth to eighth implementations of this description.

TABLE 4

Operation ranges of fixed frequency current mode DC-DC converter systems in accordance with implementation of this description

Buck/ Boost	Topology	Ton and Toff	On Duty Cycle Range	VOUT/VIN range
Boost	Fixed frequency + Peak Current	Current Regulated, Ton ≥ Ton_min T_new = max{T, Ton_min * VOUT/(VOUT − VIN)}	(0, 1 − Toff_min/T)	(1, T/Toff_min)
	Fixed frequency + Valley Current	Current Regulated, Toff ≥ Toff_min T_new = max{T, Toff * VOUT/VIN}	(Ton_min/T, 1)	(T/(T − Ton_min), ∞)
Buck	Fixed frequency + Peak Current	Current Regulated, Ton ≥ Ton_min T_new = max{T, Ton_min * VIN/VOUT}	(0, 1 − Toff_min/T)	(0, 1 − Toff_min/T)
	Fixed frequency + Valley Current	Current Regulated, Toff ≥ Toff_min T_new = max{T, Toff_min * VIN/(VIN − VOUT)}	(Ton_min/T, 1)	(Ton_min/T, 1)

Referring to FIG. **17**, a flow chart of a method **1700** for regulating a DC-DC converter system in accordance with an implementation of this description is shown. With reference to the DC-DC converter system **100** of FIG. **1**, the DC-DC converter system includes the first switch **102** coupled between the switch node SW and a voltage supply node, for example, a ground node GND. The inductor **106** is coupled between the switch node SW and the voltage input node VIN, and second switch **104** is coupled between the switch node SW and the voltage output node VOUT. The first switch **102** is configured to periodically allow the inductor current IL to flow there through. Other topologies of current mode DC-DC converter systems with the same mechanism to sensing a load current and regulate the DC-DC converter system are possible as well, such as the DC-DC converter systems **300** to **1500** respectively shown in FIGS. **3**-**15**.

Starting at step **1702**, the control logic **124** generates a PWM signal to switch the first switch **102** from a first state, e.g. on state, to a second state, e.g. off state, through the driver unit **112**.

At step **1704**, the first timer **202** of the timer unit **122** starts timing a first duration T**1**, and substantially simultaneously, the second timer **212** of the timer unit **122** starts timing a second duration T**2** that is determined based on input and output voltages VIN and VOUT of the DC-DC converter system **100** and a minimum duration of the first state of the first switch **102**, i.e., the minimum on-time Ton_min, of the first switch **102**.

In one example, for adaptive off-time/on-time current mode DC-DC converter systems such as the DC-DC converter systems **100** to **700** of FIGS. **1**, **3**, **5** and **7** with corresponding timer units **200** to **800** of FIGS. **2**A, **4**, **6** and **8**, the first and second timers **202** and **212** are configured to start timing responsive to the first switch **102** being switched from the first state to the second state, the first duration T**1** is a nominal duration of the second state of the first switch **102** determined based on a target switching frequency fsw of the DC-DC converter system and the input and output voltages, and the second duration T**2** is an adjusted duration of the second state of the first switch determined based on the input and output voltages VIN and VOUT and a predetermined duration substantially equal to greater than a minimum duration of the first state of the first switch.

In the example with reference to the DC-DC converter system **100** of FIG. **1**, the first duration T**1** is a nominal duration of the off state, i.e., a nominal off time Toff, of the first switch **102**, and provided in accordance with the equations below:

$$T1 = T \cdot \text{VIN/VOUT} \tag{11}$$

where T is a target switching cycle T=1/fsw of the DC-DC converter system **100**, fsw is a target switching frequency of the DC-DC converter system **100**.

The second duration T**2** is an adjusted duration of the off state, i.e., an adjusted off-time, of the first switch **102** determined based on the input and output voltages VIN and VOUT and a predetermined duration Ton_min' substantially equal to or greater than a minimum duration of the on state, i.e., a minimum on-time Ton_min, of the first switch **102**. The second duration T**2** is provided in accordance with the equations below:

$$T2 = \text{Ton\_min}' \cdot \frac{VOUT - VIN}{VOUT} \tag{12}$$

where Ton_min' is the predetermined duration substantially equal to or slightly greater, e.g. 10 ns greater, than the minimum on-time Ton_min of the first switch **902**.

In another example, for fixed frequency current mode DC-DC converter systems such as the DC-DC converter systems **900** of FIG. **9** with a timer unit **1000** of FIG. **10**, the first and second timers start timing responsive to the first switch **902** being switched from the second state to the first state, e.g., for the DC-DC converter system **900**, from the off state to the on state. The first duration T**1** is the target switching cycle T of the DC-DC converter system **900**. The second duration T**2** is an adjusted switching cycle determined based on the input and output voltages VIN and VOUT and a predetermined duration Ton_min' substantially equal to or greater than the minimum on time Ton_min of the first switch **902**. The second duration T**2** is provided in accordance with the equations below:

$$T2 = \text{Ton\_min}' \cdot \frac{VOUT - VIN}{VOUT} \tag{13}$$

where Ton_min' is the predetermined duration substantially equal to or slightly greater, e.g. 10 ns greater, than the minimum on-time Ton_min of the first switch **902**.

At step **1706**, the sensing unit **114** generates a control signal Sc to switch the first switch **102** from the first state, e.g. the on state, to the second state, e.g. the off state, based on a difference between a sensed voltage Vs proportional to the inductor current IL and a difference between a reference voltage VREF and a feedback voltage VFB proportional to the output voltage VOUT.

In one example, for DC-DC converter systems with a peak current control topology, such as the DC-DC converter systems **100**, **700**, **900** and **1300** respectively shown in FIGS. **1**, **7**, **9** and **13**, switching the first switch from the first state to the second state comprises switching the first switch from the on state to the off state responsive to a current through the first switch increasing to a peak value determined based on the difference between the feedback voltage VFB of the output voltage VOUT and the reference voltage VREF and expiration of a minimum on-time of the first switch.

In another example, for DC-DC converter systems with a valley current control topology, such as the DC-DC converter systems **300**, **500**, **1100** and **1500** respectively shown in FIGS. **3**, **5**, **11** and **15**, switching the first switch from the first state to the second state comprises switching the first switch from an off state to an on state responsive to a current through the second switch decreasing to a valley value determined based on a difference between the feedback voltage VFB of the output voltage VOUT and a reference voltage VREF and expiration of a minimum off-time of the first switch.

At step **1708**, the timer unit **122** generates an expiration signal S_T to switch the first switch **102** from the second state to the first state responsive to expiration of both the first and second timers.

The term "couple" is used throughout the specification. The term may cover connections, communications, or signal paths that enable a functional relationship consistent with the description of this description. For example, if device A generates a signal to control device B to perform an action, in a first example device A is coupled to device B by direct connection, or in a second example device A is coupled to device B through intervening component C if intervening component C does not alter the functional relationship between device A and device B such that device B is controlled by device A via the control signal generated by device A.

Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

What is claimed is:

1. A DC-DC converter system, comprising:

a first switch coupled to a switching terminal of the DC-DC converter system, and configured to operate between first and second states;

a first timer comprising:

a first capacitive element with a first capacitance;

a first timer switch coupled in parallel with the first capacitive element;

a first current source coupled in series with the first capacitive element and configured to source or sink a first current to or from the first capacitive element; and

a first comparator with a first input terminal coupled to the first capacitive element, a second input terminal configured to receive a first reference voltage, and an output terminal configured to generate a first timer expired signal responsive to expiration of a first duration determined in response to the first capacitance, the first current source and the first reference voltage;

a second timer comprising:

a second capacitive element with a second capacitance;

a second timer switch coupled in parallel with the second capacitive element;

a second current source coupled in series with the second capacitive element and configured to source or sink a second current to or from the second capacitive element; and

a second comparator with a first input terminal coupled to the second capacitive element, a second input terminal configured to receive a second reference voltage, and an output terminal configured to generate a second timer expired signal responsive to expiration of a second duration determined in response to the second capacitance, the second current source and the second reference voltage;

a logic gate coupled to outputs of the first and second comparators, and configured to generate an expiration signal in response to expiration of both the first and second timers; and

a control logic unit, coupled between the logic gate and a control terminal of the first switch, configured to switch the first switch from the second state to the first state in response to the expiration signal, wherein:

the first timing switch is coupled to the control logic unit, and is configured to be switched off in response to the first switch being switched from the first state to the second state; and

the second timer switch is coupled to the control logic unit, and is configured to be switched off with the first timing switch.

2. The DC-DC converter system of claim 1, wherein:

the first comparator is configured to generate the first timer expired signal responsive to a voltage difference across the first capacitive element changing by a first voltage difference, wherein the first duration is determined by a target switch cycle and input and output voltages of the DC-DC converter system,

and

the second comparator is configured to generate the second timer expired signal responsive to a voltage difference across the second capacitive element changing by a second voltage difference, wherein the second duration is determined by a predetermined duration equal to or greater than a minimum duration of the first state of the first switch and the input and output voltages of the DC-DC converter system.

3. The DC-DC converter system of claim 2, wherein:

a product of the first capacitance and a ratio of the first voltage difference to the first current equals to a duration of the second state of the first switch determined by the target switch cycle and input and output voltages of the DC-DC converter system, and

a product of the second capacitance and a ratio of the second voltage difference to the second current equals to an adjusted duration of the second state of the first switch determined by the predetermined duration and the input and output voltages of the DC-DC converter system.

4. The DC-DC converter system of claim 1, further comprising:

a one-shot signal generator configured to generate a one-shot signal in response to the first switch being switched from the second state to the first state, wherein

the first timing switch includes a control terminal coupled to receive the one-shot signal, and is configured to be switched off when the one-shot signal is de-asserted,

the first comparator is configured to generate the first timer expired signal responsive to a voltage difference across the first capacitive element changing by a first voltage difference, wherein the first duration is determined by a target switch cycle of the DC-DC converter system,

the second timing switch includes a control terminal coupled to receive the one-shot signal, and is configured to be switched off substantially simultaneously with the first timing switch, and

the second comparator is configured to generate the second timer expired signal responsive to a voltage difference across the second capacitive element changing by a second voltage difference, wherein the second duration is determined by a predetermined duration substantially equal to or longer than a minimum duration of the first state of the first switch and input and output voltages of the DC-DC converter system.

5. The DC-DC converter system of claim 4, wherein:

a product of the first capacitance and a ratio of the first voltage difference to the first current equals to a target switch cycle of the DC-DC converter system, and

a product of the second capacitance and a ratio of the second voltage difference to the second current equals to an adjusted switch cycle of the DC-DC converter system determined by the predetermined duration and the input and output voltages of the DC-DC converter system.

6. A system comprising:

a first timer configured to generate a first timer expired signal in response to a first duration time;

a second timer configured to generate a second timer expired signal in response to a second duration time;

a logic circuit configured to generate an expiration signal in response to the first timer expired signal and the second timer expired signal; and a control circuit configured to switch a switch from a second state to a first state in response to the expiration signal, wherein:

the first timer is configured to start timing of the first duration time with the second timer starting timing of the second duration time in response to the switch being switched from the first state to the second state; and

the system is capable of a target switching frequency determined by a capacitance and a resistance of a charging path in the first timer, and the first duration time is based on the target switching frequency of the system and an input voltage and an output voltage.

7. The system of claim **6**, wherein:

the second duration time is determined by a minimum off time of a second switch, the input voltage, and the output voltage.

8. The system of claim **6**, wherein:

in response to the first timer expired signal and the second timer expired signal being asserted, the expiration signal is generated by the logic circuit.

9. The system of claim **6**, wherein:

the logic circuit is an AND gate.

10. The system of claim **6**, wherein:

the first timer includes a first timer switch coupled in parallel with a first capacitor; and

the second timer includes a second timer switch coupled in parallel with a second capacitor.

11. The system of claim **10**, wherein:

the first timer includes a first comparator with a first input terminal of the first timer coupled to the first capacitor, a second input terminal coupled to a first reference voltage; and

the second timer includes a second comparator with a first input terminal of the second timer coupled to the second capacitor, a second input terminal coupled to a second reference voltage.

12. The system of claim **11**, wherein:

the first input terminal of the first timer is coupled to a first current source; and

the first input terminal of the second timer is coupled to a second current source.

13. The system of claim **12**, wherein:

the first current source is generated by an input voltage to the system; and

the second current source is generated by an output voltage of the system.

14. The system of claim **6**, wherein:

the control circuit is configured to receive a control signal; and

the control signal is determined by a current in the switch.

15. The system of claim **14**, wherein:

the control signal is asserted in response to a sensing voltage associated with the switch reaches a control voltage threshold.

16. The system of claim **14**, wherein:

the control circuit is configured to turn off the switch in response to the control signal.

17. The system of claim **6**, wherein:

the control circuit is coupled to a driver circuit; and

the driver circuit is coupled to a control terminal of the switch.

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