US Patent & Trademark Office
Patent Public Search | Text View

United States Patent Application Publication	20250261459
Kind Code	A1
Publication Date	August 14, 2025
Inventor(s)	LEE; Eun Khwang

IMAGE SENSING DEVICE

Abstract

An image sensing device includes a pixel array of a plurality of unit pixels arranged in a row direction and a column direction and including a first unit pixel that includes floating diffusion region configured to store photocharge generated within the first unit pixel in corresponding to incident light; a first gain conversion transistor connected to the first floating diffusion region; a first row booster block connected to the first gain conversion transistor and a second gain conversion transistor that is included in a second unit pixel adjacent to the first unit pixel in the row direction; and a first column booster block connected to the first gain conversion transistor and a third gain conversion transistor that is included in a third unit pixel adjacent to the first unit pixel in the column direction.

Inventors: **LEE; Eun Khwang (Icheon-si, KR)**

Applicant: **SK hynix Inc.** (Icheon-si, KR)

Family ID: **1000008560163**

Appl. No.: **19/192200**

Filed: **April 28, 2025**

Foreign Application Priority Data

KR	10-2021-0142106	Oct. 22, 2021

Related U.S. Application Data

parent US continuation 17858665 20220706 parent-grant-document US 12288793 child US 19192200

Publication Classification

Int. Cl.: **H10F39/00** (20250101); **H04N25/59** (20230101)

U.S. Cl.:

CPC **H10F39/802** (20250101); **H04N25/59** (20230101); **H10F39/80377** (20250101); **H10F39/813** (20250101);

Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION [0001] This patent document is a continuation of U.S. patent application Ser. No. 17/858,665, filed Jul. 6, 2022, which claims the priority and benefits of Korean patent application No. 10-2021-0142106, filed on Oct. 22, 2021, the disclosures of which are incorporated by reference in their entireties as part of the disclosure of this patent document.

TECHNICAL FIELD
[0002] The technology and implementations disclosed in this patent document generally relate to an image sensing device.
BACKGROUND
[0003] An image sensing device is a device for capturing optical images by converting light into electrical signals using a photosensitive semiconductive material which reacts to light. With the development of automotive, medical, computer and communication industries, the demand for high-performance image sensing devices is increasing in various fields such as smart phones, digital cameras, game machines, IoT (Internet of Things), robots, security cameras and medical micro cameras.
[0004] The image sensing device may be roughly divided into CCD (Charge Coupled Device) image sensing devices and CMOS (Complementary Metal Oxide Semiconductor) image sensing devices. The CCD image sensing devices offer a better image quality, but they tend to consume more power and are larger as compared to the CMOS image sensing devices. The CMOS image sensing devices are smaller in size and consume less power than the CCD image sensing devices. Furthermore, CMOS sensors are fabricated using the CMOS fabrication technology, and thus photosensitive elements and other signal processing circuitry can be integrated into a single chip, enabling the production of miniaturized image sensing devices at a lower cost. For these reasons, CMOS image sensing devices are being developed for many applications including mobile devices.
SUMMARY
[0005] Various embodiments of the disclosed technology relate to an image sensing device capable of adjusting a conversion gain.
[0006] In accordance with an embodiment of the disclosed technology, an image sensing device may include a pixel array of a plurality of unit pixels arranged in a row direction and a column direction and including a first unit pixel that includes a first floating diffusion region configured to store photocharge generated within the first unit pixel in corresponding to incident light, a first gain conversion transistor connected to the first floating diffusion region, a first row booster block connected to the first gain conversion transistor and a second gain conversion transistor that is included in a second unit pixel adjacent to the first unit pixel in the row direction, and a first column booster block connected to the first gain conversion transistor and a third gain conversion transistor that is included in a third unit pixel adjacent to the first unit pixel in the column direction.
[0007] In some implementations, the first column booster block is configured to receive a first horizontal column booster signal commonly applied to a plurality of column booster blocks respectively included in the plurality of unit pixels adjacent to each other in the row direction and a

first vertical column booster signal commonly applied to a plurality of column booster blocks respectively included in the plurality of unit pixels adjacent to each other in the column direction.
[0008] In some implementations, the first row booster block is configured in a manner that a first row booster signal is commonly applied to a plurality of row booster blocks respectively included in the plurality of unit pixels adjacent to each other in the column direction.
[0009] In some implementations, in response to the first horizontal column booster signal having an activation voltage and the first vertical column booster signal having an activation voltage, the first column booster block electrically interconnects the first gain conversion transistor and the third gain conversion transistor.
[0010] In some implementations, in response to the first row booster signal having an activation voltage, the first row booster block electrically interconnects the first gain conversion transistor and the second gain conversion transistor.
[0011] In some implementations, the first column booster block includes a first horizontal column booster transistor configured to receive the first horizontal column booster signal as an input and a first vertical column booster transistor configured to receive the first vertical column booster signal as an input, wherein one end of the first horizontal column booster transistor is connected to one end of the first vertical column booster transistor.
[0012] In some implementations, the first horizontal column booster transistor includes a first drain region and a first source region, the first vertical column booster transistor includes a second drain region and a second source region and the first drain region and the second source region are identical to each other.
[0013] In some implementations, the first unit pixel includes four photoelectric conversion elements each of the photoelectric conversion elements is connected to the first floating diffusion region and the photoelectric conversion elements are arranged in a (2×2) matrix array.
[0014] In some implementations, capacitance of the first row booster block or the first column booster block is smaller than capacitance of the first gain conversion transistor, the second gain conversion transistor, or the third gain conversion transistor.
[0015] In some implementations, the second unit pixel includes a second floating diffusion region and the second floating diffusion region is connected to the second gain conversion transistor.
[0016] In some implementations, the third unit pixel includes a third floating diffusion region, wherein the third floating diffusion region is connected to the third gain conversion transistor.
[0017] In some implementations, the first gain conversion transistor and the second gain conversion transistor are configured to receive the same signal as an input.
[0018] In accordance with another embodiment of the disclosed technology, an image sensing device may include a plurality of unit pixels arranged in a row direction and a column direction of a pixel array, wherein the plurality of unit pixels includes a first unit pixel that includes a first signal block including a plurality of elements and configured to output a first pixel signal corresponding to incident light, and a first connection block configured to connect the first signal block with one or more signal blocks included in other unit pixels than the first unit pixel based on control signals applied to the first connection block, and wherein a number of the one or more signal blocks connected to the first signal block depends on the control signals.
[0019] In some other implementations, the first connection block is configured to connect a second signal block included in a second unit pixel adjacent to the first unit pixel in a row direction to the first signal block, and configured to connect a third signal block included in a third unit pixel adjacent to the first unit pixel in a column direction to the first signal block.
[0020] In some other implementations, the first connection block includes a first row booster block through which a second signal block included in a second unit pixel adjacent to the first unit pixel in a row direction is connected to the first signal block and a first column booster block through which a third signal block included in a third unit pixel adjacent to the first unit pixel in a column direction is connected to the first signal block.

[0021] In some other implementations, the control signals include a first horizontal column booster signal and a first vertical column booster signal that allow, when both activated, the first signal block to be connected to the third signal block.
[0022] In some other implementations, the control signals include a first row booster signal that allows, when activated, the first signal block to be connected with the second signal block.
[0023] In some other implementations, the first row booster signal is applied to the first row booster block included in the first unit pixel and a row booster block included in another unit pixels adjacent to the first unit pixel in the column direction.
[0024] In some other implementations, the plurality of elements includes a photoelectric conversion region configured to generate photocharges in response to the incident light, and a floating diffusion region configured to receive the photocharges and store the photocharges.
[0025] In some other implementations, the floating diffusion region has capacitances that depend on the number of the one or more signal blocks connected to the first signal block.
[0026] It is to be understood that both the foregoing general description and the following detailed description of the disclosed technology are illustrative and explanatory and are intended to provide further explanation of the disclosure as claimed.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0027] The above and other features and beneficial aspects of the disclosed technology will become readily apparent with reference to the following detailed description when considered in conjunction with the accompanying drawings.
[0028] FIG. **1** is a block diagram illustrating an example of an image sensing device based on some implementations of the disclosed technology.
[0029] FIG. **2** is an example of an equivalent circuit illustrating a portion of a pixel array based on some implementations of the disclosed technology.
[0030] FIG. **3** is an example of an equivalent circuit illustrating an example of a unit pixel based on some other implementations of the disclosed technology.
[0031] FIG. **4** is a cross-sectional view illustrating an example of a first column booster block based on some implementations of the disclosed technology.
[0032] FIG. **5** is a cross-sectional view illustrating an example of a first row booster block based on some implementations of the disclosed technology.
[0033] FIG. **6** is a diagram illustrating tables for explaining a method for adjusting a conversion gain of a floating diffusion region based on some implementations of the disclosed technology.
[0034] FIG. **7** is a diagram illustrating a difference in conversion gain between unit pixels based on some implementations of the disclosed technology.
DETAILED DESCRIPTION
[0035] This patent document provides implementations and examples of image sensing device designs that may be used in configurations to substantially address one or more technical or engineering issues and to mitigate limitations or disadvantages encountered in some other image sensing device designs. Some implementations of the disclosed technology relate to an image sensing device which can adjust a conversion gain. The disclosed technology provides the image sensing device which can sufficiently acquire a conversion gain of a floating diffusion region included in each unit pixel while miniaturizing the unit pixel. The disclosed technology provides the image sensing device which can obtain a high dynamic range (HDR) image by adjusting a conversion gain of the floating diffusion region.
[0036] Reference will now be made in detail to certain embodiments, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be

used throughout the drawings to refer to the same or similar parts. In the following description, a detailed description of related known configurations or functions incorporated herein will be omitted to avoid obscuring the subject matter. However, it should be understood that the disclosed technology is not limited to specific embodiments, but includes various modifications, equivalents and/or alternatives of the embodiments.

[0037] Hereafter, various embodiments will be described with reference to the accompanying drawings. However, it should be understood that the disclosed technology is not limited to specific embodiments, but includes various modifications, equivalents and/or alternatives of the embodiments. The embodiments of the disclosed technology may provide a variety of effects capable of being directly or indirectly recognized through the disclosed technology.

[0038] FIG. **1** is a block diagram illustrating an image sensing device **100** based on some implementations of the disclosed technology.

[0039] Referring to FIG. **1**, the image sensing device **100** may include a pixel array **110**, a row driver **120**, a correlated double sampler (CDS) **130**, an analog-digital converter (ADC) **140**, an output buffer **150**, a column driver **160**, and a timing controller **170**. The components of the image sensing device **100** illustrated in FIG. **1** are discussed by way of example only, and this patent document encompasses numerous other changes, substitutions, variations, alterations, and modifications.

[0040] The pixel array **110** may include a plurality of unit pixels arranged in rows and columns. In one example, the plurality of unit imaging pixels can be arranged in a two dimensional pixel array including rows and columns.

[0041] In another example, the plurality of unit imaging pixels can be arranged in a three dimensional pixel array. The plurality of unit pixels may convert an optical signal into an electrical signal on a unit pixel basis or a pixel group basis, where unit pixels in a pixel group share at least certain internal circuitry.

[0042] The pixel array **110** may receive driving signals, including a row selection signal, a pixel reset signal and a transmission signal, from the row driver **120**. Upon receiving the driving signal, corresponding pixels in the pixel array **110** may be activated to perform the operations corresponding to the row selection signal, the pixel reset signal, and the transmission signal.

[0043] The row driver **120** may activate the pixel array **110** to perform certain operations on the pixels in the corresponding row based on commands and control signals provided by controller circuitry such as the timing controller **170**. In some implementations, the row driver **120** may select one or more pixels arranged in one or more rows of the pixel array **110**. The row driver **120** may generate a row selection signal to select one or more rows among the plurality of rows.

[0044] The row driver **120** may sequentially enable the pixel reset signal for resetting imaging pixels corresponding to at least one selected row, and the transmission signal for the pixels corresponding to the at least one selected row. Thus, a reference signal and an image signal, which are analog signals generated by each of the imaging pixels of the selected row, may be sequentially transferred to the CDS **130**. The reference signal may be an electrical signal that is provided to the CDS **130** when a sensing node of a pixel (e.g., a node connected to a floating diffusion node) is reset, and the image signal may be an electrical signal that is provided to the CDS **130** when photocharges generated by the pixel are accumulated in the sensing node. The reference signal indicating unique reset noise of each pixel and the image signal indicating the intensity of incident light may be generically called a pixel signal as necessary.

[0045] CMOS image sensors may use the correlated double sampling (CDS) to remove undesired offset values of pixels known as the fixed pattern noise by sampling a pixel signal twice to remove the difference between these two samples. In one example, the correlated double sampling (CDS) may remove the undesired offset value of pixels by comparing pixel output voltages obtained before and after photocharges generated by incident light are accumulated in the sensing node so that only pixel output voltages based on the incident light can be measured. In some embodiments

of the disclosed technology, the CDS **130** may sequentially sample and hold voltage levels of the reference signal and the image signal, which are provided to each of a plurality of column lines from the pixel array **110**. That is, the CDS **130** may sample and hold the voltage levels of the reference signal and the image signal which correspond to each of the columns of the pixel array **110**.

[0046] In some implementations, the CDS **130** may transfer the reference signal and the image signal of each of the columns as a correlate double sampling signal to the ADC **140** based on control signals from the timing controller **170**.

[0047] The ADC **140** is used to convert analog CDS signals into digital signals. In some implementations, the ADC **140** may be implemented as a ramp-compare type ADC. The ramp-compare type ADC may include a comparator circuit for comparing the analog pixel signal with a reference signal such as a ramp signal that ramps up or down, and a timer for counting until a voltage of the ramp signal matches the analog pixel signal. In some embodiments of the disclosed technology, the ADC **140** may convert the correlate double sampling signal generated by the CDS **130** for each of the columns into a digital signal, and output the digital signal. The ADC **140** may perform a counting operation and a computing operation based on the correlate double sampling signal for each of the columns and a ramp signal provided from the timing controller **170**. In this way, the ADC **140** may eliminate or reduce noises such as reset noise arising from the imaging pixels when generating digital image data.

[0048] The ADC **140** may include a plurality of column counters. Each column of the pixel array **110** is coupled to a column counter, and image data can be generated by converting the correlate double sampling signals received from each column into digital signals using the column counter. In another embodiment of the disclosed technology, the ADC **140** may include a global counter to convert the correlate double sampling signals corresponding to the columns into digital signals using a global code provided from the global counter.

[0049] The output buffer **150** may temporarily hold the column-based image data provided from the ADC **140** to output the image data. In one example, the image data provided to the output buffer **150** from the ADC **140** may be temporarily stored in the output buffer **150** based on control signals of the timing controller **170**. The output buffer **150** may provide an interface to compensate for data rate differences or transmission rate differences between the image sensing device **100** and other devices.

[0050] The column driver **160** may select a column of the output buffer upon receiving a control signal from the timing controller **170**, and sequentially output the image data, which are temporarily stored in the selected column of the output buffer **150**. In some implementations, upon receiving an address signal from the timing controller **170**, the column driver **160** may generate a column selection signal based on the address signal and select a column of the output buffer **150**, outputting the image data from the selected column of the output buffer **150** as an output signal.

[0051] The timing controller **170** may control operations of at least one of the row driver **120**, the ADC **140**, the output buffer **150**, and the column driver **160**.

[0052] The timing controller **170** may provide the row driver **120**, the CDS **130**, the ADC **140**, the output buffer **150**, and the column driver **160** with a clock signal required for the operations of the respective components of the image sensing device **100**, a control signal for timing control, and address signals for selecting a row or column. In an embodiment of the disclosed technology, the timing controller **170** may include a logic control circuit, a phase lock loop (PLL) circuit, a timing control circuit, a communication interface circuit and others.

[0053] FIG. **2** is an example of an equivalent circuit illustrating a portion of a pixel array **110** based on some implementations of the disclosed technology.

[0054] FIG. **2** illustrates the connection relationship between a plurality of unit pixels PX**11**, PX**12**, PX**21**, and PX**22** and constituent elements respectively included in the plurality of unit pixels PX**11**, PX**12**, PX**21**, and PX**22**.

[0055] The plurality of unit pixels PX**11**, PX**12**, PX**21**, and PX**22** may be disposed adjacent to each other in row and column directions of the pixel array **110**.
[0056] Referring to FIG. **2**, a unit pixel located at a first-row-and-first-column position of the pixel array may be referred to as a first unit pixel PX**11**. A unit pixel located at a first-row-and-second-column position of the pixel array while being adjacent to the first unit pixel PX**11** in the row direction may be referred to as a second unit pixel PX**12**. A unit pixel located at a second-row-and-first-column position of the pixel array while being adjacent to the first unit pixel PX**11** in the column direction may be referred to as a third unit pixel PX**21**. In addition, a unit pixel located at a second-row-and-second-column position of the pixel array may be referred to as a fourth unit pixel PX**22**.
[0057] Unit pixels included in the pixel array, which include the first unit pixel PX**11** to the fourth unit pixels PX**22**, may have the same structure as one another and may include the same elements. Thus, the description provided for the first unit pixel PX**11** can be applied to other unit pixels as well. Redundant descriptions will herein be omitted.
[0058] The first unit pixel PX**11** may include a first photoelectric conversion region PD**11** that converts light into photocharge, a first transfer transistor TX**11** coupled to the PD**11** to transfer the photocharge out of the PD**11** to be stored in a first floating diffusion region FD**11**, a first gain conversion transistor DCGX**11** coupled to the FD**11** to produce the pixel output, a first drive transistor DX**11**, and a first selection transistor SX**11**. The first unit pixel PX**11** may include a first row booster block RB**11** and a first column booster block CB**11**.
[0059] A block including the first photoelectric conversion region PD**11**, the first transfer transistor TX**11**, the first floating diffusion region FD**11**, the first gain conversion transistor DCGX**11**, the first drive transistor DX**11**, and the first selection transistor SX**11** may be referred to as a first signal block. In addition, a block including the first row booster block RB**11** and the first column booster block CB**11** may be referred to as a first connection block. The first unit pixel PX**11** may include a first signal block and a first connection block.
[0060] The first photoelectric conversion region PD**11** may generate photocharges corresponding to incident light. The first photoelectric conversion region PD**11** may include an organic or inorganic photodiode. In some implementations, the first photoelectric conversion region PD**11** may include a photosensitive element such as a photogate in addition to a photodiode. In some implementations, the first photoelectric conversion region PD**11** may include a plurality of impurity regions vertically stacked in the semiconductor substrate.
[0061] The first transfer transistor TX**11** may transmit photocharges generated in the first photoelectric conversion region PD**11** to the first floating diffusion region FD**11** according to the first transmission signal TS**11** applied to the first transfer transistor TX**11**.
[0062] For example, the first transmission signal TS**11** may have a voltage of an activation level, which is referred to as an activation voltage, or a voltage of a deactivation level, which is referred to as a deactivation voltage. When the first transmission signal TS**11** having an activation voltage is applied to the first transfer transistor TX**11**, photocharges may move from the first photoelectric conversion region PD**11** to the first floating diffusion region FD**11**.
[0063] The first floating diffusion region FD**11** may receive photocharges generated in the first photoelectric conversion region PD**11**, and may store the received photocharges. The first floating diffusion region FD**11** may be an element having a predetermined capacitance.
[0064] A conversion gain of the first floating diffusion region FD**11** may vary depending on the capacitance of the first floating diffusion region FD**11**.
[0065] The conversion gain may refer to a gain obtained when photocharges focused on the floating diffusion region is converted into a voltage. As the capacitance of a node corresponding to the floating diffusion region increases, a conversion gain of the floating diffusion region may decrease. The capacitance of the node corresponding to the floating diffusion region may be equal to the sum of capacitances of devices connected to the floating diffusion region.

[0066] In some implementations, in the high-illuminance operating environment in which a large amount of photocharges generates in a photoelectric conversion region, the operation voltage range of the image sensing device may expand only when the capacitance of the floating diffusion region is large and the conversion gain is low.
[0067] In addition, in the low-illuminance operating environment in which a small amount of photocharges generates, a pixel signal corresponding to a small amount of incident light can be easily output only when the capacitance of the floating diffusion region is small and the conversion gain is large.
[0068] The capacitance of the floating diffusion region may be equal to the sum of total capacitances of the devices connected to the floating diffusion region.
[0069] The first drive transistor DX**11** may amplify a voltage signal corresponding to photocharges stored in the first floating diffusion region FD**11** to generate the first pixel signal PS**11**.
[0070] The generated first pixel signal PS**11** may be output through the first selection transistor SX**11**. Whether to output the first pixel signal PS**11** may be determined according to the voltage level of the first selection signal SS**11** applied to the first selection transistor SX**11**.
[0071] The first floating diffusion region FD**11** may be connected to one end of the first reset transistor RX**11**, and the pixel voltage VDD may be connected to the other end of the first reset transistor RX**11**.
[0072] Devices included in the first unit pixel PX**11** may be reset to the pixel voltage VDD according to a voltage level of the first reset signal RS**11** applied to the first reset transistor RX**11**.
[0073] For example, when the first reset signal RS**11** has an activation voltage, the first photoelectric conversion region PD**11**, the first transfer transistor TS**11**, the first floating diffusion region FD**11**, and the first gain conversion transistor DCGX**11**, which are included in the first unit pixel PX**11**, may be reset to the pixel voltage VDD.
[0074] At a timing point where the first reset signal RS**11** has an activation voltage, the first transmission signal TS**11**, the first selection signal SS**11**, and the first gain conversion signal DCGS**11** may have an activation voltage.
[0075] One end of the first gain conversion transistor DCGX**11** may be connected to the first floating diffusion region FD**11**, and the other end of the first gain conversion transistor DCGX**11** may be connected to the first row booster block RB**11** and the first column booster block CB**11**.
[0076] The first gain conversion transistor DCGX**11** may have a predetermined capacitance. In some implementations, the capacitance of the first gain conversion transistor DCGX**11** may be the same as the capacitance of the first floating diffusion region FD**11**.
[0077] The sum of capacitances of the devices connected to the first floating diffusion region FD**11** may be changed according to the voltage level of the first gain conversion signal DCGS**11** applied to the first gain conversion transistor DCGX**11**.
[0078] For example, when the first gain conversion signal DCGS**11** has an activation voltage, the first floating diffusion region FD**11** and the first gain conversion transistor DCGX**11** are connected to each other, and the capacitance of the node corresponding to the first floating diffusion region FD**11** may increase. Accordingly, the amount of photocharges capable of being stored in the first floating diffusion region FD**11** can increase.
[0079] Therefore, when the image sensing device operates in the high-illuminance environment, the image sensing device receives the first gain conversion signal DCGS**11** having an activation voltage, so that the number of devices connected to the first floating diffusion region FD**11** may increase. As the number of devices connected to the first floating diffusion region FD**11** increases, the capacitance of the node corresponding to the first floating diffusion region FD**11** may increase.
[0080] The first row booster block RB**11** may connect the first gain conversion transistor DCGX**11** included in the first unit pixel PX**11** to the second gain conversion transistor DCGX**12** included in the second unit pixel PX**12** that is adjacent to the first unit pixel PX**11** in the row direction.
[0081] As the first gain conversion transistor DCGX**11** and the second gain conversion transistor

DCGX**12** are connected through the first row booster block RB**11**, the first gain conversion transistor DCGX**11**, the second gain conversion transistor DCGX**12**, and the second floating diffusion region FD**12** are connected to the first floating diffusion region FD**11**.
[0082] When the first row booster signal RBS**1** applied to the first row booster block RB**11** has an activation voltage, gain conversion transistors respectively included in unit pixels that are adjacent to each other in the row direction may be connected to each other. The number of devices connected to the floating diffusion region can be adjusted by controlling whether to connect the gain conversion transistors to each other.
[0083] For convenience of description, it is assumed that the first row booster block RB**11** has a small capacitance that can be negligible compared to capacitances of the floating diffusion regions or capacitances of the gain conversion transistors.
[0084] In some implementations, the gain conversion signals applied to the gain conversion transistors respectively included in the unit pixels adjacent to each other in the row direction may be identical to each other. The signals applied to the gain conversion transistors respectively included in the unit pixels adjacent to each other in the row direction may be equal to each other.
[0085] For example, the first gain conversion signal DCGS**11** applied to the first gain conversion transistor DCGX**11** included in the first unit pixel PX**11** may be the same signal as the second gain conversion signal DCGS**12** applied to the second gain conversion transistor DCGX**12** included in the second unit pixel PX**12**.
[0086] When each of the first gain conversion signal DCGS**11** and the second gain conversion signal DCGS**12** has an activation voltage and the first row booster signal RBS**1** has an activation voltage, the first floating diffusion region FD**11**, the first gain conversion transistor DCGX**11**, the second gain conversion transistor DCGX**12**, and the second floating diffusion region FD**12** may be connected to one another.
[0087] For convenience of explanation, it may be assumed that the first floating diffusion region FD**11**, the first gain conversion transistor DCGX**11**, the second gain conversion transistor DCGX**12**, and the second floating diffusion region FD**12** have the same capacitance. However, the scope of the disclosed technology is not limited thereto. Thus, in some implementations, the first floating diffusion region FD**11**, the first gain conversion transistor DCGX**11**, the second gain conversion transistor DCGX**12**, and the second floating diffusion region FD**12** have different capacitances from one another.
[0088] When the above-described devices are connected through the first row booster block RB**11**, the total capacitance of the first floating diffusion region FD**11** may be four times the capacitance of the first floating diffusion region FD**11** when the first gain conversion signal DCGS**11** and the second gain conversion signal DCGS**12** does not have an activation voltage.
[0089] The row booster signals applied to the row booster blocks respectively included in the unit pixels arranged in the same column in the pixel array may be equal to each other. Thus, the row booster signal lines connected to the row booster blocks respectively included in the unit pixels arranged in the same column may be equal to each other.
[0090] For example, the signal applied to the first row booster block RB**11** included in the first unit pixel PX**11** may be the same as the signal applied to the third row booster block RB**21** included in the third unit pixel PX**21**, and the signal may be referred to as the first row booster signal RBS**1**. The row booster blocks included in the unit pixels arranged in the same column from among the unit pixels arranged in the pixel array can be activated or deactivated at the same time.
[0091] The first column booster block CB**11** may connect the first gain conversion transistor DCGX**11** included in the first unit pixel PX**11** to the third gain conversion transistor DCGX**21** included in the third unit pixel PX**21** adjacent to the first unit pixel PX**11** in the column direction.
[0092] As the first gain conversion transistor DCGX**11** and the third gain conversion transistor DCGX**21** are connected through the first column booster block CB**11**, the first gain conversion transistor DCGX**11**, the third gain conversion transistor DCGX**21**, and the third floating diffusion

region FD**21** may be connected to the first floating diffusion region FD**11**.
[0093] The first column booster block CB**11** may receive a first horizontal column booster signal CBSR**1** and a first vertical column booster signal CBSC**1**.
[0094] When both the first horizontal column booster signal CBSR**1** and the first vertical column booster signal CBSC**1** have an activation voltage, gain conversion transistors respectively included in unit pixels that are adjacent to each other in the column direction may be connected to each other. By controlling the connections of the gain conversion transistors such that the gain conversion transistors of the unit pixels are connected or not connected, the number of devices connected to the floating diffusion region in one unit pixel can be adjusted, and the capacitance of the floating diffusion region in the unit pixel can also be adjusted.
[0095] In some implementations, the first column booster block CB**11** may have a small capacitance that may be negligible compared to capacitances of the floating diffusion regions or capacitances of the gain conversion transistors.
[0096] When each of the first and third gain conversion signals DCGS**11** and DCGS**21** has an activation voltage, and each of the first horizontal column booster signal CBSR**1** and the first vertical column booster signal CBSC**1** has an activation voltage, the first floating diffusion region FD**11**, the first gain conversion transistor DCGX**11**, the third gain conversion transistor DCGX**21**, and the third floating diffusion region FD**21** may be connected to each other.
[0097] The first column booster block CB**11** may interconnect the first gain conversion transistor DCGX**11** and the third gain conversion transistor DCGX**21** only when each of the first horizontal column booster signal CBSR**1** and the first vertical column booster signal CBSC**1** has an activation voltage.
[0098] In some implementations, the first floating diffusion region FD**11**, the first gain conversion transistor DCGX**11**, the third gain conversion transistor DCGX**21**, and the third floating diffusion region FD**21** may have the same capacitance. Therefore, when the devices are connected by the first column booster block CB**11**, total capacitance of the first floating diffusion region FD**11** may be increased by four times compared to a case where the above-described devices are not interconnected by the first column booster block CB**11**.
[0099] The horizontal column booster signals applied to the column booster blocks respectively included in the unit pixels arranged in the same row in the pixel array may be equal to each other. Thus, the horizontal column booster signals applied to the column booster blocks respectively included in the unit pixels adjacent to each other in the row direction may be equal to each other.
[0100] As shown in FIG. **2**, the first horizontal column booster signal CBSR**1** may be commonly applied not only to the first column booster block CB**11** included in the first unit pixel PX**11**, but also to the second column booster block CB**12** included in the second unit pixel PX**12** arranged in the same row as the first unit pixel PX**11**. The column booster signal may be commonly applied to the plurality of column booster blocks respectively included in the plurality of unit pixels adjacent to each other in the row direction.
[0101] The vertical column booster signals applied to the column booster blocks respectively included in the unit pixels arranged in the same column in the pixel array may be equal to each other. The vertical column booster signals applied to the column booster blocks respectively included in the plurality of unit pixels adjacent to each other in the column direction may be equal to each other.
[0102] As shown in FIG. **2**, the first vertical column booster signal CBSC**1** may be commonly applied not only to the first column booster block CB**11** included in the first unit pixel PX**11**, but also to the third column booster block CB**21** included in the third unit pixel PX**21** that is adjacent to the first unit pixel PX**11** in the column direction and arranged in the same column as in the first unit pixel PX**11**. Thus, a column booster signal may be commonly applied to the column booster blocks respectively included in the unit pixels adjacent to each other in the column direction.
[0103] In a situation where the column booster block is in contact with one signal line applying the

same horizontal column booster signal to column booster blocks arranged in the row direction and the other signal line applying the same vertical column booster signal to column booster blocks arranged in the column direction, only when signals received through the two signal lines have an activation voltage, the column booster block can interconnect two gain conversion transistors that are adjacent to each other in the column direction, so that the column booster blocks respectively included in different unit pixels can be independently activated.

[0104] The activation of the column booster block may allow gain conversion transistors connected to both ends of the column booster to be electrically connected to each other.

[0105] For example, when both the first horizontal column booster signal CBSR**1** and the first vertical column booster signal CBSR**1** have an activation voltage, the first column booster block CB**11** included in the first unit pixel PX**11** may be activated so that the first gain conversion transistor DCGX**11** and the third gain conversion transistor DCGX**21** can be connected to each other.

[0106] Although the first column booster block CB**11** is activated, when the signal CBSC**2** applied to the other signal line connected to the second column booster block CB**12** included in the second unit pixel PX**12** does not have an activation voltage, the second column booster block CB**12** included in the second unit pixel may not be activated, and thus the second gain conversion transistor DCGX**12** and the fourth gain conversion transistor DCGX**22** may not be connected to each other.

[0107] Although the first column booster block CB**11** is activated, when the signal CBSR**2** applied to the other signal line connected to the third column booster block CB**21** included in the third unit pixel PX**21** does not have an activation voltage, the third column booster block CB**21** included in the third unit pixel may not be activated, and the third gain conversion transistor DCGX**21** and the other gain conversion transistor may not be connected to each other.

[0108] In some implementations, the unit pixel may include a row booster block for interconnecting gain conversion transistors respectively included in unit pixels adjacent to each other in a row direction, and a column booster block for interconnecting gain conversion transistors respectively included in unit pixels adjacent to each other in a column direction, thereby adjusting the number of devices connected to the floating diffusion region included in each unit pixel.

[0109] By adjusting the number of devices to be connected to the floating diffusion region, the conversion gain of the floating diffusion region can be adjusted, and images corresponding to the operation environment having various illuminance levels can be detected.

[0110] In addition, the image sensing device according to the disclosed technology may control the number of devices (e.g., the floating diffusion region or the gain conversion transistor of another unit pixel) to be connected to the floating diffusion region for each unit pixel so that the floating diffusion regions included in the unit pixels in the pixel array may have different conversion gains.

[0111] The image sensing device according to the disclosed technology can obtain an HDR image by performing image capture only once (i.e., one photographing action). The HDR image may generally refer to an image generated when a plurality of pixel signals for the environment having different illuminances is acquired and the acquired pixel signals are then synthesized and calculated.

[0112] The image sensing device according to the disclosed technology can adjust the floating diffusion regions respectively included in the unit pixels in the pixel array so that the floating diffusion regions can have different conversion gains, thereby acquiring pixel signals corresponding to the environment having different illuminances by only one photographing action.

[0113] The image sensing device may generate an HDR image by synthesizing and calculating image data based on the pixel signal.

[0114] FIG. **3** is an example of an equivalent circuit illustrating a unit pixel based on some other implementations of the disclosed technology.

[0115] In the example of FIG. **3**, the unit pixel may be disposed in the pixel array. The unit pixel as

shown in FIG. **3** has different structures from the first to fourth unit pixels PX**11**, PX**12**, PX**21**, and PX**22** shown in FIG. **2** as discussed above.

[0116] The unit pixel may include four photoelectric conversion regions (PDa, PDb, PDc, PDd), four transfer transistors (TXa, TXb, TXc, TXd), a floating diffusion region FD, a drive transistor DX, a selection transistor SX, a reset transistor RX, a gain conversion transistor DCGX, a row booster block RB, and a column booster block CB.

[0117] The floating diffusion region FD, the drive transistor DX, the selection transistor SX, the reset transistor RX, the gain conversion transistor DCGX, the row booster block RB, and the column booster block CB shown in FIG. **3** are substantially the same as those described above with reference to FIG. **2**, so that the above-described constituent elements shown in FIG. **3** will hereinafter be described centering upon the photoelectric conversion regions PDa, PDb, PDc, and PDd and the transfer transistors TXa, TXb, TXc, and TXd.

[0118] The photoelectric conversion regions PDa, PDb, PDc, and PDd may be connected to the transfer transistors TXa, TXb, TXc, and TXd, respectively. In addition, the transfer transistors TXa, TXb, TXc, and TXd may be connected to the floating diffusion region FD.

[0119] According to another embodiment, the photoelectric conversion regions PDa, PDb, PDc, and PDd included in the unit pixel may share the floating diffusion region FD, the drive transistor DX, the selection transistor SX, the reset transistor RX, the gain conversion transistor DCGX, the row booster block RB, and the column booster block CB.

[0120] The transmission signals TSa, TSb, TSc, and TSd respectively applied to the transfer transistors TXa, TXb, TXc, and TXd may be activated at different timing points from one another, so that the pixel signal PS corresponding to photocharges generated in each of the photoelectric conversion regions PDa, PDb, PDc, and PDd can be output.

[0121] In some implementations, when photocharges generated in each of the photoelectric conversion regions PDa, PDb, PDc, and PDd are transmitted to the floating diffusion region FD, each of the transmission signals TSa, TSb, TSc, and TSd may exclusively have an activation voltage. In some implementations, any two of the transmission signals TSa, TSb, TSc, and TSd do not overlap each other.

[0122] Since the plurality of photoelectric conversion regions PDa, PDb, PDc, and PDd is connected to one floating diffusion region FD, the number of transistors included in one unit pixel may decrease and the degree of freedom in a pixel layout can increase. In addition, a region where photoelectric conversion regions and transistors can be disposed may be secured.

[0123] FIG. **4** is a cross-sectional view illustrating an example of the first column booster block CB**11** based on some implementations of the disclosed technology.

[0124] Although FIG. **4** is a cross-sectional view of the first column booster block CB**11**, other column booster blocks (e.g., CB**12**, CB**21**, CB**22**) shown in FIG. **2** may have the same cross-section as the first column booster block CB**11**.

[0125] The first column booster block CB**11** may have a dual gate MOSFET structure. The dual gate MOSFET may include two gates, and a drain region included in one transistor may be used as a source region of another transistor.

[0126] The first column booster block CB**11** may be formed over the semiconductor substrate **400**. The semiconductor substrate **400** may include a silicon substrate doped with impurities or an epitaxial layer doped with impurities. For example, the semiconductor substrate **400** may be doped with P-type impurities.

[0127] The first column booster source region **411** may be formed over the semiconductor substrate **400**, and may be a region doped with conductive-type impurities different from those of the semiconductor substrate **400**. For example, the first column booster source region **411** may be a region doped with N-type impurities.

[0128] The first column booster channel region **412** may be formed to contact the first column booster source region **411**, and may be a region doped with the same conductivity-type impurities

as those of the first column booster source region **411**. The first column booster channel region **412** may be doped at a lower density than the first column booster source region **411**.
[0129] The first column booster drain region **413** may be doped with the same conductive-type impurities as the first column booster source region **411**. In addition, the first column booster drain region **413** may be doped at the same density as the first column booster source region **411**.
[0130] The second column booster channel region **414** may be formed to contact the first column booster drain region **413**, and the second column booster channel region **414** may be doped with the same conductivity-type impurities as the first column booster drain region **413**. The second column booster channel region **414** may be doped at a lower density than the first column booster drain region **414**.
[0131] The second column booster drain region **415** may be doped with impurities of the same conductivity type as the first column booster drain region **413**. The second column booster drain region **415** may be doped at the same density as in the first column booster drain region **413**.
[0132] A column booster insulation layer **420** may be formed over the source regions, the drain regions, and the channel regions. For example, the column booster insulation layer may include an insulation material such as silicon oxide.
[0133] The first column booster terminal **431** formed through the column booster insulation layer **420** may be in contact with the first column booster source region **411**. The first column booster terminal **431** may include a conductive material, for example, metal or polysilicon. The first column booster terminal **431** may extend to one end of the first column booster block CB**11**, and may be connected to the first gain conversion transistor DCGX**11**.
[0134] The first horizontal column booster transistor gate **432** may be formed over the column booster insulation layer **420**, and may include a conductive material. In some implementations, at least a portion of the first horizontal column booster transistor gate **432** may be formed to overlap the first column booster source region **411** and the first column booster drain region **413**.
[0135] A first horizontal column booster signal line may be connected to the first horizontal column booster transistor gate **432**, and the first horizontal column booster signal line can be connected to the first horizontal column booster transistor gate **432** so that the first horizontal column booster signal CBSR**1** can be applied to the first horizontal column booster transistor gate **432**.
[0136] The first vertical column booster transistor gate **433** may be formed over the column booster insulation layer **420**, and may include a conductive material. In some implementations, at least a portion of the first vertical column booster transistor gate **433** may be formed to overlap the first column booster drain region **413** and the second column booster drain region **415**.
[0137] A first vertical column booster signal CBSC**1** may be applied to the first vertical column booster transistor gate **433**, and a first vertical column booster signal line may be connected to the first vertical column booster transistor gate **433** so that the first vertical column booster signal CBSC**1** can be applied to the first vertical column booster transistor gate **433**.
[0138] The second column booster terminal **434** may be formed through the column booster insulation layer **420**, and may be in contact with the second column booster drain region **415**. The second column booster terminal **434** may include a conductive material, for example, a metal material or polysilicon. The second column booster terminal **434** may extend to the other end of the first column booster block CB**11** so that the second column booster terminal **434** can be connected to the third gain conversion transistor DCGX**21**.
[0139] The first column booster block CB**11** according to an embodiment of the disclosed technology may include a first horizontal column booster transistor and a first vertical column booster transistor. The first horizontal column booster transistor may include a first horizontal column booster transistor gate **432**, and the first vertical column booster transistor may include a first vertical column booster transistor gate **433**.
[0140] The first horizontal column booster transistor may include a first column booster source region **411**, a first column booster channel region **412**, and a first column booster drain region **413**.

[0141] When an activation voltage is applied to the first horizontal column booster transistor gate **432**, charges may move from the first column booster source region **411** to the first column booster drain region **413** through the first column booster channel region **412**.
[0142] The first vertical column booster transistor may include a first column booster drain region **413**, a second column booster channel region **414**, and a second column booster drain region **415**. The first column booster drain region **413** may serve as a source region of the first vertical column booster transistor, and may be used as a second column booster source region. When an activation voltage is applied to the first vertical column booster transistor gate **433**, charges may move from the first column booster drain region **413** (i.e., the second source region) to the second column booster drain region **415** through the second column booster channel region **414**.
[0143] When each of the first horizontal column booster signal CBSR**1** and the first vertical column booster signal CBSC**1** has an activation voltage, charges can move between the first column booster terminal **431** and the second column booster terminal **434**, so that the first gain conversion transistor DCGX**11** and the third gain conversion transistor DCGX**21** may be electrically connected to each other.
[0144] The gain conversion transistors adjacent to each other in the column direction are connected to each other only when two column booster signals applied to the column booster block are simultaneously activated, so that connection or non-connection between the gain conversion transistors arranged in the column direction can be selectively determined.
[0145] FIG. **5** is a cross-sectional view illustrating an example of the first row booster block based on some implementations of the disclosed technology.
[0146] Although FIG. **5** exemplarily illustrates the cross-section of the first row booster block RB**11**, other row booster blocks (e.g., RB**12**, RB**21**, RB**22**) shown in FIG. **2** may have the same cross-section as in the first row booster block RB**11**.
[0147] The first row booster block RB**11** may have a MOSFET structure.
[0148] The first row booster block RB**11** may be formed over the semiconductor substrate **500**. The semiconductor substrate **500** may include a silicon substrate doped with impurities or an epitaxial layer doped with impurities. For example, the semiconductor substrate **500** may be a region doped with P-type impurities.
[0149] The row booster source region **511** may be formed over the semiconductor substrate **500**, and may be a region doped with conductivity-type impurities different from those of the semiconductor substrate **500**. For example, the row booster source region **511** may be a region doped with N-type impurities.
[0150] The row booster channel region **512** may be formed to contact the row booster source region **511**, and may be doped with the same conductivity type impurities as those of the row booster source region **511**. The row booster channel region **512** may be doped at a lower density than the row booster source region **511**.
[0151] The row booster drain region **513** may be doped with the same conductivity type impurities as those of the row booster source region **511**. In addition, the row booster drain region **513** may be doped at the same density as the row booster source region **511**.
[0152] A row booster insulation layer **520** may be formed over the source region, the drain region, and the channel region. For example, the row booster insulation layer **520** may include an insulation material such as silicon oxide.
[0153] The first row booster terminal **531** formed through the row booster insulation layer **520** may be formed to contact the row booster source region **511**. The first row booster terminal **531** may include a conductive material, for example, a metal material or polysilicon. The first row booster terminal **531** may extend to one end of the row booster block RB**11**, and may be connected to the first gain conversion transistor DCGX**11**.
[0154] The row booster transistor gate **532** may be formed over the row booster insulation layer **520**, and may include a conductive material. In some implementations, the row booster transistor

gate **532** may be formed to overlap at least a portion of the row booster source region **511** and the row booster drain region **513**.

[0155] A first row booster signal RBS**1** may be applied to the row booster transistor gate **532**, and a first row booster signal line may be connected to the row booster transistor gate **532** so that the first row booster signal RBS**1** can be applied to the row booster transistor gate **532**.

[0156] The second row booster terminal **533** may be formed through the row booster insulation layer **520**, and may be in contact with the row booster drain region **513**. The second row booster terminal **533** may include a conductive material, for example, a metal material or polysilicon. The second row booster terminal **533** may extend to the other end of the first row booster block RB**11** so that the second row booster terminal **533** can be connected to the second gain conversion transistor DCGX**12**.

[0157] The row booster transistor may include a row booster source region **511**, a row booster channel region **512**, and a row booster drain region **513**. When an activation voltage is applied to the row booster transistor gate **532**, charges may move from the row booster source region **511** to the row booster drain region **513** through the row booster channel region **512**.

[0158] When the first row booster signal RBS**1** has an activation voltage, charges may move between the first row booster terminal **531** and the second row booster terminal **533**, and the first gain conversion transistor DCGX**11** and the second gain conversion transistor DCGX**12** may be electrically connected to each other.

[0159] Since the gain conversion transistors adjacent to each other in the row direction are connected to each other only when the row booster signal applied to the row booster block is activated, connection or non-connection between the gain conversion transistors arranged in the row direction can be selectively determined.

[0160] FIG. **6** is a diagram illustrating tables for explaining a method for adjusting a conversion gain of the floating diffusion region based on some implementations of the disclosed technology.

[0161] FIG. **6** illustrates a change in capacitance based on devices connected to the first floating diffusion region FD**11** of the first unit pixel (i.e., PX**11** of FIG. **2**) included in the pixel array described with reference to FIG. **2**.

[0162] For convenience of description, it is assumed that capacitance of the gain conversion transistors is equal to capacitance of the floating diffusion regions, and this capacitance will hereinafter be denoted by C.

[0163] As can be seen from Table 1, when the first column booster block CB**11** is deactivated, the capacitance change of the first floating diffusion region (i.e., FD**11** of FIG. **2**) in response to activation or deactivation of the first row booster block RB**11** and the second row booster block RB**12** may occur. In Table 1, it is assumed that the first gain conversion transistor (DCGX**11** of FIG. **2**) and the second gain conversion transistor (DCGX**12** of FIG. **2**) are activated.

[0164] When the first column booster block CB**11** is deactivated, information as to whether connection or non-connection between devices included in the unit pixels adjacent to the first floating diffusion region FD**11** can be determined based on activation or non-activation of the row booster block RB**11**, RB**12**, or the like.

[0165] For example, when the first row booster block RB**11** and the second row booster block RB**12** are deactivated, the first floating diffusion region FD**11** and the first gain conversion transistor (i.e., DCGX**11** of FIG. **2**) are connected to each other, and capacitance of the first floating diffusion region FD**11** may be denoted by **2**C.

[0166] Also, when the first row booster block RB**11** is activated and the second row booster block RB**12** is deactivated, the second floating diffusion region FD**12** and the second gain conversion transistor DCGX**12** included in the second unit pixel (i.e., PX**12** of FIG. **2**) can be connected to the first floating diffusion region FD**11**. At this time, the sum of capacitances of four devices may be denoted by **4**C.

[0167] Finally, when the first row booster block RB**11** is activated and the second row booster

block RB**12** is deactivated, the first floating diffusion region FD**11** may be formed to contact not only the second floating diffusion region FD**12** and the second gain conversion transistor DCGX**12** included in the second unit pixel PX**12**, but also the floating diffusion region and the gain conversion transistor included in another unit pixel adjacent to the second unit pixel PX**12** in the row direction. At this time, the sum of capacitances of six devices may be denoted by **6**C.

[0168] As can be seen from Table 2, when the first column booster block CB**11** is activated, the capacitance change of the first floating diffusion region FD**11** in response to activation or deactivation of the first row booster block RB**11** and the second row booster block RB**12** may occur. In Table 2, it is assumed that the first gain conversion transistor DCGX**11**, the second gain conversion transistor DCGX**12**, and the third gain conversion transistor DCGX**21** are activated.

[0169] When the first column booster block CB**11** is activated, devices included in the third unit pixel (i.e., PX**21** of FIG. **2**) adjacent to the first unit pixel PX**11** in the column direction can be additionally connected to the first floating diffusion region FD**11**.

[0170] As the devices included in the unit pixels adjacent to each other in the column direction are additionally connected, the first floating diffusion region FD**11** may obtain an additional capacitance. For example, when the first row booster block RB**11** and the second row booster block RB**21** are activated, the capacitance of the first floating diffusion region FD**11** may be denoted by **12**C.

[0171] The image sensing device based on some implementations of the disclosed technology can variably adjust the capacitance of the floating diffusion region according to whether the row booster block and the column booster block are activated. In addition, the devices may be selectively connected to the floating diffusion region, so that the capacitance of the floating diffusion region can be selectively adjusted.

[0172] FIG. **7** is a diagram illustrating a difference in conversion gain between the unit pixels based on some implementations of the disclosed technology.

[0173] FIG. **7** is a diagram for explaining that conversion gains of the unit pixels disposed in the pixel array can be adjusted differently. In more detail, FIG. **7** illustrates the connection relationship between the floating diffusion regions and the gain conversion transistors included in the unit pixels. In some implementations, the pixel signals output from the respective unit pixels can be output at different timing points.

[0174] For convenience of explanation, it is assumed that the gain conversion signals applied to the gain conversion transistors respectively included in the unit pixels PX**11** to PX**44** shown in FIG. **7** are all activated.

[0175] Further, when the unit pixels PX**11** to PX**44** are interconnected by the row booster blocks and the column booster blocks, it can be assumed that the signal blocks TR**11** to TR**44** respectively included in the unit pixels PX**11** to PX**44** are connected to each other.

[0176] FIG. **7** illustrates 16 unit pixels PX**11** to PX**44** constructing a (4×4) matrix array, signals applied to the row booster blocks respectively included in the unit pixels PX**11** to PX**44**, and signals applied to the column booster blocks respectively included in the unit pixels PX**11** to PX**44**.

[0177] Unlike the pixel array of FIG. **2**, the unit pixels included in the pixel array shown in FIG. **7** may have a (4×4) matrix structure. In the (4×4) matrix structure shown in FIG. **7**, a unit pixel PX**11** located at a first-row-and-first-column position may be referred to as a first unit pixel, a unit pixel PX**12** located at a first-row-and-second-column position may be referred to as a second unit pixel, a unit pixel PX**13** located at a first-row-and-third-column position may be referred to as a third unit pixel, and a unit pixel located at a first-row-and-fourth-column position may be referred to as a fourth unit pixel PX**14**.

[0178] Similarly, in the (4×4) matrix structure shown in FIG. **7**, the unit pixels PX**21**, PX**22**, PX**23**, and PX**24** located at the second-row-and-first-column to second-row-and-fourth-column positions may be referred to as the fifth to eighth unit pixels, respectively, and other unit pixels PX**31**, PX**32**, PX**33**, and PX**34** located at the third-row-and-first-column to third-row-and-fourth-column

positions may be referred to as the ninth to twelfth unit pixels, respectively.
[0179] Finally, other unit pixels PX**41**, PX**42**, PX**43**, and PX**44** located at fourth-row-and-first-column to fourth-row-and-fourth-column positions may be referred to as the thirteenth to sixteenth unit pixels, respectively.
[0180] The unit pixels PX**11** to PX**44** may include signal blocks TR**11** to TR**44**, respectively. In addition, each of the unit pixels PX**11** to PX**44** may include a row booster block and a column booster block.
[0181] As shown in FIG. **2**, each of the signal blocks TR**11** to TR**44** may include a photoelectric conversion region, a floating diffusion region, a transfer transistor, a drive transistor, a selection transistor, a reset transistor, etc.
[0182] Referring to FIG. **7**, information as to whether the row booster block and the column booster blocks are activated according to the state of the row booster signal and the state of the column booster signal is displayed. When each of the row booster signal and the column booster signal has an activation voltage, “ACTIVE” may be displayed. When each of the row booster signal and the column booster signal has a deactivation voltage, “DEACTIVE” may be displayed.
[0183] As can be seen from FIG. **7**, the activated row booster block or the activated column booster block may be displayed as “ON”, and the deactivated row booster block or the deactivated column booster block may be displayed as “OFF”.
[0184] Information as to whether the adjacent unit pixels are connected to each other may be determined according to activation or deactivation of the row booster block or the column booster block.
[0185] Referring to FIG. **7**, when the first row booster signal RBS**1** has an activation voltage, the signal blocks TR**11**, TR**21**, TR**31**, and TR**41** respectively included in the unit pixels PX**11**, PX**21**, PX**31**, and PX**41** located in the first column of the pixel array can be connected to the signal blocks TR**21**, TR**22**, TR**23**, and TR**24** respectively included in the unit pixels PX**21**, PX**22**, PX**23**, and PX**24** located in the second column.
[0186] When the column booster blocks are activated, unit pixels adjacent to each other in the column direction may be connected to each other. Information as to whether or not the column booster blocks are activated can be determined according to voltage levels of two column booster signals to be applied to the column booster blocks.
[0187] For example, the first column booster block CB**11** may be activated when each of the first horizontal column booster signal CBSR**1** and the first vertical column booster signal CBSC**1** has an activation voltage, and signal blocks included in unit pixels adjacent to each other in the column direction may be connected to each other.
[0188] When the first column booster block CB**11** included in the first unit pixel PX**11** is activated, the first signal block TR**11** included in the first unit pixel PX**11** and the fifth signal block TR**21** included in the fifth unit pixel PX**21** may be connected to each other.
[0189] Although the column booster blocks are disposed in the same column or the same row, information as to whether the column booster blocks are activated can be determined independently, irrespective of the arrangement position of the column booster blocks.
[0190] For example, as shown in FIG. **7**, when the activation state of the row booster signals RBS**1**, RBS**2**, and RBS**3** and the activation state of the column booster signals CBSR**1**, CBSR**2**, CBSR**3**, CBSR**4**, CBSC**1**, CBSC**2**, CBSC**3**, and CBSC**4** are determined, the first unit pixel PX**11**, the second unit pixel PX**12**, the fifth unit pixel PX**21**, and the sixth unit pixel PX**22** may be connected to each other.
[0191] In addition, the third unit pixel PX**13**, the seventh unit pixel PX**23**, the eleventh unit pixel PX**33**, the twelfth unit pixel PX**34**, the fifteenth unit pixel PX**43**, and the sixteenth unit pixel PX**44** may not be connected to adjacent unit pixels.
[0192] Here, the capacitance of the floating diffusion region included in the first unit pixel PX**11** may be four times the capacitance of the third unit pixel PX**13**.

[0193] As described above, the capacitance of the floating diffusion regions respectively included in the unit pixels may vary depending on the activation state of the column booster blocks and the row booster blocks.
[0194] As described above, an HDR image may generally refer to an image generated when the plurality of pixel signals for the environment having different illuminances is obtained and the obtained signals are then processed and synthesized.
[0195] When the unit pixels in the pixel array have different capacitances, the HDR image can be acquired by only one photographing action.
[0196] In other words, the image sensing device according to the disclosed technology can adjust the floating diffusion regions respectively included in the unit pixels of the pixel array in a manner that the floating diffusion regions have different conversion gains, and can acquire pixel signals corresponding to different illumination environments by only one photographing action.
[0197] The image sensing device may generate an HDR image by synthesizing and calculating image data based on the pixel signal.
[0198] As is apparent from the above description, the image sensing device based on some implementations of the disclosed technology can sufficiently acquire a conversion gain of a floating diffusion region included in each unit pixel while miniaturizing the unit pixel.
[0199] In addition, the image sensing device based on some implementations of the disclosed technology can obtain a high dynamic range (HDR) image by adjusting a conversion gain of the floating diffusion region.
[0200] The embodiments of the disclosed technology may provide a variety of effects capable of being directly or indirectly recognized through the above-mentioned patent document.
[0201] Those skilled in the art will appreciate that the disclosed technology may be carried out in other specific ways than those set forth herein. In addition, claims that are not explicitly presented in the appended claims may be presented in combination as an embodiment or included as a new claim by a subsequent amendment after the application is filed.
[0202] Although a number of illustrative embodiments have been described, it should be understood that modifications and/or enhancements to the disclosed embodiments and other embodiments can be devised based on what is described and/or illustrated in this patent document.

Claims

1. An image sensing device comprising: a plurality of unit pixels arranged in a row direction and a column direction of a pixel array, wherein the plurality of unit pixels includes a first unit pixel that includes: a first signal block including a plurality of elements and configured to output a first pixel signal corresponding to incident light; and a first connection block configured to connect the first signal block with one or more signal blocks included in other unit pixels than the first unit pixel based on control signals applied to the first connection block, and wherein a number of the one or more signal blocks connected to the first signal block depends on the control signals.
2. The image sensing device of claim 1, wherein the first connection block is configured to connect a second signal block included in a second unit pixel adjacent to the first unit pixel in a row direction to the first signal block, and configured to connect a third signal block included in a third unit pixel adjacent to the first unit pixel in a column direction to the first signal block.
3. The image sensing device according to claim 1, wherein the first connection block includes: a first row booster block through which a second signal block included in a second unit pixel adjacent to the first unit pixel in a row direction is connected to the first signal block; and a first column booster block through which a third signal block included in a third unit pixel adjacent to the first unit pixel in a column direction is connected to the first signal block.
4. The image sensing device according to claim 3, wherein the control signals include: a first horizontal column booster signal and a first vertical column booster signal that allow, when both

activated, the first signal block to be connected to the third signal block.
5. The image sensing device according to claim 3, wherein the control signals include a first row booster signal that allows, when activated, the first signal block to be connected with the second signal block.
6. The image sensing device according to claim 5, wherein the first row booster signal is applied to the first row booster block included in the first unit pixel and a row booster block included in another unit pixels adjacent to the first unit pixel in the column direction.
7. The image sensing device according to claim 1, wherein the plurality of elements includes a photoelectric conversion region configured to generate photocharges in response to the incident light, and a floating diffusion region configured to receive the photocharges and store the photocharges.
8. The image sensing device according to claim 7, wherein the floating diffusion region has capacitances that depend on the number of the one or more signal blocks connected to the first signal block.
9. The image sensing device according to claim 7, wherein the photoelectric conversion region includes impurity regions that are vertically stacked in a semiconductor substrate.
10. The image sensing device according to claim 3, wherein the first unit pixel further includes a first gain conversion transistor having a capacitance and configured to provide a pixel output.
11. The image sensing device according to claim 10, wherein the first row booster block is connected to the first gain conversion transistor and a second gain conversion transistor that is included in a second unit pixel adjacent to the first unit pixel in the row direction.
12. The image sensing device according to claim 10, wherein the first column booster block is connected to the first gain conversion transistor and a third gain conversion transistor that is included in a third unit pixel adjacent to the first unit pixel in the column direction.
13. The image sensing device according to claim 10, wherein capacitance of the first row booster block or the first column booster block is smaller than the capacitance of the first gain conversion transistor.
14. An image sensing device, comprising: a first unit pixel including: a first photoelectric conversion element configured to generate photocharges in response to an incident light, a first floating diffusion region configured to store the photocharges; a first signal block including a first gain conversion transistor having a first terminal connected to the first floating diffusion region and a second terminal; a first connection block connected to the second terminal of the first gain conversion transistor and configured to connect the first signal block with one or more signal blocks included in other unit pixels than the first unit pixel based on control signals applied to the first connection block, and wherein a number of the one or more signal blocks connected to the first signal block depends on the control signals.
15. The image sensing device according to claim 14, wherein the first connection block includes: a first row booster block through which a second signal block included in a second unit pixel adjacent to the first unit pixel in a row direction is connected to the first signal block; and a first column booster block through which a third signal block included in a third unit pixel adjacent to the first unit pixel in a column direction is connected to the first signal block.
16. The image sensing device according to claim 15, wherein capacitance of the first row booster block or the first column booster block is smaller than a capacitance of the first gain conversion transistor.
17. The image sensing device according to claim 15, wherein the control signals include: a first horizontal column booster signal and a first vertical column booster signal that allow, when both activated, the first signal block to be connected to the third signal block.
18. The image sensing device according to claim 15, wherein the control signals include a first row booster signal that allows, when activated, the first signal block to be connected with the second signal block.

19. The image sensing device according to claim 14, wherein the first floating diffusion region has capacitances that depend on the number of the one or more signal blocks connected to the first signal block.