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(54) **SEMICONDUCTOR DEVICE**

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(57) **ABSTRACT**

A semiconductor device includes: a first electric-current generator circuit generating a first electric current having a positive temperature coefficient and not having dependency on a first power-supply voltage; a second electric-current generator circuit generating a second electric current having a negative temperature coefficient and not having dependency on the first power-supply voltage; and a third electric-current generator circuit generating a third electric current neither having dependency on the temperature nor the first power-supply voltage, based on the first electric current and the second electric current.

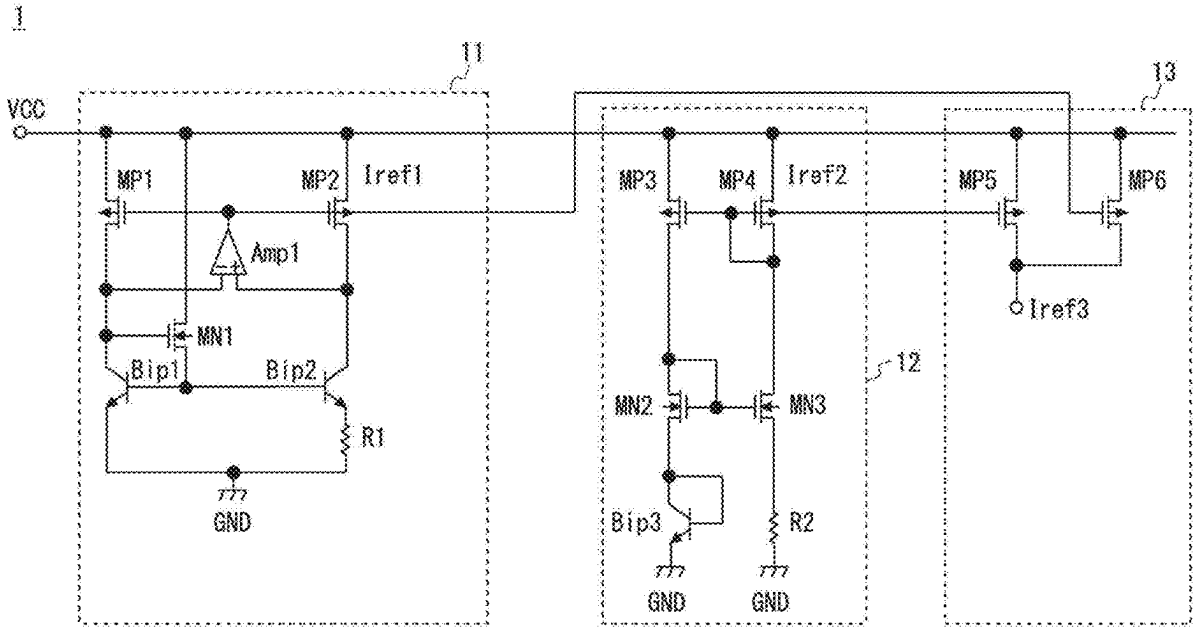


FIG. 1

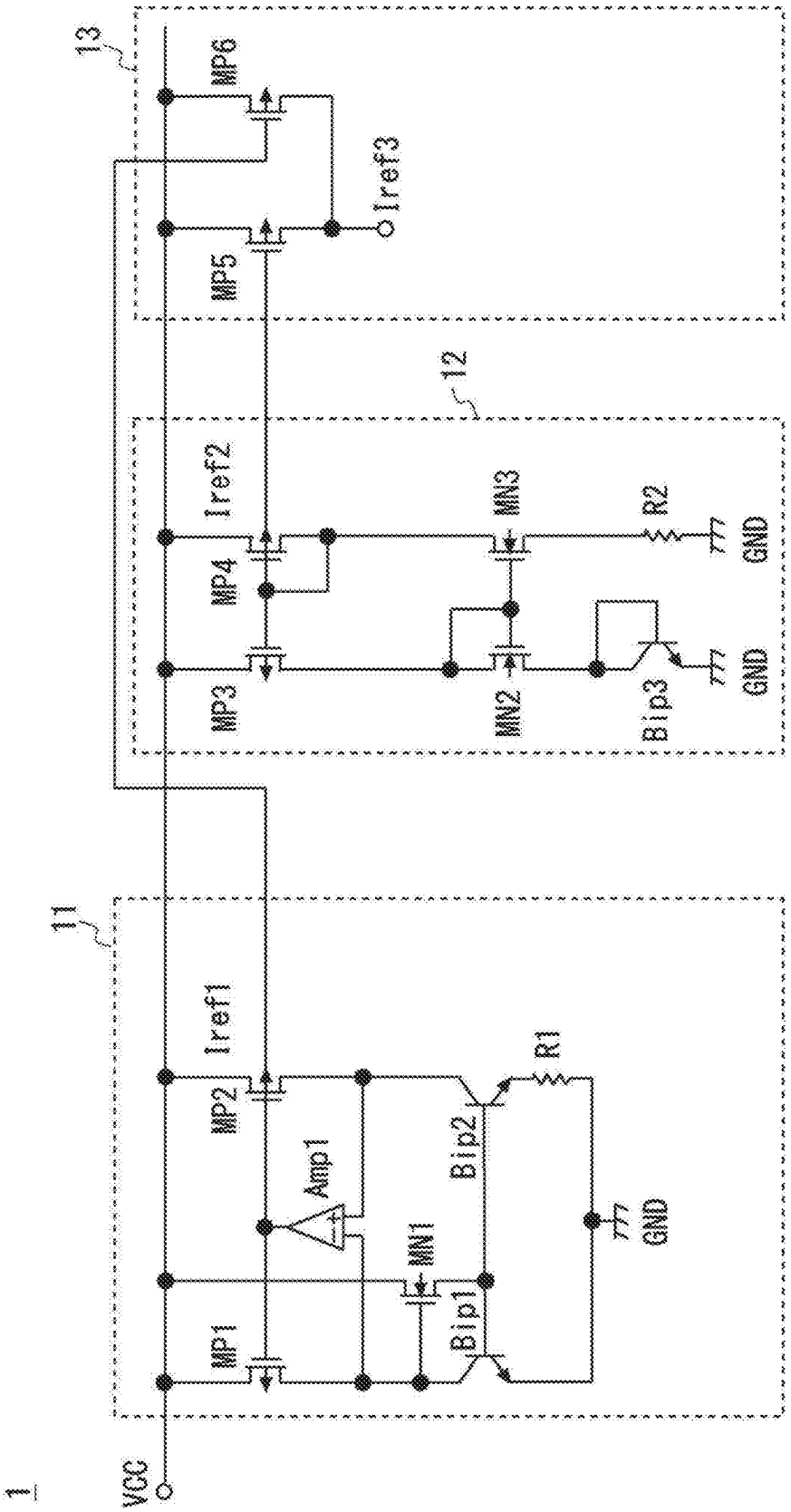

1
VCC
11
Iref1
MP1
MP2
Amp1
MN1
Bip1
Bip2
R1
GND
12
Iref2
MP3
MP4
MN2
MN3
Bip3
R2
GND
GND
13
Iref3
MP5
MP6

FIG. 2

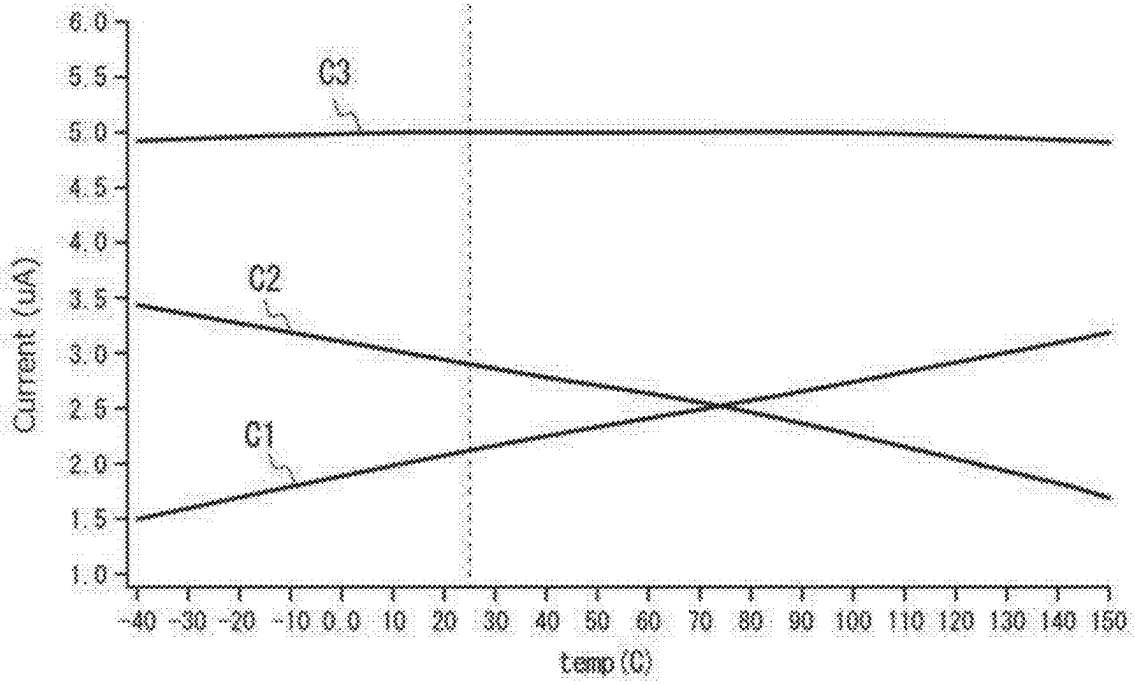

6.0
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
Current (uA)
C3
C2
C1
-40 -30 -20 -10 0.0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150
temp (C)

FIG. 3

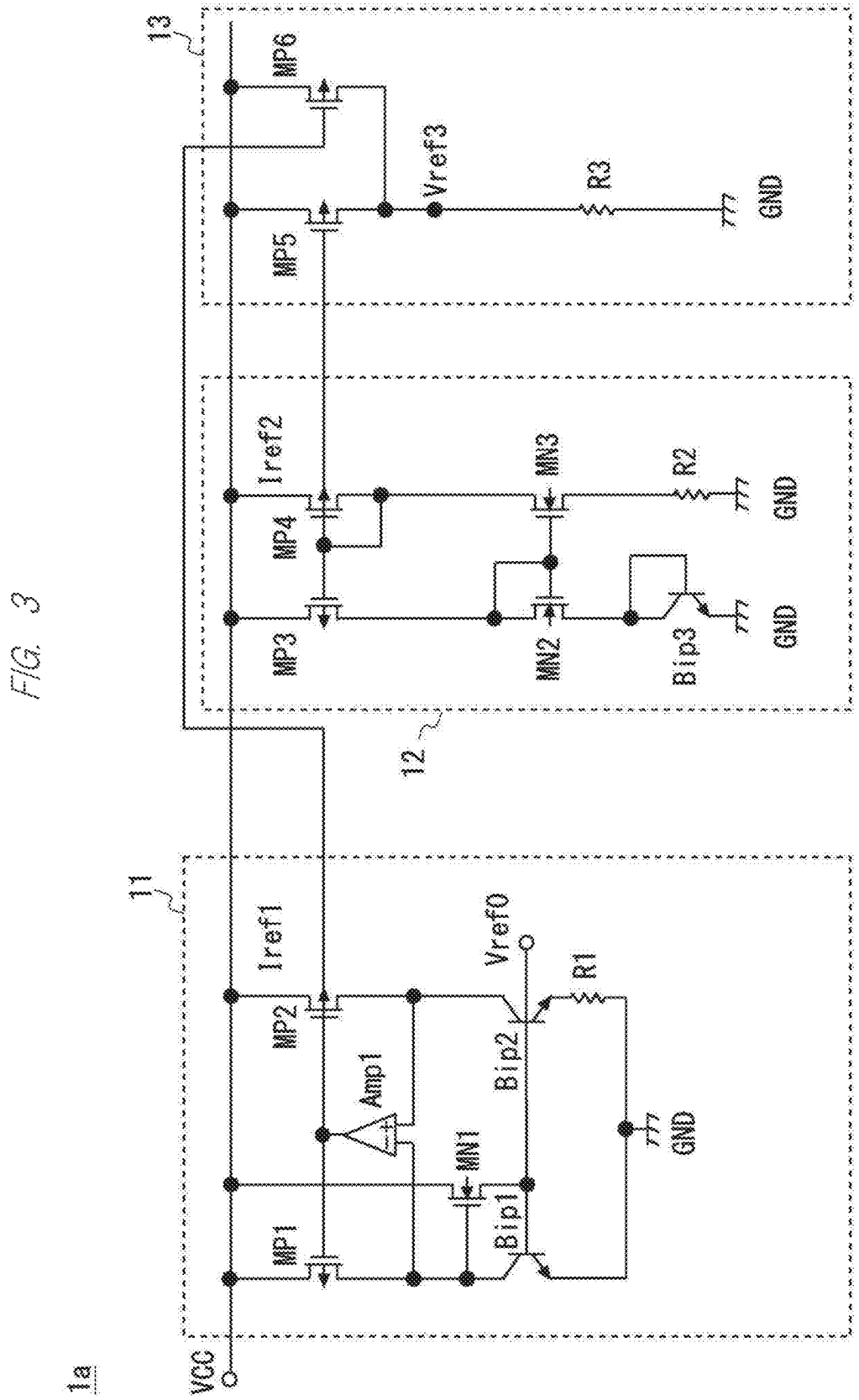

1a
VCC
11
Iref1
MP1
MP2
Amp1
MN1
Vref0
R1
Bip1
Bip2
GND
12
Iref2
MP3
MP4
MN2
MN3
R2
Bip3
GND
13
MP5
MP6
Vref3
R3
GND

FIG. 4

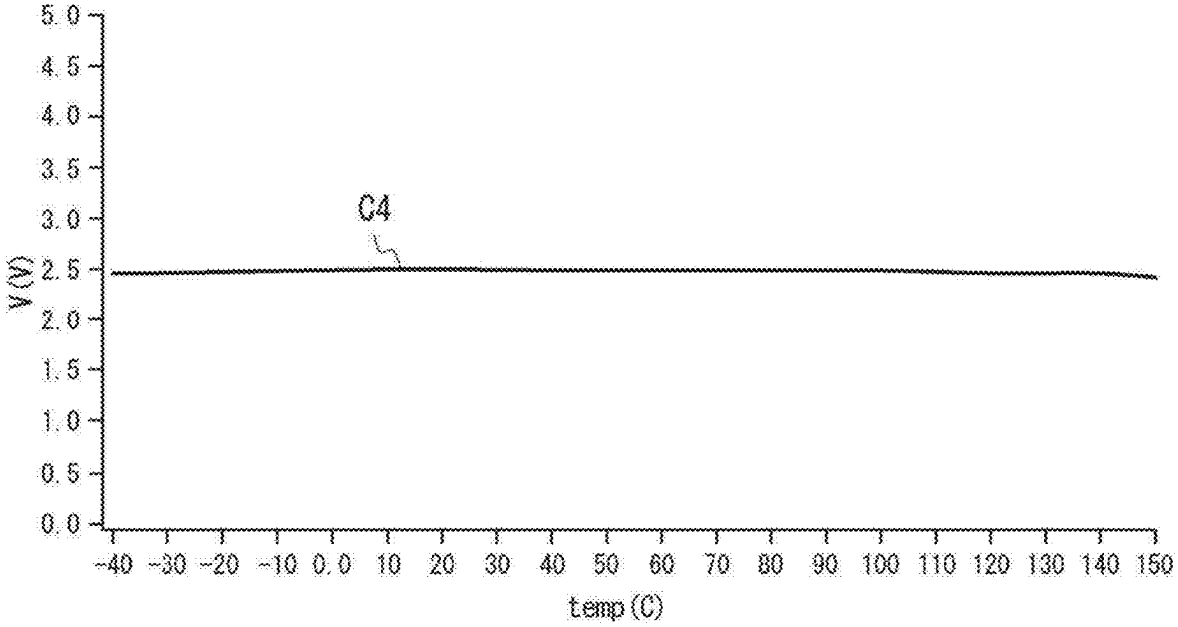

5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
V(V)
C4
-40 -30 -20 -10 0.0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150
temp(C)

FIG. 5

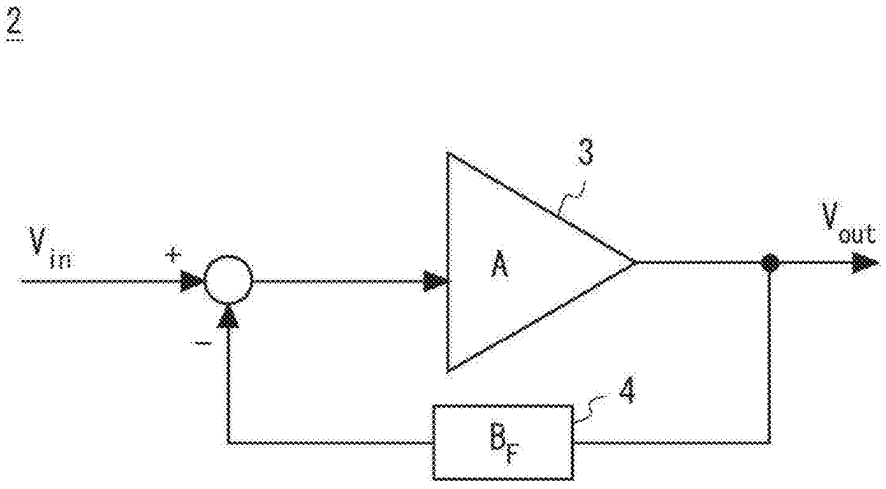

2
3
A
V_{in}
+
−
V_{out}
4
B_F

FIG. 6

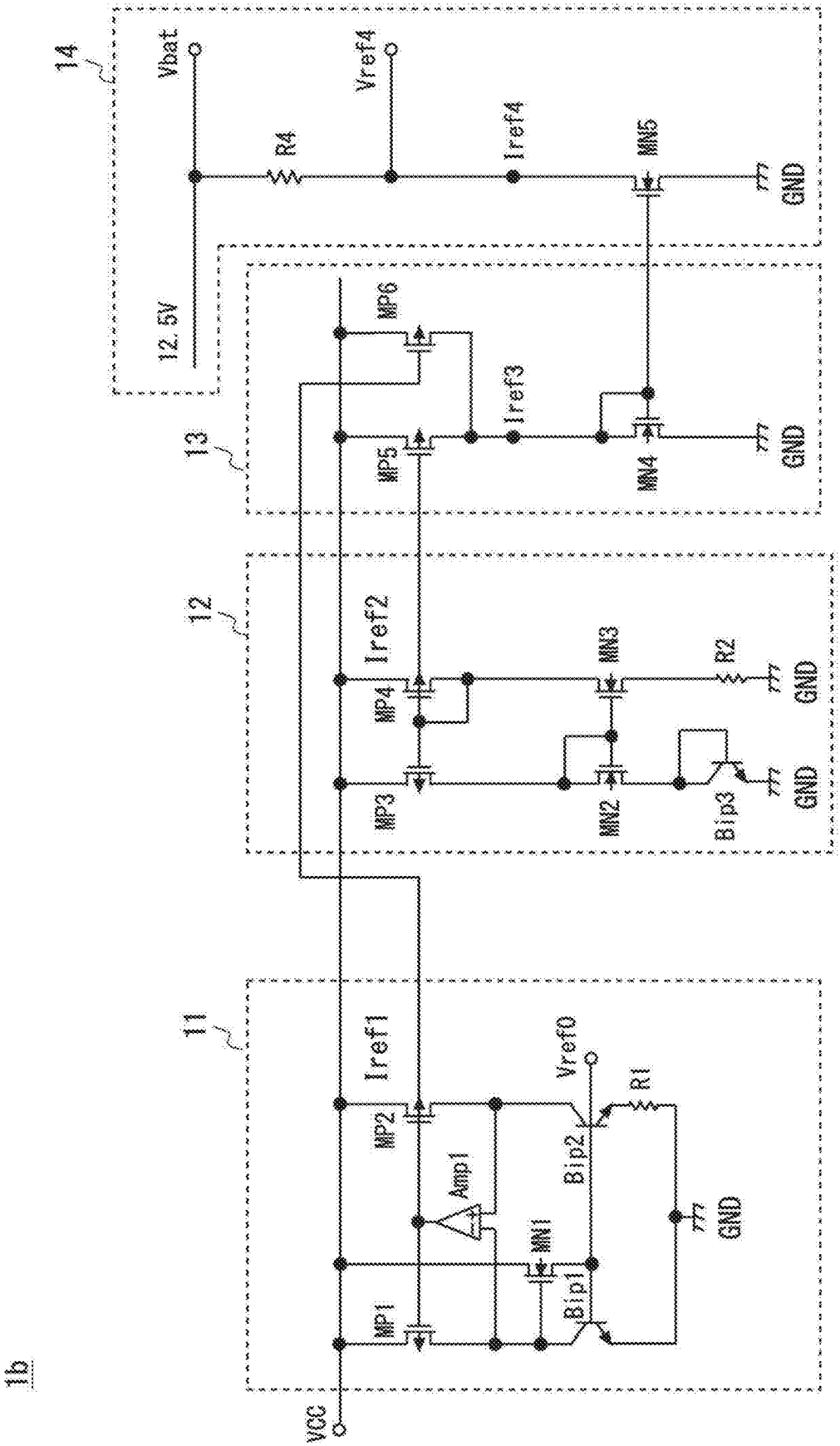
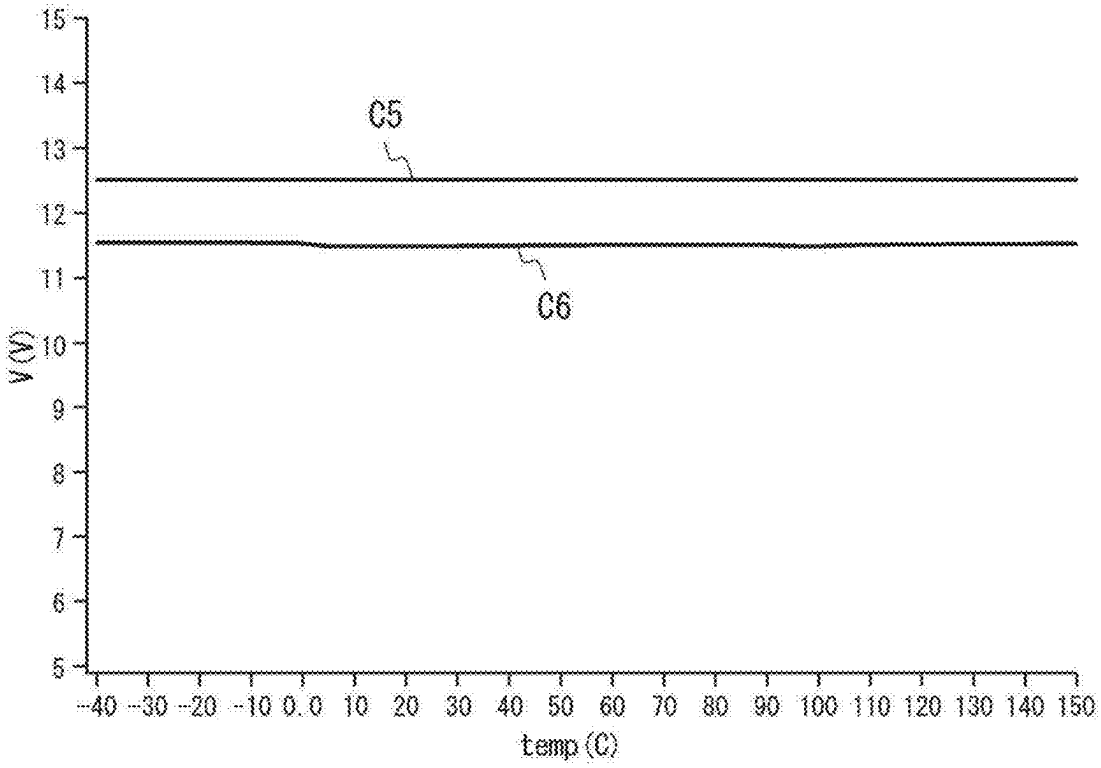

1b
14
Vbat
Vref4
R4
Iref4
MN5
GND
12.5V
13
MP6
Iref3
MP5
MN4
GND
12
Iref2
MN3
R2
MP4
GND
MP3
MN2
Bip3
GND
11
Iref1
Vref0
R1
MP2
Amp1
Bip2
GND
MN1
Bip1
MP1
VCC

FIG. 7


15
14
13
12
11
10
9
8
7
6
5
V(V)
C5
C6
-40 -30 -20 -10 0.0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150
temp(C)

SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. § 119 to Japanese Patent Application No. 2024-018375 filed on Feb. 9, 2024. The disclosure of Japanese Patent Application No. 2024-018375, including the specification, drawings and abstract, is incorporated herein by reference in its entirety.

BACKGROUND

[0002] The present invention relates to a semiconductor device, and more particularly relates to a semiconductor device generating a temperature-compensated electric current.

[0003] There is disclosed a technique listed below.

[0004] [Patent Document 1] Japanese Unexamined Patent Application Publication No. 2004-206633

[0005] The Patent Document 1 discloses a technique of generating a reference voltage compensated in terms of temperature and power-supply voltage and that is equal to or lower than 1.2 V.

SUMMARY

[0006] A reference-voltage generator circuit described in the Patent Document 1 has a problem that is failure to generate a voltage compensated in terms of temperature and power-supply voltage and that is equal to or higher than 1.2 V.

[0007] The present disclosure has been designed to solve such a problem, and an objective of the present disclosure is to achieve a semiconductor device generating an electric current compensated in terms of temperature and power-supply voltage.

[0008] Other objects and novel characteristics will become apparent from the description of the present specification and the drawings.

[0009] A semiconductor device according to an embodiment includes: a first electric-current generator circuit generating a first electric current having a positive temperature coefficient and not having dependency on a first power-supply voltage; a second electric-current generator circuit generating a second electric current having a negative temperature coefficient and not having dependency on the first power-supply voltage; and a third electric-current generator circuit generating a third electric current neither having dependency on the temperature nor the first power-supply voltage, based on the first electric current and the second electric current.

[0010] According to the embodiment, a semiconductor device generating an electric current compensated in terms of temperature and power-supply voltage can be provided.

BRIEF DESCRIPTIONS OF THE DRAWINGS

[0011] FIG. **1** is a circuit diagram showing a configuration of a semiconductor device according to a first embodiment.

[0012] FIG. **2** is a graph showing dependency on temperature for an electric current according to the first embodiment.

[0013] FIG. **3** is a circuit diagram showing a configuration of a semiconductor device according to a second embodiment.

[0014] FIG. **4** is a graph showing dependency on temperature for a reference voltage according to the second embodiment.

[0015] FIG. **5** is a diagram for explaining one of effects of the second embodiment.

[0016] FIG. **6** is a circuit diagram showing a configuration of a semiconductor device according to a third embodiment.

[0017] FIG. **7** is a graph showing dependency on temperature for a reference voltage according to the third embodiment.

DETAILED DESCRIPTION

[0018] The following description and drawings are appropriately omitted or simplified for clear explanation. The same components are denoted with the same reference signs throughout each drawing, and the repetitive description thereof is omitted as needed.

First Embodiment

[0019] FIG. **1** is a circuit diagram showing a configuration of a semiconductor device **1** according to a first embodiment. The semiconductor device **1** includes electric-current generator circuits **11**, **12** and **13**. The electric-current generator circuits **11**, **12** and **13** are also referred to as first electric-current generator circuit, second electric-current generator circuit and third electric-current generator circuit, respectively.

[0020] The electric-current generator circuit **11** includes p-channel type MOS (Metal-Oxide Semiconductor) transistors MP**1** and MP**2**, an n-channel type MOS transistor MN**1**, npn-type bipolar transistors Bip**1** and Bip**2**, a resistor R**1** and an amplifier Amp**1**.

[0021] The MOS transistor MP**1** and the bipolar transistor Bip**1** are connected in series between a power-supply voltage VCC and a ground voltage GND. The power-supply voltage VCC is also referred to as first power-supply voltage. The MOS transistor MP**2**, the bipolar transistor Bip**2** and the resistor R**1** are connected in series, and connected in parallel to the MOS transistor MP**1** and the bipolar transistor Bip**1**. Gates of the bipolar transistors Bip**1** and Bip**2** are connected to a source of the MOS transistor MN**1**, and a gate of the MOS transistor MN**1** is connected to a connection node between the MOS transistor MP**1** and the bipolar transistor Bip**1**. A drain of the MOS transistor MN**1** is connected to the power-supply voltage VCC. A negative-input terminal of the amplifier Amp**1** is connected to a connection node between the MOS transistor MP**1** and the bipolar transistor Bip**2**. A positive-input terminal of the amplifier Amp**1** is connected to a connection node between the MOS transistor MP**2** and the bipolar transistor Bip**2**. An output terminal of the amplifier Amp**1** is connected to gates of the MOS transistors MP**1** and MP**2**. The amplifier Amp**1** controls the MOS transistors MP**1** and MP**2** such that a voltage of the connection node connected to the positive-input terminal and a voltage of the connection node connected to the negative-input terminal are equal to each other.

[0022] If device sizes, in other words, gate lengths and gate widths of the MOS transistors MP**1** and MP**2** are equal to each other, an electric current (also referred to as first electric current) Iref**1** flowing between the source and the drain of the MOS transistor MP**2** of the electric-current generator circuit **11** is expressed by the following equation

(1). A temperature coefficient ΔIref**1**/ΔT of the electric current Iref**1** is expressed by the following equation (2).

$$Iref = 1/R1 * (kT/q) * (\ln M) \quad \text{Equation (1)}$$

$$\Delta Iref1/\Delta T = (1/R1) * (k/q) * (\ln M) \quad \text{Equation (2)}$$

[0023] The term "M" herein represents a ratio of an emitter area of the bipolar transistor Bip**1** and an emitter area of the bipolar transistor Bip**2**. The elementary charge is "q=1.6*10^(−19) [C]", the Boltzmann constant is "k=1.38*10^(−23) [J/K]", and the term "T" represents an absolute temperature [K]. Note that a resistance value of the resistor R**1** is assumed to be "R**1**".

[0024] From the equation (2), it is found that an equation (3) "ΔIref**1**/ΔT>0" is established.

[0025] The electric-current generator circuit **12** includes p-channel type MOS transistors MP**3** and MP**4**, n-channel type MOS transistors MN**2** and MN**3**, an npn-type bipolar transistor Bip**3** and a resistor R**2**.

[0026] The MOS transistor MP**3**, the MOS transistor MN**1** and the bipolar transistor Bip**3** are connected in series between the power-supply voltage VCC and the ground voltage GND. A collector and a base of the bipolar transistor Bip**3** are connected to each other. The MOS transistor MP**4**, the MOS transistor MN**3** and the resistor R**2** are connected in series, and connected in parallel to the MOS transistor MP**3**, the MOS transistor MN**1** and the bipolar transistor Bip**3**. Gates of the MOS transistors MP**3** and MP**4** are connected to a connection node between the MOS transistor MP**4** and the MOS transistor MN**3**. Gates of the MOS transistors MN**2** and MN**3** are connected to a connection node between the MOS transistor MP**3** and the MOS transistor MN**2**. The MOS transistors MP**3**, MP**4**, MN**2** and MN**3** configure a current mirror circuit. If the device sizes of the MOS transistors MP**3**, MP**4**, MN**1** and MN**2** are equal to one another, the electric currents flowing in the MOS transistors MP**3**, MP**4**, MN**1** and MN**2** are equal to one another. A voltage of the connection node between the MOS transistors MN**2** and the bipolar transistor Bip**3** is equal to a voltage of the connection node between the MOS transistors MN**3** and the resistor R**2**.

[0027] If the device sizes of the MOS transistors MP**3**, MP**4**, MN**1** and MN**2** are equal to one another, the electric current Iref**2** (also referred to as second electric current) flowing in the MOS transistor MP**4** of the electric-current generator circuit **12** is expressed by the following equation (4). Its temperature coefficient ΔIref**2**/ΔT is expressed by the following equation (5).

$$Iref2 = (\mathrm{VBE\_Bip3})/R2 \quad \text{Equation (4)}$$

$$\Delta Iref2/\Delta T = ((\Delta \mathrm{VBE\_Bip3})/\Delta T)/R2 \quad \text{Equation (5)}$$

[0028] The term "VBE_Bip**3**" herein represents a voltage between the base and the emitter of the bipolar transistor Bip**3**. Note that a resistance value of the resistor R**2** is assumed to be "R**2**".

[0029] Because of "(ΔVBE_Bip**3**)/ΔT<0", the following equation (6) is derived from the equation (5).

$$\Delta Iref2/\Delta T < 0 \quad \text{Equation (6)}$$

[0030] The electric-current generator circuit **13** includes p-channel type MOS transistors MP**5** and MP**6**. A source of the MOS transistor MP**5** is connected to the power-supply voltage VCC, and a gate of the MOS transistor MP**5** is connected to a gate of the MOS transistor MP**4**. The MOS transistor MP**6** is connected in parallel to the MOS transistor MP**5**, and a gate of the MOS transistor MP**6** is connected to a gate of the MOS transistor MP**2**. The MOS transistor MP**5** copies the electric current Iref**2** at a predetermined mirror ratio, the electric current flowing between the source and the drain of the MOS transistor MP**4**. The MOS transistor MP**6** copies the electric current Iref**1** at a predetermined mirror ratio, the electric current flowing between the source and the drain of the MOS transistor MP**2**. The electric current flowing between the source and the drain of the MOS transistor MP**5** and the electric current flowing between the source and the drain of the MOS transistor MP**6** are synthesized to generate an electric current Iref**3** (also referred to as third electric current).

[0031] The electric current Iref**3** is expressed by the following equation (7). Its temperature coefficient ΔIref**3**/ΔT is expressed by the following equation (8).

$$Iref3 = A * Iref1 + B * Iref2 \quad \text{Equation (7)}$$

$$\Delta Iref3/\Delta T = A * \Delta Iref1/\Delta T + B * \Delta Iref2/\Delta T \quad \text{Equation (8)}$$

[0032] The term "A" herein represents the mirror ratio between the MOS transistors MP**2** and MP**6**, and the term "B" herein represents the mirror ratio between the MOS transistors MP**4** and MP**5**.

[0033] By appropriately setting the terms "A" and "B", the electric current Iref**3** not having dependency on temperature is derived from the equations (8), (3) and (6). Also, the equation (8) does not include a term relating to the power-supply voltage VCC. Therefore, the semiconductor device **1** according to the first embodiment can generate the electric current neither having dependency on the power-supply voltage nor the temperature.

[0034] Next, a case of setting the following condition (1) will be specifically explained.

$$R1 = 50\ [\mathrm{k\Omega}],\ M = 8,\ R2 = 900\ [\mathrm{k\Omega}],\ A = 2,\ B = 4 \quad \text{Condition (1)}$$

[0035] The following equations (1'), (2'), (4'), (5'), (7'), and (8') are derived from substitution of the numerical values of the condition (1) into the equations (1), (2), (4), (5), (7), and (8).

$$Iref1 = (1/50K) * (kT/q) * (\ln 8) = 1\ [\mu\mathrm{A}] \quad \text{Equation (1')}$$

$$\Delta Iref1/\Delta T = (1/50K) * (k/q) * (\ln 8) = 3.6\ [\mathrm{nA/^{\circ}\ C.}]] \quad \text{Equation (2')}$$

$$Iref2 = (VBE\_Bip3)/900K = 770\ [nA] \quad \text{Equation (4')}$$

$$\Delta Iref2/\Delta T = \quad \text{Equation (5')}$$

$$(\Delta VBE/\Delta T)/900K = 162\ [mV/^\circ C.]/900\ [k\Omega] = 18\ [nA/^\circ C.]$$

$$Iref3 = 2 * Iref1 + 4 * Iref2 = 5\ [\mu A] \quad \text{Equation (7')}$$

$$\Delta Iref3/\Delta T + 4 * \Delta Iref2/\Delta T = 0\ [A/^\circ C.] \quad \text{Equation (8')}$$

[0036] The result "(ΔVBE/ΔT)=−1.62 [mV/° C.]" herein is set from simulation results for the temperature coefficient of the VBE in a case of "Emitter electric current: IE=770 nA".

[0037] Since the temperature coefficient in the equation (8') is 0, it is verified that the electric current not having dependency on temperature can be generated.

[0038] FIG. **2** shows the simulation results in the case of setting of the condition (1). Its horizontal axis represents the temperature, and its vertical axis represents the electric current. The term "C1" represents the electric current flowing between the source and the drain of the MOS transistor MP**6**, in other words, represents the dependency on temperature for "Iref**1***4". The term "C2" represents the electric current flowing between the source and the drain of the MOS transistor MP**5**, in other words, represents the dependency on temperature for "Iref**2***4". The term "C3" represents the dependency on temperature for "Iref**3**". A vertically-extending dotted line represents 25° C. The temperature of 25° C. meets "Iref**1***2=2 [μA]", "Iref**2***4=3 [μA]" and "Iref**3**=5 [μA]". It is found that the Iref**1** has the positive dependency on temperature, the Iref**12** has the negative dependency on temperature, and the Iref**3** has no dependency on temperature.

Second Embodiment

[0039] FIG. **3** is a circuit diagram of a semiconductor device **1***a* according to a second embodiment. The semiconductor device **1***a* generates a reference voltage neither having the dependency on the temperature nor the power-supply voltage VCC, based on the electric current Iref**3**.

[0040] In comparison between FIGS. **1** and **3**, an electric-current generator circuit **13** of the semiconductor device **1***a* further includes a resistor R**3**. One end of the resistor R**3** is connected to a connection node between the MOS transistor MP**5** and he MOS transistor MP**6**. The other end of the resistor R**3** is connected to the ground voltage GND. When the electric current Iref**3** flows in the resistor R**3**, a reference voltage Vref**3** is generated on one end of the resistor R**3**.

[0041] The reference voltage Vref**3** is expressed by the following equation (9). Its temperature coefficient "ΔVref**3**/ΔT" is expressed by the following equation (10).

$$Vref3 = Iref3 * R3 \quad \text{Equation (9)}$$

$$\Delta Vref3/\Delta T = (\Delta Iref3/\Delta T) * R3 \quad \text{Equation (10)}$$

[0042] As described above, by appropriately setting the terms "A" and "B" in the equation (8), the electric current Iref**3** having the temperature coefficient "ΔIref**3**/ΔT" in the following equation (11) and not having the dependency on temperature can be achieved.

$$\Delta Iref3/\Delta T = 0 \quad \text{Equation (11)}$$

[0043] It is found that "ΔVref**3**/ΔT=0" is achieved by substitution of the equation (11) into the equation (10).

[0044] As described above, it is found that the optional reference voltage Vref compensated in terms of the temperature and the power-supply voltage can be generated by appropriately selecting the resistance value of the resistor R**3**. Particularly, the reference voltage Vref that is equal to or higher than 1.2 V can be generated.

[0045] Next, a case of setting the following condition (2) in addition to the condition (1) will be specifically explained.

$$R3 = 500\ [k\Omega] \quad \text{Condition (2)}$$

[0046] The following equation (9') is derived from substitution of the condition (2) and the Iref**3** calculated from the equation (7') into the equation (9). And, the following equation (10') is derived from substitution of "ΔIref**3**/ΔT=0" in the equation (11) into the equation (10).

$$Vref3 = Iref3 * R3 = 5\ [\mu A] * 500\ [k\Omega] = 2.5\ [V] \quad \text{Equation (9')}$$

$$\Delta Vref3/\Delta T = (\Delta Iref3/\Delta T) * R3 = 0 * 500\ [k\Omega] = 0\ [V/^\circ C.] \quad \text{Equation (10')}$$

[0047] It is verified that the reference voltage Vref having the temperature coefficient of 0 in the equation (10) and not having the dependency on temperature can be generated. With reference to the equation (9'), it is verified that the reference voltage that is equal to or higher than 1.2 V can be generated.

[0048] FIG. **4** shows simulation results in a case of setting the condition (1) and the condition (2). Its horizontal axis represents the temperature, and its vertical axis represents the voltage. The term "C4" represents the dependency on temperature for the reference voltage Vref. The reference voltage Vref is about 2.5 V to be equal to or larger than 1.2 V. From the simulation results, it is found that the second embodiment can generate the reference voltage not having the dependency on temperature and being equal to or larger than 1.2 V.

[0049] Next, with reference to FIG. **5**, one of effects caused by the generation of the optional reference voltage neither having the dependency on the temperature nor the power-supply voltage and being equal to or larger than 1.2 V will be explained. A negative-feedback amplifier circuit **2** includes an amplifier circuit **3** and a feedback circuit **4**. The feedback circuit **4** returns a part of a voltage amplified by the amplifier circuit **3** to an input of the amplifier circuit **3** in the opposite phase. Regarding an input voltage Vin and an output voltage Vout of the negative-feedback amplifier circuit **2**, the following equation (12) is established.

$$Vout/Vin = A/(1 + \beta_F * A) \quad \text{Equation (12)}$$

[0050] The term "β_F" herein represents a feedback rate of the feedback circuit **4**, and the term "A" herein represents a gain of the amplifier circuit **3**.

[0051] Generally, the term "A" is sufficiently larger than 1, and is equal to or larger than 1000 times. Therefore, the equation (12) can be deformed to be the following equation (13).

$$Vout/Vin = A/(1 + \beta_F * A) = 1/\beta_F \quad \text{Equation (13)}$$

[0052] It is known that the larger the term "β_F" configuring the equation (13) is, the lower the distortion is, and the higher the speed is. For example, if the reference voltage "Vref=2.5 V" in the second embodiment is supplied as the Vin in order to provide "Vout=2.5 [V]", a relation "β_F=1" is derived from the equation (13). On the other hand, if the reference voltage "Vref=1.25 V" in the related art is supplied as the Vin, a relation "β_F=0.5" is established.

[0053] Since the feedback amount β_F of the negative-feedback amplifier circuit can be set to large, the second embodiment can achieve the low distortion and the high speed of the negative-feedback amplifier circuit.

Third Embodiment

[0054] FIG. **6** is a circuit diagram of a semiconductor device **1***b* according to a third embodiment. The semiconductor device **1***b* generates a reference voltage with reference to a power-supply voltage Vbat, based on the electric current Iref**3**.

[0055] In comparison between FIGS. **1** and **6**, the semiconductor device **1***b* further includes a reference-voltage generator circuit **14** with reference to the power-supply voltage Vbat. The reference-voltage generator circuit **14** includes an n-channel type MOS transistor MN**5** and a resistor R**4**. The electric-current generator circuit **13** further includes an n-channel type MOS transistor MN**4**.

[0056] The MOS transistor MN**4** is arranged between the ground voltage GND and a connection node between the MOS transistor MP**3** and the MOS transistor MP**4**. The resistor R**4** and the MOS transistor MN**5** are connected in series between the power-supply voltage Vbat and the ground voltage GND. The power-supply voltage Vbat is also referred to as second power-supply voltage. Gates of the MOS transistors MN**4** and MN**5** are connected to a drain of the MOS transistor MN**4**. One end of the resistor R**4** is connected to the power-supply voltage Vbat, and the reference voltage Vref**4** is generated on the other end of the resistor R**4**.

[0057] The power-supply voltage Vbat is, for example, a voltage of a battery mounted on a vehicle. The MOS transistors MN**4** and MN**5** configure a current mirror circuit, and the MOS transistor MN**5** makes a flow of a mirror electric current Iref**4** of the electric current Iref**3** to the resistor R**4**. As a result, a reference voltage Vref**4** is generated on a connection node between the resistor R**4** and the MOS transistor MN**5**.

[0058] The reference voltage Vref**4** is expressed by the following equation (14). Its temperature coefficient "ΔVref**4**/ΔT" is expressed by the following equation (15).

$$Vref4 = Vbat - (Iref4 * R4) \quad \text{Equation (14)}$$

$$Vout/Vin = \Delta Vref4/\Delta T = (\Delta Iref4/\Delta T) * R4 \quad \text{Equation (15)}$$

[0059] The term "Iref**4**" herein represents the mirror electric current of the electric current Iref**3** as described above. Since a relation "ΔIref**3**/ΔT=0" in the equation (11) is established, a relation "ΔIref**4**/ΔT=0" is also established. Therefore, from the equation (15), it is also found that a relation "ΔVref**4**/ΔT=0" is achieved.

[0060] Therefore, the third embodiment can provide the optional reference voltage Vref**4** compensated in terms of temperature with reference to the power-supply voltage Vbat different from the power-supply voltage VCC, by appropriately selecting the resistor R**4**. The power-supply voltage Vref**4** does not depend on the power-supply voltage VCC.

[0061] Next, a case of setting the following condition (3) in addition to the condition (1) will be specifically explained.

$$R4 = 200\ [k\Omega],\ Vbat = 12.5\ [V] \quad \text{Condition (3)}$$

[0062] The following equation (14') is derived from substitution of the condition (3) into the equation (14). The following equation (15') is derived from substitution of the condition (3) into the equation (15). Because of a relation "Iref**3**=5 [μA]" in the equation (7'), a relation "Iref**4**=5 [μA]" is set.

$$Vref4 = \quad \text{Equation (14')}$$

$$Vbat - (Iref4 * R4) = 12.5\ [V] - 5\ [\mu A] * 200\ [k\Omega] = 11.5$$

$$\Delta Vref4/\Delta T = (\Delta Iref4/\Delta T) * R4 = 0 * 200\ [k\Omega] = 0 \quad \text{Equation (15')}$$

[0063] It is verified that the reference Voltage Vref**4** having the temperature coefficient of 0 in the equation (15') and not having the dependency on temperature can be generated.

[0064] FIG. **7** shows simulation results in a case of setting the condition (1) and the condition (3). Its horizontal axis represents the temperature, and its vertical axis represents the voltage. The term "C5" represents the power-supply voltage Vbat, and the term "C6" represents the dependency on temperature for the reference voltage Vref. The power-supply voltage Vbat is 12.5 V, and the reference voltage Vref**4** is about 11.5 V. From the simulation results, it is found that the third embodiment can generate the reference voltage Vref**4** not having the dependency on temperature.

[0065] In the third embodiment, the mirror electric current Iref**4** of the electric current Iref**3** generated with reference to the ground voltage GND is flown in the resistor R**4** connected to the power-supply voltage Vbat. As a result, the third embodiment can generate the reference voltage Vref with reference to the power-supply voltage Vbat.

[0066] Generally, in order to generate the reference voltage with reference to the power-supply voltage Vbat, it is necessary to prepare a reference voltage source with reference to the power-supply voltage Vbat as different from a reference voltage source with reference to the ground voltage GND. In the third embodiment, it is unnecessary to

prepare it, and therefore, the circuit area and the consumed electric current can be reduced.

[0067] The reference-voltage generator circuit **14** may be included in a semiconductor device different from the semiconductor device including the electric-current generator circuits **11**, **12** and **13**. For example, the semiconductor device including the reference-voltage generator circuit **14** may be an intelligent power device (IPD) including the power MOSFET, and the semiconductor device including the electric-current generator circuits **11**, **12** and **13** may be a MCU controlling the IPD. The IPD may include a controller circuit connected to the battery power supply (Vbat) and controlling the power MOSFET. If a reference voltage is necessary for the controller circuit in this IPD, the IPD needs to include a reference voltage source with reference to the battery power supply Vbat, such as a bandgap reference circuit. In this case, the reference voltage source included in the IPD needs to be made of a high withstand voltage device. However, the third embodiment can generate the reference voltage with reference to the battery power supply Vbat by using a simpler circuit configuration than the bandgap reference circuit as the reference-potential generator circuit included in the IPD. As a result, the circuit area and the consumed electric current of the IPE can be reduced.

[0068] In the foregoing, the invention made by the inventors of the present application has been concretely described on the basis of the embodiments. However, the present invention is not limited to the foregoing embodiments, and various modifications can be made within the scope of the present invention.

[0069] For example, a regulator according to the embodiments may be configured such that the conductivity types (p-type or n-type) of the semiconductor substrate, the semiconductor layer, the diffusion layer (diffusion region) and the like are inverted. Therefore, if either one of the n-type and the p-type is set as a first conductivity type while the other conductivity type is set as a second conductivity type, the first conductivity type may be the p-type while the second conductivity type may be the n-type, and conversely, the first conductivity type may be the n-type while the second conductivity type may be the p-type.

What is claimed is:

1. A semiconductor device comprising:

a first electric-current generator circuit generating a first electric current having a positive temperature coefficient and not having dependency on a first power-supply voltage;

a second electric-current generator circuit generating a second electric current having a negative temperature coefficient and not having dependency on the first power-supply voltage; and

a third electric-current generator circuit generating a third electric current neither having dependency on the temperature nor the first power-supply voltage, based on the first electric current and the second electric current.

2. The semiconductor device according to claim **1**,

wherein the third electric current is generated by synthesis of an electric current copied at a first mirror ratio from the first electric current and an electric current copied at a second mirror ratio from the second electric current, and

the first mirror ratio and the second mirror ratio are set such that a temperature coefficient of the third electric current is zero.

3. The semiconductor device according to claim **1**,

wherein a reference voltage neither having dependency on the temperature nor the first power-supply voltage is generated based on the third electric current.

4. The semiconductor device according to claim **3**,

wherein the reference voltage is larger than 1.2 V.

5. The semiconductor device according to claim **3** further comprising

a negative-feedback amplifier circuit amplifying the reference voltage.

6. The semiconductor device according to claim **5**,

wherein a feedback rate of the negative-feedback amplifier circuit is larger than 0.5.

7. The semiconductor device according to claim **3** further comprising

a current mirror circuit making flow of an electric current copied from the third electric current to a resistor, one end of which is connected to a second power-supply voltage,

wherein the reference voltage is generated on the other end of the resistor.

8. The semiconductor device according to claim **7**,

wherein the second power-supply voltage is a battery voltage.

9. The semiconductor device according to claim **1**,

wherein the second electric current is generated based on a voltage between a base and an emitter of a bipolar transistor.

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