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Method and apparatus for low-complexity symbol-rate receiver digital signal processing

Abstract

A digital signal processor (DSP) for a receiver and a method for processing signals in a receiver are provided. The DSP comprises a processor configured to: receive a digital signal at a symbol rate in a frequency domain; and compensate an impairment of the digital signal in the frequency domain.

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Background/Summary

RELATED APPLICATIONS (1) This application is a continuation of International Patent Application No. PCT/CN2020/125638, filed Oct. 31, 2020, the contents of which are incorporated herein by reference.

FIELD
(1) The present invention generally relates to digital signal processing, and in particular, to a method and apparatus for low-complexity symbol-rate receiver digital signal processing.
BACKGROUND

(2) Coherent detection together with digital signal processing (DSP) is capable of compensating various linear and nonlinear impairments. For short-reach applications, the complexity and power consumption of DSP are major concerns. Therefore, reducing the complexity and power consumption for short-reach DSP applications is desirable.

SUMMARY

(3) The present disclosure provides a low-power and efficient low-complexity symbol-rate DSP scheme with a frequency domain equalizer structure for short-reach applications.

(4) The present disclosure reduces the ADC sample rate to symbol rate at the receiver so that the receiver (Rx) DSP operates at symbol rate (T/1). As such, the power consumption of both ADC and Rx DSP are greatly reduced. The present disclosure also provides an efficient T/1 timing recovery approach.

(5) According to an aspect, there is provided a digital signal processor (DSP) for a receiver, which comprises a processor configured to: receive a digital signal at a symbol rate in a frequency domain; and compensate an impairment of the digital signal in the frequency domain.

(6) According to an aspect, there is provided a method for processing signals in a receiver, comprising: receiving a digital signal at a symbol rate in frequency domain; and compensating an impairment of the digital signal in frequency domain.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) Reference will now be made, by way of example, to the accompanying drawings which show example embodiments of the present application, and in which:

(2) FIG. **1** is a block diagram of a telecommunication system with a transmitter and a receiver (Rx) having a digital signal processor (DSP), according to the present disclosure;

(3) FIG. **2** is a block diagram of an example logical structure of the Rx DSP in FIG. **1**;

(4) FIG. **3** is a flowchart illustrating an example process of digital signal processing using the Rx DSP in FIG. **1**;

(5) FIG. **4** illustrates simulated performance of the Rx DSP in FIG. **1**, in accordance with embodiments of present disclosure, in terms of bit error rate (BER) and received optical power (ROP); and

(6) FIG. **5** is a block diagram of an example hardware structure of the Rx DSP in FIG. **1**.

(7) Similar reference numerals may have been used in different figures to denote similar components.

DESCRIPTION OF EXAMPLE EMBODIMENTS

(8) Unless otherwise defined or unless context indicates otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the described embodiments appertain.

(9) FIG. **1** is a block diagram of an optical communication system **10**. In the example of FIG. **1**, the system **10** comprises a transmitter **12**, a receiver **14**, and a fiber link **62** interconnecting the transmitter **12** and receiver **14**. The transmitter **12** comprises a transmitter (Tx) digital signal processor (DSP) **20**, a Tx digital to analog convertor (DAC) **30**, a driver **40**, an in-phase quadrature modulator (IQM) **50**, and a Tx laser **60**. The receiver **14** includes an integrated coherent receiver (ICR) **70**, a receiver (Rx) laser **75**, an Rx analog to digital convertor (ADC) **80**, a voltage-controlled oscillator **90**, and an Rx DSP **100**.

(10) In the transmitter **12**, the Tx DSP **20** is configured to receive digital signals and process, such as pre-compensate, the received digital signals. A received digital signal is a two-dimensional vector having an X-polarization and a Y-polarization. The Tx DAC **30** is configured to convert the processed digital signals to analog signals. The analog signals are amplified by the driver **40**. The

amplified analog signals are then modulated at IQM **50** by the Tx laser **60**. The IQM **50** converts the amplified analog signals into optical signals having X-polarization and Y-polarization.

(11) The X- and Y-polarized optical signals are transmitted through fiber link **62**. In some examples, the analog signals may also be modulated to RF signals and the analog RF signals may be transmitted wirelessly by one or more antennas.

(12) In the receiver **14**, the X- and Y-polarized optical signals are detected at ICR **70**. A local oscillator that includes Rx laser **75** provides an optical demodulating signal to enable the ICR **70** to convert or demodulate the optical signals to X- and Y-polarized analog signals.

(13) The Rx ADC **80** is configured to convert the X- and Y-polarized analog signals to X- and Y-polarized digital signals. The X- and Y-polarized digital signals are then forwarded the Rx DSP **100** for processing.

(14) In system **10**, due to the differences in hardware in the transmitter **12** and the receiver **14**, and physical characteristics of the transmission medium (e.g. fiber link **62**), the digital signals received at the Rx DSP **100** may suffer various impairments, including linear and non-linear channel impairment, frequency shift, time delay and timing misalignment, channel impairment, etc. Some impairments are non-time-varying impairments such as chromatic dispersion (CD), S**21**, match filtering, while some impairments are time-varying impairments such as polarization mode dispersion (PMD), polarization division de-multiplexing, etc. Adaptive equalization can be used to compensate time-varying impairments and residual non-time-varying impairments, such as residual CD.

(15) In the present application, by processing the received digital signals, the Rx DSP **100** is configured to compensate various impairments suffered by the received digital signals. The Rx DSP **100** may compensate impairments of the digital signals by adjusting the received digital signals to reduce time delays, phase shifts, frequency offsets, timing errors, and other applicable parameters of the digital signals to an acceptable extent. In some examples, as will be described in greater detail below, the Rx DSP **100** may adjust the digital signals by equalizing the digital signals, such as by correlating the digital signals in frequency domain with the MIMO taps, updating MIMO taps and the digital signals, until the time domain error of the received digital signals is within an acceptable range.

(16) However, time-domain equalization can contribute significantly to overall DSP complexity, especially when used to support a large number of taps. Frequency-domain equalization (FDEQ) structures may be used to reduce complexity by taking advantage of a block-by-block signal processing strategy in frequency domain and efficient implementation of a discrete Fourier transform (DFT) function.

(17) In the present disclosure, in receiver **14**, when the Rx ADC **80** converts the X- and Y-polarized analog signals to digital signals, the Rx ADC **80** is configured to sample the X- and Y-polarized analog signals from the ICR **70** at a sample rate equal to the symbol rate (T/1) of the digital signals received at the Tx DSP **20**. As such, the digital signals output from the Rx ADC **80** are at the original symbol rate (T/1). The Rx ADC **80** forwards the X- and Y-polarized digital signals at the symbol rate to the Rx DSP **100** for processing, including impairment compensation, as will be described in greater detail below. The Rx DSP **100** is also configured to adjust the VCO **90**, which in turn controls the frequency and phase of sampling clock signals used in the Rx ADC **80**.

(18) The optical communication system **10** may be a short reach application. For example, the distance between the transmitter **12** and receiver **14**, or the length of the fiber link **62**, is less or equal to 40 kilometers. In the short reach application, the channel impairments are not as severe as those in long haul system. Thus, in at least some applications, over sampling is not essential for impairment compensation.

(19) The overall complexity of the Rx ADC **80** and Rx DSP **100** is proportional to sample rate. Thus, reducing sampling rate can enable a low power design. By reducing sample rate of the Rx ADC **80** to one sample per symbol (T/1) (e.g., sample rate=symbol rate), the complexity and power

consumption Rx ADC **80** and Rx DSP **100** may be greatly reduced. As well, operating Rx ADC **80** at a sample rate that equals the symbol rate can consume less power.

(20) As illustrated in the example of FIG. **2**, the Rx DSP **100** includes a concatenator module **119**, a Fast Fourier Transformation (FFT) module **120**, a IQC unit **122**, a 2×2 multiple input multiple output (MIMO) module **124**, an Inverse Fast Fourier Transform (IFFT) module **126**, a save last block module **127**, a Carrier Recovery (CR) module **128**, a MIMO taps update module **130**, a timing error calculator **132**, and a loop filter **134**.

(21) As used here, a “module” can refer to a combination of a hardware processing circuit and machine-readable instructions (software and/or firmware) executable on the hardware processing circuit. A hardware processing circuit can include any or some combination of a microprocessor, a core of a multi-core microprocessor, a microcontroller, a programmable integrated circuit, a programmable gate array, a digital signal processor, or another hardware processing circuit.

(22) As illustrated in FIG. **2**, the Rx DSP **100** comprises a concatenator module **119** configured to concatenate X- and Y-polarized time-domain digital signals from the ADC **80** at a symbol rate. The m.sup.th block of data in signal x and y in time domain contains the most recent N data samples from the previous N data samples in time domain for both X polarization and Y polarization, respectively. For example, the concatenator module **119** concatenates the m.sup.th block of most recent X-polarized N data samples in the digital signals with previous block of X-polarized N data samples in the digital signals. Similarly, the block concatenator **119** concatenates the m.sup.th block of most recent Y-polarized N data samples with previous block of Y-polarized N data samples in digital signals. Hence, the overall length of the m.sup.th block of the X- and Y-polarized digital signals output from the concatenator module **119** is 2N.

(23) The FFT module **120** is configured to convert the input time domain digital signals from the concatenator module **119** to frequency domain signals. The FFT module **120** performs **2**N point FFT and transforms the X- and Y-polarized digital signals in time-domain to X- and Y-polarized digital signals in frequency domain. The X- and Y-polarized digital signals in time domain are represented by x and y, and their corresponding X- and Y-polarized digital signals frequency domain may be represented by X and Y respectively. The output signals from FFT module **120** are as follows:

$$X=FFT(x)$$

$$Y=FFT(y).$$

(24) As illustrated in the example of FIG. **2**, the Rx DSP **100** includes an IQC unit **122** to compensate signals X and Y output from FFT module **120**. The IQC unit **122** is configured to compensate the In-phase Quadrature (IQ) skew and quadrature error of the signals in frequency domain. The Rx DSP **100** may first compensate In-phase Quadrature (IQ) skew and quadrature error in frequency domain X- and Y-polarized digital signals at IQC unit **122**. In-phase Quadrature Compensation (IQC) includes IQ skew compensation and quadrature error compensation. Due to imperfection of ICR **70**, in-phase and quadrature signals X and Y may have a delay or skew $\Delta\tau$ and quadrature errors ΔErr. The impairments caused by IQ skew and quadrature error are compensated in frequency domain by IQC unit **122** at the front-end of the Rx DSP **100** before compensation of other impairments. Unlike typical DSPs in which IQC is performed in the time domain, in Rx DSP **100**, the IQC unit **122** is in frequency-domain and performs IQC in frequency domain for further power reduction.

(25) Each of signals X and Y is a complex signal, which includes, in frequency domain, a first element I, and a second element Q. For example, signal X can be denoted as X=XI+jXQ, where

(26)
$$XI(k)=\frac{X(k)+X^*(N-k)}{2}$$
$$jXQ(k)=\frac{X(k)-X^*(N-k)}{2},$$

where N is the number of data samples, and K is an integer.

(27) In some examples, in IQ skew compensation, the IQC unit **122** compensates XQ according to

the function (where skew is represented as Δτ):
XQ=*XQ*.*Math*.*e*.sup.j2πfπΔτ.
(28) In quadrature compensation, the IQC unit **122** compensates XQ according to the function (where quadrature error is represented as ΔErr):
(29) $XQ = XQ + XI$ .Math. $\sin(\frac{\Delta Err}{\pi})$.
(30) The IQC unit **122** also compensates signal YQ and YI in frequency domain in the same manner as signal X as descried above. By compensating the signals X and Y at IQC unit **122**, the skew Δτ and quadrature errors ΔErr are eliminated from the signals X and Y output from IQC unit **122** to MIMO module **124**. The IQ compensated signals X and Y are input to the MIMO module **124** and the MIMO taps update module **130**.
(31) The 2×2 MIMO module **124** is configured to compensate for signal impairments in frequency domain, based on MIMO tap value inputs from the MIMO taps update module **130**, as will be described in greater detail in FIG. **3**.
(32) As illustrated in FIG. **2**, the output signals X and Y from the 2×2 MIMO module **124** are provided to IFFT module **126**. The IFFT module **126** is configured to convert the signals in frequency domain to signals in time domain. In order to update values of the MIMO taps update module **130**, the output signals X and Y from the 2×2 MIMO module **124** in the frequency domain are converted to time domain signals. The IFFT module **126** is configured to perform **2**N point IFFT to convert frequency domain digital signals X and Y to corresponding digital signals x and y in time domain.
(33) In the example of FIG. **2**, the time domain digital signals x and y output from the IFFT module **126** are provided to the save last block module **127**. The save last block module **127** removes first N samples from time domain digital signals x and y.
(34) In the example of FIG. **2**, after the save last block module **127** removes first N samples from time domain digital signals x and y, in an embodiment, the time domain digital signals x and y are input to the CR module **128**.
(35) The CR module **128** is configured to further compensate frequency offset and phase shift of the signals in time domain. The carrier frequency offset and phase shift compensated signals x and y are then provided to the MIMO taps update module **130**.
(36) In another embodiments, the time domain digital signals x and y output from the save last block module **127** are input to the MIMO taps update module **130**.
(37) The MIMO taps update module **130** is configured to update the MIMO tap values based on a time domain error signal associated with the signals output from the IFFT module **126**. In the example of FIG. **2**, the MIMO taps update module **130** comprises a slicer **129**, a first adder **150**, an insert zero block module **152**, a second FFT module **140**, a second multiplier **142**, a conjugate module **141**, gradient constraint unit **144**, a third multiplier **146**, a delay element **148**, and a second adder **154**.
(38) The slicer **129** is configured to generate, based on the carrier frequency offset and phase shift compensated signals x and y output from the save last block module **127**, a desired response.
(39) The first adder **150** subtracts the output of the save last block module **150** from the desired response from the slicer **129** to generate a time domain error signal. The length of the time domain error signal is N.
(40) The time domain error signal is provided to insert zero block module **152**. The insert zero block module **152** is configured to add a block of N zeros to the time domain error signal in order to make the length of the error signal to **2**N. The second FFT module **140** performs **2**N point FFT to convert the time domain error signal into frequency domain error signals E(m), which includes E.sub.x(m) and E.sub.y(m) in X-polarization and Y-polarization respectively. The X- and Y-polarized frequency domain error signals E.sub.x(m) and E.sub.y(m) are provided to the second multiplier **142**.
(41) The conjugate module **141** conjugates the frequency domain signals X, Y output from the IQC

module **122**, which are IQ compensated as described above. The conjugate module **141** provides conjugated signals [X,Y] to the second multiplier **142**. The second multiplier **142** multiplies the conjugated signals [X,Y] with X- and Y-polarized frequency domain error signals E.sub.x(m) and E.sub.y(m), and provides the resultant to the gradient constraint unit **144**.
(42) The gradient constraint unit **144** is configured to generate a gradient constraint G{.Math.} from the output of the multiplier **142**. Typically, the gradient constraint unit **144** performs IFFT on the received signals having a length of 2N, deletes last N samples of the time domain received signal, and adds a block of N zeroes and performs **2**N point FFT to the gradient constraint G{.Math.}. The gradient constraint G{.Math.} is multiplied with μ by the third multiplier **146** to generate updated MIMO taps update module **130**.
(43) In FIG. **2**, In order to provide the 2×2 MIMO module **124** with current MIMO tap values W(m), the second adder **154** and the delay element **148** of the MIMO taps update module **130** provide a delay. The MIMO taps update module **130** forwards the current MIMO tap values W(m) to the MIMO module **124** and the timing error calculator **132** for compensating impairments of digital signals.
(44) The timing error calculator **132** is configured to determine a timing error in Baud τ.sub.Baud of the signals based on the input W(m) generated from the MIMO taps update module **130**.
(45) Using τ.sub.Baud, the loop filter **134** is configured to tune the VCO **90**. The VCO **90** is configured to adjust the sampling clock frequency of Rx ADC **80**.
(46) FIG. **3** is a flowchart showing an operational process **200** of the Rx DSP **100** for compensating further impairments of signals X and Y. After IQC unit **122** compensates signals X and Y for impairments of IQ skew and quadrature error, the signals X and Y may be provided to MIMO module **124** for further compensating of impairments.
(47) At step **202**, the MIMO module **124** estimates a chromatic dispersion (CD) and generates a compensation response of fixed impairments H.sub.comp in the frequency domain to compensate fixed impairments. H.sub.comp is a vector. The compensation response of the fixed impairments H.sub.comp may be obtained by CD estimation (CDE) and S**21** calibration.
(48) At step **204**, the MIMO module **124** sets the initial value for MIMO taps update module **130** for the 2×2 MIMO module **124** as
W.sub.xx=*W*.sub.yy=[1 1 1 . . . 1].Math.*H*.sub.comp*;* *W*.sub.xy=*W*.sub.yx=[0 0 0 . . . 0].
(49) The initial value of the MIMO taps update module **130** is saved for use in a blind equalization at step **208** to be described below.
(50) At step **206**, the MIMO module **124** is configured to perform a two-dimensional clock frequency offset and carrier frequency offset scanning. The scanning uses the training symbols inserted in the signals at the transmitter **12**. At the Tx DSP **20** in time domain, a plurality of training symbols, such as **16** training symbols, are inserted in the digital signals. The plurality of training symbols form a training sequence (TrainSeq). The training symbols are therefore also included in the digital signals received by the Rx DSP **100**. The Rx DSP **100** at the receiver **14** is pre-configured with the same training symbol information as the transmitter **12**, such as clock frequency of the training symbols, and the number of the training symbols.
(51) The two-dimensional clock frequency offset and carrier frequency offset scanning estimates the clock frequency offset between Tx DAC **30** and Rx ADC **80**, and the carrier frequency offset between Tx Laser **60** and Rx Laser **75**.
(52) Due to the separate and independent sampling clocks of the Tx DAC **30** and the Rx ADC **80**, there can be a sampling clock difference between the sampling clocks. After the signal is processed at the Rx ADC **80**, the signal may include a variable sampling delay t at the time domain, and may be denoted as below:
signal(t−τ),
where signal (t) denotes both x(t) and y(t) in X- and Y-polarizations in time domain.
(53) The delay t causes a sampling phase offset, and the sampling phase offset can be time varying

due to clock frequency offset and random phase jitter. The sampling phase offset is equivalent to a phase shift $e^{j2\pi f\tau}$ of the signal in frequency domain:

$$fft(\text{signal}(t))\cdot e^{j2\pi f\tau}$$

where fft(signal(t)) denotes both signals X and Y in frequency domain.

(54) Blind equalizers, such as Constant Modulus Algorithm (CMA) and Least Mean Squares (LMS), can compensate the clock frequency offset to a limited extent. However, blind LMS can only lock within a limited clock frequency offset range, for example smaller than 20 ppm. If the signal has a clock frequency offset greater than 20 ppm, clock frequency offset scanning is used to roughly estimate the clock frequency offset and to ensure the convergence of blind LMS.

(55) Clock frequency offset scanning estimates the clock frequency offset between the clock of Tx DAC **30** and Rx ADC **80**. The MIMO module **124** is configured to scan the clock frequency offset Δf_{clk} by adjusting the control signal of VCO **90**. In some examples, the MIMO module **124** correlates the digital signal with the training sequence (TrainSeq) to perform the clock frequency offset scanning. Based on the correlation between the training sequence and the digital signal under different scan values of Δf_{clk}, the estimated clock frequency offset corresponds to the scan value at the maximum correlation peak value. Under each scanning value of Δf_{clk}, the maximum correlation peak value can be determined by multiplying the digital signal at symbol rate in frequency domain with the conjugate of training sequence (TrainSeq) in frequency domain as denoted below:

$$\text{correlation peak}=\max[\text{ifft}(\text{conj}(fft(\text{TrainSeq}))\cdot fft(\text{signal}(t)))]$$

which corresponds to correlation of the training sequence and signal in time domain:

$$\text{correlation peak}=\max[\text{TrainSeq}*(\text{signal}(t))]$$

where (*) denotes correlation in time domain, which corresponds to vector conjugate multiplication (conj( ).Math.) in frequency domain.

(56) The maximum correlation peak value of the digital signal at a symbol rate with the training sequence (TrainSeq) corresponds to the minimum residual clock frequency offset with the VCO adjusting. After the scan value of clock frequency offset at the maximum correlation peak value is identified, the VCO **90** is configured to compensate Rx clock frequency offset with the estimated frequency offset value $\Delta f_{clk\text{-}est}$. If the clock frequency offset is too big, the blind LMS cannot converge. As the carrier frequency offset also affects the maximum correlation value, another scanning dimension for carrier frequency offset estimation is also used in a two-dimensional clock frequency offset and carrier frequency offset scanning to ensure a reliable clock frequency offset scanning.

(57) As described above, due to the separation and independence of Tx laser **60** and Rx laser **75**, there can be a central frequency difference Δf, also known as carrier frequency offset, between Tx laser **60** and Rx laser **75**. The value of Δf can be several GHz.

(58) The carrier frequency offset scanning is based on the correlation between the training sequence and the digital signal with the frequency difference Δf. In time-domain compensation schemes, a time-domain numeral controlled oscillator (NCO) is used to compensate carrier frequency offset Δf to the digital signal. The estimated carrier frequency offset Δf_{est} corresponds to the scan value of frequency difference at the maximum correlation value.

(59) However, the frequency domain compensation performed by Rx DSP **100** at IQC unit **122** does not include a time-domain NCO. As frequency point spacing=sample rate/FFT size, frequency shift can be used to adjust frequency offset in low capacity cases. However, the resolution of the frequency shift in high capacity cases is too low to have a good frequency offset shift.

(60) In Rx DSP **100**, the MIMO module **124** is configured to perform a carrier frequency offset scanning in frequency domain. The carrier frequency offset scanning in time domain corresponds to the equations (a) and (b) below:

$$(\text{TrainSeq}\cdot e^{j2\pi\Delta ft})*\text{signal}(t) \qquad \text{(a)}$$

which is equivalent to

TrainSeq*(signal(t).Math.e.sup.−j2πΔft) (b)
in equations (a) and (b) above, e.sup.j2πΔft is the NCO for determining the carrier frequency offset Δf, and * denotes correlation operation.

(61) Both equations (a) and (b) may obtain the carrier frequency offset estimation. In equation (a), the training sequence is already factored in NCO, the MIMO module **124** adds different frequency offsets in the training sequence, and therefore, the NCO does not need to be determined in the digital signal. In equation (b), as the training sequence is not factored in the NCO, the NCO would be required to be calculated in the digital signal when the MIMO module **124** performs carrier frequency offset scanning. As such, the digital signal has to be first transformed back to time domain, and after NCO transformed back to frequency domain, which causes substantial extra complexity and power consumption. Therefore, in example embodiments, equation (a) is used instead of equation (b), because equation (a) enables the training sequence to be pre-processed with NCO, and is ready for use to directly correlate with the input digital signal.

(62) As the carrier frequency offset also affects the maximum correlation value, the clock frequency offset scanning and carrier frequency offset scanning are simultaneously performed in a two-dimensional (2D) clock frequency offset and carrier frequency offset scanning, in order to obtain a relatively accurate estimation of clock frequency offset. As such, a 2D clock frequency offset and carrier frequency offset scanning simultaneously determines the estimation of sampling frequency offset Δf.sub.clk-est and carrier frequency offset Δf.sub.est in the digital signal. A reliable clock recovery in a T/1 receiver system typically is difficult. However, a 2D clock frequency offset and carrier frequency offset scanning ensures accuracy and stability for locking the sampling clock of the digital signal.

(63) At step **206**, the 2×2 MIMO module **124** performs a two-dimensional clock frequency offset and carrier frequency offset scanning based on the training sequence (TrainSeq) formed by the training symbols used at the transmitter **12**. The input signals X and Y to the 2×2 MIMO module **124** are IQ compensated signals X and Y in frequency domain from the IQC unit **122**. As discussed above, the signals X and Y input to the MIMO module **124** are a two-dimensional vector [X, Y], where:

$X = fft(\text{signalx})$

$Y = fft(\text{signaly})$

(64) As discussed above, the sampling phase offset and carrier frequency offset still exist in the signal x and signal y. In order to determine the clock frequency offset estimation Δf.sub.clk-est and carrier frequency offset estimation Δf.sub.est, a 2D clock frequency offset and carrier frequency offset scanning is performed at the MIMO module **124** by multiplying the input signal X and Y with the values in the MIMO taps update module **130**, which is a 2×2 array in frequency domain:

(65) $\begin{bmatrix} W_{xx} & W_{xy} \\ W_{yx} & W_{yy} \end{bmatrix}$

The values of MIMO taps update module **130** are:

W.sub.xx=W.sub.xy=conj(fft(TrainSeqx.Math.e.sup.jπΔft))

W.sub.yy=W.sub.yx=conj(fft(TrainSeqy.Math.e.sup.jπΔft))

(66) The clock frequency offset estimation Δf.sub.clk-est and carrier frequency offset estimation Δf.sub.est correspond to the scan value at the maximum correlation peak value.

(67) In a 2D clock frequency offset and carrier frequency offset scanning, the MIMO module **124** scans the carrier frequency offset Δf. The VCO **90**, which is controlled by the MIMO module **124** of the Rx DSP **100**, adjusts the clock frequency offset Δf.sub.clk. The output of IFFT module **126** corresponds to the correlation result between the received digital signal X and Y with the known training sequences TrainSeqx, and TrainSeqy. The correlation maximum peak value is saved during each scanning that includes both clock frequency offset scanning and carrier frequency offset scanning. After the 2D clock frequency offset and carrier frequency offset scanning, the MIMO

module **124** performs a 2D search to identify the maximum correlation peak value between the received digital signal X and Y with the known training sequences TrainSeqx, and TrainSeqy. The maximum correlation peak value determines the clock frequency offset estimation Δf.sub.clk-est and carrier frequency offset estimation Δf.sub.est.
(68) The VCO **90** is configured to adjust the sampling clock frequency of ADC **80** with a −Δf.sub.clk-est that corresponds to the estimated clock frequency offset Δf.sub.clk-est. After this initial compensation, the residual clock frequency offset of signals x and y output from ADC **80** is reduced, for example, to less than 20 ppm. With the reduced residual clock frequency offset of signals X and Y, the MIMO module **124** may easily converge at blind equalizer step **208**, such as a Blind LMS stage, and accurately and stably lock the sampling clock of the signals X and Y at a Timing Recovery (TR) stage. In some examples, the IQC unit **122** may roughly compensate the signals X and Y in frequency domain by the estimated carrier frequency offset estimation Δf.sub.est with an approximate frequency shift−Δf.sub.est′. In some examples, the CR module **128** may compensate the entire or residual carrier frequency offset of signals X and Y.
(69) After the signals X and Y are compensated with the initial estimated clock frequency offsets, at step **208**, the MIMO module **124** equalizes digital signals X and Y in frequency domain. At step **208**, MIMO module **124** uses the MIMO tap values set at step **204** as follows:
W.sub.xx=*W*.sub.yy=[1 1 1 . . . 1].Math.*H*.sub.comp*;* *W*.sub.xy=*W*.sub.yx=[0 0 0 . . . 0]
and the MIMO module **124** equalizes the input signals X=fft(signalx) and Y=fft(signaly) by multiplying the X=fft(signalx) and Y=fft(signaly) with the MIMO taps values at the MIMO taps update module **130**.
(70) The output signals X and Y are updated according to the equations (1) and (2) below:
X=*X.Math.W*.sub.xx+*Y.Math.W*.sub.yx (1)
Y=*X.Math.W*.sub.xy+*Y.Math.W*.sub.yy (2)
At step **208**, in some examples, the carrier recovery (CR) is bypassed and not involved in the signal processing process.
(71) During the blind equalization process at step **208**, in order to determine that the appropriate values of the MIMO taps update module **130**, the MIMO module **124** is configured to continuously update the values of the MIMO taps update module **130**. The criteria whether the MIMO module **124** is locked will be described in detail at step **210** below.
(72) In the example of FIG. **2**, the output of the IFFT module **126** is used to update the MIMO tap values of the taps update module **130**, according to the following equations:
W.sub.xx(*m*+1)=*W*.sub.xx(*m*)+2μ.Math.*G*{*E*.sub.x(*m*)*X**(*m*)} (3)
W.sub.yx(*m*+1)=*W*.sub.yx(*m*)+2μ.Math.*G*{*E*.sub.x(*m*)*Y**(*m*)} (4)
W.sub.xy(*m*+1)=*W*.sub.xy(*m*)+2μ.Math.*G*{*E*.sub.y(*m*)*X**(*m*)} (5)
W.sub.yy(*m*+1)=*W*.sub.yy(*m*)+2μ.Math.*G*{*E*.sub.y(*m*)*Y**(*m*)} (6)
where X*(m) and Y*(m) are conjugate of the frequency domain digital signals containing X(m) and Y(m) in x and y polarization respectively, E.sub.x(m) and E.sub.y(m) are error signals associated with the frequency domain digital signals X(m) and Y(m) respectively, and G{.Math.} is a gradient constraint, and μ is a step function representing a step size.
(73) The MIMO taps update module **130** in FIG. **2** can update the MIMO tap values in accordance with equations (3)-(6).
(74) The updated MIMO taps values are then used to update the signals X and Y using the Equations (1)-(2) above.
(75) At step **210**, the MIMO module **124** determines whether MIMO module **124** is locked or converged. If the root mean square (rms) value of the time domain error signal generated by the first adder **150** is smaller than a threshold set by the MIMO module **124**, the MIMO module **124** is locked or converged.
(76) If the MIMO module **124** is not locked, MIMO module **124** repeats step **208** to update the MIMO taps update module **130** in accordance with the equations (3)-(6), and to update the signals

X and Y in accordance with the equations (1) and (2) until the rms value of the time domain error signal generated by the first adder **150** is smaller than the threshold.
(77) After the MIMO module **124** is locked, at step **212**, the Rx DSP **100** continues to perform timing recovery (TR) by calculating timing error in Baud τ.sub.Baud using the timing error calculator **132**. The timing error calculator **132** in FIG. **2** uses the output W(m) from the adder **154** to obtain the determinant as follows:
detW=*W*.sub.xx*W*.sub.yy−*W*.sub.xy*W*.sub.yx.
(78) The timing error calculator **132** derives the angle of the determinant, which contains timing error information represented by the equation below:
(79)
$\varphi = \angle(\text{detW}) = 2\pi f \tau = 2\pi \frac{k}{N} f_s \tau = 2\pi \frac{k}{N} f_{Baud} \tau = 2\pi \frac{k}{N} \frac{\tau}{T_{Baud}} = 2\pi \frac{k}{N} \tau_{Baud}, k \in [0: N - 1]$,
where N is the number of the sample data points, k is an integer, and
(80) $f = \frac{k}{N} f_s$, k is an integer smaller than N, fs is a sampling rate equal to the baud rate.
(81) The mean of difference of φ is:
(82) $\overline{\text{diff}}(\varphi) = \frac{2\pi}{N} \tau_{Baud}$
and τ.sub.Baud is:
(83) $\tau_{Baud} = \frac{\overline{\text{diff}}(\varphi) \text{ .Math. } N}{2\pi}$
(84) Using τ.sub.Baud, the loop filter **134** in FIG. **2** tunes the VCO **90** by the following filter:
loopFilt=(τ.sub.Baud(*n*)−τ.sub.Baud(*n*−1)*μ.sub.p+sign(τ.sub.Baud(*n*)*μ.sub.i (7)
where μ.sub.p and μ.sub.i are step sizes, n is an integer.
(85) In some examples, the loop filter 134 tunes the VCO **90** by the following filter:
loopFilt=sign(τ.sub.Baud(*n*)−τ.sub.Baud(*n*−1)**k*.sub.p+sign(τ.sub.Baud(*n*)**k*.sub.i (8)
where k.sub.p and k.sub.i are step sizes.
(86) Filter (**8**) converges faster than filter (**7**) by using the sign ( ) function.
(87) VCO **90** in turn adjusts the sampling operation of the ADC **80** such that the timing error t Baud generated at the ADC **80** may be further reduced. At step **214**, if the RMS value of timing errors τ.sub.Baud of recent p blocks of data is less than or equal to a threshold, the timing recovery (TR) of the MIMO module **124** is locked. If τ.sub.Baud is greater than the threshold at step **214**, MIMO module **124** repeats steps **208-214** until timing error τ.sub.Baud is less than or equal to the threshold and the timing recovery (TR) is locked.
(88) In FIG. **3**, after the TR is locked, to synchronize the frames of the digital signals X and Y at the receiver **14**, the MIMO module **124** proceeds to a framer process at step **216** in order to determine the position of the training symbols in the digital signals X and Y.
(89) Before the framing process, the MIMO module **124** saves the converged MIMO tap values as H.sub.xx, H.sub.yy, H.sub.xy, H.sub.yx.
(90) At step **216**, during the framing process, the MIMO module **124** correlates the timing recovered digital signal X and Y in frequency domain with the correlation results of the training sequence in frequency domain and the converged MIMO taps after blind equalizer at step **208**.
(91) In some examples, at step **216**, the timing recovered digital signals X and Y input to the MIMO module **124** are denoted as:
X=*fft*(signalx)
Y=*fft*(signaly)
x and y are timing recovered signals at step **212**.
(92) The values of the MIMO taps update module **130** are the vector multiplication results of the frequency domain training sequences in X and Y polarizations and respective MIMO taps update module **130** before framing process:
W.sub.xx=*fft*(TrainSeqx).Math.*H*.sub.xx
W.sub.yy=*fft*(TrainSeqy).Math.*H*.sub.yy
W.sub.xy=*fft*(TrainSeqx).Math.*H*.sub.xy

$W_{yx}=fft(TrainSeqy)\cdot H_{yx}$

where TrainSeqx, TrainSeqy are formed by the training symbols in the X and Y-polarized signals, and H_{xx}, H_{yy}, H_{xy}, H_{yx} are vectors containing converged MIMO taps values before framing process.

(93) By correlating (multiplying in frequency domain) the input digital signals with MIMO taps update module **130** at the MIMO module **124**, the MIMO module **124** derives the position of the training symbols in a frame in accordance with the position of the maximum correlation value.

(94) At step **216**, the MIMO module **124** suspends the MMO taps updating and timing recovery (TR) during the framer process. As MIMO module **124** has already been locked at step **216**, only limited number of blocks of data is sufficient in the framing process to identify the training symbol position in the frame.

(95) In short-reach applications, for example the distance between the transmitter **12** and the receiver **14** is within 40 Kilometers, as the adaptive channel impairments varies slowly and timing variation is slow, temporary suspension of MIMO and TR updating generally does not affect performance, such as Bit Error Rate (BER). In the worse circumstance, the framer may be misaligned by one or more symbols. Due to the misalignment, the estimated timing error may shift by one or more symbols. Although the timing error τ_{Baud} may gradually reduce to 0, the BER of the digital signals may increase.

(96) To solve this problem, the MIMO module **124** may adjust a framer index by the number of symbols corresponding to the number of symbols of a timing error shifting. For example, once the timing error is shifted by one or more symbols after framer at step **216**, the MIMO module **124** may accordingly adjust framer index by one or more symbols to reduce the BER. As such, the BER may be maintained at an acceptable range.

(97) Before the framer synchronization, as discussed above, as the location of the training symbol at the step **208** is unknown, the MIMO taps update module **130** is updated by the desired response generated by the slicer **129**. After the famer synchronization at step **216**, the MIMO module **124** is able to identify the position of the training symbols in a frame, and the location of payload data in a frame. As such, the MIMO module **124** may further update the MIMO taps update module **130** with the training symbols to further compensate the impairment at step **218**.

(98) At step **218**, MIMO module **124** turns on the CR module **128** in FIG. **2** and uses training symbols to further update the MIMO taps update module **130**. The input signal to the MIMO module **124** are denoted as follows:

$X=fft(signalx)$

$Y=fft(signaly)$

where x and y are TR locked digital signals in time domain. The initial value of the MIMO taps update module **130** at step **218** are as follows:

$W_{xx}=H_{xx}$

$W_{yy}=H_{yy}$

$W_{xy}=H_{xy}$

$W_{yx}=H_{yx}$

where H_{xx}, H_{yy}, H_{xy}, H_{yx} are vectors containing converged MIMO taps before framing process.

(99) In the example of FIG. **2**, after the save last block module **127** removes first N samples from time domain digital signals x and y, the time domain digital signals x and y are input to the CR module **128**. The CR module **128** is configured to compensate the carrier frequency offset and phase shift in signals x and y. The carrier frequency offset and phase shift compensated signals x and y are then provide to the slicer **129**.

(100) The slicer **129**, based on the identified position of the training symbols in the digital signals x and y at step **216**, compares the training symbols in the digital signals x and y from the save last block module **127** with the standard training symbols, and compares the payload portion with a

desired response. The slicer **129** generates a time domain error signal using the comparison results of the training symbols and the payload. By using the training symbols as the reference value, the slicer **129** can more accurately determine the error signal than using blind desired response at step **208**.
(101) The time domain error signal is provided to insert zero block module **152** for updating the MIMO taps update module **130** as described at step **208** above. The MIMO taps update module **130** may be updated in accordance with equations (3)-(6) described above, and MIMO module **124** updates the signal X and Y in frequency domain in accordance with equations (1)-(2).
(102) The digital signals output from the CR module **128** may be used for further processing by the Rx DSP **100**, such as Forward Error Correction (FEC).
(103) At step **218**, the MIMO module **124** updates the MIMO taps until the rms value of a time domain error of the digital signal X- and Y-polarizations is smaller than or equal to a second predetermined threshold. In some examples, the second predetermined threshold is smaller than the first predetermined threshold used for equalizing the digital signals at step **208**. As such, at step **218**, the errors in signals X and Y is in a smaller scale than the blind equalizing processing step **208** without using the training symbols.
(104) For each subsequent signal received by the Rx DSP **100**, the MIMO module **124** may update MIMO taps update module **130** using only step **218**, without performing steps **202-216**.
(105) As described above, the frequency domain signals X and Y are multiplied at the MIMO module **124** with the vectors of MIMO taps update module **130** for various impairment compensations. Frequency domain vector multiplication corresponds to correlation operation in time domain. As the MIMO module **124** processes the X and Y signals by vector in frequency domain, the processing speed of MIMO module **124** in frequency domain is therefore faster than processing one signal at a time in the time domain. As such, processing the X and Y signals in frequency domain by the MIMO module **124** also saves power.
(106) In some examples, the MIMO module **124** may be a single-stage FDMIMO for the Rx DSP **100** to further reduce power consumption. Single-stage FDMIMO is disclosed in a related patent application No. 63/010,827, entitled "System and Method for signal-stage Frequency-Domain Equalization", filed on Apr. 16, 2020, the content of which is incorporated herein in its entirety by reference.
(107) The Rx DSP **100** for the receiver **14** provides a low-power and efficient symbol-rate Rx DSP scheme. FIG. **4** shows BER performance comparison of T/1.25 (sampling rate=1.25*symbol rate) DSP and T/1 Rx DSP **100** at a receiver **14** in terms of received optical power (ROP) at ideal and typical test cases, respectively. Compared with T/1.25, the power consumption of Rx DSP **100** in T/1 in the present disclosure can be saved by around 20% for ADC **80**. The total saved power by the T/1 Rx DSP **100** may reach 30%.
(108) It should be noted that for all the tests measured, S**21** is used for both the transmitter **12** and receiver **14**, and that the ideal case is B2B case with no impairments except for S**21**, while 'typical' case corresponds to a 10 km transmission scenario with various impairments.
(109) In ideal case, Rx DSP **100** performs 0.2 dB worse than T/1.25 at a Forward Error Correction (FEC) threshold of 1.25e-2. This penalty comes from imperfection of S**21** shape and aliasing. While in typical case, Rx DSP **100** performs 0.7 dB worse than T/1.25. The increased penalty in the typical case comes from the limited ability of impairment compensation in T/1, such as skew compensation. However, the penalty is acceptable for the low-power design.
(110) FIG. **5** is a block diagram, illustrating an example hardware structure of the Rx DSP **100**. In FIG. **5**, the Rx DSP **100** comprises a processing unit **102**, an Input/Output (I/O) interface **104**, and a memory **108**.
(111) The processing unit **102** may be a processor, a microprocessor, an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a dedicated logic circuitry, or combinations thereof.

(112) The input/output (I/O) interfaces **104** allows to receive input digital signals **105** from the ADC **80** and to transmit processed digital signals **106** for further processing in system **10**.
(113) The memory **108** may include a volatile or non-volatile memory e.g., a flash memory, a random-access memory (RAM), and/or a read-only memory (ROM). The non-transitory memory **108** may store instructions for execution by the processing unit **102**, such as to carry out methods or processes described in the example of the present disclosure. The memory **108** may include other software instructions, such as for implementing an operating system and other applications/functions.
(114) In the Rx DSP **100**, the Fast Fourier Transformation (FFT) module **120**, IQC unit **122**, 2×2 multiple input multiple output (MIMO) **124**, IFFT module **126**, Carrier Recovery (CR) module **128** and the timing error calculator **132** may be implemented by the processing unit **102**, and MIMO taps updating module **130** may be implemented in the processing unit **102** and memory **108**.
(115) In some other examples, memory **108** may be provided by a transitory or non-transitory computer-readable medium. Examples of non-transitory computer readable media include a RAM, a ROM, an erasable programmable ROM (EPROM), an electrically erasable programmable ROM (EEPROM), a flash memory, a CD-ROM, or other portable memory storage.
(116) The bus **110** providing communication channels among components of the Rx DSP **100**, including the processing unit **102**, I/O interface **104**, and/or memory **108**. The bus **108** may be any suitable bus architecture including, for example, a memory bus, or a peripheral bus.
(117) Although the present disclosure describes methods and processes with steps in a certain order, one or more steps of the methods and processes may be omitted or altered as appropriate. One or more steps may take place in an order other than that in which they are described, as appropriate.
(118) An example embodiment is a method for processing signals in a receiver, comprising: receiving a digital signal at a symbol rate in frequency domain; and compensating an impairment of the digital signal in frequency domain.
(119) In another example embodiment, in the preceding methods, compensating the impairment comprises compensating the digital signal in an in-phase and quadrature skew and a quadrature error in frequency domain.
(120) In another example embodiment, in the preceding methods, the in-phase and quadrature skew of the digital signal in X polarization is compensated by
$XQ{=}XQ.Math.e$.sup.j2πΔτ
where XQ is a phase Q of signal X in frequency domain, and Δτ is a skew of signal X.
(121) In another example embodiment, in the preceding methods, the quadrature error of the digital signal in X polarization is compensated by
(122) $XQ = XQ$ + XI .Math. sin($\frac{\Delta Err}{II}$)
where XI is phase I of the digital signal in X polarization in frequency domain, and ΔErr is quadrature errors of the digital signal in X polarization.
(123) In another example embodiment, in the preceding methods, compensating the impairment comprises: determining, at a 2×2 multiple input multiple output (MIMO), a clock frequency offset estimation Δf.sub.clk-est and a carrier frequency offset estimation Δf.sub.est in the digital signal; and adjusting a sampling clock frequency of an analog to digital convertor (ADC) of the receiver by a −Δf.sub.clk-est.
(124) In another example embodiment, the preceding methods further comprise: compensating, at an In-phase Quadrature Compensation (IQC), the digital signal in frequency domain by a −Δf.sub.est.
(125) In another example embodiment, in the preceding methods, the Δf.sub.clk-est and the Δf.sub.est is determined by correlating in frequency domain, at the 2×2 MIMO, digital signals x and y in time domain in X- and Y-polarizations with a MIMO taps:

(126) $[\begin{matrix} W_{xx} & W_{xy} \\ W_{yx} & W_{yy} \end{matrix}]$

$X = fft(\text{signalx})$

$Y = fft(\text{signaly})$

where:

$W_{xx} = W_{xy} = \text{conj}(fft(\text{TrainSeqx} \cdot e^{j2\pi\Delta ft}))$

$W_{yy} = W_{yx} = \text{conj}(ft(\text{TrainSeqy} \cdot e^{j2\pi\Delta ft}))$

and where TrainSeqx and TrainSeqy are training sequences of signals x and y in X- and Y-polarizations, respectively, wherein the $\Delta f_{clk\text{-}est}$ and the Δf_{est} correspond to scan values at a maximum correlation peak value.

(127) In another example embodiment, in the preceding methods, compensating the impairment of the digital signal comprises: equalizing the digital signals in X- and Y-polarizations in frequency domain until a time domain error signal of the digital signal X- and Y-polarizations is less than or equal to a predetermined threshold.

(128) In another example embodiment, in the preceding methods, equalizing the digital signals in X- and Y-polarizations in frequency domain comprises: correlating the digital signals in X- and Y-polarizations in frequency domain with the MIMO taps, wherein values of the MIMO taps are:

$W_{xx} = W_{yy} = [1\ 1\ 1\ \ldots\ 1] \cdot H_{comp}$; $W_{xy} = W_{yx} = [0\ 0\ 0\ \ldots\ 0]$

and updating the digital signals in X- and Y-polarizations by

$X = X \cdot W_{xx} + Y \cdot W_{yx}$, $Y = X \cdot W_{xy} + Y \cdot W_{yy}$

where H_{comp} is a compensation response to compensate non-time-varying fixed impairments.

(129) In another example embodiment, in the preceding methods, equalizing the digital signals in X- and Y-polarizations in frequency domain comprises: updating the MIMO taps by

$W_{xx}(m+1) = W_{xx}(m) + 2\mu \cdot G\{E_x(m)X^*(m)\}$

$W_{yx}(m+1) = W_{yx}(m) + 2\mu \cdot G\{E_x(m)Y^*(m)\}$

$W_{xy}(m+1) = W_{xy}(m) + 2\mu \cdot G\{E_y(m)X^*(m)\}$

$W_{yy}(m+1) = W_{yy}(m) + 2\mu \cdot G\{E_y(m)Y^*(m)\}$ where $X^*(m)$ and $Y^*(m)$ are conjugate of the frequency domain digital signals containing X(m) and Y(m) in x and y polarization respectively, $E_x(m)$ and $E_y(m)$ are error signals associated with the frequency domain digital signals X(m) and Y(m) respectively, and $G\{\cdot\}$ is a gradient constraint, and μ is a step function.

(130) In another example embodiment, the preceding methods further comprise: determining a timing error τ_{Baud} of the digital signal; and tuning, by a loop filter, a voltage-controlled oscillator (VCO) until the timing error is less than or equal to a threshold.

(131) In another example embodiment, in the preceding methods, the timing error τ_{Baud} is determined based on

(132) 0

$$\tau_{Baud} = \frac{\overline{\text{diff}}(\varphi) \cdot N}{2\pi}$$

$$\varphi = \text{unwrap}(\text{angle}(\text{fftshift}(\text{detW}))) = 2\pi f \tau = 2\pi \frac{(0{:}\,N-1)}{N} \tau_{Baud}$$

$\text{detW} = W_{xx} * W_{yy} - W_{xy} * W_{yx}$ where W_{xx}, W_{yy} W_{xy}. W_{yx} are converged MIMO tap values, N is sample data point number, and $f = k/Nf_s$ is a frequency of the digital signals, K is an integer smaller than N, fs is a sampling rate equal to a baud rate.

(133) In another example embodiment, in the preceding methods, the loop filter tunes the VCO using a following equation:

$\text{loopFilt} = (\tau_{Baud}(n) - \tau_{Baud}(n-1) * \mu_p + \text{sign}(\tau_{Baud}(n) * \mu_i$

where μ_p and μ_i are step sizes.

(134) In another example embodiment, in the preceding methods, the loop filter tunes the VCO using the following equation:

$\text{loopFilt} = \text{sign}(\tau_{Baud}(n) - \tau_{Baud}(n-1)) * k_p + \text{sign}(\tau_{Baud}(n)) * k_i$

where k.sub.p and k.sub.i are step sizes.
(135) In another example embodiment, the preceding methods further comprise: suspending MIMO and timing recovery updating; and determining a position of training symbols in the digital signal.
(136) In another example embodiment, in the preceding methods, determining the position of training symbols in the digital signal comprises: correlating timing error recovered digital signal in X- and Y-polarizations in frequency domain with the MIMO taps having values of:
W.sub.xx=*fft*(TrainSeqx).Math.*H*.sub.xx
W.sub.yy=*fft*(TrainSeqy).Math.*H*.sub.yy
W.sub.xy=*fft*(TrainSeqx).Math.*H*.sub.xy
W.sub.yx=*fft*(TrainSeqy).Math.*H*.sub.yx
where TrainSeqx and TrainSeqy are formed by the training symbols in the X and Y-polarized signals in time domain, and H.sub.xx, H.sub.yy, H.sub.xy, H.sub.yx are converged MIMO taps after equalizing the digital signal in X- and Y-polarizations in frequency domain.
(137) In another example embodiment, the preceding methods further comprise adjusting, by the 2×2 MIMIO, a framer index corresponding to a timing error shifting amount.
(138) In another example embodiment, the preceding methods further comprise: determining a time domain error of the digital signal X- and Y-polarizations in time domain by using training symbols; and updating MIMO taps until the time domain error of the digital signal X- and Y-polarizations is smaller than or equal to a second predetermined threshold.
(139) In another example embodiment, in the preceding methods, updating the MIMO taps comprises updating the MIMO taps by:
W.sub.xx(*m*+1)=*W*.sub.xx(*m*)+2μ.Math.*G{E*.sub.x(*m*)*X**(*m*)}
W.sub.yx(*m*+1)=*W*.sub.yx(*m*)+2μ.Math.*G{E*.sub.x(*m*)*Y**(*m*)}
W.sub.xy(*m*+1)=*W*.sub.xy(*m*)+2μ.Math.*G{E*.sub.y(*m*)*X**(*m*)}
W.sub.yy(*m*+1)=*W*.sub.yy(*m*)+2μ.Math.*G{E*.sub.y(*m*)*Y**(*m*)}. where X*(m) and Y*(m) are conjugate of the frequency domain digital signals containing X(m) and Y(m) in x and y polarization respectively, E.sub.x(m) and E.sub.y(m) are error signals associated with the frequency domain digital signals X(m) and Y(m) respectively, G{ } is a gradient constraint, and μ is a step function, wherein initial value of the MIMO taps are as follows:
W.sub.xx=*H*.sub.xx
W.sub.yy=*H*.sub.yy
W.sub.xy=*H*.sub.xy
W.sub.yx=*H*.sub.yx.
(140) In another example embodiment, in the preceding methods, the second predetermined threshold is smaller than the predetermined threshold.
(141) In another example embodiment, the preceding methods further comprise compensating for frequency offset and phase shift of the digital signals using a carrier recovery.
(142) Although the present disclosure is described, at least in part, in terms of methods, a person of ordinary skill in the art will understand that the present disclosure is also directed to the various components for performing at least some of the aspects and features of the described methods, be it by way of hardware components, software or any combination of the two. Accordingly, the technical solution of the present disclosure may be embodied in the form of a software product. A suitable software product may be stored in a pre-recorded storage device or other similar non-volatile or non-transitory computer readable medium, including DVDs, CD-ROMs, USB flash disk, a removable hard disk, or other storage media, for example. The software product includes instructions tangibly stored thereon that enable a processor device (e.g., a personal computer, a server, or a network device) to execute examples of the methods disclosed herein.
(143) The present disclosure may be embodied in other specific forms without departing from the subject matter of the claims. The described example embodiments are to be considered in all respects as being only illustrative and not restrictive. Selected features from one or more of the

above-described embodiments may be combined to create alternative embodiments not explicitly described, features suitable for such combinations being understood within the scope of this disclosure.
(144) All values and sub-ranges within disclosed ranges are also disclosed. Also, although the systems, devices and processes disclosed and shown herein may comprise a specific number of elements/components, the systems, devices and assemblies could be modified to include additional or fewer of such elements/components. For example, although any of the elements/components disclosed may be referenced as being singular, the embodiments disclosed herein could be modified to include a plurality of such elements/components. The subject matter described herein intends to cover and embrace all suitable changes in technology.
(145) Certain adaptations and modifications of the described embodiments can be made. Therefore, the above discussed embodiments are considered to be illustrative and not restrictive.

Claims

1. A digital signal processor (DSP) for a receiver, comprising: a processor configured to: receive a digital signal at a symbol rate in a frequency domain; and compensate an impairment of the digital signal in the frequency domain by determining, at a 2×2 multiple input multiple output (MIMO), a clock frequency offset estimation Δf.sub.clk-est and a carrier frequency offset estimation Δf.sub.est in the digital signal, and adjusting a sampling clock frequency of an analog to digital convertor (ADC) of the receiver by a −Δf.sub.clk-est.
2. The DSP of claim 1, further comprising: compensating, at an In-phase Quadrature Compensation (IQC), the digital signal in frequency domain by a −Δf.sub.est.
3. The DSP of claim 1, wherein the Δf.sub.clk-est and the Δf.sub.est are determined by correlating in frequency domain, at the 2×2 MIMO, digital signals x and y in time domain in X- and Y-polarizations with a MIMO taps: [$\begin{matrix} W_{\text{xx}} & W_{\text{xy}} \\ W_{\text{yx}} & W_{\text{yy}} \end{matrix}$]

$X=fft(\text{signalx})$
$Y=fft(\text{signaly})$
where:
W.sub.xx=*W*.sub.xy=conj(*fft*(TrainSeqx.Math.*e*.sup.jπΔft))
W.sub.yy=*W*.sub.yx=conj(*fft*(TrainSeqy.Math.*e*.sup.jπΔft)) and where TrainSeqx and TrainSeqy are training sequences or signals x and y in X- and Y-polarizations, respectively, wherein the Δf.sub.clk-est and the Δf.sub.est correspond to scan values at a maximum correlation peak value.
4. The DSP of claim 3, wherein compensating the impairment of the digital signal comprises: equalizing the digital signals in X- and Y-polarizations in frequency domain until a root mean square value of a time domain error signal of the digital signal X- and Y-polarizations is smaller than or equal to a predetermined threshold.
5. The DSP of claim 4, wherein equalizing the digital signals in X- and Y-polarizations in frequency domain comprises: correlating the digital signals in X- and Y-polarizations in frequency domain with the MIMO taps, at the MIMO, wherein values of the MIMO taps are: *W*.sub.xx=*W*.sub.yy=[1 1 1 . . . 1].Math.*H*.sub.comp*;* *W*.sub.xy=*W*.sub.yx=[0 0 0 . . . 0];and updating the digital signals in X- and Y-polarizations by *X=X.Math.W*.sub.xx+*Y.Math.W*.sub.yx, *Y=X.Math.W*.sub.xy+*Y.Math.W*.sub.yy where H.sub.comp is a compensation response to compensate non-time-varying fixed impairments.
6. The DSP of claim 5, further comprising: updating the MIMO taps by
W.sub.xx(*m*+1)=*W*.sub.xx(*m*)+2μ.Math.*G{E*.sub.x(*m*)*X**(*m*)}
W.sub.yx(*m*+1)=*W*.sub.yx(*m*)+2μ.Math.*G{E*.sub.x(*m*)*Y**(*m*)}
W.sub.xy(*m*+1)=*W*.sub.xy(*m*)+2μ.Math.*G{E*.sub.y(*m*)*X**(*m*)}

W.sub.yy(m+1)=W.sub.yy(m)+2μ.Math.G{E.sub.y(m)Y*(m)}. where X*(m) and Y*(m) are conjugate of the frequency domain digital signals containing X(m) and Y(m) in x and y polarization respectively, E.sub.x(m) and E.sub.y(m) are error signals associated with the frequency domain digital signals X(m) and Y(m) respectively, G{.Math.} is a gradient constraint, and μ is a step function.

7. The DSP of claim 4, wherein compensating impairment of the digital signal comprises: determining a timing error τ.sub.Baud of the digital signal; and tuning, by a loop filter, a voltage-controlled oscillator (VCO) until the timing error is smaller than a predetermined threshold.

8. The DSP of claim 7, the timing error τ.sub.Baud is determined based on

$$\tau_{Baud} = \frac{\mathrm{diff}(\bar{\varphi})\text{ .Math. } N}{2\pi}$$

$$\varphi = \mathrm{unwrap}(\mathrm{angle}(\mathrm{fftshift}(\mathrm{detW}))) = 2\pi f \tau = 2\pi \frac{(0{:}\ N\text{ - }1)}{N} \tau_{\mathrm{Baud}}$$

detW=W.sub.xx*W.sub.yy−W.sub.xy*W.sub.yx where W.sub.xx, W.sub.yy W.sub.xy, W.sub.yx are converged MIMO tap values, N is sample data point number, and f=k/Nf.sub.s is a frequency of the digital signals, K is an integer smaller than N, fs is a sampling rate equal to a baud rate.

9. The DSP of claim 8, wherein the loop filter tunes the VCO based on: loopFilt=sign(τ.sub.Baud(n)−τ.sub.Baud(n−1))*k.sub.p+sign(τ.sub.Baud(n))*k.sub.i where k.sub.p and k.sub.i are step sizes.

10. The DSP of claim 7, wherein the loop filter tunes the VCO based on: loopFilt=(τ.sub.Baud(n)−T.sub.Baud(n−1))*μ.sub.p+sign(τ.sub.Baud(n))*μ.sub.i Where μ.sub.p and μ.sub.i are step sizes.

11. The DSP of claim 7, further comprising: suspending MIMO and timing recovery updating; and determining position of training symbols in the digital signal.

12. The DSP of claim 11, wherein determining position of training symbols in the digital signal comprises: correlating timing error recovered digital signal in X- and Y-polarizations in frequency domain with the MIMO taps having values of:

W.sub.xx=fft(TrainSeqx).Math.H.sub.xx

W.sub.yy=fft(TrainSeqy).Math.H.sub.yy

W.sub.xy=fft(TrainSeqx).Math.H.sub.xy

W.sub.yx=fft(TrainSeqy).Math.H.sub.yx where TrainSeqx and TrainSeqy are formed by the training symbols in the X and Y-polarized signals in time domain, and H.sub.xx, H.sub.yy, H.sub.xy, H.sub.yx are converged MIMO taps after equalizing the digital signal in X- and Y-polarizations in frequency domain.

13. The DSP of claim 11, further comprising adjusting, by the 2×2 MIMIO, a framer index corresponding to a timing error shifting amount.

14. The DSP of claim 11, wherein compensating impairment of the digital signal further comprises: determining a time domain error of the digital signal X- and Y-polarizations in time domain by using training symbols; and updating MIMO taps until the time domain error of the digital signal X- and Y-polarizations is smaller than or equal to a second predetermined threshold.

15. The DSP of claim 14, wherein updating MIMO taps comprises updating the MIMO taps by:

W.sub.xx(m+1)=W.sub.xx(m)+2μ.Math.G{E.sub.x(m)X*(m)}

W.sub.yx(m+1)=W.sub.yx(m)+2μ.Math.G{E.sub.x(m)Y*(m)}

W.sub.xy(m+1)=W.sub.xy(m)+2μ.Math.G{E.sub.y(m)X*(m)}

W.sub.yy(m+1)=W.sub.yy(m)+2μ.Math.G{E.sub.y(m)Y*(m)}. where X*(m) and Y*(m) are conjugate of the frequency domain digital signals containing X(m) and Y(m) in x and y polarization respectively, E.sub.x(m) and E.sub.y(m) are error signals associated with the frequency domain digital signals X(m) and Y(m) respectively, G{.Math.} is a gradient constraint, and μ is a step function, wherein initial value of the MIMO taps are as follows:

W.sub.xx=H.sub.xx

W.sub.yy=H.sub.yy

W.sub.xy=H.sub.xy
W.sub.yx=H.sub.yx.
16. The DSP of claim 14, wherein the second predetermined threshold is smaller than the predetermined threshold.
17. The DSP of claim 14 further comprising compensating for frequency offset and phase shift of the digital signals using a carrier recovery.
18. A method for processing a digital signal at a digital signal processor (DSP) of a receiver, comprising: receiving the digital signal at a symbol rate in a frequency domain; and compensating an impairment of the digital signal in the frequency domain by: determining, at a 2×2 multiple input multiple output (MIMO), a clock frequency offset estimation Δf.sub.clk-est and a carrier frequency offset estimation Δf.sub.est in the digital signal, and adjusting a sampling clock frequency of an analog to digital convertor (ADC) of the receiver by a −Δf.sub.clk-est.
19. The method of claim 18, further comprising: compensating, at an In-phase Quadrature Compensation (IQC), the digital signal in frequency domain by a −Δf.sub.est.
20. The method of claim 18, wherein the Δf.sub.clk-est and the Δf.sub.est are determined by correlating in frequency domain, at the 2×2 MIMO, digital signals x and y in time domain in X- and Y-polarizations with a MIMO taps: $\left[\begin{matrix} W_{xx} & W_{xy} \\ W_{yx} & W_{yy} \end{matrix}\right]$

X=fft(signalx)
Y=fft(signaly)
where:
W.sub.xx=W.sub.xy=conj(fft(TrainSeqx.Math.e.sup.jπΔft))
W.sub.yy=W.sub.yx=conj(ft(TrainSeqy.Math.e.sup.jπΔft)) and where TrainSeqx and TrainSeqy are training sequences or signals x and y in X- and Y-polarizations, respectively, wherein the Δf.sub.clk-est and the Δf.sub.est correspond to scan values at a maximum correlation peak value.