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(54) **SEMICONDUCTOR MODULE AND VEHICLE**

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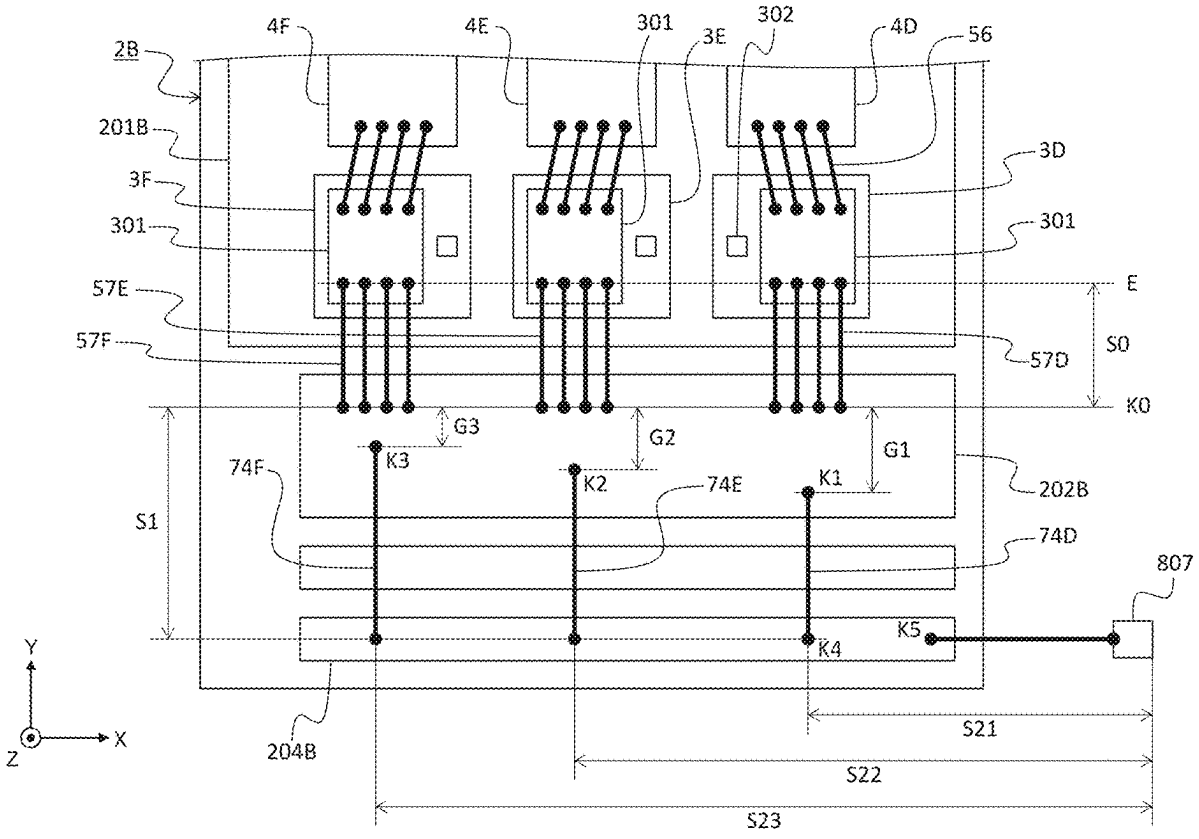
(57) **ABSTRACT**

A semiconductor module, including: a wiring board having first and second conductor patterns; a plurality of semiconductor elements disposed on the first conductor pattern; first and second bonding members connecting first and second main electrodes of the semiconductor elements to the first and second conductor patterns, respectively; first and second terminals connected to the first and second main electrodes of the semiconductor elements through the first and second conductor patterns, respectively; and a third terminal connected to the second conductor pattern through a plurality of third bonding members. A distance between a connection point of each of the third bonding members to the second conductor pattern and a connection point of the second bonding member to the second conductor pattern varies depending on a distance between a predetermined position and a connection point of the second bonding member to the second main electrode of each semiconductor element.



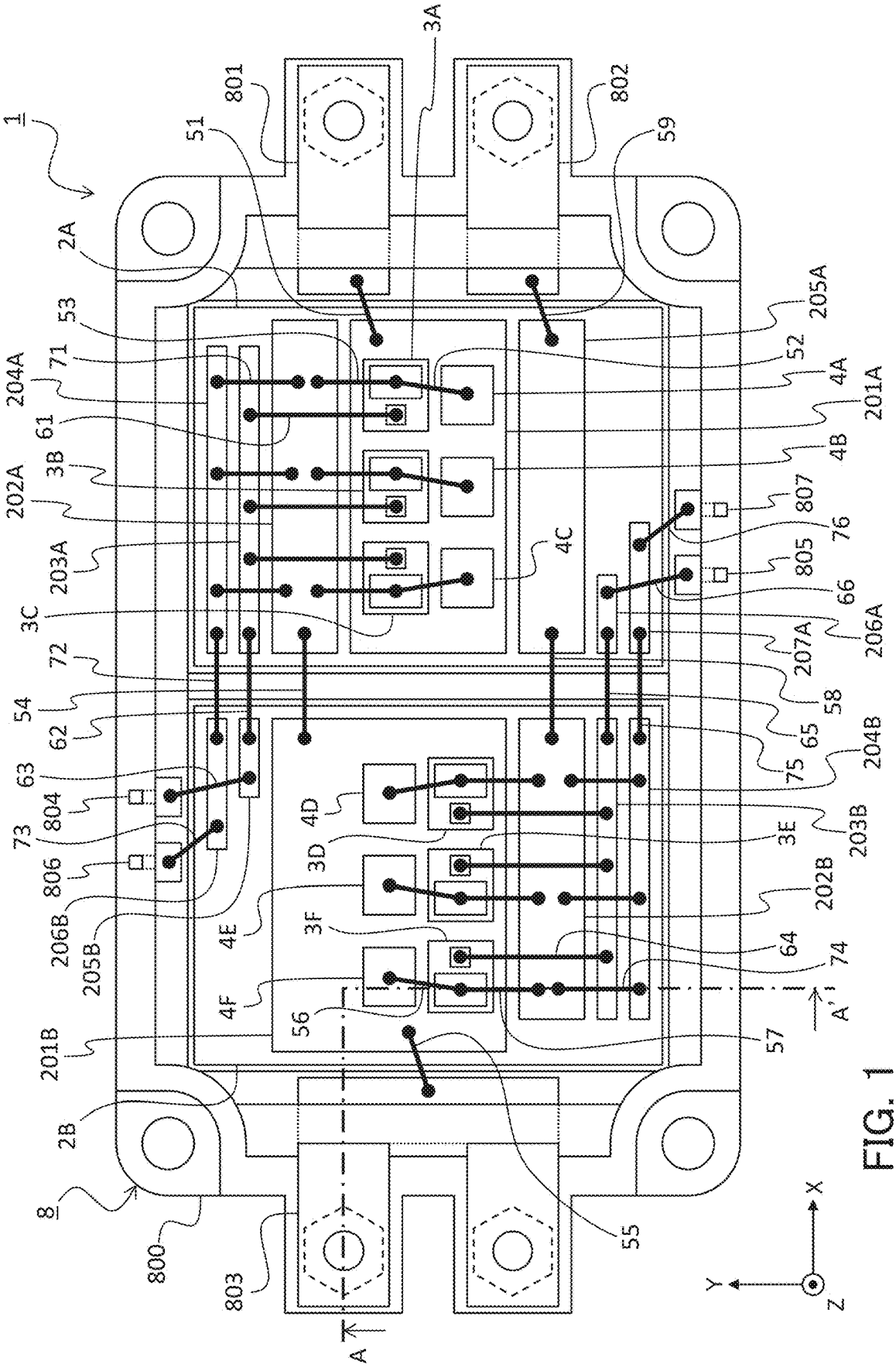

1
2A
2B
3A
3B
3C
3D
3E
3F
4A
4B
4C
4D
4E
4F
51
52
53
54
55
56
57
58
59
61
62
63
64
65
66
71
72
73
74
75
76
800
801
802
803
804
805
806
807
8
201A
201B
202A
202B
203A
203B
204A
204B
205A
205B
206A
206B
207A
A
A'
X
Y
Z

FIG. 1

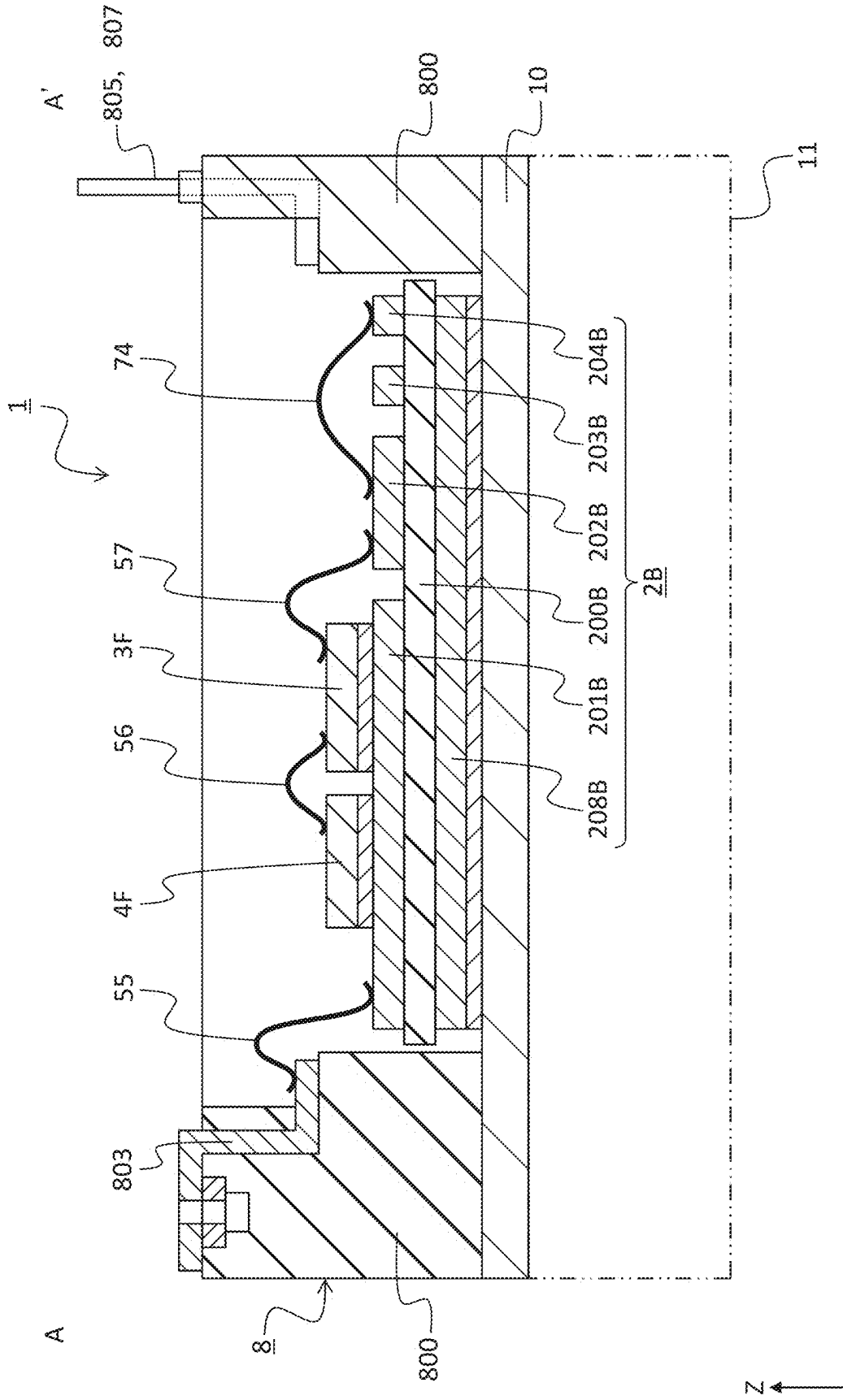

A'
805, 807
800
10
11
74
1
204B
203B
202B
200B
201B
208B
2B
57
3F
56
4F
55
803
A
8
800
X, Y
Z

FIG. 2

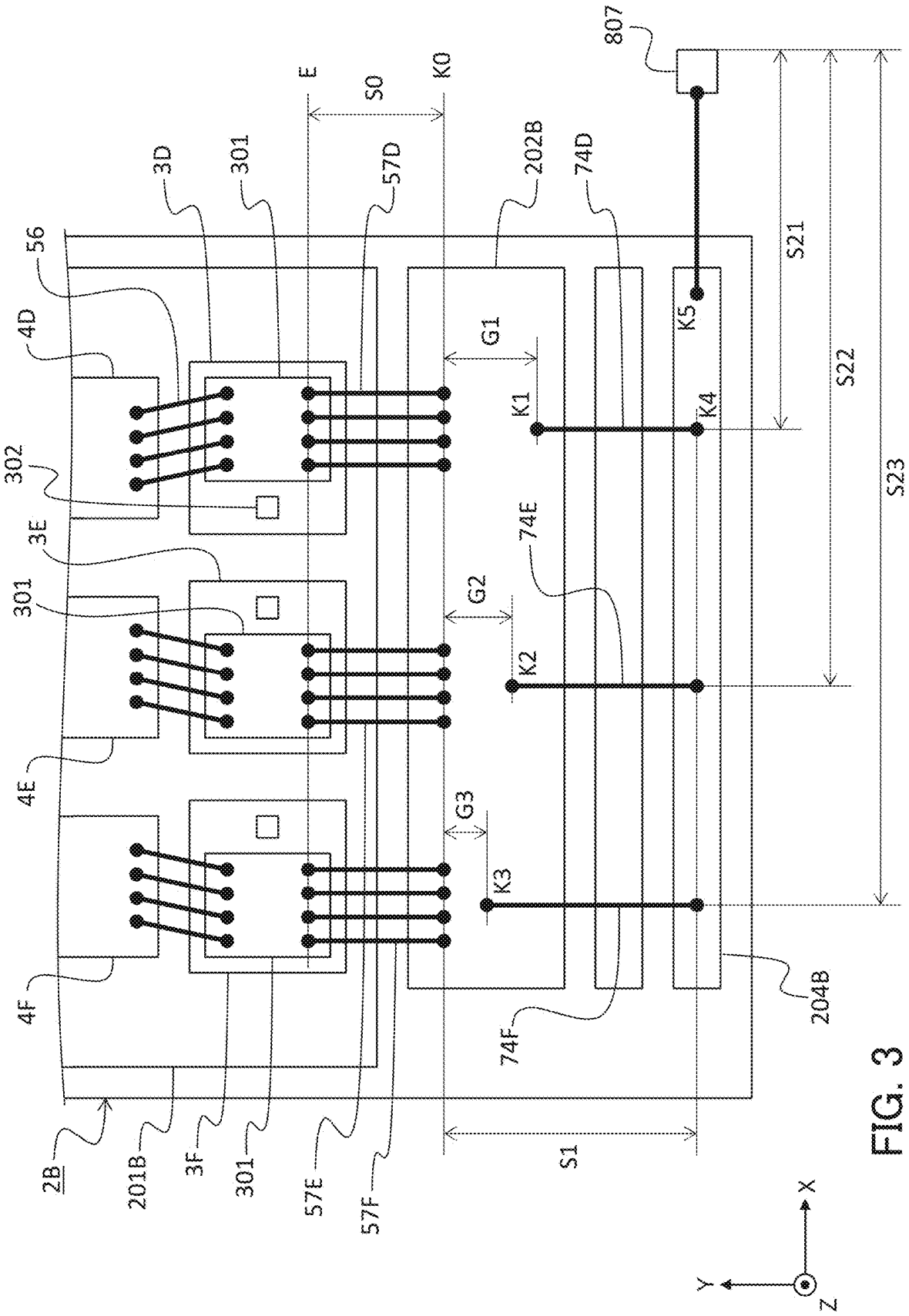

807
E
S0
K0
3D
301
57D
202B
74D
56
S21
4D
G1
K5
K1
K4
S22
302
3E
74E
301
G2
K2
S23
4E
G3
K3
4F
204B
74F
2B
201B
3F
301
57E
57F
S1
X
Y
Z

FIG. 3

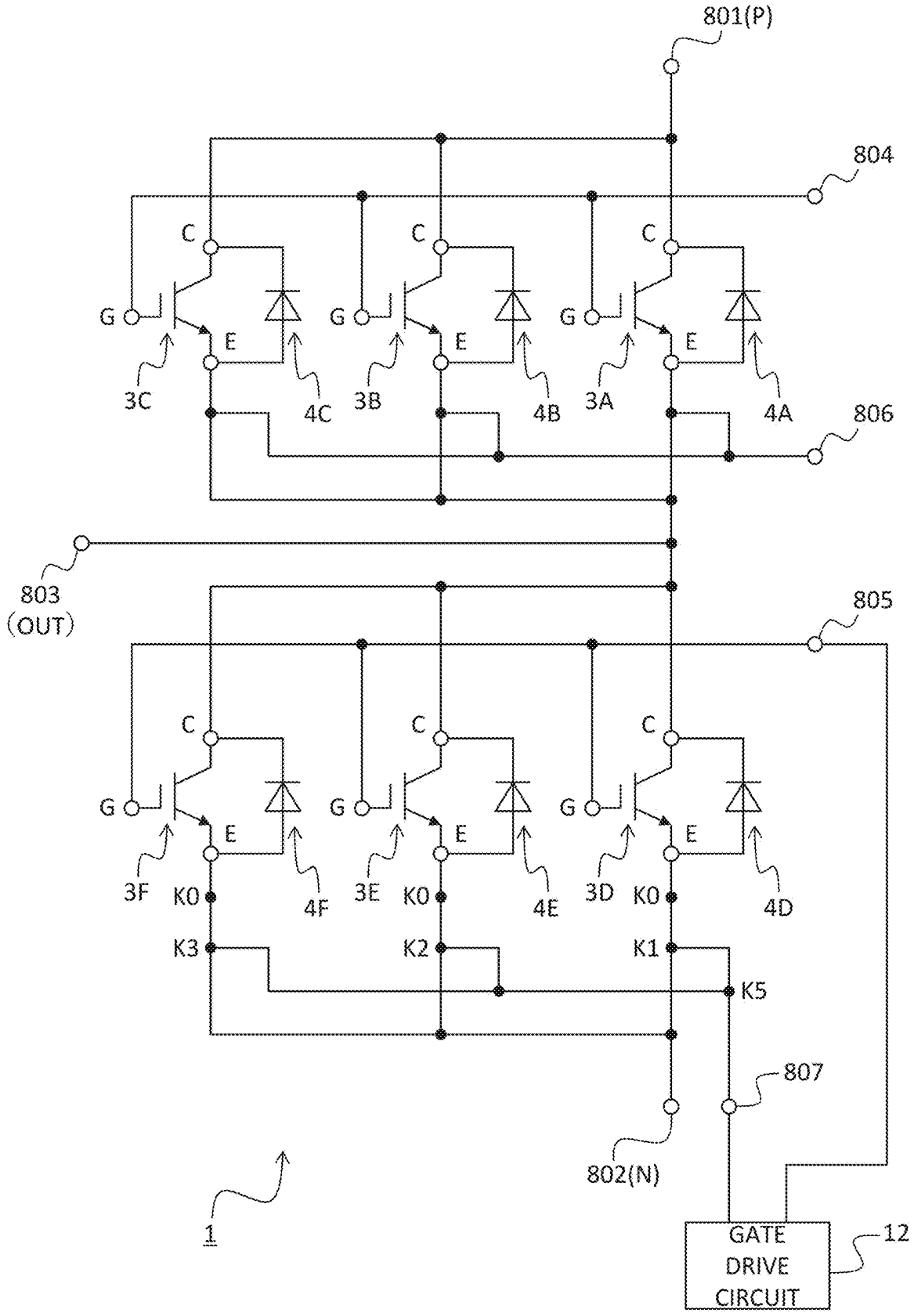

801(P)
804
C
G
E
3C
4C
3B
4B
3A
4A
806
803
(OUT)
805
3F
K0
4F
3E
4E
3D
4D
K3
K2
K1
K5
807
802(N)
1
GATE
DRIVE
CIRCUIT
12

FIG. 4

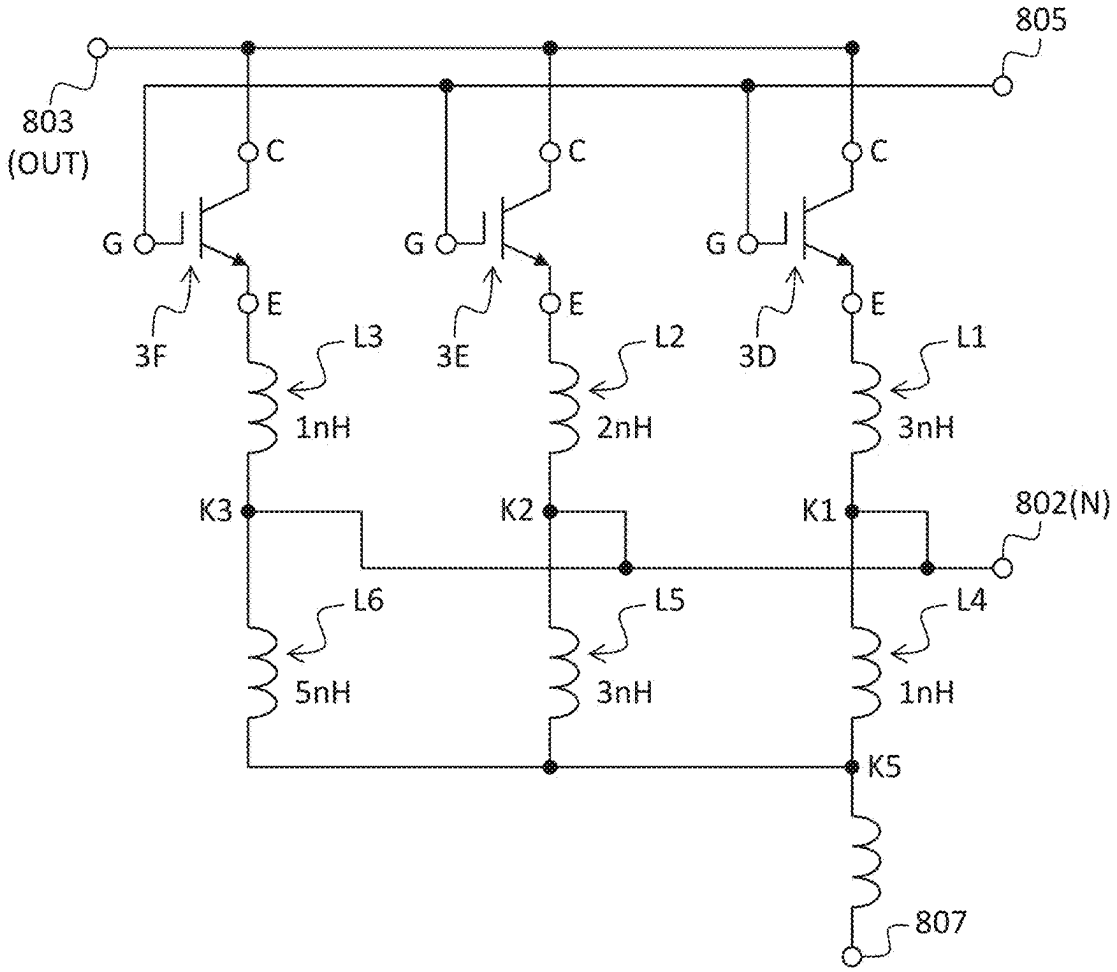

805
803
(OUT)
C
C
C
G
G
G
E
E
E
3F
3E
3D
L3
L2
L1
1nH
2nH
3nH
K3
K2
K1
802(N)
L6
L5
L4
5nH
3nH
1nH
K5
807

FIG. 5A

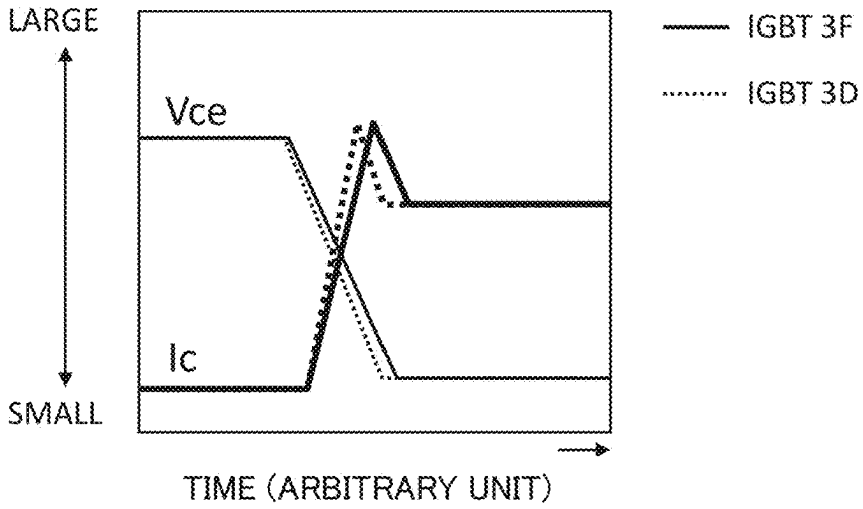

LARGE
SMALL
Vce
Ic
IGBT 3F
IGBT 3D
TIME (ARBITRARY UNIT)

FIG. 5B

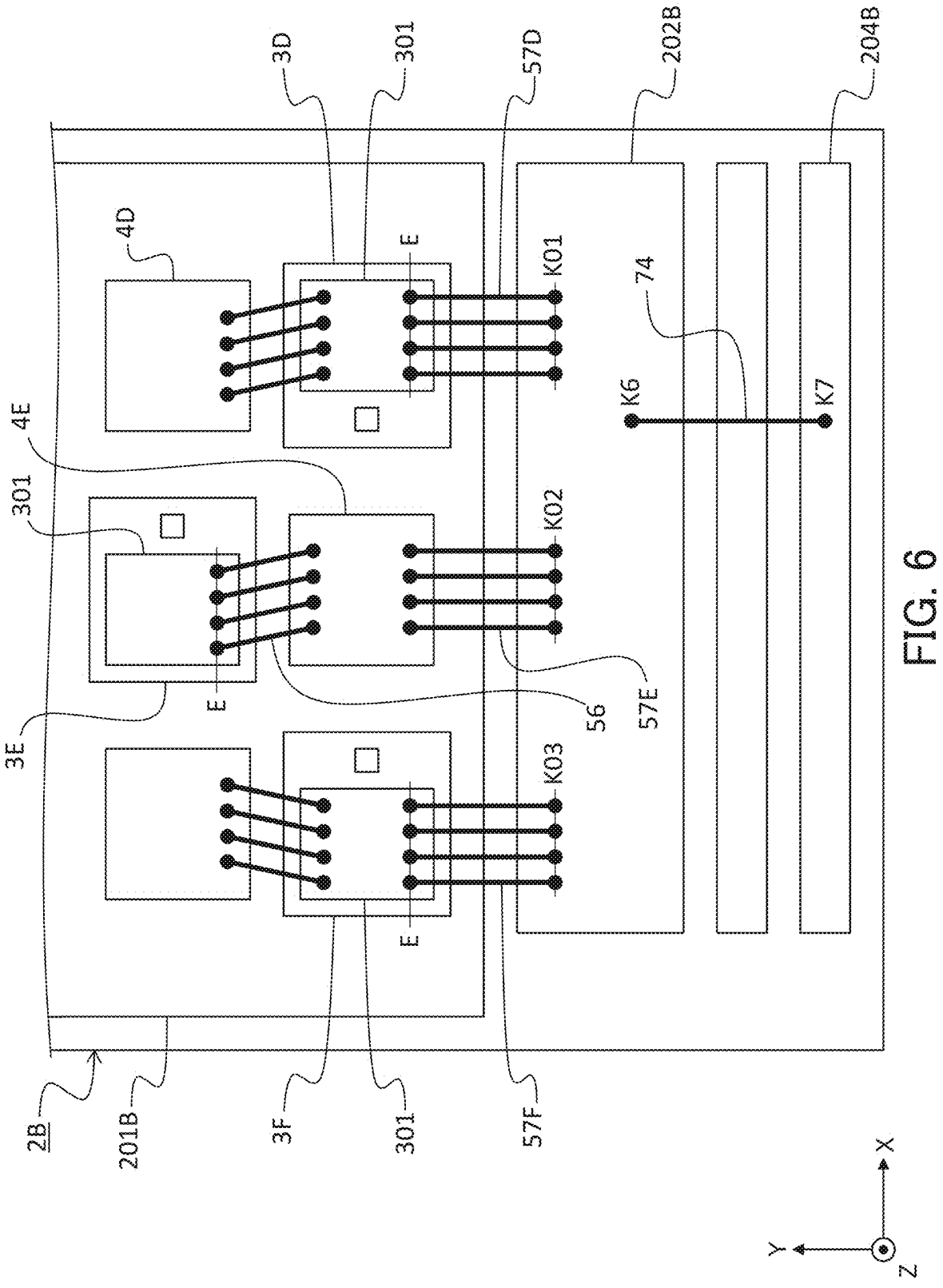

3D
301
57D
202B
204B
4D
E
K01
74
K6
K7
4E
301
K02
E
3E
56
57E
K03
E
2B
201B
3F
301
57F
X
Y
Z

FIG. 6

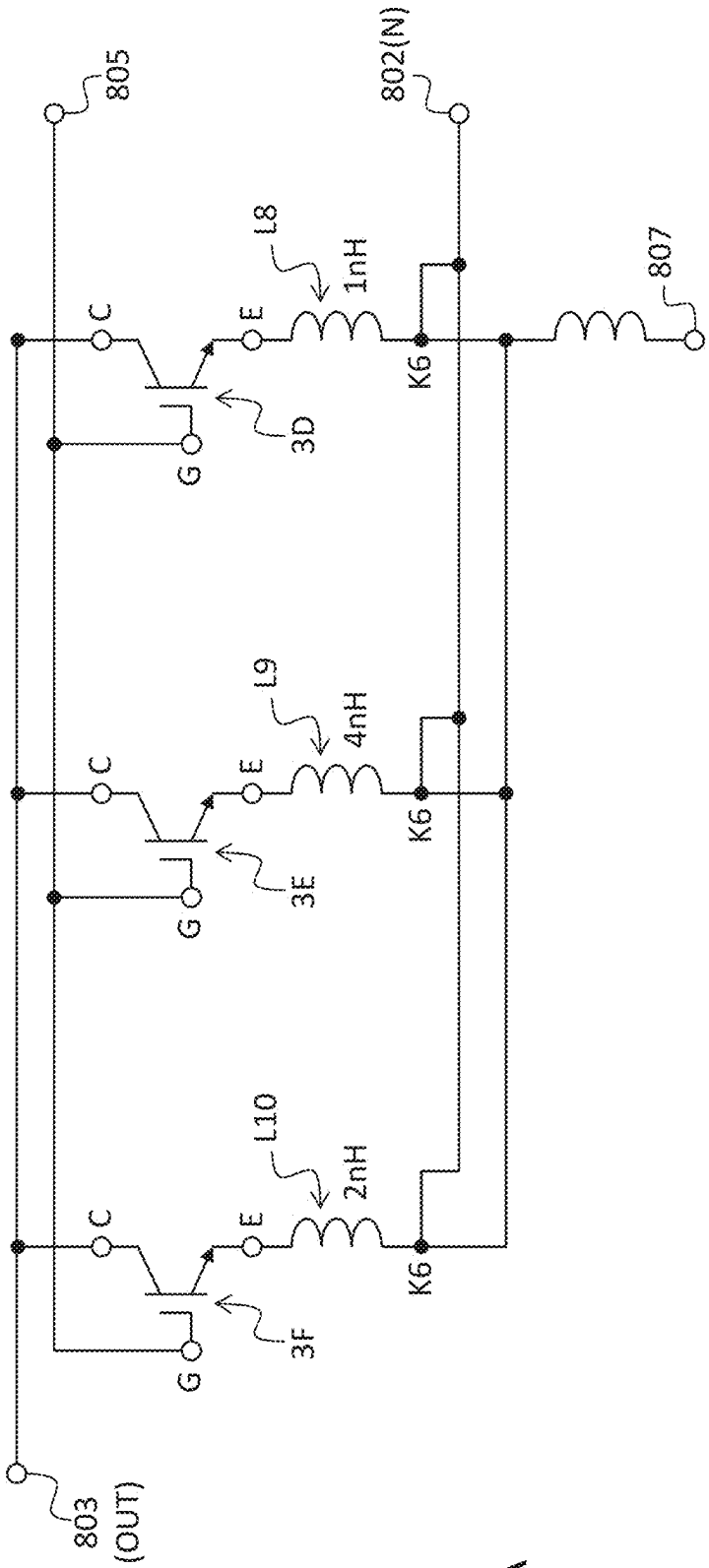

805
802(N)
807
L8
1nH
L9
4nH
L10
2nH
C
E
G
3D
3E
3F
K6
803
(OUT)

FIG. 7A

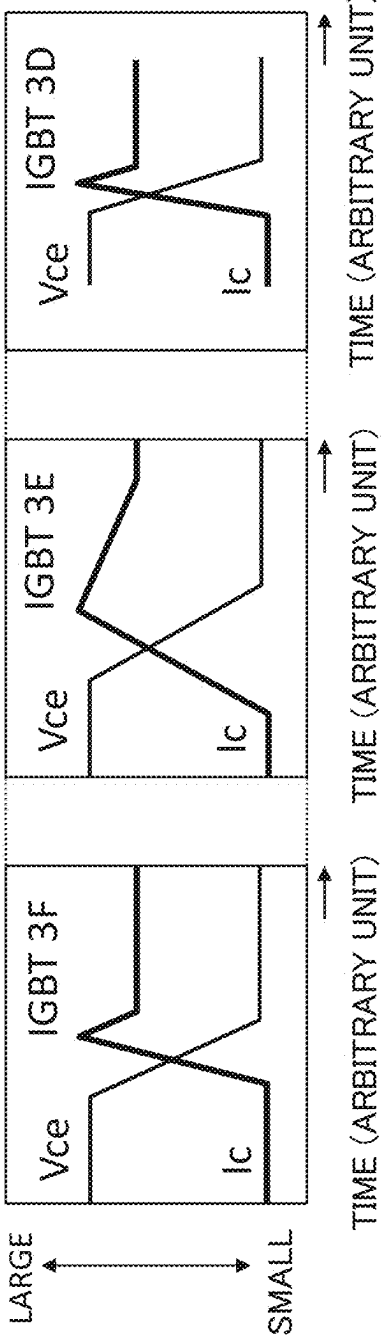

IGBT 3D
IGBT 3E
IGBT 3F
Vce
Ic
LARGE
SMALL
TIME (ARBITRARY UNIT)

FIG. 7B

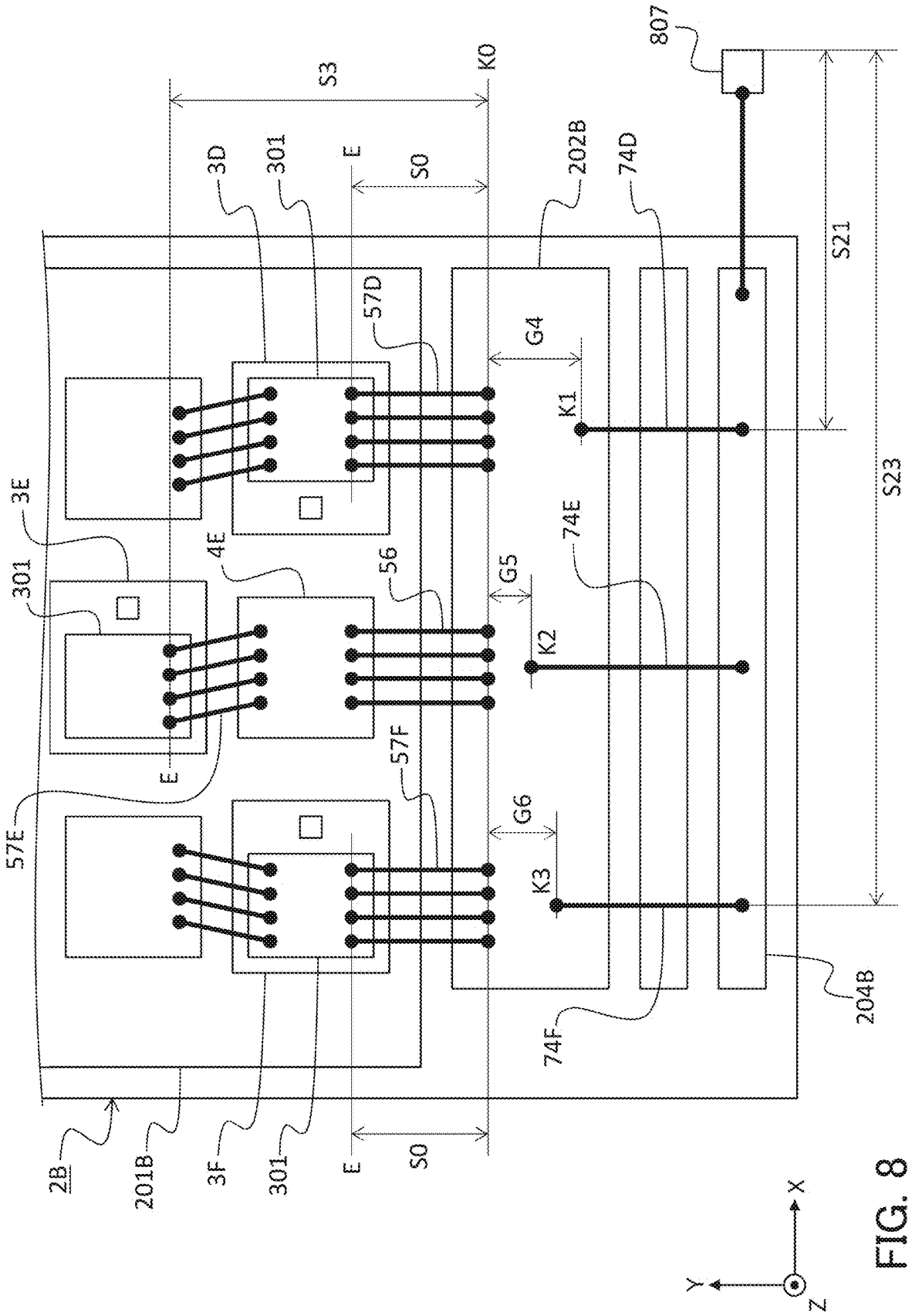

807
S3
K0
3D
301
E
S0
202B
74D
S21
57D
G4
K1
3E
301
4E
56
74E
S23
G5
K2
E
57F
57E
G6
K3
204B
74F
2B
201B
3F
301
E
S0
X
Y
Z

FIG. 8

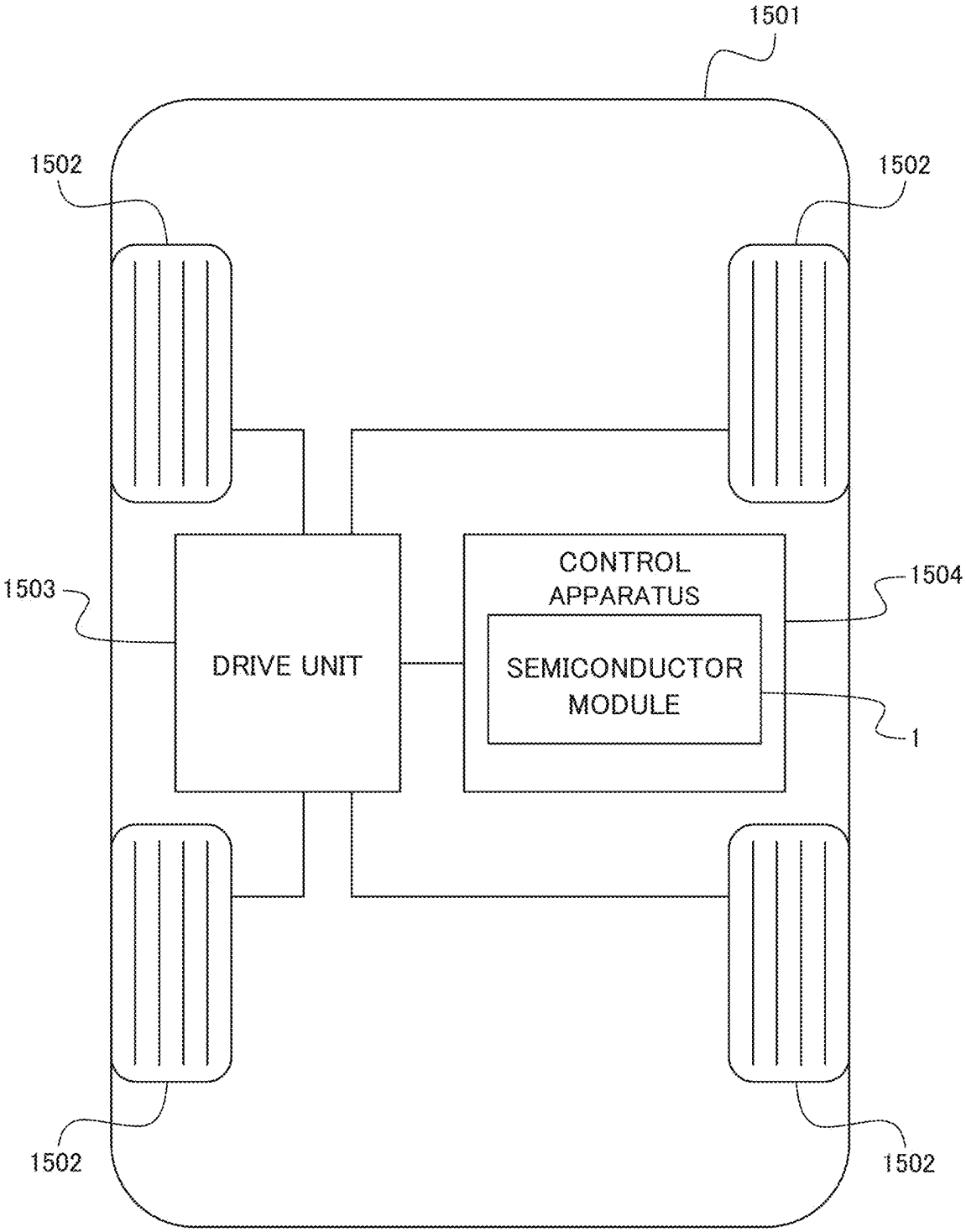

1501
1502
1502
1503
DRIVE UNIT
CONTROL APPARATUS
SEMICONDUCTOR MODULE
1504
1
1502
1502

FIG. 9

SEMICONDUCTOR MODULE AND VEHICLE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based upon and claims the benefit of priority to Japanese Patent Application No. 2024-018488, filed on Feb. 9, 2024, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Technical Field

[0002] The present invention relates to a semiconductor module and a vehicle.

2. Description of the Related Art

[0003] A semiconductor module used in a power conversion apparatus includes a plurality of insulated gate bipolar transistor (IGBT) elements connected in parallel. In this type of semiconductor module, there is provided a conductive member that is referred to as an auxiliary emitter for connecting an emitter of an IGBT element to a gate drive circuit connected to gates of a plurality of IGBT elements connected in parallel (for example, JP 2023-167403 A, WO 2020/054806 A, WO 2022/059251 A, and WO 2022/264851 A).

SUMMARY OF THE INVENTION

[0004] In the semiconductor module including the auxiliary emitter, the non-uniform switching operation in each of the plurality of IGBT elements connected in parallel causes variation in heat generation of each IGBT element, and the reliability of the semiconductor module may deteriorate.

[0005] An object of the present invention is to reduce variations in switching operation among a plurality of switching elements connected in parallel in a semiconductor module.

[0006] A semiconductor module according to one aspect includes: a wiring board having a first conductor pattern and a second conductor pattern disposed on one surface of an insulating substrate; a plurality of semiconductor elements disposed on the first conductor pattern of the wiring board; a first bonding member for connecting each of first main electrodes of the plurality of semiconductor elements to the first conductor pattern; a second bonding member for connecting each of second main electrodes of the plurality of semiconductor elements to the second conductor pattern; a first terminal connected to the first main electrodes of the plurality of semiconductor elements through the first conductor pattern, through which a main current flows; a second terminal connected to the second main electrodes of the plurality of semiconductor elements through the second conductor pattern, through which a main current flows; and a third terminal connected to the second conductor pattern through a third bonding member. Each of the plurality of semiconductor elements includes a switching element that controls a current flowing between the first main electrode and the second main electrode. The third bonding member includes a plurality of bonding members associated with each of the plurality of semiconductor elements. The distance from a connection point of the plurality of bonding members on the second conductor pattern to a connection point of the second bonding member varies depending on the distance from a predetermined position in the third terminal to a connection point with the second bonding member in the second main electrode of the plurality of semiconductor elements.

[0007] According to the above-described aspect, it is possible to reduce variations in switching operation among the plurality of switching elements connected in parallel in the semiconductor module.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. **1** is a plan view of a semiconductor module according to an embodiment;

[0009] FIG. **2** is a cross-sectional view for illustrating a configuration example in a case of the semiconductor module of FIG. **1**;

[0010] FIG. **3** is a partially enlarged cross-sectional view for illustrating a configuration example of an auxiliary emitter wiring in the semiconductor module of FIG. **1**;

[0011] FIG. **4** is an equivalent circuit diagram of an inverter circuit formed in the semiconductor module of FIG. **1**;

[0012] FIG. **5**A is an equivalent circuit diagram for illustrating an example of inductances of the auxiliary emitter wiring in the semiconductor module according to the embodiment, and FIG. **5**B is a graph illustrating an example of a switching operation in the semiconductor module according to the embodiment;

[0013] FIG. **6** is a partially enlarged plan view for illustrating a conventional example of the auxiliary emitter wiring in a semiconductor module in which a plurality of semiconductor elements is connected in parallel;

[0014] FIG. **7**A is an equivalent circuit diagram for illustrating an example of the inductance of the auxiliary emitter wiring in the semiconductor module of FIG. **6**, and FIG. **7**B is a graph illustrating an example of a switching operation in the semiconductor module of FIG. **6**;

[0015] FIG. **8** is a partially enlarged plan view for illustrating a modification of the semiconductor module according to the embodiment; and

[0016] FIG. **9** is a schematic plan view for illustrating an example of a vehicle to which the semiconductor module according to the present invention is applied.

DETAILED DESCRIPTION

[0017] Hereinafter, an embodiment of the present invention will be described in detail with reference to the drawings. A "semiconductor module" in the following description is obtained by sealing semiconductor elements, which are referred to as semiconductor chips, dies, or the like, with an insulating material. The semiconductor module may be referred to as a "semiconductor device" or the like.

[0018] An X axis, a Y axis, and a Z axis in each of the drawings to be referred to are illustrated for the purpose of defining a plane and a direction in the illustrated semiconductor module. The X axis, the Y axis, and the Z axis are perpendicular to each other and form a right-handed system. In the following description, a direction parallel to the X axis is referred to as an X direction, a direction parallel to the Y axis is referred to as a Y direction, and a direction parallel to the Z axis is referred to as a Z direction. Also, in a case where each of the X direction, the Y direction, and the Z direction is associated with a direction of an arrow (positive

or negative) of the X axis, the Y axis, and the Z axis illustrated, a "positive side" or a "negative side" is added.

[0019] In the present specification, the Z direction may be referred to as a vertical direction. In the present specification, "on" and "upper side" are intended to be on the positive side in the Z direction with respect to the reference surface, member, position, and the like, and "below" and "lower side" are intended to be on the negative side in the Z direction with respect to the reference surface, member, position, and the like. For example, when it is described that "the member B is disposed on the member A", the member B is disposed on the positive side in the Z direction as viewed from the member A. Also, when the term "upper surface of the member A" is described, the surface includes a surface that is positioned at the end of the member A on the positive side in the Z direction and faces the positive side in the Z direction. These directions and surfaces associated with the directions are words used for convenience of description, and a correspondence relationship with the directions of the X axis, the Y axis, and the Z axis may change depending on the mounting posture of the semiconductor module and the like. For example, in the present specification, a surface of a semiconductor element facing a wiring board is referred to as a lower surface, and a surface opposite to the lower surface is referred to as an upper surface, but the terms are not limited thereto, and the surface facing the wiring board may be referred to as the upper surface, and the surface opposite thereto may be referred to as the lower surface.

[0020] An aspect ratio and a magnitude relationship between respective members in each drawing are merely schematically represented, and do not necessarily coincide with a relationship in a semiconductor module actually manufactured. For convenience of description, it is also assumed that a magnitude relationship between respective members is exaggeratedly expressed, or an expression is different from an outer shape of a member used in an actual semiconductor module. Also, for convenience of description, some of the cross-sectional views illustrate a cross-sectional configuration of the semiconductor module cut along a virtual cutting line that is not able to be accurately illustrated in the plan view.

[0021] The descriptions of "not illustrated", "not shown" and the like in the present specification are intended not to clearly indicate, by use of a specific reference sign and a leader line, which portion of the drawing is a component to which the descriptions are given. For example, a "first main electrode not illustrated" is intended to mean both that a portion representing the first main electrode (for example, a shape, a line, or the like) is not illustrated in the drawing, and that there is neither a reference sign nor a leader line clearly indicating a portion corresponding to the first main electrode in the drawing. Also, the underlined reference sign in the drawing indicates a whole component that encompasses a plurality of portions distinguished by a plurality of reference signs.

[0022] A semiconductor module to be illustrated in the following description may be applied to, for example, a power conversion apparatus such as an inverter apparatus of industrial or electrical equipment (for example, an in-vehicle motor). Thus, in the following description, a detailed description of the same or similar configuration, function, operation, manufacturing method, and the like as or to those of a known semiconductor module will be skipped.

[0023] FIG. **1** is a plan view of a semiconductor module according to an embodiment. FIG. **2** is a cross-sectional view for illustrating a configuration example in a case of the semiconductor module of FIG. **1**. FIG. **3** is a partially enlarged cross-sectional view for illustrating a configuration example of the auxiliary emitter wiring in the semiconductor module of FIG. **1**. FIG. **4** is an equivalent circuit diagram of an inverter circuit formed in the semiconductor module of FIG. **1**. The cross-sectional view of FIG. **2** may be an example of a cross-sectional configuration of the semiconductor module I cut along an alternate long and short dash line A-A' in a semiconductor module **1** of FIG. **1**.

[0024] The semiconductor module **1** according to the present embodiment includes wiring boards **2**A and **2**B, semiconductor elements **3**A to **3**F, and **4**A to **4**F, bonding members **51** to **59**, **61** to **66**, and **71** to **76**, a case **8**, a scaling material (not shown), and heat sink **10**. In the present specification, in a case where a plurality of identical components is distinguished, a reference sign represented by combination of a number and an alphabet following the number is described, and in a case where a plurality of identical components is not distinguished, a reference sign represented by only the number is described. For example, when a specific semiconductor element among the plurality of semiconductor elements **3**A to **3**F is designated, the reference sign (any one of **3**A to **3**F) assigned to the specific semiconductor element is described in FIG. **1**, and in other cases, the semiconductor element is simply described as "semiconductor element **3**".

[0025] The wiring board **2** is an element-mounted component on which the semiconductor elements **3** and **4**, which are sometimes referred to as semiconductor chips, dies, or the like, arc mounted. The semiconductor element **3** is a switching element such as an insulated gate bipolar transistor (IGBT) element, and the semiconductor element **4** is a diode such as a free wheeling diode (FWD) element. The wiring board **2**, the semiconductor element **3**, and the semiconductor element **4** are circuit components for forming a half-bridge inverter circuit illustrated in FIG. **4**.

[0026] The wiring board **2**A includes an insulating substrate **200**A, conductor patterns **201**A to **207**A disposed on the upper surface of the insulating substrate **200**A, and a heat dissipation pattern **208**A disposed on the lower surface of insulating substrate **200**A. The wiring board **2**B includes an insulating substrate **200**B, conductor patterns **201**B to **206**B disposed on the upper surface of insulating substrate **200**B, and a heat dissipation pattern **208**B disposed on the lower surface of insulating substrate **200**B. The wiring board **2** may be a direct copper bonding (DCB) substrate or an active metal brazing (AMB) substrate, but is not limited thereto.

[0027] The insulating substrate **200** may be, for example, a ceramic substrate made of a ceramic material such as aluminum oxide (Al_2O_3), aluminum nitride (AlN), silicon nitride (Si_3N_4), or a composite material of aluminum oxide (Al_2O_3) and zirconium oxide (ZrO_2). The insulating substrate **200** may be a substrate obtained by molding an insulating resin such as epoxy resin into a sheet shape, a substrate obtained by impregnating a base material such as a glass fiber with an insulating resin, a substrate obtained by coating a surface of a flat plate-shaped metal core with an insulating resin, or the like.

[0028] These conductor patterns **201** to **207** disposed on the upper surface of the insulating substrate **200** are used as wiring in an electronic circuit such as an inverter circuit

formed in the semiconductor module **1**. The heat dissipation pattern **208** disposed on the lower surface of insulating substrate **200** is used as a thermally conductive material that conducts heat generated by the semiconductor element **3** during operation of semiconductor module **1** to heat sink **10**. These conductor patterns **201** to **207** and the heat dissipation pattern **208** are formed of, for example, metal plates, metal foils, or the like such as copper or aluminum.

[0029] The wiring board **2** is disposed on the upper surface of the heat sink **10** together with case **8**. The case **8** includes a frame-shaped insulating member **800** having open ends on the upper surface and the lower surface thereof, and a plurality of terminals **801** to **807** integrated with the insulating member **800**. When being disposed on the upper surface of the heat sink **10**, the insulating member **800** of the case **8** may have a shape in which a space is defined that houses the wiring board **2**, the semiconductor element **3**, the semiconductor element **4**, the bonding members **5**, **6**, **7**, and the like, and that may be filled with a scaling material for scaling them. The wiring board **2**A and the wiring board **2**B may be integrated. The heat dissipation pattern **208** of the wiring board **2** is connected to be in close contact with the upper surface of the heat sink **10** by a bonding material such as solder (not illustrated) or a thermally conductive material such as thermal grease or thermal compound. The heat sink **10** may be, for example, a metal plate such as copper or aluminum. A plurality of fins may be provided on the lower surface of the heat sink **10**. The heat sink **10** may be a portion of a cooler **11** or a component connected to the cooler **11**. That is, the cooler **11** is any component in the semiconductor module **1** of the present embodiment.

[0030] The terminals **801** to **807** of the case **8** are roughly divided into main terminals **801** to **803** and control terminals **804** to **807**. The main terminals **801** to **803** are connected to an electrode through which a main current flows in a switching element such as an IGBT element. In the case of the semiconductor module **1** in which the inverter circuit illustrated in FIG. **4** is formed, a first main terminal **801** is a P-IN terminal connected to the positive electrode of a DC power supply, and is connected to the collector electrode of the semiconductor element (IGBT element) **3** disposed on the upper surface of the wiring board **2**A. A second main terminal **802** is an N-IN terminal connected to the negative electrode of the DC power supply, and is connected to the emitter electrode of the semiconductor element (IGBT chip) **3** disposed on the upper surface of the wiring board **2**B. A third main terminal **803** is an OUT terminal connected to a load consuming alternating current converted from direct current by the semiconductor module **1**, and is connected to the emitter electrode of the semiconductor element **3** disposed on the upper surface of the wiring board **2**A and the collector electrode of the semiconductor element **3** disposed on the upper surface of the wiring board **2**B. A control terminal **804** is connected to a gate electrode of the semiconductor element **3** disposed on the upper surface of the wiring board **2**A, and a control terminal **805** is connected to a gate electrode of the semiconductor element **3** disposed on the upper surface of the wiring board **2**B. A control terminal **806** is connected to the emitter electrode of the semiconductor element **3** disposed on the upper surface of the wiring board **2**A, and a control terminal **807** is connected to the emitter electrode of the semiconductor element **3** disposed on the upper surface of the wiring board **2**B. The control terminals **806** and **807** are terminals for connecting the emitter electrode of the semiconductor element **3** to a gate drive circuit **12** (see FIG. **4**) connected to the gate electrode of the semiconductor element **3**, and are referred to as an auxiliary emitter terminal, a sense emitter terminal, an emitter sense terminal, or the like. The gate drive circuit **12** is a circuit that generates a control signal for controlling on/off of the switching element of the semiconductor element **3** using the emitter potential input through the control terminals **806** and **807** as a ground, and applies the control signal to the gate electrode of the semiconductor element **3**. Control signals for the semiconductor elements **3**A to **3**C disposed on the upper surface of the wiring board **2**A are generated based on the potential of the control terminal **806**, and control signals for the semiconductor elements **3**D to **3**F disposed on the upper surface of the wiring board **2**B are generated based on the potential of the control terminal **807**. The gate drive circuit connected to the gate electrodes of the semiconductor elements **3**A to **3**C, and the gate drive circuit connected to the gate electrodes of the semiconductor elements **3**D to **3**E may be formed in separate elements or may be formed in a single element. These terminals **801** to **807** are integrally formed with the insulating member **800**, and have an outer terminal portion extending to the outside of the semiconductor module **1** and an inner terminal portion exposed to a space in which the wiring board **2** and the like are disposed.

[0031] On the upper surface of the wiring board **2**A, there are disposed semiconductor elements **3**A to **3**C, which are switching elements, and semiconductor elements **4**A to **4**C, which are diodes. As illustrated in FIG. **4**, the semiconductor elements **3**A to **3**C are connected in parallel between the first main terminal **801** and the third main terminal **803** of the case **8**, and the semiconductor elements **4**A to **4**C are connected in anti-parallel to the semiconductor elements **3**A to **3**C.

[0032] The semiconductor elements **3**A to **3**C are disposed on the conductor pattern **201**A of the wiring board **2**A in a direction in which a surface provided with the collector electrode is the lower surface and another surface provided with the emitter electrode and the gate electrode is the upper surface, and the collector electrode and the conductor pattern **201**A are bonded by a bonding material (not shown) such as solder. In this case, the semiconductor elements **4**A to **4**C arc disposed on the conductor pattern **201**A in a direction in which a surface provided with a cathode electrode is the lower surface and another surface provided with an anode electrode is the upper surface, and the cathode electrode and the conductor pattern **201**A are bonded by a bonding material (not shown) such as solder. The bonding material for bonding the collector electrode of the semiconductor element **3** and the conductor pattern **201** is an example of a first bonding member for connecting the first main electrode of the semiconductor element **3** and a first conductor pattern of the wiring board **2**.

[0033] The conductor pattern **201**A of the wiring board **2**A is connected to the first main terminal **801** by a bonding member **51**. Emitter electrodes of the semiconductor elements **3**A to **3**C are respectively connected to anode electrodes of the semiconductor elements **4**A to **4**C by a bonding member **52**, and connected to a conductor pattern **202**A of the wiring board **2**A by a bonding member **53**. The conductor pattern **202**A is connected to the third main terminal **803** through a bonding member **54**, the conductor pattern **201**B of the wiring board **2**B, and a bonding member **55**. The gate

electrodes of the semiconductor elements **3**A to **3**C are connected to the conductor pattern **203**A of the wiring board **2**A by a bonding member **61**. The conductor pattern **203**A is connected to the control terminal **804** through a bonding member **62**, the conductor pattern **205**B of the wiring board **2**B, and a bonding member **63**. Also, the conductor pattern **202**A of the wiring board **2**A is connected to the conductor pattern **204**A of the wiring board **2**A by a bonding member **71**. The conductor pattern **204**A is connected to the control terminal (auxiliary emitter terminal) **806** through a bonding member **72**, the conductor pattern **206**B of the wiring board **2**B, and a bonding member **73**. The bonding member **53** for connecting the emitter electrode of the semiconductor element **3** and the conductor pattern **202** is an example of a second bonding member for connecting the second main electrode of the semiconductor element **3** and the second conductor pattern of the wiring board **2**. The bonding member **71** for connecting the conductor pattern **202** and the conductor pattern **204** of the wiring board **2** is an example of a third bonding member for connecting the second conductor pattern of the wiring board **2** to a third terminal.

[0034] On the upper surface of the wiring board **2**B, there are disposed semiconductor elements **3**D to **3**F, which are switching elements, and semiconductor elements **4**D to **4**F, which are diodes. As illustrated in FIG. **4**, the semiconductor elements **3**D to **3**F are connected in parallel between the third main terminal **803** and the second main terminal **802** of the case **8**, and the semiconductor elements **4**D to **4**F are connected in anti-parallel to the semiconductor elements **3**D to **3**F.

[0035] The semiconductor elements **3**D to **3**F are disposed on the conductor pattern **201**B of the wiring board **2**B in a direction in which a surface provided with the collector electrode is the lower surface and another surface provided with an emitter electrode **301** and a gate electrode **302** is the upper surface (see FIG. **3**), and the collector electrode and the conductor pattern **201**B are bonded by a bonding material (not shown) such as solder. In this case, the semiconductor elements **4**D to **4**F are disposed on the conductor pattern **201**B in a direction in which a surface provided with a cathode electrode is the lower surface and another surface provided with an anode electrode is the upper surface, and the cathode electrode and the conductor pattern **201**B are bonded by a bonding material (not shown) such as solder.

[0036] The conductor pattern **201**B of the wiring board **2**B is connected to the third main terminal **803** by the bonding member **55**. The emitter electrode **301** of each of the semiconductor elements **3**D to **3**F is connected to the anode electrode of each of the semiconductor elements **4**A to **4**C by a bonding member **56**, and is connected to the conductor pattern **202**B of the wiring board **2**B by a bonding member **57**. The conductor pattern **202**B is connected to the second main terminal **802** through a bonding member **58**, the conductor pattern **205**A of the wiring board **2**A, and a bonding member **59**. Each of the gate electrodes **302** of semiconductor elements **3**D to **3**F is connected to the conductor pattern **203**B of the wiring board **2**B by a bonding member **64**. The conductor pattern **203**B is connected to the control terminal **805** through a bonding member **65**, the conductor pattern **206**A of the wiring board **2**A, and a bonding member **66**. Also, the conductor pattern **202**B of the wiring board **2**B is connected to the conductor pattern **204**B of the wiring board **2**B by a bonding member **74**. The conductor pattern **204**B is connected to the control terminal (auxiliary emitter terminal) **807** through a bonding member **75**, the conductor pattern **207**A of the wiring board **2**A, and a bonding member **76**.

[0037] The bonding members **51** to **59**, the bonding members **61** to **66**, and the bonding members **71** to **76** of the semiconductor module **1** may be bonding wires (metal thin wires). In the following description, the bonding members **51** to **59**, the bonding members **61** to **66**, and the bonding members **71** to **76** are also referred to as bonding wires **51** to **59**, bonding wires **61** to **66**, and bonding wires **71** to **76**. For example, in the semiconductor module **1**, as illustrated in FIG. **3**, the emitter electrode **301** of each semiconductor element **3** is connected to the anode electrode of the semiconductor element **4** by four bonding wires **56**, and is connected to the conductor pattern **202**B of the wiring board **2**B by four bonding wires **57**. Also, in the semiconductor module **1** of the present embodiment, the conductor pattern **202**B and the conductor pattern **204**B connected to the control terminal (auxiliary emitter terminal) **807** are connected by separate bonding wires **74**D to **74**F for each emitter electrode **301** of semiconductor elements **3**D to **3**F connected in parallel. Furthermore, in the semiconductor module **1** of the present embodiment, the length of a wiring section common to the path of the main current in the auxiliary emitter wiring is changed depending on the length of the auxiliary emitter wiring from different emitter electrode **301** in each of the semiconductor elements **3**D to **3**F to the control terminal (auxiliary emitter terminal) **807**. Specifically, as illustrated in FIG. **3**, the longer the auxiliary emitter wiring is, the shorter the wiring section common to the path of the main current is. Note that FIG. **3** illustrates only the auxiliary emitter wiring for the semiconductor elements **3**D to **3**F connected in parallel between the third main terminal **803** and the second main terminal **802**. The auxiliary emitter wiring for the semiconductor elements **3**A to **3**C connected in parallel between the first main terminal **801** and the third main terminal **803** may have the same configuration as the auxiliary emitter wiring for the semiconductor elements **3**D to **3**F.

[0038] The length of the auxiliary emitter wiring is represented by the sum of the length of the bonding wire **57** for connecting the emitter electrode **301** of the semiconductor element **3** and the conductor pattern **202**B of the wiring board **2**B, the length of the bonding wire **74** for connecting the conductor pattern **202**B and the conductor pattern **204**B, the distance from the connection point of the bonding wire **57** on the conductor pattern **202**B to the connection point of the bonding wire **74**, and the distance from the connection point of the bonding wire **57** on the conductor pattern **204**B to the control terminal **807**.

[0039] In the example of FIG. **3**, lengths S**0** of the bonding wires **57**D to **57**F connected to each emitter electrode **301** of the semiconductor elements **3**D to **3**E are substantially the same, and distances S**1** from the connection point K**0** of the bonding wires **57**D to **57**F on the conductor pattern **202**B side to the connection point K**4** of the bonding wires **74**D to **74**F on the conductor pattern **204**B side in the plan view are substantially the same. The "connection point" in the present specification is intended to be a representative point in a region where the conductor pattern of the wiring board **2** and the third bonding member are connected. Also, in the example of FIG. **3**, a magnitude relationship among a distance S**21** from the connection point K**4** of the bonding wire **74**D on the side of the conductor pattern **204**B to the

control terminal **807**, a distance S**22** from the connection point K**4** of the bonding wire **74**E on the side of the conductor pattern **204**B to the control terminal **807**, and a distance S**23** from the connection point K**4** of the bonding wire **74**F on the side of the conductor pattern **204**B to the control terminal **807** is a relationship of S**23**>S**22**>S**21**. In such a case, as illustrated in FIG. **3**, a magnitude relationship among a distance G**1** from the connection point K**0** of the bonding wire **57**D to the connection point K**1** of the bonding wire **74**D on the conductor pattern **202**B, a distance G**2** from the connection point K**0** of the bonding wire **57**E to the connection point K**2** of the bonding wire **74**E, and a distance G**3** from the connection point K**0** of the bonding wire **57**F to the connection point K**3** of the bonding wire **74**F should be a relationship of G**3**<G**2**<G**1**. In this way, for example, in the auxiliary emitter wiring of the semiconductor elements **3**D to **3**F connected in parallel, voltage drops in sections from the connection point K**5** of the bonding wire **75** in the conductor pattern **204**B of the wiring board **2**B to the emitter electrode **301** may be easily made uniform.

[0040] FIG. **5**A is an equivalent circuit diagram for illustrating an example of the inductances of the auxiliary emitter wiring in the semiconductor module according to the embodiment, and FIG. **5**B is a graph illustrating an example of a switching operation in the semiconductor module according to the embodiment.

[0041] When focusing on inductances, the auxiliary emitter wiring for the switching elements (semiconductor elements) **3**D to **3**F in the semiconductor module **1** described above with reference to FIGS. **1** to **4** may be represented as the equivalent circuit diagram of FIG. **5**A. In FIG. **5**A, a white circle (○) with "E" corresponds to the connection point E between the emitter electrode **301** of the semiconductor elements **3**D to **3**F and each of the bonding wires **57**D to **57**F as illustrated in FIG. **3**. Also, the connection points K**1** to K**3** and the connection point K**5** in FIG. **5**A correspond to the connection points K**1** to K**3** and the connection point K**5** in FIG. **3**.

[0042] In the circuit diagram of FIG. **5**A, the magnitude relationship among an inductance L**1** in the section from the connection point E of the switching element **3**D to the connection point K**1**, an inductance L**2** in the section from the connection point E of the switching element **3**E to the connection point K**2**, and an inductance L**3** in the section from the connection point E of the switching element **3**F to the connection point K**3** coincides with the magnitude relationship of the lengths of each section in the auxiliary emitter wiring, and is the relationship of L**3**<L**2**<L**1**. Similarly, the magnitude relationship of inductances L**4** to L**6** in sections from the connection points K**1** to K**3** to the connection point K**5** coincides with the magnitude relationship of the lengths of each section in the auxiliary emitter wiring, and is the relationship of L**6**>L**5**>L**4**. On the other hand, the magnitude relationship of the inductances of the entire auxiliary emitter wiring is (L**3**+L**6**)>(L**2**+L**5**)>(L**1**+L**4**), but the main current and the temporal change of the main current are larger than a current flowing through a single section (section where no main current flows) in the auxiliary emitter wiring so that the influences of the inductances L**1**, L**2**, and L**3** are larger than those of the inductances L**4**, L**5**, and L**6** when viewed in terms of the voltage drop. Therefore, by adjusting the position of the connection point of the bonding wires **74**D to **74**F with the conductor pattern **202**B of the wiring board **2**B and the position of the connection point of the bonding wires **74**D to **74**F with the conductor pattern **204**B, voltage drops of the auxiliary emitter wiring with respect to each of the switching elements **3**D to **3**F may be easily made uniform.

[0043] Also, voltage drops across the auxiliary emitter wiring for each of the switching elements **3**D to **3**F are made uniform, thereby reducing variations in the switching speed, the switching loss, and the like among the switching elements **3**D to **3**F connected in parallel. For example, FIG. **5**B schematically illustrates waveforms of the collector current Ic and the collector-emitter voltage Vce during the turn-on of the semiconductor elements **3**D and **3**F, which are associated with the switching speed and the switching loss in the conventional configuration. In the semiconductor module **1** of the present embodiment, a difference between the waveform of the collector current Ic of the semiconductor element **3**D and the waveform of the collector current Ic of the semiconductor element **3**F, and a difference between the waveform of the collector-emitter voltage Vce of the semiconductor element **3**D and the waveform of the collector-emitter voltage Vce of the semiconductor element **3**F are smaller than differences as illustrated in FIG. **5**B. Also, the waveform of the collector current Ic and the waveform of the collector-emitter voltage Vce of the semiconductor element **3**E have smaller differences from the waveform of the collector current Ic and the waveform of the collector-emitter voltage Vce of the semiconductor elements **3**D and **3**F. That is, in the semiconductor module **1** of the present embodiment, variations in heat generation among the switching elements (semiconductor elements) **3**D to **3**F may be suppressed, and the reliability of the semiconductor module **1** may be improved.

[0044] For example, in the semiconductor devices (semiconductor modules) of WO 2022/059251 A and WO 2022/264851 A, the conductor pattern, which is a part of the auxiliary emitter wiring corresponding to the conductor pattern **204**B and through which no main current flows, and the emitter electrode of the semiconductor element are directly connected by a bonding wire as illustrated in FIG. **3**. That is, in the semiconductor devices of WO 2022/059251 A and WO 2022/264851 A, the auxiliary emitter wiring does not include a section where the main current flows. In such a semiconductor device, for example, variations such as inductances L**4** to L**6** in the section where no main current flows as illustrated in FIG. **5**A, occur in the inductance of the auxiliary emitter wiring with respect to each of the semiconductor elements connected in parallel. Therefore, voltage drops across the auxiliary emitter wiring vary. That is, in the semiconductor devices of WO 2022/059251 A and WO 2022/264851 A, voltage drops across the auxiliary emitter wiring for each of the semiconductor elements connected in parallel may not be made uniform using inductances in sections where the main current flows as in the semiconductor module **1** of the present embodiment. Therefore, in the semiconductor devices of WO 2022/059251 A and WO 2022/264851 A, it is difficult to reduce variations in the switching speed, the switching loss, and the like among the semiconductor elements connected in parallel.

[0045] Also, in the semiconductor device (semiconductor module) of JP 2023-167403 A, the conductor pattern **202**B and the conductor pattern corresponding to the conductor pattern **204**B are connected by one bonding wire as illustrated in FIG. **3**. In such a semiconductor device, for example, variations such as inductances L**1** to L**3** in sections

where the main current flows as illustrated in FIG. **5**A, occur, resulting in variations in the voltage drop. That is, in the semiconductor device of JP 2023-167403 A, voltage drops across the auxiliary emitter wiring for each of the semiconductor elements connected in parallel may not be made uniform using the combination of inductances in sections where the main current flows and inductances in sections where no main current flows as in the semiconductor module **1** of the present embodiment. Therefore, in the semiconductor device of JP 2023-167403 A, it is difficult to reduce variations in the switching speed, the switching loss, and the like among semiconductor elements connected in parallel. Also, in the semiconductor device of WO 2020/054806 A, the two configurations of JP 2023-167403 A are connected in parallel, and similarly, voltage drops are not made uniform using inductances in sections where the main current flows.

[0046] FIG. **6** is a partially enlarged plan view for illustrating a conventional example of the auxiliary emitter wiring in the semiconductor module in which a plurality of semiconductor elements is connected in parallel. FIG. **7**A is an equivalent circuit diagram for illustrating an example of the inductance of the auxiliary emitter wiring in the semiconductor module of FIG. **6**, and FIG. **7**B is a graph illustrating an example of a switching operation in the semiconductor module of FIG. **6**. FIG. **8** is a partially enlarged plan view for illustrating a modification of the semiconductor module according to the embodiment.

[0047] Similarly to the semiconductor module **1** of the present embodiment, three semiconductor elements (switching elements) **3**D to **3**F as illustrated in FIG. **6** are connected in parallel between the third main terminal **803** and the second main terminal **802** (sec FIG. **7**A). The emitter electrode **301** of each of the semiconductor elements **3**D to **3**F disposed on the conductor pattern **201**B of the wiring board **2** is connected to the conductor pattern **202**B of the wiring board **2**, and the emitter electrode **301** of each of the semiconductor elements **3**D and **3**F is directly connected to the conductor pattern **202**B by each of the bonding wires **57**D and **57**F, whereas the emitter electrode **301** of the semiconductor element **3**E is connected to the conductor pattern **202**B through the anode electrode of the diode (semiconductor element) **4** connected in anti-parallel. Also, in the semiconductor module as illustrated in FIG. **6**, the conductor pattern **202**B and the conductor pattern **204**B which is a part of the auxiliary emitter wiring and is connected to the control terminal (auxiliary emitter terminal) (not illustrated) are connected by one bonding wire **74**. That is, the auxiliary emitter wiring of the semiconductor module as illustrated in FIG. **6** is similar to, for example, the auxiliary emitter wiring of the semiconductor device of JP 2023-167403 A.

[0048] When focusing on inductance, the auxiliary emitter wiring in the semiconductor module as illustrated in FIG. **6** may represented as the equivalent circuit diagram of FIG. **7**A. In FIG. **7**A, a white circle (○) with "E" corresponds to the connection point E between the emitter electrode **301** of the semiconductor elements **3**D, **3**E, and **3**F and each of the bonding wires **57**D, **56**, and **57**F as illustrated in FIG. **6**. Also, connection point KK**6** in FIG. **7**A corresponds to connection point K**6** of the bonding wire in FIG. **6**.

[0049] In the semiconductor module as illustrated in FIG. **6**, the length from the connection point E to the connection point K**01** in the auxiliary emitter wiring for the semiconductor element **3**D and the length from the connection point E to the connection point K**03** in the auxiliary emitter wiring for the semiconductor element **3**F are substantially the same. However, the length from the connection point E to the connection point K**02** in the auxiliary emitter wiring for the semiconductor element **3**E is longer than lengths between the connection points in the auxiliary emitter wiring for each of the semiconductor elements **3**D and **3**F. Also, as compared with the distance from the connection point K**01** to the connection point K**6** in the auxiliary emitter wiring with respect to the semiconductor element **3**D, the distance from the connection point K**02** to the connection point K**6** in the auxiliary emitter wiring with respect to the semiconductor element **3**E and the distance from the connection point K**03** to the connection point K**6** in the auxiliary emitter wiring with respect to the semiconductor element **3**F become longer. In such a semiconductor module, as in inductances L**8** to L**10** illustrated in FIG. **7**A, variations in the inductance in sections from the connection point E through which the main current flows in the auxiliary emitter wiring for each of the semiconductor elements **3**D to **3**F to the connection point K**6** become even greater. That is, variations in the voltage drop of the auxiliary emitter wiring with respect to each of the semiconductor elements (switching elements) **3**D to **3**F become greater. In this case, as illustrated in FIG. **7**B, there is a tendency for variations in the switching speed, the switching loss, and the like to become greater among the three semiconductor elements **3**D to **3**F connected in parallel. FIG. **7**B schematically illustrates waveforms of the collector current Ic and the collector-emitter voltage Vce during the turn-on of the semiconductor elements **3**D to **3**F, which are associated with the switching speed and the switching loss.

[0050] On the other hand, in the semiconductor module **1** according to the present embodiment, for example, as illustrated in FIG. **8**, the conductor pattern **202**B and the conductor pattern **204** of the wiring board **2**B are connected by separate bonding wires **74**D to **74**F for each of the emitter electrodes **301** of the three semiconductor elements **3**D to **3**F connected in parallel. At this time, as described above, the longer the auxiliary emitter wiring is, the shorter the wiring section common to the path of the main current in the auxiliary emitter wiring is, so that it is possible to reduce variations in voltage drops among the auxiliary emitter wiring for each of three semiconductor elements (switching elements) **3**D to **3**F connected in parallel, and it is possible to reduce variations in the switching speed, the switching loss, and the like among the semiconductor elements **3**D to **3**F. Also, as illustrated in FIG. **8**, in a case where dimensions of the semiconductor element **3** which is a switching element and the semiconductor element **4** which is a diode element are different from each other in a plan view, by disposing the semiconductor element **3** and the semiconductor element **4** in a staggered manner, the semiconductor element **3** and the semiconductor element **4** may be densely disposed as compared with a case where the semiconductor element **3** and the semiconductor element **4** are disposed such that distances to the conductor pattern **202**B are the same (see FIG. **3**), which is advantageous for downsizing of the semiconductor module **1** and the like.

[0051] Note that the number of semiconductor elements (switching elements) **3** connected in parallel in the semiconductor module **1** is not limited to three described above, and may be two, or four or more. Also, the switching

element is not limited to the IGBT element, and may be configured with, for example, a power metal oxide semiconductor field effect transistor (MOSFET), a bipolar junction transistor (BJT), or the like. In a case where the switching element is a power MOSFET, the auxiliary source wiring connected to a source electrode of the MOSFET is provided as a line corresponding to the auxiliary emitter wiring. Also, the diodes connected in anti-parallel to the switching element may be configured with, for example, a schottky barrier diode (SBD), a junction barrier schottky (JBS) diode, a merged PN schottky (MPS) diode, a PN diode, or the like. Also, the semiconductor module **1** may use a reverse conducting (RC)-IGBT element in which a function of a switching element and a function of a diode are integrated, instead of the semiconductor element **3** which is a switching element and the semiconductor element **4** which is a diode. Furthermore, the semiconductor module **1** may include a gate drive circuit **12** (sec FIG. **4**) and the like.

[0052] In the bonding members **71** and **74** used as a part of the auxiliary emitter wiring in the semiconductor module **1**, the position of the connection point on the conductor pattern **202** side through which the main current flows is not limited to a specific position as long as the influence of the potential of the emitter electrode **301** of the semiconductor element **3** associated with the bonding member is sufficiently larger than the influence of the potential of the emitter electrode **301** of other semiconductor elements (in other words, the influence of the potential of the emitter electrode **301** of other semiconductor elements become sufficiently small). Also, for example, the extending directions of the bonding members (bonding wires) **71** and **74** in the plan view may be directions different from the extending directions of the bonding members **53** and **57**. Furthermore, the extending directions of the bonding wires **74**D, **74**E, and **74**F in the plan view may not be the same. The bonding members **71** and **74** used as a part of the auxiliary emitter wiring in the semiconductor module I may be directly connected to control terminals (auxiliary emitter terminals) **806** and **807** provided in the case **8** without going through the conductor patterns of the wiring board **2**.

[0053] Instead of bonding wires, metal plates such as copper plates may be used for some of the bonding members in the semiconductor module **1**. For example, the bonding member **51** for connecting the first main terminal **801** and the conductor pattern **201**A of the wiring board **2**A, the bonding member **53** for connecting the emitter electrode of each of the semiconductor elements **3**A to **3**C and the conductor pattern **202**A of the wiring board **2**A, the bonding member **56** for connecting the emitter electrode of each of the semiconductor elements **3**D to **3**F and the conductor pattern **202**B of the wiring board **2**B, and the like may be metal plates referred to as leads, lead frames, and the like. The wiring board **2** in the semiconductor module **1** may be, for example, one in which the heat dissipation pattern **208** is omitted.

[0054] The semiconductor module **1** of the above embodiment is not limited to a specific application, but in particular, the semiconductor module **1** including the cooler **11** is suitable for use in a high-temperature environment. For example, the semiconductor module **1** of the above-described embodiment may be applied to a power conversion apparatus such as an inverter apparatus of an in-vehicle motor. A vehicle to which the semiconductor module **1** according to the present invention is applied is described with reference to FIG. **9**.

[0055] FIG. **9** is a schematic plan view for illustrating an example of a vehicle to which the semiconductor module according to the present invention is applied. A vehicle **1501** illustrated in FIG. **9** is configured with, for example, a four-wheeled vehicle including four wheels **1502**. The vehicle **1501** may be, for example, an electric vehicle that drives wheels by a motor or the like, or a hybrid vehicle using power of an internal combustion engine in addition to the motor. Also, the vehicle to which the semiconductor module **1** is applied is not limited to a four-wheeled vehicle, and may be a two-wheeled vehicle, a railway vehicle, or the like.

[0056] The vehicle **1501** includes a drive unit **1503** that applies power to the wheels **1502** and a control apparatus **1504** that controls the drive unit **1503**. The drive unit **1503** may be configured with, for example, at least one of an engine, the motor, and a hybrid of the engine and the motor.

[0057] The control apparatus **1504** performs control (for example, power control) on the drive unit **1503**. The control apparatus **1504** has the semiconductor module **1** including the cooler **11** of the above-described embodiment. The semiconductor module **1** may be configured to perform power control on the drive unit **1503**.

[0058] The semiconductor module **1** of the above-described embodiment may be applied to, for example, an industrial power conversion apparatus such as an inverter apparatus that drives a motor of an elevator, an escalator, an air conditioning system of a building, or the like. Also, the circuit formed in the semiconductor module **1** is not limited to the half-bridge inverter circuit as illustrated in FIG. **4**. The circuit formed in the semiconductor module **1** may have, for example, only an upper arm (circuit portion between the main terminal **801** and the main terminal **803**) or a lower arm (circuit portion between the main terminal **803** and the main terminal **802**) in the half-bridge circuit of FIG. **4**, or may have a plurality of (for example, three) half-bridge inverter circuits. The circuit formed in the semiconductor module **1** may be a full-bridge inverter circuit. Furthermore, the circuit formed in the semiconductor module **1** is not limited to the power conversion circuit that converts direct current into alternating current, and may be another circuit.

[0059] Hereinafter, feature points in the above-described embodiment will be summarized.

[0060] The semiconductor module according to the above-described embodiment includes: a wiring board having a first conductor pattern and a second conductor pattern disposed on one surface of an insulating substrate; a plurality of semiconductor elements disposed on the first conductor pattern of the wiring board; a first bonding member for connecting each of the first main electrodes of the plurality of semiconductor elements to the first conductor pattern; a second bonding member for connecting each of the second main electrodes of the plurality of semiconductor elements to the second conductor pattern; a first terminal connected to the first main electrodes of the plurality of semiconductor elements through the first conductor pattern, through which a main current flows; a second terminal connected to the second main electrodes of the plurality of semiconductor elements through the second conductor pattern, through which a main current flows; and a third terminal connected to the second conductor pattern through a third bonding

member. Each of the plurality of semiconductor elements includes a switching element that controls a current flowing between the first main electrode and the second main electrode, the third bonding member includes a plurality of bonding members associated with each of the plurality of semiconductor elements, and the distance from a connection point of the plurality of bonding members on the second conductor pattern to a connection point of the second bonding member varies depending on the distance from a predetermined position in the third terminal to a connection point with the second bonding member in the second main electrode of the plurality of semiconductor elements.

[0061] In the semiconductor module according to the above embodiment, the plurality of semiconductor elements include a first semiconductor element and a second semiconductor element, and in a case where the distance from the predetermined position in the third terminal to a connection point with the second bonding member in the second main electrode of the first semiconductor element is longer than the distance from the predetermined position in the third terminal to a connection point with the second bonding member in the second main electrode of the second semiconductor element, the distance from a connection point of a bonding member associated with the first semiconductor element in the third bonding member to a connection point of the second bonding member connected to the second main electrode of the first semiconductor element on the second conductor pattern is shorter than the distance from a connection point of a bonding member associated with the second semiconductor element in the third bonding member to a connection point of the second bonding member connected to the second main electrode of the second semiconductor element.

[0062] In the semiconductor module according to the above embodiment, the third terminal is connected to a control circuit that generates a control signal to be applied to the control electrodes of the plurality of semiconductor elements.

[0063] In the semiconductor module according to the above embodiment, each of the plurality of semiconductor elements includes the switching element and a diode connected in anti-parallel to the switching element.

[0064] The semiconductor module according to the above embodiment further includes a plurality of second semiconductor elements connected to each of the plurality of semiconductor elements, and each of the plurality of second semiconductor elements includes a diode connected in anti-parallel to the switching element in each of the plurality of semiconductor elements.

[0065] In the semiconductor module according to the above embodiment, the second bonding member includes a bonding member that connects, through an electrode of one semiconductor element of the plurality of second semiconductor elements, the second main electrode of the semiconductor element and the second conductor pattern.

[0066] In the semiconductor module according to the above embodiment, the plurality of semiconductor elements is disposed on the first conductor pattern such that lengths from a connection point with the second main electrode in the second bonding member to a connection point with the second conductor pattern are substantially the same.

[0067] In the semiconductor module according to the above embodiment, the first bonding member is a bonding material, and the second bonding member and the third bonding member are bonding wires.

[0068] In the semiconductor module according to the above embodiment, the switching element is an insulated gate bipolar transistor (IGBT) element, the first main electrode is a collector electrode of the IGBT element, and the second main electrode is an emitter electrode of the IGBT element.

[0069] In the semiconductor module according to the above embodiment, the plurality of semiconductor elements is disposed such that distances to the second conductor pattern are the same.

[0070] The semiconductor module according to the above embodiment further includes a cooler which is disposed in a direction opposite to a direction in which the semiconductor element is disposed in the wiring board and which is connected to the wiring board.

[0071] The vehicle according to the above-described embodiment includes the semiconductor module according to the above embodiment.

[0072] Note that the present invention is not limited to the above-described embodiments, and various changes, substitutions, and modifications may be made without departing from the spirit of the technical idea. Further, when the technical idea may be implemented in another method by the progress of the technology or another derived technology, the technical idea may be carried out by using the method thereof. Therefore, the claims cover all implementations that may be included within the scope of the technical idea.

[0073] As described above, the present invention has an effect that variations in switching operation among a plurality of switching elements connected in parallel in a semiconductor module may be reduced, and a decrease in operation reliability of the semiconductor module due to variations in heat generation of the switching elements may be suppressed, and is particularly useful for an industrial or on-vehicle semiconductor module used as a power conversion apparatus.

What is claimed is:

1. A semiconductor module comprising:

a wiring board, having:

an insulating substrate, and

a first conductor pattern and a second conductor pattern disposed on a surface of the insulating substrate;

a plurality of semiconductor elements disposed on the first conductor pattern of the wiring board, each having a switching element including a first main electrode and a second main electrode, and controlling a current flowing between the first main electrode and the second main electrode;

a first bonding member connecting each of the first main electrodes of the plurality of semiconductor elements to the first conductor pattern;

a second bonding member connecting each of the second main electrodes of the plurality of semiconductor elements to the second conductor pattern;

a first terminal connected to the first main electrodes of the plurality of semiconductor elements through the first conductor pattern;

a second terminal connected to the second main electrodes of the plurality of semiconductor elements through the second conductor pattern; and

a third terminal connected to the second conductor pattern through a plurality of third bonding members respectively corresponding to the plurality of semiconductor elements, wherein

a distance between a connection point of each of the plurality of third bonding members to the second conductor pattern and a connection point of the second bonding member to the second conductor pattern varies depending on a distance between a predetermined position in the third terminal and a connection point of the second bonding member to the second main electrode of each of the plurality of semiconductor elements.

2. The semiconductor module according to claim **1**, wherein

the plurality of semiconductor elements includes a first semiconductor element and a second semiconductor element,

the plurality of third bonding members includes a first third bonding member and a second third bonding member corresponding to the first semiconductor element and the second semiconductor element, respectively,

the distance between the predetermined position in the third terminal and the connection point of the second bonding member to the second main electrode of the first semiconductor element is longer than the distance between the predetermined position in the third terminal and the connection point of the second bonding member to the second main electrode of the second semiconductor element, and

the distance between the connection point of the first third bonding member to the second conductor pattern and the connection point of the second bonding member to the second main electrode of the first semiconductor element is shorter than the distance between the connection point of the second third bonding member to the second conductor pattern and the connection point of the second bonding member to the second main electrode of the second semiconductor element.

3. The semiconductor module according to claim **1**, wherein

the third terminal is configured to receive, from a control circuit, a control signal, and to apply the control signal to each of the plurality of switching elements.

4. The semiconductor module according to claim **3**, wherein

each of the plurality of semiconductor elements is a semiconductor chip that includes the switching element and a diode connected in anti-parallel to the switching element.

5. The semiconductor module according to claim **3**, further comprising:

a plurality of second semiconductor elements connected to each of the plurality of semiconductor elements,

wherein each of the plurality of second semiconductor elements includes:

a diode connected in anti-parallel to the switching element.

6. The semiconductor module according to claim **5**, wherein

each of the second semiconductor elements has an electrode, and

the second bonding member includes a plurality of bonding members that respectively connects, the plurality of electrodes, the second main electrodes of the semiconductor elements of the plurality of second semiconductor elements and the second conductor pattern.

7. The semiconductor module according to claim **1**, wherein the plurality of semiconductor elements is disposed on the first conductor pattern such that distances respectively between connection points of the second bonding member to the second main electrodes of the plurality of semiconductor elements and connection points of the second bonding member to the second conductor pattern are substantially the same.

8. The semiconductor module according to claim **1**, wherein

the first bonding member is a bonding material, and

each of the second bonding member and the third bonding members is a bonding wire.

9. The semiconductor module according to claim **1**, wherein

the switching element is an insulated gate bipolar transistor (IGBT) element,

the first main electrode is a collector electrode of the IGBT element, and

the second main electrode is an emitter electrode of the IGBT element.

10. The semiconductor module according to claim **1**, wherein the plurality of semiconductor elements is disposed such that distances respectively between the plurality of semiconductor elements and the second conductor pattern are the same.

11. The semiconductor module according to claim **1**, further comprising:

a cooler connected to the wiring board, the cooler and the plurality of semiconductor elements being disposed on opposite sides of the wiring board.

12. A vehicle comprising the semiconductor module according to claim **10**.

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