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Three-dimensional ferroelectric random-access memory (FeRAM)

Abstract

A 3-dimensional vertical memory string array includes high-speed ferroelectric field-effect transistor (FET) cells that are low-cost, low-power, or high-density and suitable for SCM applications. The memory circuits of the present invention provide random-access capabilities. The memory string may be formed above a planar surface of substrate and include a vertical gate electrode extending lengthwise along a vertical direction relative to the planar surface and may include (i) a ferroelectric layer over the gate electrode, (ii) a gate oxide layer; (iii) a channel layer provided over the gate oxide layer, and (iv) conductive semiconductor regions embedded in and isolated from each other by an oxide layer, wherein the gate electrode, the ferroelectric layer, the gate oxide layer, the channel layer and each adjacent pair of semiconductor regions from a storage transistor of the memory string, and wherein the adjacent pair of semiconductor regions serve as source and drain regions of the storage transistor.

Inventors: **Chen; Yung-Tin (Taoyuan, TW)**

Applicant: **SAMSUNG ELECTRONICS CO., LTD.** (Suwon-si, KR)

Family ID: **1000008748357**

Assignee: **SAMSUNG ELECTRONICS CO., LTD. (Suwon-si, KR)**

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Primary Examiner: Rahman; Moin M

Attorney, Agent or Firm: Sughrue Mion, PLLC

Background/Summary

CROSS REFERENCE TO RELATED APPLICATIONS (1) The present application is a continuation-in-part of U.S. patent application ("Parent Application I"), Ser. No. 17/039,746, entitled "THREE-DIMENSIONAL FERROELECTRIC RANDOM-ACCESS MEMORY (FERAM)," filed on Sep. 30, 2020, which is a divisional application of U.S. patent application ("Parent Application II), Ser. No. 16/733,102, entitled "Three-Dimensional Ferroelectric Random-Access Memory (FeRAM)," filed on Jan. 2, 2020, which is a continuation-in-part application of U.S. patent application ("Parent Application III"), Ser. No. 16/558,072, entitled "Three-

Dimensional Ferroelectric Random-Access Memory (FeRAM),” filed on Aug. 31, 2019, which is related to and claims priority of U.S. provisional patent application (“Provisional Application”), Ser. No. 62/846,418, entitled “3D Ferroelectric Random-Access Memory With MLC Capability,” filed on May 10, 2019. (2) The disclosures of Parent Application I, Parent Application II, Parent Application III and Provisional Application are hereby incorporated by reference in their entireties.

BACKGROUND OF THE INVENTION

1. Field of the Invention

(1) The present invention relates to memory circuits. In particular, the present invention relates to high-density, ferroelectric random-access memory arrays including memory cells provided in a 3-dimensional configuration.

2. Discussion of the Related Art

(2) An erase operation in a 3-dimensional non-volatile memory circuits (e.g., NAND-type flash memory circuits) is typically carried out on a block-by-block basis, which involves a long access time. Such memory circuits are not suitable for use in high speed (˜50 ns), high density storage class memory (SCM) applications.

(3) Other alternative memory circuits, for example, include: (i) 3D XPoint memory circuits, jointly developed by Intel Corporation and Micron Corporation, while allowing bit-by-bit access that is suitable for SCM applications, use cross-point patterning (i.e., double exposures for patterning each material layer), which is prohibitively high in manufacturing cost. Also, such 3D XPoint memory circuits are based on a phase-change material (PCM), which results in high leakage currents and, hence, high power dissipation from sneak paths. Selector devices are needed to reduce the leakage currents from sneak paths, which increase the complexity of process and device integration. (ii) U.S. Pat. Nos. 10,249,370, 10,121,554, 10,121,553, and 9,892,800 disclose 3-dimensional vertical NOR-type memory string arrays, which require complicated X and Y patterning schemes. Due to NOR architecture, the power consumption is also high.

(4) Ferroelectric memory circuits provide yet another alternative. U.S. Pat. No. 6,067,244 to T. Ma, entitled “Erroelectric Dynamic Random Access Memory, filed on Sep. 16, 1998, discloses a ferroelectric field-effect transistor (FeFET) that can serve as a memory circuit, as dipole moments in the FeFET can be aligned in either one of two configurations by an electric field. However, conventional ferroelectric materials, such as those based on lead zirconate titanate (PZT) and strontium bismuth tantalate (SBT), for example, do not provide high-density memory circuits. This is because the ferroelectric layer in an FeFET based on these materials must at least 70 nm thick.

(5) FeFETs based on Hafnium oxide (HfO.sub.2) are, however, promising. U.S. patent application publication 2018/0366547A1 (“Liu”) discloses various examples of FeFETs. For example, FIGS. **2***a* and **2***b*, reproduced respectively from FIG. **4**A and FIG. **4**B in Liu's disclosure, illustrate the programmed states of exemplary FeFET **1**.

(6) As shown in both FIGS. **2***a* and **2***b*, FeFET **1** is formed on a p.sup.+-type substrate **10** and includes n.sup.+-type source and drain regions **101** and **102**, respectively, channel region **103**, tunneling dielectric layer **13**, charge storage region **12** and gate electrode **11**. Charge region **12** includes ferroelectric layer **120** and paraelectric layer **121**. Paraelectric layer **121** has a “quantum well” energy band structure, which enables a charge-trapping capability suitable for a data storage application. Paraelectric layer **121** may have, for example, alternating layers of a base material and a dielectric material. The base material may be, for example, Hf.sub.1-xSi.sub.xO.sub.2—x being a value between 0.02 and 0.65, while the dielectric material may be selected from the group consisting of hafnium oxide, zirconium oxide, titanium oxide, titanium nitride, tantalum nitride, aluminum oxide, tantalum oxide and any combination thereof. The alternating layers of base and dielectric materials may be formed using, for example, ALD processes.

(7) Ferroelectric layer **120** may include an alkaline earth metal oxide or a transition metal oxide, such as hafnium oxide, zirconium oxide or hafnium zirconium oxide, with or without a 2-10%

dopant selected from the group consisting of silicon, aluminum, yttrium, strontium, gadolinium, lanthanum and any combination thereof. One example of a ferroelectric material is Hf.sub.1-xSi.sub.xO.sub.2, x ranging between 0.01 and 0.05. The composite material may also include hydrogen atoms in the manufacturing process. Liu discloses that the charge storage region **12** may be 1.0-30.0 nm thick, preferably 5.0-15.0 nm thick.

(8) As shown in FIG. **2***a*, when a positive bias (e.g., Vt) is applied to gate electrode **11**, the electric dipoles in the ferroelectric layer **12** align with the electric field, such that electrons in channel region **103** tunnel through tunnel dielectric layer **13** into and are trapped in paraelectric layer **121**. The trapped charge causes positive charge carriers (i.e., holes) to accumulate in channel region **103** ("0" state, which provides a polarization switching voltage for the storage transistor). In this "0" state, FeFET **1** is non-conducting at the read voltage.

(9) As shown in FIG. **2***b*, when a negative bias (e.g., −Vt) is applied to gate electrode **11**, the electric dipoles in charge storage region **12** allow holes in channel region **103** to tunnel to and be trapped in paraelectric layer **121**. The trapped charge cause electron accumulation at channel region **103** ("1" state, which provides a negative polarization switching voltage). In this "1" state, FeFET **1** conducting at the read voltage.

(10) Liu also discloses that the ferroelectric layer **120** and paraelectric layer **121** need not be distinct. The ferroelectric layer **120** and paraelectric layer **121** may be provided as a single layer as a blend of the ferroelectric and paraelectric materials.

(11) As disclosure in Liu, a hafnium oxide-based FeFET may be made with a ferroelectric layer that is less than 10 nm thick. Furthermore, such an FeFET may provide a 1-volt threshold-shift window. For example, the article, entitled "Low-Leakage-Current DRAM-Like Memory Using a One-Transistor Ferroelectric MOSFET With a Hf-Based Gate Dielectric" ("Cheng"), by C. Cheng and A. Chin, published in IEEE Electronic Device Letters, vol. 35, No. 1, 2014, pp. 138-140, disclose a high-endurance FeFET with a 30 nm thick zirconium-doped HfO.sub.2 ferroelectric layer that can be programmed or erase in 5 ns.

(12) FIG. **1***a* shows an architecture of an AND-type FeFET array that can be laid out in a conventional 4F.sup.2 configuration. FIG. **1***a* also provides a table that shows the voltage biases for the word line (WL(m), the source line (SL(m)) and the bit line (BL(m)) of a selected FeFET, as well as the voltage biases for the word line (WL(m+1), the source line (SL(m+1)) and the bit line (BL(m+1)) of a non-selected FeFET, during program, erase and read operations. In Cheng, for example, the programming voltage V.sub.pmg and the read voltage V.sub.read for such an FeFET may be −4.0 volts and −0.1 volts, respectively.

(13) FIG. **1***b* shows an architecture of a NOR-type FeFET array. FIG. **1***b* also provides a table that shows the voltage biases for the word line (WL(m), the source line (SL(m)) and the bit line (BL(m)) of a selected FeFET, as well as the voltage biases for the word line (WL(m+1), the source line (SL(m+1)) and the bit line (BL(m+1)) of a non-selected FeFET, during program, erase and read operations.

SUMMARY

(14) The present invention provides a 3-dimensional vertical memory string array that includes high-speed ferroelectric field-effect transistor (FET) cells that are low-cost, low-power, or high-density and suitable for SCM applications. The memory circuits of the present invention provide random-access capabilities.

(15) According to one embodiment of the present invention, a memory string formed above a planar surface of substrate includes: (a) a vertical gate electrode (e.g., tungsten or a heavily doped semiconductor) extending lengthwise along a vertical direction relative to the planar surface, (b) a ferroelectric layer provided over at least a portion of the gate electrode along a horizontal direction substantially parallel the planar surface and extending lengthwise along the vertical direction; (c) a gate oxide layer provided over at least a portion of the ferroelectric layer along the horizontal direction and extending lengthwise along the vertical direction; (d) a channel layer provided over at

least a portion of the gate oxide layer along the horizontal direction and extending lengthwise along the vertical direction; and conductive semiconductor regions embedded in and isolated from each other by an oxide layer arrayed along the horizontal direction, wherein the gate electrode, the ferroelectric layer, the channel layer, the gate oxide layer and each adjacent pair of semiconductor regions from a storage transistor of the memory string, and wherein the adjacent pair of semiconductor regions serve as source and drain regions of the storage transistor. In addition, a barrier layer (e.g., titanium nitride, tungsten nitride or tantalum nitride) may be provided between the gate electrode and the ferroelectric layer. The drain or source region may also be provided drain or source electrodes (e.g., tungsten or n.sup.+ polysilicon).
(16) The memory strings of the present invention may be organized into a memory array, and a staircase configuration provides electrical contacts to each of the source or drain electrodes. Storage transistors may be provided on opposite sides of each memory hole in which the gate, the ferroelectric layer, the gate oxide layer and the channel silicon layer are provided. One or more networks of global word line conductors each connecting the gate electrodes of a selected group of the memory strings may be provided above the memory array, below the memory array or both.
(17) The ferroelectric layer comprises a zirconium-doped or silicon-doped HfO.sub.2 ferroelectric material. The zirconium-doped hafnium silicon oxide may have a zirconium content of 40-60%, preferably 45-55%. The silicon-doped hafnium silicon oxide may have a silicon content of 2.0-5.0%, preferably 2.5-4.5%. The hafnium silicon oxide is prepared by depositing HfO.sub.2 and SiO.sub.2 or ZrO.sub.2 using an ALD layer-by-layer lamination step.
(18) In one embodiment the memory string further includes a charge-trapping layer that is between the gate oxide layer and the ferroelectric layer or between the ferroelectric layer and the barrier layer.
(19) In one embodiment, the channel layer and the conductive semiconductor regions are provided by doped silicon carbide (SiC) materials, formed using chemical vapor deposition (CVD) or atomic layer deposition (ALD).
(20) Various manufacturing processes, some of which are illustrated herein, may be used to fabricate a memory array of the memory strings of the present invention.
(21) The present invention is better understood upon consideration of the detailed description below in conjunction with the accompanying drawings.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
(1) FIG. **1***a* shows an architecture of an AND-type FeFET array that can be laid out in a conventional 4F.sup.2 configuration.
(2) FIG. **1***b* shows an architecture of a NOR-type FeFET array.
(3) FIGS. **2***a* and **2***b*, reproduced from FIGS. 4A and 4B of U.S. patent application publication 2018/0366547A1 (“Liu”), illustrate the programmed states of exemplary FeFET **1**.
(4) FIG. **3***a* shows a vertical section of memory array **300**, which includes a regular arrangement of vertical 3-dimensional (3-D) FeFET strings; FIG. **3***a* shows, in particular, vertical 3-D FeFET strings **300***a*, **300***b* and **300***c*, according to one embodiment of the present invention.
(5) FIG. **3***b* shows an Y-Z plane cross section of memory array **300**, showing the gate, drain and source connectivity's of eight vertical 3-D FeFET strings, according to one embodiment of the present invention.
(6) FIGS. **4***a*, **4***b*, **4***c*, **4***d*(*i*), **4***d*(*ii*), **4***e*, **4***f*, **4***g*, **4***h*(*i*), **4***h*(*ii*), **4***i*(*i*), **4***i*(*ii*), **4***j*(*i*), **4***j*(*ii*), **4***k*(*i*), **4***k*(*ii*), **4***l*(*i*), and **4***l*(*ii*) illustrate an exemplary fabrication process for memory array **400**, in accordance with one embodiment of the present invention.
(7) FIG. **5** shows memory array **400** provided electrical contacts or connections to drain or source

electrodes **423** via staircase structures on both sides of memory array **400** and contacts or connections to gate electrodes **423** using the bottom global word lines (e.g., global word line **401**).
(8) FIGS. **6***a*, **6***b*, **6***c*(*i*), **6***c*(*ii*), **6***d*, **6***e*, **6***f*(*i*), **6***f*(*ii*), **6***g*(*i*), **6***g*(*ii*), **6***h*(*i*), **6***h*(*ii*), **6***i*, and **6***j* illustrate an exemplary fabrication process for memory array **600**, in accordance with one embodiment of the present invention.
(9) FIGS. **7***a*, **7***b*(*i*), **7***b*(*ii*), **7***c*(*i*), **7***c*(*ii*), **7***d*, **7***e*, **7***f*, and **7***g* illustrate an exemplary fabrication process for memory array **700**, in accordance with one embodiment of the present invention.
(10) FIGS. **8***a*, **8***b*-**1**, **8***b*-**2**, **8***c*, **8***d*-**1**, **8***d*-**2**, **8***e*, **8***f*, **8***g*(*i*), **8***g*(*ii*), **8***h*(*i*), **8***h*(*ii*), **8***i*(*i*), **8***i*(*ii*), **8***i*(*iii*) and **8***j* illustrate an exemplary fabrication process for memory array **800**, in accordance with one embodiment of the present invention.
(11) To facilitate cross-referencing among the figures, like elements are assigned like reference numerals. The figures may depict 3-dimensional objects from different perspectives. To facilitate description of 3-dimensional objects, a cartesian coordinate system is provided, with X- and Y-directions denoting orthogonal horizontal directions and the Z-direction denoting the vertical direction. As this detailed description refers to structures fabricated on a planar surface of a substrate, “vertical” is understood to refer to the direction substantially perpendicular to the planar surface and “horizontal” is understood to refer to directions substantially parallel to the planar surface.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

(12) The present invention may be carried out by, for example, a vertical metal-ferroelectric-insulator semiconductor (MFIS) transistor that includes (a) tungsten/titanium nitride or n.sup.+ polysilicon/titanium nitride gate electrode, (ii) zirconium-doped or silicon-doped HfO.sub.2 ferroelectric layer, (iii) a gate oxide layer, (iv) a p-type channel region, (v) an n-type source region, and (v) an n-type drain region.
(13) In such an MFIS transistor, n.sup.+ polysilicon in the gate electrode may be arsenic-doped polysilicon with dopant concentration of 5.0×10.sup.21 to 1.0×10.sup.22 cm.sup.−3. The HfO.sub.2 ferroelectric layer may be 5.0-15.0 nm thick, preferably 8.0-12.0 nm thick, deposited by ALD. If doped by zirconium, the ferroelectric layer should have zirconium content of 40-60%, preferably 45-55%. If doped by silicon, the ferroelectric layer should have silicon content of 2.0-5.0%, preferably 2.5-4.5%. The gate oxide layer may be, for example, 1.0-3.0 nm thick silicon oxide (SiO.sub.2) or silicon oxynitride (SiON). The p-type channel region may be, for example, intrinsic polysilicon or boron-doped polysilicon with a dopant concentration of 1.0×10.sup.16 to 1.0×10.sup.18 cm.sup.−3, deposited by CVD, using any of boron, diborane (H.sub.2B.sub.2), and trimethyl borane (B(CH.sub.3).sub.3 gases, or any of their combinations). The n-type drain and source regions may each be, for example, phosphorus-doped or arsenic-doped polysilicon with a dopant concentration of 1.0×10.sup.20 to 1.0×10.sup.22 cm.sup.−3, deposited by CVD, using phosphine (PH.sub.3) or phosphorus trichloride (PCl.sub.3), if phosphorus-doped, and arsenic or arsenic hydride (AsH.sub.3), if arsenic-doped.
(14) Alternatively, in some embodiments, the p-type channel region may be, for example, boron-doped or aluminum-doped SiC with a dopant concentration of 1.0×10.sup.15 to 1.0×10.sup.18 cm.sup.−3, deposited by ALD or CVD. SiC may be deposited using an ALD process, at a temperature between 590° C.-675° C., using acetylene (C.sub.2H.sub.2) or ethylene (C.sub.2H.sub.4), as a carbon precursor, and silicon chloride (Si.sub.2Cl.sub.2) or silicon hydride (Si.sub.2H.sub.6) as a silicon precursor. The n-type drain region and the n-type source region may be similarly provided by ALD nitrogen-doped or phosphorus-doped SiC, with a dopant concentration of 1.0×10.sup.19 to 1.0×10.sup.22 cm.sup.−3.
(15) Si-doped Hf.sub.1-xSi.sub.xO.sub.y ferroelectric thin-film may be formed by depositing HfO.sub.2 and SiO.sub.2 using ALD layer-by-layer lamination, which allows the values of x and y be adjusted by the individual cycle numbers of HfO.sub.2 and SiO.sub.2. For example, x may range from 0.02 to 0.05, preferably between 0.025 and 0.04, and y may range from 1.8 to 2.2,

preferably between 1.9 and 2.1. A suitable Hf.sub.1-xSi.sub.xO.sub.y ferroelectric thin-film may be, for example, between 5.0-15.0 nm thick, preferably between 8.0-12.0 nm thick for FeFET memory applications. HfO.sub.2 may be prepared from any of the following precursors: tetrakis(ethylmethylamino) hafnium (TEMAH), tetrakis(dimethylamino) hafnium (TDMAH) and hafnium tetrachloride (HfCl.sub.4), using as oxidant O.sub.3 or H.sub.2O, at a deposition temperature between 150-400° C. Similarly, SiO.sub.2 can be prepared from any of the following precursors: tetrakis(dimethylamino) silane (4DMAS), tris(dimethylamino) silane (3DMAS), tetrakis(ethylmethylamino) silane (TEMA-Si) and silicon tetrachloride (SiCl.sub.4), using as oxidant O.sub.3 or H.sub.2O, at a deposition temperature between 150-400° C.

(16) Zr-doped Hf.sub.xZr.sub.1-xO.sub.y ferroelectric thin-films may be formed by depositing HfO.sub.2 and ZrO.sub.2 using ALD layer-by-layer lamination, which allows the values of x and y be adjusted by the individual cycle numbers of HfO.sub.2 and ZrO.sub.2. For example, x may range between 0.4 and 0.6, preferably between 0.45 and 0.55, and y may range between 1.8 and 2.2, preferably between 1.9 to 2.1. A suitable Hf.sub.xZr.sub.1-xO.sub.y ferroelectric thin-film may be 5.0-15.0 nm thick, preferably 8.0-12.0 nm thick for FeFET memory applications. HfO.sub.2 may be prepared from any of the following precursors: tetrakis(ethylmethylamino) hafnium (TEMAH), tetrakis(dimethylamino) hafnium (TDMAH), and hafnium tetrachloride (HfCl.sub.4), using as oxidant O.sub.3 or H.sub.2O, at a deposition temperature of 150-400° C. ZrO.sub.2 may be prepared from any of the following precursors: tetrakis(ethylmethylamino) zirconium (TEMAZ), tetrakis(dimethylamino) zirconium (TDMAZ) and zirconium tetrachloride (ZrCl.sub.4), using as oxidant O.sub.3 or H.sub.2O, at a deposition temperature between 150-400° C.

(17) FIG. **3***a* shows a vertical section in the X-Z plane of memory array **300**, which includes a regular arrangement of vertical 3-dimensional (3-D) FeFET strings; FIG. **3***a* shows, in particular, vertical 3-D FeFET strings **300***a*, **300***b* and **300***c*, according to one embodiment of the present invention. FIG. **3***a* shows three vertical 3-D FeFET strings merely for the purpose of illustration; memory array **300** may include many more than vertical 3-D FeFET strings arranged along each of the X- and Y-directions.

(18) As shown in FIG. **3***a*, each vertical 3-D FeFET string includes (i) multiple annular drain electrodes **301-1**, **301-2**, . . . , and **301**-*n*, (ii) multiple annular source electrodes **302-1**, **302-2**, . . . , and **302**-*n*, (iii) annular channel region **303**, (iv) gate or tunnel oxide layer **303***a*, and (v) annular ferroelectric layer **304**, surrounding common gate electrode **308**. Common gate electrode **308** may have a conductor core (e.g., tungsten or heavily doped n-type polysilicon) with an outer adhesion layer or barrier layer (e.g., titanium nitride) **305**. Each vertical 3-D FeFET string is electrically isolated by top and bottom isolation layers **307** and **309**.

(19) Each drain or source electrode may be provided, for example, by n-type polysilicon or n-type SiC, titanium nitride, tungsten or any combination of these materials. Channel region may be provided, for example, by p-type polysilicon or n-type SiC. Ferroelectric layer **304** may be provided by, zirconium-doped or silicon-doped HfO.sub.2 ferroelectric material. Common gate electrode may be provided, for example, by tungsten/titanium nitride or n.sup.+ polysilicon/titanium nitride. Gate oxide layer **303***a* may be provided, for example, SiO.sub.2 or SiON.

(20) In each vertical 3-D FeFET string, each memory cell is an MFIS transistor formed by an adjacent pair of drain and source electrodes (e.g., drain electrode **301-1** and source electrode **302-1**), and the portions of channel region **303**, gate or tunnel oxide layer **303***a*, annular ferroelectric-paraelectric layer **304**, and common gate electrode **308** between the adjacent drain and source electrodes. FIG. **3***a* also shows that the gate electrodes of vertical 3-D FeFET strings **300***a*, **300***b* and **300***c* are electrically connected by conductive global word line **306**. In memory array **300**, (i) the common gate electrodes in a row of vertical 3-D FeFET strings along the X-direction are electrically connected; (ii) drain electrodes at the same vertical level of the vertical 3-D FeFET strings in a row along the Y-direction are electrically connected; and source electrodes at the same

vertical level of the vertical 3-D FeFET strings in a row along the Y-direction are electrically connected.

(21) FIG. **3***b* shows an Y-Z plane cross section of memory array **300**, showing the gate, drain and source connectivity's of eight vertical 3-D FeFET strings, according to one embodiment of the present invention. Again, FIG. **3***b* shows eight vertical 3-D FeFET strings merely for the purpose of illustration. In any embodiment, memory array **300** may include more than eight vertical 3-D FeFET strings arranged along each of the X- and Y-directions. FIG. **3***b* illustrate selection of MRS transistor or cell **401** by applying selection voltage biases on associated gate electrode **308**-*m*, drain electrode **301**-*m* and source electrode **302**-*m*. There are three types of non-selected MRS transistors: (a) "selected gate, non-selected drain or source" MFIS transistors—those sharing selected gate electrode **308**-*m*, but are associated with one of non-selected drain electrodes **301** and one of the non-selected source electrodes **302**; (b) "non-selected gate, selected drain or source" MRS transistors—those MRS transistors associated with one of the non-selected gate electrodes **308**, but associated with selected drain electrode **301**-*m* and selected source electrode **302**-*m*; and (c) "non-selected gate, non-selected drain or source" MRS transistors—those MRS transistors associated with neither selected gate electrode **308**-*m*, nor with selected drain electrode **301**-*m* and selected source electrode **302**-*m*. In a reading, programming, or erase operation, different voltage biases are required for a selected MFIS transistor and each of the three types of non-selected MRS transistors.

(22) FIGS. **4***a*-**4***l* illustrate an exemplary fabrication process for memory array **400**, in accordance with one embodiment of the present invention. As shown in vertical section in FIG. **4***a*, a network of conductors ("global gate lines"), including global gate line **402**, are formed over semiconductor substrate **401**, which may be a semiconductor wafer. The global gate lines may be formed out of tungsten, isolated from each other and from semiconductor substrate **401** by an isolation layer (e.g., silicon oxide).

(23) Thereafter, as shown in vertical section FIG. **4***b*, oxide layer **403** (e.g., silicon oxide) and bottom etch stop layer **404** (e.g., n.sup.+ polysilicon) are deposited over the global gate lines. Etch stop layer **404** may be patterned, as shown, and embedded in oxide layer **403**. Then, as shown in vertical section in FIG. **4***c*, alternating layers of silicon oxide layers **405** and silicon nitride layers **406** are deposited, numbered herein as silicon oxide layers **405**-**1**, . . . , and **405**-*n*, and silicon nitride layers **406**-**1**, . . . , **406**-*n*, respectively.

(24) An array of shafts ("memory holes") **407** (e.g., memory holes **407**-**1**, **407**-**2** and **407**-**3**) are then etched through the alternating layers of silicon oxide layers **405** and silicon nitride layers **406** down to etch stop layer **404**, as shown in vertical section in FIG. **4***d*(*i*). FIG. **4***d*(*ii*) shows in horizontal cross section through one of silicon nitride layers **406**, showing memory holes **407**-**1** to **407**-**9** of memory array **400** at this step of formation.

(25) Channel layer **409** is then conformally deposited, followed by deposition of thin gate oxide layer **410**. Channel layer **409** may be deposited as amorphous silicon and annealed at 850° C. for 2 hours to crystallize. (Alternatively, channel layer **409** may be ALD SiC). Protective layer **408** may then be deposited over gate oxide layer **410**. A spacer etch is then carried out to remove any deposited polysilicon and gate oxide from the bottom of memory holes **407**. Chemical mechanical polishing (CMP) step may be carried out to remove materials of protective layer **408**, gate oxide **410**, and channel layer **409** from the top of the structure. The resulting structure (i.e., memory array **400** at this step of formation) is shown in vertical section in FIG. **4***e*.

(26) Protective layer **408** is then removed. Ferroelectric layer **411** (e.g., a Si-doped or Zr-doped Hf.sub.1-xSi.sub.xO.sub.y, Hf.sub.xZr.sub.1-xO.sub.y ferroelectric thin-film) is then deposited. CMP and a bottom etch step removes excess ferroelectric material from the top of the structure and the bottom of memory holes **407**. The portion of etch stop layer **404** exposed at the bottom of memory holes **407** is then removed. An oxide etch then creates vias that expose the global gate lines (e.g., global gate line **402**) underlying memory holes **407**. The resulting structure (vertical

section) is shown in FIG. **4***f*.

(27) An adhesion/barrier layer of titanium nitride (TiN) **412** is then conformally deposited. An etch step then removes the TiN material from the portion of memory holes **407**. Other barrier layers (e.g., tungsten nitride or tantalum nitride) may also be used. Memory holes **407** are then filled with gate electrode material **413**, which may be a chemical vapor deposited tungsten ("CVD W") or an n.sup.+ polysilicon (i.e., a heavily doped n-type polysilicon). Excess deposited material is then removed by CMP from the top of the structure. The resulting structure (vertical section) is shown in FIG. **4***g*.

(28) Thereafter, top isolation layer **415** (e.g., silicon nitride) is provided over memory array **400**. Top isolation layer **415** is then patterned and an etch step creates slots **414** (e.g., slots **414-1**, **414-2**, **414-3** and **414-4**) through top isolation layer **415** and the alternating silicon nitride layers **406** and oxide layers **405**. The resulting structure (vertical section) is shown in FIG. **4***h*(*i*). FIG. **4***h*(*ii*) shows a horizontal cross section of memory array **400** through one of nitride layers **406**.

(29) A wet etch step (e.g., hot phosphoric acid) is carried out to remove the silicon nitride layers **406**. During this step, the silicon nitride material is removed from the exposed surfaces of silicon nitride layers **406** in the sidewalls of slots **414**. A further etch step removes exposed portions of channel layer **409** and gate oxide **410**. A layer of n.sup.+ semiconductor layer **420** (e.g., n.sup.+ polysilicon or n.sup.+ SiC) is then deposited and annealed. TiN layer **418** and tungsten **419** are then deposited successively to fill the voids left over from removing the silicon nitride. Excess n.sup.+ semiconductor, TiN and tungsten materials are removed from the top of the structure and the sidewalls of slots **414**. The resulting structure is shown in vertical and horizontal cross sections in FIGS. **4***i*(*i*) and **4***i*(*ii*), respectively. In FIG. **4***i*(*i*), the resulting structure is magnified in inset where the top two silicon nitride layers **406** (i.e., silicon nitride layers **406**-*n* and **406**-(*n*−1)) have been removed. As shown in the inset, in each of the silicon nitride layer, (a) n.sup.+ semiconductor layer **420** forms pockets in channel layer **409** and gate oxide layer **410** after thermal anneal diffusion, (b) TiN layer **418** lines the outside of n.sup.+ semiconductor layer **420**, and (c) tungsten layer **419** fills the remainder of the voids. The pockets of n.sup.+ semiconductor layer **420** become drain and source regions of an MRS transistor. TiN layers **418** and tungsten layers **419** become source or drain electrodes **423**.

(30) In some embodiments, silicon nitride layers **406** is not completely removed. As etching of silicon nitride layers **406** proceeds from the sidewalls of slots **414**, so that a strip of silicon nitride divides and electrically the resulting source or drain terminals isolates on opposite sides of each memory hole. In this manner, each memory hole now provides two vertical 3-D FeFET strings, as the n.sup.+ semiconductor pockets on opposite sides of each silicon nitride layer of each memory hole form separate drain or source regions. This alternative embodiment is illustrated in the structure is shown in vertical and horizontal cross sections in FIGS. **4***j*(*i*) and **4***j*(*ii*), respectively. As shown in FIG. **4***j*(*ii*), silicon nitride layers **421**, which is left over from the incomplete removal of silicon nitride layers **406** provide separate sets **423**L and **423**R of drain or source electrodes.

(31) Silicon oxide **422** is then deposited to fill slots **414**. A CMP step removes excess silicon oxide from the top of memory array **400**. The resulting structure in vertical and horizontal cross sections are shown in FIGS. **4***k*(*i*) and **4***k*(*ii*), respectively, for the embodiment of FIGS. **4***i*(*i*) and **4***i*(*ii*). Likewise, the resulting structure in vertical and horizontal cross sections are shown in FIGS. **4***l*(*i*) and **4***l*(*ii*), respectively, for the embodiment of FIGS. **4***j*(*i*) and **4***j*(*ii*).

(32) Connections to the drain or source electrodes **423** (or **423**L and **423**R, in the alternative embodiment) can be made using the staircase configuration used in 3-D NAND non-volatile memory arrays. FIG. **5** shows memory array **400** provided electrical contacts or connections to drain or source electrodes **423** via staircase structures on both sides of memory array **400** and contacts or connections to gate electrodes **413** using the bottom global gates (e.g., global gate **402**). The staircase configuration and associated fabrication methods are known to those of ordinary skill in the art.

(33) In one embodiment, the polarization switching voltages are ±1.5 volts across the ferroelectric capacitor layer of the MRS, for “1” and “0” states, respectively. During a programming or an erase operation, the voltage across the ferroelectric layer is roughly half of the gate-to-source voltage (V.sub.GS) of the MFIS. Thus, programming of the MRS may be achieved using a programming voltage V.sub.PGM Of 6-7 volts at the gate electrode. Table 1 shows the voltage biases for MRS transistors in memory array **400** during a programming operation:

(34) TABLE-US-00001 TABLE 1 MFIS TYPE Gate Voltage Drain Voltage Source Voltage Selected cell V.sub.PGM 0.0 0.0 Selected Gate, non- V.sub.PGM 2/3 V.sub.PGM 2/3 V.sub.PGM selected source or drain Non-selected gate, 1/3 V.sub.PGM 0.0 0.0 selected drain or source Non-selected gate, 1/3 V.sub.PGM 2/3 V.sub.PGM 2/3 V.sub.PGM non-selected drain or source

(35) As shown in Table 1, program disturb is avoided in the non-selected MRS transistors because in each case, the magnitude of half gate-to-source voltage (VS) is less than ⅓ V.sub.PGM, which is by design less than the polarization switching voltage for state “0”.

(36) Similarly, an erase operation on an MRS transistor may be achieved using an erase voltage V.sub.ERA of 6-7 volts at the gate electrode. Table 2 shows the voltage biases for MRS transistors in memory array **400** during an erase operation:

(37) TABLE-US-00002 TABLE 2 MFIS TYPE Gate Voltage Drain Voltage Source Voltage Selected cell 0.0 V.sub.ERA V.sub.ERA Selected Gate, non- 0.0 1/3 V.sub.ERA 1/3 V.sub.ERA selected source or drain Non-selected gate, 2/3 V.sub.ERA V.sub.ERA V.sub.ERA selected drain or source Non-selected gate, 2/3 V.sub.ERA V.sub.ERA V.sub.ERA non-selected drain or source

(38) As shown Table 2, erase disturb is avoided in the non-selected MRS transistors because in each case, the magnitude of half the gate-to-source voltage (V.sub.GS) are less than ⅓ V.sub.ERA, which is by design less than the polarization switching voltage for state “1”.

(39) A read operation may be achieved using a read voltage V.sub.READ of 0.0-0.5 volts at the gate electrode and drain voltage V.sub.DD at 0.5-2.0 volts. Table 3 shows the voltage biases for MRS transistors in memory array **400** during a read operation:

(40) TABLE-US-00003 TABLE 3 MFIS TYPE Gate Voltage Drain Voltage Source Voltage Selected cell V.sub.READ V.sub.DD 0.0 Selected Gate, non- V.sub.READ 0.0 0.0 selected source or drain Non-selected gate, 0.0 or negative V.sub.DD 0 selected drain or source Non-selected gate, 0.0 or negative 0.0 0.0 non-selected drain or source

(41) As shown Table 3, MRS transistors not on the same word line (i.e., non-selected gate electrodes) are provided a gate voltage of 0.0 volts or less, which results in a very low current drawn in these transistors.

(42) FIGS. **6***a*-**6***j* illustrate an exemplary fabrication process for memory array **600**, in accordance with one embodiment of the present invention. Unlike memory array **400**, the gate electrodes of the MRS transistors in memory array **600** are not connected by a network of global gate lines formed underneath the memory array. Instead, as shown in vertical section FIG. **6***a*, oxide layer **603** (e.g., silicon oxide) and bottom etch stop layer **604** (e.g., silicon nitride) are deposited in succession over a planar surface of semiconductor substrate **601**. Etch stop layer **604** may be patterned, as shown, and embedded in oxide layer **603**. Then, as shown in vertical section in FIG. **6***b*, alternating layers of silicon oxide layers **605** and silicon nitride layers **606** are deposited, numbered herein as silicon oxide layers **605-1**, . . . , and **605**-*n*, and silicon nitride layers **606-1**, . . . , **606**-*n*, respectively. An array of memory holes **607** (e.g., memory holes **607-1**, **607-2** and **607-3**) are then etched through the alternating layers of silicon oxide layers **605** and silicon nitride layers **606** down to etch stop layer **604**, as shown in vertical section in FIG. **6***c*(*i*). FIG. **6***c*(*ii*) shows in horizontal cross section through one of silicon nitride layers **606**, showing memory holes **607-1** to **607-9** of memory array **600** at this step of formation.

(43) Channel layer **609** is then conformally deposited, followed by deposition of thin gate oxide

layer **610**. Channel layer **609** may be deposited as amorphous silicon and annealed at 850° C. for 2 hours to crystallize. Alternatively, channel layer **609** may be provided by ALD SiC. Ferroelectric layer **611** (e.g., a Si-doped or Zr-doped Hf.sub.1-xSi.sub.xO.sub.y, Hf.sub.xZr.sub.1-xO.sub.y ferroelectric thin-film) is then deposited. The resulting structure (vertical section) is shown in FIG. **6***d*.

(44) An adhesion/barrier layer of titanium nitride (TiN) **612** is then conformally deposited. Memory holes **607** are then filled with gate electrode material **613**, which may be a CVD W or an n.sup.+ polysilicon. A CMP step removes excess gate oxide material **613** from the top of memory array **600**. The resulting structure (vertical section) is shown in FIG. **6***e*.

(45) Thereafter, top isolation layer **615** (e.g., silicon nitride) is provided over memory array **600**. Top isolation layer **615** is then patterned and an etch step creates slots **614** (e.g., slots **614-1**, **614-2**, **614-3** and **614-4**) through top isolation layer **615**, TiN layer **612**, ferroelectric layer **611**, gate oxide layer **610**, channel layer **609** and the alternating silicon nitride layers **606** and oxide layers **605**. The resulting structure (vertical section) is shown in FIG. **6***f*(*i*). FIG. **6***f*(*ii*) shows a horizontal cross section of memory array **600** through one of nitride layers **606**.

(46) An etch step (hot phosphoric acid) is carried out to remove the silicon nitride layers **606**. During this step, the silicon nitride material is removed from the exposed surfaces of silicon nitride layers **606** in the sidewalls of slots **614**. A further etch step removes exposed portions of channel **609** and gate oxide **610**. A layer of n.sup.+ semiconductor layer **620** (e.g., n.sup.+ polysilicon or n.sup.+ SiC) is then deposited and annealed. TiN layer **618** and tungsten **619** are then deposited successively to fill the voids left over from removing the silicon nitride. Excess n.sup.+ semiconductor, TiN and tungsten materials are removed from the top of the structure and the sidewalls of slots **614**, in substantially. These steps are provided in substantially the same manner as discussed above with respect to vertical and horizontal cross sections in FIGS. **4***i*(*i*) and **4***i*(*ii*), respectively. The pockets of n.sup.+ semiconductor layer **620** become drain and source regions of an MFIS transistor. TiN layers **618** and tungsten layers **619** become source or drain electrodes **623**. Silicon oxide **622** is then deposited to fill slots **614**. A CMP step removes excess silicon oxide from the top of memory array **600**. The resulting structure in vertical and horizontal cross sections are shown in FIGS. **6***g*(*i*) and **6***g*(*ii*), respectively,

(47) As discussed above with respect to FIGS. **4***j*(*i*) and **4***j*(*ii*), in some embodiments, silicon nitride layers **606** is not completely removed. As etching of silicon nitride layers **606** proceeds from the sidewalls of slots **614**, so that a strip of silicon nitride divides and electrically the resulting source or drain terminals isolates on opposite sides of each memory hole. In this manner, each memory hole now provides two vertical 3-D FeFET strings, as the n.sup.+ semiconductor pockets on opposite sides of each silicon nitride layer of each memory hole form separate drain or source regions. This alternative embodiment is illustrated in the structure is shown in vertical and horizontal cross sections in FIGS. **6***h*(*i*) and **6***h*(*ii*), respectively. As shown in FIG. **6***h*(*ii*), silicon nitride layers **621**, which is left over from the incomplete removal of silicon nitride layers **606** provide separate sets **623**L and **623**R of drain or source electrodes.

(48) Silicon oxide layer **618** is deposited over top isolation layer **615**, filling any gap on memory array **600** and planarized by a CMP step. Thereafter, silicon oxide layer **618** is patterned. An etch step creates via through silicon oxide layer **618** and top isolation layer **615** to expose gate electrode material **613**. Metallic conductor (e.g., TiN and tungsten plug) **616** is then provided to fill the vias. A CMP step planarizes the surface of memory array **600**. The resulting structure is shown in vertical section in FIG. **6***i*. Thereafter, top global gates (e.g., global gate **617**) are provided above silicon oxide layer **618** to electrically connect gate electrodes **613** through the conductor-filled vias, as shown in FIG. **6***j*.

(49) FIGS. **7***a*-**7***g* illustrate an exemplary fabrication process for memory array **700**, in accordance with one embodiment of the present invention. Unlike the MRS transistors of memory arrays **400** and **600** discussed above, an MFIS transistor of memory array **700** includes an additional charge-

storage layer between the gate oxide layer and the ferroelectric layer.
(50) FIG. **7***a* shows memory array **700** after (*i*) a network of global gate lines (e.g., tungsten), including global gate line **702**, are formed over semiconductor substrate **701**, which may be a semiconductor wafer, and (*ii*) oxide layer **703** (e.g., silicon oxide) and bottom etch stop layer **704** (e.g., n.sup.+ polysilicon) are deposited over the global gate lines; and (iii) alternating layers of silicon oxide layers **705** and n.sup.+ semiconductor (e.g., n.sup.+ polysilicon or n.sup.+ SiC) **706** are deposited, numbered herein as silicon oxide layers **705-1**, . . . , and **705**-*n*, and n.sup.+ polysilicon layers **706-1**, . . . , **706**-*n*, respectively. The structure of FIG. **7***a* may be formed using substantially the same steps as those described above with respect to FIGS. **4***a*-**4***c*, except conductive n.sup.+ semiconductor material replaces silicon nitride in the alternating layers. Using n.sup.+ polysilicon or n.sup.+ SiC is an option for drain and source electrodes, although n.sup.+ semiconductor materials have a higher resistivity than metal. However, if metal is selected for drain and source electrodes, a metal replacement step (see, e.g., FIGS. **4***i* and **4***j* for memory array **400** and FIGS. **6***f* and **6***g* for memory array **600**) may be required.
(51) Slots **714** may be created at this time, instead of after the MRS transistors have been substantially formed (see, e.g., FIGS. **4***h*(*i*) and **6***f*(*i*), which creating slots **414** of memory array **400** and slots **614** of memory array **600**), because the metal replacement step is not necessary. (The metal replacement steps access the silicon nitride layers through the slots.) Slots **714**, which divide memory array **700** into sections **708**, may then be filled with oxide, as shown in vertical and horizontal sections in FIGS. **7***b*(*i*) and **7***b*(*ii*).
(52) Memory holes **707** (e.g., memory holes **407-1**, **407-2** and **407-3**) are then etched through the alternating layers of silicon oxide layers **705** and n.sup.+ polysilicon layers **706** down to etch stop layer **704**, as shown in vertical section in FIG. **7***c*(*i*). FIG. **7***c*(*ii*) shows in horizontal cross section through one of n.sup.+ polysilicon layers **706**, showing memory holes **707-1** to **707-9** of memory array **700** at this step of formation.
(53) Channel layer **709** is then conformally deposited, followed by deposition of thin gate oxide layer **710**. Channel layer **709** may be deposited as amorphous silicon and annealed at 850° C. for 2 hours to crystallize. Alternatively, channel layer **709** may be provided by ALD SiC. Protective layer **708** may then be deposited over gate oxide layer **710**. A spacer etch is then carried out to remove any deposited polysilicon and gate oxide from the bottom of memory holes **707**. A CMP step may be carried out to remove materials of protective layer **708**, gate oxide **710**, and channel layer **709** from the top of the structure. The resulting structure (i.e., memory array **700** at this step of formation) is shown in vertical section in FIG. **7***d*.
(54) Protective layer **708** is then removed. Thereafter, charge-trapping layer **733** is conformally deposited. An anisotropic etch then removes the charge-trapping material at the bottom of memory holes **707** to expose the underlying etch stop layer **704**. The exposed portions of etch stop layer **704** and the portions of oxide layer **703** are removed in successive etching steps to create vias that expose the global gate lines underneath. The resulting structure is shown in vertical section in FIG. **7***e*.
(55) Ferroelectric layer **711** (e.g., a Si-doped or Zr-doped Hf.sub.1-xSi.sub.xO.sub.y, Hf.sub.1-xZr.sub.xO.sub.y ferroelectric thin-film) is then deposited. CMP and a bottom etch step removes excess ferroelectric material from the top of the structure and the bottom of memory holes **707**. An adhesion/barrier layer of titanium nitride (TiN) **712** is then conformally deposited. An etch step then removes the TiN material from the portion of memory holes **707**. Memory holes **707** are then filled with gate electrode material **713**, which may be a CVD W or an n.sup.+ polysilicon. Excess deposited material is then removed by CMP from the top of the structure. The resulting structure (vertical section) is shown in FIG. **7***f*.
(56) Thereafter, top isolation layer **715** (e.g., silicon nitride) is provided over memory array **700**. The resulting structure (vertical section) is shown in FIG. **7***g*.
(57) FIGS. **8***a*-**8***j* illustrate an exemplary fabrication process for memory array **800**, in accordance

with one embodiment of the present invention. Unlike the MRS transistors of memory arrays **400**, **600** and **700** discussed above, an MRS transistor of memory array **800** has a unit cell in which the source and drain lines are fabricated out of the same layer of semiconductor material.

(58) FIG. **8***a* shows memory array **800** after (i) a network of global gate lines (e.g., tungsten), including global gate line **802**, are formed over semiconductor substrate **801**, which may be a semiconductor wafer, and (ii) oxide layer **803** (e.g., silicon oxide) and bottom etch stop layer **804** (e.g., n.sup.+ polysilicon) are deposited over the global gate lines; and (iii) alternating layers of silicon oxide layers **805** and silicon nitride layers **806** are deposited, numbered herein as silicon oxide layers **805-1**, . . . , and **805**-*n*, and silicon nitride layers **806-1**, . . . , **806**-*n*, respectively. (In FIG. **8***a*, semiconductor substrate **801** and global gate layer **802** are omitted; semiconductor substrate **801** and global gate layer **802** have substantially the same structure, and are formed in substantially the same manner, as semiconductor substrate **701** and global gate layer **702** discussed above.) The structure of FIG. **8***a* may be formed using substantially the same steps as those described above with respect to FIGS. **4***a*-**4***c* Memory holes **807** (e.g., memory holes **407-1**, **407-2** and **407-3**) are then etched through the alternating layers of silicon oxide layers **805** and silicon nitride layers **806** down to etch stop layer **804**, as shown in vertical section in FIG. **8***b*(*i*). FIG. **8***b*(*ii*) shows in horizontal cross section through one of silicon nitride layers **706**, showing memory holes **807-1** to **807-9** of memory array **800** at this step of formation.

(59) Thereafter, a silicon nitride recess etch using, for example, hot phosphoric acid, is performed to recess silicon nitride layers **806** from exposed sidewalls of memory holes **807**, as shown in FIG. **8***c*. Channel layer **809** (e.g., p.sup.−-type polysilicon or p.sup.−-type SiC) is then deposited to fill the recesses created by the silicon nitride recess etch. An anisotropic etch step removes the excess channel material from memory holes **809**, including the sidewalls, exposing etch stop layer **804**. Excess channel material may also be removed from top oxide layer **805**-*n*. The resulting structure is shown in FIG. **8***d*(*i*). FIG. **8***d*(*ii*) shows a horizontal section through one of silicon nitride layers **806**. Channel layer **709** may be deposited as amorphous silicon or SiC and annealed to crystallize.

(60) Thin gate oxide layer **810** and ferroelectric layer **811** (e.g., a Si-doped or Zr-doped Hf.sub.1-xSi.sub.xO.sub.y, Hf.sub.1-xZr.sub.xO.sub.y ferroelectric thin-film) are then conformally deposited into memory holes **807**. A CMP step removes excess gate oxide and ferroelectric materials from the top of the structure. An adhesion/barrier layer of titanium nitride (TiN) **812** is then conformally deposited. The resulting structure is shown in FIG. **8***e*.

(61) Gate electrode material **813**, which may be a CVD W or an n.sup.+ polysilicon, is then deposited to fill the remainder of memory holes **807**. Excess deposited gate electrode and TiN materials are then removed by CMP from the top of memory array **800**. The resulting structure (vertical section) is shown in FIG. **8***f*. Thereafter, top isolation layer **815** (e.g., silicon nitride) is provided over memory array **800**. Slots **814** are then cut. The resulting structure is shown in FIG. **8***g*(*i*). A horizontal structure through one of the silicon nitride-channel layers is shown in FIG. **8***g*(*ii*).

(62) A hot phosphoric acid etch recesses silicon nitride layers **806** from the sidewalls of slots **814**, as shown in FIG. **8***h*(*i*). A horizontal structure through one of the silicon nitride-channel layers is shown in FIG. **8***g*(*ii*). Thereafter, n.sup.+ semiconductor layer (e.g., n.sup.+ polysilicon or n.sup.+ SiC) **818** is deposited by diffusion conformally to line the layers of pockets from recessing silicon nitride layers **805**. If necessary, an anneal step provides crystallization and activates the dopants. Thereafter, the remaining of the layers of pockets are lined by adhesive layer **817** (e.g., TiN) and filled by tungsten layer **819**. Excess TiN, tungsten and n.sup.+ semiconductor materials are then removed from the sidewalls and at the bottoms of slots **814** and from the top of structure. The n.sup.+ semiconductor pockets in each slot is designated to become either source regions **821** or drain regions **822**, with adjacent slots being assigned the opposite types. The resulting structure is shown in FIG. **8***i*(*i*). A horizontal structure through one of the pocket layers is shown in FIG. **8***i*(*ii*). Portion **820** of the structure of FIG. **8***i*(*i*) is enlarged in FIG. **8***i*(*iii*).

(63) Slots **814** are then filled with by insulator **825** (e.g., a silicon oxide), which also provided as a top gap fill layer. After planarization using CMP, gate line contacts **826** are through top gap fill layer **825** and top isolation layer **813**. One or more layers **827** of conductors ("gate lines") may be provided to electrically connect gate line contacts **826**. The resulting structure is shown in FIG. **8***j*.
(64) The detailed description above describes alternative embodiments in which SiC is provided in source, drain and channel regions of an FeFET. These FeFETs ("SiC FeFETs") have very low leakage currents, resulting in higher endurance than its polysilicon counterparts (e.g., 10.sup.9 or higher in SiC FeFETs, versus **105** in comparable polysilicon-based FeFETs). Also, because of the low intrinsic carrier concentration between 10.sup.−7 cm.sup.−3 (4H) and 10.sup.−5 cm.sup.−3 (6H), data retention time in SiC FeFETs is considerably higher (e.g., 10.sup.6 years). In one implementation, an SiC FeFET has data retention of 10 year operating at 150° C. In comparison, a comparable silicon channel FeFET has comparable data retention operating at a much lower operating temperature of 80° C. In fact, SiC FeFET can operate at 200° C. or higher. A SiC FeFET also has the advantage of higher switching frequencies due to its larger saturation drift velocity. For example, 4H SiC has a saturation drift velocity that is 2.7 times greater than silicon.
(65) The above detailed description is provided to illustrate specific embodiments of the present invention and is not intended to be limiting. Numerous variations and modifications within the scope of the present invention are possible. For example, with respect to FIGS. **7***a*-**7***g*, the locations of ferroelectric layer **711** and charge-trapping layer **733** can be swapped, and an additional blocking oxide layer can be inserted between titanium nitride layer **712** and ferroelectric layer **711**. The present invention is set forth in the accompanying drawings.

Claims

1. A memory string formed above a planar surface of substrate, comprising: a gate electrode extending lengthwise along a first direction substantially orthogonal to the planar surface, a ferroelectric layer provided over at least a portion of the gate electrode along a second direction orthogonal to the first direction and extending lengthwise along the first direction; a gate oxide layer provided over at least a portion of the ferroelectric layer along the second direction and extending lengthwise along the first direction; a plurality of semiconductor structure provided along the first direction adjacent the gate oxide layer, wherein each semiconductor structure comprises (*i*) a first semiconductor material of a first conductivity type; and (*ii*) second and third semiconductor materials electrically being isolated from each other and each being coplanar with and adjacent the first semiconductor material, the second and third semiconductor materials each being of a second conductivity type different from the first conductivity type, (iii) wherein at least one of the first, the second and the third semiconductor materials comprise silicon carbide (SiC), (iv) wherein the gate electrode, the ferroelectric layer, the gate oxide layer and the semiconductor structure form a storage transistor of the memory string, and (v) wherein the first, second and third semiconductor materials form the channel, source and drain regions of the storage transistor.
2. The memory string of claim 1, wherein the first semiconductor material comprises p-type atomic layer deposited silicon carbide.
3. The memory string of claim 1, wherein at least one of the second and the third semiconductor materials comprises n.sup.+-type chemical vapor deposited silicon carbide.
4. The memory string of claim 1, further comprising a barrier layer provided between the gate electrode and the ferroelectric layer.
5. The memory string of claim 4, wherein the barrier layer comprises titanium nitride, tungsten nitride or tantalum nitride.
6. The memory string of claim 1, wherein the gate electrode comprises tungsten or a heavily doped semiconductor.
7. The memory string of claim 1, further comprising a conductor adjacent to each of the second and

third semiconductor materials of each semiconductor structure.
8. The memory string of claim 7, wherein the conductor comprises tungsten, a metallic adhesive layer, or a combination thereof.
9. The memory string of claim 7, wherein the drain or source region each comprise n.sup.+ polysilicon.
10. The memory string of claim 1, wherein the memory string is one of a plurality of memory strings in a memory array, wherein the memory array comprises a staircase configuration providing electrical contacts to each of the source or drain electrodes.
11. The memory string of claim 1, wherein the memory string is one of a plurality of memory strings in a memory array, wherein the memory array comprises a network of global word line conductors each connecting the gate electrodes of a selected group of the memory strings.
12. The memory string of claim 11, wherein the network of global word line conductors is provided above the memory strings.
13. The memory string of claim 1, wherein the ferroelectric layer comprises a HfO.sub.2 ferroelectric material.
14. The memory string of claim 13, wherein the ferroelectric layer is 5.0-30.0 nm thick, preferably 8.0-20.0 nm thick.
15. The memory string of claim 13, wherein the ferroelectric layer comprises a zirconium-doped hafnium silicon oxide.
16. The memory string of claim 15, wherein the zirconium-doped hafnium silicon oxide has a zirconium content of 40-60%, preferably 45-55%.
17. The memory string of claim 15, wherein the zirconium-doped hafnium silicon oxide comprises Hf.sub.xZr.sub.1-xO.sub.y ferroelectric thin-films, where x ranges between 0.4 and 0.6, preferably between 0.45 and 0.55, and y ranges between 1.8 and 2.2, preferably between 1.9 to 2.1.
18. The memory string of claim 15, wherein the zirconium-doped hafnium silicon oxide is prepared by depositing HfO.sub.2 and ZrO.sub.2 using an ALD layer-by-layer lamination step.
19. The memory string of claim 13, wherein the ferroelectric layer comprises a silicon-doped hafnium silicon oxide.
20. The memory string of claim 19, wherein the silicon-doped hafnium silicon oxide has a silicon content of 2.0-5.0%, preferably 2.5-4.5%.
21. The memory string of claim 19, wherein the silicon-doped hafnium silicon oxide comprises Hf.sub.xSi.sub.1-xO.sub.y ferroelectric thin-films, where x ranges from 0.02 to 0.05, preferably between 0.025 and 0.04, and y ranges from 1.8 to 2.2, preferably between 1.9 and 2.1.
22. The memory string of claim 19, wherein the silicon-doped hafnium silicon oxide is prepared by depositing HfO.sub.2 and SiO.sub.2 using an ALD layer-by-layer lamination step.
23. The memory string of claim 20, further comprising a charge-trapping layer between the gate oxide layer and the ferroelectric layer or between the ferroelectric layer and a barrier layer adjacent the gate electrode.
24. The memory string of claim 1, wherein the barrier layer comprises titanium nitride.