United States Patent Application Publication	20250259827
Kind Code	A1
Publication Date	August 14, 2025
Inventor(s)	Hur; Minyoung et al.

PLASMA PROCESSING APPARATUS

Abstract

A plasma processing apparatus includes a chamber body including a chamber, an electrostatic chuck supporting a substrate within the chamber body and including a lower electrode, a high-frequency power supply device configured to supply high-frequency power to generate plasma with gas supplied to the chamber, and a bias power supply device configured to supply pulse power for ion acceleration to the lower electrode. The bias power supply device is configured to supply a positive voltage pulse having a duty ratio of (1-D) to the lower electrode when a target duty ratio D of an acceleration period for accelerating ions in the plasma during a process cycle exceeds a threshold.

Inventors: **Hur; Minyoung (Suwon-si, KR), Na; Donghyeon (Suwon-si, KR), Kim; Kyungsun (Suwon-si, KR), Kim; Namkyun (Suwon-si, KR), Kim; Sungyeol (Suwon-si, KR), Kim; Hyunbae (Suwon-si, KR), Seok; Hwasoo (Suwon-si, KR), Yoon; Kuihyun (Suwon-s, KR), Lim; Sungyong (Suwon-si, KR)**

Applicant: **SAMSUNG ELECTRONICS CO., LTD.** (Suwon-si, KR)

Family ID: **1000008107763**

Assignee: **SAMSUNG ELECTRONICS CO., LTD. (Suwon-si, KR)**

Appl. No.: **18/811382**

Filed: **August 21, 2024**

Foreign Application Priority Data

KR	10-2024-0020139	Feb. 13, 2024

Publication Classification

Int. Cl.: **H01J37/32** (20060101)

U.S. Cl.:

CPC **H01J37/32568** (20130101); **H01J37/32715** (20130101); H01J2237/04735 (20130101); H01J2237/2007 (20130101); H01J2237/334 (20130101)

Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from Korean Patent Application No. 10-2024-0020139 filed on Feb. 13, 2024, in the Korean Intellectual Property Office, the disclosure of which is incorporated by reference herein in its entirety.

BACKGROUND

[0002] The present disclosure relates to a plasma processing apparatus.

[0003] Plasma processing apparatuses are used to manufacture semiconductor devices. A plasma processing apparatus generally includes a chamber body, a stage, and a high-frequency power supply. The chamber body includes an internal space thereof as a chamber. The chamber body is grounded. The stage is provided in the chamber and is configured to support the substrate disposed thereon. The stage includes a lower electrode. The high-frequency power supply supplies high frequencies to excite gas in the chamber. In a plasma processing apparatus, ions are accelerated by a potential difference between the potential of a lower electrode and the potential of plasma, and the accelerated ions are irradiated on the substrate.

[0004] As a type of plasma processing apparatus, a plasma processing apparatus configured to supply high frequency waves for bias to a lower electrode may be used. High frequency for bias may be supplied to the lower electrode to increase the energy of ions irradiated on the substrate and increase an etching rate of the substrate.

SUMMARY

[0005] One or more example embodiments provide a plasma processing apparatus in which Unit Per Equipment Hour (UPEH) may be increased while suppressing an increase in power consumption for supplying high frequencies for bias.

[0006] One or more example embodiments provide a plasma processing apparatus in which a search range of a duty ratio of an etching period may be extended to optimize an etching period, a passivation period, and an exhaust period in a plasma process cycle.

[0007] According to an aspect of one or more example embodiments, a plasma processing apparatus includes: a chamber body including a chamber; an electrostatic chuck supporting a substrate within the chamber body and including a lower electrode; a high-frequency power supply device configured to supply high-frequency power to generate plasma with gas supplied to the chamber; and a bias power supply device configured to supply pulse power configured for ion acceleration to the lower electrode, wherein the bias power supply device is configured to apply a positive voltage pulse having a duty ratio of (1-D) to the lower electrode, where D is a real number between 0 and 1, when a target duty ratio D of an acceleration period for accelerating ions in the plasma during a process cycle is greater than a threshold.

[0008] According to a further aspect of one or more example embodiments, a plasma processing apparatus includes: a chamber body including a chamber; an electrostatic chuck supporting a substrate within the chamber body and including a lower electrode; a high-frequency power supply device configured to supply high-frequency power to generate plasma with gas supplied to the chamber; and a bias power supply device configured to supply non-sinusoidal power to the lower electrode for ion acceleration, wherein the bias power supply device is configured to control a direct current level of the non-sinusoidal power using a ratio of a first acceleration period during a

process cycle, in which ions in the plasma are accelerated to have a first energy, a ratio of a second acceleration period during which ions in the plasma are accelerated to have a second energy, and a ratio of a rest period excluding the first acceleration period and the second acceleration period.
[0009] According to a still further aspect of one or more example embodiments, a plasma processing apparatus includes: a chamber body including a chamber; an electrostatic chuck supporting a substrate within the chamber body and including a lower electrode; a high-frequency power supply device configured to supply high-frequency power to generate plasma with gas supplied to the chamber; and a bias power supply device configured to supply non-sinusoidal power to the lower electrode for ion acceleration, wherein the bias power supply device is configured to control a direct current level of the non-sinusoidal power, such that a zero voltage is applied to the lower electrode during a longest period among one or more acceleration periods for accelerating ions in the plasma and a rest period excluding the one or more acceleration periods during one process cycle.

Description

BRIEF DESCRIPTION OF DRAWINGS
[0010] The above and other aspects, features, and advantages will be more apparent from the following detailed description of one or more example embodiments, taken in conjunction with the accompanying drawings, in which:
[0011] FIG. **1** is a diagram illustrating a plasma processing apparatus according to one or more example embodiments;
[0012] FIG. **2** is a diagram illustrating substrate voltage, bias voltage, bias current, and power consumption over time in an etching process cycle, according to one or more example embodiments;
[0013] FIG. **3** is a diagram illustrating DC self-bias characteristics of plasma, according to one or more example embodiments;
[0014] FIGS. **4**A and **4**B are diagrams for comparing and illustrating substrate voltage, bias voltage, bias current, and power consumption over time in one or more example embodiments and a comparative example;
[0015] FIGS. **5**A, **5**B and **5**C are diagrams illustrating simulation results of substrate voltage and Ion Energy Distribution Function (IEDF) according to bias voltage in one cycle of an etching process, according to one or more example embodiments;
[0016] FIGS. **6**A, **6**B and **6**C are diagrams illustrating simulation results of substrate voltage and IEDF according to bias voltage in one cycle of an etching process;
[0017] FIG. **7** is a diagram illustrating a bias power circuit according to one or more example embodiments;
[0018] FIG. **8** is a diagram illustrating bias voltage according to a switching state of a bias power circuit, according to one or more example embodiments;
[0019] FIGS. **9**A and **9**B are diagrams illustrating switching state control according to bias voltage, according to one or more example embodiments;
[0020] FIG. **10** is a diagram illustrating an etching process cycle according to one or more example embodiments;
[0021] FIGS. **11**A, **11**B and **11**C are diagrams illustrating simulation results of substrate voltage and IEDF according to bias voltage in one cycle of an etching process, according to one or more example embodiments; and
[0022] FIGS. **12**A, **12**B and **12**C illustrate the bias voltage according to the duty ratio of the first acceleration period, the second acceleration period, and the rest period during the etching process cycle, according to one or more example embodiments; and

[0023] FIGS. **13**A, **13**B and **13**C illustrate the bias voltage according to the duty ratio of the first acceleration period, the second acceleration period, and the rest period during the etching process cycle.

DETAILED DESCRIPTION

[0024] According to one or more example embodiments, one or more example embodiments will be described with reference to the accompanying drawings.

[0025] FIG. **1** is a diagram illustrating a plasma processing apparatus according to one or more example embodiments.

[0026] Referring to FIG. **1**, a plasma processing apparatus **100** according to one or more example embodiments may include a chamber body **110**, a process gas supply unit **120**, a high-frequency power supply device **130**, an electrostatic chuck **140**, a lower structure **150**, and a bias power supply device **1000**. Additionally, the plasma processing apparatus **100** may further include a cooling device, an exhaust unit, a controller, and the like.

[0027] The chamber body **110** may serve as a housing forming a chamber defined by an outer wall. The chamber may be used to perform an etching process for processing a substrate W to be processed using plasma P generated by exciting the process gas supplied by the process gas supply unit **120**. The outer wall may be formed of a material with excellent wear resistance and corrosion resistance. The chamber may maintain the internal space thereof in a sealed state with a predetermined pressure and temperature during a plasma process, for example, an etching process. A pump may be disposed on the outer wall of the chamber body **110** to exhaust gas in the internal space.

[0028] The chamber body **110** may include an upper electrode **111** and an induction electrode **113**. For example, the chamber may be divided by the induction electrode **113**, and the process gas supply unit **120** may supply process gas for forming plasma P in the chamber space between the upper electrode **111** and the induction electrode **113**.

[0029] The process gas supply unit **120** may supply process gas for performing a plasma process to the chamber. For example, the process gas may include O.sub.2, Cl.sub.2, SF.sub.6, and the like.

[0030] The structure of the upper electrode **111** may not be limited to the one or more example embodiments illustrated in FIG. **1**. For example, the process gas supply unit **120** may have a structure connected to the upper electrode **111**. According to one or more example embodiments, the upper electrode **111** may be a showerhead-shaped electrode, and the process gas supplied from the process gas supply unit **120** may be injected into the chamber through the injection hole of the upper electrode **111**. Depending on one or more example embodiments, the upper electrode **111** may be disposed on an upper portion or a side portion of the chamber body **110**.

[0031] The supplied process gas may be converted into a plasma state by power supplied from the high-frequency power supply device **130**. The high-frequency power supply device **130** may be connected to the upper electrode **111** and may supply high-frequency power for plasma generation to the upper electrode **111**.

[0032] In the plasma processing apparatus **100** according to one or more example embodiments, the supplied high-frequency power may be a Radio frequency (RF) voltage, and the RF voltage may form a high-frequency electric field between the upper electrode **111** and the induction electrode **113**. A high-frequency electric field may excite the process gas supplied inside the chamber body **110** into a plasma P state.

[0033] The electrostatic chuck **140** may be disposed inside the chamber body **110** where a plasma process is performed, and the substrate W may be fixed to the upper surface of the electrostatic chuck **140** using static electricity. The electrostatic chuck **140** may include a lower electrode **112**.

[0034] A substrate W may be disposed between the induction electrode **113** and the lower electrode **112**, and a plasma process may be performed by ions included in the plasma P being accelerated and the accelerated ions being irradiated on the substrate W. For example, the lower electrode **112** may be included in the electrostatic chuck **140**. The lower electrode **112** may have a circular planar

shape to support the circular substrate W, but one or more example embodiments are not limited thereto.
[0035] The lower structure **150** may support the electrostatic chuck **140**. In one or more example embodiments, if the temperature of the substrate W increases due to heat generated during the plasma process, the lower structure **150** may further include an edge ring used to control the temperature in the edge area of the substrate W. For example, the edge ring may be arranged to surround the side of the substrate W and may be spaced apart from the side of the substrate W.
[0036] In a plasma process, the upper electrode **111** and the lower electrode **112** may generate reflected power. As the reflected power increases, the overall output for plasma formation may decrease. Therefore, an impedance matcher may minimize reflected power by matching the impedance of the circuit and the power source. For example, high-frequency power output from the high-frequency power supply device **130** may be supplied to the upper electrode **111** through an impedance matcher. FIG. **1** illustrates only the impedance matcher included in the high frequency power supply device **130**, but one or more example embodiments are not limited thereto.
[0037] The lower electrode **112** may receive non-sinusoidal power from the bias power supply device **1000**. For example, periodic negative voltage pulses may be applied to the substrate W by non-sinusoidal power supplied to the lower electrode **112**. When the plasma process is an etching process, positive ions contained in the plasma P may be accelerated during the acceleration period when the negative voltage pulse is applied during the process cycle, and the substrate W may be etched by accelerated positive ions colliding with the substrate W. During the process cycle, a passivation operation, an exhaust operation, etc. may be performed during a rest period excluding the acceleration period.
[0038] Non-sinusoidal power may have the advantage of being able to fine-tune the acceleration period of the plasma treatment process compared to sinusoidal Radio Frequency (RF) power. Although it is difficult to adjust the ratio of the acceleration period during the process cycle with sinusoidal power, the bias power supply device **1000** may adjust the ratio of the acceleration period by adjusting the duty ratio of the negative voltage pulse applied to the substrate W.
[0039] The higher the duty ratio, the longer the substrate W may be etched in one process cycle, and because the time required to etch the substrate W by the target etching amount may be shortened, Unit Per Equipment Hour (UPEH) may increase. As the maximum duty ratio increases, the search range for determining the optimal duty ratio during the etching process may become wider.
[0040] However, in order for the bias power supply device **1000** to apply a negative voltage pulse to the substrate W, if a negative voltage is uniformly supplied to the lower electrode **112** during the acceleration period and a zero voltage is supplied to the lower electrode **112** during the rest period, as the duty ratio is increased, the time for which the negative voltage is applied becomes longer, and thus the power consumption of the bias power supply device **1000** may increase.
[0041] According to one or more example embodiments, the bias power supply device **1000** uses the direct current (DC) self-bias characteristics of plasma to supply a zero voltage to the lower electrode **112** during the acceleration period and a positive voltage to the lower electrode **112** during the rest period, and may be controlled so that a negative voltage is applied to the substrate W during the acceleration period and a plasma voltage having a weak positive voltage is applied to the substrate W during the rest period.
[0042] In the case in which the target duty ratio D of the negative voltage pulse applied to the substrate W during the process cycle exceeds 0.5 (50%), the bias power supply device **1000** may apply a positive voltage pulse having a duty ratio of (1-D) to the lower electrode **112**, thereby reducing the time during which a voltage other than zero voltage is applied during the process cycle and reducing power consumption of the bias power supply device **1000** (where D is a real number between 0 and 1).
[0043] According to one or more example embodiments, the bias power supply device **1000** may

increase the maximum duty ratio while suppressing an increase in power consumption. Therefore, the UPEH of the etching process may be increased, and the search range for determining the optimal duty ratio may be expanded.

[0044] According to one or more example embodiments, with reference to FIG. **2**, the etching process cycle of a plasma processing apparatus **100** and the power consumption of the bias power supply device **1000** according to the etching period during the etching process cycle will be described in detail.

[0045] FIG. **2** is a diagram illustrating substrate voltage, bias voltage, bias current, and power consumption over time in the plasma process cycle, according to one or more example embodiments.

[0046] Referring to FIG. **2**, the substrate voltage Vwafer formed on the lower surface of the substrate over time during the plasma process is illustrated. A plurality of operations may be performed in chronological order during the process cycle PR. For example, when the plasma process is an etching process, an etching operation, a passivation operation, an exhaust operation, etc. may be performed during the process cycle PR.

[0047] During the acceleration period E, during which the etching operation is performed, a strong negative voltage of, for example, several thousand volts may need to be formed on the bottom of the substrate. When a negative voltage is formed on the bottom of the substrate, positive ions contained in the plasma formed on the upper part of the substrate are accelerated toward the substrate, and the positive ions collide with the substrate, thereby etching the substrate. During a rest period in which an etching operation is not performed, a plasma voltage having a weak positive voltage close to zero voltage may be formed on the lower surface of the substrate. During the rest period, the etching operation may be stopped, and a passivation operation, an exhaust operation, etc. may be performed.

[0048] Referring to FIG. **2**, a bias voltage Vbias that may be applied to the lower electrode **112** to control the substrate voltage Vwafer during the etching process is illustrated. The bias power supply device **1000** described with reference to FIG. **1** has a negative voltage during the acceleration period E of the etching process cycle PR, and the bias power supply device **1000** may control the substrate voltage Vwafer by applying repeated negative voltage pulses to the lower electrode **112** to have a zero voltage during the rest period.

[0049] Referring to FIG. **2**, a bias current Ibias generated in the load, while the bias power supply device **1000** applies a bias voltage Vbias to the lower electrode **112**, is illustrated. The process cycle PR may include: a voltage charging period p**1** for charging the bias voltage Vbias from zero voltage to negative voltage, a voltage maintenance period p**2** maintaining the bias voltage Vbias at a negative voltage, a voltage discharge period p**3** changing the bias voltage Vbias from negative voltage to zero voltage, and a zero voltage period p**4** during which the bias voltage Vbias is maintained at zero voltage. Peak current may occur in the load during the voltage charging period p**1** and voltage discharge period p**3**, and continuous current may occur in the load during the voltage maintenance period p**2**.

[0050] Referring to FIG. **2**, DC power Pdcps consumed by the bias power supply device **1000** to apply a bias voltage Vbias is illustrated. DC power Pdcps may be determined as a product of the bias voltage Vbias applied to the load and the bias current Ibias flowing through the load. Peak power may occur during the voltage charging period p**1**, and power may be continuously consumed during the voltage maintenance period p**2**. Additionally, power may not be consumed during the voltage discharge period p**3** and the zero voltage period p**4**.

[0051] Referring to FIG. **2**, if the bias voltage Vbias has a negative voltage during the acceleration period E and a zero voltage during the rest period, the period in which DC power Pdcps occurs may coincide with the acceleration period E. As the target etching period of the plasma etching device **100** becomes longer, the period during which DC power Pdcps is generated may become longer, and the amount of power consumed during the process cycle PR may increase.

[0052] According to one or more example embodiments, when the target duty ratio D of the substrate voltage Vwafer is 0.5 or less, the bias power supply device **1000** may apply a bias voltage Vbias having a negative voltage during the acceleration period E and a zero voltage during the rest period to the lower electrode **112**. When the target duty ratio D exceeds 0.5, the bias power supply device **1000** may apply a bias voltage Vbias having a zero voltage during the acceleration period E and a positive voltage during the rest period to the lower electrode **112**.
[0053] Due to the DC self-bias characteristics of plasma, even when the bias power supply device **1000** applies a bias voltage Vbias having a zero voltage during the acceleration period E and a positive voltage during the rest period to the lower electrode, the substrate voltage Vwafer may be controlled to have a negative voltage during the acceleration period E and to have a plasma voltage during the rest period.
[0054] According to one or more example embodiments, the bias power supply device **1000** may reduce the power consumption time to equal to or less than 0.5 times the etching process cycle PR even when the target duty ratio D exceeds 0.5. For example, the bias power supply device **1000** may increase the maximum duty ratio of the substrate voltage Vwafer while suppressing power consumption, and may increase the range of possible duty ratios.
[0055] Below, the DC self-bias characteristics of the plasma are described in detail with reference to one or more example embodiments consistent with FIG. **3**.
[0056] FIG. **3** is a diagram to explain the DC self-bias characteristics of plasma, according to one or more example embodiments.
[0057] FIG. **3** illustrates the upper electrode **111**, the lower electrode **112**, and the bias power supply device **1000** of the plasma etching device **100** as described with reference to one or more example embodiments consistent with FIG. **1**.
[0058] A bulk plasma region and a sheath region may be formed between the upper electrode **111** and the lower electrode **112**. For example, a sheath region may be formed around the bulk plasma region between the upper electrode **111** and the lower electrode **112**. The bulk plasma region may have a higher plasma density than the sheath region. In FIG. **3**, plasma P formed in the bulk plasma region is illustrated. In FIG. **3**, positive ions (+) and electrons (−) that may be included in the plasma of the sheath region between the bulk plasma region and the lower electrode **112** are illustrated.
[0059] When a periodic signal is applied to the lower electrode **112** while plasma is formed, the direct current level on the bottom of the substrate may move in the direction in which the electron flux and ion flux during one cycle of the signal coincide.
[0060] In general, the mass of a positive ion (+) may be 10,000 or more times greater than the mass of an electron (−). Therefore, the mobility of electrons (−) may be higher than that of positive ions (+). For example, when a positive voltage is applied to the lower electrode **112**, the movement speed of electrons (−) may be faster than the movement speed of positive ions (+) when a negative voltage is applied. Accordingly, the direct current level Vsb on the surface of the lower electrode **112** may move in the negative direction so that the electron flux and ion flux coincide.
[0061] FIG. **3** illustrates the direct current level of plasma depending on the position inside the chamber space, according to one or more example embodiments. The bulk plasma region may have a plasma voltage Vpp. As the plasma voltage Vpp approaches the lower electrode **112**, the direct current level of the plasma may be lowered in the sheath region between the bulk plasma region and the lower electrode **112**.
[0062] Meanwhile, the direct current level Vsb formed on the lower surface of the substrate W is determined by the amount of movement of positive ions (+) and electrons (−) in one cycle, and the direct current level Vsb is affected by the amplitude of the bias voltage Vbias applied to the lower electrode **112**, and may be determined almost independently of the direct current level. For example, changing only the DC level of the bias voltage Vbias may have little effect on the DC level Vsb formed on the lower surface of the substrate W.

[0063] According to one or more example embodiments, the bias power supply device **1000** applies a bias voltage Vbias having a zero voltage during the acceleration period E and a positive voltage during the rest period to the lower electrode. The substrate voltage Vwafer may be controlled to have a negative voltage during the acceleration period E and a plasma voltage Vpp during the rest period.

[0064] FIGS. **4**A and **4**B are diagrams for comparing and illustrating the substrate voltage, bias voltage, bias current, and power consumption over time in one or more example embodiments and a comparative example.

[0065] Referring to FIG. **4**A, the substrate voltage Vwafer to be formed on the lower surface of the substrate over time during the etching process is illustrated. Similar to that described with reference to FIG. **2**, the process cycle PR may include an acceleration period E. During the acceleration period E, during which the etching operation is performed, a strong negative voltage of, for example, several thousand volts may need to be applied to the bottom of the substrate. In the example of FIG. **4**A, the target duty ratio D of the acceleration period E during the etching process cycle PR may exceed 0.5.

[0066] Referring to FIG. **4**A, a bias voltage Vbias that may be applied to the lower electrode **112** to control the substrate voltage Vwafer in the etching process is illustrated.

[0067] According to one or more example embodiments, the bias power supply device **1000** described with reference to FIG. **1** may control the substrate voltage Vwafer by repeatedly applying a bias voltage Vbias to the lower electrode **112** to have a zero voltage during the acceleration period E of the etching process cycle PR and a positive voltage during the rest period (PR-E). For example, the bias power supply device **1000** may apply a bias voltage Vbias whose duty ratio of the positive voltage is (1-D) when the target duty ratio D of the substrate voltage Vwafer exceeds 0.5.

[0068] As described with reference to FIG. **3**, due to the DC self-bias characteristics of plasma, the substrate voltage Vwafer is almost unaffected by the DC level of the bias voltage Vbias. When the bias voltage Vbias has a positive voltage level, it may have a plasma voltage Vpp, and when it has a zero voltage level, it may have a negative voltage level. Therefore, by applying a bias voltage Vbias whose duty ratio of the positive voltage is less than 0.5, a target duty ratio D exceeding 0.5 may be provided to the substrate voltage Vwafer.

[0069] Referring to FIG. **4**A, a bias current Ibias generated in the load while the bias power supply device **1000** applies a bias voltage Vbias to the lower electrode **112** is illustrated, according to one or more example embodiments. The etching process cycle PR may include a voltage charging period p**1** for charging the bias voltage Vbias from zero voltage to negative voltage, a voltage maintenance period p**2** maintaining the bias voltage Vbias at a negative voltage, a voltage discharge period p**3** changing the bias voltage Vbias from negative voltage to zero voltage, and a zero voltage period p**4** during which the bias voltage Vbias is maintained at zero voltage.

[0070] Referring to FIG. **4**A, DC power Pdcps consumed by the bias power supply device **1000**, to apply a bias voltage Vbias, is illustrated. As described with reference to FIG. **2**, peak power may occur during the voltage charging period p**1**, and power may be continuously consumed during the voltage maintenance period p**2**. Additionally, power may not be consumed during the voltage discharge period p**3** and the zero voltage period p**4**. For example, referring to FIG. **4**A, power may be consumed at a time corresponding to a duty ratio of (1-D), which is shorter than the target duty ratio D.

[0071] Referring to FIG. **4**B, a bias voltage Vbias that may be applied to the lower electrode **112** to control the substrate voltage Vwafer according to a comparative example different from one or more example embodiments described above, is illustrated. According to a comparative example, as illustrated in FIG. **4**A, a bias voltage Vbias having a duty ratio of a negative voltage D may be applied to control the substrate voltage Vwafer, whose duty ratio D exceeds 0.5.

[0072] Referring to FIG. **4**B, as described according to one or more example embodiments with

reference to FIG. **2**, peak power may occur during the voltage charging period p**1**, and power may be continuously consumed during the voltage maintenance period p**2**. Additionally, power may not be consumed during the voltage discharge period p**3** and the zero voltage period p**4**. For example, when applying a bias voltage Vbias whose duty ratio of negative voltage is D, power may be consumed in a time corresponding to the duty ratio D. For example, the bias power supply device according to the comparative example of FIG. **4**B may consume power for a longer period of time than the bias power supply device **1000** according to one or more example embodiments described with reference to FIG. **4**A.

[0073] According to one or more example embodiments, when the target duty ratio D of the substrate voltage Vwafer exceeds 0.5, the bias power supply device **1000** may reduce power consumption by applying a voltage with a positive voltage duty ratio of (1-D).

[0074] According to one or more example embodiments, in a case of applying a negative voltage pulse having a duty ratio equal to the target duty ratio D of the substrate voltage Vwafer to the lower electrode **112**, and in a case of applying a positive voltage pulse having a duty ratio of (1-D), simulation results illustrating that the substrate voltage Vwafer has substantially the same waveform are described.

[0075] FIGS. **5**A, **5**B and **5**C are diagrams illustrating simulation results of substrate voltage and Ion Energy Distribution Function (IEDF) according to bias voltage during one cycle of the etching process.

[0076] Referring to FIG. **5**A, during the etching process cycle, an example of the bias voltage over time is illustrated when a negative bias voltage NBIAS in which a negative voltage pulse has a duty ratio of 0.3 (Dn=0.3) is applied to the lower electrode **112** and when a positive bias voltage PBIAS in which the positive voltage pulse has a duty ratio of 0.7 (Dp=0.7) is applied thereto.

[0077] The magnitude of the negative voltage pulse of the negative bias voltage NBIAS and the positive voltage pulse of the positive bias voltage PBIAS may be substantially the same. For example, a negative voltage pulse may have a potential of −6000V, and a positive voltage pulse may have a potential of +6000V. The duty ratio (Dn) of the negative voltage pulse and the duty ratio (Dp) of the positive voltage pulse may have a relationship of (Dp=1−Dn).

[0078] In the example of FIG. **5**A, because the duty ratio (Dn) of the negative voltage pulse is shorter than the duty ratio (Dp) of the positive voltage pulse, during the etching process cycle, the power consumption of the negative bias voltage NBIAS may be lower than the power consumption of the positive bias voltage PBIAS.

[0079] FIG. **5**B illustrates the substrate voltage Vwafer over time when the negative bias voltage NBIAS is applied to the lower electrode **112** during the etching process cycle and when the positive bias voltage PBIAS is applied.

[0080] When a negative bias voltage NBIAS is applied to the lower electrode **112**, the substrate voltage Vwafer may have a negative voltage pulse having the same duty ratio (D=0.3) and the same potential as the negative voltage pulse of the negative bias voltage NBIAS. When a positive bias voltage PBIAS is applied to the lower electrode **112**, due to the DC self-bias characteristics of the substrate, the DC level of the positive bias voltage PBIAS may be lowered. As a result, the substrate voltage Vwafer may have the same magnitude as the positive voltage pulse of the positive bias voltage and may have a negative voltage pulse having a duty ratio of (1−Dp).

[0081] As a result, a negative bias voltage NBIAS with negative voltage pulses having a duty ratio of Dn and a positive bias voltage PBIAS with positive voltage pulses of the same magnitude having a duty ratio of (Dp=1−Dn) are applied. According to one or more example embodiments, the duty ratio D and magnitude of the negative voltage pulses of the substrate voltage Vwafer may be substantially the same.

[0082] Referring to FIG. **5**C, the IEDF is illustrated when a negative bias voltage NBIAS is applied to the lower electrode **112** and when a positive bias voltage PBIAS is applied during the etching process cycle. When the negative bias voltage NBIAS is applied, and when the positive bias

voltage PBIAS is applied, the ion energy distribution may be almost the same. For example, in both cases, the distribution of ion energy may be formed centered around 6000 eV.

[0083] According to one or more example embodiments, when the target duty ratio D of the substrate voltage Vwafer is 0.5 or less, power consumption may be reduced by applying a voltage in which the duty ratio of the negative voltage pulse is the same voltage as the target duty ratio D to the lower electrode **112** as a bias voltage Vbias.

[0084] FIGS. **6**A, **6**B and **6**C are diagrams illustrating simulation results of substrate voltage and IEDF according to bias voltage during one cycle of the etching process, according to one or more example embodiments.

[0085] Referring to FIG. **6**A, during the etching process cycle, in the case where a negative bias voltage NBIAS in which the negative voltage pulse has a duty ratio of 0.7 (Dn=0.7) is applied to the lower electrode **112**, and in the case where a positive bias voltage PBIAS in which the positive voltage pulse has a duty ratio of 0.3 (Dp=0.3) is applied, an example of the bias voltage over time is illustrated.

[0086] The magnitudes of the negative voltage pulse of the negative bias voltage NBIAS and the positive voltage pulse of the positive bias voltage PBIAS may be substantially the same. For example, a negative voltage pulse may have a potential of −6000V, and a positive voltage pulse may have a potential of +6000V. The duty ratio (Dn) of the negative voltage pulse and the duty ratio (Dp) of the positive voltage pulse may have a relationship of (Dp=1−Dn).

[0087] In the one or more example embodiments of FIG. **6**A, because the duty ratio (Dp) of the positive voltage pulse is shorter than the duty ratio (Dn) of the negative voltage pulse, during the etching process cycle, the power consumption of the positive bias voltage PBIAS may be lower than the power consumption of the negative bias voltage NBIAS.

[0088] FIG. **6**B illustrates the substrate voltage Vwafer over time when the negative bias voltage NBIAS is applied to the lower electrode **112** during the etching process cycle and when the positive bias voltage PBIAS is applied, according to one or more example embodiments.

[0089] When a negative bias voltage NBIAS is applied to the lower electrode **112**, the substrate voltage Vwafer may have a negative voltage pulse having the same duty ratio (D=0.7) and the same potential as the negative voltage pulse of the negative bias voltage NBIAS. When the positive bias voltage PBIAS is applied to the lower electrode **112**, the direct current (DC) level of the positive bias voltage PBIAS may be lowered due to the DC self-bias characteristics of the substrate. As a result, the substrate voltage Vwafer may have a negative voltage pulse having a duty ratio of (1−Dp) and the same magnitude as the positive voltage pulse of the positive bias voltage.

[0090] As a result, even when the target duty ratio D is greater than 0.5, in the case of applying a negative bias voltage NBIAS with a negative voltage pulse having a duty ratio of Dn and a positive bias voltage PBIAS having a duty ratio of (Dp=1−Dn) and a positive voltage pulse of the same magnitude, the duty ratio D of the negative voltage pulse of the substrate voltage Vwafer may be substantially the same.

[0091] Referring to FIG. **6**C, the IEDF is illustrated when a negative bias voltage NBIAS is applied to the lower electrode **112** during the etching process cycle and when a positive bias voltage PBIAS is applied.

[0092] In the example of FIG. **6**C, the ion energy when applying the positive bias voltage PBIAS may be about 7% lower than the ion energy when applying the negative bias voltage NBIAS. This difference may be offset by increasing the size of the positive ion pulse of the positive bias voltage PBIAS by about 7%.

[0093] According to one or more example embodiments, when the target duty ratio D of the substrate voltage Vwafer is greater than 0.5, power consumption may be reduced by applying a voltage having a duty ratio (1-D) of the positive voltage pulse to the lower electrode **112** as a bias voltage Vbias.

[0094] Below, an example of the structure and operation method of the bias power supply device

1000 according to one or more example embodiments is described in detail with reference to FIGS. **7**, **8** and **9**.

[0095] FIG. **7** is a diagram illustrating a bias power circuit according to one or more example embodiments.

[0096] Referring to FIG. **7**, the bias power circuit **1000** may include a direct current power source Vdc, a first switch pair S**1**, ˜S**1**, a second switch pair S**2**, ˜S**2**, and a load L.

[0097] The load L may be connected to the first node N**1** and the second node N**2**. The first node N**1** and the second node N**2** may correspond to the first node N**1** and the second node N**2** illustrated in FIG. **1**. For example, the first node N**1** may be connected to the lower electrode **112** of FIG. **1**, and the second node N**2** may be connected to ground. A bias voltage Vbias may be applied to the load L between the first node N**1** and the second node N**2**, and a bias current Ibias may flow.

[0098] The direct current power source Vdc may apply a bias voltage Vbias between the first node N**1** and the second node N**2**. The direct current power source Vdc may be connected between the third node N**3** and the fourth node N**4**.

[0099] The first switch pair S**1**, ˜S**1** may include a first switch S**1** and a first complementary switch ˜S**1**, operating complementary. The fact that the first switch S**1** and the first complementary switch ˜S**1** operate complementary, may refer to the fact that the first complementary switch ˜S**1** is in an OFF state when the first switch S**1** is in the ON state, and the first complementary switch ˜S**1** is in the ON state when the first switch S**1** is in the OFF state.

[0100] The first switch S**1** may be connected between the third node N**3** and the first node N**1**, and the first complementary switch ˜S**1** may be connected between the first node N**1** and the fourth node N**4**. The first switch S**1** and the first complementary switch ˜S**1** operate complementary to selectively connect the first node N**1** to the third node N**3** or the fourth node N**4**.

[0101] The second switch pair S**2**, ˜S**2** may include a second switch S**2** and a second complementary switch ˜S**2** that operate complementary. The second switch S**2** may be connected between the third node N**3** and the second node N**2**, and the second complementary switch ˜S**2** may be connected between the fourth node N**4** and the second node N**2**. The second switch S**2** and the second complementary switch ˜S**2** operate complementary to selectively connect the second node N**2** to the third node N**3** and the fourth node N**4**.

[0102] The direct current power source Vdc may apply a positive voltage, a zero voltage, or a negative voltage between the first node N**1** and the second node N**2** depending on whether the first switch pair S**1**, ˜S**1** and the second switch pair S**2**, ˜S**2** are ON/OFF.

[0103] FIG. **8** is a diagram illustrating the bias voltage according to the switching state of the bias power circuit, according to one or more example embodiments.

[0104] FIG. **8** is a diagram illustrating the first node voltage Vn**1**, the second node voltage (Vn**2**), and the bias voltage Vbias according to the switching states of the first switch S**1** and the second switch S**2**.

[0105] Referring to FIG. **8**, the first switch S**1** and the second switch S**2** may have four switching states St**1**, St**2**, St**3**, and St**4**.

[0106] Referring to FIGS. **7** and **8**, in the first switching state St**1**, in which the first switch S**1** is ON and the second switch S**2** is OFF, the positive pole of the direct current power source Vdc may be connected to the first node N**1**, and the negative pole of the direct current power source Vdc may be connected to the second switch. Therefore, in the first switching state St**1**, the bias voltage Vbias may have a positive voltage of the same magnitude as the direct current power source Vdc.

[0107] In the second switching state St**2**, in which the first switch S**1** is turned ON and the second switch S**2** is turned on, the positive pole of the direct current power source Vdc may be connected to both the first node N**1** and the second node N**2**. Accordingly, the bias voltage Vbias in the second switching state St**2** may have a zero voltage.

[0108] In the third switching state St**3**, in which the first switch S**1** is OFF and the second switch S**2** is ON, the negative pole of the direct current power source Vdc may be connected to the first

node N**1**, and the positive pole of the direct current power source Vdc may be connected to the second switch. Therefore, in the third switching state St**3**, the bias voltage Vbias may have a negative voltage of the same magnitude as the direct current power source Vdc.
[0109] In the fourth switching state (St**4**), in which the first switch S**1** is turned OFF and the second switch S**2** is turned OFF, the negative pole of the direct current power source Vdc may be connected to both the first node N**1** and the second node N**2**. Accordingly, the bias voltage Vbias in the second switching state St**2** may have a zero voltage.
[0110] The bias power supply device **1000** may further include a control unit for controlling the first switch pair S**1**, ˜S**1** and the second switch pair S**2**, ˜S**2**. According to one or more example embodiments, the bias power supply device **1000** may control the first switch pair S**1**, ˜S**1** and the second switch pair S**2**, ˜S**2** to generate positive or negative voltage pulse as a bias voltage Vbias.
[0111] FIGS. **9**A and **9**B are diagrams illustrating switching state control according to bias voltage, according to one or more example embodiments.
[0112] FIG. **9**A illustrates the bias voltage Vbias over time and the states of the first switch S**1** and the second switch S**2** when the target duty ratio D of the substrate voltage Vwafer is 0.5 or less.
[0113] As described above, when the target duty ratio D of the substrate voltage Vwafer is 0.5 or less, a negative voltage pulse having a duty ratio D may be applied as the bias voltage Vbias. In one or more example embodiments, the bias power supply device **1000** maintains the first switch S**1** in the OFF state and periodically toggles the second switch S**2** such that the ON state of the second switch S**2** has a duty ratio D, thereby applying a bias voltage Vbias to the lower electrode **112**.
[0114] However, one or more example embodiments is not limited thereto, and the bias power supply device **1000** may maintain the second switch S**2** in the ON state and may periodically toggle the first switch S**1** so that the ON state of the first switch S**1** has a duty ratio (1-D), thereby applying a bias voltage Vbias to the lower electrode **112**.
[0115] FIG. **9**B illustrates the bias voltage Vbias over time and the states of the first switch S**1** and the second switch S**2** when the target duty ratio D of the substrate voltage Vwafer is greater than 0.5, according to one or more example embodiments.
[0116] As described above, when the target duty ratio D of the substrate voltage Vwafer is greater than 0.5, a positive voltage pulse having a duty ratio (1-D) may be applied as the bias voltage Vbias. In one or more example embodiments, the bias power supply device **1000** maintains the first switch S**2** in the ON state and periodically toggles the second switch S**2** so that the ON state of the second switch S**2** has a duty ratio D, thereby applying a bias voltage Vbias to the lower electrode **112**.
[0117] However, one or more example embodiments is not limited thereto, and the bias power supply device **1000** may maintain the second switch S**2** in the OFF state and may periodically toggle the first switch S**1** so that the ON state of the first switch S**1** has a duty ratio (1-D), thereby applying a bias voltage Vbias to the lower electrode **112**.
[0118] Referring to FIGS. **1**, **2**, **3**, **4**A, **4**B, **5**A, **5**B, **5**C, **6**A, **6**B, **6**C, **7**, **8**, **9**A and **9**B, one or more example embodiments are described taking as an example a case in which the substrate voltage Vwafer has two states, one negative voltage state and a positive voltage state close to zero voltage, during the etching process cycle. However, one or more example embodiments are not limited thereto. For example, during an etching process cycle, the substrate voltage Vwafer may have two or more negative voltage states.
[0119] According to one or more example embodiments, a method of operating the bias power supply device **1000** when the substrate voltage Vwafer has two or more negative voltage states will be described with reference to FIGS. **10**, **11**A, **11**B, **11**C, **12**A, **12**B, **12**C, **13**A, **13**B and **13**C.
[0120] FIG. **10** is a diagram illustrating the etching process cycle according to one or more example embodiments.
[0121] FIG. **10** illustrates the substrate voltage Vwafer over time during the etching process cycle

PR. Referring to FIG. **10**, the substrate voltage Vwafer may have two or more negative voltage states. In detail, the etching process cycle PR may include a first acceleration period, during which the substrate voltage Vwafer has a relatively large first negative voltage NH, a second acceleration period during which the substrate voltage Vwafer has a relatively small second negative voltage NL, and a rest period during which the substrate voltage Vwafer has a positive voltage close to zero voltage. FIG. **10** illustrates the proportion of the first acceleration period D**1**, the proportion of the second acceleration period D**2**, and the proportion of the rest period DO during the etching process cycle PR, according to one or more example embodiments.

[0122] During the first acceleration period, positive ions in the plasma may be accelerated to have first energy by the first negative voltage NH, and during the second acceleration period, positive ions in the plasma may be accelerated to have a second energy that is lower than the first energy by the second negative voltage NL.

[0123] For example, the plasma processing apparatus **100** as described with reference to one or more example embodiments consistent with FIG. **1** may perform a coarse etching operation by colliding cations with the first energy into the substrate at the first etching time, and then may perform a fine etching operation by colliding positive ions with relatively low second energy onto the substrate during the second etching time. Also, during the rest period, passivation operations and exhaust operations may be performed.

[0124] According to one or more example embodiments, in the bias power supply device **1000**, power consumption for forming the substrate voltage Vwafer may be reduced by controlling the direct current level of the bias voltage Vbias based on the ratio D**1** of the first etching time and the ratio D**2** of the second etching time.

[0125] FIGS. **11**A, **11**B and **11**C are diagrams illustrating simulation results of substrate voltage and IEDF according to bias voltage in one cycle of the etching process, according to one or more example embodiments.

[0126] FIG. **11**A illustrates the bias voltage level Vbias according to time of the first bias voltage BIAS**1** and the second bias voltage BIAS**2** during the etching process cycle. The first bias voltage BIAS**1** may have a relatively high negative voltage level of −6000V during the first etching period D**1**, may have a relatively low negative voltage level of −3000V during the second etching period D**2**, and may have a positive voltage level close to zero voltage during the rest period DO.

[0127] The second bias voltage BIAS**2** may have a negative voltage level of −3000V during the first etch period D**1** and a zero voltage level during the second etch period D**2**, and may have a positive voltage level of +3000V during the rest period DO. For example, the first bias voltage BIAS**1** and the second bias voltage BIAS**2** may have the same waveform and different DC levels.

[0128] FIG. **11**B illustrates the substrate voltage Vwafer over time when the first bias voltage BIAS**1** and the second bias voltage BIAS**2** are applied to the lower electrode **112** during the etching process cycle, according to one or more example embodiments. Due to the DC self-bias characteristics of the plasma described with reference to one or more example embodiments consistent with FIG. **3**, the first bias voltage BIAS**1** and the second bias voltage BIAS**2**, which have the same waveform and different DC levels, may form substantially the same substrate voltage Vwafer.

[0129] FIG. **11**C illustrates IEDF over time when the first bias voltage BIAS**1** and the second bias voltage BIAS**2** are applied to the lower electrode **112** during the etching process cycle. When the first bias voltage BIAS**1** is applied and when the second bias voltage BIAS**2** is applied, the ion energy distribution may be substantially the same. In both cases, one may have a relatively low ion energy distribution of about 3000 eV and a relatively high ion energy distribution of about 6000 eV.

[0130] According to one or more example embodiments, the bias power supply device **1000** may control the direct current level of the bias voltage Vbias to minimize power consumption due to the bias voltage Vbias for forming the substrate voltage Vwafer. In detail, the bias power supply device **1000** may control a DC level of bias voltage Vbias so that the bias voltage Vbias becomes zero

voltage during the period having the highest ratio among the first acceleration period, the second acceleration period, and the rest period.

[0131] FIGS. **12**A, **12**B and **12**C are diagrams illustrating bias voltage according to the duty ratio of the substrate voltage during one cycle of the etching process, according to one or more example embodiments.

[0132] FIGS. **12**A, **12**B and **12**C illustrate the bias voltage Vbias according to the duty ratio of the first acceleration period, the second acceleration period, and the rest period during the etching process cycle, according to one or more example embodiments.

[0133] FIG. **12**A illustrates the substrate voltage Vwafer and bias voltage Vbias when the ratio D**1** of the first acceleration period is greater than the threshold. For example, the threshold may be 0.5.

[0134] If a voltage having the same DC level as the substrate voltage Vwafer is applied as the bias voltage Vbias, power of the bias power supply device **1000** may be consumed to apply a negative voltage during the first acceleration period and the second acceleration period. When the first acceleration period is the longest, if power is consumed during the first acceleration period, the power consumption of the etching process cycle may increase.

[0135] According to one or more example embodiments, the bias power supply device **1000** may control the direct current level of the bias voltage Vbias so that a zero voltage is applied during the first acceleration period. For example, the bias voltage Vbias may have a zero voltage during the first acceleration period, may have a positive voltage PL at the first level during the second acceleration period, and may have a positive voltage PH of a second level, greater than the first level, during the rest period. The bias power supply device **1000** may consume power during the second acceleration period and the rest period, and may not consume power during the longest first acceleration period, and thus, power consumption of the etching process cycle may be reduced.

[0136] FIG. **12**B illustrates the substrate voltage Vwafer and bias voltage Vbias when the ratio D**2** of the second acceleration period is greater than the threshold, according to one or more example embodiments. For example, the threshold may be 0.5.

[0137] According to one or more example embodiments, the bias power supply device **1000** may control the direct current level of the bias voltage Vbias so that a zero voltage is applied during the second acceleration period. For example, the bias voltage Vbias may have a third level negative voltage NL during the first acceleration period and a zero voltage during the second acceleration period, and may have a first level positive voltage PL during the rest period. Because the bias power supply device **1000** may not consume power during the longest second acceleration period, the power consumption of the etching process cycle may be reduced.

[0138] FIG. **12**C illustrates the substrate voltage Vwafer and the bias voltage Vbias when the ratio D**1** of the first acceleration period and the ratio D**2** of the second acceleration period are the threshold or less. According to one or more example embodiments, a zero voltage may be applied to the bias power supply device **1000** during the rest period, and a negative voltage NH of a fourth level greater than the third level may be applied during the first acceleration period, and the DC level of the bias voltage Vbias may be controlled so that the third level of negative voltage NL is applied during the second acceleration period.

[0139] Meanwhile, referring to FIGS. **12**A, **12**B and **12**C, the bias power supply device **1000** may form at least two levels of positive voltages PH and PL, a zero voltage, and at least two levels of negative voltages NH and NL, in the load. For example, the bias power supply device **1000**, in addition to that described with reference to one or more example embodiments consistent with FIG. **7**, may further include a switch that selectively turns ON and OFF an additional load that may reduce the voltage applied to the load L. The bias power supply device **1000** may form various levels of positive and negative voltages by turning the switch ON and OFF.

[0140] However, one or more example embodiments are not limited thereto, and the bias power supply device **1000** may have the same circuit structure as described with reference to FIG. **7**, and various levels of positive and negative voltages may be formed by controlling the voltage level of

the direct current power source Vdc as well as the states of the first switch pair S**1**, ˜S**1** and the second switch pair S**2**, ˜S**2**, and positive and negative voltages of various levels may be formed by using a plurality of direct current power sources having different levels.

[0141] In one or more example embodiments, in the plasma etching device **100**, unlike what is described with reference to one or more example embodiments consistent with FIGS. **12**A, **12**B and **12**C, it may be controlled that a relatively low level of negative voltage is applied during the first acceleration period of the process cycle, a relatively high level of negative voltage is applied during the second acceleration period, and a positive voltage close to zero voltage is applied during the remaining time. According to one or more example embodiments, the bias power supply device **1000** may also control a DC level of bias voltage Vbias, such that the bias voltage Vbias becomes zero voltage during the period having the highest ratio among the first acceleration period, the second acceleration period, and the rest period.

[0142] FIGS. **13**A, **13**B and **13**C are diagrams illustrating bias voltage according to the duty ratio of the substrate voltage in one cycle of the etching process, according to one or more example embodiments.

[0143] FIGS. **13**A, **13**B and **13**C illustrate the bias voltage Vbias according to the duty ratio of the first acceleration period, the second acceleration period, and the rest period during the etching process cycle.

[0144] FIG. **13**A illustrates the substrate voltage Vwafer and bias voltage Vbias when the ratio D**2** of the second acceleration period is greater than the threshold, according to one or more example embodiments. For example, the threshold could be 0.5.

[0145] According to one or more example embodiments, the bias power supply device **1000** may control the DC level of the bias voltage Vbias, such that the bias voltage Vbias has a zero voltage during the second acceleration period, a first level positive voltage PL during the first acceleration period, and a second level positive voltage PH higher than the first level during the rest period.

[0146] FIG. **13**B illustrates the substrate voltage Vwafer and bias voltage Vbias when the ratio D**1** of the first acceleration period is greater than the threshold, according to one or more example embodiments. For example, the threshold may be 0.5.

[0147] According to one or more example embodiments, the bias power supply device **1000** may control a DC level of bias voltage Vbias, such that the bias voltage Vbias has a zero voltage during the first acceleration period, a third level of negative voltage NL during the second acceleration period, and a first level of positive voltage PL during the rest period.

[0148] FIG. **13**C illustrates the substrate voltage Vwafer and bias voltage Vbias when the ratio D**1** of the first acceleration period and the ratio D**2** of the second acceleration period are both less than the threshold, according to one or more example embodiments. For example, the threshold may be 0.5.

[0149] The bias power supply device **1000** may control a DC level of bias voltage Vbias, such that a zero voltage is applied during the rest period, a third level negative voltage NL is applied during the first acceleration period, and a fourth level negative voltage NH, greater than the third level, is applied during the second acceleration period.

[0150] According to one or more example embodiments described with reference to FIGS. **13**A, **13**B and **13**C, the bias power supply device **1000** may control the direct current level of the bias voltage Vbias so that the bias voltage Vbias has a zero voltage during the longest period of the first etching period, the second etching period, and the rest period. Power consumption may be reduced by reducing the time power is consumed during the etching process cycle.

[0151] According to one or more example embodiments, the bias power supply device **1000** may control the direct current level of the non-sinusoidal power, so that during one process cycle, a zero voltage is applied to the lower electrode during the longest period among one or more acceleration periods for accelerating ions in the plasma and a rest period excluding the one or more acceleration periods, thereby increasing the maximum duty ratio during the acceleration period while

suppressing power consumption, and extending the range of possible duty ratios.
[0152] Therefore, the bias power supply device **1000** according to one or more example embodiments may expand the scope of search to find the optimal duty ratio of the etch time to optimize the etch time, passivation time, and exhaust time of the plasma processing apparatus **100**, and may increase UPEH while suppressing power consumption.
[0153] As set forth above, in a plasma processing apparatus according to one or more example embodiments, during one cycle of a plasma processing process, the duty ratio of an etching period may be set to 0.5 or more while the duty ratio of high-frequency bias power is controlled to be 0.5 or less, and thus, UPEH may be increased while suppressing an increase in power consumption.
[0154] Because a plasma processing apparatus according to one or more example embodiments may increase the range of a duty ratio of an etching period while power consumption is suppressed, the scope of the search for optimizing an etch period may be expanded.
[0155] While one or more example embodiments have been particularly illustrated and described above, it will be apparent to those skilled in the art that modifications and variations in form and details may be made therein without departing from the spirit and scope of the appended claims.

Claims

1. A plasma processing apparatus comprising: a chamber body comprising a chamber; an electrostatic chuck supporting a substrate within the chamber body and comprising a lower electrode; a high-frequency power supply device configured to supply high-frequency power to generate plasma with gas supplied to the chamber; and a bias power supply device configured to supply pulse power configured for ion acceleration to the lower electrode, wherein the bias power supply device is configured to apply a positive voltage pulse having a duty ratio of (1-D) to the lower electrode, where D is a real number between 0 and 1, when a target duty ratio D of an acceleration period for accelerating ions in the plasma during a process cycle is greater than a threshold.
2. The plasma processing apparatus of claim 1, wherein the bias power supply device is configured to apply a negative voltage pulse having the target duty ratio D to the lower electrode when the target duty ratio D is less than or equal to the threshold.
3. The plasma processing apparatus of claim 1, wherein the bias power supply device is configured to control the positive voltage pulse to have a zero voltage during the acceleration period during the process cycle and to have a positive voltage during a rest period excluding the acceleration period, and wherein the bias power supply device is configured to control the positive voltage pulse such that a lower surface of the substrate has a negative voltage during the acceleration period and the lower surface of the substrate has a plasma voltage during the rest period, due to the positive voltage pulse and DC self-bias characteristics of the plasma.
4. The plasma processing apparatus of claim 3, wherein a magnitude of the positive voltage that the positive voltage pulse exhibits during the rest period is greater than or equal to a magnitude of the negative voltage that the lower surface of the substrate exhibits during the acceleration period.
5. The plasma processing apparatus of claim 1, wherein the threshold is 0.5.
6. The plasma processing apparatus of claim 1, wherein the bias power supply device includes: a load provided between a first node connected to the lower electrode and a second node connected to ground; a first switch pair comprising: a first switch connected between the first node and a third node; and a first complementary switch connected between the first node and a fourth node and configured to operate complementary to the first switch: a second switch pair comprising: a second switch connected between the second node and the third node; and a second complementary switch connected between the second node and the fourth node and configured to operate complementary to the second switch; and a direct current power source connected between the third node and the fourth node.

7. The plasma processing apparatus of claim 6, wherein the bias power supply device is configured to apply the positive voltage pulse having the duty ratio of (1-D) to the lower electrode by maintaining the first switch in an ON state and controlling an ON state of the second switch to have the target duty ratio D.
8. The plasma processing apparatus of claim 6, wherein the bias power supply device is configured to apply a negative voltage pulse having the target duty ratio D to the lower electrode by maintaining the first switch in an OFF state and controlling an ON state of the second switch to have a duty ratio of (1-D), when the target duty ratio D is the threshold or less.
9. The plasma processing apparatus of claim 1, wherein the plasma processing apparatus is configured to perform an etching operation of the substrate during the acceleration period, and is configured to perform a passivation operation and an exhaust operation during a rest period excluding the acceleration period during the process cycle.
10. The plasma processing apparatus of claim 1, wherein the plasma processing apparatus further includes: an upper electrode on an upper portion or a side portion of the chamber body; and an induction electrode disposed between the upper electrode and the lower electrode, and provided inside the chamber.
11. A plasma processing apparatus comprising: a chamber body comprising a chamber; an electrostatic chuck supporting a substrate within the chamber body and comprising a lower electrode; a high-frequency power supply device configured to supply high-frequency power to generate plasma with gas supplied to the chamber; and a bias power supply device configured to supply non-sinusoidal power to the lower electrode for ion acceleration, wherein the bias power supply device is configured to control a direct current level of the non-sinusoidal power using a ratio of a first acceleration period during a process cycle, in which ions in the plasma are accelerated to have a first energy, a ratio of a second acceleration period during which ions in the plasma are accelerated to have a second energy, and a ratio of a rest period excluding the first acceleration period and the second acceleration period.
12. The plasma processing apparatus of claim 11, wherein the first energy is higher than the second energy, and wherein the bias power supply device is configured to control the direct current level of the non-sinusoidal power, such that when the ratio of the first acceleration period is greater than a threshold, the non-sinusoidal power exhibits a zero voltage during the first acceleration period, exhibits a positive voltage of a first level during the second acceleration period, and exhibits a positive voltage of a second level greater than the first level during the rest period.
13. The plasma processing apparatus of claim 12, wherein the threshold is 0.5.
14. The plasma processing apparatus of claim 11, wherein the first energy is higher than the second energy, and wherein the bias power supply device is configured to control the direct current level of the non-sinusoidal power, such that when the ratio of the second acceleration period is greater than a threshold, the non-sinusoidal power exhibits a negative voltage during the first acceleration period, exhibits a zero voltage during the second acceleration period, and exhibits a positive voltage during the rest period.
15. The plasma processing apparatus of claim 11, wherein the first energy is higher than the second energy, and wherein the bias power supply device is configured to control the direct current level of the non-sinusoidal power, such that when the ratios of the first acceleration period and the ratio of the second acceleration period are less than or equal to a threshold, the non-sinusoidal power exhibits a negative voltage of a third level during the first acceleration period, exhibits a negative voltage of a fourth level smaller than the third level during the second acceleration period, and exhibits a zero voltage during the rest period.
16. The plasma processing apparatus of claim 11, wherein the first energy is lower than the second energy, and wherein the bias power supply device is configured to control the direct current level of the non-sinusoidal power, such that when the ratio of the second acceleration period is greater than a threshold, the non-sinusoidal power exhibits a positive voltage of a first level during the first

acceleration period, exhibits a zero voltage during the second acceleration period, and exhibits a positive voltage of a second level greater than the first level during the rest period.

17. The plasma processing apparatus of claim 11, wherein the first energy is lower than the second energy, and wherein the bias power supply device is configured to control the direct current level of the non-sinusoidal power, such that when the ratio of the first acceleration period is greater than a threshold, the non-sinusoidal power exhibits a zero voltage during the first acceleration period, exhibits a negative voltage during the second acceleration period, and exhibits a positive voltage during the rest period.

18. The plasma processing apparatus of claim 11, wherein the first energy is lower than the second energy, and wherein the bias power supply device is configured to control the direct current level of the non-sinusoidal power, such that when the ratio of the first acceleration period and the ratio of the second acceleration period are less than or equal to a threshold, the non-sinusoidal power exhibits a negative voltage of a fourth level during the first acceleration period, exhibits a negative voltage of a third level greater than the fourth level during the second acceleration period, and exhibits a zero voltage during the rest period.

19. The plasma processing apparatus of claim 11, wherein the bias power supply device is configured to control the direct current level of the non-sinusoidal power, such that the non-sinusoidal power exhibits a zero voltage during a period with a highest ratio among the first acceleration period, the second acceleration period, and the rest period.

20. A plasma processing apparatus comprising: a chamber body comprising a chamber; an electrostatic chuck supporting a substrate within the chamber body and comprising a lower electrode; a high-frequency power supply device configured to supply high-frequency power to generate plasma with gas supplied to the chamber; and a bias power supply device configured to supply non-sinusoidal power to the lower electrode for ion acceleration, wherein the bias power supply device is configured to control a direct current level of the non-sinusoidal power, such that a zero voltage is applied to the lower electrode during a longest period among one or more acceleration periods for accelerating ions in the plasma and a rest period excluding the one or more acceleration periods during one process cycle.