

FIG. 1A

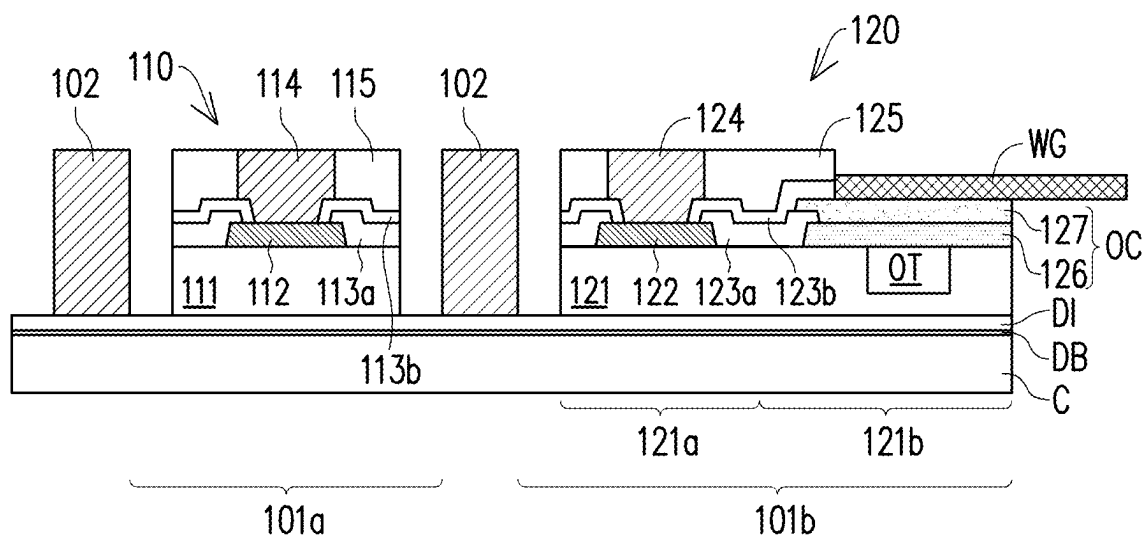


FIG. 1B

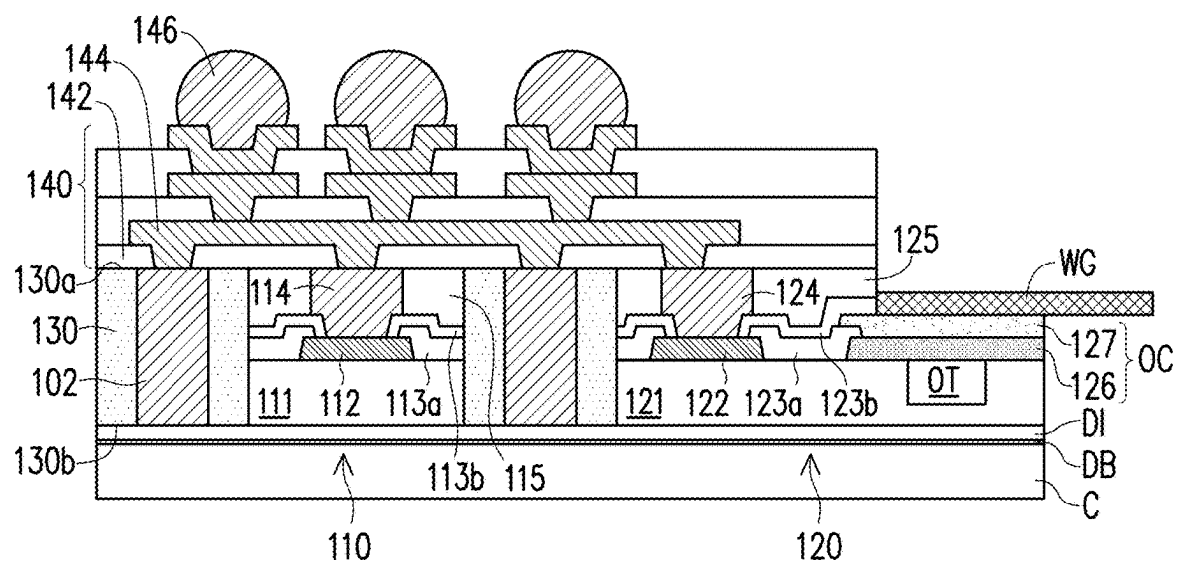


FIG. 1C

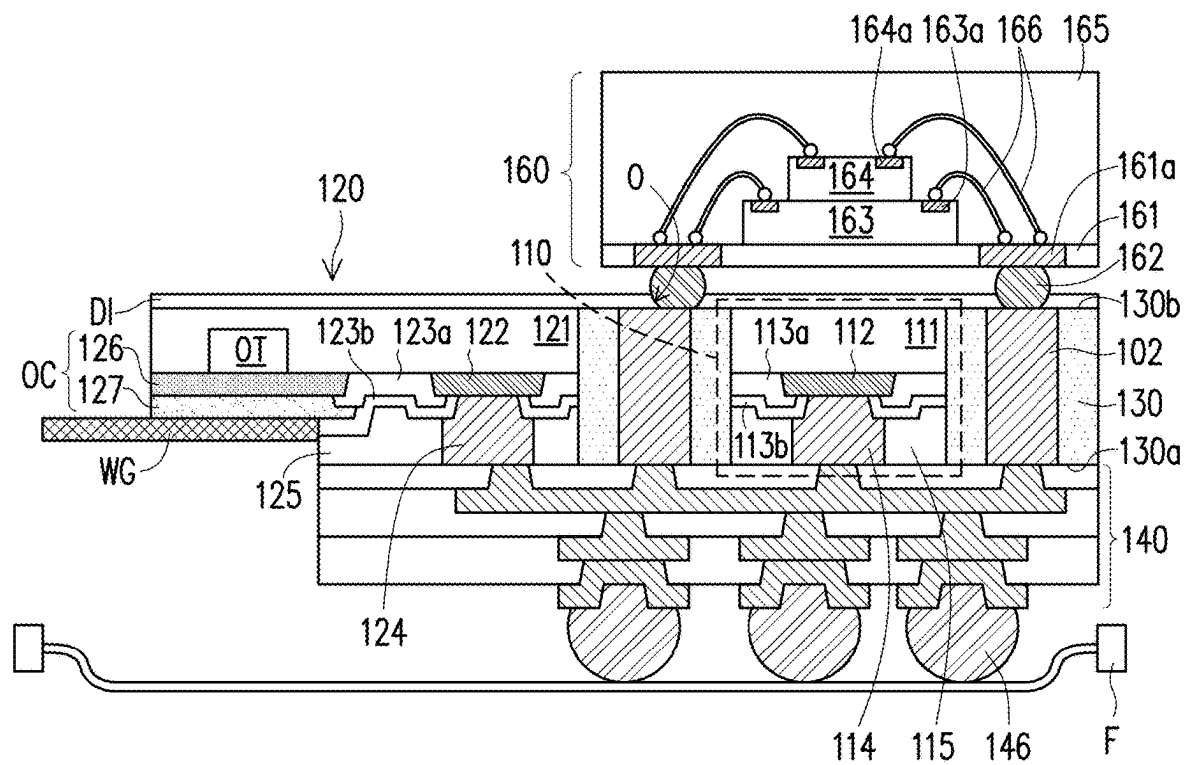


FIG. 1D

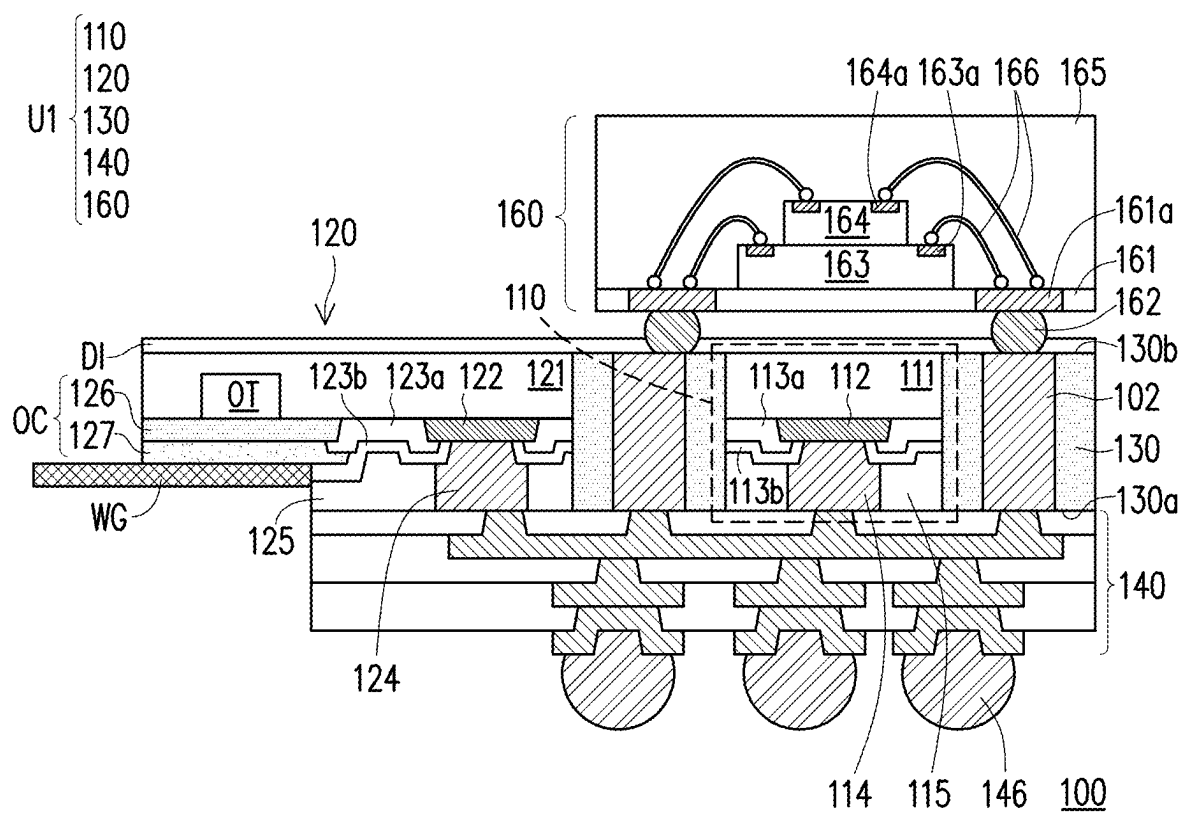


FIG. 1E

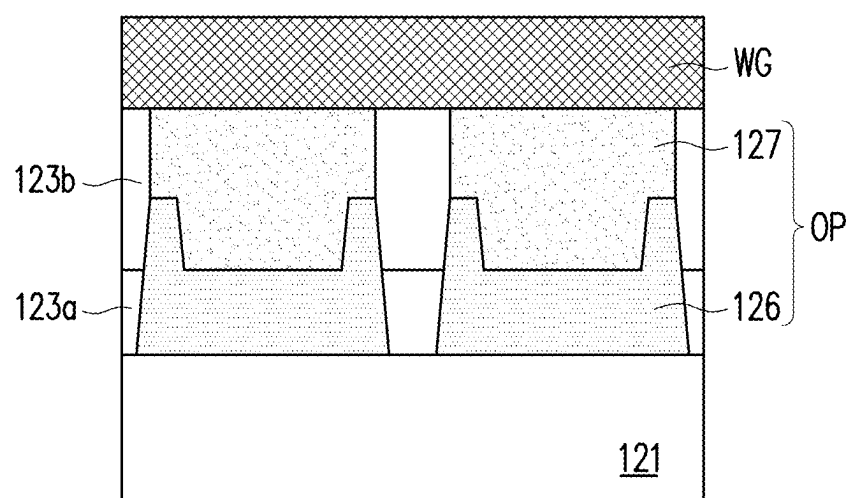


FIG. 2

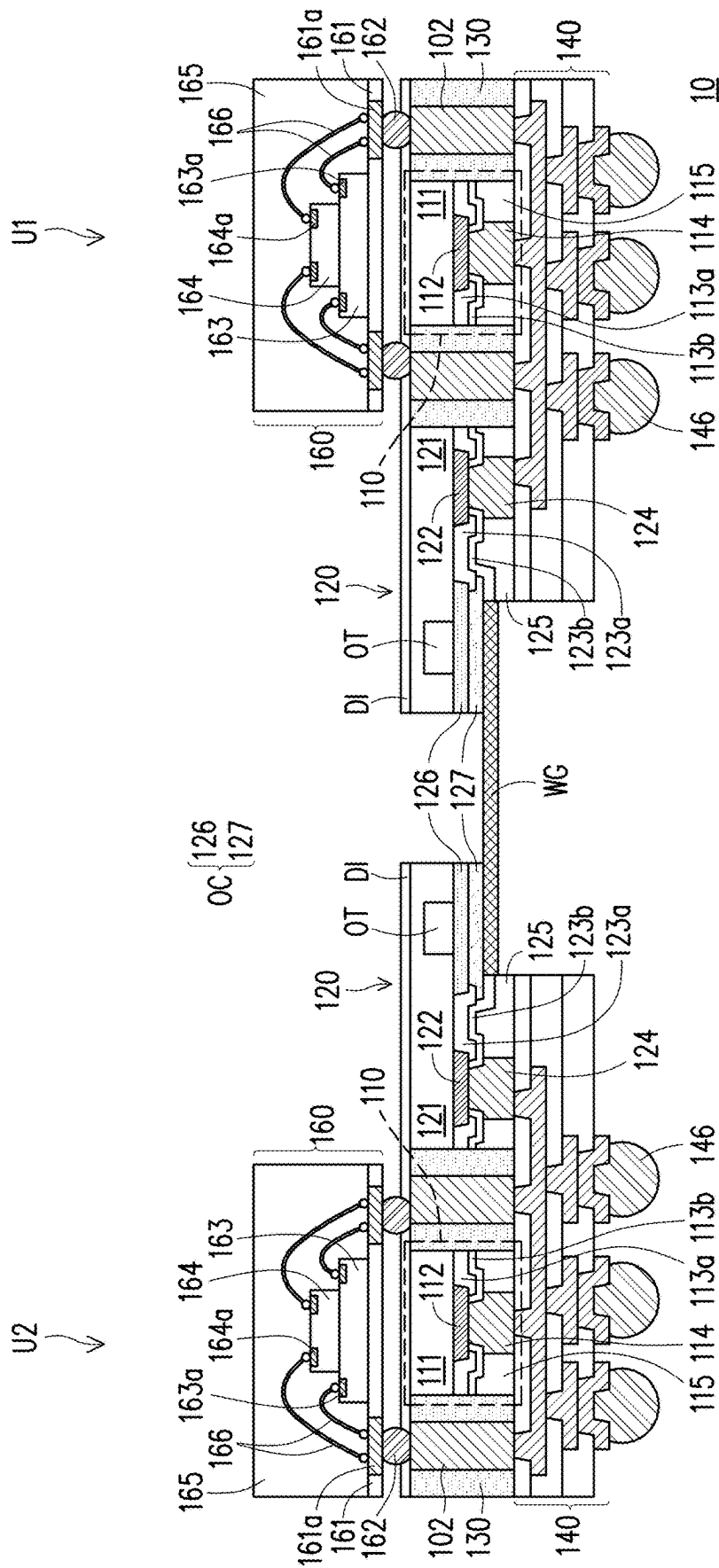


FIG. 3

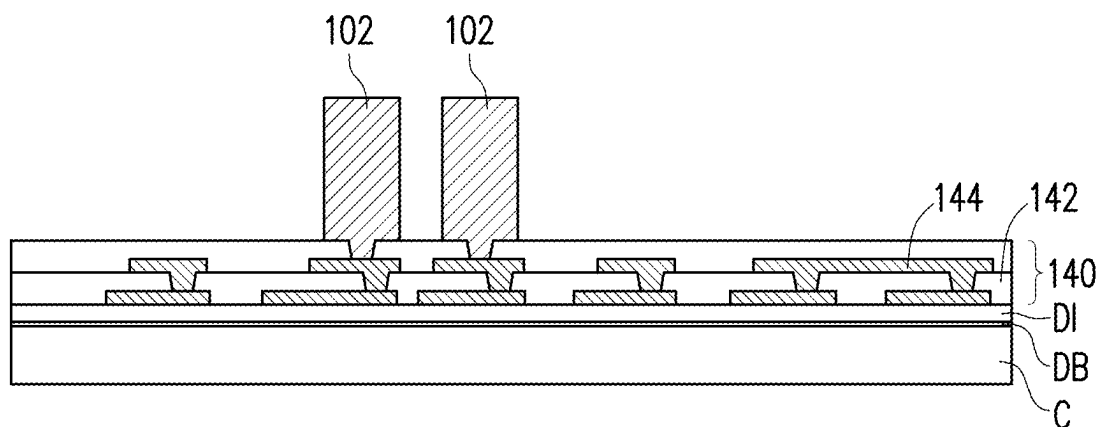


FIG. 4A

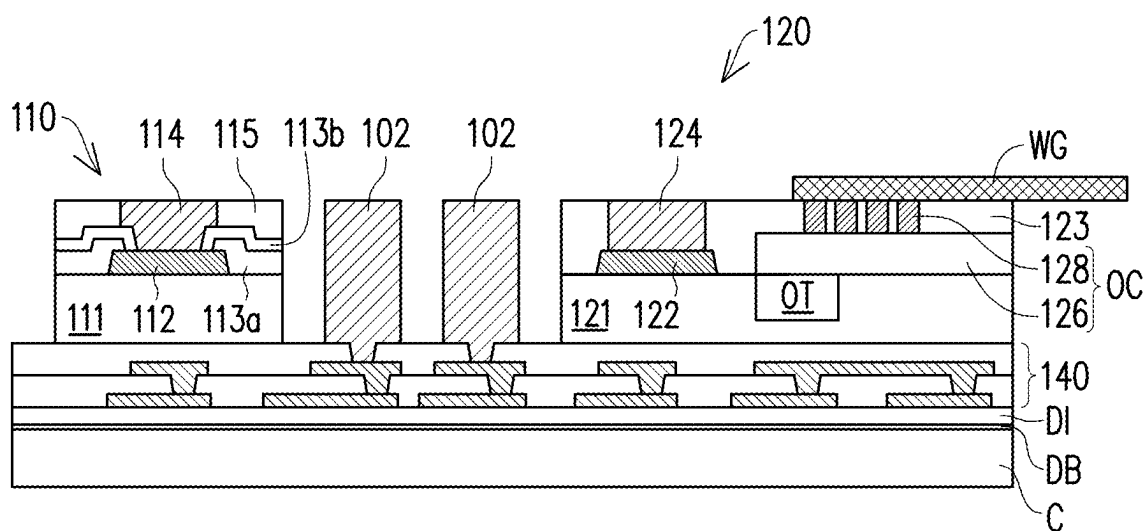


FIG. 4B

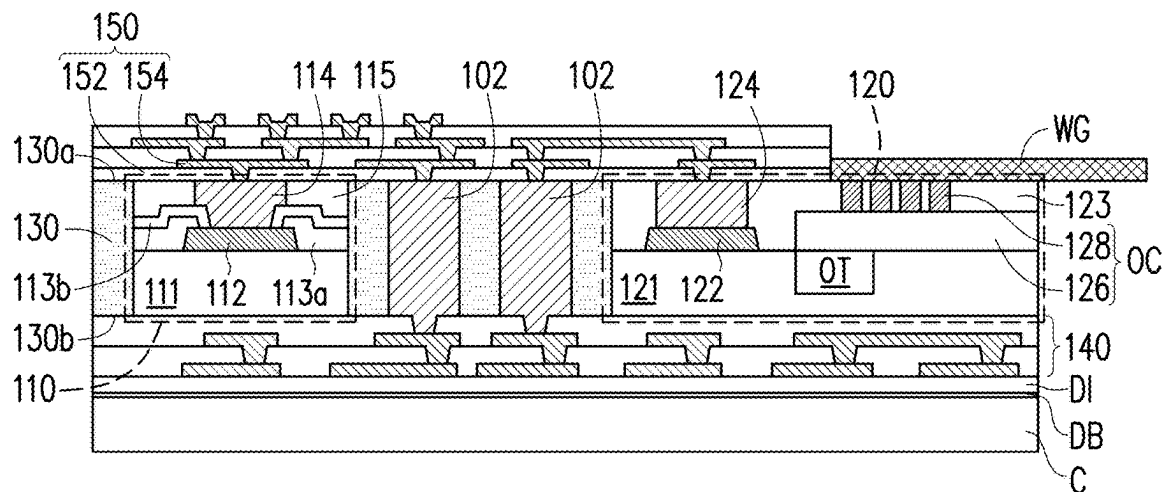


FIG. 4C

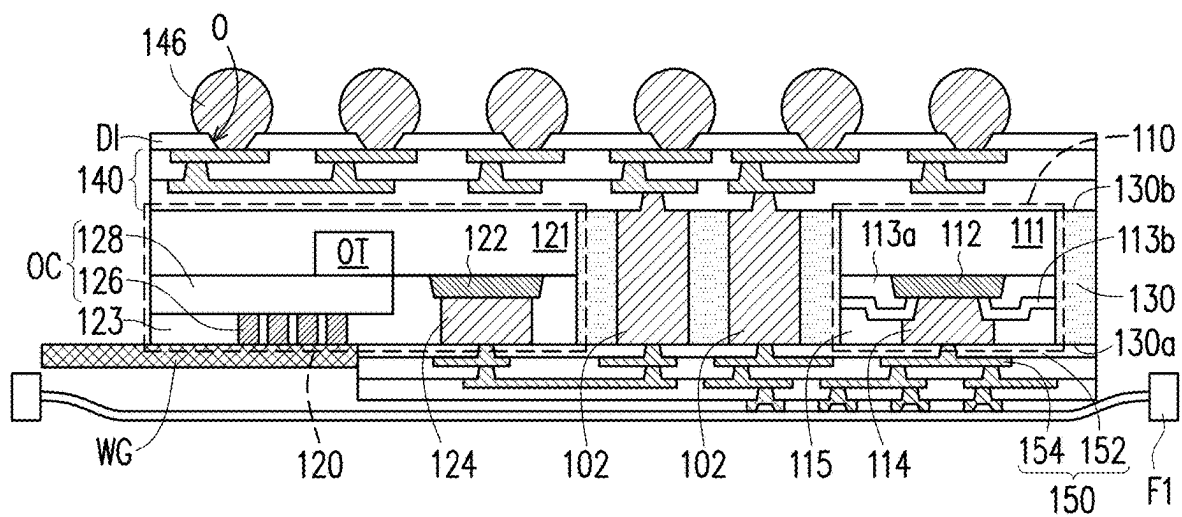


FIG. 4D



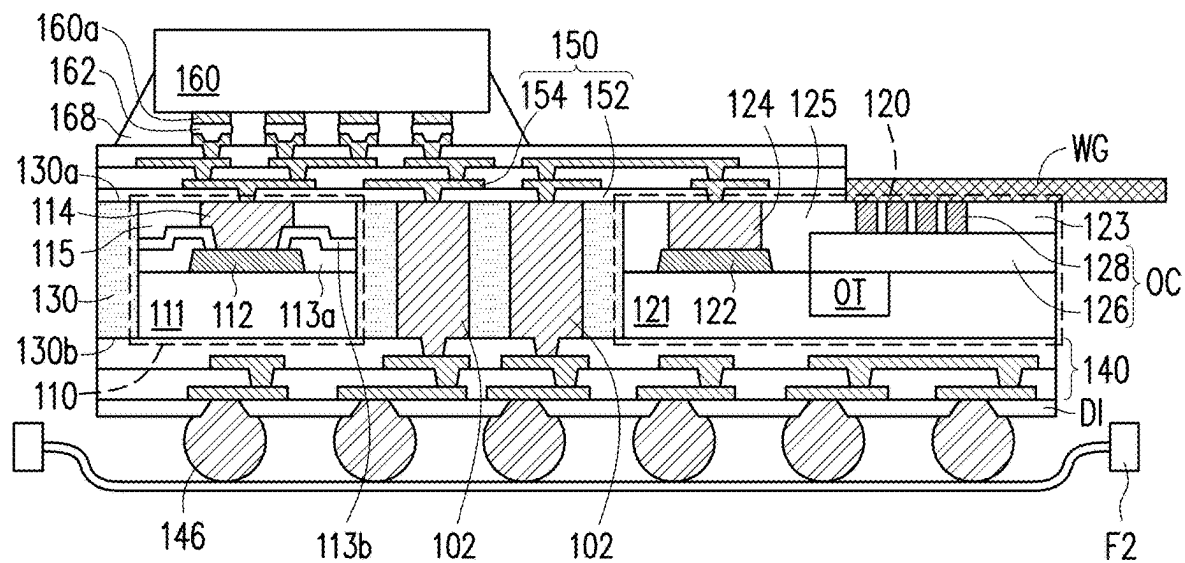


FIG. 4E

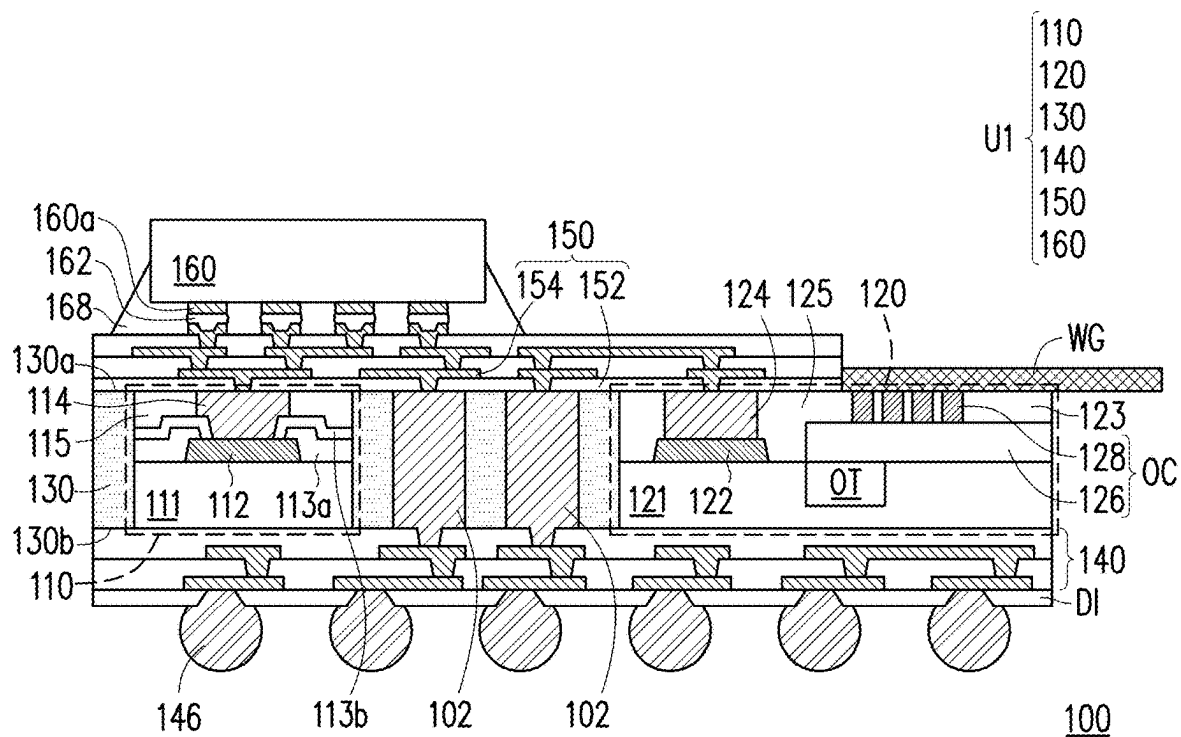


FIG. 4F

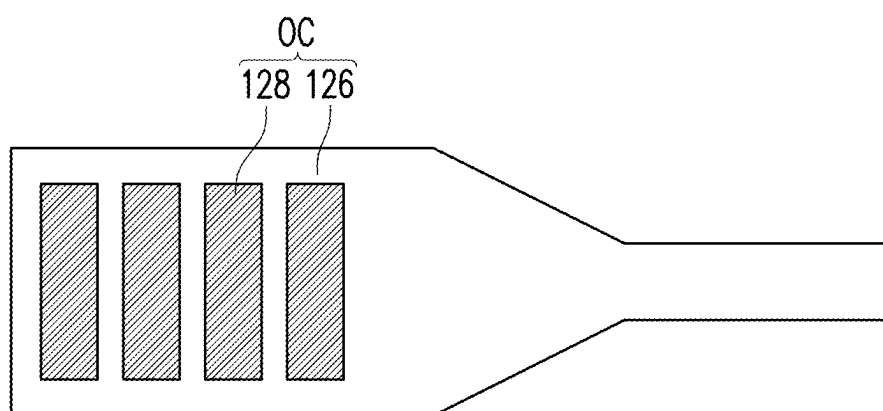


FIG. 5

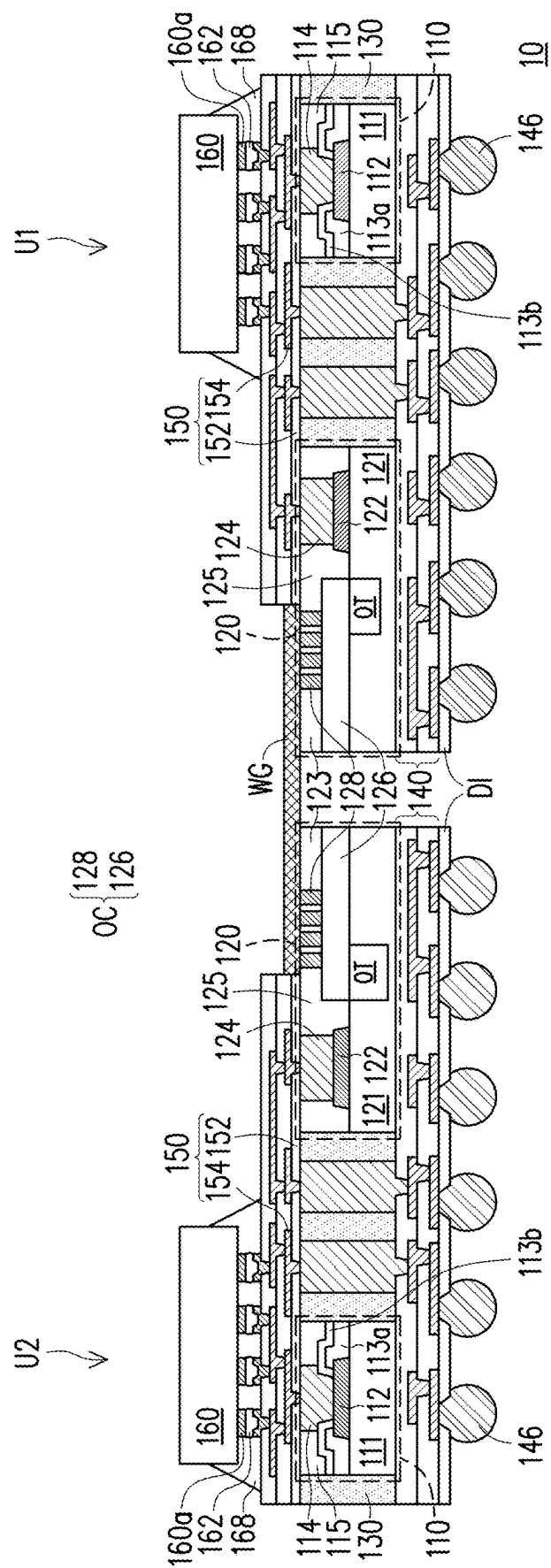


FIG. 6

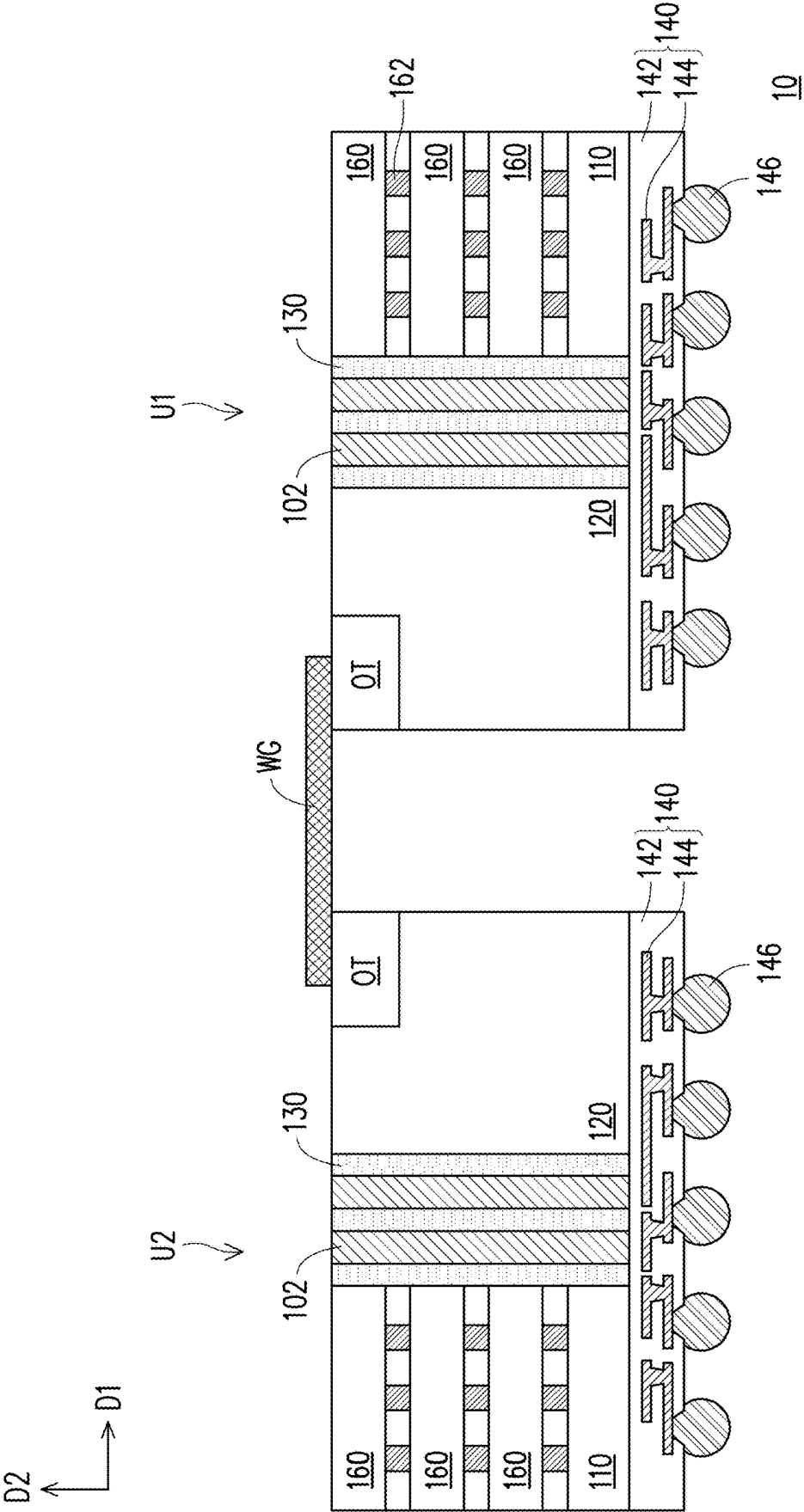


FIG. 7

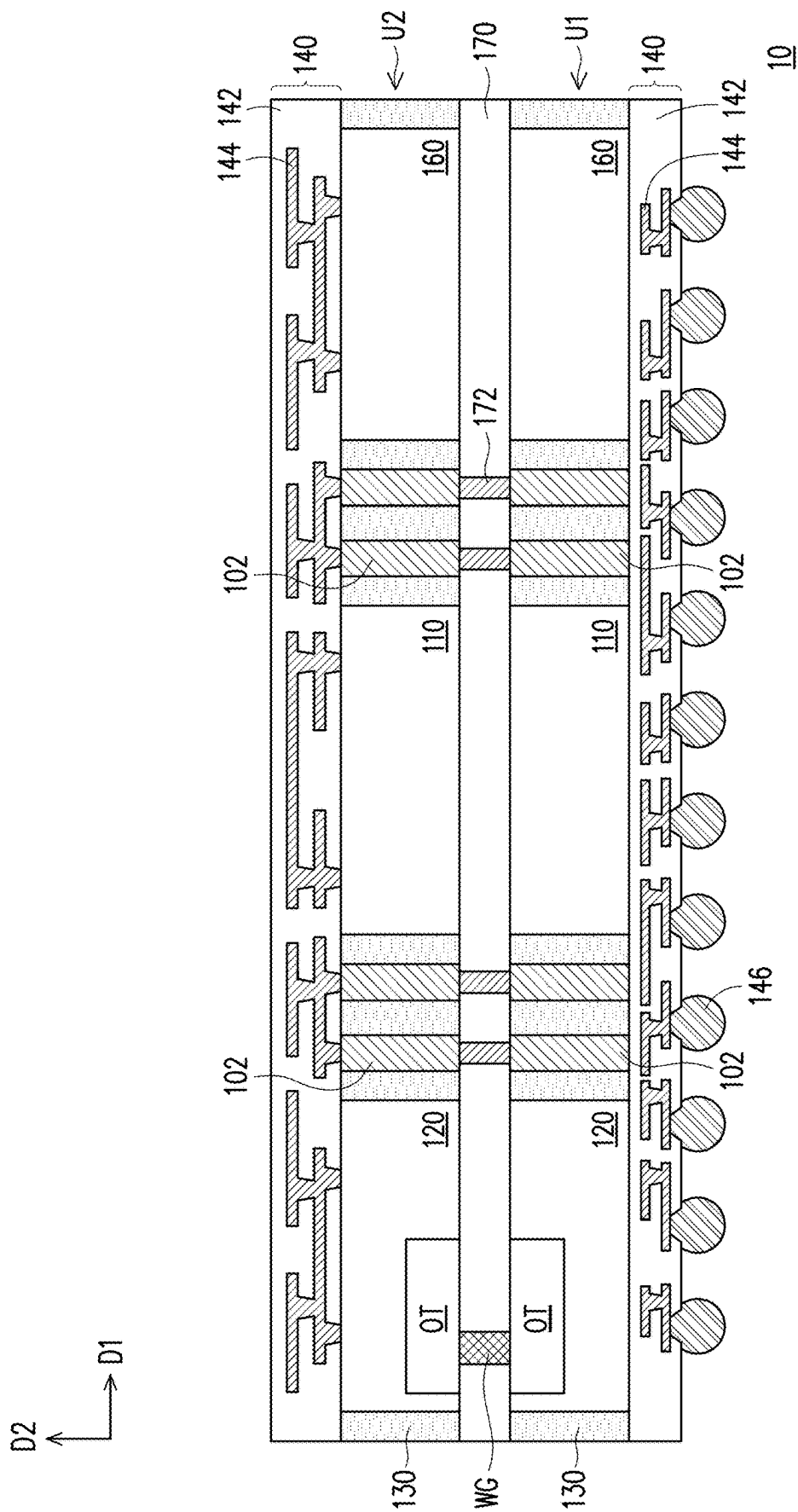


FIG. 8

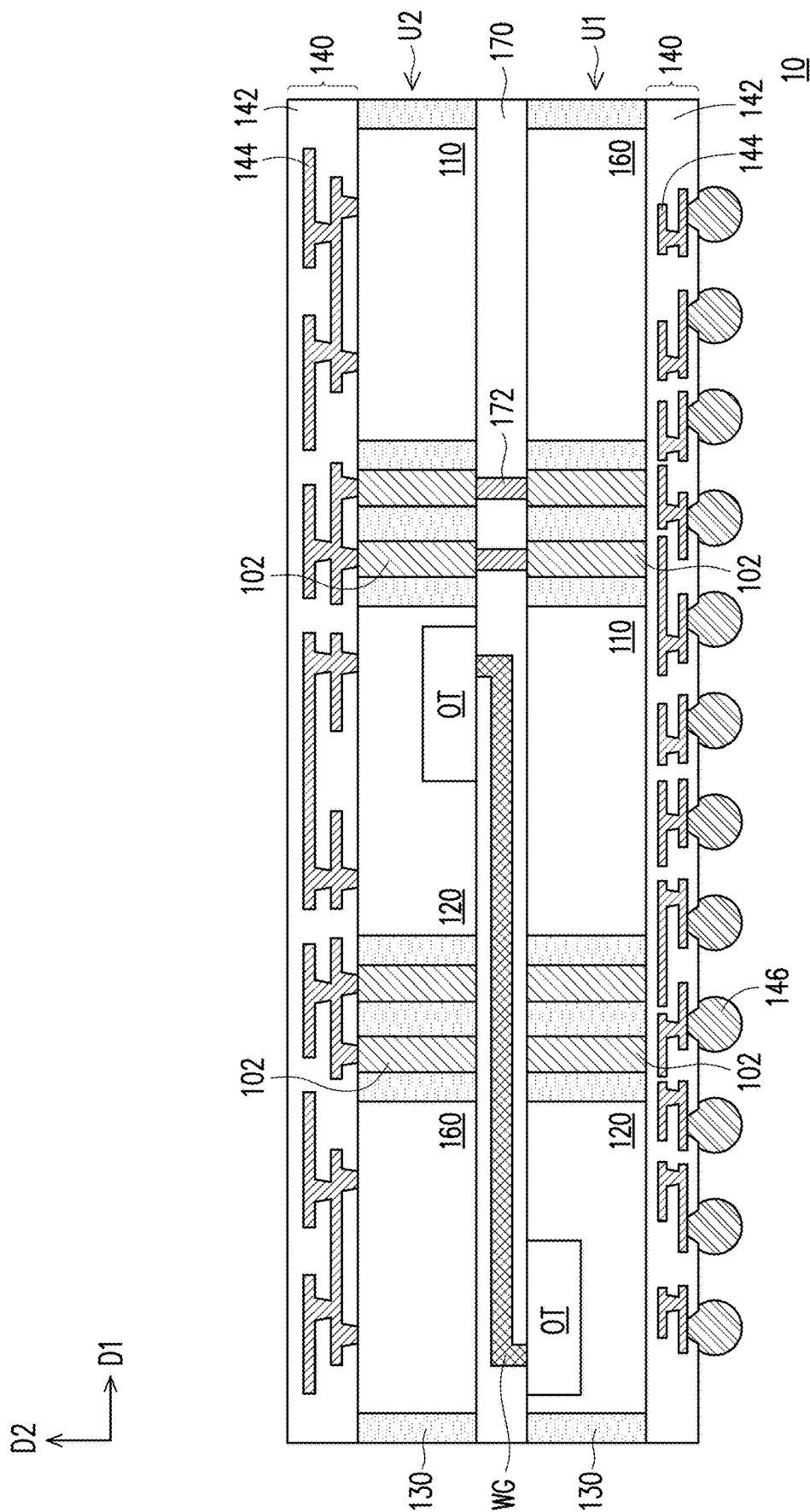


FIG. 9

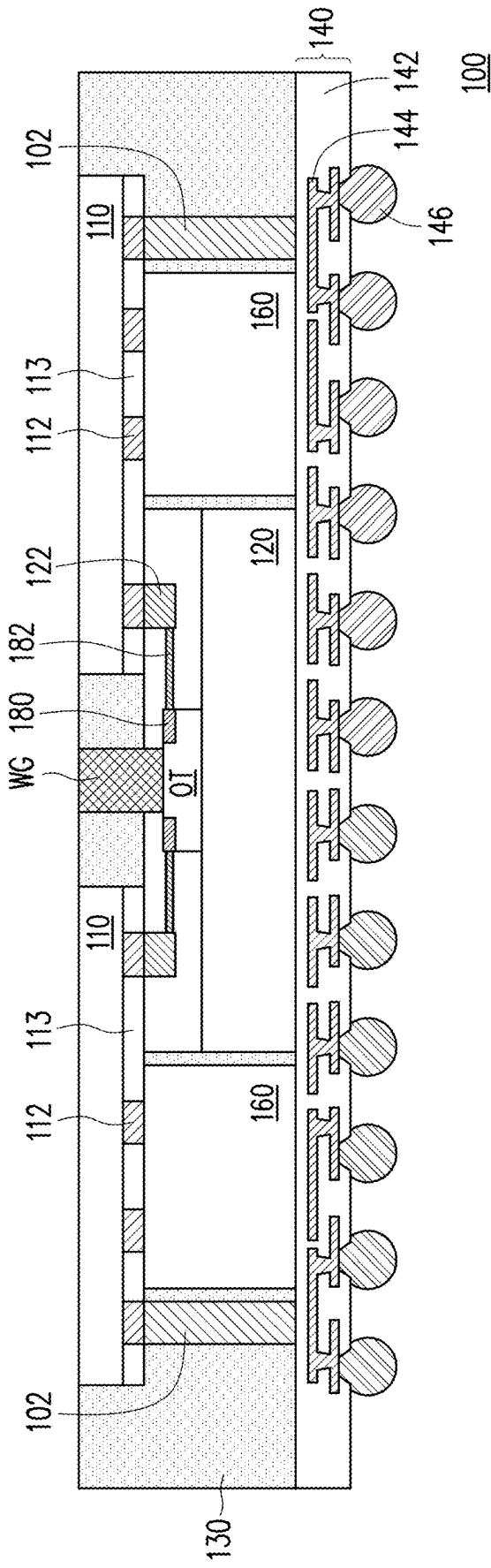


FIG. 10

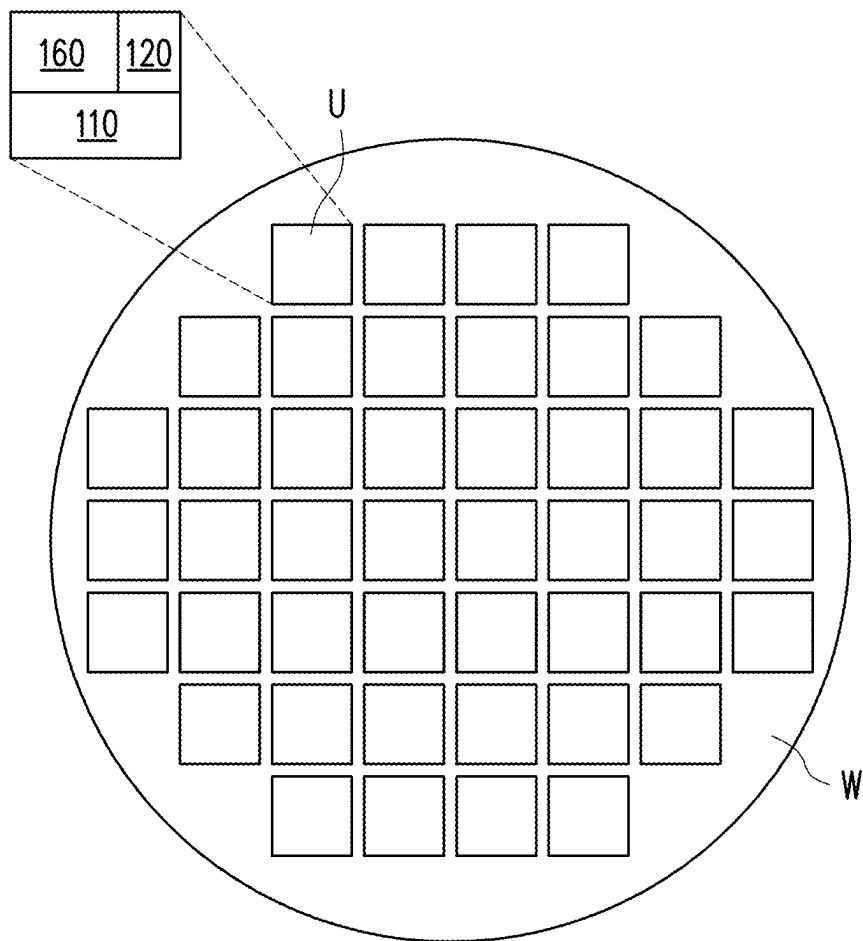


FIG. 11



## SEMICONDUCTOR PACKAGES

### CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation application of and claims the priority benefit of a prior application Ser. No. 18/315,463, filed on May 10, 2023 and now allowed, which is a continuation application of and claims the priority benefit of U.S. application Ser. No. 17/578,372, filed on Jan. 18, 2022, now issued as U.S. Pat. No. 11,688,725, which is a continuation application of and claims the priority benefit of U.S. application Ser. No. 16/866,561, filed on May 5, 2020, now issued as U.S. Pat. No. 11,233,039, which claims the priority benefit of U.S. provisional application Ser. No. 62/893,774, filed on Aug. 29, 2019. The entirety of each of the above-mentioned patent applications is hereby incorporated by reference herein and made a part of this specification.

### BACKGROUND

[0002] Optical signals are usable for high speed and secure data transmission between two devices. In some applications, a device capable of optical data transmission includes at least an integrated circuit (IC or “chip”) having a laser die for transmitting and/or receiving optical signals. Also, the device usually has one or more other optical or electrical components, a waveguide for the transmission of the optical signals, and a support, such as a substrate of a printed circuit board, on which the chip equipped with the laser die and the one or more other components are mounted. Various approaches for mounting a chip equipped with a laser die on a substrate have been studied.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0004] FIG. 1A to FIG. 1E are schematic cross-sectional views of a method of forming a semiconductor package in accordance with some embodiments.

[0005] FIG. 2 is another cross-sectional view an optical coupler of FIG. 1B.

[0006] FIG. 3 is a schematic cross-sectional view of a semiconductor package in accordance with some embodiments.

[0007] FIG. 4A to FIG. 4F are schematic cross-sectional views of a method of forming a semiconductor package in accordance with some embodiments.

[0008] FIG. 5 is a top view of an optical coupler of FIG. 4B.

[0009] FIG. 6 is a schematic cross-sectional view of a semiconductor package in accordance with some embodiments.

[0010] FIG. 7 is a schematic cross-sectional view of a semiconductor package in accordance with some embodiments.

[0011] FIG. 8 is a schematic cross-sectional view of a semiconductor package in accordance with some embodiments.

[0012] FIG. 9 is a schematic cross-sectional view of a semiconductor package in accordance with some embodiments.

[0013] FIG. 10 is a schematic cross-sectional view of a semiconductor package in accordance with some embodiments.

[0014] FIG. 11 is a schematic cross-sectional view of a semiconductor package in accordance with some embodiments.

### DETAILED DESCRIPTION

[0015] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0016] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0017] In addition, terms, such as “first,” “second,” “third,” “fourth,” and the like, may be used herein for ease of description to describe similar or different element(s) or feature(s) as illustrated in the figures, and may be used interchangeably depending on the order of the presence or the contexts of the description.

[0018] Other features and processes may also be included. For example, testing structures may be included to aid in the verification testing of the 3D packaging or 3DIC devices. The testing structures may include, for example, test pads formed in a redistribution circuit structure or on a substrate that allows the testing of the 3D packaging or 3DIC, the use of probes and/or probe cards, and the like. The verification testing may be performed on intermediate structures as well as the final structure. Additionally, the structures and methods disclosed herein may be used in conjunction with testing methodologies that incorporate intermediate verification of known good dies to increase the yield and decrease costs.

[0019] FIG. 1A to FIG. 1E are schematic cross-sectional views of a method of forming a semiconductor package in accordance with some embodiments.

[0020] Referring to FIG. 1A, a carrier C with a de-bonding layer DB coated thereon is provided. In some embodiments, the carrier C may be a glass carrier, a ceramic carrier, a metal carrier or any other carrier suitable for carrying a semicon-

ductor wafer or a reconstituted wafer for the manufacturing method of the semiconductor package. In some embodiments, the de-bonding layer DB may be any other material suitable for bonding and debonding the carrier C from the above layers or wafer disposed thereon. The de-bonding layer DB includes, for example, a light-to-heat conversion ("LTHC") layer, and such layer enables debonding from the carrier by applying laser irradiation. In some alternative embodiments, a buffer layer may be formed between the de-bonding layer DB and the carrier C. In some embodiments, a dielectric layer DI is formed over the de-bonding layer DB. In some embodiments, the dielectric layer DI is, for example, polymer such as polyimide, benzocyclobutene ("BCB"), polybenzoxazole ("PBO"), or the like. In some alternative embodiments, the dielectric layer DI may include non-organic dielectric materials such as silicon oxide, silicon nitride, silicon carbide, silicon oxynitride, or the like. However, the materials of the carrier C, the de-bonding layer DB and the dielectric layer DI are merely for illustration, and the disclosure is not limited thereto.

[0021] Then, a plurality of conductive posts 102 are provided over the dielectric layer DI. The conductive posts 102 may be copper pillars. In some embodiments, the conductive posts 102 are separated from each other, to define a first region 101a for an electrical integrated circuit and a second region 101b for a photonic integrated circuit. That is, the electrical integrated circuit and the photonic integrated circuit will be then disposed in the first region 101a and the second region 101b respectively. However, the disclosure is not limited thereto.

[0022] Referring to FIG. 1B, an electrical integrated circuit 110 and a photonic integrated circuit 120 are disposed between the conductive posts 102 over the dielectric layer DI. For example, the electrical integrated circuit 110 is picked and placed onto the dielectric layer DI in the first region 101a, and the photonic integrated circuit 120 is picked and placed onto the dielectric layer DI in the second region 101b. In some embodiments, a die attach film is located between the electrical integrated circuit 110 and the dielectric layer DI for adhering the electrical integrated circuit 110 onto the dielectric layer DI. Similarly, a die attach film is located between the photonic integrated circuit 120 and the dielectric layer DI for adhering the photonic integrated circuit 120 onto the dielectric layer DI.

[0023] In some embodiments, the electrical integrated circuit 110 includes a substrate 111, a conductive pad 112, passivation layers 113a, 113b, a conductive post 114 and a protection layer 115. The substrate 111 includes an elementary semiconductor such as silicon or germanium and/or a compound semiconductor such as silicon germanium, silicon carbide, gallium arsenic, indium arsenide, gallium nitride or indium phosphide. In some embodiments, the substrate 111 is a semiconductor-on-insulator (SOI) substrate. In some alternative embodiments, the substrate 111 may take the form of a planar substrate, a substrate with multiple fins, nanowires or any other form known to people having ordinary skill in the art. Depending on the requirements of design, the substrate 111 may be a P-type substrate or an N-type substrate and may have doped regions therein. The doped regions may be configured for an N-type device or a P-type device.

[0024] The electrical integrated circuit 110 may include a device layer formed in or on the substrate 111. In some embodiments, the device layer may include transistors,

resistors, capacitors, inductors, and/or the like. The conductive pad 112 may be formed on and electrically connected to the device layer and may be a pad of an interconnect structure. The conductive pad 112 is an aluminum contact pad, for example. The passivation layers 113a, 113b may be sequentially formed on the substrate 111 and expose a portion of the conductive pad 112. In some embodiments, a material of the passivation layer 113a is different from a material of the passivation layer 113b. A material of the passivation layer 113a, 113b may include silicon oxide, silicon oxynitride, silicon nitride, BCB, PBO, polyimide or a combination thereof. The conductive post 114 is disposed on and electrically connected to the conductive pad 112. The conductive post 114 is a copper pillar or copper alloy pillar, for example. The protection layer 115 covers the conductive post 114 and the passivation layers 113a, 113b. In some alternative embodiments, before placing the electrical integrated circuit 110 over the carrier C, the conductive post 114 is uncovered (i.e., bare dies not molded or encapsulated). A material of the protection layer 115 may include silicon oxide, silicon nitride, silicon oxynitride, a low-k material, a photo-sensitive material such as a siloxane based inorganic-organic hybrid material, polyimide, a combination thereof, or the like.

[0025] In some embodiments, the photonic integrated circuit 120 includes a substrate 121, the optical coupler OC and an optical transceiver OT. The substrate 121 may be divided into two regions: an electro-interconnection region 121a and an optical region 121b. The substrate 121 includes silicon, silicon oxide, aluminum oxide, sapphire, germanium, silicon germanium, gallium arsenic, gallium nitride, indium arsenide, indium phosphide or any other suitable material. In some embodiments, the substrate 121 may include an epitaxial layer. For example, the substrate 121 has an epitaxial layer overlying a bulk semiconductor. Further, the substrate 121 may be strained for performance enhancement. The epitaxial layer may include a semiconductor material different from those of the bulk semiconductor such as a layer of silicon germanium overlying bulk silicon or a layer of silicon overlying a bulk silicon germanium formed by a process including selective epitaxial growth (SEG). Furthermore, the substrate 121 may include a semiconductor-on-insulator (SOI) structure such as a buried dielectric layer. In one embodiment, the substrate 121 includes silicon with (100) crystal orientation. The electro-connection region 121a includes a plurality of patterned dielectric layers and patterned conductive layers that provide interconnections (e.g., wiring) between the various components, circuitry, and input/output of an IC device. For example, the electro-interconnection region 121a includes a conductive pad 122 on the substrate 121, passivation layers 123a, 123b partially covering the substrate 121, a conductive post 124 and a protection layer 125. The conductive pad 122, the passivation layers 123a, 123b, the conductive post 124 and the protection layer 125 may be similar to the conductive pad 112, the passivation layers 113a, 113b, the conductive post 114 and the protection layer 115 respectively. In some embodiments, the optical transceiver OT is disposed in the optical region 121b. The optical transceiver OT is embedded in the substrate 121, for example. The optical transceiver OT includes an optical receiver such as a photodiode and an optical transmitter such as a laser diode.

[0026] FIG. 1B is a schematic cross-sectional view along a first line, and FIG. 2 is another cross-sectional view along

a second line which is substantially perpendicular to the first line. Referring to FIGS. 1B and 2, in some embodiments, the optical coupler OC is disposed in the optical region 121*b*. In some embodiments, the optical coupler OC includes a plurality of waveguides 126, 127. The waveguide 126 may be a silicon waveguide, and the waveguide 127 may be a polymer waveguide. The waveguide 126 is formed over the substrate 121. In some embodiments, a material of the waveguide 126 is silicon, silicon oxynitride, polyimide or any other suitable material. A material of the waveguide 127 is different from the material of the waveguide 126, and a material of the waveguide 127 is a polymer material such as a photo-sensitive polymer. The photo-sensitive polymer may be a negative photo-sensitive polymer or a positive photo-sensitive polymer. In some embodiments, the waveguide 126 is disposed adjacent to an edge of the substrate 121, for example. The waveguide 127 is disposed on the waveguide 126 and the passivation layer 123*a*, for example. As shown in FIG. 2, in some embodiments, the waveguide 127 is partially disposed in the waveguide 126 and partially covered by the passivation layer 123*b*, for example. In some embodiments, the waveguide 127 may be also referred to as a core layer.

[0027] Then, a waveguide WG is formed over the photonic integrated circuit 120 to optically couple with the optical coupler OC. In some embodiments, the waveguide WG is formed at an edge of the photonic integrated circuit 120. The waveguide WG is disposed on and in direct and physical contact with the waveguide 127, for example. In some embodiments, the waveguide WG is an optical fiber. In some embodiments, the waveguide WG is extended beyond the optical coupler OC and protruded from the edge of the photonic integrated circuit 120. In some embodiments, edges of the waveguide 126, the waveguide 127 and the substrate 121 are substantially aligned with one another, and the waveguide WG is extended beyond the edges of the waveguide 126, the waveguide 127 and the substrate 121. In some embodiments, the protection layer 125 may be also referred to as a cladding layer. In some embodiments, the waveguide WG is entirely exposed. In some embodiments, an outer sidewall of the protection layer 125 is substantially perpendicular to a surface of the substrate 121. However, the disclosure is not limited thereto. In some alternative embodiments, the outer sidewall of the protection layer 125 is inclined with respect to a surface of the substrate 121.

[0028] Referring to FIG. 1C, an encapsulant 130 is formed over the carrier C to encapsulate the electrical integrated circuit 110, the photonic integrated circuit 120 and the conductive posts 102. In some embodiments, the encapsulant 130 fills between or surrounds the electrical integrated circuit 110, the photonic integrated circuit 120 and the conductive posts 102. In some embodiments, a first surface 130*a* (i.e., top surface) of the encapsulant 130 is substantially coplanar with top surfaces of the electrical integrated circuit 110, the photonic integrated circuit 120 and the conductive posts 102. In some embodiments, the first surface 130*a* of the encapsulant 130 is substantially flush with top surfaces of the conductive post 114 and the protection layer 115 of the electrical integrated circuit 110, the conductive post 124 and the protection layer 125 of the photonic integrated circuit 120 and the conductive posts 102. The encapsulant 130 is formed by a molding process and a planarization process, for example. In some embodiments, as shown in FIG. 1B, the top surfaces of the electrical

integrated circuit 110, the photonic integrated circuit 120 and the conductive posts 102 are illustrated as being substantially coplanar with each other before forming the encapsulant 130. However, the disclosure is not limited thereto. In some alternative embodiments, the top surfaces of the electrical integrated circuit 110, the photonic integrated circuit 120 and the conductive posts 102 may be not flush with each other before performing the planarization process. That is, the planarization process may remove portions of the conductive post 114, the protection layer 115, the conductive post 124, the protection layer 125 and/or the conductive posts 102.

[0029] Then, a redistribution layer structure 140 is formed over the first surface 130*a* of the encapsulant 130 to electrically connect to the electrical integrated circuit 110, the photonic integrated circuit 120 and the conductive posts 102. As shown in FIG. 1C, the waveguide WG is exposed without being covered by the redistribution layer structure 140. In some embodiments, the redistribution layer structure 140 includes a plurality of dielectric layers 142 and a plurality of conductive patterns 144 in the dielectric layers 142. The conductive patterns 144 are electrically connected to each other. The conductive patterns 144 includes conductive lines, conductive vias or the like. In some embodiments, a material of the conductive patterns 144 includes aluminum, titanium, copper, nickel, tungsten, silver and/or alloys thereof. In some embodiments, a material of the dielectric layers 142 includes silicon oxide, silicon oxynitride, silicon nitride, BCB, PBO, polyimide or a combination thereof. In some embodiments, the bottommost conductive patterns 144 of the redistribution layer structure 140 are electrically connected to the conductive post 114 of the electrical integrated circuit 110, the conductive post 124 of the photonic integrated circuit 120 and the conductive posts 102 respectively. However, the disclosure is not limited thereto.

[0030] After that, a plurality of conductive terminals 146 are formed over and electrically connected to the redistribution layer structure 140. In some embodiments, the conductive terminals 146 are electrically connected to the electrical integrated circuit 110, the photonic integrated circuit 120 and the conductive posts 102 through the redistribution layer structure 140. In some embodiments, the conductive terminals 146 are, for example, solder balls or ball grid array ("BGA") balls. In some embodiments, the conductive terminals 146 may be placed on the conductive patterns 144 (e.g., under-ball metallurgy patterns) through a ball placement process or any other suitable process.

[0031] Referring to FIG. 1D, the dielectric layer DI is de-bonded from the de-bonding layer DB such that the structure of FIG. 1C is separated from the carrier C. That is, the carrier C is removed. In some embodiments, the de-bonding layer DB (e.g., the LTHC release layer) may be irradiated by an UV laser such that the dielectric layer DI adhered on a second surface 130*b* (i.e., bottom surface) of the encapsulant 130 is peeled from the carrier C. Then, the formed structure is turned upside down and disposed on a frame F. As illustrated in FIG. 1D, the dielectric layer DI is then patterned such that a plurality of contact openings O are formed to partially expose the conductive posts 102. The number of the contact openings O corresponds to the number of the conductive posts 102. In some embodiments, the contact openings O of the dielectric layer DI are formed by a laser drilling process, a mechanical drilling process or any other suitable process.

[0032] Then, a memory 160 is disposed on and electrically connected to the conductive posts 102. In some embodiments, the memory 160 is disposed over the second surface 130b of the encapsulant 130. In some embodiments, the memory 160 is electrically connected to the conductive posts 102 through a plurality of conductive terminals 162 such as micro-bumps therebeneath. In some embodiments, the memory 160 includes a substrate 161, a first die 163 on the substrate 161, a second die 164 stacked on the first die 163 and an encapsulant 165 encapsulating the first die 163 and the second die 164. The substrate 161, the first die 163 and the second die 164 respectively have a plurality of conductive pads 161a, 163a, 164a, for example. The conductive terminals 162 are electrically connected to the conductive pads 161a. In some embodiments, the memory 160 further includes a plurality of conductive wires 166 encapsulated by the encapsulant 165. The conductive wires 166 are formed between the conductive pads 161a of the substrate 161 and the conductive pads 163a of the first die 163, to electrically connect the substrate 161 and the first die 163. Similarly, the conductive wires 166 are formed between the conductive pads 161a of the substrate 161 and the conductive pads 164a of the second die 164, to electrically connect the substrate 161 and the second die 164.

[0033] Referring to FIG. 1E, the structure in FIG. 1D is de-bonded from the frame F, and a semiconductor package 100 is formed. In some embodiments, the semiconductor package 100 includes a unit U1 and the waveguide WG optically coupled to the unit U1. In some embodiments, the unit U1 includes the electrical integrated circuit 110, the photonic integrated circuit 120 and the memory 160. In some embodiments, as shown in FIG. 3, the unit U1 of the FIG. 1E may be connected to another unit U2 by the waveguide WG therebetween, so as to form a semiconductor package 10. In some embodiments, the unit U2 has a configuration similar to the unit U1. However, the disclosure is not limited thereto. In some alternative embodiments, the units U1, U2 may have different configuration.

[0034] FIG. 4A to FIG. 4F are schematic cross-sectional views of a method of forming a semiconductor package in accordance with some embodiments. Referring to FIG. 4A, a redistribution layer structure 140 is formed over a carrier C, and a plurality of conductive posts 102 are formed on the redistribution layer structure 140. In some embodiments, a de-bonding layer DB and a dielectric layer DI are sequentially formed on the carrier C, and the redistribution layer structure 140 is formed on the dielectric layer DI. In some embodiments, the redistribution layer structure 140 is a back-side redistribution layer structure. The redistribution layer structure 140 includes a plurality of dielectric layers 142 and a plurality of conductive patterns 144 in the dielectric layers 142. The conductive patterns 144 are electrically connected to each other. The conductive posts 102 are electrically connected to the uppermost conductive patterns 144 of the redistribution layer structure 140. In some embodiments, two conductive posts 102 are disposed immediately adjacent to each other, to define a first region 101a for an electrical integrated circuit and a second region 101b for a photonic integrated circuit. That is, the electrical integrated circuit and the photonic integrated circuit will be then disposed in the first region 101a and the second region 101b respectively. However, the disclosure is not limited thereto. In some alternative embodiments, one conductive post or more than two conductive posts may be disposed to

separate the first region 101a and the second region 101b. Materials and/or forming methods of the carrier C, the conductive posts 102 and the redistribution layer structure 140 may be similar to or substantially the same as those of the carrier C, the conductive posts 102 and the redistribution layer structure 140 described above, and thus details are omitted herein.

[0035] Referring to FIG. 4B, then, an electrical integrated circuit 110 and a photonic integrated circuit 120 are disposed on the redistribution layer structure 140. For example, the electrical integrated circuit 110 is picked and placed onto the dielectric layer DI in the first region 101a, and the photonic integrated circuit 120 is picked and placed onto the dielectric layer DI in the second region 101b. In some embodiments, the photonic integrated circuit 120 includes a substrate 121 including an electro-interconnection region 121a and an optical region 121b, a conductive pad 122 and a conductive post 124 in the electro-interconnection region 121a and an optical transceiver OT and an optical coupler OC in the optical region 121b. In some embodiments, the photonic integrated circuit 120 further includes a passivation layer 123 is disposed on the substrate 121, and the conductive pad 122, the conductive post 124 and the optical coupler OC are disposed in the passivation layer 123. The passivation layer 123 may be a single layered or multiple layered structure. In some embodiments, the electrical integrated circuit 110 and the photonic integrated circuit 120 may be similar to the electrical integrated circuit 110 and the photonic integrated circuit 120 of FIG. 1E, and the main difference is described below.

[0036] FIG. 5 is a top view of an optical coupler of FIG. 4B. Referring to FIGS. 4B and 5, the optical coupler OC includes a waveguide 126 and a grating 128, for example. In some embodiments, the waveguide 126 may be a silicon waveguide, and the grating 128 may be a metal grating. A material of the waveguide 126 may be silicon nitride. The grating 128 may be formed directly on the waveguide 126 or have some spacing therebetween. In some embodiments, the grating 128 changes the direction of an incident optical signal light, and the waveguide 126 guides the optical signal light towards the optical transceiver OT. The electrical signal generated by the optical transceiver OT from the optical signal can be sent through the electro-connection region 121a interconnected to a desired part of the photonic integrated circuit 120. A material of the grating 128 may be copper, aluminum or any other suitable material. In some embodiments, as shown in FIG. 5, the waveguide 126 and the grating 128 have a triangular shape for coupling the optical signal on the wide right side that narrows towards the left side. In some alternative embodiments, the waveguide 126 and the grating 128 may have any other suitable shape.

[0037] Then, a waveguide WG is formed over the photonic integrated circuit 120 to optically couple with the optical coupler OC. In some embodiments, the waveguide WG is formed at an edge of the photonic integrated circuit 120. The waveguide WG is disposed on and in direct and physical contact with the grating 128, for example. In some embodiments, the waveguide WG is an optical fiber. In some embodiments, the waveguide WG is extended beyond the optical coupler OC and protruded from the edge of the photonic integrated circuit 120. For example, the waveguide WG is extended beyond the edges of the passivation layer 123 and the substrate 121.

[0038] Referring to FIG. 4C, an encapsulant 130 is formed over the carrier C to encapsulate the electrical integrated circuit 110, the photonic integrated circuit 120 and the conductive posts 102. In some embodiments, the encapsulant 130 fills between or surrounds the electrical integrated circuit 110, the photonic integrated circuit 120 and the conductive posts 102. A first surface 130a (i.e., top surface) of the encapsulant 130 is substantially coplanar with top surfaces of the electrical integrated circuit 110, the photonic integrated circuit 120 and the conductive posts 102. In some embodiments, the first surface 130a of the encapsulant 130 is substantially flush with top surfaces of the conductive post 114 and the protection layer 115 of the electrical integrated circuit 110, the conductive post 124, the protection layer 125 and the grating 128 of the photonic integrated circuit 120 and the conductive posts 102.

[0039] Then, a redistribution layer structure 150 is formed over the first surface 130a of the encapsulant 130 to electrically connect to the electrical integrated circuit 110, the photonic integrated circuit 120 and the conductive posts 102. In some embodiments, the redistribution layer structure 150 is separated from the waveguide WG. That is, a horizontal distance is formed between the redistribution layer structure 150 and the waveguide WG. In some embodiments, the redistribution layer structure 150 includes a plurality of dielectric layers 152 and a plurality of conductive patterns 154 in the dielectric layers 152. The conductive patterns 154 are electrically connected to each other. The conductive patterns 154 includes conductive lines, conductive vias or the like. In some embodiments, a material of the conductive patterns 154 includes aluminum, titanium, copper, nickel, tungsten, silver and/or alloys thereof. In some embodiments, a material of the dielectric layer 152 includes silicon oxide, silicon oxynitride, silicon nitride, BCB, PBO, polyimide or a combination thereof. In some embodiments, the bottommost conductive patterns 154 of the redistribution layer structure 150 are electrically connected to the conductive post 114 of the electrical integrated circuit 110, the conductive post 124 of the photonic integrated circuit 120 and the conductive posts 102 respectively. However, the disclosure is not limited thereto. In some embodiments, an outer sidewall of the redistribution layer structure 150 is substantially flush with a sidewall of the encapsulant 130. However, the disclosure is not limited thereto.

[0040] Referring to FIG. 4D, the dielectric layer DI is de-bonded from the de-bonding layer DB such that the structure of FIG. 4C is separated from the carrier C. That is, the carrier C is removed. Then, the formed structure is turned upside down and disposed on a frame F1. In some embodiments, the de-bonding layer DB (e.g., the LTHC release layer) may be irradiated by an UV laser such that the dielectric layer DI adhered on a second surface 130b (i.e., bottom surface) of the encapsulant 130 is peeled from the carrier C. After that, the dielectric layer DI is then patterned such that a plurality of contact openings O are formed to partially expose some of the conductive patterns 144. Then, a plurality of conductive terminals 146 are formed over and electrically connected to the redistribution layer structure 140. In some embodiments, the conductive terminals 146 are electrically connected to the electrical integrated circuit 110, the photonic integrated circuit 120 and the conductive posts 102 through the redistribution layer structure 140. In some embodiments, the conductive terminals 146 are, for example, solder balls or ball grid array ("BGA") balls.

[0041] Referring to FIG. 4E, the structure of FIG. 4D is de-bonded from the frame F1, and is turned upside down and disposed on a frame F2. Then, a memory 160 is disposed on and electrically connected to the redistribution layer structure 150. In some embodiments, the memory 160 is joined onto the redistribution layer structure 150 through a plurality of conductive terminals 162 and an underfill 168. The conductive terminals 162 are disposed on a surface of the memory 160 and electrically connected to a plurality of conductive pads 160a of the memory 160. After bonding, the conductive terminals 162 are electrically connected to the conductive patterns 154 of the redistribution layer structure 150. The underfill 168 is dispensed aside the conductive terminals 162 to protect the electrical connection between the conductive terminals 162 of the memory 160 and the conductive patterns 154 of the redistribution layer structure 150 and securely adhere the memory 160 onto the redistribution layer structure 150.

[0042] Referring to FIG. 4F, the structure in FIG. 4E is de-bonded from the frame F2, and a semiconductor package 100 is formed. In some embodiments, the semiconductor package 100 includes a unit U1 and the waveguide WG optically coupled to the unit U1. In some embodiments, the unit U1 includes the electrical integrated circuit 110, the photonic integrated circuit 120 and the memory 160. In some embodiments, as shown in FIG. 6, the unit U1 of the FIG. 4F may be connected to another unit U2 by the waveguide WG therebetween, so as to form a semiconductor package 10. In some embodiments, the unit U2 has a configuration similar to the unit U1. However, the disclosure is not limited thereto. In some alternative embodiments, the units U1, U2 may have different configuration.

[0043] FIG. 7 is a schematic cross-sectional view of a semiconductor package in accordance with some embodiments. The semiconductor package of FIG. 7 may be similar to the semiconductor package of FIG. 3, and thus the same reference numerals are used to refer to the same and liked parts, and its detailed description will be omitted herein. The difference is illustrated in details below.

[0044] Referring to FIG. 7, a semiconductor package 10 includes a plurality of units U1, U2 and a waveguide WG between the units U1, U2. In some embodiments, the unit U1, U2 includes a redistribution layer structure 140, an electrical integrated circuit 110, a photonic integrated circuit 120, a plurality of memories 160 and an encapsulant 130. In some embodiments, the electrical integrated circuit 110, the photonic integrated circuit 120 and the memories 160 are disposed on a first side of the redistribution layer structure 140 and encapsulated by the encapsulant 130. The electrical integrated circuit 110 and the photonic integrated circuit 120 are disposed side by side in a first direction D1 (e.g., horizontal direction). The memories 160 are stacked on the electrical integrated circuit 110 in a second direction D2 (e.g., vertical direction) substantially perpendicular to the first direction D1, for example. In some embodiments, the memories 160 and the electrical integrated circuit 110 are stacked vertically and electrically connected by conductive terminals 162 such as micro-bumps. In some embodiments, a plurality of conductive posts 102 are disposed between the photonic integrated circuit 120 and the electrical integrated circuit 110 and between the photonic integrated circuit 120 and the memory 160. The conductive posts 102 penetrate the encapsulant 130. In some embodiments, the redistribution layer structure 140 includes a plurality of dielectric layers

**142** and a plurality of conductive patterns **144** in the dielectric layers **142**. A plurality of conductive terminals **146** are disposed on a second side opposite to the first side of the redistribution layer structure **140** and electrically connected to the redistribution layer structure **140**. By the redistribution layer structure **140**, the electrical integrated circuit **110** and the photonic integrated circuit **120** are electrically connected. The configurations of the electrical integrated circuit **110** and the photonic integrated circuit **120** may be similar to or substantially the same as the configurations of the electrical integrated circuit **110** and the photonic integrated circuit **120** of FIG. 1E or FIG. 4F, and thus the details are omitted herein. However, the electrical integrated circuit **110** and the photonic integrated circuit **120** may have any other suitable configuration.

[0045] In some embodiments, the unit **U1**, **U2** are disposed side by side and separated from each other. In some embodiments, the waveguide **WG** is optically coupled to optical transceivers **OT** of the photonic integrated circuits **120** respectively, so as to connect the units **U1**, **U2**. In some embodiments, the waveguide **WG** is disposed between and on the optical transceivers **OT** over the encapsulants **130**, for example.

[0046] FIG. 8 is a schematic cross-sectional view of a semiconductor package in accordance with some embodiments. The semiconductor package of FIG. 7 may be similar to the semiconductor package of FIG. 3, and thus the same reference numerals are used to refer to the same and liked parts, and its detailed description will be omitted herein. The difference is illustrated in details below.

[0047] Referring to FIG. 8, a semiconductor package **10** includes a plurality of units **U1**, **U2** and a waveguide **WG** between the units **U1**, **U2**. In some embodiments, the unit **U1**, **U2** includes a redistribution layer structure **140**, an electrical integrated circuit **110**, a photonic integrated circuit **120**, a memory **160** and an encapsulant **130**. In some embodiments, the electrical integrated circuit **110**, the photonic integrated circuit **120** and the memory **160** are disposed side by side in a first direction **D1** (e.g., horizontal direction) on the redistribution layer structure **140** and encapsulated by the encapsulant **130**. In some alternative embodiments, the electrical integrated circuit **110** is disposed between the photonic integrated circuit **120** and the memory **160**. However, the disclosure is not limited thereto. In some alternative embodiments, the photonic integrated circuit **120** is disposed between the electrical integrated circuit **110** and the memory **160**, or the memory **160** is disposed between the electrical integrated circuit **110** and the photonic integrated circuit **120**. In some embodiments, a plurality of conductive posts **102** are disposed between the photonic integrated circuit **120** and the electrical integrated circuit **110** and between the electrical integrated circuit **110** and the memory **160**. The conductive posts **102** penetrate the encapsulant **130**. The configurations of the electrical integrated circuit **110** and the photonic integrated circuit **120** may be similar to or substantially the same as the configurations of the electrical integrated circuit **110** and the photonic integrated circuit **120** of FIG. 1E or FIG. 4F, and thus the details are omitted herein. However, the electrical integrated circuit **110** and the photonic integrated circuit **120** may have any other suitable configuration.

[0048] In some embodiments, the units **U1**, **U2** are bonded to each other in a face to face configuration. After bonding, the unit **U2** is disposed on the unit **U1** in a second direction

**D2** (e.g., vertical direction) substantially perpendicular to the first direction **D1**. In some embodiments, the electrical integrated circuits **110**, the photonic integrated circuits **120** and the memories **160** are disposed between the redistribution layer structures **140**. In some embodiments, the waveguide **WG** is disposed in a dielectric layer **170** on the unit **U1**, and the unit **U2** is disposed on the waveguide **WG** and the dielectric layer **170**. In some embodiments, the waveguide **WG** is optically coupled to optical transceivers **OT** of the units **U1**, **U2** respectively, so as to connect the units **U1**, **U2**. In some embodiments, a plurality of conductive vias **172** are further formed in the dielectric layer **170** to electrically connect the conductive posts **102** of the units **U1**, **U2**. In some embodiments, a plurality of conductive terminals **146** are disposed under the redistribution layer structure **140** of the unit **U1**. However, the disclosure is not limited thereto.

[0049] In some embodiments, the optical transceiver **OT** of the unit **U2** is partially overlapped with the optical transceiver **OT** of the unit **U1** in the second direction **D2**. For example, the optical transceiver **OT** of the unit **U2** is disposed directly on the optical transceiver **OT** of the unit **U1**. However, the disclosure is not limited thereto. In some alternative embodiments, as shown in FIG. 9, the optical transceiver **OT** of the unit **U2** is not overlapped with the optical transceiver **OT** of the unit **U1** in the second direction **D2**. For example, the photonic integrated circuit **120** of the unit **U2** is disposed above the electrical integrated circuit **110** of the unit **U1**. The memory **160** of the unit **U2** is disposed above the electrical integrated circuit **110** of the unit **U1**. The electrical integrated circuit **110** of the unit **U2** is disposed above the memory **160** of the unit **U1**. In other words, the optical transceivers **OT** of the units **U1**, **U2** are disposed offset from each other. In some embodiments, the waveguide **WG** is extended between the optical transceivers **OT** of the units **U1**, **U2** in the first direction **D1** (e.g., horizontal direction) substantially perpendicular to the second direction **D2**, to optically couple the optical transceivers **OT** respectively, so as to connect the units **U1**, **U2**.

[0050] FIG. 10 is a schematic cross-sectional view of a semiconductor package in accordance with some embodiments. The elements of the semiconductor package **100** of FIG. 10 may be similar to the elements of the semiconductor package **100** of FIG. 1E, and thus the same reference numerals are used to refer to the same and liked parts, and its detailed description will be omitted herein. The difference is illustrated in details below.

[0051] In some embodiments, the semiconductor package **100** includes a plurality of electrical integrated circuits **110**, a plurality of memories **160**, a photonic integrated circuit **120**, a waveguide **WG**, a redistribution layer structure **140** and an encapsulant **130**. In some embodiments, the memories **160** and the photonic integrated circuit **120** are disposed side by side, and the photonic integrated circuit **120** is disposed between the electrical integrated circuits **110**. In some embodiments, the electrical integrated circuits **110** are disposed over and electrically connected to the memories **160**, respectively. In some embodiments, the electrical integrated circuits **110** are electrically connected to an optical transceiver **OT** of the photonic integrated circuit **120**. For example, conductive pads **112** of the electrical integrated circuits **110** are electrically connected to conductive pads **122** of the photonic integrated circuit **120**, and the conductive pads **122** are electrically connected to conductive pads

**180** of the optical transceiver OT by connective patterns **182**. The waveguide WG is optically coupled to the optical transceiver OT. In some embodiments, the electrical integrated circuits **110**, the photonic integrated circuit **120**, the memories **160** and the waveguide WG are disposed over a first side of the redistribution layer structure **140** and encapsulated by the encapsulant **130**. In some embodiments, a plurality of conductive posts **102** are disposed between and electrically connected to the electrical integrated circuit **110** and the redistribution layer structure **140**. The conductive posts **102** penetrate the encapsulant **130**. In some embodiments, a plurality of conductive terminals **146** are disposed on a second side opposite to the first side of the redistribution layer structure **140**. In some embodiments, by the photonic integrated circuit **120**, a plurality of the electrical integrated circuits **110** are connected. Furthermore, the semiconductor package **100** may be connected to another semiconductor package through the waveguide WG. The configurations of the electrical integrated circuit **110** and the photonic integrated circuit **120** may be similar to or substantially the same as the configurations of the electrical integrated circuit **110** and the photonic integrated circuit **120** of FIG. 1E or FIG. 4F, and thus the details are omitted herein. However, the electrical integrated circuit **110** and the photonic integrated circuit **120** may have any other suitable configuration.

**[0052]** In some embodiments, as shown in FIG. 11, a plurality of units U are arranged in an array on a wafer W, and the units U are connected to each other by a waveguide (not shown) therebetween. The wafer is a semiconductor wafer, a reconstituted wafer or any other suitable wafer for carrying the semiconductor package. The units U may include an electrical integrated circuit **110**, a photonic integrated circuit **120** and a memory **160**. In some embodiments, the unit U and the waveguide may be similar to the unit U1 and the waveguide WG of FIG. 1E, 4F, 7, 8, 9 or 10. However, the disclosure is not limited thereto. In some alternative embodiments, the units U and the waveguide may have any other suitable configuration. Further, in some alternative embodiments, the units U may be horizontally arranged in an array, and further vertically stacked on one another. Accordingly, one system packaged on one wafer may be achieved.

**[0053]** In some embodiments, by using integrated fan-out (InFO) technique and the waveguide, optical interconnection between the photonic integrated circuit and the electrical integrated circuit are realized. Accordingly, ultra-speed signal transmission may be obtained, and the semiconductor package may be applied in multi-core high performance computing (HPC) applications. In addition, multiple dies such as the photonic integrated circuit, the electrical integrated circuit and the memory may be easily integrated without using an interposer. Conventionally, the interposer includes semiconductor materials such as silicon, and thus using the interposer increases the cost of manufacturing the semiconductor package. Accordingly, a form factor (or a thickness) of the semiconductor package and/or a cost for manufacturing the semiconductor package may become reduced.

**[0054]** According to some embodiments, a semiconductor package includes a first redistribution layer structure, a photonic integrated circuit, an electronic integrated circuit, a waveguide and a memory. The photonic integrated circuit is disposed over and electrically connected to the first redi-

tribution layer structure, and includes an optical transceiver and an optical coupler. The electronic integrated circuit is disposed over and electrically connected to the first redistribution layer structure. The waveguide is optically coupled to the optical coupler. The memory is electrically connected to the electronic integrated circuit.

**[0055]** According to some embodiments, a semiconductor package includes a first unit, a second unit and a waveguide. The first unit includes a first photonic integrated circuit, a first electronic integrated circuit and a first memory electrically connected to each other, and the first photonic integrated circuit includes a first optical transceiver. The second unit includes a second photonic integrated circuit, a second electronic integrated circuit and a second memory electrically connected to each other, and the second photonic integrated circuit includes a second optical transceiver. The waveguide is disposed between and optically coupled to the first optical transceiver and the second optical transceiver.

**[0056]** According to some embodiments, a semiconductor package includes a redistribution layer structure, a plurality of memories, a photonic integrated circuit, a plurality of electronic integrated circuits and a waveguide. The memories are disposed over and electrically connected to the redistribution layer structure. The photonic integrated circuit includes an optical transceiver and is disposed between the memory devices over the redistribution layer structure. The electronic integrated circuits are respectively disposed over and electrically connected to the memories and the photonic integrated circuit. The waveguide is disposed between the electronic integrated circuits and optically coupled to the optical transceiver.

**[0057]** According to some embodiments, a semiconductor package includes a photonic integrated circuit, an electronic integrated circuit and a waveguide. The photonic integrated circuit includes an optical coupler. The electronic integrated circuit is disposed aside the photonic integrated circuit. The waveguide is optically coupled to the optical coupler, wherein the waveguide is disposed at an edge of the photonic integrated circuit and protrudes from the edge of the photonic integrated circuit.

**[0058]** According to some embodiments, a semiconductor package includes a first photonic integrated circuit, a second photonic integrated circuit and a waveguide. The first photonic integrated circuit includes a first optical transceiver. The second photonic integrated circuit includes a second optical transceiver. The waveguide is disposed between and optically coupled to the first optical transceiver and the second optical transceiver.

**[0059]** According to some embodiments, a semiconductor package includes a photonic integrated circuit, a plurality of electronic integrated circuits and a waveguide. The photonic integrated circuit includes an optical transceiver. The electronic integrated circuits are disposed over and electrically connected to the photonic integrated circuit. The waveguide is disposed between the electronic integrated circuits and optically coupled to the optical transceiver.

**[0060]** According to some embodiments, a semiconductor package includes a first integrated circuit and a first waveguide. The first integrated circuit includes an optical coupler. The first waveguide is optically coupled to the optical coupler, wherein the first waveguide protrudes beyond the optical coupler.

**[0061]** According to some embodiments, a semiconductor package includes a first integrated circuit and a first wave-

guide. The first integrated circuit includes an optical coupler. The first waveguide is optically coupled to the optical coupler, wherein the first waveguide is partially overlapped with the optical coupler.

**[0062]** According to some embodiments, a semiconductor package includes a first integrated circuit, a second integrated circuit and a first waveguide. The first integrated circuit includes a first optical transceiver. The second integrated circuit includes a second optical transceiver. The first waveguide extends between the first integrated circuit and the second integrated circuit.

**[0063]** According to some embodiments, a semiconductor package includes a first integrated circuit, a first waveguide, a second integrated circuit and a first redistribution layer structure. The first integrated circuit includes an optical coupler. The first waveguide is optically coupled to the optical coupler. The second integrated circuit is electrically connected to the first integrated circuit through the first redistribution layer structure.

**[0064]** According to some embodiments, a semiconductor package includes a first waveguide and an optical coupler. The optical coupler is optically coupled to the first waveguide, wherein the optical coupler includes a second waveguide and a grating between the first waveguide and the second waveguide.

**[0065]** According to some embodiments, a semiconductor package includes a first waveguide, a second waveguide and a third waveguide. The first waveguide is disposed in a first passivation layer. The second waveguide is disposed on the first waveguide and optically coupled to the first waveguide. The third waveguide is disposed on the second waveguide and over the first passivation layer.

**[0066]** The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A semiconductor package, comprising:  
a first integrated circuit, comprising an optical coupler;  
a first waveguide, optically coupled to the optical coupler;  
a second integrated circuit; and  
a first redistribution layer structure, wherein the second integrated circuit is electrically connected to the first integrated circuit through the first redistribution layer structure.
2. The semiconductor package as claimed in claim 1, wherein the first integrated circuit and the second integrated circuit are encapsulated in an encapsulant.
3. The semiconductor package as claimed in claim 1, wherein the first integrated circuit and the second integrated circuit are disposed on a first surface of the first redistribution layer structure.
4. The semiconductor package as claimed in claim 3, further comprising a through via between the first integrated

circuit and the second integrated circuit and a third integrated circuit electrically connected to the first redistribution layer structure through the through via.

5. The semiconductor package as claimed in claim 1, further comprising a second redistribution layer structure, wherein the first integrated circuit and the second integrated circuit are disposed between the first redistribution layer structure and the second redistribution layer structure.

6. The semiconductor package as claimed in claim 1, wherein the first waveguide protrudes from a first sidewall of the first redistribution layer structure and beyond the first integrated circuit.

7. The semiconductor package as claimed in claim 1, wherein the first waveguide is overlapped with the optical coupler.

8. The semiconductor package as claimed in claim 1, wherein the optical coupler comprises a second waveguide.

9. The semiconductor package as claimed in claim 8, wherein the optical coupler further comprises a third waveguide, and the third waveguide is disposed between the first waveguide and the second waveguide.

10. The semiconductor package as claimed in claim 8, wherein a sidewall of the second waveguide is substantially flush with a sidewall of the third waveguide.

11. A semiconductor package, comprising:

- a first waveguide; and
- an optical coupler, optically coupled to the first waveguide, wherein the optical coupler comprises a second waveguide and a grating between the first waveguide and the second waveguide.

12. The semiconductor package as claimed in claim 11, wherein the first waveguide protrudes beyond the optical coupler.

13. The semiconductor package as claimed in claim 11, wherein the first waveguide, the second waveguide and the grating are overlapped.

14. The semiconductor package as claimed in claim 11, further comprising an encapsulant encapsulating the grating, wherein a sidewall of the encapsulant is substantially flush with a sidewall of the second waveguide.

15. The semiconductor package as claimed in claim 11, further comprising an optical transceiver, wherein the second waveguide is disposed between the optical transceiver and the grating.

16. A semiconductor package, comprising:

- a first waveguide in a first passivation layer;
- a second waveguide on the first waveguide and optically coupled to the first waveguide; and
- a third waveguide on the second waveguide and over the first passivation layer.

17. The semiconductor package as claimed in claim 16, wherein the third waveguide protrudes beyond the first waveguide and the second waveguide.

18. The semiconductor package as claimed in claim 16, wherein the second waveguide is disposed in a second passivation layer on the first passivation layer.

19. The semiconductor package as claimed in claim 16, wherein a sidewall of the first waveguide is substantially flush with a sidewall of the second waveguide.

20. The semiconductor package as claimed in claim 16, further comprising an optical transceiver under the first waveguide, the second waveguide and the third waveguide.

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