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SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

Abstract

A method of manufacturing a semiconductor device includes: forming a well region of a second conductivity-type on a top surface side of a semiconductor base-body of a first conductivity-type; forming a plurality of channel formation regions of the first conductivity-type on a top surface side of the well region; forming a plurality of drift regions on the top surface side of the well region alternately with the channel formation regions; forming a plurality of gate electrodes on top surface sides of the respective channel formation regions with a gate insulating film interposed; and forming a wiring layer arranged over the well region, wherein forming the well region including: forming a plurality of first ion implantation regions formed into slits and having different widths, and forming a second ion implantation region at a position overlapping with the wiring layer on an end part side of the first ion implantation regions having a relatively narrow width; and forming the well region by annealing.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims benefit of priority under 35 USC 119 based on Japanese Patent Application No. 2024-017742 filed on Feb. 8, 2024, the entire contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present disclosure relates to semiconductor devices and methods of manufacturing the same.

2. Description of the Related Art

[0003] JP2015-233056A discloses a lateral MOSFET in which source regions and drain regions are alternately arranged in a short-side direction (a gate-length direction) perpendicular to a longitudinal direction of gate electrodes.

[0004] Semiconductor devices such as a lateral MOSFET include an n-type well region implementing a voltage blocking structure on a top surface side of a p-type semiconductor base-body.

[0005] Upon the formation of the n-type well region, n-type impurity ions are implanted into plural slits in order to adjust an impurity concentration in the n-type well region, and then subject the implanted n-type impurity ions to annealing to be activated so as to form the single n-type well region.

[0006] However, the provision of the thin slit-shaped parts in the ion-implanted region impedes a sufficient diffusion of the implanted n-type impurity ions in the lateral direction, which may cause a region having a locally low impurity concentration in the n-type well region. If a wiring layer overlaps with the region with the low impurity concentration, a channel may be formed on the surface of such a region, leading to a leakage path accordingly.

SUMMARY OF THE INVENTION

[0007] In view of the foregoing problems, the present disclosure provides a semiconductor device having a configuration capable of avoiding a reduction in impurity concentration in an n-type well region provided immediately under a wiring layer and preventing a cause of a leakage path, and also provides a method of manufacturing the same.

[0008] An aspect of the present disclosure inheres in a semiconductor device including: A semiconductor device including: a semiconductor base-body of a first conductivity-type; a well region of a second conductivity-type provided on a top surface side of the semiconductor base-body; a plurality of channel formation regions of the first conductivity-type provided on a top surface side of the well region and extending parallel to each other in one direction in a planar view; a plurality of drift regions provided on the top surface side of the well region alternately with the channel formation regions and extending parallel to each other in the one direction; a plurality of carrier-supply regions of the second conductivity-type provided on top surface sides of the

respective channel formation regions; a plurality of carrier-reception regions of the second conductivity-type provided on top surface sides of the respective drift regions; a plurality of gate electrodes provided on top surface sides of the respective channel formation regions with a gate insulating film interposed at positions between the carrier-supply regions and the well region, and extending parallel to each other in the one direction; and a wiring layer arranged over the well region on an end part side of the channel formation regions and the drift regions in the one direction to extend in a direction perpendicular to the one direction, wherein an impurity concentration of the well region at a position located on the end part side of the channel formation regions interposed between the drift regions next to each other and overlapping with the wiring layer is greater than or equal to that of the well region at a position on the end part side of the drift regions and overlapping with the wiring layer.

[0009] Another aspect of the present disclosure inheres in a method of manufacturing the above semiconductor device, the method includes forming the well region including: implanting impurity ions of the second conductivity-type to form a plurality of first ion implantation regions formed into slits extending parallel to the one direction and having different widths, and form a second ion implantation region extending in the direction perpendicular to the one direction at a position overlapping with the wiring layer on an end part side of one of the first ion implantation regions having a relatively narrow width; and diffusing the impurity ions implanted to the first ion implantation regions and the second ion implantation region in a lateral direction by annealing so as to form the well region.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. **1** is a cross-sectional view illustrating a semiconductor device according to a first embodiment;

[0011] FIG. **2** is a plan view illustrating the semiconductor device according to the first embodiment;

[0012] FIG. **3** is a plan view illustrating the semiconductor device according to the first embodiment;

[0013] FIG. **4** is a cross-sectional view taken along line A-A′ in FIG. **2** and FIG. **3**;

[0014] FIG. **5** is a cross-sectional view taken along line B-B′in FIG. **2** and FIG. **3**;

[0015] FIG. **6** is a cross-sectional view for explaining a method of manufacturing the semiconductor device according to the first embodiment;

[0016] FIG. **7** is a cross-sectional view for explaining the method of manufacturing the semiconductor device according to the first embodiment;

[0017] FIG. **8**A is a plan view for explaining the method of manufacturing the semiconductor device according to the first embodiment;

[0018] FIG. **8**B is a plan view for explaining the method of manufacturing the semiconductor device according to the first embodiment;

[0019] FIG. **9** is a cross-sectional view taken along line A-A′ in FIG. **8**A and FIG. **8**B;

[0020] FIG. **10** is a cross-sectional view taken along line B-B′ in FIG. **8**A and FIG. **8**B;

[0021] FIG. **11** is a cross-sectional view continued from FIG. **6**, for explaining the method of manufacturing the semiconductor device according to the first embodiment;

[0022] FIG. **12** is a cross-sectional view taken along line A-A′ in FIG. **8**A and FIG. **8**B at a phase corresponding to FIG. **11**;

[0023] FIG. **13** is a cross-sectional view taken along line B-B′ in FIG. **8**A and FIG. **8**B at a phase corresponding to FIG. **11**;

[0024] FIG. **14** is a cross-sectional view continued from FIG. **11**, for explaining the method of

manufacturing the semiconductor device according to the first embodiment;
[0025] FIG. **15** is a cross-sectional view continued from FIG. **14**, for explaining the method of manufacturing the semiconductor device according to the first embodiment;
[0026] FIG. **16** is a cross-sectional view continued from FIG. **15**, for explaining the method of manufacturing the semiconductor device according to the first embodiment;
[0027] FIG. **17** is a cross-sectional view illustrating a semiconductor device of a first comparative example;
[0028] FIG. **18** is a cross-sectional view for explaining a method of manufacturing the semiconductor device of the first comparative example;
[0029] FIG. **19** is a plan view for explaining a method of manufacturing a semiconductor device of a second comparative example;
[0030] FIG. **20** is a plan view for explaining a method of manufacturing a semiconductor device according to a second embodiment; and
[0031] FIG. **21** is a plan view for explaining a method of manufacturing a semiconductor device according to a third embodiment.

DETAILED DESCRIPTION

[0032] With reference to the drawings, first to third embodiments of the present disclosure will be described below.
[0033] In the drawings, the same or similar elements are indicated by the same or similar reference numerals. The drawings are schematic, and it should be noted that the relationship between thickness and planer dimensions, the thickness proportion of each layer, and the like are different from real ones. Accordingly, specific thicknesses or dimensions should be determined with reference to the following description. Moreover, in some drawings, portions are illustrated with different dimensional relationships and proportions. The first to third embodiments described below merely illustrate schematically devices and methods for specifying and giving shapes to the technical idea of the present disclosure, and the span of the technical idea is not limited to materials, shapes, structures, and relative positions of elements described herein.
[0034] In the specification, a “carrier-supply region” means a semiconductor region which supplies majority carriers as a main current. The carrier-supply region is assigned to a semiconductor region which will be a source region in a field-effect transistor (FET) or a static induction transistor (SIT), an emitter region in an insulated-gate bipolar transistor (IGBT), and an anode region in a diode, a static induction (SI) thyristor or a gate turn-off (GTO) thyristor. A “carrier-reception region” means a semiconductor region which receive the majority carriers as the main current. The carrier-reception region is assigned to a semiconductor region which will be the drain region in the FET or the SIT, the collector region in the IGBT, and the cathode region in the diode, SI thyristor or GTO thyristor.
[0035] In the specification, definitions of directions such as an up-and-down direction in the following description are merely definitions for convenience of understanding, and are not intended to limit the technical ideas of the present disclosure. For example, as a matter of course, when the subject is observed while being rotated by 90°, the subject is understood by converting the up-and-down direction into the right-and-left direction. When the subject is observed while being rotated by 180°, the subject is understood by inverting the up-and-down direction.
[0036] In the specification, there is exemplified a case where a first conductivity-type is a p-type and a second conductivity-type is an n-type. However, the relationship of the conductivity-types may be inverted to set the first conductivity-type to the n-type and the second conductivity-type to the p-type. Further, a semiconductor region denoted by the symbol “n” or “p” attached with “+” indicates that such semiconductor region has a relatively high impurity concentration as compared to a semiconductor region denoted by the symbol “n” or “p” without “+”. A semiconductor region denoted by the symbol “n” or “p” attached with “−” indicates that such semiconductor region has a relatively low impurity concentration as compared to a semiconductor region denoted by the

symbol “n” or “p” without “−”. However, even when the semiconductor regions are denoted by the same reference symbols “n” and “n”, it is not indicated that the semiconductor regions have exactly the same impurity concentration. Moreover, the members and the regions that are limited by adding “first conductivity-type” and “second conductivity-type” in the following description indicate the members and the regions formed of semiconductor materials without particular obvious limitations.

FIRST EMBODIMENT

<Configuration of Semiconductor Device>

[0037] A semiconductor device according to a first embodiment is illustrated below with a lateral n-channel metal-oxide-semiconductor field-effect transistor (MOSFET). As illustrated in FIG. **1**, the semiconductor device according to the first embodiment includes an array of plural transistor cells T**1** to T**6**. While FIG. **1** illustrates the case of including the six transistor cells T**1** to T**6**, the number of the transistor cells in array may be changed as appropriate. The semiconductor device according to the first embodiment has a breakdown voltage of about 60 volts or higher, for example.

[0038] The semiconductor device according to the first embodiment includes a semiconductor base-body **1** of a first conductivity-type (p-type). The semiconductor base-body **1** is a semiconductor substrate such as a silicon (Si) substrate, for example. The semiconductor base-body **1** may be a semiconductor substrate including silicon carbide (SiC), gallium nitride (GaN), gallium oxide (Ga.sub.2O.sub.3), gallium arsenide (GaAs), or diamond (C), for example. Alternatively, the semiconductor base-body **1** may be implemented by a semiconductor region (a semiconductor layer) of p-type provided on the top surface side of a semiconductor substrate of p-type or n-type.

[0039] A well region (deep n-well: DNW) **2** of a second conductivity-type (n-type) is provided on the top surface side (at the upper part) of the semiconductor base-body **1**. A plurality of channel formation regions (well regions) **3***a* to **3***d* of p-type are provided separately from each other on the top surface side (at the upper part) of the well region **2**. A plurality of drift regions **4***a* to **4***c* of n-type having a higher impurity concentration than the well region **2** are provided separately from each other on the top surface side (at the upper part) of the well region **2**. The drift regions **4***a* to **4***c* are arranged alternately with the channel formation regions **3***a* to **3***d*.

[0040] A contact region **7***a* of p.sup.+-type and a carrier-supply region (a source region) **8***a* of n.sup.+-type are provided on the top surface side (at the upper part) of the channel formation region **3***a*. The contact region **7***a* and the source region **8***a* are in contact with each other. The contact region **7***a* has a higher impurity concentration than the channel formation region **3***a*. The contact region **7***a* is connected to a source electrode **22** arranged on the top surface side of an interlayer insulating film **32** provided on the top surface side of the semiconductor base-body **1** through a via **22***a* penetrating the interlayer insulating film **32**. The source region **8***a* is connected to the source electrode **22** through a via **22***b* penetrating the interlayer insulating film **32**. The source electrode **22** is covered with a passivation insulating film **33** provided on the top surface side of the interlayer insulating film **32**.

[0041] The interlayer insulating film **32** as used herein can be a non-doped silicon oxide film without containing phosphorus (P) or boron (B) (an SiO.sub.2 film) which is referred to as a non-doped silicate glass (NSG) film. Other examples used as the interlayer insulating film **32** include a phosphosilicate glass film (a PSG film), a borosilicate glass film (a BSG film), a borophosphosilicate glass film (a BPSG film), a silicon nitride (Si.sub.3N.sub.4) film, and a stacked layer including the above films stacked on one another. The passivation insulating film **33** as used herein can be a film including resin such as polyimide.

[0042] A carrier-reception region (a drain region) **9***a* of n.sup.+-type having a higher impurity concentration than the drift region **4***a* is provided on the top surface side (at the upper part) of the drift region **4***a*. The drain region **9***a* is connected to a drain electrode **23** provided on the top surface side of the interlayer insulating film **32** through a via **23***a* penetrating the interlayer insulating film **32**. An insulating film (an element-separation insulating film) **31** is provided on both sides of the

respective side surfaces of the drift region **4***a* and the drain region **9***a*.
[0043] The element-separation insulating film **31** is an oxide film such as a local insulating film (a LOCOS film) selectively (locally) formed by local oxidation of silicon (LOCOS).
[0044] A gate electrode **11***a* is provided on the top surface sides of the channel formation region **3***a* and the well region **2** with the gate insulating film **10***a* interposed at a position between the source region **8***a* and the drain region **9***a*. A side-wall insulating film **12***a* is provided to cover the side surfaces on both sides of the gate electrode **11***a*.
[0045] The gate insulating film **10***a* as used herein can be a silicon oxide (SiO.sub.2) film, or can be any of a silicon oxynitride (SiON) film, a strontium oxide (SrO) film, a silicon nitride (Si.sub.3N.sub.4) film, an aluminum oxide (Al.sub.2O.sub.3) film, a magnesium oxide (MgO) film, an yttrium oxide (Y.sub.2O.sub.3) film, a hafnium oxide (HfO.sub.2) film, a zirconium oxide (ZrO.sub.2) film, a tantalum oxide (Ta.sub.2O.sub.5) film, or a bismuth oxide (Bi.sub.2O.sub.3) film, or a composite film including some of the above films stacked on one another. The gate electrode **11***a* may be a polysilicon layer (a doped polysilicon layer) heavily doped with p-type impurities such as boron (B) or n-type impurities such as phosphorus (P), or may be a layer including refractory metal.
[0046] A carrier-supply region (a source region) **8***b* of n.sup.+-type, a contact region **7***b* of p.sup.+-type, and a carrier-supply region (a source region) **8***c* of n.sup.+-type are provided on the top surface side (at the upper part) of the channel formation region **3***b*. The source region **8***b* and the contact region **7***b* are in contact with each other. The contact region **7***b* and the source region **8***c* are in contact with each other. The source region **8***b* is connected to a source electrode **24** provided on the top surface side of the interlayer insulating film **32** through a via **24***a* penetrating the interlayer insulating film **32**. The contact region **7***b* has a higher impurity concentration than the channel formation region **3***b*. The contact region **7***b* is connected to the source electrode **24** through a via **24***b* penetrating the interlayer insulating film **32**. The source region **8***c* is connected to the source electrode **24** through a via **24***c* penetrating the interlayer insulating film **32**. The source electrode **24** is covered with the passivation insulating film **33**.
[0047] A gate electrode **11***b* is provided on the top surface sides of the channel formation region **3***b* and the well region **2** with the gate insulating film **10***b* interposed at a position between the drain region **9***a* and the source region **8***b*. A side-wall insulating film **12***b* is provided to cover the side surfaces on both sides of the gate electrode **11***b*.
[0048] A carrier-reception region (a drain region) **9***b* of n.sup.+-type having a higher impurity concentration than the drift region **4***b* is provided on the top surface side (at the upper part) of the drift region **4***b*. The drain region **9***b* is connected to a drain electrode **25** provided on the top surface side of the interlayer insulating film **32** through a via **25***a* penetrating the interlayer insulating film **32**. The element-separation insulating film **31** is provided on both sides of the respective side surfaces of the drift region **4***b* and the drain region **9***b*.
[0049] A gate electrode **11***c* is provided on the top surface sides of the channel formation region **3***b* and the well region **2** with the gate insulating film **10***c* interposed at a position between the source region **8***c* and the drain region **9***b*. A side-wall insulating film **12***c* is provided to cover the side surfaces on both sides of the gate electrode **11***c*.
[0050] A carrier-supply region (a source region) **8***d* of n.sup.+-type, a contact region **7***c* of p.sup.+-type, and a carrier-supply region (a source region) **8***e* of n.sup.+-type are provided on the top surface side (at the upper part) of the channel formation region **3***c*. The source region **8***d* and the contact region **7***c* are in contact with each other. The contact region **7***c* and the source region **8***e* are in contact with each other. The source region **8***d* is connected to a source electrode **26** provided on the top surface side of the interlayer insulating film **32** through a via **26***a* penetrating the interlayer insulating film **32**. The contact region **7***c* has a higher impurity concentration than the channel formation region **3***c*. The contact region **7***c* is connected to the source electrode **26** through a via **26***b* penetrating the interlayer insulating film **32**. The source region **8***e* is connected to the source

electrode **26** through a via **26***c* penetrating the interlayer insulating film **32**. The source electrode **26** is covered with the passivation insulating film **33**.

[0051] A gate electrode **11***d* is provided on the top surface sides of the channel formation region **3***c* and the well region **2** with the gate insulating film **10***d* interposed at a position between the drain region **9***b* and the source region **8***d*. A side-wall insulating film **12***d* is provided to cover the side surfaces on both sides of the gate electrode **11***d*.

[0052] A carrier-reception region (a drain region) **9***c* of n.sup.+-type having a higher impurity concentration than the drift region **4***c* is provided on the top surface side (at the upper part) of the drift region **4***c*. The drain region **9***c* is connected to a drain electrode **27** provided on the top surface side of the interlayer insulating film **32** through a via **27***a* penetrating the interlayer insulating film **32**. The element-separation insulating film **31** is provided on both sides of the respective side surfaces of the drift region **4***c* and the drain region **9***c*.

[0053] A gate electrode **11***e* is provided on the top surface sides of the channel formation region **3***c* and the well region **2** with the gate insulating film **10***e* interposed at a position between the source region **8***e* and the drain region **9***c*. A side-wall insulating film **12***e* is provided to cover the side surfaces on both sides of the gate electrode **11***e*.

[0054] A carrier-supply region (a source region) **8***f* of n.sup.+-type and a contact region **7***d* of p.sup.+-type are provided on the top surface side (at the upper part) of the channel formation region **3***d*. The source region **8***f* and the contact region **7***d* are in contact with each other. The source region **8***f* is connected to a source electrode **28** provided on the top surface side of the interlayer insulating film **32** through a via **28***a* penetrating the interlayer insulating film **32**. The contact region **7***d* has a higher impurity concentration than the channel formation region **3***d*. The contact region **7***d* is connected to the source electrode **28** through a via **28***b* penetrating the interlayer insulating film **32**. The source electrode **28** is covered with the passivation insulating film **33**.

[0055] A gate electrode **11***f* is provided on the top surface sides of the channel formation region **3***d* and the well region **2** with the gate insulating film **10***f* interposed at a position between the drain region **9***c* and the source region **8***f*. A side-wall insulating film **12***f* is provided to cover the side surfaces on both sides of the gate electrode **11***f*.

[0056] The transistor cell T**1** includes the contact region **7***a*, the source region **8***a*, the drain region **9***a*, and the gate electrode **11***a*. The transistor cell T**2** has a linearly symmetric structure with respect to the transistor cell T**1** about the drain region **9***a*. The transistor cell T**2** includes the contact region **7***b*, the source region **8***b*, the drain region **9***b*, and the gate electrode **11***b*. The drain region **9***a* is commonly used in the respective transistor cells T**1** and T**2**.

[0057] The transistor cell T**3** has a linearly symmetric structure with respect to the transistor cell T**2** about the contact region **7***b*. The transistor cell T**3** includes the contact region **7***b*, the source region **8***c*, the drain region **9***b*, and the gate electrode **11***c*. The contact region **7***b* is commonly used in the respective transistor cells T**2** and T**3**.

[0058] The transistor cell T**4** has a linearly symmetric structure with respect to the transistor cell T**3** about the drain region **9***b*. The transistor cell T**4** includes the contact region **7***c*, the source region **8***d*, the drain region **9***b*, and the gate electrode **11***d*. The drain region **9***b* is commonly used in the respective transistor cells T**3** and T**4**.

[0059] The transistor cell T**5** has a linearly symmetric structure with respect to the transistor cell T**4** about the contact region **7***c*. The transistor cell T**5** includes the contact region **7***c*, the source region **8***e*, the drain region **9***c*, and the gate electrode **11***d*. The contact region **7***c* is commonly used in the respective transistor cells T**4** and T**5**.

[0060] The transistor cell T**6** has a linearly symmetric structure with respect to the transistor cell T**5** about the drain region **9***c*. The transistor cell T**6** includes the contact region **7***d*, the source region **8***f*, the drain region **9***c*, and the gate electrode **11***f*. The drain region **9***c* is commonly used in the respective transistor cells T**5** and T**6**.

[0061] A well region **5** of p-type having a higher impurity concentration than the semiconductor

base-body **1** is provided on the top surface side (at the upper part) of the semiconductor base-body **1** on the outside of the well region **2**. A contact region **6** of p.sup.+-type having a higher impurity concentration than the well region **5** is provided on the top surface side (at the upper side) of the well region **5**. The contact region **6** is connected to substrate contact electrodes **21** and **29** provided on the top surface side of the interlayer insulating film **32** through vias **21***a* and **29***a* penetrating the interlayer insulating film **32**. The substrate contact electrodes **21** and **29** can be connected to each other on the frontward and backward sides of FIG. **1**. The substrate contact electrodes **21** and **29** are covered with the passivation insulating film **33**. The element-separation insulating film **31** is provided on both sides of the respective side surfaces of the well region **5** and the contact region **6**.

[0062] FIG. **2** is a plan view illustrating a part of the semiconductor device according to the first embodiment illustrated in FIG. **1**. The cross-section taken along line C-C′ in FIG. **2** corresponds to the region including the transistor cells TI to T**4** on the left side of the cross section in FIG. **1**. FIG. **2** omits the illustration of the interlayer insulating film **32**, the passivation insulating film **33**, the vias **21***a*, **22***a*, **22***b*, **23***a*, **24***a* to **24***c*, and **25***a*, the substrate contact electrode **21**, the source electrodes **22** and **24**, and the drain electrodes **23** and **25** illustrated in FIG. **1**.

[0063] As illustrated in FIG. **2**, the gate electrodes **11***a* to **11***d* each have a stripe-shaped planar pattern to extend parallel to each other in one direction (in the upper-lower direction in FIG. **2**). A gate wiring layer **42** is arranged above the respective end parts of the gate electrodes **11***a* to **11***d*. The gate wiring layer **42** has a stripe-shaped planar pattern extending in the direction perpendicular to the extending direction of the gate electrodes **11***a* to **11***d* (in the right-left direction in FIG. **2**). The gate wiring layer **42** is electrically connected to the gate electrodes **11***a* to **11***d*. The gate electrodes **11***e* and **11***f* illustrated in FIG. **1** also each have a strip-shaped planar pattern to extend parallel to each other in one direction (in the upper-lower direction in FIG. **2**) in the same manner as the gate electrodes **11***a* to **11***d*, and are electrically connected to the gate wiring layer **42**.

[0064] A wiring layer **41** is provided separately from the gate wiring layer **42**. The wiring layer **41** has a stripe-shaped planar pattern extending parallel to the extending direction of the gate wiring layer **42** (in the right-left direction in FIG. **2**). The wiring layer **41** may be a source wiring layer connected to the respective source electrodes **22**, **24**, **26**, and **28** illustrated in FIG. **1**, for example. Alternately, the wiring layer **41** may be a drain wiring layer connected to the respective drain electrodes **23**, **25**, and **27**. The wiring layer **41** may be another layer to which a potential is applied, other than the source wiring layer or the drain wiring layer.

[0065] The element-separation insulating film **31** is provided with openings **31***a* to **31***e*. FIG. **2** illustrates the openings **31***a* and **31***c* of the element-separation insulating film **31** and also schematically indicates, by the broken lines, the parts of the openings **31***a* and **31***c* hidden immediately under the gate electrodes **11***a* to **11***c*. The contact region **7***a* and the source region **8***a* are exposed to the opening **31***a* of the element-separation insulating film **31**. The drain region **9***a* is exposed to the opening **31***b* of the element-separation insulating film **31**. The contact region **7***b* and the source regions **8***a* and **8***c* are exposed to the opening **31***c* of the element-separation insulating film **31**. The drain region **9***b* is exposed to the opening **31***d* of the element-separation insulating film **31**. The contact region **6** is exposed to the opening **31***e* of the element-separation insulating film **31**.

[0066] FIG. **3** is a plan view illustrating the semiconductor device according to the first embodiment at a region common to that illustrated in FIG. **2**. FIG. **3** schematically indicates, by the solid lines, the n″-type well region **2**, the p-type channel formation regions **3***a* and **3***b*, the p-type connection region **3***e*, and the p-type well region **5** provided in the p-type semiconductor base-body **1**.

[0067] As illustrated in FIG. **3**, the well region **2** has a substantially rectangular planar pattern. The channel formation regions **3***a* and **3***b* are provided inside the well region **2**. The channel formation regions **3***a* and **3***b* each have a stripe-shaped planar pattern extending in the extending direction of the gate electrodes **11***a* to **11***d* (in the upper-lower direction in FIG. **3**). The connection region **3***e* is

connected to the end parts of the channel formation regions **3***a* and **3***b* in the extending direction. The connection region **3***e* has a stripe-shaped planar pattern extending in the direction perpendicular to the extending direction of the gate electrodes **11***a* to **11***d* (in the right-left direction in FIG. **3**). The channel formation regions **3***c* and **3***d* illustrated in FIG. **1** also each have a stripe-shaped planar pattern extending in the extending direction of the gate electrodes **11***a* to **11***d* (in the upper-lower direction in FIG. **3**), and are connected to the connection region **3***e,* as in the case of the channel formation regions **3***a* and **3***b.* The well region **5** has a loop-shaped planar pattern surrounding the circumference of the well region **2**.

[0068] Although not illustrated in FIG. **3**, the drift regions **4***a* to **4***c* illustrated in FIG. **1** each have a stripe-shaped planar pattern extending in the extending direction of the gate electrodes **11***a* to **11***d* (in the upper-lower direction in FIG. **3**). The end parts of the drift regions **4***a* to **4***c* are located inside the well region **2**.

[0069] FIG. **3** illustrates, as a region A**1** indicated by the broken line, a position of the end part of the well region **2** overlapping with the wiring layer **41** on the end part side of the gate electrode **11***a* and the channel formation region **3***a* in the extending direction. FIG. **3** also illustrates, as a region A**2** indicated by the broken line, a position of the end part of the well region **2** overlapping with the wiring layer **41** on the end part side of the gate electrode **11***b* and the channel formation region **3***b* in the extending direction. FIG. **3** also illustrates, as a region A**3** indicated by the broken line, a position of the end part of the well region **2** overlapping with the wiring layer **41** on the end part side of the gate electrode **11***c* and the channel formation region **3***b* in the extending direction.

[0070] In the semiconductor device according to the first embodiment, the impurity concentration of the well region **2** at the positions corresponding to the regions A**2** and A**3** indicated by the broken lines is higher than or equal to that of the well region **2** at the position overlapping with the wiring layer **41** other than the regions A**2** and A**3**. For example, the impurity concentration of the well region **2** at the positions corresponding to the regions A**2** and A**3** is higher than or equal to that of the well region **2** at the position corresponding to the region A**1**. In addition, the impurity concentration of the well region **2** at the positions corresponding to the regions A**2** and A**3** is higher than or equal to that of the well region **2** at the position overlapping with the wiring layer **41** on the end part side of the drift regions **4***a* to **4***c* in the extending direction.

[0071] FIG. **4** is a cross-sectional view taken along taken along line A-A′ passing through the gate electrode **11***a* illustrated in FIG. **2** and FIG. **3**. As illustrated in FIG. **3** and FIG. **4**, the end part of the channel formation region **3***a* is located on the outside of the end part of the gate electrode **11***a* in the extending direction of the gate electrode **11***a.* The end part of the well region **2** is located on the outside of the end part of the channel formation region **3***a* so as to overlap with the wiring layer **41**. The element-separation insulating film **31** is provided on the top surface side of the respective end parts of the channel formation region **3***a* and the well region **2**. The region A**1** indicated by the broken line surrounds the surface of the end part of the well region **2**.

[0072] FIG. **5** is a cross-sectional view taken along taken along line B-B′ passing through the gate electrode **11***b* illustrated in FIG. **2** and FIG. **3**. As illustrated in FIG. **3** and FIG. **5**, the end part of the channel formation region **3***b* is located on the outside of the end part of the gate electrode **11***b* in the extending direction of the gate electrode **11***b.* The end part of the well region **2** is located on the outside of the end part of the channel formation region **3***b* so as to overlap with the wiring layer **41**. The element-separation insulating film **31** is provided on the top surface side of the respective end parts of the channel formation region **3***b* and the well region **2**. The region A**2** indicated by the broken line surrounds the surface of the end part of the well region **2**.

[0073] The semiconductor device according to the first embodiment has the configuration in which the impurity concentration of the well region **2** at the positions corresponding to the regions A**2** and A**3** indicated by the broken lines in FIG. **3** to FIG. **5** is regulated to be higher than or equal to that of the well region **2** at the position overlapping with the wiring layer **41** other than the regions A**2** and A**3**. This configuration can avoid a formation of a channel on the surface of the well region **2** at

the positions corresponding to the regions A**2** and A**3** indicated by the broken lines if a potential is applied to the wiring layer **41**, so as to prevent a cause of a leakage path.

<Method of Manufacturing Semiconductor Device>

[0074] An example of a method of manufacturing the semiconductor device according to the first embodiment is described below. The explanations for the manufacturing method according to the present embodiment are made below while focusing on the cross section of the semiconductor device illustrated in FIG. **1**. It should be understood that the method of manufacturing the semiconductor device described below is an example, and the semiconductor device can be manufactured by various methods not disclosed herein including modified examples within the scope of the appended claims.

[0075] First, the p-type semiconductor base-body **1** (refer to FIG. **6**) is prepared. A photoresist film is applied to the top surface of the semiconductor base-body **1**, and is delineated by photolithography. Using the delineated photoresist film as a mask for ion implantation, n-type impurity ions such as phosphorus (P) are implanted so as to form the n-type well region **2**. The photoresist film is then removed.

[0076] Next, a photoresist film is applied to the top surface of the semiconductor base-body **1**, and is delineated by photolithography. Using the delineated photoresist film as a mask for ion implantation, p-type impurity ions such as boron (B) are implanted so as to form the p-type channel formation regions **3***a* to **3***d* and the p-type well region **5**. The photoresist film is then removed.

[0077] Next, a photoresist film is applied to the top surface of the semiconductor base-body **1**, and is delineated by photolithography. Using the delineated photoresist film as a mask for ion implantation, p-type impurity ions such as phosphorus (P) are implanted so as to form the n-type drift regions **4***a* to **4***c*. The photoresist film is then removed. The order of executing the ion implantation for forming the well region **2**, the ion implantation for forming the p-type channel formation regions **3***a* to **3***d* and the p-type well region **5**, and the ion implantation for forming the n-type drift regions **4***a* to **4***c* is not limited to the case described above, and may be changed as appropriate.

[0078] FIG. **6** is a cross-sectional view illustrating regions (ion implantation regions) **2***a* to **2***g*, indicated by the broken lines, to which the n-type impurity ions for forming the n-type well region **2** are implanted. FIG. **7** is a cross-sectional view schematically illustrating, instead of the n-type well region **2**, the ion implantation regions **2***a* to **2***g* illustrated in FIG. **6** superposed on the semiconductor device according to the first embodiment illustrated in FIG. **1**. For example, a single ion implantation region is formed for the provision of the well region **2** until the breakdown voltage reaches about **50** volts, while a plurality of ion implantation regions of n-type impurity ions for the provision of the well region **2** are formed into a slit state when the breakdown voltage is about **60** volts or higher in order to further decrease the impurity concentration of the well region **2**. The implanted n-type impurity ions are then diffused in the lateral direction by annealing, so as to form the single well region **2**.

[0079] As illustrated in FIG. **6** and FIG. **7**, the ion implantation region **2***a* is formed to have a width w**11** at a position overlapping with the channel formation region **3***a*. The ion implantation region **2***b* is formed to have a width w**21** wider than the width w**11** at a position overlapping with the drift region **4***a*. The ion implantation region **2***c* is formed to have a width w**31** narrower than the widths w**11** and w**21** at a position overlapping with the channel formation region **3***b*. The ion implantation region **2***d* is formed to have a width w**22** substantially equal to the width w**21** at a position overlapping with the drift region **4***b*. The ion implantation region **2***e* is formed to have a width w**32** substantially equal to the width w**31** at a position overlapping with the channel formation region **3***c*. The ion implantation region **2***f* is formed to have a width w**23** substantially equal to the widths w**21** and w**22** at a position overlapping with the drift region **4***c*. The ion implantation region **2***g* is formed to have a width w**12** substantially equal to the width w**11** at a position overlapping with the channel formation region **3***d*.

[0080] FIG. **8**A is a plan view, at the phase corresponding to FIG. **6**, schematically illustrating the ion implantation regions **2***a* to **2***d* and **2***x* surrounded by the broken lines and hatched by the right-downward oblique lines. FIG. **8**A also schematically indicates, by the broken lines, ion implantation regions **3***x* to **3***z* for forming the p-type channel formation regions **3***a* and **3***b* and the p-type connection region **3***e*, and an ion implantation region **5***x* for forming the p-type well region **5**. FIG. **8**A also schematically indicates, by the broken lines, the gate electrodes **11***a* to **11***d*, the wiring layer **41**, and the gate wiring layer **42** formed in the process described below.
[0081] The ion implantation regions **2***a* to **2***d* each have a stripe-shaped planar pattern extending in the extending direction of the gate electrodes **11***a* to **11***d* (in the upper-lower direction in FIG. **8**A). The respective end parts of the ion implantation regions **2***a* to **2***d* overlap with the wiring layer **41**.
[0082] The ion implantation region **2***x* is provided to overlap with the wiring layer **41** on the end part side of the ion implantation region **2***c* having the relatively narrow width w**31** among the ion implantation regions **2***a* to **2***d*. The ion implantation region **2***x* has a stripe-shaped planar pattern extending in the direction perpendicular to the extending direction of the ion implantation region **2***c* (in the right-left direction in FIG. **8**A). The ion implantation region **2***x* is connected to the end part of the ion implantation region **2***c*. The arrangement of the ion implantation region **2***x* and the ion implantation region **2***c* provides a T-shaped planar pattern. The ion implantation region **2***x* is separated from the other ion implantation regions **2***b* and **2***d*.
[0083] A length L**1** of the ion implantation region **2***x* in the extending direction can be changed as appropriate within a range that leads the ion implantation region **2***x* to be separated from the ion implantation regions **2***b* and **2***d*. A width w**2** of the ion implantation region **2***x* in the direction perpendicular to the extending direction can also be changed as appropriate. While FIG. **8**A illustrates the case in which the width w**2** of the ion implantation region **2***x* is narrower than the width w**1** of the wiring layer **41**, the width w**2** of the ion implantation region **2***x* may be either equal to or wider than the width w**1** of the wiring layer **41** instead. Further, FIG. **8**A illustrates the case in which the entire ion implantation region **2***x* overlaps with the wiring layer **41**, but the ion implantation region **2***x* may partly overlap with the wiring layer **41**, while the other part of the ion implantation region **2***x* may be located on the outside of the wiring layer **41**.
[0084] The other ion implantation regions **2***e* to **2***g* illustrated in FIG. **6** also have the stripe-shaped planar pattern extending in the extending direction of the gate electrodes **11***a* to **11***d* (in the upper-lower direction in FIG. **8**A), as in the case of the ion implantation regions **2***a* to **2***d*. An ion implantation region similar to the ion implantation region **2***x* is connected to the end part of the ion implantation region **2***e* having the relatively narrow width w**32**. The ion implantation region **5***x* for forming the p-type well region **5**, not hatched by the right-downward oblique lines, has a loop-shaped planar pattern.
[0085] While FIG. **8**A illustrates the ion implantation regions **2***a* to **2***d* and **2***x* hatched by the right-downward oblique lines, FIG. **8**B is a plan view schematically illustrating the ion implantation regions **3***x* to **3***z*, hatched by the right-downward oblique lines, for forming the p-type channel formation regions **3***a* and **3***b* and the p-type connection region **3***e*.
[0086] The ion implantation regions **3***x* and **3***y* each have a stripe-shaped planar pattern extending in the extending direction of the gate electrodes **11***a* to **11***d* (in the upper-lower direction in FIG. **8**B). The ion implantation region **3***z* has a planar pattern including a stripe-shaped part extending in the extending direction of the ion implantation regions **3***x* and **3***y* (in the upper-lower direction in FIG. **8**B) and a stripe-shaped part extending in the direction perpendicular to the extending direction of the ion implantation regions **3***x* and **3***y* (in the right-left direction in FIG. **8**B).
[0087] FIG. **9** is a cross-sectional view taken along line A-A′ in FIG. **8**A and FIG. **8**B. As illustrated in FIG. **9**, the ion implantation regions **3***x* and **3***z* for forming the p-type channel formation region **3***a* and the p-type connection region **3***e* and the ion implantation region **5***x* for forming the p-type well region **5** are provided at the upper part of the semiconductor base-body **1**.
[0088] FIG. **10** is a cross-sectional view taken along line B-B′ in FIG. **8**A and FIG. **8**B. As

illustrated in FIG. **10**, the ion implantation regions **3***y* and **3***z* for forming the p-type channel formation region **3***b* and the p-type connection region **3***e* and the ion implantation region **5***x* for forming the p-type well region **5** are provided at the upper part of the semiconductor base-body **1**. Further, the ion implantation region **2***x* for forming the n-type well region **2** is provided between the respective ion implantation regions **3***y* and **5***x* at the upper part of the semiconductor base-body **1**.

[0089] The p-type impurity ions and the n-type impurity ions implanted to the semiconductor base-body **1** are activated by annealing after the ion implantation for forming the well region **2**, the ion implantation for forming the p-type channel formation regions **3***a* to **3***d* and the p-type well region **5**, and the ion implantation for forming the n-type drift regions **4***a* to **4***c*. This step diffuses the n-type impurity ions in the ion implantation regions **2***a* to **2***g* in the lateral direction, so as to form the single n-type well region **2** on the top surface side of the semiconductor base-body **1**, as illustrated in FIG. **11**. In addition, the p-type channel formation regions **3***a* to **3***d* and the n-type drift regions **4***a* to **4***c* are also formed on the top surface side of the semiconductor base-body **1**. The p-type well region **5** is also formed on the outside of the well region **2** on the top surface side of the semiconductor base-body **1**. FIG. **12** is a cross-sectional view, at the phase corresponding to FIG. **11**, taken along line A-A′ in FIG. **8**A and FIG. **8**B. FIG. **13** is a cross-sectional view, at the phase corresponding to FIG. **11**, taken along line B-B′in FIG. **8**A and FIG. **8**B.

[0090] The annealing for forming the well region **2**, the annealing for forming the channel formation regions **3***a* to **3***d* and the well region **5**, and the annealing for forming the drift regions **4***a* to **4***c* are not necessarily executed collectively, but may be executed independently of each other upon each ion implantation.

[0091] Next, as illustrated in FIG. **14**, the element-separation insulating film **31** is formed on the top surface side of the semiconductor base-body **1** by LOCOS, for example. Next, a gate insulating film is formed on the top surface side of the semiconductor base-body **1** by thermal oxidation or chemical vapor deposition (CVD), for example. Further, a polysilicon layer (a doped polysilicon layer) heavily doped with n-type impurities or p-type impurities is provided by CVD using dopant gas. The doped polysilicon layer and the gate insulating film are then partly and selectively removed by photolithography and dry etching so as to form the gate insulating films **10***a* to **10***f* and the gate electrodes **11***a* to **11***f* (refer to FIG. **15**). Subsequently, the side-wall insulating films **12***a* to **12***f* are formed on both sides of the respective side surfaces of the gate electrodes **11***a* to **11***f* by CVD and dry etching. This step provides the gate electrodes **11***a* to **11***f* on the top surface side of the semiconductor base-body **1** with the gate insulating films **10***a* to **10***f* interposed, and the side-wall insulating films **12***a* to **12***f* are formed on both sides of the respective side surfaces of the gate electrodes **11***a* to **11***f*, as illustrated in FIG. **15**.

[0092] Next, the n.sup.+-type source regions **8***a* to **8***d* and the p.sup.+-type contact regions **7***a* to **7***d* are formed on the top surface side of the channel formation regions **3***a* to **3***d* by photolithography, ion implantation, and annealing, as illustrated in FIG. **16**. Further, the n.sup.+-type drain regions **9***a* to **9***c* are formed on the top surface side of the drift regions **4***a* to **4***c*. Further, the p.sup.+-type contact region **6** is formed on the top surface side of the well region **5**.

[0093] Next, the interlayer insulating film **32** is deposited so as to cover the gate electrodes **11***a* to **11***f* by CVD, for example. A part of the interlayer insulating film **32** is then selectively removed by photolithography, dry etching, and the like, so as to form contact holes to which the respective top surfaces of the source regions **8***a* to **8***d*, the drain regions **9***a* to **9***c*, the contact regions **7***a* to **7***d*, and the contact region **6** are exposed. Next, the contact holes are filled with a metal film by sputtering, photolithography, and dry etching, for example, so as to form the vias **21***a*, **22***a*, **22***b*, **23***a*, **24***a* to **24***c*, **25***a*, **26***a* to **26***c*, **27***a*, **28***a*, **28***b*, and **29***a*, the substrate contact electrodes **21** and **29**, the source electrodes **22**, **24**, **26**, and **28**, and the drain electrodes **23**, **25**, and **27**. Thereafter, the passivation insulating film **33** is formed so as to cover the substrate contact electrodes **21** and **29**, the source electrodes **22**, **24**, **26**, and **28**, and the drain electrodes **23**, **25**, and **27**. The semiconductor device according to the first embodiment illustrated in FIG. **1** is thus completed.

[0094] A semiconductor device of a first comparative example is described below. FIG. **17** is a cross-sectional view illustrating the semiconductor device of the first comparative example. As illustrated in FIG. **17**, the semiconductor device of the first comparative example differs from the semiconductor device according to the first embodiment illustrated in FIG. **1** in including a lateral MOSFET not having an arrayed structure. The semiconductor device of the first comparative example includes a semiconductor base-body **101** of p-type, and a well region **102** of n-type provided on the top surface side of the semiconductor base-body **101**. The semiconductor device of the first comparative example further includes channel formation regions **103***a* and **103***b* of p-type on the top surface side of the well region **102**.

[0095] A contact region **107***a* of p.sup.+-type and a source region **108***a* of n.sup.+-type are provided on the top surface side of the channel formation region **103***a*. The contact region **107***a* is connected to a source electrode **122** through a via **122***a* penetrating an interlayer insulating film **132**. The source region **108***a* is connected to the source electrode **122** through a via **122***b* penetrating the interlayer insulating film **132**. The source electrode **122** is covered with a passivation insulating film **133**.

[0096] A drift region **104** of n-type is provided in the middle on the top surface side of the well region **102**. A drain region **109** of n.sup.+-type is provided on the top surface side of the drift region **104**. The drain region **109** is connected to a drain electrode **123** through a via **123***a* penetrating the interlayer insulating film **132**. An element-separation insulating film **131** is provided on both sides of the respective side surfaces of the drift region **104** and the drain region **109**.

[0097] A gate electrode **111***a* is provided on the respective top surface sides of the channel formation region **103***a* and the well region **102** with a gate insulating film **110***a* interposed at a position between the source region **108***a* and the drain region **109**. A side-wall insulating film **112***a* is provided to cover the side surfaces on both sides of the gate electrode **111***a*.

[0098] A source region **108***b* of n.sup.+-type and a contact region **107***b* of p.sup.+-type are provided on the top surface side of the channel formation region **103***b*. The source region **108***b* is connected to a source electrode **124** through a via **124***a* penetrating the interlayer insulating film **132**. The contact region **107***b* is connected to the source electrode **124** through a via **124***b* penetrating an interlayer insulating film **132**.

[0099] A gate electrode **111***b* is provided on the respective top surface sides of the channel formation region **103***b* and the well region **102** with a gate insulating film **110***b* interposed at a position between the drain region **109** and the source region **108***b*. A side-wall insulating film **112***b* is provided to cover the side surfaces on both sides of the gate electrode **111***b*.

[0100] A transistor cell T**11** includes the contact region **107***a*, the source region **108***a*, the drain region **109**, and the gate electrode **111***a*. A transistor cell T**12** has a linear symmetric structure with respect to the transistor cell T**11** about the drain region **109**. The transistor cell T**12** includes the contact region **107***b*, the source region **108***b*, the drain region **109**, and the gate electrode **111***b*. The drain region **109** is commonly used in the respective transistor cells T**11** and T**12**.

[0101] A well region **105** of p-type is provided on the top surface side of the semiconductor base-body **101** on the outside of the well region **102**. A contact region **106** of p.sup.+-type is provided on the top surface side of the well region **105**. The contact region **106** is connected to a substrate contact electrode **121** through a via **121***a* penetrating the interlayer insulating film **132**. The element-separation insulating film **131** is provided on both sides of the respective side surfaces of the well region **105** and the contact region **106**.

[0102] FIG. **18** is a cross-sectional view schematically illustrating, instead of the n-type well region **102** illustrated in FIG. **17**, ion implantation regions **102***a* to **102***c* for forming the well region **102** during the manufacture of the semiconductor device of the first comparative example. The ion implantation region **102***a* is formed to have a width w**41** so as to overlap with the channel formation region **103***a*. The ion implantation region **102***b* is formed to have a width w**42** wider than the width w**41** so as to overlap with the drift region **104**. The ion implantation region **102***c* is

formed to have a width w**43** substantially equal to the width w**41** so as to overlap with the channel formation region **103***b*.

[0103] As compared with this comparative example, the semiconductor device according to the first embodiment has the configuration, as illustrated in FIG. **6** and FIG. **7**, in which the widths w**31** and w**32** of the ion implantation regions **2***c* and **2***e*, among the ion implantation regions **2***a* to **2***f*, located at the positions overlapping with the channel formation regions **3***b* and **3***c* are narrower than the widths w**41** to w**43** of the ion implantation regions **102***a* to **102***c* in the semiconductor device of the first comparative example. This configuration avoids the sufficient diffusion of the n-type impurities included in the ion implantation regions **2***c* and **2***e* in the lateral direction by the annealing, which leads a region having a low impurity concentration to be locally formed in the well region **2**.

[0104] A semiconductor device of a second comparative example is described below. The semiconductor device of the second comparative example has a configuration common to that of the semiconductor device according the first embodiment in including the lateral MOSFET having the arrayed structure. FIG. **19** is a plan view for explaining a method of manufacturing the semiconductor device of the second comparative example, corresponding to the plan view for explaining the method of manufacturing the semiconductor device according to the first embodiment illustrated in FIG. **8**A.

[0105] The method of manufacturing the semiconductor device of the second comparative example also forms the ion implantation regions **2***a* to **2***d* in the ion implantation step for forming the n-type well region **2**, but differs from the method of manufacturing the semiconductor device according to the first embodiment illustrated in FIG. **8**A in not forming the ion implantation region **2***x* connected to the ion implantation region **2***c*, as illustrated in FIG. **19**.

[0106] FIG. **19** indicates a region A**1** by the broken line at a position corresponding to the end part of the gate electrode **11***a* and the end part of the well region **2** immediately under the wiring layer **41**. FIG. **19** also indicates a region A**2** by the broken line at a position corresponding to the end part of the gate electrode **11***b* and the end part of the well region **2** immediately under the wiring layer **41**. FIG. **19** also indicates a region A**3** by the broken line at a position corresponding to the end part of the gate electrode **11***c* and the end part of the well region **2** immediately under the wiring layer **41**.

[0107] The semiconductor device of the second comparative example can lead the n-type impurities to be sufficiently diffused in the lateral direction by the annealing, since the ion implantation regions **2***a*, **2***b*, and **2***d* each have a greater width than the ion implantation region **2***c*. The impurity concentration at the end part of the well region **2**, corresponding to the region A**1** indicated by the broken line, between the ion implantation regions **2***a* and **2***b* is not decreased, or no channel is formed on the surface of the end part of the well region **2** even immediately under the wiring layer **41**.

[0108] On the other hand, the ion implantation region **2***c*, which is narrower than the ion implantation regions **2***a*, **2***b*, and **2***d*, does not lead the n-type impurities to be diffused sufficiently in the lateral direction by the annealing. The impurity concentration at the end part of the well region **2**, corresponding to the region A**2** indicated by the broken line between the ion implantation regions **2***b* and **2***c*, is thus lower than that of the well region **2** at the position corresponding the region A**1** indicated by the broken line. Further, the impurity concentration at the end part of the well region **2**, corresponding to the region A**3** indicated by the broken line between the ion implantation regions **2***c* and **2***d*, is also lower than that at the position corresponding the region A**1** indicated by the broken line. A channel is thus formed on the surface of the well region **2** at the respective positions with the relatively low impurity concentration corresponding to the regions A**2** and A**3** indicated by the broken lines if a potential is applied to the wiring layer **41**, resulting in a cause of a leakage path.

[0109] In contrast, the method of manufacturing the semiconductor device according to the first

embodiment includes the ion implantation step for forming the well region **2** that forms the ion implantation region **2***x* on the end part side of the ion implantation region **2***c* having the narrower width than the ion implantation regions **2***a*, **2***b*, and **2***d*, as illustrated in FIG. **8**A. The impurity concentration at the end part of the well region **2**, corresponding to the region A**2** indicated by the broken line between the ion implantation regions **2***b* and **2***c*, is thus higher than or equal to that of the well region **2** at the position indicated by the region A**1**. In addition, the impurity concentration at the end part of the well region **2**, corresponding to the region A**3** indicated by the broken line between the ion implantation regions **2***c* and **2***d*, is also higher than or equal to that of the well region **2** at the position indicated by the region A**1**. The configuration of the semiconductor device according to the first embodiment thus can avoid a formation of a channel on the surface of the well region **2** at the positions indicated by the regions A**2** and A**3**, so as to prevent a cause of a leakage path accordingly.

SECOND EMBODIMENT

[0110] FIG. **20** is a plan view for explaining a method of manufacturing a semiconductor device according to a second embodiment, corresponding to the plan view for explaining the manufacturing method according to the first embodiment illustrated in FIG. **8**A. As illustrated in FIG. **20**, the method of manufacturing the semiconductor device according to the second embodiment differs from the manufacturing method according to the first embodiment illustrated in FIG. **8**A in forming the ion implantation region **2***x* separately from the ion implantation region **2***c* in the ion implantation step for forming the n-type well region **2**. The other steps of the method of manufacturing the semiconductor device according to the second embodiment are substantially the same as those according to the first embodiment, and overlapping explanations are not repeated below.

[0111] The method of manufacturing the semiconductor device according to the second embodiment that provides the ion implantation region **2***x*, as in the case according to the first embodiment, can also prevent a decrease in the impurity concentration of the well region **2** at the positions corresponding the regions A**2** and A**3** indicated by the broken lines in FIG. **3** to FIG. **5**. The present embodiment thus can avoid a formation of a channel on the surface of the well region **2** at the positions indicated by the regions A**2** and A**3** if a potential is applied to the wiring layer **41**, so as to prevent a cause of a leakage path accordingly.

THIRD EMBODIMENT

[0112] FIG. **21** is a plan view for explaining a method of manufacturing a semiconductor device according to a third embodiment, corresponding to the plan view for explaining the manufacturing method according to the first embodiment illustrated in FIG. **8**A. As illustrated in FIG. **21**, the method of manufacturing the semiconductor device according to the third embodiment differs from the manufacturing method according to the first embodiment illustrated in FIG. **8** in forming ion implantation regions **2***y* and **2***z* separately from the ion implantation region **2***c* in the ion implantation step for forming the n-type well region **2**. The ion implantation regions **2***y* and **2***z* are provided separately from each other. The other steps of the method of manufacturing the semiconductor device according to the third embodiment are substantially the same as those according to the first embodiment, and overlapping explanations are not repeated below.

[0113] The method of manufacturing the semiconductor device according to the third embodiment, which provides the ion implantation regions **2***y* and **2***z*, can also prevent a decrease in the impurity concentration of the well region **2** at the positions corresponding the regions A**2** and A**3** indicated by the broken lines in FIG. **3** to FIG. **5**, as in the case according to the first embodiment. The present embodiment thus can avoid a formation of a channel on the surface of the well region **2** at the positions indicated by the regions A**2** and A**3** if a potential is applied to the wiring layer **41**, so as to prevent a cause of a leakage path accordingly.

OTHER EMBODIMENTS

[0114] As described above, the invention has been described according to the first to third

embodiments, but it should not be understood that the description and drawings implementing a portion of this disclosure limit the invention. Various alternative embodiments of the present disclosure, examples, and operational techniques will be apparent to those skilled in the art from this disclosure.

[0115] For example, the first to third embodiments each illustrate the method of manufacturing the semiconductor device with the configuration in which the ion implantation regions **2***c* and **2***e* located at the positions overlapping with the channel formation regions **3***b* and **3***c* have the relatively narrow widths among the ion implantation regions **2***a* to **2***g*, as illustrated in FIG. **7**, but the present disclosure is not limited to this case. The ion implantation regions **2***b*, **2***d*, and **2***f* overlapping with the drift regions **4***a* to **4***c* may each have a relatively narrow width. In such a case, an ion implantation region similar to the ion implantation region **2***x* as illustrated in FIG. **8**A may be formed on the end part side of the respective ion implantation regions **2***b*, **2***d*, and **2***f* with the relatively narrow width.

[0116] Further, the semiconductor devices according to the first to third embodiments are illustrated with the lateral MOSFET, but the present disclosure can also be applied to a lateral IGBT.

[0117] In addition, the respective configurations disclosed in the first to third embodiments can be combined together as appropriate without contradiction with each other. As described above, the invention includes various embodiments of the present disclosure and the like not described herein. Therefore, the scope of the present disclosure is defined only by the technical features specifying the present disclosure, which are prescribed by claims, the words and terms in the claims shall be reasonably construed from the subject matters recited in the present specification.

Claims

1. A semiconductor device comprising: a semiconductor base-body of a first conductivity-type; a well region of a second conductivity-type provided on a top surface side of the semiconductor base-body; a plurality of channel formation regions of the first conductivity-type provided on a top surface side of the well region and extending parallel to each other in one direction in a planar view; a plurality of drift regions provided on the top surface side of the well region alternately with the channel formation regions and extending parallel to each other in the one direction; a plurality of carrier-supply regions of the second conductivity-type provided on top surface sides of the respective channel formation regions; a plurality of carrier-reception regions of the second conductivity-type provided on top surface sides of the respective drift regions; a plurality of gate electrodes provided on top surface sides of the respective channel formation regions with a gate insulating film interposed at positions between the carrier-supply regions and the well region, and extending parallel to each other in the one direction; and a wiring layer arranged over the well region on an end part side of the channel formation regions and the drift regions in the one direction to extend in a direction perpendicular to the one direction, wherein an impurity concentration of the well region at a position located on the end part side of the channel formation regions interposed between the drift regions next to each other and overlapping with the wiring layer is greater than or equal to that of the well region at a position on the end part side of the drift regions and overlapping with the wiring layer.

2. The semiconductor device of claim 1, further comprising a plurality of transistor cells, wherein two of the transistor cells each including one of the gate electrodes located next to each other commonly use one of the carrier-supply regions and have a linearly symmetric structure about the common carrier-supply region.

3. The semiconductor device of claim 1, further comprising a plurality of transistor cells, wherein two of the transistor cells each including one of the gate electrodes located next to each other commonly use one of the carrier-reception regions and have a linearly symmetric structure about

the common carrier-reception region.

4. A method of manufacturing the semiconductor device according to claim 1, the method comprising forming the well region including: implanting impurity ions of the second conductivity-type to form a plurality of first ion implantation regions formed into slits extending parallel to the one direction and having different widths, and form a second ion implantation region extending in the direction perpendicular to the one direction at a position overlapping with the wiring layer on an end part side of one of the first ion implantation regions having a relatively narrow width; and diffusing the impurity ions implanted to the first ion implantation regions and the second ion implantation region in a lateral direction by annealing so as to form the well region.

5. The method of manufacturing the semiconductor device of claim 4, wherein the one of the first ion implantation regions having the relatively narrow width is provided at a position overlapping with one of the channel formation regions interposed between the drift regions next to each other.

6. The method of manufacturing the semiconductor device of claim 4, wherein the second ion implantation region is formed so as to be connected to an end part of the one of the first ion implantation regions having the relatively narrow width.

7. The method of manufacturing the semiconductor device of claim 4, wherein the second ion implantation region is formed separately from the end part of the one of the first ion implantation regions having the relatively narrow width.

8. The method of manufacturing the semiconductor device of claim 4, wherein the step of forming the well region forms a plurality of the second ion implantation regions separately from each other in the direction perpendicular to the one direction.