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Multi-Source Inverter and Modulation Schemes Therefor

Abstract

A multi-source inverter (MSI) topology features significant advantages over conventional MSI converters such as NPC-based and T-Type-based topologies, including a lower number of switching devices, higher efficiency, and better thermal distribution of switching devices. A space vector modulation (SVM) scheme for MSI topologies presented herein and for conventional MSI topologies uses three or four adjacent vectors to generate a reference voltage vector, resulting in lower voltage and current total harmonic distortion (THD) at the MSI output, a lower switching frequency, and increased efficiency relative to conventional MSI modulation. Embodiments are suitable for use in electric vehicles and energy storage systems.

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Background/Summary

RELATED APPLICATION [0001] This application claims the benefit of the filing date of Application No. 63/551,337, filed on Feb. 8, 2024, the contents of which are incorporated herein by reference in their entirety.

FIELD
[0002] The invention relates to topologies and modulation schemes that improve performance and reduce size and cost of multi-source inverters.
BACKGROUND
[0003] A multi-source inverter (MSI) is a power converter that connects distinct DC sources to the same AC output using a single conversion stage. The use of multi-source inverters as a new generation of traction inverters in electric vehicles has been proposed [2]-[3]. In an electric vehicle (EV), a multi-source inverter allows independent DC sources to drive the propulsion motor while simultaneously using the battery voltage as one DC voltage link. This topology can be applied to hybrid electric vehicle (HEV) and plug-in hybrid electric vehicle (PHEV) powertrains, where the input is directly connected to the battery pack and the DC-link voltage is shared between both inverters, as shown in FIG. **1** [3]. This enables the battery pack to transfer power directly to the traction motor without requiring a DC/DC converter to step up the voltage. In addition, the high-power DC/DC converter can be dissociated from the traction mode and only used for starting the internal combustion engine (ICE) and for regenerative braking. Further, unlike conventional hybrid powertrains, the battery and the DC/DC converter are connected in parallel. As a result, the DC/DC converter can be bypassed in traction mode. This allows its power rating to be reduced from tens of kW to a few kW without degrading the battery system. Having only a single conversion stage between the battery and motor also improves the overall efficiency of an electrified traction drive.
[0004] A combination of input voltage sources can be applied to the load using a multi-source inverter. In this regard, different DC storage devices can feed the same AC load through a single-stage magnetic-less DC/AC power conversion. These structures improve the overall volume, weight, and efficiency of the system due to the elimination of the magnetics from the circuit. Moreover, MSI circuits introduce a high degree of freedom for the selection and integration of storage devices with complementary characteristics to satisfy the load requirements based on the load features. From the voltage source inverter point of view, the DC link voltage of an MSI is not fixed. In other words, a combination of input voltage sources can be applied to the load as the load reference voltage or current changes. This way, improved efficiency performance can be achieved for the hybrid energy storage system (HESS). Moreover, in EV applications, the efficiency of the electric motor is compromised at low speeds where the value of the modulation index is very small. However, in an MSI topology, this voltage is not fixed. Thus, a combination of different voltage amplitudes can be applied to the electric motor based on the value of the reference speed, which improves the performance of the electric motor in comparison with traditional systems.
[0005] FIG. **2** shows the prior topology with two DC inputs V.sub.DC1 and V.sub.DC2 connected between (O) and (P.sub.1) and (O) and (P.sub.2). When the multi-source inverter is applied to hybrid powertrains, the DC-link voltage V.sub.DC1 is shared with the other inverter while V.sub.DC2 is supplied by a battery pack. By replacing the ideal switches in FIG. **2** with insulated gate bipolar transistors (IGBTs), two circuits can be used to realize the multi-source inverter and are very similar to three-level inverters, namely the neutral point clamped (NPC) and T-NPC topologies (see FIG. **3**).
[0006] The MSI has been studied for use in the powertrain of certain hybrid vehicles for the purpose of reducing the power rating of the DC/DC converter between the storage systems and the high voltage DC link. The same topology is used in [3] for active control of the battery/super

capacitor combination. This topology is based on the neutral point clamped three-level inverter structure. A study of the functionality of the same topology as an AC/DC rectifier in the regenerative braking mode for EV applications has been reported in [3]. Despite the positive operational benefits of this topology, practical issues of the neutral point clamped converter, including the need for high-power switching devices, loss balancing, and thermal cycling of the switching devices limit its application in EVs.

SUMMARY

[0007] According to one aspect of the invention there is provided a modulation scheme for a three-phase multi-source inverter (MSI), comprising: defining a stationary αβ plan of the three-phase voltages comprising six sectors I to VI, wherein each sector has seven existing space voltage vectors; defining V.sub.ref as a three-phase reference voltage vector in the αβ plan; for each sector, calculating new space voltage vectors V.sub.M, V.sub.S, and V.sub.R as linear combinations of at least two of the existing space voltage vectors; dividing each sector into nine operating regions; generating switching signals for switching devices of the MSI in each operating region in each sector using the V.sub.ref, selected new space voltage vectors, and selected existing space voltage vectors.

[0008] In one embodiment the generating switching signals comprises using four selected existing space voltage vectors.

[0009] In one embodiment the four selected existing space voltage vectors include V.sub.3-V.sub.6.

[0010] In one embodiment the modulation scheme comprises: calculating the new space voltage vectors for one sector selected from sectors I to VI; determining corresponding new space voltage vectors in other sectors by interchanging the new space voltage vectors determined for the selected sector.

[0011] According to another aspect of the invention there is provided a controller for a three-phase MSI, comprising: a processor; non-transitory computer readable media storing an algorithm that directs the processor to implement a space vector modulation (SVM) scheme for the MSI; an output circuit that outputs switching signals to switches of the MSI according to the SVM scheme; wherein the SVM scheme comprises: defining a stationary αβ plan of the three-phase voltages comprising six sectors I to VI, wherein each sector has seven existing space voltage vectors; defining V.sub.ref as a three-phase reference voltage vector in the αβ plan; for each sector, calculating new space voltage vectors V.sub.M, V.sub.S, and V.sub.R as linear combinations of at least two of the existing space voltage vectors; dividing each sector into nine operating regions; generating switching signals for switching devices of the MSI in each operating region in each sector using the V.sub.ref, selected new space voltage vectors, and selected existing space voltage vectors.

[0012] The controller may be implemented in an electric vehicle.

[0013] According to another aspect of the invention there is provided a three-phase multi-source inverter (MSI), comprising: a first switch having an input terminal adapted to receive a positive side of a first DC source (V.sub.DC1); a second switch having an input terminal adapted to receive a negative side of the first DC source (V.sub.DC1) and a negative side of a second DC source (V.sub.DC2); an output of the first switch connected to inputs of third, fifth, seventh, and ninth switches; the third switch having an output terminal adapted to receive a positive side of the second DC source (V.sub.DC2) and connected to an input of a fourth switch; outputs of the fifth, seventh, and ninth switches connected to inputs of sixth, eighth, and tenth switches and to output nodes corresponding to respective MSI three-phase output currents i.sub.a, i.sub.b, and i.sub.c; outputs of the second, fourth, sixth, eighth, and tenth switches connected together.

[0014] One embodiment comprises at least one DC-DC converter that provides the first DC source or the second DC source.

[0015] In one embodiment the first DC source comprises a high voltage source and the second DC source comprises a low voltage source.

[0016] In one embodiment the first DC source comprises a high voltage source and the second DC source comprises a battery, a super capacitor, or an ultra capacitor.
[0017] In one embodiment the three-phase MSI may be configured for use in an electric vehicle.
[0018] In one embodiment the three-phase MSI may comprise a controller.
[0019] In one embodiment the controller controls switches of the MSI according to a space vector modulation (SVM) scheme.
[0020] In one embodiment the SVM scheme comprises: defining a stationary αβ plan of the three-phase voltages comprising six sectors I to VI, wherein each sector has seven existing space voltage vectors; defining V.sub.ref as a three-phase reference voltage vector in the αβ plan; for each sector, calculating new space voltage vectors V.sub.M, V.sub.S, and V.sub.R as linear combinations of at least two of the existing space voltage vectors; dividing each sector into nine operating regions; generating switching signals for switching devices of the MSI in each operating region in each sector using the V.sub.ref, selected new space voltage vectors, and selected existing space voltage vectors.
[0021] In one embodiment the three-phase MSI may be configured for use in an electric vehicle.
[0022] According to another aspect of the invention there is provided a three-phase MSI comprising a controller, wherein the controller controls switches of the MSI according to a space vector modulation (SVM) scheme as described herein. In one embodiment the three-phase MSI comprising a controller may be configured for use in an electric vehicle.
[0023] According to another aspect of the invention there is provided a non-transitory computer readable media compatible with a processor, the non-transitory computer readable media storing an algorithm that directs the processor to implement a space vector modulation (SVM) scheme for an MSI; wherein the SVM scheme comprises: defining a stationary αβ plan of the three-phase voltages comprising six sectors I to VI, wherein each sector has seven existing space voltage vectors; defining V.sub.ref as a three-phase reference voltage vector in the αβ plan; for each sector, calculating new space voltage vectors V.sub.M, V.sub.S, and V.sub.R as linear combinations of at least two of the existing space voltage vectors; dividing each sector into nine operating regions; generating switching signals for switching devices of the MSI in each operating region in each sector using the V.sub.ref, selected new space voltage vectors, and selected existing space voltage vectors.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0024] For a greater understanding of the invention, and to show more clearly how it may be carried into effect, embodiments will be described, by way of example, with reference to the accompanying drawings, wherein:
[0025] FIG. **1** is a block diagram of a hybrid powertrain with a multi-source inverter suitable for use in a hybrid electric vehicle, according to the prior art.
[0026] FIG. **2** is a diagram of a multi-source inverter topology showing three operating modes, according to the prior art.
[0027] FIG. **3** is a schematic diagram of a multi-source inverter based on an NPC topology, according to the prior art.
[0028] FIG. **4** is a schematic diagram of a multi-source inverter, according to one embodiment.
[0029] FIG. **5** is a schematic diagram of a multi-source inverter, according to one embodiment.
[0030] FIG. **6** is a space vector plan of a multi-source inverter.
[0031] FIG. **7** is a voltage space vector diagram of sector I of a multi-source inverter.
[0032] FIG. **8** is a diagram defining new space vectors in sector I.
[0033] FIG. **9** is a diagram showing the regions in sector I.

[0034] FIGS. **10**A-**10**C are plots of conduction loss, switching loss, and efficiency, respectively, of multi-source inverters according to an embodiment and according to the prior art, under a modulation scheme according to an embodiment and a conventional modulation scheme.
[0035] FIGS. **11**A-**11**C are plots of experimental results of a multi-source inverter according to an embodiment operating in mode I, wherein (A) is line voltage, (B) is load currents, and (C) is DC currents (lower: DC source current, upper: UC current).
[0036] FIGS. **12**A-**12**C are plots of experimental results of a multi-source inverter according to an embodiment for a transition from operating mode I to operating mode II, wherein (A) is line voltage, (B) is load currents, and (C) is DC currents (upper: DC source current, lower: UC current).
[0037] FIGS. **13**A-**13**C are plots of experimental results of a multi-source inverter according to an embodiment operating in mode III, wherein (A) is line voltage, (B) is load currents, and (C) is DC currents (upper: DC source current, lower: UC current).
[0038] FIGS. **14**A-**14**C are plots of experimental results of a multi-source inverter according to an embodiment for a load step change from full load to 20% of full load, wherein (A) is line voltage, (B) is load currents, and (C) is DC currents (upper: DC source current, lower: UC current).

DETAILED DESCRIPTION OF EMBODIMENTS

MSI Topology

[0039] Described herein is a hybrid MSI topology that features significant advantages over conventional state-of-the-art converters such as NPC-based and T-Type-based topologies, including: [0040] Lower number of switching devices, [0041] Higher efficiency, [0042] Simple hardware design and packaging, [0043] Lower cost, volume, and weight, [0044] Better thermal distribution of switching devices.
[0045] Embodiments are suitable for applications such as, but not limited to, an electric vehicle, examples of which may include a battery electric vehicle (BEV), hybrid electric vehicle (HEV), and plug-in hybrid electric vehicle (PHEV), all of which are referred to herein generally as an electric vehicle (EV), and other applications such as a hybrid energy storage system (HESS).
[0046] An embodiment will be described in detail with reference to the MSI topology shown in FIG. **4**. Referring to FIG. **4**, the embodiment includes inputs for first and second DC-link voltages, V.sub.DC1 and V.sub.DC2. For example, V.sub.DC1 may be a battery and V.sub.DC22 may be the output of a DC-DC converter. Switching pairs (T.sub.1, T.sub.2), and (T.sub.3, T.sub.4) operate in a complementary manner to prevent short circuit of the input DC-links. Output currents i.sub.a, i.sub.b, and i.sub.c, respectively produced at the node between switches S.sub.1, S.sub.2, switches S.sub.3, S.sub.4, and switches S.sub.5, S.sub.6, are delivered to the electric motor. Table 1 indicates switching states of the MSI topology, according to one embodiment. In Table I the switching functions 0 and 1 indicate that the switch is turned off and turned on, respectively.
[0047] As shown in FIG. **5**, in one embodiment the topology may be implemented as a multi-source converter utilizing a high-voltage DC source with the voltage rating of V.sub.DC1 and a second DC source having the voltage rating of V.sub.DC2 as the two DC-links. V.sub.DC2 may be, for example, a low-voltage battery pack or a super capacitor (SC) bank to handle the high number of charge/discharge modes in a typical driving cycle of an EV. In one embodiment the converter may be operated according to a modulation scheme to generate a voltage waveform with a peak-to-peak amplitude of DC link voltage with a desired fundamental frequency. In one embodiment there are three different values for discrete adjustable DC-link voltages, namely, V.sub.DC1, V.sub.DC2, and the subtraction of the two sources which is V.sub.DC1-V.sub.DC2.
[0048] By selecting different values of the discrete DC links, embodiments of the MSI may be operated in three DC/AC conversion modes where different combinations of the input DC sources may be connected to the load. For example:
[0049] 1) Mode I: The load is supplied by the source V.sub.DC2 and the source V.sub.DC1 is not used. Due to the smaller amplitude of the source V.sub.DC2, this mode is appropriate for light loads with small power/voltage requirements.

[0050] 2) Mode II: The two DC sources are connected in differential series connection and the value of DC-link voltage is equal to V.sub.DC1-V.sub.DC2. With the positive current idc1, the source V.sub.DC1 supplies the load and simultaneously charges the source V.sub.DC2. This mode may be used for cases where the state of charge (SOC) of the second DC source is less than a certain level or the load requires more power/voltage in comparison to Mode I.
[0051] 3) Mode III: The load is supplied by the source V.sub.DC1 and the source V.sub.DC2 is not used. Since the voltage of the first DC link is essentially selected to be higher than V.sub.DC2 and V.sub.DC1-V.sub.DC2, this mode may be selected for loads that require higher power/voltage values than Mode 1 and Mode II.
TABLE-US-00001 TABLE 1 Switching States of MSI Topology in Various Operating Modes States of Switches Line-to-Line Voltages Mode T.sub.1 T.sub.3 S.sub.1 S.sub.2 S.sub.3 V.sub.AB V.sub.BC V.sub.CA I 0 1 1 1 1 0 0 0 1 1 0 0 V.sub.DC2 −V.sub.DC2 1 0 1 V.sub.DC2 −V.sub.DC2 0 1 0 0 V.sub.DC2 0 −V.sub.DC2 0 1 1 −V.sub.DC2 0 V.sub.DC2 0 1 0 −V.sub.DC2 V.sub.DC2 0 0 0 1 0 −V.sub.DC2 V.sub.DC2 0 0 0 0 0 0 II 1 0 1 1 1 0 0 0 1 1 0 0 V.sub.DC1 − V.sub.DC2 −V.sub.DC1 + V.sub.DC2 1 0 1 V.sub.DC1 − V.sub.DC2 −V.sub.DC1 + V.sub.DC2 0 1 0 0 V.sub.DC1 − V.sub.DC2 0 −V.sub.DC1 + V.sub.DC2 0 1 1 −V.sub.DC1 + V.sub.DC2 0 V.sub.DC1 − V.sub.DC2 0 1 0 −V.sub.DC1 + V.sub.DC2 V.sub.DC1 − V.sub.DC2 0 0 0 1 0 −V.sub.DC1 + V.sub.DC2 V.sub.DC1 − V.sub.DC21 0 0 0 0 0 0 III 1 1 1 1 1 0 0 0 1 1 0 0 V.sub.DC1 −V.sub.DC1 1 0 1 V.sub.DC1 −V.sub.DC1 0 1 0 0 V.sub.DC1 0 −V.sub.DC1 0 1 1 −V.sub.DC1 0 V.sub.DC1 0 1 0 −V.sub.DC1 V.sub.DC1 0 0 0 1 0 −V.sub.DC1 V.sub.DC1 0 0 0 0 0 0
MSI Modulation
[0052] High-frequency modulation schemes may be utilized for synthesis of desired reference voltages at the AC side of a voltage-source converter. Space vector modulation (SVM) is an enhanced PWM scheme that offers several degrees of freedom for reference voltage generation in three-phase voltage source converters. SVM provides better utilization of the DC-link voltage and reduces THD as well as switching losses.
[0053] Described herein is a SVM method for controlling switches of multisource inverters. Embodiments may use three or four adjacent vectors to generate a reference voltage vector, in contrast to conventional SVM approaches in multi-source inverters that synthesize the reference voltage vector from two active vectors and one zero vector. A comparison of a MSI voltage waveform resulting from a modulation strategy embodiment as described herein to that using a conventional SVM approach showed that the voltage waveform of the embodiment provides a multi-level waveform scheme which decreases voltage and current total harmonic distortion (THD) at the output of the MSI relative to the conventional approach. In addition, a modulation scheme as described herein results in a substantial reduction in switching frequency. As a result, MSI efficiency is significantly increased at different operating points.
[0054] Embodiments provide SVM schemes for multi-source inverters that generate appropriate switching signals at various operating modes to achieve the above-mentioned advantages. FIG. **6** shows the voltage vectors resulting from the switching states of three operating modes of the MSI. The set of balanced three-phase reference voltages in the abc frame are transformed into a two-dimensional complex frame by the following transformation.

$$[00001]\quad \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = \frac{2}{3} \times \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_{An} \\ v_{Bn} \\ v_{Cn} \end{bmatrix} \quad (1)$$

where v.sub.an, v.sub.bn, and v.sub.cn are the three-phase voltages in the abc frame, and v.sub.α and v.sub.β are the resultant voltages in the stationary αβ plan. Applying the transformation to the output phase voltages of operating modes results in a set of switching voltage vectors that establish a three-layer hexagon centered at the origin of the αβ plan. Each hexagon includes six non-zero space voltage vectors and two zero vectors. Therefore, there are 18 non-zero voltage vectors in the

αβ plan and six zero voltage vectors located at the origin of the αβ plan. The αβ plan is split up to six symmetric sectors shown by I to VI in FIG. **6**.

[0055] The sector I of the corresponding αβ plan is shown in FIG. **7**, where the voltage vectors at each vertex are shown with [l.sub.a l.sub.b l.sub.c]. l.sub.a, l.sub.b, and l.sub.c represent the generated voltage level of the phases a, b, and c, respectively. The voltage levels 0 and 1 correspond to the output voltages 0 and V.sub.dc relative to the negative DC-link of the VSI, respectively. As shown in FIG. **6**, the reference voltage vector V.sub.ref represents the three-phase reference voltages in the αβ plan. In a balanced three-phase system, V.sub.ref has a constant magnitude of |V.sub.ref| and rotates counterclockwise at an angular frequency of ω. The modulation index is defined as follows:

[00002] $M = \frac{2 \text{ .Math. } V_{ref} \text{ .Math.}}{\sqrt{3}V_{dc1}}$ (2) .Math. V_{ref} .Math. $= \sqrt{v^2 + v^2}$ (3)

[3]-[6] The operating modes can be determined based on the magnitude of V.sub.ref. As can be seen in FIG. **6**, the maximum magnitude of V.sub.ref in each hexagon is equal to the radius of the biggest inscribed circle. The appropriate operating mode is determined based on the |V.sub.ref| as follows:

[00003] $$\begin{cases} \text{Mode}I & \text{.Math. } V_{ref} \text{ .Math. } \leq \frac{\sqrt{3}}{2}V_{\text{dc2}} \\ \text{ModeII} & \frac{\sqrt{3}}{2}V_{\text{dc2}} < \text{ .Math. } V_{\text{ref}} \text{ .Math. } \leq \frac{\sqrt{3}}{2}(V_{\text{dc1}} - V_{\text{dc2}}) \\ \text{ModeIII} & \frac{\sqrt{3}}{2}(V_{dc1} - V_{dc2}) < \text{ .Math. } V_{\text{ref}} \text{ .Math. } \leq \frac{\sqrt{3}}{2}V_{dc1} \end{cases} \quad (4)$$

[0056] However, according to embodiments described herein, new space voltage vectors V.sub.M, V.sub.S, V.sub.R are defined as linear combinations of selected existing space voltage vectors. For example, in one embodiment the selected existing space voltage vectors are V.sub.3-V.sub.6. According to this embodiment, as shown in FIG. **8** for the first sector, the new space voltage vectors are as follows:

[00004] $V_M = \frac{V_3 + V_4}{2}$ (5) $V_S = \frac{V_5 + 2V_6}{2} V_R = \frac{2V_5 + V_6}{2}$

[0057] According to the new space voltage vectors defined above, the first sector is divided into nine regions as illustrated in FIG. **9**. Every sampling period three adjacent voltage vectors are used to provide a voltage-second equivalent to V.sub.ref. For the reference vector V.sub.ref and the selected space voltage vectors (i.e., the three nearest adjacent space voltage vectors, e.g., for region 1 the three space voltage vectors are V.sub.0, V.sub.1, and V.sub.2), the basic volt-second balance of the SVM scheme is implemented. Then, duty ratios of the new space voltage vectors are calculated. This may be repeated for each of the six sectors, although as described below steps may be implemented to reduce the number of calculations and thereby improve speed and efficiency of modulation implementations.

[0058] For example, the related equations and duty ratio determination for the nine different regions for one sector are as follows:

Region 1:

[00005] $V_{\text{ref}} = V_0 D_0 + V_1 D_1 + V_2 D_2 D_0 + D_1 + D_2 = 1$

[0059] The duty ratios D.sub.0, D.sub.1, and D.sub.2 are calculated using the above equations. Then, the duty ratios of three voltage vectors V.sub.0, V.sub.1, and V.sub.2 are as follows:

[00006] $$\begin{cases} D_{V_0} = D_0 \\ D_{V_1} = D_1 \\ D_{V_2} = D_2 \end{cases}$$

Region 2:

[00007] $V_{\text{ref}} = V_1 D_1 + V_3 D_3 + V_M D_M D_1 + D_3 + D_M = 1$

[0060] The duty ratios D.sub.1, D.sub.3, and D.sub.M are calculated using the above equations. Then, the duty ratios of three voltage vectors V.sub.1, V.sub.3, and V.sub.4 are as follows:

$$D_{V_1} = D_1$$

[00008]{ $D_{V_3} = D_3 + \frac{D_M}{2}$

$$D_{V_4} = \frac{D_M}{2}$$

Region 3:

[00009] $V_{\text{ref}} = V_1 D_1 + V_M D_M + V_2 D_2$

$$D_1 + D_M + D_2 = 1$$

[0061] The duty ratios D.sub.1, D.sub.M, and D.sub.2 are calculated using the above equations. Then, the duty ratios of four voltage vectors V.sub.1, V.sub.2, V.sub.3, and V.sub.4 are as follows:

$$D_{V_1} = D_1$$

$$D_{V_2} = D_2$$

[00010]{ $D_{V_3} = \frac{D_M}{2}$

$$D_{V_4} = \frac{D_M}{2}$$

Region 4:

[00011] $V_{\text{ref}} = V_2 D_2 + V_M D_M + V_4 D_4$ }

$$D_2 + D_M + D_4 = 1$$

[0062] The duty ratios D.sub.2, D.sub.M, and D.sub.4 are calculated using the above equations. Then, the duty ratios of three voltage vectors V.sub.2, V.sub.3, and V.sub.4 are as follows:

$$D_{V_2} = D_2$$

[00012]{ $D_{V_3} = \frac{D_M}{2}$

$$D_{V_4} = D_4 + \frac{D_M}{2}$$

Region 5:

[00013] $V_{\text{ref}} = V_2 D_2 + V_M D_M + V_4 D_4$ }

$$D_2 + D_M + D_4 = 1$$

[0063] The duty ratios D.sub.2, D.sub.M, and D.sub.4 are calculated using the above equations. Then, the duty ratios of three voltage vectors V.sub.2, V.sub.3, and V.sub.4 are as follows:

$$D_{V_3} = D_3$$

[00014]{ $D_{V_5} = D_5 + \frac{2}{3} D_R$

$$D_{V_6} = \frac{D_R}{3}$$

Region 6:

[00015] $V_{\text{ref}} = V_3 D_3 + V_M D_M + V_R D_R$ }

$$D_3 + D_M + D_R = 1$$

[0064] The duty ratios D.sub.3, D.sub.M, and D.sub.R are calculated using the above equations. Then, the duty ratios of four voltage vectors V.sub.3, V.sub.4, V.sub.5 and V.sub.6 are as follows:

$$D_{V_3} = D_3 + \frac{D_M}{2}$$

[00016]{ $D_{V_4} = \frac{D_M}{2}$

$$D_{V_5} = \frac{2}{3} D_R$$

$$D_{V_6} = \frac{D_R}{3}$$

Region 7:

[00017] $V_{\text{ref}} = V_R D_R + V_M D_M + V_S D_S$ }

$$D_R + D_M + D_S = 1$$

[0065] The duty ratios D.sub.R, D.sub.M, and D.sub.S are calculated using the above equations. Then, the duty ratios of three voltage vectors V.sub.3, V.sub.4, V.sub.5 and V.sub.6 are as follows:

$$\text{[00018]}\{\quad \begin{aligned} D_{V_3} &= \tfrac{D_M}{2} \\ D_{V_4} &= \tfrac{D_M}{2} \\ D_{V_5} &= \tfrac{2}{3}D_R + \tfrac{1}{3}D_S \\ D_{V_6} &= \tfrac{1}{3}D_R + \tfrac{2}{3}D_S \end{aligned}$$

Region 8:

$$\text{[00019]}\quad \begin{aligned} V_{\text{ref}} &= V_2 D_2 + V_M D_M + V_4 D_4 \\ D_2 + D_M + D_4 &= 1 \end{aligned} \}$$

[0066] The duty ratios D.sub.2, D.sub.M, and D.sub.4 are calculated using the above equations. Then, the duty ratios of three voltage vectors V.sub.3, V.sub.4, V.sub.5 and V.sub.6 are as follows:

$$\text{[00020]}\{\quad \begin{aligned} D_{V_3} &= \tfrac{D_M}{2} \\ D_{V_4} &= D_4 + \tfrac{D_M}{2} \\ D_{V_5} &= \tfrac{1}{3}D_S \\ D_{V_6} &= \tfrac{2}{3}D_S \end{aligned}$$

Region 9:

$$\text{[00021]}\quad \begin{aligned} V_{\text{ref}} &= V_4 D_4 + V_S D_S + V_6 D_6 \\ D_4 + D_S + D_6 &= 1 \end{aligned} \}$$

[0067] The duty ratios D.sub.2, D.sub.M, and D.sub.4 are calculated using the above equations. Then, the duty ratios of three voltage vectors V.sub.4, V.sub.5 and V.sub.6 are as follows:

$$\text{[00022]}\{\quad \begin{aligned} D_{V_4} &= D_4 \\ D_{V_5} &= \tfrac{1}{3}D_S \\ D_{V_6} &= D_6 + \tfrac{2}{3}D_S \end{aligned}$$

[0068] The adjacent three space voltage vectors in sector I are the coordinates of the vertices of the triangle in which the tip of V.sub.ref is located (FIG. **9**). Based on the above equations for regions 1-9 in sector I, duty ratios of adjacent space voltage vectors may be determined.

[0069] The same procedure may be applied when the tip of the reference voltage vector V.sub.ref is located in another sector. However, due to symmetry, the corresponding space voltage vectors in other sectors may be determined by interchanging the space voltage vectors determined in sector I. The corresponding duty ratios are the same as determined by the above equations for each region in sector I. This allows for a reduction in the number of calculations performed and improved efficiency of the controller.

MSI Modulation Implementation

[0070] Embodiments may be implemented in a controller with power switching device gate drivers and logic circuitry in whole or in part using discrete (e.g., analogue) components and/or using digital technology. Embodiments may include integrated circuit (IC) implementation, which greatly reduces component cost and design complexity. Examples of suitable digital technologies include processors such as, but not limited to, digital signal processor (DSP), field programmable gate array (FPGA), application specific integrated circuit (ASIC), and microcontroller unit (MCU). For example, one or more components of a controller may be implemented using a suitable computer or hardware language (i.e., code) such as, for example, very high speed integrated circuit (VHSIC) hardware descriptive language (VHDL), register transfer language (RTL), or Verilog. Such an algorithm may be stored in a memory device and implemented in, for example, a DSP, FPGA, ASIC, or MCU device of a controller.

[0071] A controller may include components such as current sensor, voltage sensor, comparator, reference current generator, reference voltage generator, proportional-integral (PI) control, PWM, gate driver/buffer, nonvolatile memory device, etc.

[0072] Another aspect of the invention relates to non-transitory computer readable media for use with a processor, the computer readable media having stored thereon instructions that, when executed by the processor of a controller for a MSI, cause the controller to perform a modulation method according to embodiments described herein.

[0073] The invention is further described by way of the following non-limiting Examples.

Example 1. Comparison of Topology with Prior Topologies

[0074] An embodiment based on FIG. **4** was compared to the prior NPC-based MSI topology [3] and the prior T-type based MSI topology (T-MSI) [4]. For the comparison, parameters that have a direct influence on the size, cost, and performance of the converters were taken into consideration.

[0075] Table 2 presents a comparison of features of the three different topologies. It can be seen from Table 2 that the number of DC links and operating modes is the same for each topology, however, the embodiment requires fewer switches, no diodes, and has good loss balancing of the switches compared to the prior approaches.

TABLE-US-00002 TABLE 2 Comparison of Prior Art MSI Topologies and MSI Embodiment NPC MSI T-MSI MSI Feature [3] [4] Embodiment Number of input DC links 2 2 2 Number of operating modes 3 3 3 Number of HF switches 12 12 6 Number of LF switches 0 0 4 Total number of switches 12 12 10 Number of diodes 6 0 0 Loss balancing of Weak Weak Good switching devices

Example 2. Comparison of Switching Frequency and Output Voltage THD

[0076] An embodiment based on FIG. **4** was compared to the prior NPC-based MSI topology [3] under both conventional SVM and SVM according to an embodiment.

[0077] Measurements and calculations were carried out using the PSIM™ software simulation package (Altair Engineering Inc., Troy, MI, USA). The IGBT switch was IXYS IXGH40N60C2 (Littelfuse, Chicago, IL, USA) with current and voltage rating of 40 A and 600 V. The voltage amplitude of DC source 1, V.sub.DC1, was considered to be three times of the voltage amplitude of DC source 2, V.sub.DC2. Therefore, the MSIs have modulation indexes in the intervals [0 0.333], [0.333 0.666], and [0.666 1] when operating at mode 1, 2, and 3, respectively.

[0078] Results are presented in Table 3A (NPC-based MSI topology) and Table 3B (topology according to an embodiment) wherein it can be seen that the SVM scheme according to the embodiment enabled reduced switching frequencies and lower THD in the NPC-based topology, and the topology embodiment demonstrated improvements over the NPC-based topology under both modulation schemes.

TABLE-US-00003 TABLE 3A Switching Frequency and Output Voltage THD of NPC-based MSI. Output voltage Switching frequency (kHz) THD f.sub.Sx1, f.sub.Sx2, f.sub.Sx3, f.sub.Sx4 (%) (x = a, b, c) Mode Mode Mode Topology Modulation Mode III Mode II Mode I III II I NPC-based Conventional 10, 10, 10, 10 10, 0, 10, 0 0, 10, 0, 10 51 51 51 MSI Embodiment 3.3, 6.8, 3.3, 6.8, 5.4, 6.8, 0, 6.7, 0, 6.7 40 43 51 6.8 5.4

TABLE-US-00004 TABLE 3B Switching Frequency and Output Voltage THD of MSI according to one embodiment. Output voltage Switching frequency (kHz) THD f.sub.S1, f.sub.S2 (%) f.sub.T1, f.sub.T3 Mode Mode Mode Topology Modulation Mode III Mode II Mode I III II I Embodiment Conventional 10, 10 10, 10 10, 10 51 51 51 0, 0 0, 0 0, 0 Embodiment 3.3, 3.3 3.3, 3.3 6.7, 6.7 40 43 51 0, 10 10, 10 0, 0

Example 3. Comparison of Losses and Efficiency

[0079] Losses and efficiency of an embodiment based on FIG. **4** were compared to the prior NPC-based MSI topology [3] under both conventional SVM and SVM according to an embodiment as described above. The power losses associated with a static converter mainly consist of the filter losses, the switching losses, and the conduction losses of the switching devices. Since the filter losses for different converters are expected to be similar if the harmonic spectra of their output

voltages are similar, they were not considered.
[0080] The power loss calculation of the switching devices was carried out using the PSIM™ software simulation package (Altair Engineering Inc., Troy, MI, USA). The IGBT switch was IXYS IXGH40N60C2 (Littelfuse, Chicago, IL, USA) with current and voltage rating of 40 A and 600V, respectively. The voltage amplitude of DC source 1, V.sub.DC1, was considered to be three times of the voltage amplitude of DC source 2, V.sub.DC2. Therefore, the MSIs have modulation indexes in the intervals [0 0.333], [0.333 0.666], and [0.666 1] when operating at mode 1, 2, and 3, respectively.
[0081] Results of the comparisons are shown in FIGS. **10**A-**10**C, wherein it can be seen that conduction loss of the embodiment was less than that of the prior NPC-based topology under both modulation schemes (FIG. **10**A) in all three operating modes. Switching loss of the embodiment MSI topology operating under the modulation scheme embodiment was lowest in all three operating modes (FIG. **10**B). The calculated efficiency of the embodiment MSI topology was higher than the NPC-based topology under both modulation schemes in all three operating modes (FIG. **10**C).
Example 4. Prototype Testing
[0082] A scaled-down laboratory prototype was built and its performance evaluated. The prototype was modulated using a conventional space vector PWM (SVPWM) scheme with pulses generated using a digital signal processor (DSP). The experimental system parameters are given in Table 4. In the experimental setup, the first DC-link (V.sub.DC1) was a DC source and the second DC-link (V.sub.DC2) was an ultracapacitor (UC) implemented with a capacitor connected in parallel with a DC source.
TABLE-US-00005 TABLE 4 Experimental prototype system parameters. System Parameter Value Switching devices IGBT Infineon IKW25N120H3 Gate driver optocouplers Avago Technologies ACPL-336J DC source voltage 180 V UC voltage 60 V UC capacitance 10 mF Digital Signal Processor Texas Instruments TMS320F28335 Sampling frequency 10 kHz Reference voltage frequency (f.sub.o) 50 Hz Load-Resistive, Inductive (R, L) 5 Ω, 9 mH
[0083] FIGS. **11**A-**11**C show the experimental line-to-line voltages, three-phase load currents, and DC currents (FIG. **11**C: lower, DC source current (V.sub.DC1); upper, UC current (V.sub.DC2)) of the prototype operating under mode I. The load reference current was set to 2.5 A. The negative and positive peak values of the line-to-line voltage waveforms are associated with the DC voltage of the UC bank, which was 60 V. The three-phase sinusoidal load currents have amplitude near the reference current. As can be seen in FIG. **11**C, the DC source current (lower trace) in mode I was zero and the load power was provided by the UC bank.
[0084] To show transient performance of the prototype embodiment, a step change from operating mode I to operating mode II was applied. The output line voltages, load currents, and DC currents are shown in FIGS. **12**A-**12**C. Initially the MSI embodiment was operating in mode I. The UC bank supplied the load with a current of 2.5 A. The converter was then switched to mode II. As can be seen in FIG. **12**C (note the different time scale), in mode II, the DC source current and UC bank current were positive and negative, respectively. The DC source charged the UC bank with a current of about 4 A and supplied the load concurrently. The three-phase currents are shown in FIG. **12**B, in which the peak current amplitude changed from 2.5 A to 5.5 A by the transition from mode I to mode II.
[0085] To show performance of the MSI embodiment operating in mode III, the reference current was increased to 4.5 A. The experimental results are shown in FIGS. **13**A-**13**C. The DC link voltage of the voltage source inverter (VSI) had a voltage amplitude equal to the DC voltage source. Consequently, the line voltage waveform had a maximum amplitude equal to the DC voltage source (V.sub.DC1), which was around 180 V. The DC source currents are shown in FIG. **13**C. The DC source (upper trace) provided the load power, and the current of the UC bank (V.sub.DC2, lower trace) was zero.

[0086] A step-change of 80 ms duration was implemented to test the performance of the MSI embodiment during a load transition from full load to 20% of full load. The output line voltages, load currents, and DC currents are shown in FIGS. **14**A-**14**C. The MSI embodiment was operating in mode III. The DC source supplied a current of approximately 6 A to the load. The load current then decreased to one-fifth of its nominal value. The DC source current dropped to 1.5 A, and it supplied the load. When the load transition occurred, the peak AC current amplitude dropped from 5 A to 1 A, as shown in FIG. **14**B. The converter returned to full load after 80 ms.

EQUIVALENTS

[0087] It will be appreciated that modifications may be made to the embodiments described herein without departing from the scope of the invention. Accordingly, the invention should not be limited by the specific embodiments set forth, but should be given the broadest interpretation consistent with the teachings of the description as a whole.

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Claims

1. A modulation scheme for a three-phase multi-source inverter (MSI), comprising: defining a stationary αβ plan of the three-phase voltages comprising six sectors I to VI, wherein each sector has seven existing space voltage vectors; defining V.sub.ref as a three-phase reference voltage vector in the αβ plan; for each sector, calculating new space voltage vectors V.sub.M, V.sub.S, and V.sub.R as linear combinations of at least two of the existing space voltage vectors; dividing each sector into nine operating regions; determining switching signals for switching devices of the MSI in each operating region in each sector using the V.sub.ref, selected new space voltage vectors, and selected existing space voltage vectors.

2. The modulation scheme of claim 1, wherein the generating switching signals comprises using four selected existing space voltage vectors.

3. The modulation scheme of claim 2, wherein the four selected existing space voltage vectors include V.sub.3-V.sub.6.

4. The modulation scheme of claim 1, comprising: calculating the new space voltage vectors for one sector selected from sectors I to VI; determining corresponding new space voltage vectors in other sectors by interchanging the new space voltage vectors determined for the selected sector.

5. A non-transitory computer readable media compatible with a processor, the non-transitory computer readable media storing an algorithm that directs the processor to implement a space vector modulation (SVM) scheme for an MSI; wherein the SVM scheme comprises: defining a stationary αβ plan of the three-phase voltages comprising six sectors I to VI, wherein each sector has seven existing space voltage vectors; defining V.sub.ref as a three-phase reference voltage vector in the αβ plan; for each sector, calculating new space voltage vectors V.sub.M, V.sub.S, and

V.sub.R as linear combinations of at least two of the existing space voltage vectors; dividing each sector into nine operating regions; determining switching signals for switching devices of the MSI in each operating region in each sector using the V.sub.ref, selected new space voltage vectors, and selected existing space voltage vectors.

6. A controller for a three-phase MSI, comprising: a processor that executes an algorithm that implements the modulation scheme of claim 1; and an output circuit that outputs the switching signals to switches of the MSI according to the modulation scheme.

7. The controller of claim 6, implemented in an electric vehicle.

8. A three-phase multi-source inverter (MSI) comprising the controller of claim 6.

9. A three-phase multi-source inverter (MSI), comprising: a first switch having an input terminal adapted to receive a positive side of a first DC source (V.sub.DC1); a second switch having an input terminal adapted to receive a negative side of the first DC source (V.sub.DC1) and a negative side of a second DC source (V.sub.DC2); an output of the first switch connected to inputs of third, fifth, seventh, and ninth switches; the third switch having an output terminal adapted to receive a positive side of the second DC source (V.sub.DC2) and connected to an input of a fourth switch; outputs of the fifth, seventh, and ninth switches connected to inputs of sixth, eighth, and tenth switches and to output nodes corresponding to respective MSI three-phase output currents i.sub.a, i.sub.b, and i.sub.c; outputs of the second, fourth, sixth, eighth, and tenth switches connected together.

10. The three-phase MSI of claim 9, comprising at least one DC-DC converter that provides the first DC source or the second DC source.

11. The three-phase MSI of claim 9, wherein the first DC source comprises a high voltage source and the second DC source comprises a low voltage source.

12. The three-phase MSI of claim 9, wherein the first DC source comprises a high voltage source and the second DC source comprises a battery, a super capacitor, or an ultra capacitor.

13. The three-phase MSI of claim 9, configured for use in an electric vehicle.

14. The three-phase MSI of claim 9, comprising a controller.

15. The three-phase MSI of claim 14, wherein the controller controls switches of the MSI according to a space vector modulation (SVM) scheme.

16. The three-phase MSI of claim 15, wherein the SVM scheme comprises: defining a stationary αβ plan of the three-phase voltages comprising six sectors I to VI, wherein each sector has seven existing space voltage vectors; defining V.sub.ref as a three-phase reference voltage vector in the αβ plan; for each sector, calculating new space voltage vectors V.sub.M, V.sub.S, and V.sub.R as linear combinations of at least two of the existing space voltage vectors; dividing each sector into nine operating regions; determining switching signals for switching devices of the MSI in each operating region in each sector using the V.sub.ref, selected new space voltage vectors, and selected existing space voltage vectors.

17. The three-phase MSI of claim 16, configured for use in an electric vehicle.