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(54) **GATE DRIVING CIRCUIT FOR WIDE BANDGAP (WBG) POWER DEVICES**

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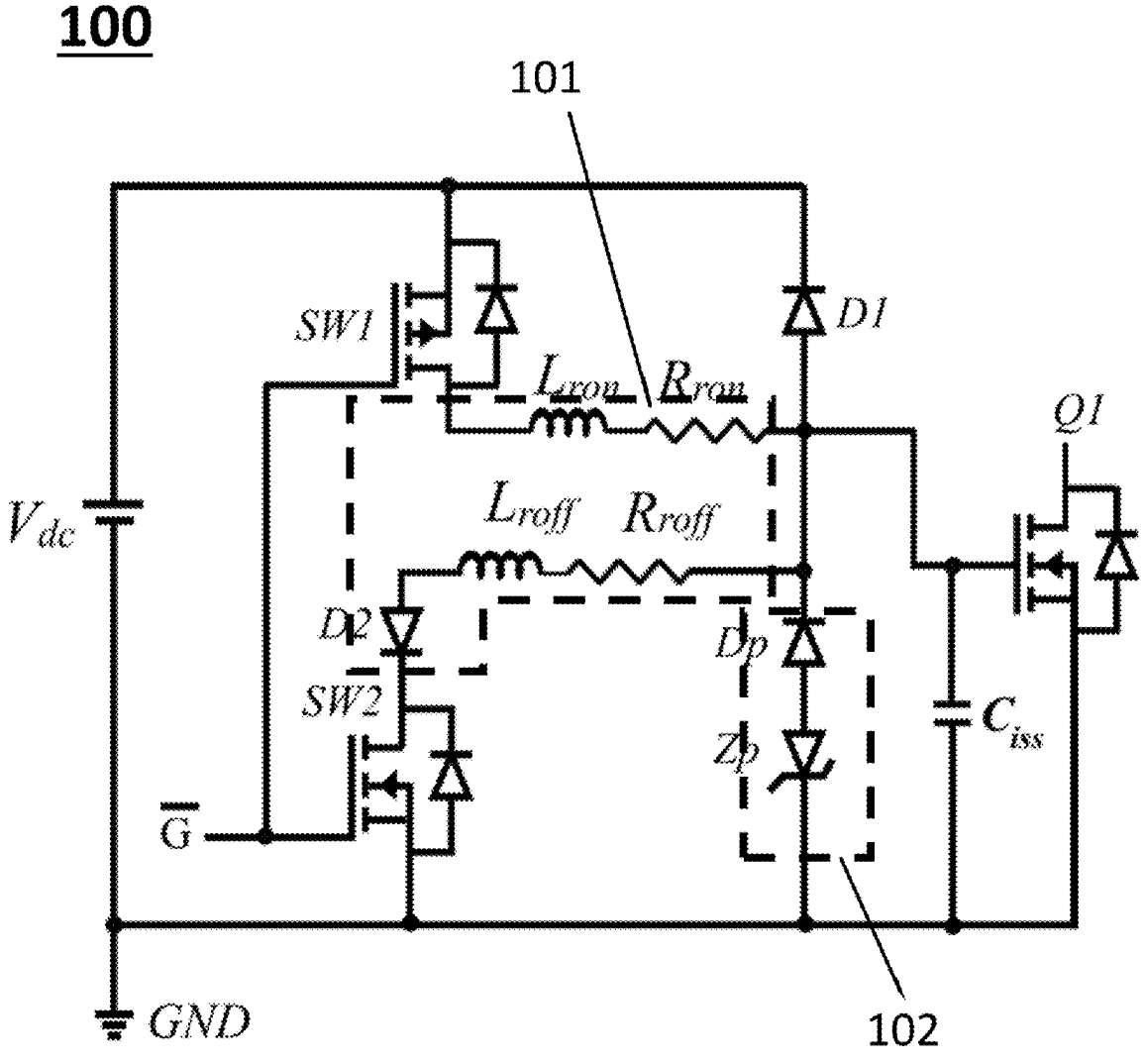
(57) **ABSTRACT**

A resonant-based gate driving circuit for WBG power semiconductor devices is provided to suppress crosstalk in one leg configured power converters. The gate driving circuit comprises DC voltage source, first and second semiconductor switches, and a crosstalk suppressing circuit including: a first resonant inductor and a first resistor configured to form a path for charging an input capacitance of the WBG device up to the DC voltage source when a logic high control signal is generated from controller output and applied to the gate terminal of first and second semiconductor switches; a diode, a second resonance inductor, and a second resistor configured to form a path for discharging the input capacitance of WBG device, and to provide an adjustable negative gate-source turn-off voltage to the WBG device when a logic low control signal is generated from controller output and applied to the gate terminal of first and second semiconductor switches.



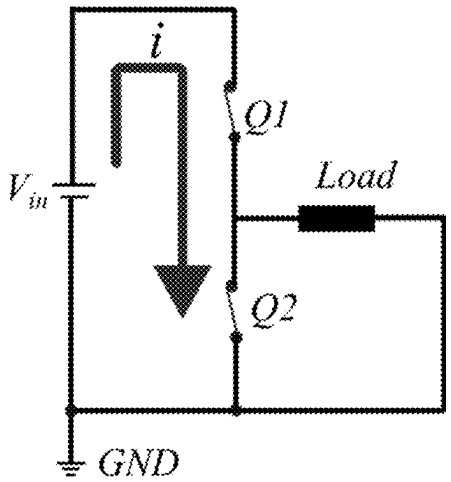


FIG. 1

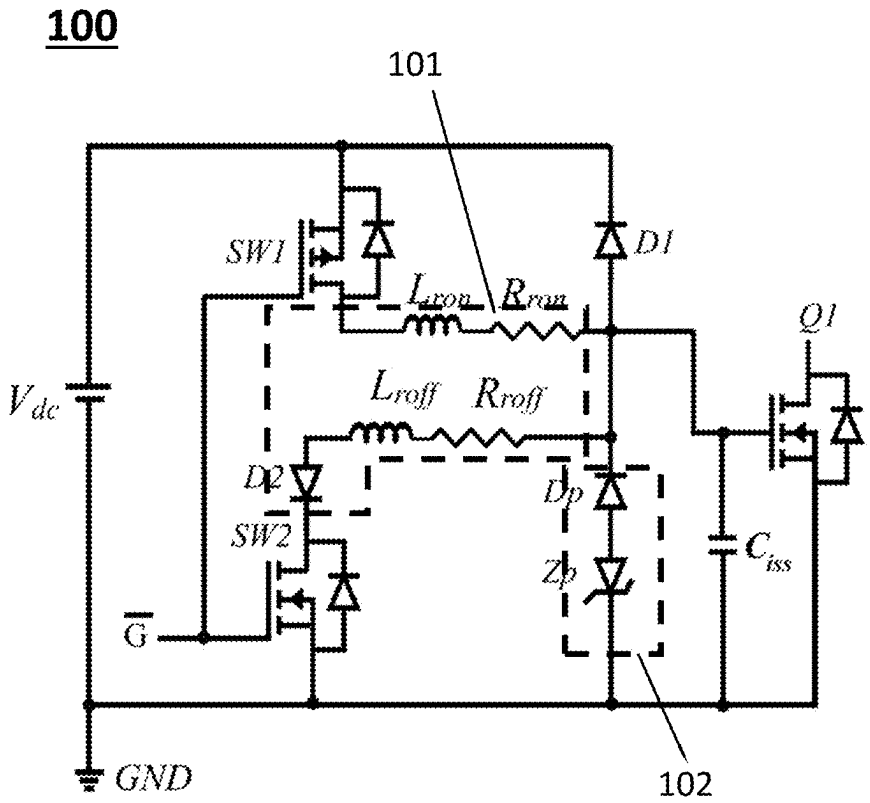

100
101
SW1
D1
L_{ron}
R_{ron}
Q1
V_{dc}
L_{roff}
R_{roff}
D2
D_p
SW2
Z_p
C_{iss}
G
GND
102

FIG. 2

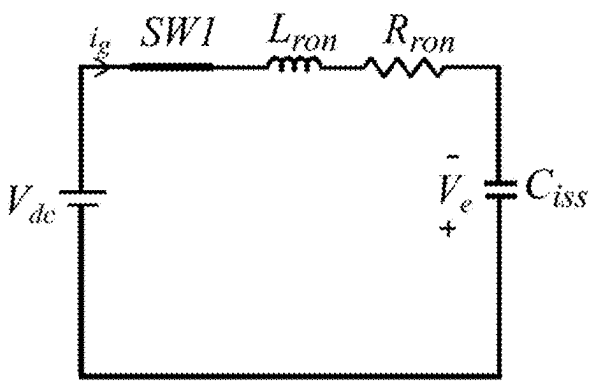


FIG. 3A

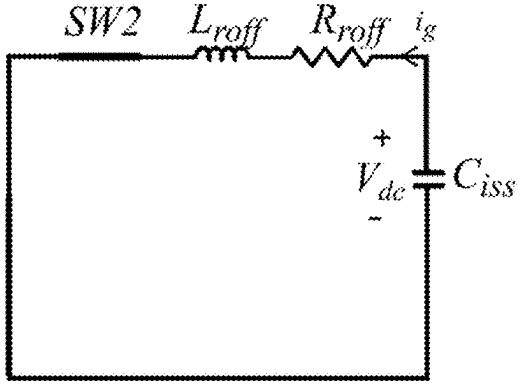


FIG. 3B

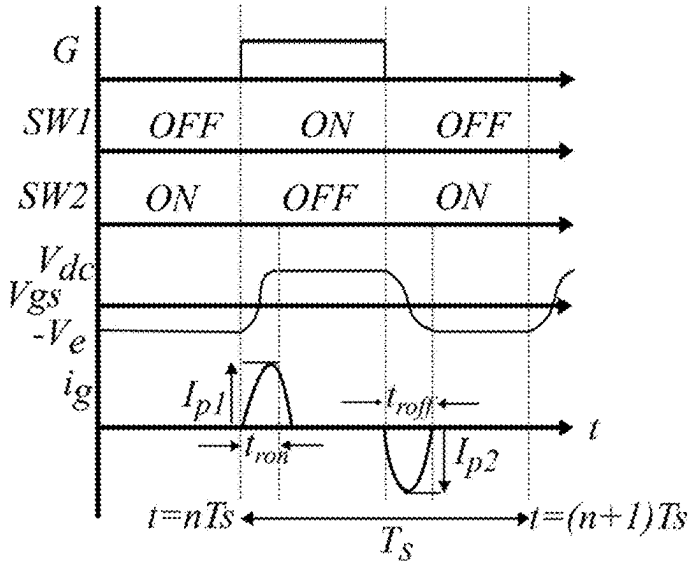


FIG. 4

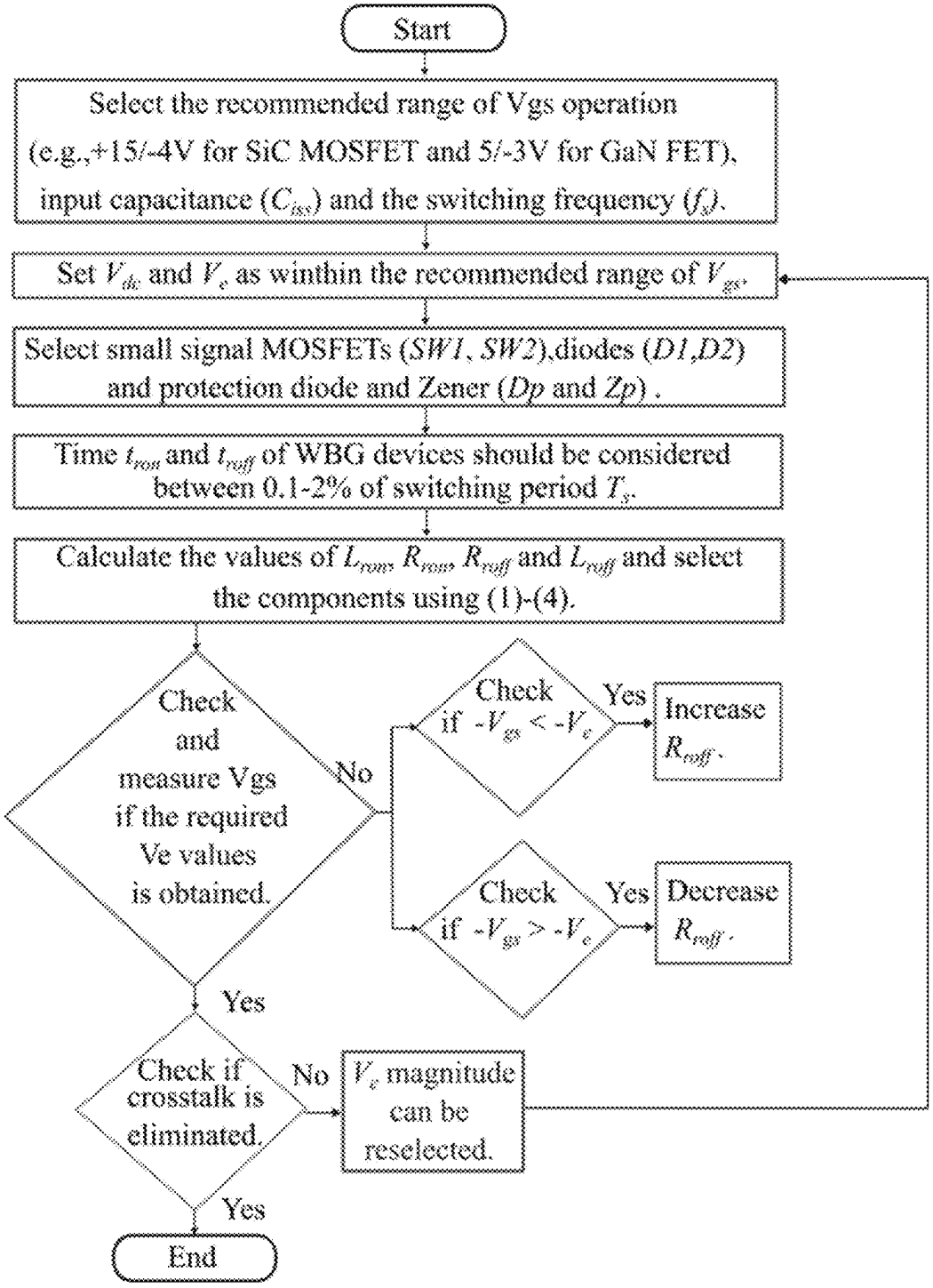

Start
Select the recommended range of Vgs operation (e.g.,+15/-4V for SiC MOSFET and 5/-3V for GaN FET), input capacitance (C_{iss}) and the switching frequency (f_s).
Set V_{dc} and V_e as winthin the recommended range of V_{gs}.
Select small signal MOSFETs (SW1, SW2),diodes (D1,D2) and protection diode and Zener (Dp and Zp) .
Time t_{ron} and t_{roff} of WBG devices should be considered between 0.1-2% of switching period T_s.
Calculate the values of L_{ron}, R_{ron}, R_{roff} and L_{roff} and select the components using (1)-(4).
Check and measure Vgs if the required Ve values is obtained.
No
Check if $-V_{gs} < -V_e$
Yes
Increase R_{roff}.
Check if $-V_{gs} > -V_e$
Yes
Decrease R_{roff}.
Yes
Check if crosstalk is eliminated.
No
V_e magnitude can be reselected.
Yes
End

FIG. 5

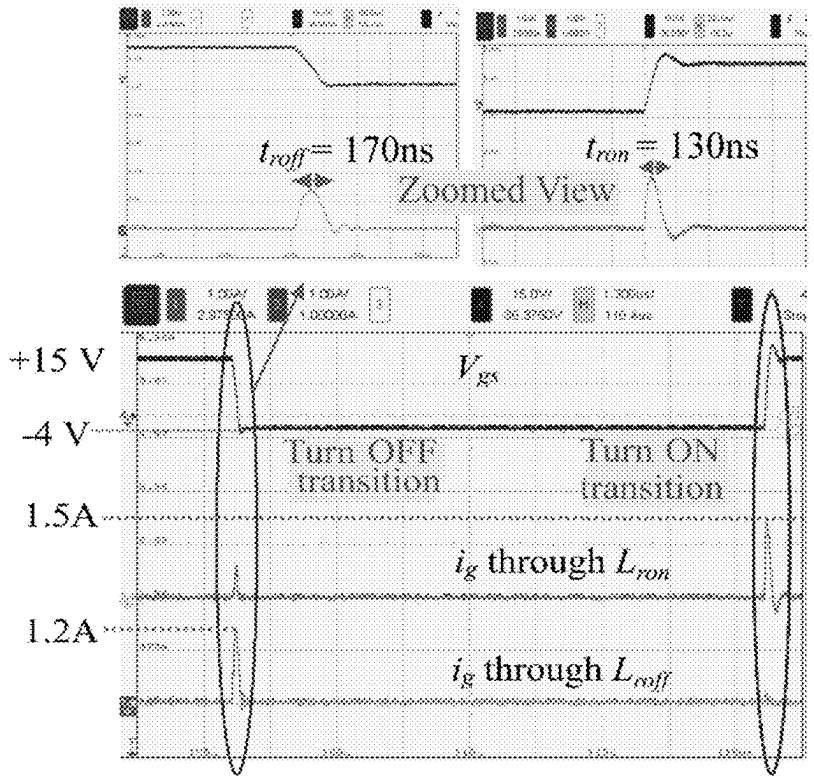

t_{roff} = 170ns
t_{ron} = 130ns
Zoomed View
+15 V
-4 V
1.5A
1.2A
V_{gs}
Turn OFF transition
Turn ON transition
i_g through L_{ron}
i_g through L_{roff}

FIG. 6

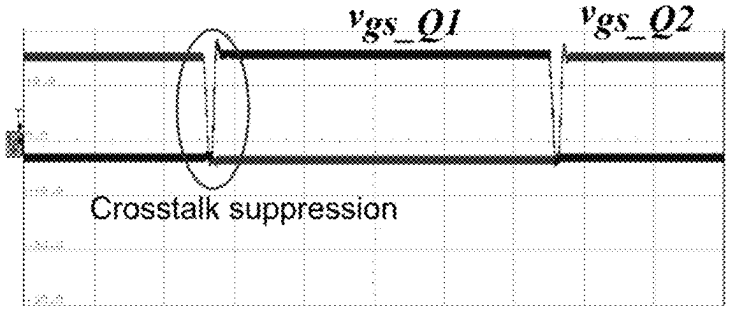

v_{gs_Q1}
v_{gs_Q2}
Crosstalk suppression

FIG. 7

200

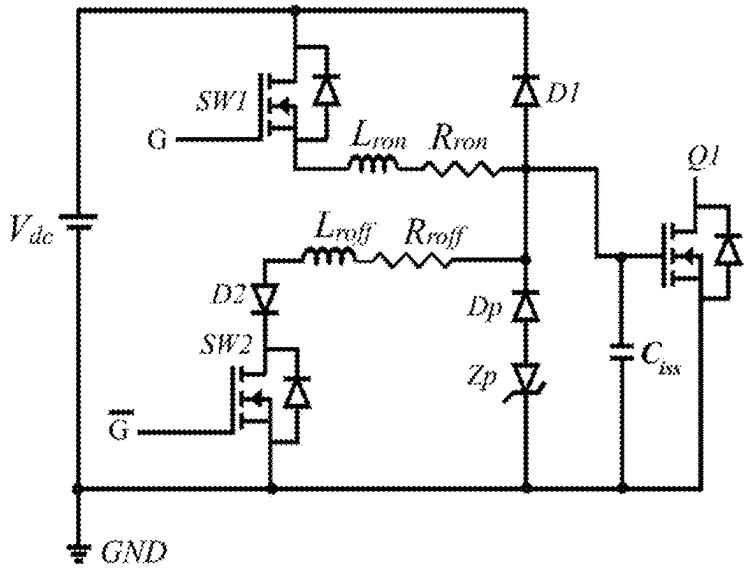


FIG. 8

300

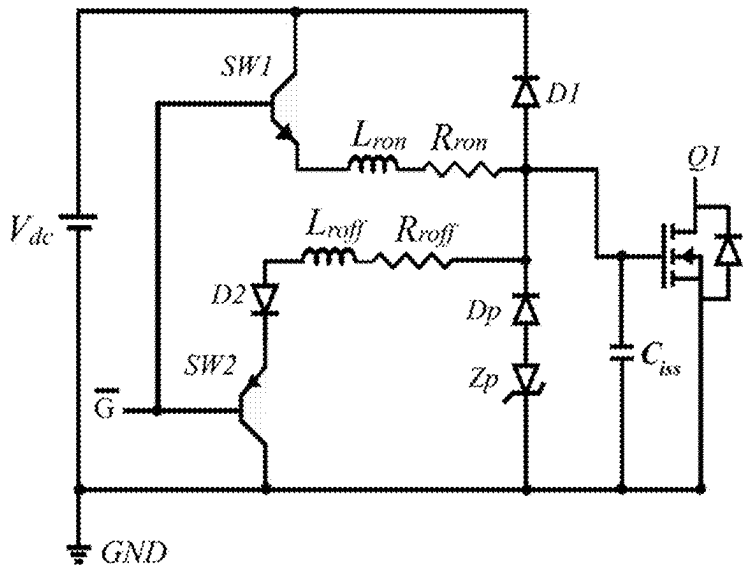


FIG. 9

400

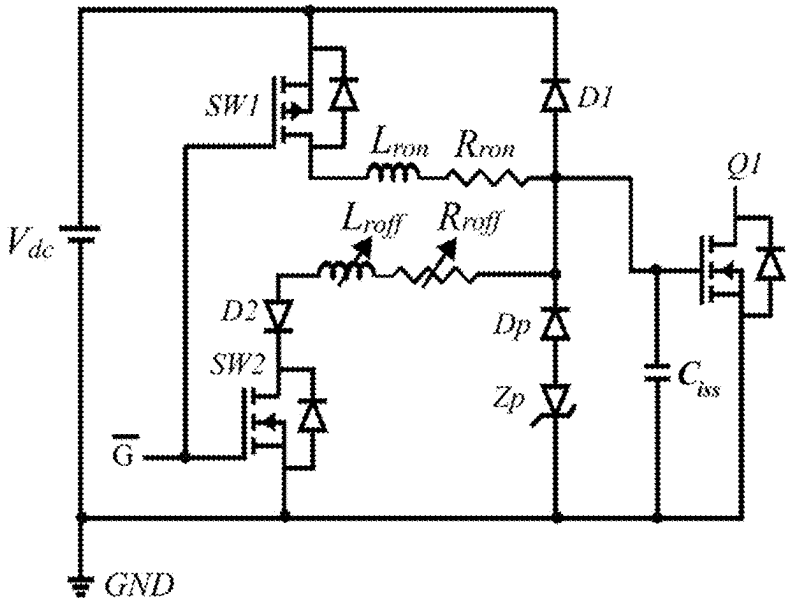


FIG. 10

500

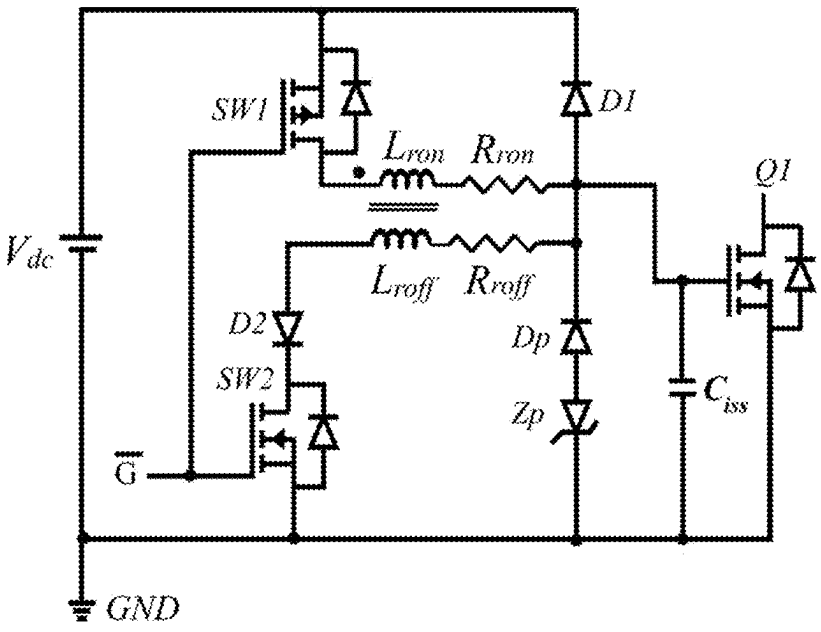


FIG. 11

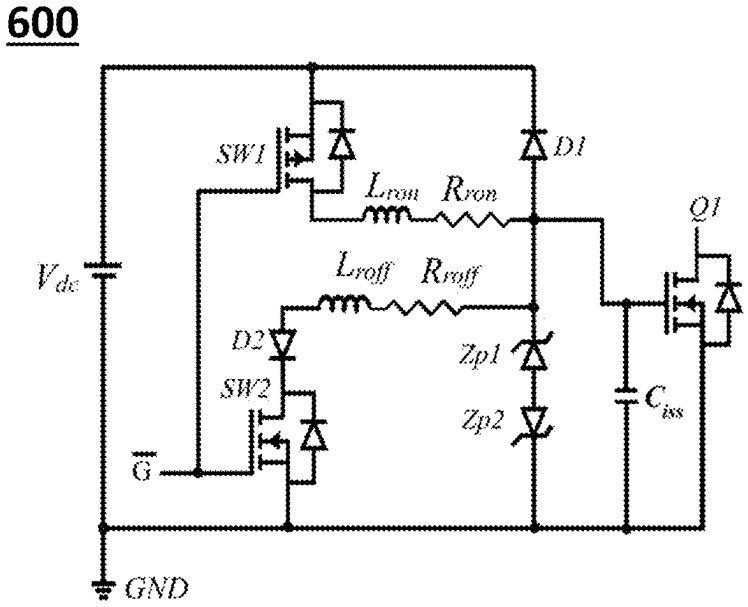

600
SW1
D1
Lron
Rron
Q1
Vdc
Lroff
Rroff
D2
Zp1
SW2
Ciss
Zp2
G
GND

FIG. 12

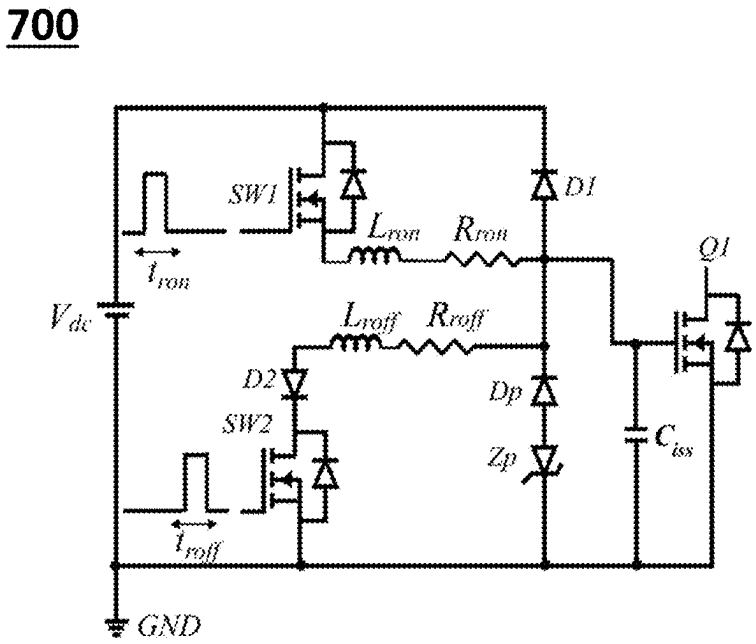

700
SW1
D1
Lron
Rron
Q1
Tron
Vdc
Lroff
Rroff
D2
Dp
SW2
Ciss
Zp
Troff
GND

FIG. 13

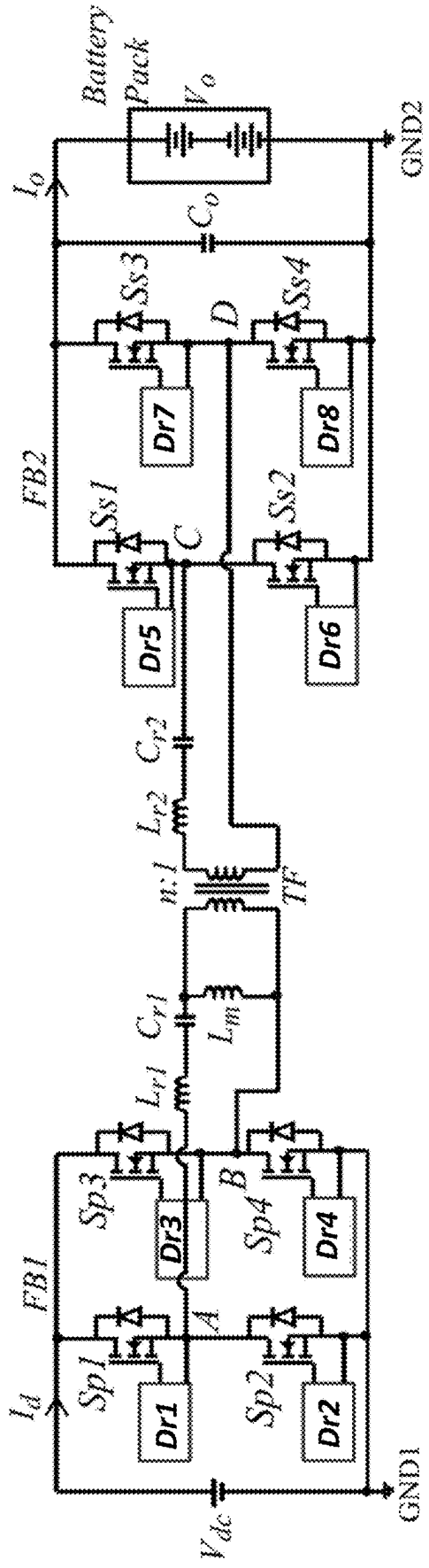

Battery Pack
V_o
GND2
I_o
C_o
Ss3
Ss4
D
Dr7
Dr8
FB2
Ss1
Ss2
C
Dr5
Dr6
C_{r2}
L_{r2}
n:1
TF
C_{r1}
L_m
L_{r1}
Sp3
Sp4
B
Dr3
Dr4
FB1
A
I_d
Sp1
Sp2
Dr1
Dr2
V_{dc}
GND1

FIG. 14

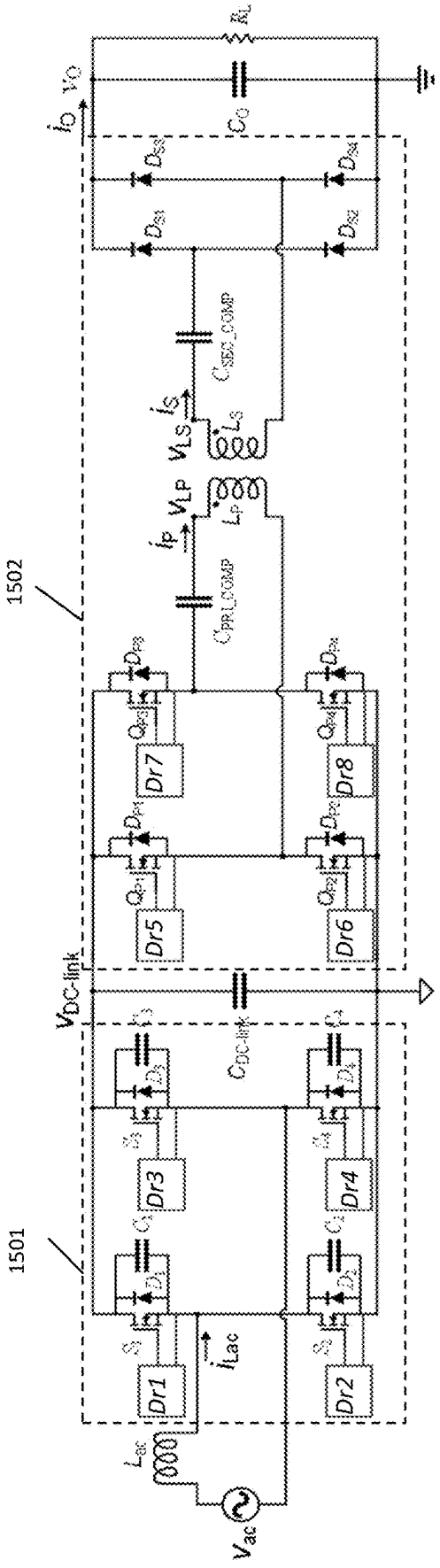

1502
1501
Dr1
Dr2
Dr3
Dr4
Dr5
Dr6
Dr7
Dr8
Lac
Vac
VDC-link
CDC-link
LS
LP
CSEO_COMP
CPP1_COMP
CO
RL
VO
iO
iS
iP
iLac

FIG. 15

GATE DRIVING CIRCUIT FOR WIDE BANDGAP (WBG) POWER DEVICES

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FIELD OF THE INVENTION

[0002] The present invention generally relates to a methodology for gate driving approach of wide bandgap (WBG) power semiconductor devices. More specifically the present invention relates to a resonance-based circuit for suppressing crosstalk when driving a wide bandgap device.

BACKGROUND OF THE INVENTION

[0003] Wide bandgap (WBG) power semiconductor devices, such as silicon carbide (SIC) power metal-oxide-semiconductor field-effect transistors (MOSFETs) and gallium nitride (GaN) field-effect transistors (FETs), are emerging solutions for high-efficiency and high-power-density power electronics and systems applications. As shown in FIG. **1**, a half-bridge converter is composed of a one leg configuration including two WBG power switches such as SiC MOSFETs. When the SiC MOSFETs are operated at high switching frequency, during turn-on transition of the high side MOSFET, a high dv/dt at the low side MOSFET induces a charging current to its input capacitance, resulting in a sudden increase in gate source voltage of the low side MOSFET, causing a spurious pulse which exceeds the threshold voltage of the low side MOSFET. Therefore, false turn-on occurs and both power MOSFETs are turned on accidentally. Such a phenomenon is called crosstalk. The crosstalk issue may cause shoot-through resulting in high short-circuit current which may lead to the damage of WBG power semiconductor devices or even explosion. Moreover, oscillations in voltage and current may cause severe electromagnetic interference (EMI) problems and will degrade converter's reliability and efficiency.

SUMMARY OF THE INVENTION

[0004] It is one objective of the present invention to provide a gate driving circuit which can suppress crosstalk in one leg configured power converters, such as half bridge, full-bridge, or synchronous buck converters and suitable for diving WBG power semiconductor devices in. It is another objective of the present invention to provide a resonant-based gate driving circuit with simpler configuration and less power consumption when compared to conventional solutions.

[0005] In accordance with a first aspect of the present invention, a gate driving circuit for driving a wide bandgap power device is provided. The gate driving circuit comprises: a DC voltage source, a first semiconductor switching device having a high voltage terminal connected to a positive terminal of the DC voltage source and a control terminal connected to a controller output; a second semiconductor switching device having a low voltage terminal connected to a negative terminal of the DC voltage source and a control terminal connected to a controller output; and a crosstalk suppressing circuit. The crosstalk suppressing circuit includes a first resonant inductor having a first end connected to a low voltage terminal of the first semiconductor switching device; a first resistor having a first end connected to a second end of the first resonant inductor and a second end connected to a gate terminal of the WBG power semiconductor device; a first diode having an anode terminal connected to the gate of the WBG power semiconductor device and a cathode terminal connected to a positive terminal of the DC voltage source; a second diode having a cathode connected to a high voltage terminal of the second semiconductor switching device; a second resonant inductor having a first end connected to an anode of the second diode; a second resistor having a first end connected to a second end of the second resonant inductor and a second end connected to the gate of the WBG power semiconductor device. The first resonant inductor and the first resistor are configured to form a path for charging an input capacitance of the WBG power semiconductor device up to the DC voltage source when a logic high control signal is generated from the controller output and applied to the gate terminal of first and second semiconductor switches. The first diode is configured to clamp a gate-to-source voltage of the WBG power semiconductor device to the DC voltage source to serve as a protection; and the second diode, the second resonant inductor, and the second resistor are configured to form a path for discharging the input capacitance of WBG power semiconductor device, and to provide an adjustable negative gate-source turn-off voltage to the WBG power semiconductor device when a logic low control signal is generated from the controller output and applied to the gate terminal of first and second semiconductor switches.

[0006] In accordance with a second aspect of the present invention, a CLLC resonant converter-based battery energy storage system is provided. The CLLC resonant converter-based battery energy storage system comprises one or more gate driving circuits according to the first aspect of the present invention.

[0007] In accordance with a third aspect of the present invention, a wireless power transfer system having an AC/DC hard-switched converter and a DC/DC hard-switched converter is provided. Each of the AC/DC hard-switched converter and DC/DC hard-switched converter comprises one or more gate driving circuits according to the first aspect of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS:

[0008] Embodiments of the invention are described in more details hereinafter with reference to the drawings, in which:

[0009] FIG. **1** shows a half bridge converter having a one leg configuration including two WBG power semiconductor switches, Q**1** and Q**2**.

[0010] FIG. **2** shows a circuit diagram of a gate driving circuit for driving a WBG power semiconductor device Q**1** in accordance with one embodiment of the present invention.

[0011] FIGS. **3**A and **3**B show equivalent circuits of the gate driving circuit during the turn-on transition period (denoted as t_{ron}) and the turn-off transition period (denoted as t_{roff}). respectively.

[0012] FIG. **4** shows waveforms of the control signal G, switching states of switches SW**1** and SW**2**, the gate-source voltage V_{gs} of the WBG power semiconductor device Q**1**, and the gate current i_g.

[0013] FIG. **5** shows the flow chart of key design steps required for the gate driving circuit.

[0014] FIG. **6** shows experimental results of turn-on transition period t_{ron} and the turn-off transition period t_{roff} achieved with the gate driving circuit according to the present invention.

[0015] FIG. **7** shows experimental results of V_{gs} of two WBG power semiconductor devices Q**1**, Q**2** in a half bridge converter for illustration of crosstalk suppression.

[0016] FIG. **8** shows a circuit diagram of a gate driving circuit according to another embodiment of the present invention.

[0017] FIG. **9** shows a circuit diagram of a gate driving circuit according to another embodiment of the present invention.

[0018] FIG. **10** shows a circuit diagram of a gate driving circuit according to another embodiment of the present invention.

[0019] FIG. **11** shows a circuit diagram of a gate driving circuit according to another embodiment of the present invention.

[0020] FIG. **12** shows a circuit diagram of a gate driving circuit according to another embodiment of the present invention.

[0021] FIG. **13** shows a circuit diagram of a gate driving circuit according to another embodiment of the present invention.

[0022] FIG. **14** shows a circuit diagram of a CLLC resonant converter-based battery energy storage system constructed with the gate driving circuits (denoted as Dr**1**-Dr**8**) according to the embodiments of the present invention.

[0023] FIG. **15** shows a circuit diagram of a wireless power transfer system having an AC/DC and a DC/DC hard-switched based converters constructed with the gate driving circuits (denoted as Dr**1**-Dr**8**) according to the embodiments of the present invention.

DETAILED DESCRIPTION

[0024] In the following description, details of the present invention are set forth as preferred embodiments. It will be apparent to those skilled in the art that modifications, including additions and/or substitutions may be made without departing from the scope and spirit of the invention. Specific details may be omitted so as not to obscure the invention; however, the disclosure is written to enable one skilled in the art to practice the teachings herein without undue experimentation.

[0025] FIG. **2** shows a circuit diagram of a gate driving circuit **100** for driving a WBG power semiconductor device Q**1** in accordance with one embodiment of the present invention.

[0026] As shown, the gate driving circuit **100** comprises a DC voltage source V_{dc}; a first semiconductor switching device SW**1** having a high voltage terminal connected to a positive terminal of the DC voltage source V_{dc} and a control terminal connected to a controller output $\overline{G}$; and a second semiconductor switching device SW**2** having a low voltage terminal connected to a negative terminal of the DC voltage source and a control terminal connected to the controller output $\overline{G}$.

[0027] The gate driving circuit **100** may further comprise a crosstalk suppressing circuit **101** including: a resonant inductor L_{ron} having a first end connected to a low voltage terminal of the first semiconductor switching device SW**1**; a resistor R_{ron} having a first end connected to a second end of the resonant inductor L_{ron} and a second end connected to the gate terminal of the WBG power semiconductor device Q**1**; a diode D**2** having a cathode connected to a high voltage terminal of the second semiconductor switching device SW**2**; a resonant inductor L_{roff} having a first end connected to an anode of the diode D**2**; a resistor R_{roff} having a first end connected to a second end of the resonant inductor L_{roff} and a second end connected to the gate terminal of the WBG power semiconductor device Q**1**.

[0028] The resonant inductor L_{ron} and the resistor R_{ron} are configured to form a path for charging an input capacitance C_{iss} of the the WBG power semiconductor device Q**1** up to the DC voltage source V_{dc} when a logic high control signal is generated from the controller output. The diode D**2** is configured to form a path for discharging the input capacitance C_{iss} of WBG power semiconductor device Q**1**. The resonant inductor L_{roff} and the resistor R_{roff} are configured to provide an adjustable negative gate-source turnoff voltage $-V_e$ to the WBG power semiconductor device Q**1** to suppress crosstalk in various applications, such as bridge converters, when a logic low control signal is generated from controller output.

[0029] The gate driving circuit **100** may further comprise a protection circuit **102** across the gate and source of the WBG power semiconductor device Q**1**. The protection circuit **102** may include a Zener diode Zp and a diode Dp connected back-to-back with the Zener diode Zp. That is, the diode Dp has a cathode connected to the gate terminal of the WBG power semiconductor device Q**1**; the Zener diode Zp has an anode connected to an anode of the diode Dp and a cathode connected to the source terminal of the WBG power semiconductor device Q**1**.

[0030] The gate driving circuit **100** further comprises a clamping diode D**1** configured for clamping a gate source voltage V_{gs} of the WBG power semiconductor device power device Q**1** to the supply voltage of the DC voltage source V_{dc}, that is, to prevent the gate source voltage V_{gs} applied on the WBG power semiconductor device Q**1** from exceeding the voltage V_{dc}. The clamping diode D**1** has an anode connected to a gate terminal of the WBG power semiconductor device Q**1** and a cathode connected to the positive terminal of the voltage source V_{dc}.

[0031] FIGS. **3**A and **3**B show equivalent circuits of the gate driving circuit **100** during the turn-on transition period (denoted as t_{ron}) and the turn-off transition period (denoted as t_{roff}), respectively.

[0032] The resonant frequency of the crosstalk suppressing circuit during t_{ron} is given by:

$$\omega_{r1} = \frac{1}{\sqrt{L_{ron} C_{iss}}} \tag{1a}$$

[0033] The resonant frequency of the crosstalk suppressing circuit during t_{roff} is given by:

$$\omega_{r2} = \frac{1}{\sqrt{L_{roff} C_{iss}}} \quad (1b)$$

[0034] The gate current is given by:

$$i_g(t) = \frac{V_{dc} + V_e}{\omega_{d1} L_{ron}} e^{-\alpha 1 t} \sin(\omega_{d1} t) \quad (2)$$

[0035] The gate-source voltage V_{gs} of **Q1** during t_{ron} is given by:

$$v_{gs1}(t) = (V_{dc} + V_e)\left(1 - e^{-\alpha 1 t}\cos(\omega_{d1} t) - \frac{\alpha 1}{\omega_{d1}} e^{-\alpha 1 t}\sin(\omega_{d1} t)\right) - V_e \quad (3)$$

[0036] The gate-source voltage V_{gs} of **Q1** during t_{roff} is given by:

$$v_{gs2}(t) = (V_{dc})\left(1 - e^{-\alpha 2 t}\cos(\omega_{d2} t) - \frac{\alpha 2}{\omega_{d2}} e^{-\alpha 2 t}\sin(\omega_{d2} t)\right) \quad (4)$$

[0037] Where,

$$\alpha 1 = \frac{R_{ron}}{2L_{ron}} \text{ and } \alpha 2 = \frac{R_{roff}}{2L_{roff}}$$

are attenuation constants; $\omega_{d1}=\sqrt{\omega_{r1}^2-\alpha 1^2}$ and $\omega_{d2}=\sqrt{\omega_{r2}^2-\alpha 2^2}$ are natural frequencies.

[0038] In some embodiments, for a WBG power semiconductor device operating at a particular switching frequency (f_s), the resonant inductors L_{ron} and L_{roff} may be tuned such that the resonant frequencies of the crosstalk suppressing circuit are in a range of 0.1-2% of switching period $T_s=1/f_s$.

[0039] FIG. **4** shows waveforms of the control signal G, switching states of SW**1** and SW**2**, the gate-source voltage V_{gs} of the WBG power semiconductor device **Q1**, and the gate current i_g. As shown, the gate driving circuit can generate a bipolar gate-source voltage V_{gs} with a stable positive voltage V_{dc} and an adjustable negative voltage $-V_e$ from a unipolar auxiliary source V_{dc} for a chosen wide band gap device.

[0040] For instance, only a +5 V unipolar voltage source is required to generate a Vgs with amplitude of +5/−3 V for a GaN device; and only a +15V unipolar voltage source is required to generate a V_{gs} with amplitude of of +15/−4V for a SiC device.

[0041] FIG. **5** shows the flow chart of key design steps for the gate driving circuit, starting with the selection of WBG power semiconductor device, switching devices and diodes, followed by calculations based on all the design equations (1)-(4) and crosstalk suppression check.

[0042] Table 1 shows a summary table of exemplary parameters of a gate driving circuit for driving a WBG SiC device having an input capacitance C_{iss} of 3863 pF operating at a switching frequency of 50 kHz with a unipolar DC voltage source of 15 V amplitude. Preferably, the resonant inductor L_{ron} has an inductance of 100 nH; the resonant inductor L_{roff} has an inductance of 300 nH; the resistor R_{ron} has a resistance of 1 Ω; and the resistor R_{roff} has a resistance of 3 Ω.

TABLE 1

Exemplary parameters of a gate driving circuit

Parameters	Values
V_{dc}	15 V
C_{iss}	3863 pF
L_{ron}	100 nH
L_{roff}	300 nH
R_{on}	1 Ω
R_{off}	3 Ω
f_{sw}	50 kHz

[0043] The experimental results in FIG. **6** show that the achieved turn-on transition period t_{ron} and the turn-off transition period t_{roff} are 130 ns and 170 ns, respectively. With the use of the gate drive circuit **100**, the input capacitance C_{iss} is charged and discharged sinusoidally based on the series resonance principle in each switching transition. Moreover, the utilization of two different inductors L_{ron}, L_{roff} offers distinct dv/dt control during turn-on and turn-off transitions of WBG power semiconductor devices operating at high switching frequencies and allows energy recycling between L_{ron}, L_{roff} and C_{iss} during each switching transitions.

[0044] Therefore, V_{gs} of WBG power semiconductor device is stabilized after each switching transition. Moreover, the provided gate driving circuit is more compact and has a low bill of materials (BOM) cost. It consumes lesser power and produces negligible harmonics, thus has less electromagnetic interference (EMI) issues.

[0045] The experimental results in FIG. **7** show the V_{gs} of two WBG power semiconductor devices **Q1**, **Q2** in one leg configuration of a half bridge converter driven by the gate driver circuit where crosstalk is entirely suppressed.

[0046] Preferably, referring to FIG. **2**, the semiconductor switching device SW**1** is a p-channel MOSFET having a source being the high voltage terminal of the semiconductor switching device SW**1**; a drain being the low voltage terminal of the semiconductor switching device SW**1**; and a gate being the control terminal of the semiconductor switching device SW**1**. The semiconductor switching device SW**2** is a n-channel MOSFET having a drain being the high voltage terminal of the semiconductor switching device SW**2**; a source being the low voltage terminal of the semiconductor switching device SW**2**; and a gate being the control terminal of the semiconductor switching device SW**2**.

[0047] FIG. **8** shows a circuit diagram of a gate driving circuit **200** according to another embodiment of the present invention. The gate driving circuit **200** is similar to the gate driving circuit **100** except that the semiconductor switching device SW**1** is a n-channel MOSFET having a drain being the high voltage terminal of the semiconductor switching device SW**1**; a source being the low voltage terminal of the semiconductor switching device SW**1**; and a gate being the control terminal of the semiconductor switching device SW**1**.

[0048] FIG. **9** shows a circuit diagram of a gate driving circuit **300** according to another embodiment of the present invention. The gate driving circuit **300** is similar to the gate

driving circuit **100** except that the semiconductor switching device SW**1** is a npn bipolar junction transistor having a collector being the high voltage terminal of the semiconductor switching device SW**1**; an emitter being the low voltage terminal of the semiconductor switching device SW**1**; and a base being the control terminal of the semiconductor switching device SW**1**. And the semiconductor switching device SW**2** is a pnp bipolar junction transistor having an emitter being the high voltage terminal of the semiconductor switching device SW**2**; a collector being the low voltage terminal of the semiconductor switching device SW**2**; and a base being the control terminal of the semiconductor switching device SW**2**.

[0049] FIG. **10** shows a circuit diagram of a gate driving circuit **400** according to another embodiment of the present invention. The gate driving circuit **400** is similar to the gate driving circuit **100** except that the resonant inductor L_{roff} is a variable inductor and the resistor R_{roff} is a variable resistor. With the variable resonant inductor L_{roff} and resistor R_{roff}, the negative gate to source voltage $-V_e$ and the turn-off transition period can be fine-tuned in practical implementations.

[0050] FIG. **11** shows a circuit diagram of a gate driving circuit **500** according to another embodiment of the present invention. The gate driving circuit **500** is similar to the gate driving circuit **100** except that the resonant inductor L_{ron} and the resonant inductor L_{roff} are coupled inductor with galvanic isolation to save the component count.

[0051] FIG. **12** shows a circuit diagram of a gate driving circuit **600** according to another embodiment of the present invention. The gate driving circuit **600** is similar to the gate driving circuit **100** except that the protection circuit may include a first Zener diode Zp**1** and a second Zener diode Zp**2** connected back-to-back with the first Zener diode Zp**1**. More specifically, the first Zener diode Zp**1** has a cathode connected to the gate terminal of the WBG power semiconductor device Q**1**; the second Zener diode Zp**2** has an anode connected to the anode of the first Zener diode Zp**1** and a cathode connected to the source terminal of the WBG power semiconductor device Q**1**.

[0052] FIG. **13** shows a circuit diagram of a gate driving circuit **700** according to another embodiment of the present invention. The gate driving circuit **700** is similar to the gate driving circuit **100** except that the semiconductor switching devices SW**1** and SW**2** are driven by pulsed signals for further reducing the driver power consumption.

[0053] FIG. **14** shows a circuit diagram of a CLLC resonant converter-based battery energy storage system constructed with the gate driving circuits according to the embodiments of the present invention. As shown, the CLLC resonant converter-based battery energy storage system comprises one or more gate driving circuits Dr**1**-Dr**8** configured for driving one or more wide band gap power devices Sp**1**-Sp**4** and Ss**1**-Ss**4**, respectively.

[0054] FIG. **15** shows a circuit diagram of a wireless power transfer system with an AC/DC hard-switched converter **1501** and a DC/DC hard-switched converter **1502**, both converters are constructed with the gate driving circuits according to the embodiments of the present invention. As shown, the AC/DC hard-switched converter **1501** comprises gate driving circuits Dr**1**-Dr**4** configured for driving wide bandgap power devices S_1-S_4, respectively; and the DC/DC hard-switched converter **1502** comprises gate driving circuits Dr**5**-Dr**8** configured for driving wide bandgap power devices Q_{p1}-Q_{p4}, respectively.

[0055] While the present disclosure has been described and illustrated with reference to specific embodiments thereof, these descriptions and illustrations are not limited. The illustrations may not necessarily be drawn to scale. There may be distinctions between the artistic renditions in the present disclosure and the actual apparatus due to manufacturing processes and tolerances. There may be other embodiments of the present disclosure which are not specifically illustrated. Modifications may be made to adapt a particular situation, material, composition of matter, method, or process to the objective and scope of the present disclosure. All such modifications are intended to be within the scope of the claims appended hereto. While the methods disclosed herein have been described with reference to particular operations performed in a particular order, it will be understood that these operations may be combined, sub-divided, or re-ordered to form an equivalent method without departing from the teachings of the present disclosure. Accordingly, unless specifically indicated herein, the order and grouping of the operations are not limited.

What is claimed is:

1. A gate driving circuit for driving a wide bandgap power device, comprising:

a DC voltage source;

a first semiconductor switching device having a high voltage terminal connected to a positive terminal of the DC voltage source and a control terminal connected to a controller output;

a second semiconductor switching device having a low voltage terminal connected to a negative terminal of the DC voltage source and a control terminal connected to a controller output; and

a crosstalk suppressing circuit including:

a first resonant inductor having a first end connected to a low voltage terminal of the first semiconductor switching device;

a first resistor having a first end connected to a second end of the first resonant inductor and a second end connected to a gate of the WBG power semiconductor device;

a first diode having an anode terminal connected to the gate of the WBG power semiconductor device and a cathode terminal connected to a positive terminal of the DC voltage source;

a second diode having a cathode connected to a high voltage terminal of the second semiconductor switching device;

a second resonant inductor having a first end connected to an anode of the second diode; and

a second resistor having a first end connected to a second end of the second resonant inductor and a second end connected to a gate of the WBG power semiconductor device; and

wherein the first resonant inductor and the first resistor are configured to form a path for charging an input capacitance of the WBG power semiconductor device up to the DC voltage source when a logic high control signal is generated from the controller output and applied to the gate terminal of first and second semiconductor switches; and

wherein the first diode is configured to clamp a gate-to-source voltage of the WBG power semiconductor device to the DC voltage source to serve as a protection; and

wherein the second diode, the second resonant inductor, and the second resistor are configured to form a path for discharging the input capacitance of WBG power semiconductor device, and to provide an adjustable negative gate-source turnoff voltage to the WBG power semiconductor device when a logic low control signal is generated from the controller output and applied to the gate terminal of first and second semiconductor switches.

2. The gate driving circuit according to claim **1**, wherein

the first semiconductor switching device is a p-channel MOSFET having a source being the high voltage terminal of the first semiconductor switching device; a drain being the low voltage terminal of the first semiconductor switching device; and a gate being the control terminal of the first semiconductor switching device; and

the second semiconductor switching device is a n-channel MOSFET having a drain being the high voltage terminal of the second semiconductor switching device; a source being the low voltage terminal of the second semiconductor switching device; and a gate being the control terminal of the second semiconductor switching device.

3. The gate driving circuit according to claim **1**, wherein

the first semiconductor switching device is a n-channel MOSFET having a drain being the high voltage terminal of the first semiconductor switching device; a source being the low voltage terminal of the first semiconductor switching device; and a gate being the control terminal of the first semiconductor switching device; and

the second semiconductor switching device is a n-channel MOSFET having a drain being the high voltage terminal of the second semiconductor switching device; a source being the low voltage terminal of the second semiconductor switching device; and a gate being the control terminal of the second semiconductor switching device.

4. The gate driving circuit according to claim **1**, wherein

the first semiconductor switching device is a npn bipolar junction transistor having a collector being the high voltage terminal of the first semiconductor switching device; an emitter being the low voltage terminal of the first semiconductor switching device; and a base being the control terminal of the first semiconductor switching device; and

the second semiconductor switching device is a pop bipolar junction transistor having an emitter being the high voltage terminal of the second semiconductor switching device; a collector being the low voltage terminal of the second semiconductor switching device; and a base being the control terminal of the second semiconductor switching device.

5. The gate driving circuit according to claim **1**, wherein the second resonant inductor is a variable inductor, and the second resistor is a variable resistor.

6. The gate driving circuit according to claim **1**, wherein the first and second resonant inductors are coupled inductors.

7. The gate driving circuit according to claim **1**, further comprising a protection circuit across the gate and source terminals of the WBG power semiconductor device.

8. The gate driving circuit according to claim **1**, wherein the protection circuit includes a diode having a cathode connected to the gate of the WBG power semiconductor device; and a Zener diode having an anode connected to an anode of the diode and a cathode connected to the source terminal of the WBG power semiconductor device.

9. The gate driving circuit according to claim **1**, wherein the protection circuit includes a first Zener diode having a cathode connected to the gate of the WBG power semiconductor device; and a second Zener diode having an anode connected to an anode of the first Zener diode and a cathode connected to the source terminal of the WBG power semiconductor device.

10. A CLLC resonant converter-based battery energy storage system comprising one or more gate driving circuits of claim **1** configured for driving one or more wide band gap power devices respectively.

11. The CLLC resonant converter-based battery energy storage system according to claim **9**, wherein

the first semiconductor switching device is a p-channel MOSFET having a source being the high voltage terminal of the first semiconductor switching device; a drain being the low voltage terminal of the first semiconductor switching device; and a gate being the control terminal of the first semiconductor switching device; and

the second semiconductor switching device is a n-channel MOSFET having a drain being the high voltage terminal of the second semiconductor switching device; a source being the low voltage terminal of the second semiconductor switching device; and a gate being the control terminal of the second semiconductor switching device.

12. The CLLC resonant converter-based battery energy storage system according to claim **9**, wherein the second resonant inductor is a variable inductor; and the second resistor is a variable resistor.

13. The CLLC resonant converter-based battery energy storage system according to claim **9**, wherein the protection circuit includes a diode having a cathode connected to the gate of the WBG power semiconductor device; and a Zener diode having an anode connected to an anode of the diode and a cathode connected to the source terminal of the WBG power semiconductor device.

14. The CLLC resonant converter-based battery energy storage system according to claim **9**, wherein the protection circuit includes a first Zener diode having a cathode connected to the gate of the WBG power semiconductor device; and a second Zener diode having an anode connected to an anode of the first Zener diode and a cathode connected to the source terminal of the WBG power semiconductor device.

15. A wireless power transfer system having an AC/DC hard-switched converter and a DC/DC hard-switched converter, each of the AC/DC hard-switched converter and the DC/DC hard-switched converter comprising one or more gate driving circuits of claim **1** configured for driving one or more wide band gap power devices respectively.

16. The wireless power transfer system according to claim **15**, wherein

the first semiconductor switching device is a p-channel MOSFET having a source being the high voltage

terminal of the first semiconductor switching device; a drain being the low voltage terminal of the first semiconductor switching device; and a gate being the control terminal of the first semiconductor switching device; and

the second semiconductor switching device is a n-channel MOSFET having a drain being the high voltage terminal of the second semiconductor switching device; a source being the low voltage terminal of the second semiconductor switching device; and a gate being the control terminal of the second semiconductor switching device.

17. The wireless power transfer system according to claim **15**, wherein the second resonant inductor is a variable inductor, and the second resistor is a variable resistor.

18. The wireless power transfer system according to claim **15**, wherein the first and second resonant inductors are coupled inductors.

19. The wireless power transfer system according to claim **15**, wherein the protection circuit includes a diode having a cathode connected to the gate of the WBG power semiconductor device; and a Zener diode having an anode connected to an anode of the diode and a cathode connected to the source terminal of the WBG power semiconductor device.

20. The wireless power transfer system according to claim **15**, wherein the protection circuit includes a first Zener diode having a cathode connected to the gate of the WBG power semiconductor device; and a second Zener diode having an anode connected to an anode of the first Zener diode and a cathode connected to the source terminal of the WBG power semiconductor device.

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