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(54) **ENLARGING SPACER THICKNESS BY FORMING A DIELECTRIC LAYER OVER A RECESSED INTERLAYER DIELECTRIC**

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See application file for complete search history.

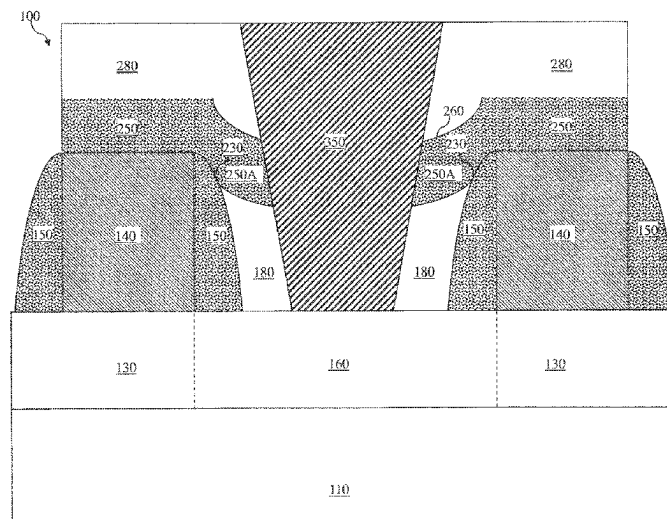
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(57) **ABSTRACT**

An exemplary semiconductor device includes first spacers disposed along sidewalls of a first gate structure and second spacers disposed along sidewalls of a second gate structure. A source/drain region is disposed between the first gate structure and the second gate structure. A first ILD layer is disposed between the first spacers and the second spacers. A portion of the first ILD layer has a first recessed upper surface. A dielectric layer is disposed over the first spacers, the second spacers, and the first recessed upper surface of the first ILD layer. A portion of the dielectric layer has a second recessed upper surface that is disposed over the portion of the first ILD layer having the first recessed upper surface. A second ILD layer is disposed over the dielectric layer. A contact extends through the second ILD layer, the dielectric layer, and the first ILD layer to the source/drain region.

**20 Claims, 9 Drawing Sheets**



**Related U.S. Application Data**

continuation of application No. 16/166,762, filed on Oct. 22, 2018, now Pat. No. 10,679,989, which is a division of application No. 15/063,907, filed on Mar. 8, 2016, now Pat. No. 10,109,627.

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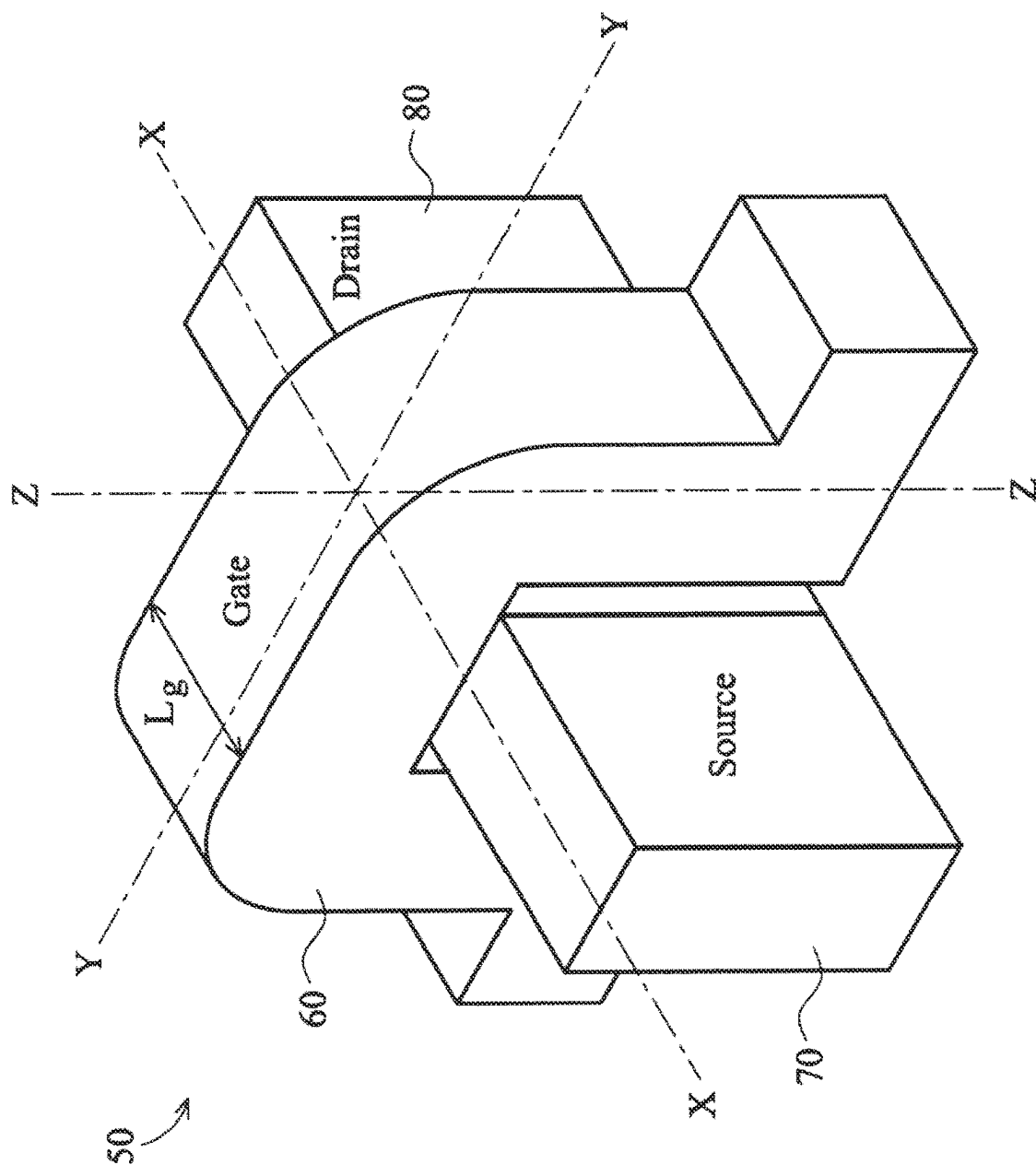


Fig. 1

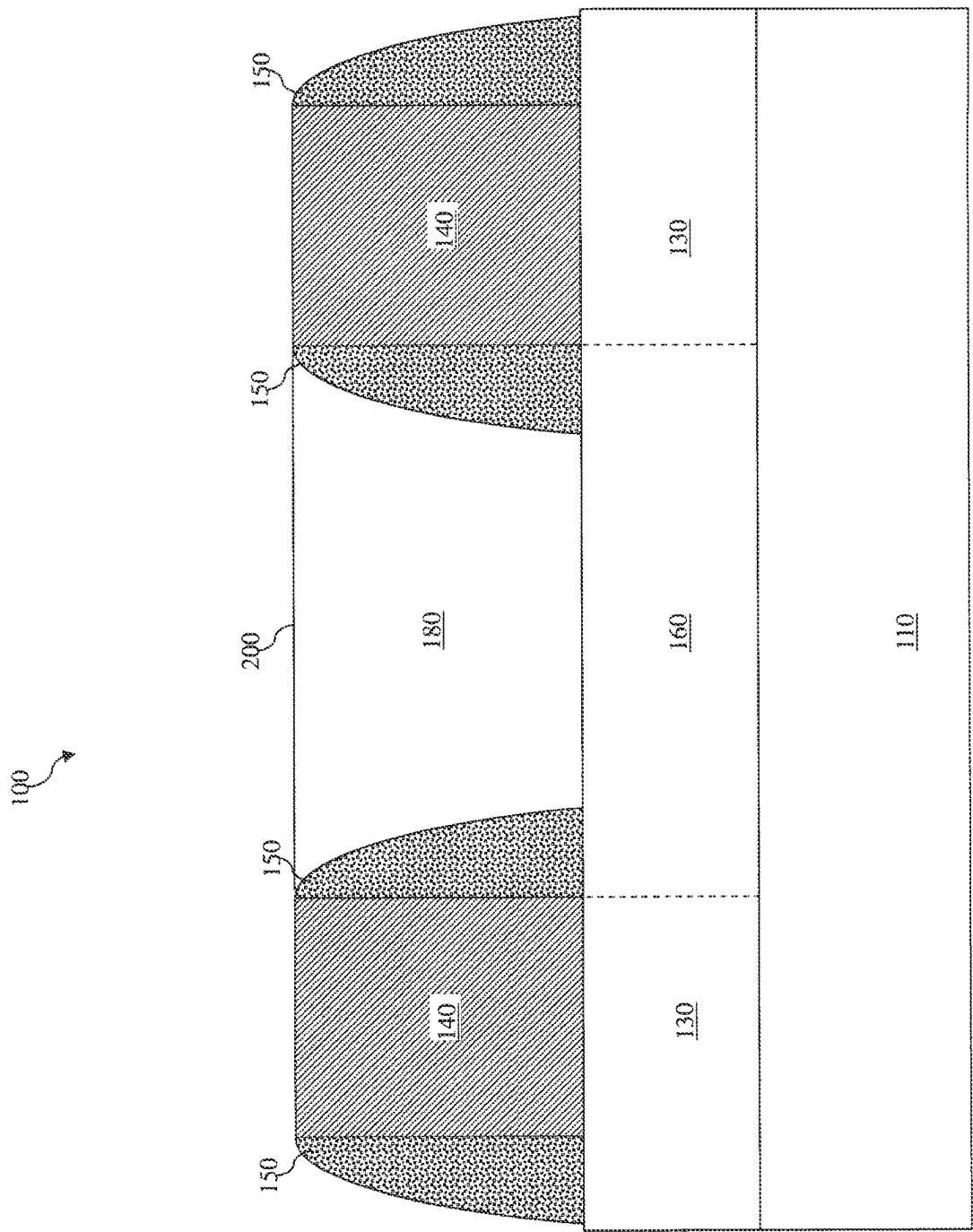


Fig. 2

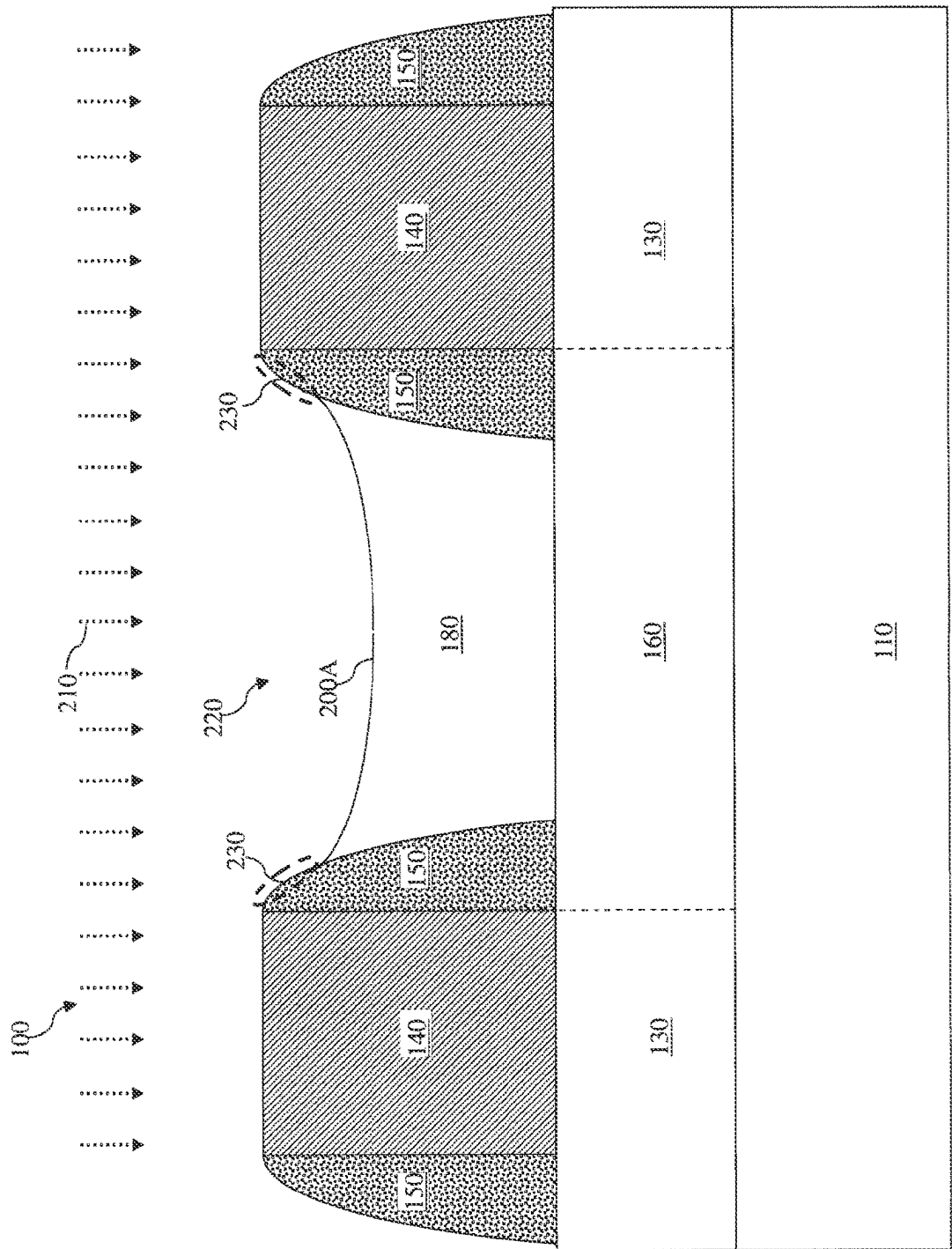


Fig. 3

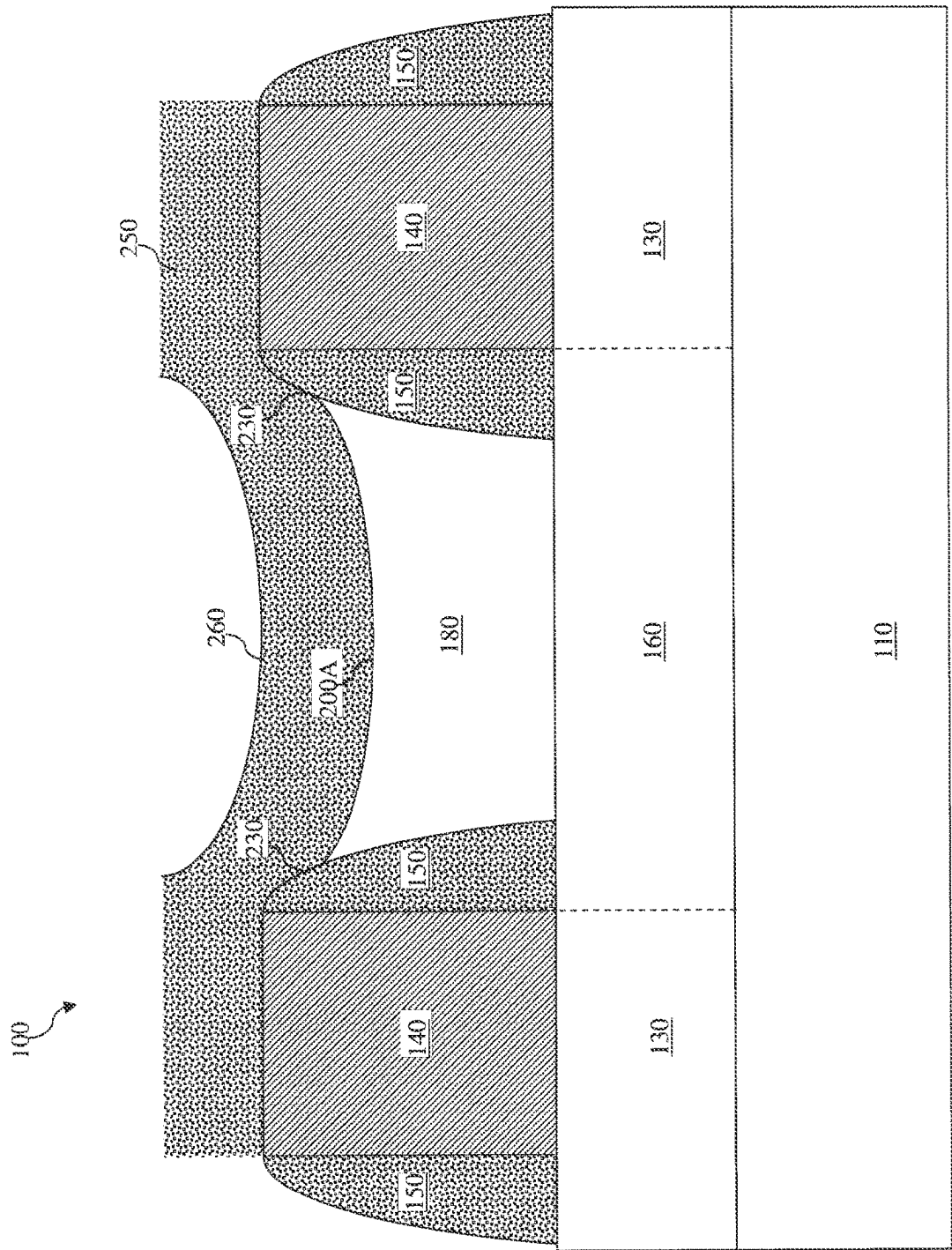


Fig. 4

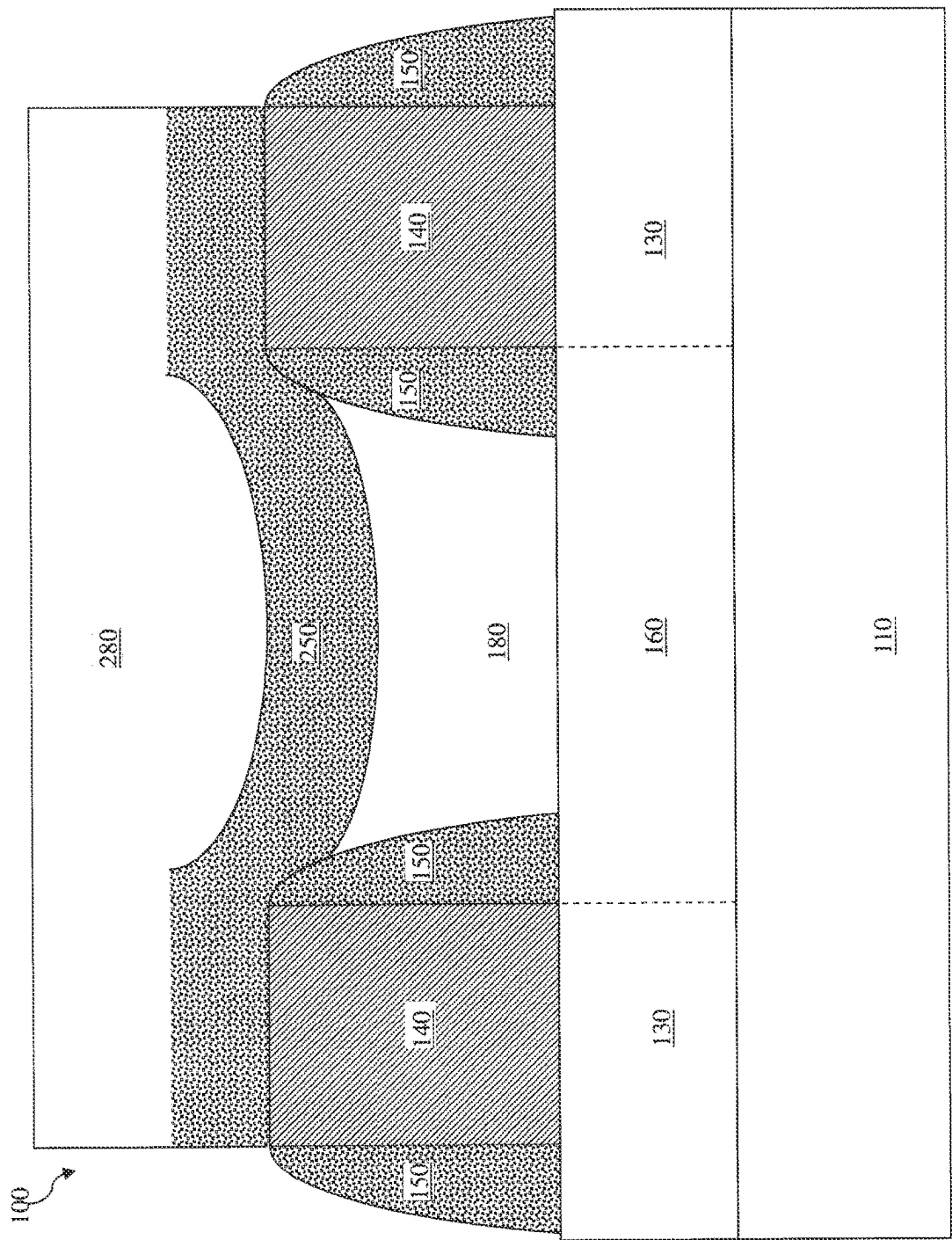


Fig. 5

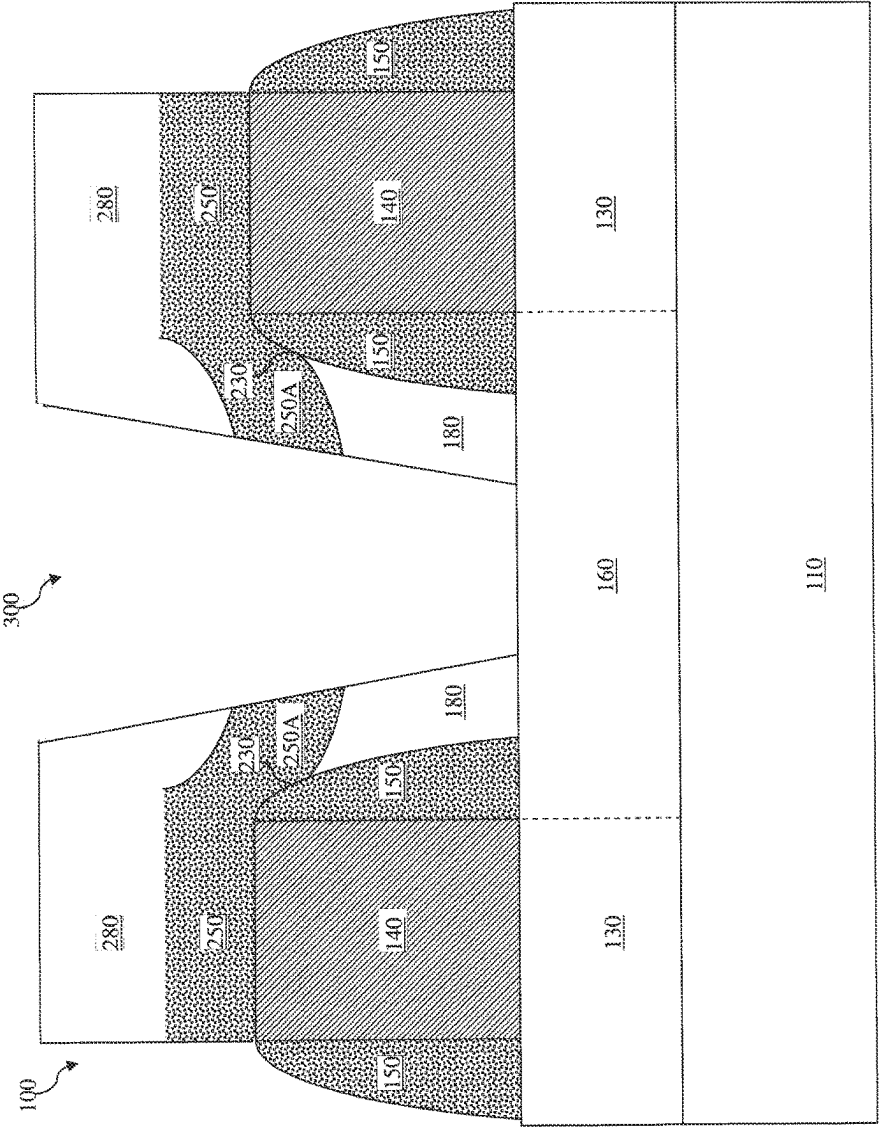


Fig. 6



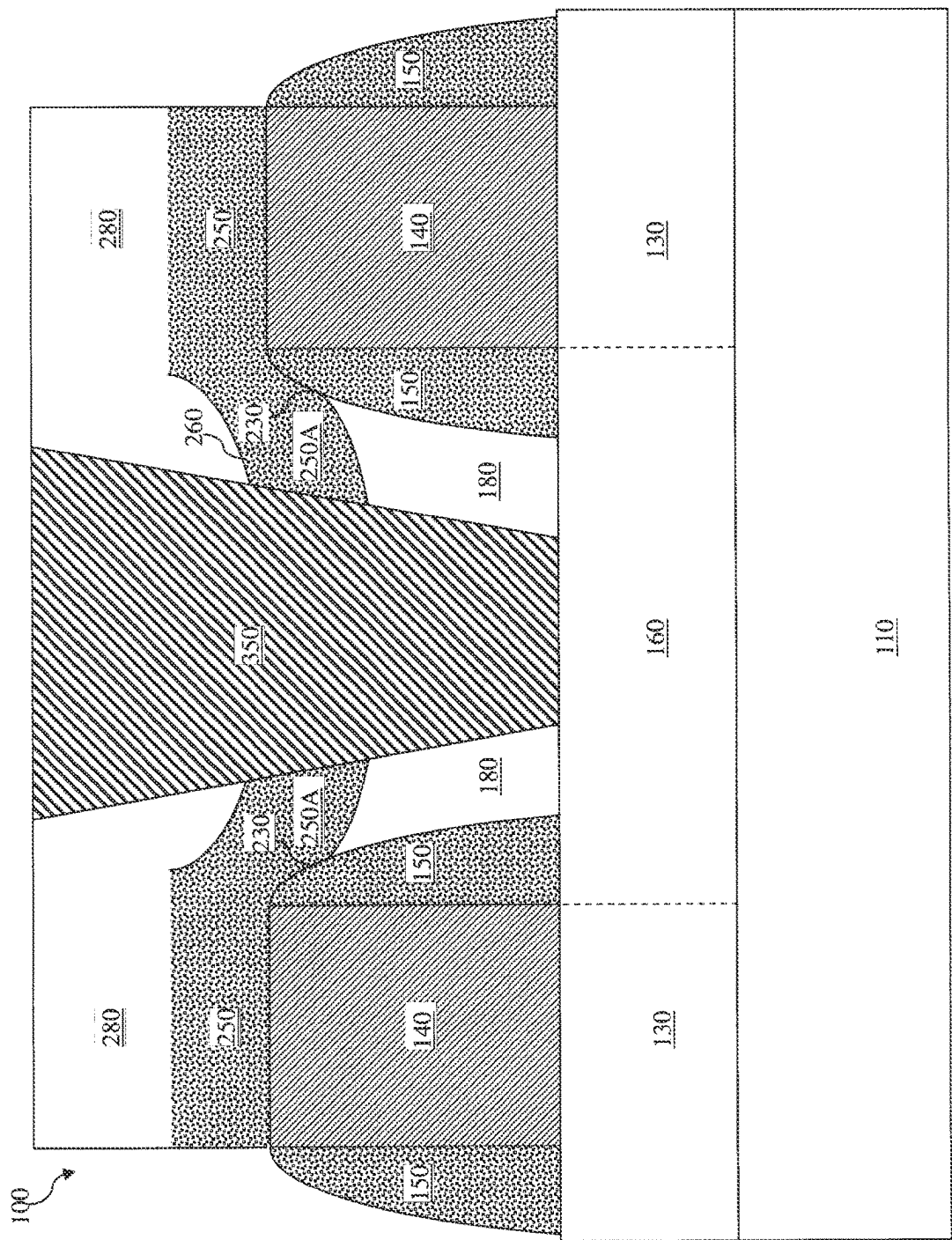
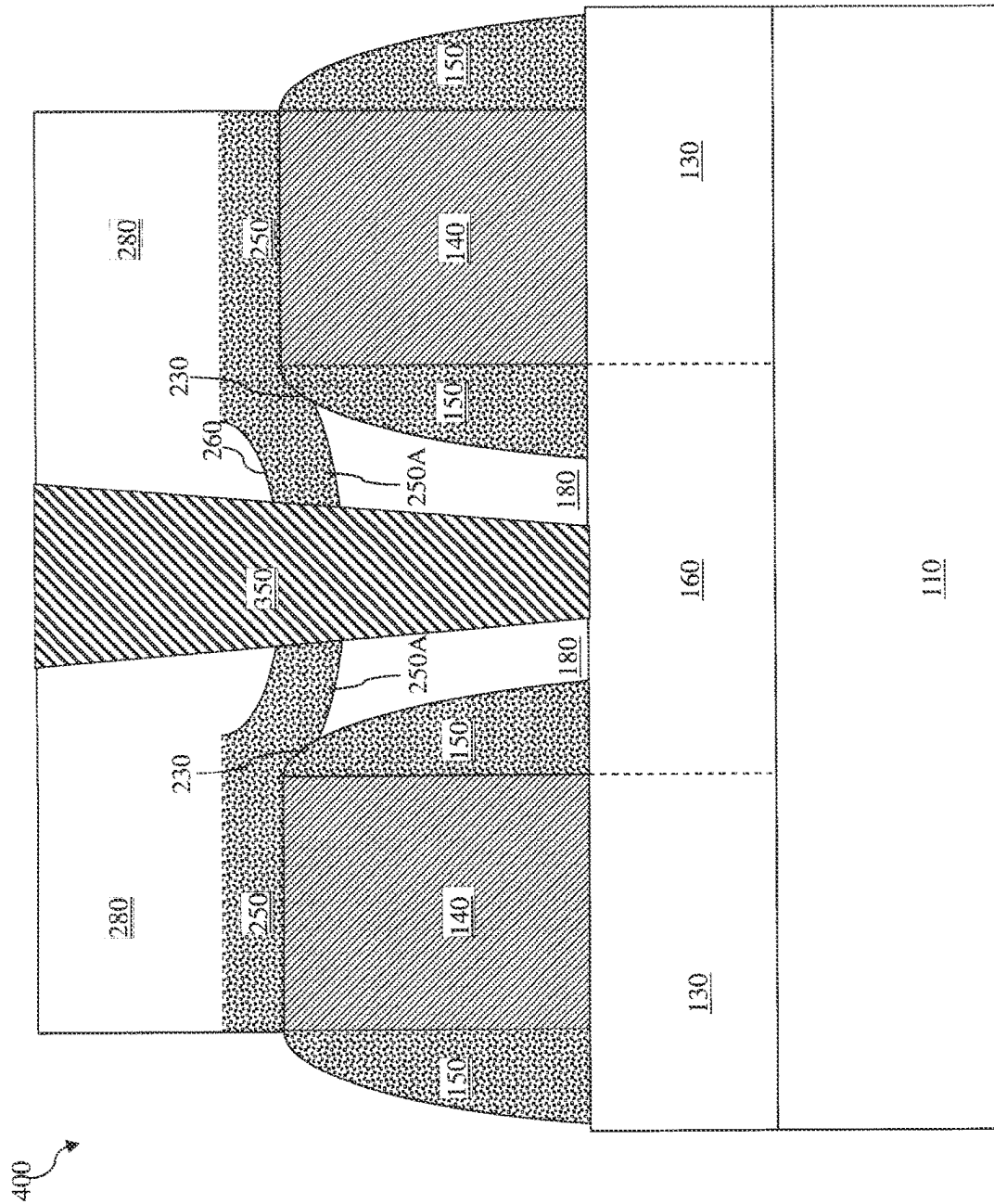


Fig. 7



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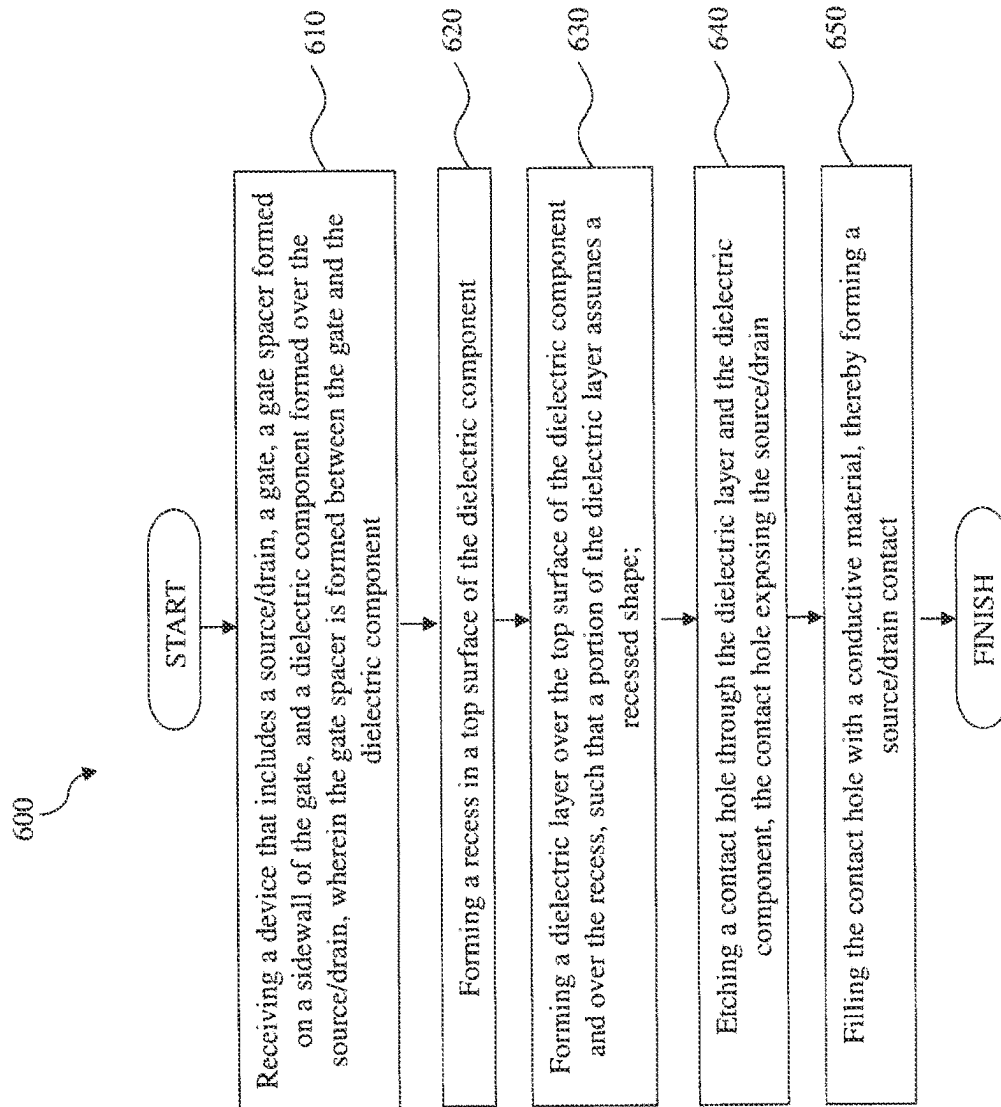


Fig. 9

# ENLARGING SPACER THICKNESS BY FORMING A DIELECTRIC LAYER OVER A RECESSED INTERLAYER DIELECTRIC

This is a divisional application of U.S. patent application Ser. No. 16/891,992, filed Jun. 3, 2020, which is a continuation application of U.S. patent application Ser. No. 16/166,762, filed Oct. 22, 2018, now U.S. Pat. No. 10,679,989, which is a divisional application of U.S. patent application Ser. No. 15/063,907, filed Mar. 8, 2016, now U.S. Pat. No. 10,109,627, the entire disclosures of which are incorporated herein by reference.

## BACKGROUND

The semiconductor integrated circuit (IC) industry has experienced rapid growth. Technological advances in IC materials and design have produced generations of ICs where each generation has smaller and more complex circuits than the previous generation. However, these advances have increased the complexity of processing and manufacturing ICs and, for these advances to be realized, similar developments in IC processing and manufacturing are needed. In the course of integrated circuit evolution, functional density (i.e., the number of interconnected devices per chip area) has generally increased while geometry size (i.e., the smallest component (or line) that can be created using a fabrication process) has decreased.

The ever-shrinking geometry size brings challenges to semiconductor fabrication. For example, misalignment between microelectronic components (such as misalignment between a source/drain and a conductive contact formed thereover) during fabrication may occur, which may damage the semiconductor device or degrade its performance. In addition, the smaller device sizes may lead to more significant parasitic capacitance, which could also negatively affect semiconductor device performance.

Therefore, while existing semiconductor devices and the fabrication thereof have been generally adequate for their intended purposes, they have not been entirely satisfactory in every aspect.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIG. 1 is a perspective view of an example semiconductor device.

FIGS. 2-8 are different cross-sectional side views of a semiconductor device according to various embodiments of the present disclosure.

FIG. 9 is a flowchart a method of fabricating a semiconductor device in accordance with embodiments of the present disclosure.

## DETAILED DESCRIPTION

It is understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely

examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the sake of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. Moreover, various features may be arbitrarily drawn in different scales for the sake of simplicity and clarity.

Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as being “below” or “beneath” other elements or features would then be oriented “above” the other elements or features. Thus, the exemplary term “below” can encompass both an orientation of above and below. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

The present disclosure is directed to, but not otherwise limited to, a fin-like field-effect transistor (FinFET) device. The use of FinFET devices has been gaining popularity in the semiconductor industry. A FinFET device, for example, may be a complementary metal-oxide-semiconductor (CMOS) device including a P-type metal-oxide-semiconductor (PMOS) FinFET device and an N-type metal-oxide-semiconductor (NMOS) FinFET device. In a typical FinFET device, a gate wraps around a fin structure, in which the source and drain are formed. However, due at least in part to the narrowness of the fin structure, it may be challenging to align the source/drain with a conductive source/drain contact hole to be formed thereabove. A lateral shift of the source/drain contact hole (i.e., misalignment) may inadvertently damage the gate, as the etching process used to form the source/drain contact hole may cause the gate to be undesirably etched as well.

To improve the alignment between the source/drain contact with the source/drain, the present disclosure forms a recessed dielectric layer that effectively serves as an “extra gate spacer”. This “extra gate spacer” protects the gate from being inadvertently etched. The various aspects of the present disclosure are discussed below with reference to FIGS. 1-9. It is understood that the following disclosure will continue with one or more FinFET examples to illustrate various embodiments of the present invention. It is understood, however, that the application should not be limited to a particular type of device, except as specifically claimed.

Referring to FIG. 1, a perspective view of an example FinFET device 50 is illustrated. The FinFET device 50 is a non-planar multi-gate transistor that is built on a substrate. A thin silicon “fin-like” structure (referred to as fin) forms the body of the FinFET device 50. A gate 60 of the FinFET device 50 is wrapped around this fin. Lg denotes a length (or width, depending on the perspective) of the gate 60. A source 70 and a drain 80 of the FinFET device 50 are formed in extensions of the fin on opposite sides of the gate 60. The fin

itself serves as a channel. The effective channel length of the FinFET device **50** is determined by the dimensions of the fin.

FinFET devices offer several advantages over traditional Metal-Oxide Semiconductor Field Effect Transistor (MOS-FET) devices (also referred to as planar devices). These advantages may include better chip area efficiency, improved carrier mobility, and fabrication processing that is compatible with the fabrication processing of planar devices. Thus, it may be desirable to design an integrated circuit (IC) chip using FinFET devices for a portion of, or the entire IC chip.

Referring now to FIG. 2, a semiconductor device **100** is illustrated. The semiconductor device **100** shown in FIG. 2 is a diagrammatic cross-sectional side view of a FinFET device taken along the X-Z plane of FIG. 1. The semiconductor device **100** includes a substrate **110**. In an embodiment, the substrate **110** includes a dielectric material, for example silicon oxide ( $\text{SiO}_2$ ). In other embodiments, the substrate **110** may include another suitable material, for example a semiconductor material.

A semiconductor layer **130** is formed on the substrate **110**. In an embodiment, the semiconductor layer **130** includes a crystal silicon material. It is understood that the semiconductor layer **130** may include other suitable materials in alternative embodiments. An implantation process may be performed to implant a plurality of dopant ions to the semiconductor layer **130**. The dopant ions may include an n-type material in some embodiments, for example arsenic (As) or phosphorous (P), or they may include a p-type material in some other embodiments, for example boron (B), depending on whether an NMOS or a PMOS is needed. After the implantation process is performed, a doping concentration level in the semiconductor layer **130** is in a range from about  $1 \times 10^{17}$  ions/cm<sup>3</sup> to about  $5 \times 10^{19}$  ions/cm<sup>3</sup> in some embodiments. In other embodiments, the doping concentration levels and the thickness of the substrate may be different.

The semiconductor layer **130** is patterned to form a fin structure (e.g., the fin structure shown in FIG. 1). The fin structure extends in an elongate manner along the X direction. As discussed previously, a portion of the fin structure will serve as a conductive channel for the semiconductor device **100**, and another portion of the fin structure will serve as the source/drain region of the semiconductor device **100**.

The semiconductor device **100** includes gate structures **140**. The gate structures **140** are formed to wrap around the fin structure in the manner as shown in FIG. 1. However, since FIG. 2 illustrates the cross-sectional side view of the FinFET device taken across the X-Z plane (i.e., cutting the FinFET device on the fin structure), only a portion of each of the gate structures **140** is shown. That is, FIG. 2 shows the portion of the gate structures **140** disposed over the fin structure, but not the portion of the gate structures **140** disposed beside the fin structure.

Each gate structure **140** includes a respective gate dielectric layer that is formed around the fin structure and a gate electrode layer that is formed on the gate dielectric layer. The gate dielectric layer and the gate electrode layer may each be formed using a deposition process known in the art, for example chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), combinations thereof, or another suitable process.

In some embodiments, the gate structures **140** are high-k metal gate structures. In these embodiments, the gate dielectric layer contains a high-k dielectric material. A high-k dielectric material is a material having a dielectric constant that is greater than a dielectric constant of  $\text{SiO}_2$ , which is

approximately 4. In an embodiment, the gate dielectric layer contains hafnium oxide ( $\text{HfO}_2$ ), which has a dielectric constant that is in a range from approximately 18 to approximately 40. In alternative embodiments, the gate dielectric layer may contain one of  $\text{ZrO}_2$ ,  $\text{Y}_2\text{O}_3$ ,  $\text{La}_2\text{O}_3$ ,  $\text{Gd}_2\text{O}_3$ ,  $\text{TiO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{HfErO}$ ,  $\text{HfLaO}$ ,  $\text{HfYO}$ ,  $\text{HfGdO}$ ,  $\text{HfAlO}$ ,  $\text{HfZrO}$ ,  $\text{HfTiO}$ ,  $\text{HfTaO}$ , and  $\text{SrTiO}$ . The gate electrode layer contains a metal or metal compound. For example, the gate electrode layer may contain titanium nitride (TiN) material, tungsten (W), tungsten nitride (WN), or tungsten aluminum (WAl), aluminum (Al), titanium (Ti), copper (Cu), or combinations thereof.

The formation of the high-k metal gate may involve a gate replacement process flow. In one embodiment of the gate replacement process flow, a dummy gate electrode layer (e.g., containing polysilicon) is formed on a high-k gate dielectric layer. After ion implantation processes are performed to form the source and drain regions (discussed below in more detail), the dummy gate electrode layer is removed, and then a metal gate electrode layer is formed in place of the dummy gate electrode layer. This gate replacement process flow may be referred to as a gate-last process flow. In another embodiment of the gate replacement process flow, a dummy gate dielectric layer (e.g., containing silicon oxide) is formed, and the dummy gate electrode layer is formed over the dummy gate dielectric layer. After ion implantation processes are performed to form the source and drain regions, the dummy gate dielectric layer and the dummy gate electrode layer are both removed. A high-k gate dielectric layer is formed to replace the dummy gate dielectric layer, and a metal gate electrode layer is formed to replace the dummy gate electrode layer. This gate replacement process flow may be referred to as a high-k-last process flow. As an example, the details of forming high-k metal gate structures are described in more detail in U.S. patent application Ser. No. 13/440,848, filed on Apr. 5, 2012, entitled "Cost-effective gate replacement process" to Zhu et al., which is issued as U.S. Pat. No. 8,753,931 on Jun. 17, 2014, the disclosure of which is hereby incorporated by reference in its entirety.

Gate spacers **150** are formed on sidewall surfaces of the gate structures **140**. The gate spacers **150** are formed by depositing a spacer material over the gate structures **140** and thereafter performing a patterning process (for example an etching process) on the spacer material. The spacer material may include a dielectric material. In an embodiment, the spacer material includes silicon oxide. In another embodiment, the spacer material includes silicon nitride.

Still referring to FIG. 2, a channel region is disposed below each of the gate structures **140** in a portion of the semiconductor layer **130**. A source/drain region **160** is formed in another portion of the semiconductor layer **130**, between the gate structures **140**. Alternatively stated, source/drain regions **160** (one of which is shown in FIG. 2) are formed on opposite sides of each of the gate structures **140**. In some embodiments, the source/drain region **160** may include a lightly doped source/drain region and a heavily doped source/drain region. The lightly doped source/drain region may be formed by an ion implantation process in which dopant ions are implanted into the portion of the fin structure located on either side (or opposite sides) of the gate structures **140**. The ion implantation process used to form the lightly doped source/drain region is performed before the gate spacers **150** are formed. After the formation of the gate spacers, another ion implantation process is performed to implant dopant ions into the portion of the fin structure not protected by the gate structures **140** or the gate spacers **150**.

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This ion implantation process forms the heavily doped source/drain regions, which have a greater dopant concentration level than the lightly-doped source/drain regions.

The semiconductor device **100** also includes an interlayer dielectric (ILD) **180**. In the embodiment illustrated in FIG. 2, the ILD **180** is disposed laterally adjacent to the gate spacers **150** and vertically above the source/drain region **160**. In some embodiments, the ILD **180** contains a low-k dielectric material (dielectric constant smaller than that of silicon oxide). For example, the low-k dielectric material may include fluorine-doped silicon dioxide, carbon-doped silicon dioxide, porous silicon dioxide, porous carbon-doped silicon dioxide, or a spin-on polymeric dielectric material. As is shown in FIG. 2, the ILD **180** has a planar (or flat) upper surface **200** that is co-planar with the upper surface of the gate structures **140**.

Referring now to FIG. 3, a process **210** is performed to the semiconductor device **100** to form a recess **220** in the upper surface **200** of the ILD. In some embodiments, the process **210** includes one or more etching processes. The etching processes may include a wet etching process, a dry etching process, or a combination thereof. The one or more etching processes are configured to etch away the material of the ILD **180** without substantially etching away the materials of the gate structures **140** or the gate spacers **150**. For example, this may be done by configuring the etchant to have a substantially higher etching rate with respect to the material of the ILD **180** than with respect to the materials of the gate structures **140** or the gate spacers **150**.

In some other embodiments, the process **210** includes one or more polishing processes such as a chemical mechanical polishing (CMP) process. The CMP process uses a carefully-tuned slurry that is different from the slurries in conventional CMP processes, so that the material of the ILD **180** is polished away at a faster rate than the materials of the gate structures **140** or the materials of the gate spacers **150**.

Regardless of how the process **210** is implemented, the result is that the partial removal of the ILD **180** causes an opening **220** to be formed over the ILD **180**. Or stated differently, the ILD **180** is “caved in” and has a recessed upper surface **200A**. The recessed upper surface **200A** slopes downward (toward the substrate **110**). The recessed upper surface **200A** may also have a downward curvature in some embodiments. In some embodiments, the removal of the ILD **180** causes an upper portion of the gate spacers **150** to be exposed to be opening **220**. In other words, the gate spacers **150** (that are disposed next to the ILD **180**) each have a portion **230** of a sidewall surface that is exposed.

It is understood that according to conventional semiconductor fabrication, the process **210** would not have been performed. The process **210** is performed according to the various aspects of the present disclosure in order to allow a subsequently formed dielectric layer to effectively enlarge the thickness of the gate spacers **150**, as discussed below in more detail.

Referring now to FIG. 4, a dielectric layer **250** is formed over the gate structures **140** and over the ILD **180**. The dielectric layer **250** at least partially fills the opening **220** and is in direct physical contact with the ILD **180** and the portions **230** of the upper sidewall surfaces of the gate spacers **150**. In some embodiment, the dielectric layer **250** is formed by a conformal deposition process, and as a result, an upper surface **260** of the dielectric layer **250** partially assumes the recessed shape or profile of the recessed upper surface **200A** of the ILD **180**. In other words, the dielectric layer **250** is also formed to have a recessed upper surface **260**. This allows portions of the dielectric layer **250** to be

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laterally disposed on the portions **230** of the sidewalls of the gate spacers **150**. In some embodiments, the dielectric layer **250** is an etching-stop layer (ESL) and has a different material composition than the ILD **180**. The dielectric layer **250** may or may not have the same material composition as the gate spacers **150**. In some embodiments, the dielectric layer **250** contains silicon nitride.

Referring now to FIG. 5, another dielectric layer **280** is formed over the dielectric layer **250**. The dielectric layer **280** may be formed by a suitable deposition process. The dielectric layer **280** is also considered an interlayer dielectric (ILD) and may be referred to as ILD **280** hereinafter. In some embodiments, the ILD **280** and the ILD **180** have the same material compositions, for example they may both contain a low-k dielectric material. However, the ILD **280** and the dielectric layer **250** have different material compositions.

Referring now to FIG. 6, a contact hole **300** is formed using various etching processes. The contact hole **300** extends vertically through the ILD **280**, the dielectric layer **250**, and the ILD **180**. The contact hole **300** exposes a portion of the source/drain region **160**. During the etching of the contact hole **300**, a portion **250A** of the dielectric layer **250** effectively serves as an extra gate spacer to protect the gate structures **140** from being damaged. In more detail, since the dielectric layer **250** is formed on the recessed upper surface **200A** (see FIG. 4) of the ILD **180**, the dielectric layer **250** assumes the recessed shape/profile of the upper surface **200A** of the ILD **180**, and a portion **250A** of the dielectric layer **250** disposed directly on the portion **230** of the sidewall of each of the gate spacers **150**. The portion **250A** of the dielectric layer **250** effectively “thickens” the gate spacers **150**. Alternatively stated, the gate spacers **150** may be viewed as having an increased lateral thickness at the top portions.

During the etching of the contact hole **300**, a lateral shift may occur. In more detail, the contact hole **300** may shift laterally toward either of the gate structures **140**. This is undesirable, because as the contact hole **300** shifts too close to either of the gate structure **140**s, the gate spacer **150** of that gate structure **140** may be “punched through.” In other word, enough of the gate spacers **150** may be etched away (due to the lateral shift of the contact hole **300**), so that they can no longer protect the gate structure **140** from being etched. As a result, the gate structure **140** may be damaged by the etching performed to form the contact hole **300**. However, since the portions **250A** of the dielectric layer **250** effectively “thickens” the gate spacers **150**, the “punch-through” of the gate spacers **150** is more difficult. Stated differently, even if the contact hole **300** is undesirably shifted laterally toward either of the gate structures **140**, the effectively “thicker” gate spacer **150** can more adequately prevent itself from being “punched through”, and thus the gate spacers **150** can better protect the gate structures **140** from being inadvertently damaged during the formation of the contact hole **300**.

Note that this would not have been possible if the ILD **180** had not been formed to have a recessed upper surface. Had the ILD **180** been left alone with a planar/flat upper surface **200** as shown in FIG. 2, the subsequent formation of the dielectric layer **250** thereon would have been over (or above) the gate spacers **150**. In other words, no portion of the dielectric layer **250** would have been formed on the sidewalls of the gate spacers **150**, and as such, the gate spacers **150** would not have had the increased lateral thickness as they do according to the present disclosure.

Referring now to FIG. 7, a source/drain contact **350** is formed in the contact hole **300**. The source/drain contact **350** may be formed by filling the contact hole **300** with a conductive material, for example via a deposition process, and then polishing away the excess portions of the conductive material outside the contact hole **300**. The remaining portion of the conductive material forms the source/drain contact **350**. In some embodiments, the source/drain contact **350** contains tungsten. In other embodiments, the source/drain contact **350** contains aluminum or copper. The source/drain contact **350** is electrically coupled to the source/drain **160** (e.g., through physical contact) and provides electrical connectivity to the source/drain **160**.

Since the source/drain contact **350** and the gate electrode of the structure **140** are both conductive, and since the materials disposed therebetween (e.g., the ILD **180** and the gate spacers **150**) are dielectric, this leads to parasitic capacitance, as capacitance arises when a dielectric material is disposed between two conductive plates. Capacitance is inversely correlated to a distance between the two conductive plates. In other words, as the distance increases between the two conductive plates, capacitance decreases; as the distance decreases between the two conductive plates, capacitance increases. In a conventionally fabricated semiconductor device, the lateral shift of the source/drain contact hole decreases the distance between the two conductive plates (i.e., the source/drain contact **350** and the gate structure **140**). The gate spacer **150** may help prevent the source/drain contact hole from being etched too close to the gate structure **140**, but since the gate spacer **150** is thin (especially at the top), this may not be sufficient. Consequently, parasitic capacitance arising from the source/drain contact **350** being formed too close (i.e., small distance) to the gate structure **140** may become significant, especially as semiconductor device sizes get smaller with each technology generation. This parasitic capacitance adversely affects semiconductor device performance.

In comparison, the present disclosure reduces the parasitic capacitance by effectively “enlarging” the spacers **150** with the portions **250A** of the dielectric layer **250** disposed on the sidewalls **230** of the spacers **150**. Due to the “enlarged” or “thicker” spacers **150**, it is more difficult for the source/drain contact hole to punch it through. In other words, the source/drain contact hole is formed in a more self-aligned manner (i.e., better vertically aligned with the source/drain region **160**). Thus, the effective distance between the source/drain contact **350** and the gate electrode of the gate structure **140** is increased, compared to a scenario in prior fabrication where lateral shift of the source/drain contact made such distance too small.

It is understood that the amount or degree of recess formed in the ILD **180** may be dependent on the type of semiconductor device **100**. For example, the semiconductor device **100** may be an Input/Output (I/O) device. I/O devices include devices that handle the input and/or output voltages/currents, and as such they need to be able to tolerate a greater amount of voltage or current swing than non-I/O devices. In comparison, non-I/O devices may include core devices, which may include logic devices (that do not need to handle the input/output voltages/currents directly). For example, the core devices may include various logic gates such as NAND, NOR, INVERTER, etc. In some embodiments, the core devices include an SRAM (static random-access memory) region.

One physical difference between the I/O device and the non-I/O device is that the distance between adjacent gate structures is longer for an I/O device than for a non-I/O

device. In other words, the ILD **180** for an I/O device is wider than the ILD for a non-I/O device. For example, FIG. **8** illustrates a semiconductor device **400** that is a non-I/O device (e.g., a core device) but is otherwise similar to the I/O device **100** of FIG. 7. The non-I/O device **400** undergoes substantially similar fabrication processes discussed above with reference to FIGS. 2-7 to form the I/O device **100**. Therefore, for reasons of clarity and consistency, similar components will be labeled the same for the non-I/O device **400** of FIG. **8** and for the I/O device **100** of FIG. 7.

In addition to the differences in ILD widths, another difference between the non-I/O device **400** in FIG. **8** and the I/O device **100** in FIG. 7 is that the non-I/O device **400** has a less recessed ILD **180** (and thus a less recessed dielectric layer **250**) than the I/O device **100**. In some embodiments, the less recessed ILD **180** means that the upper surface of the ILD **180** (or the upper surface **260** of the dielectric layer **250**) of the non-I/O device **400** is shallower than the upper surface of the ILD **180** (or the upper surface **260** of the dielectric layer **250**) of the I/O device **100**. For example, the difference between the ILD depths for the I/O device **100** and the non-I/O device **400** is at least 1 nm. In other embodiments, the less recessed ILD **180** also means that the upper surface of the ILD **180** of the non-I/O device **400** is less curved than the upper surface of the ILD **180** of the I/O device **100**. The same may be said about the upper surface **260** of the dielectric layer **250** for the I/O device **100** and the non-I/O device **400**.

One reason for the more recessed ILD **180** for the I/O device **100** is that I/O devices need to handle greater amounts of voltage/current, and parasitic capacitance may be a greater concern in that situation. Thus, the more recessed ILD **180** for the I/O device **100** can better alleviate the concerns of parasitic capacitance by making sure that enough dielectric material will be formed on the upper sidewalls of the spacers (due to the more recessed ILD), which effectively thickens the spacer **150** as discussed above.

It is understood that additional fabrication processes may be performed to complete the fabrication of the semiconductor device **100**. For example, gate contacts may be formed, and a multi-layered interconnect structure containing a plurality of metal lines and vias may also be formed. The semiconductor device **100** may also undergo packaging and testing processes. For reasons of simplicity, these additional processes are not discussed in detail herein. In addition, though the processes discussed above with reference to FIGS. 1-8 are performed using a FinFET as an example semiconductor device, it is understood that the various aspects of the present disclosure (and their benefits) also apply to “planar” non-FinFET devices as well.

FIG. 9 is a flowchart of a method **600** for fabricating a semiconductor device in accordance with embodiments of the present disclosure. The method **600** includes a step **610** of receiving a device that includes a source/drain, a gate, a gate spacer formed on a sidewall of the gate, and a dielectric component formed over the source/drain. The gate spacer is formed between the gate and the dielectric component. In some embodiments, the receiving of the device comprises receiving a FinFET as the device. The FinFET device includes a fin structure in which the source/drain is formed, and the gate is formed to wrap around the fin structure.

The method **600** includes a step **620** of forming a recess in a top surface of dielectric component. In some embodiments, the forming of the recess comprises performing a chemical-mechanical polishing (CMP) process to the gate and the dielectric component. A slurry of the CMP process

is configured such that the dielectric component is polished at a faster rate than the gate. In some other embodiments, the forming of the recess comprises removing portions of the dielectric component via an etching process. The etching process may include a wet etching process or a dry etching process.

The method 600 includes a step 630 of forming a dielectric layer over the top surface of the dielectric component and over the recess, such that a portion of the dielectric layer assumes a recessed shape.

The method 600 includes a step 640 of etching a contact hole through the dielectric layer and the dielectric component, the contact hole exposing the source/drain.

The method 600 includes a step 650 of filling the contact hole with a conductive material, thereby forming a source/drain contact.

In some embodiments, the forming of the recess is performed such that a portion of a sidewall of the gate spacer is exposed, and the forming the dielectric layer is performed such that a portion of the dielectric layer is formed directly on the exposed portion of the sidewall of the gate spacer. The portion of the dielectric layer remains on the sidewall of the gate spacer after the contact hole is etched.

In some embodiments, the receiving the device in step 610 comprises receiving a non-Input/Output (non-I/O) device and an Input/Output (I/O) device that each include their respective source/drain, gate, gate spacer, and dielectric component. The dielectric component of the I/O device is formed to have a greater lateral dimension than the dielectric component of the non-I/O device. In some embodiments, the forming of the recess in step 620 is performed such that the I/O device is formed to have a deeper recess than the non-I/O device.

It is understood that additional process steps may be performed before, during, or after the steps 610-650 discussed above to complete the fabrication of the semiconductor device. For example, the semiconductor device may undergo testing and packaging processes before the fabrication is completed. Other process steps are not discussed herein for reasons of simplicity.

Based on the above discussions, it can be seen that the present disclosure offers advantages over conventional semiconductor devices and the fabrication thereof. It is understood, however, that other embodiments may offer additional advantages, and not all advantages are necessarily disclosed herein, and that no particular advantage is required for all embodiments.

One advantage is that the semiconductor device of the present disclosure can reduce potential damage caused by misalignment between the source/drain and the source/drain contact hole. As discussed above, instead of leaving the ILD planarized, the present disclosure uses etching or carefully tuned polishing processes to make the ILD “caved-in” or recessed. The subsequent deposition of a dielectric layer on the recessed ILD effectively enlarges or thickens the spacers. As a result, the etching processes used to form the source/drain contact holes cannot easily pierce through the “thickened” spacers, and this prevents the gate structures from being damaged.

Along similar lines, another advantage is that the “thickened” spacers can relax the overlay requirements or the etching process loading associated with the formation of the source/drain contact hole. This is because even if there is some lateral shift of the source/drain contact hole, the consequences are unlikely to be disastrous, as the “thickened” spacers formed herein can still adequately protect the gate structures.

Furthermore, the present disclosure also offers the advantage of reducing parasitic capacitance. In the context of the present disclosure, parasitic capacitance is an inverse function of a distance between the gate structure and the source/drain contact. The “thickened” spacers herein ensure that the source/drain contact does not get “too close” to the gate structure on either side. In other words, the “thickened” spacers effectively lengthen a minimum distance between the gate structures and the source/drain contact. As this distance increases, the resulting parasitic capacitance is reduced. The reduction of parasitic capacitance improves yield and enhances semiconductor device performance.

One aspect of the present disclosure involves a semiconductor device. The semiconductor device includes a transistor. The transistor includes a source/drain region, a gate structure, a gate spacer disposed on a sidewall of the gate structure, a first dielectric material disposed adjacent to an upper portion of the gate spacer, and a second dielectric material disposed adjacent to a lower portion of the gate spacer. The second dielectric material and the first dielectric material have different material compositions.

Another aspect of the present disclosure involves a semiconductor device. The semiconductor device includes a non-Input/Output (non-I/O) device. The non-I/O device includes a first source/drain, a first gate structure, a first gate spacer disposed on a sidewall of the first gate structure, a first interlayer dielectric (ILD) disposed next to the first gate spacer, a first dielectric layer disposed over the first gate structure and over the first ILD, the first dielectric layer having a first recessed upper surface, and a first contact disposed over the first source/drain. The first contact extends through the first ILD and the first dielectric layer. The semiconductor device also includes an Input/Output (I/O) device. The I/O device includes a second source/drain, a second gate structure, a second gate spacer disposed on a sidewall of the second gate structure, a second interlayer dielectric (ILD) disposed next to the second gate spacer, a second dielectric layer disposed over the second gate structure and over the second ILD, the second dielectric layer having a second recessed upper surface, and a second contact disposed over the second source/drain. The second contact extends through the second ILD and the second dielectric layer. The second recessed upper surface has a greater depth than the first recessed upper surface.

Yet another aspect of the present disclosure involves a method of fabricating a semiconductor device. A device is received that includes a source/drain, a gate, a gate spacer formed on a sidewall of the gate, and a dielectric component formed over the source/drain. The gate spacer is formed between the gate and the dielectric component. A recess is formed in a top surface of the dielectric component. A dielectric layer is formed over the top surface of the dielectric component and over the recess, such that a portion of the dielectric layer assumes a recessed shape. A contact hole is etched through the dielectric layer and the dielectric component. The contact hole exposes the source/drain.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may



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make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A method comprising:

forming a first dielectric layer over a gate stack and gate spacers disposed along sidewalls of the gate stack, wherein the gate stack is disposed over and wraps a channel of a fin structure extending from a substrate, the gate stack includes a gate dielectric and a gate electrode, and the gate stack is disposed between source/drain regions of the fin structure;

recessing the first dielectric layer below a top of the gate spacers to expose an upper sidewall portion of one of the gate spacers, wherein a remaining portion of the first dielectric layer is disposed adjacent to a lower sidewall portion of the one of the gate spacers, wherein the recessing the first dielectric layer to expose the upper sidewall portion of the one of the gate spacers includes performing a planarization process that uses a slurry tuned to polish a first composition of the first dielectric layer at a faster rate than a third composition of the gate spacers and a fourth composition of the gate stack;

depositing a second dielectric layer over the recessed, remaining portion of the first dielectric layer, a top surface of the gate stack, and the gate spacers, wherein the second dielectric layer is disposed adjacent to the upper sidewall portion of the one of the gate spacers and the first composition of the first dielectric layer is different than a second composition of the second dielectric layer;

forming a source/drain contact opening that extends through the second dielectric layer and the first dielectric layer to expose one of the source/drain regions of the fin structure; and

forming a source/drain contact in the source/drain contact opening, wherein the first dielectric layer is disposed between the source/drain contact and the lower sidewall portion of the one of the gate spacers and the second dielectric layer is disposed between the source/drain contact and the upper sidewall portion of the one of the gate spacers.

2. The method of claim 1, further comprising, depositing a third dielectric layer over the second dielectric layer before forming the source/drain contact opening, wherein the third dielectric layer further extends over the top surface of the gate stack, the second composition of the second dielectric layer is different than a fifth composition of the third dielectric layer, and the source/drain contact opening extends through the third dielectric layer.

3. The method of claim 2, wherein the depositing the second dielectric layer includes performing a conformal deposition process, such that the second dielectric layer has a curved top surface over the first dielectric layer and a flat top surface over the top surface of the gate stack, and wherein the second dielectric layer and the third dielectric layer have a curvilinear interface therebetween and a linear interface therebetween.

4. The method of claim 3, wherein a thickness of the second dielectric layer over the first dielectric layer is the same as a thickness of the second dielectric layer over the top surface of the gate stack.

5. The method of claim 1, wherein a sum of a thickness of the recessed first dielectric layer and a thickness of the second dielectric layer over the recessed first dielectric layer is at least a height of the gate stack.

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6. The method of claim 1, wherein the recessing the first dielectric layer provides the first dielectric layer with a curved surface, such that the first dielectric layer and the second dielectric layer have a curvilinear interface therebetween.

7. The method of claim 1, wherein the second composition of the second dielectric layer is the same as the third composition of the gate spacers.

8. The method of claim 1, wherein the second composition of the second dielectric layer is different than the third composition of the gate spacers.

9. A method comprising:

forming a first FinFET having a first gate stack, first gate spacers disposed along first sidewalls of the first gate stack, and a first fin structure, wherein the first gate stack is disposed over and wraps a first channel of the first fin structure and is further disposed between first source/drain regions of the first fin structure;

forming a second FinFET having a second gate stack, second gate spacers disposed along second sidewalls of the second gate stack, and a second fin structure, wherein the second gate stack is disposed over and wraps a second channel of the second fin structure and is further disposed between second source/drain regions of the second fin structure;

forming a first dielectric layer over the first gate stack, the first gate spacers disposed along the first sidewalls of the first gate stack, the second gate stack, and the second gate spacers disposed along the second sidewalls of the second gate stack;

recessing the first dielectric layer to expose a first upper sidewall portion of one of the first gate spacers and a second upper sidewall portion of one of the second gate spacers, wherein a remaining portion of the first dielectric layer is disposed adjacent to a first lower sidewall portion of the one of the first gate spacers and a second lower sidewall portion of the one of the second gate spacers and the remaining portion of the first dielectric layer has a first dished top surface, wherein the recessing includes performing a planarization process that uses a slurry that polishes the first dielectric layer at a first rate, the first gate spacers and the second gate spacers at a second rate, and the first gate stack and the second gate stack at a third rate, wherein the first rate is greater than the second rate and the third rate;

conformally depositing a second dielectric layer over the remaining portion of the first dielectric layer, a first top surface of the first gate stack, the first gate spacers, a second top surface of the second gate stack, and the second gate spacers, such that the second dielectric layer has a dished profile over the remaining portion of the first dielectric layer and a planar profile over the first top surface of the first gate stack and the second top surface of the second gate stack, wherein the second dielectric layer has a second dished top surface over the first dished top surface of the remaining portion of the first dielectric layer, the second dielectric layer is disposed adjacent to the first upper sidewall portion of the one of the first gate spacers, the second dielectric layer is disposed adjacent to the second upper sidewall portion of the one of the second gate spacers, and further wherein a first composition of the first dielectric layer is different than a second composition of the second dielectric layer;

forming a first source/drain contact opening and a second source/drain contact opening that extends through the second dielectric layer and the first dielectric layer to

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expose one of the first source/drain regions of the first fin structure and one of the second source/drain regions of the second fin structure, respectively; and  
forming a first source/drain contact in the first source/drain contact opening and a second source/drain contact in the second source/drain contact opening, wherein:  
the first dielectric layer is disposed between the first source/drain contact and the first lower sidewall portion of the one of the first gate spacers,  
the first dielectric layer is disposed between the second source/drain contact and the second lower sidewall portion of the one of the second gate spacers,  
the first dielectric layer is disposed between the second dielectric layer and each of the first fin structure and the second fin structure,  
the second dielectric layer extends over the first top surface of the first gate stack and the second top surface of the second gate stack,  
the second dielectric layer is disposed between the first source/drain contact and the first upper sidewall portion of the one of the first gate spacers, and  
the second dielectric layer is disposed between the second source/drain contact and the second upper sidewall portion of the one of the second gate spacers.

10. The method of claim 9, wherein:  
the first dielectric layer that is disposed between the first source/drain contact and the first lower sidewall portion of the one of the first gate spacers has a first width;  
the first dielectric layer that is disposed between the second source/drain contact and the second lower sidewall portion of the one of the second gate spacers has a second width; and  
the first width is different than the second width.

11. The method of claim 9, wherein the recessing of the first dielectric layer forms:  
a first recessed top surface of the first dielectric layer that is disposed adjacent to the first lower sidewall portion of the one of the first gate spacers;  
a second recessed top surface of the first dielectric layer that is disposed adjacent to the second lower sidewall portion of the one of the second gate spacers; and  
wherein a first distance between a first top fin surface of the first fin structure and the first recessed top surface is different than a second distance between a second top fin surface of the second fin structure and the second recessed top surface.

12. The method of claim 11, wherein a difference between the first distance and the second distance is at least one nanometer.

13. The method of claim 9, wherein:  
a distance is between a lowest point of the first dished top surface and tops of the first gate stack and the second gate stack; and  
a thickness of the second dielectric layer is greater than the distance.

14. The method of claim 9, wherein the conformally depositing the second dielectric layer includes forming a silicon nitride layer.

15. The method of claim 9, wherein the forming the first dielectric layer includes forming a low-k dielectric layer.

16. A method comprising:  
forming a fin structure over a substrate;  
forming a first gate stack over and wrapping a first channel of the fin structure and a second gate stack over and wrapping a second channel of the fin structure,

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wherein the first gate stack includes a first gate dielectric and a first gate electrode, the second gate stack includes a second gate dielectric and a second gate electrode, and a source/drain region of the fin structure is disposed between the first gate stack and the second gate stack;  
forming first gate spacers along first sidewalls of the first gate stack and second gate spacers along second sidewalls of the second gate stack;  
forming a first low-k silicon oxide layer over the source/drain region of the fin structure, a silicon nitride layer over the first low-k silicon oxide layer, and a second low-k silicon oxide layer over the silicon nitride layer, wherein:  
the silicon nitride layer extends over a first top surface of the first gate stack and a second top surface of the second gate stack, the second low-k silicon oxide layer extends over the first top surface of the first gate stack and the second top surface of the second gate stack, and a portion of the silicon nitride layer between the first gate stack and the second gate stack has a dished top surface and a dished bottom surface, the dished top surface abuts the second low-k silicon oxide layer, the dished bottom surface abuts the first low-k silicon oxide layer, and the portion of the silicon nitride layer abuts a first upper sidewall portion of the first gate spacers and a second upper sidewall portion of the second gate spacers, and  
the forming the first low-k silicon oxide layer includes a deposition process and a chemical mechanical polishing (CMP) process after the deposition process, wherein the CMP process implements a slurry tuned to polish the first low-k silicon oxide layer at a faster rate than the first gate spacers, the second gate spacers, the first gate stack, and the second gate stack; and  
forming a source/drain contact that extends through the second low-k silicon oxide layer, the silicon nitride layer, and the first low-k silicon oxide layer to the source/drain region of the fin structure, wherein the first low-k silicon oxide layer is disposed between the source/drain contact and a first lower sidewall portion of the first gate spacers, the first low-k silicon oxide layer is disposed between the source/drain contact and a second lower sidewall portion of the second gate spacers, the silicon nitride layer is disposed between the source/drain contact and the first upper sidewall portion of the first gate spacers, and the silicon nitride layer is disposed between the source/drain contact and the second upper sidewall portion of the second gate spacers.

17. The method of claim 16, wherein the CMP process includes recessing the first low-k silicon oxide layer below the first top surface of the first gate stack and the second top surface of the second gate stack before forming the silicon nitride layer.

18. The method of claim 17, wherein the recessing the first low-k silicon oxide layer exposes the first upper sidewall portion of the first gate spacers and the second upper sidewall portion of the second gate spacers and the recessing the first low-k silicon oxide layer provides the first low-k silicon oxide layer with a topmost, dished surface.

19. The method of claim 16, wherein a first width of the silicon nitride layer that is disposed between the source/drain contact and the first upper sidewall portion of the first gate spacers is different than a second width of the silicon

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nitride layer that is disposed between the source/drain contact and the second upper sidewall portion of the second gate spacers.

**20.** The method of claim **16**, wherein a first width of the silicon nitride layer that is disposed between the source/ 5  
drain contact and the first upper sidewall portion of the first gate spacers is the same as a second width of the silicon nitride layer that is disposed between the source/drain contact and the second upper sidewall portion of the second gate spacers. 10

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