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Power limiting circuits

Abstract

A power limiting circuit is provided to control operation power of a power device during operation. The power limiting circuit includes a detection circuit and a control circuit. The detection circuit is coupled to the power device. The detection circuit is configured to detect a cross voltage between an input terminal and an output terminal of the power device and generate at least one detection signal associated with the detected cross voltage. The control circuit is coupled to the detection circuit and the power device. The control circuit is configured to generate a control signal based on the at least one detection signal. The control signal is provided to enable or disable the power device to control the operation power of the power device.

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Background/Summary

CROSS REFERENCE TO RELATED APPLICATIONS

(1) This Application claims priority of Taiwan Patent Application No. 111128774, filed on Aug. 1, 2022, the entirety of which is incorporated by reference herein.

BACKGROUND OF THE INVENTION

Field of the Invention

(2) The present invention relates to a current limiting circuit, and more particularly to a current limiting circuit for a power device.

Description of the Related Art

(3) One characteristic of power devices is that they are high-voltage tolerant, and as such are ideal for use in energy conversion circuits of electronic devices, such as circuits for frequency conversion, rectification, voltage transformation, or power amplification. When a cross voltage between an input terminal and an output terminal of a power device (such as a drain-source voltage (Vds) of a power transistor) is large, the load current flowing through the power device results in a larger amount of power. Where high power is maintained for an extended period of time, thermal

energy is generated, which induces a high temperature. Under long-term use, the high power may cause the power device to be damaged.

BRIEF SUMMARY OF THE INVENTION

(4) The present invention provides a power limiting circuit for a power device performing a current and voltage detection, which may reduce a load current flowing through the power device when an input-output voltage of the power device is great, thereby limiting the operation power of the power device.

(5) An exemplary embodiment of the present invention provides a power limiting circuit for controlling an operation power of the power device during operation. The power limiting circuit comprises a detection circuit and a control circuit. The detection circuit is coupled to the power device. The detection circuit is configured to detect a cross voltage between an input terminal and an output terminal of the power device and generate at least one detection signal associated with the detected cross voltage. The control circuit is coupled to the detection circuit and the power device. The control circuit is configured to generate a control signal based on the at least one detection signal. The control signal is provided to enable or disable the power device to control the operation power of the power device.

(6) A detailed description is given in the following embodiments with reference to the accompanying drawings.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) The invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

(2) FIG. **1** shows an electronic device having a power limiting function according to an embodiment of the present invention;

(3) FIG. **2** shows a power limiting circuit according to an embodiment of the present invention;

(4) FIGS. **3**A-**3**B are schematic diagrams showing changes in main signals and voltages of the power limiting circuit of FIG. **2**;

(5) FIG. **4** shows a power limiting circuit according to another embodiment of the present invention;

(6) FIG. **5** shows a power limiting circuit according to another embodiment of the present invention;

(7) FIGS. **6**A-**6**B show schematic diagrams showing changes in main signals and voltages of the power limiting circuit of FIG. **5**;

(8) FIG. **7** shows a power limiting circuit according to another embodiment of the present invention;

(9) FIG. **8** shows a voltage detection circuit according to another embodiment of the present invention; and

(10) FIG. **9** shows a current detection circuit according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

(11) The following description is of the best-contemplated model of carrying out the invention. This description is made for the purpose of illustrating the general principles of the invention and should not be taken in a limiting sense. The scope of the invention is best determined by reference to the appended claims.

(12) FIG. **1** shows an electronic device with a power limiting function according to an embodiment of the present invention. Referring to FIG. **1**, an electronic device **1** comprises a power limiting circuit **10** and a power device **11**. In the embodiment, the power device **11** is a high-voltage-tolerant

device. The power limiting circuit **10** detects the voltage across an input terminal and an output terminal of the power device **11** and further detects the load current flowing through the power device **11**. The power limiting circuit **10** controls the operation power of the power device **11** based on the detection results.
(13) Referring to FIG. **1**, the power limiting circuit **10** comprises a control circuit **100** and a detection circuit **101**. The detection circuit **101** is coupled to the power device **11** to detect a cross voltage between the input terminal and the output terminal of the power device **11** and further detect the load current flowing through the power device **11**. The detection circuit **101** generates at least one detection signal based on the detection results. In the embodiment, the detection signal may be a current signal, which is associated with the cross voltage between the input terminal and the output terminal of the power device **11**. For example, the detection circuit **101** generates two currents based on the detection results as two detection signals. Of the two detection signals, one indicates the detected cross voltage of the power device **11**, and the other indicates the detected load current. Since the load current is the current flowing through the power device **11**, the load current is associated with the above-mentioned cross voltage of the power device **11**. Accordingly, one or more detection signals generated by the detection circuit **101** are all associated with the above-mentioned cross voltage of the power device **11**.
(14) The control circuit **100** generates a control signal S**10** to enable or disable the power device **11**, for example, to turn the power device **11** on or off. The control circuit **100** also receives the detection signals generated by the detection circuit **101** and adjusts the duty cycle of the control signal S**10** based on the detection signals, thereby adjusting the on-time of the power device **11**. By adjusting the on-time of the power device **11**, the load current flowing through the power device **11** is controlled, which accomplishes the control of the operation power of the power device **11** (the operation power is equal to the product of the above-mentioned cross voltage and the load current).
(15) Through the above-mentioned operation, when the above-mentioned cross voltage of the power device **11** is large, the power limiting circuit **1** can shorten the on-time of the power device **11** to reduce the load current, so that the operation power of the power device **11** is controlled to remain at a predetermined fixed value. Therefore, the power limiting current **1** of the present application can control the operation power of the power device **11** to remain at a predetermined fixed value, thereby preventing the power device **11** from being damaged due to a large cross voltage.
(16) Various embodiments of the power limiting circuit **10** of the present invention will be described below.
(17) FIG. **2** shows a power limiting circuit according to an embodiment of the present invention. The power limiting circuit **10** of FIG. **1** can be implemented by the power limiting circuit **10**A of FIG. **2**. Referring to FIG. **2**, in order to clearly illustrate the operation of the power limiting circuit, FIG. **2** not only shows the power limiting circuit **10**A, but also shows the power device **11** coupled to the power limiting circuit **10**A. The power limiting circuit comprises a control circuit **100**A and a detection circuit **101**A. The control circuit **100** and the detection circuit **101** in FIG. **1** can be implemented by the control circuit **100**A and the detection circuit **101**A in FIG. **2** respectively.
(18) As shown in FIG. **2**, the power device **11** may be implemented by an N-type metal-oxide-semiconductor (NMOS) transistor **110**. The detection circuit **101**A comprises a current detection circuit **20**A and a voltage detection circuit **21**A. The current detection circuit comprises an NMOS transistor **22**. The voltage detection circuit **21**A comprises P-type metal-oxide-semiconductor (PMOS) transistors **23**-**25**, NMOS transistors **26** and **27**, and a resistor R**20**. In the embodiment, each MOS transistor comprises three electrode terminals, including an input terminal, an output terminal, and a control terminal. For an NMOS transistor, the input terminal, the output terminal, and the control terminal are the drain, the source, and the gate, respectively; for a PMOS transistor, the input terminal, the output terminal, and the control terminal are the source, the drain, and the gate respectively. In the embodiment, the drain of the NMOS transistor **110** serves as the input

terminal of the power device **11**, and the source of the NMOS transistor **110** serves as the output terminal of the power device **11**.

(19) Referring to FIG. **2**, the gate of the NMOS transistor **110** receives the control signal S**10** generated by the control circuit **100**A. The gate of the NMOS transistor **22** of the current detection circuit **20**A receives the control signal S**10**, the drain thereof is coupled to the drain of the NMOS transistor **110**, and the source thereof is coupled to a comparison circuit CMP**21**. The size of NMOS transistor **22** is K times that of NMOS transistor **110**. In detail, the width-to-length ratio of the gate of the NMOS transistor **22** is K times (K W/L) the width-to-length ratio (W/L) of the gate of the NMOS transistor **110**.

(20) The first terminal of the resistor R**20** is coupled to the drain of the NMOS transistor **110**. The source of the PMOS transistor **23** is coupled to the second terminal of the resistor R**20**, and the gate of the PMOS transistor **23** is coupled to a node N**23**. The drain and gate of the NMOS transistor **26** are coupled to the drain of the PMOS transistor **23**, and the source thereof is coupled to a reference terminal, such as a ground terminal (represented by an inverted triangle in the figures). The source of the PMOS transistor **24** is coupled to the source of the NMOS transistor **110**, and the gate and drain thereof are coupled to the node N**23**. The drain of the NMOS transistor **27** is coupled to the gate and the drain of the PMOS transistor **24** (that is, the drain of the NMOS transistor **27** is also coupled to the node N**23**), and the gate thereof is coupled to the gate and the drain of the NMOS transistor **26**, and the source thereof is coupled to the ground terminal. The source of the PMOS transistor **25** is coupled to the source of the NMOS transistor **110**, the gate thereof is coupled to the node N**23**, and the drain thereof is coupled to a comparison circuit CMP**20** at a node N**20**.

(21) The comparison circuits CMP**20** and CMP**21** is included in the control circuit **100**A. The comparison circuit CMP**20** comprises a comparator OP**20**, a capacitor C**20**, a switch SW**20**, a resistor R**21**, and a current source CS**20**. The comparator OP**20** has an inverting input terminal (−), a non-inverting input terminal (+), and an output terminal. The inverting input terminal (−) of the comparator OP**20** is coupled to a node N**21**, and the non-inverting input terminal (+) thereof is coupled to the node N**20**. The comparison circuit CMP**20** is coupled to the voltage detection circuit **21**A at the node N**20**. The current source CS**20** is coupled to the node N**21** and provides a current I**22** to the node N**21**. The capacitor C**20** is coupled between the node N**21** and the ground terminal. The switch SW**20** is coupled between the node N**21** and the ground terminal. The resistor R**21** is coupled between the node N**20** and the ground terminal. The output terminal of the comparator OP**20** generates a comparison signal S**20**.

(22) The comparison circuit CMP**21** comprises a comparator OP**21**, switches SW**21** and SW**22**, and a capacitor C**22**. The comparator OP**21** has an inverting input terminal (−), a non-inverting input terminal (+), and an output terminal. The inverting input terminal (−) of the comparator OP**21** is coupled to a node N**22**, and the non-inverting input terminal (+) thereof receives a reference voltage V**22**. The input terminal of the switch SW**21** is coupled to the current detection circuit **20**A, and the output terminal thereof is coupled to the node N**22**. The switch SW**21** receives the comparison signal S**20** from the comparison circuit CMP**20** to determine its on/off state. The switch SW**22** is coupled between the node N**22** and the ground terminal. The capacitor C**21** is coupled between the node N**22** and the ground terminal. The control signal S**10** is generated at the output terminal of the comparator OP**21**.

(23) The detailed operation of the power limiting circuit **10**A of FIG. **2** will be described in detail below.

(24) Referring to FIG. **2** and FIG. **3**A, when the electronic device operates, the NMOS transistor **110** and the NMOS transistor **22** are turned on based on the high level of the control signal S**10**. At this time, based on the high level of the control signal S**10**, there is a cross voltage Vds (drain-source voltage) between the drain and the source of the NMOS transistor **110**, and a load current Iload flows through the NMOS transistor **110**. The voltage detection circuit **21**A generates a current I**20** (I**20**=Vds/r**20**) based on the resistance value r**20** of the resistor R**20** and the cross voltage Vds.

Through the operation of the current mirror circuit composed of the transistors **23-25** in the voltage detection circuit **21**A, a mirrored current Idet flowing through the PMOS transistor **25** is obtained. In the embodiment, the current Idet is equal to the current I**20**. The current Idet is a detection signal generated by the voltage detection circuit **21**A, which is provided to the node N**20** of the comparison circuit CMP**20** as an input signal of the control circuit **100**A. Accordingly, the voltage detection circuit **21**A can be regarded as a current source for generating the current Idet. In order to clearly show the relationship between the voltage detection circuit **21**A and the comparison circuit CMP**20**, in FIG. **2**, the voltage detection circuit **21**A is represented by the symbol of a current source that is coupled to the node N**20** and provides the current (detection signal) Idet.

(25) In addition, when the electronic device operates, the time when the control signal S**10** is at the high level is t**22**. The NMOS transistor **22** of the current detection circuit **20**A is turned on based on the high level of the control signal S**10**. Since the size of the NMOS transistor **22** is K times that of the NMOS transistor **110**, the generated current I**21** flowing through the NMOS transistor **22** is equal to K times the load current Iload, that is, I**21**=KIload. The current I**21** serves as a detection signal generated by the current detection circuit **20**A, which is provided to the comparison circuit CMP**21** as another input signal of the control circuit **100**A. In order to clearly show the relationship between the current detection circuit **20**A and the comparison circuit CMP**21**, in FIG. **2**, the current detection circuit **20**A is represented by the symbol of a current source that is coupled to the switch SW**21** and provides the current (detection signal) I**21**.

(26) When the electronic device operates, the switches SW**20** and SW**22** are turned on simultaneously to reset the voltages on the nodes N**21** and N**22** respectively, and then the switches SW**20** and SW**22** are turned off for a period of time T. As shown in FIG. **3**A, current I**22** charges capacitor C**20**, and a ramp voltage V**21** is thus generated at the node N**21**. An input voltage V**20** is generated at the node N**20** based on the resistance value r**21** of the resistor R**21** and the current Idet provided to the node N**20**. The comparator OP**20** compares the input voltage V**20** with the ramp voltage V**21** to generate a comparison signal S**20** based on the comparison result. Referring to FIG. **3**A, when the input voltage V**20** is greater than the ramp voltage V**21**, the comparison signal S**20** is at a high level. Once the input voltage V**20** becomes less than the ramp voltage V**21**, the comparison signal S**20** is switched to a low level.

(27) Referring to FIG. **2** and FIG. **3**A, the comparison signal S**20** is at the high level during time t**21**, and the switch SW**21** is turned on based on the high level of the comparison signal S**20**. Since switch SW**21** is turned on, the current I**21** charges the capacitor C**21**, and an input voltage V**23** is thus generated at the node N**22**. The current I**21** continues to charge the capacitor C**21** until the comparison signal S**20** switches to the low level. As shown in FIG. **3**B, the input voltage V**23** gradually increases. The comparator OP**21** compares the input voltage V**23** with the reference voltage V**22** to generate the control signal S**10** based on the comparison result. When the reference voltage V**22** is greater than the input voltage V**23**, the control signal S**10** is at a high level. Once the reference voltage V**22** becomes less than the input voltage V**23**, the control signal S**10** is switched to a low level. Referring to FIG. **3**B, when the control signal S**10** is at the high level during time t**22**, the NMOS transistor **110** and the NMOS transistor **22** are turned on based on the high level of the control signal S**10**; when the control signal S**10** is switched to the low level, the NMOS transistor **110** and the NMOS transistor **22** are turned off.

(28) During the operation of the electronic device, when the cross voltage Vds of the NMOS transistor **110** increases, both the current I**20** and the load current Iload that are generated based on the cross voltage Vds increase. Therefore, the operation power P (P=Ioad×Vds) of the NMOS transistor **110** increases. An increase in the current I**20** results in an increase in the obtained current Idet. Therefore, the input voltage V**20** at the node N**20** increases with the cross voltage Vds, that is, the input voltage V**20** is proportional to the cross voltage Vds (V**20**∝cVds). Referring to FIG. **3**A, the level of the input voltage V**20** is raised upward, as indicated by the arrow. As the input voltage V**20** increases, the time t**21** when the input voltage V**20** is greater than the ramp voltage V**21** is

extended to time t**21**′, so that the period during which the comparison signal S**20** is at the high level is extended, that is, the duty cycle of the comparison signal S**20** increases.
(29) Based on the extended period of the high level of the comparison signal S**20** and the increase of the load current Iload, the input voltage V**23** at the node N**22** increase more rapidly, that is, the rising slope of the input voltage V**23** is proportional to the load current Iload (V**23**∝Iload). Referring to FIG. **3**B, the rising slope of the input voltage V**23** increases as indicated by the arrow. As the rising slope of the input voltage V**23** increases, the time t**22** when the reference voltage V**22** is greater than the input voltage V**23** is shortened to time t**22**′, so that the period during which the control signal S**10** is at the high level is shortened, that is, the duty cycle of the control signal S**10** decreases.
(30) Based on the decrease of the duty cycle of the control signal S**10**, the on-time of the NMOS transistor (power device) **110** is shortened, so that the load current Iload is reduced. As such, the operation power of the NMOS transistor **110** can decreases accordingly. According to the embodiment, when the operation power of the NMOS transistor **110** increases, the operation power decreases by shortening the on-time of the NMOS transistor **110** to avoid damage to the NMOS transistor **110** caused by high power.
(31) After the duty cycle of the control signal S**10** is adjusted once, the switches SW**20** and SW**22** are turned on to discharge the capacitors C**20** and C**21** to reset the voltage V**21** at the node N**21** and the voltage V**23** at the node N**22**, respectively.
(32) In the embodiment of the present invention, the power limiting circuit **10**A can limit the operation power of the NMOS transistor **110** to a predetermined value. For example, when the power limiting circuit **10**A detects that the operation power of the NMOS transistor **110** increases, the operation power can decrease to a predetermined value by shortening the on-time of the NMOS transistor **110**. The predetermined value can be determined by the resistance value r**20** of the resistor R**20**, the capacitance value c**20** of the capacitor C**20**, the current I**22**, the resistance value r**21** of the resistor R**21**, the capacitance value c**21** of the capacitor C**21**, the reference voltage V**22**, and the multiple K of the size of the NMOS transistor **22** relative to the size of the NMOS transistor **110**. The detailed analysis is described below.
(33) When the electronic device operates, the NMOS transistor **110** has a cross voltage Vds. The current I**20** can be expressed as:
$I20=Vds/r20$ Equation (1)
(34) Since the current Idt is equal to the current I**20**, Equation (1) can be rewritten as:
$Idet=Vds/r20$ Equation (2)
(35) Based on Equation (2), the input voltage V**20** can be obtained:
$V20=r21\times Vds/r20$ Equation (3)
(36) The current I**22** charges the capacitor C**20** during the time t**21**. The charge quantity Q**20** corresponding to the period t**21** can be expressed as:
$Q20=I22\times t21=c20\times V21$ Equation (4)
(37) When the ramp voltage V**21** is equal to the input voltage V**20** (V**21**=V**20**), the time t**21** can be obtained:
$t21=c20\times r21\times(Vds/r20)/I22$ Equation (5)
(38) Referring to Equation (3) and Equation (5), r**21**×(Vds/r**20**) in Equation (5) is equal to the input voltage V**20**. Therefore, when the cross voltage Vds increases, the input voltage V**20** increases accordingly, so that the time t**21** also increases, which extends the time when the comparison signal S**20** is at the high level. As a result, the time when the capacitor C**21** is changed by the current I**21** is also extended. The amount of charge Q**21** used to charge the capacitor C**21** can be expressed as:
$Q21=I21\times t21=c21\times V23$ Equation (6)
(39) Wherein, I**21**=KIload, and Equation (6) is rewritten as:
$Q21=KIload\times t21=c21\times V23$ Equation (7)
(40) When the input voltage V**23** is equal to the reference voltage V**22** (V**23**=V**22**), Equation (5) is

taken into Equation (7) to obtain Equation (8):

$KIload \times c20 \times r21 \times (Vds/r20)/I22 = c21 \times V22$ Equation (8)

(41) Equation (8) is rewritten as follows:

$Iload \times Vds = (c21 \times V22 \times I22 \times r20)/(K \times c20 \times r21)$ Equation (9)

(42) Equation (9) represents the operation power P of the NMOS transistor **110** (P=load×Vds). Since the parameters c**21**, V**22**, I**22**, r**20**, K, c**20**, and r**21** in Equation (9) are all constant values, the predetermined value of the operation power can be determined by adjusting at least one of these parameters.

(43) FIG. **4** shows a power limiting circuit according to another embodiment of the present invention. The power limiting circuit **10** of FIG. **1** can be implemented by the power limiting circuit **10**B of FIG. **4**. The circuit structure of the power limiting circuit **10**B is substantially the same as that of the power limiting circuit **10**A in FIG. **2**. The only difference between the power limiting circuits **10**B and **10**A is that the current I**21** (a detection signal) generated by the current detection circuit **20**A is provided to the node N**20** of the comparator circuit CMP**20** as an input signal of the control circuit **100**A and the current Idet (another detection signal) generated by the voltage detection circuit **21**A is provided to the comparison circuit CMP**21** as another input signal of the control circuit **100**A. The circuit structure and operation of the power limiting circuit **10**B are as described in the embodiment of FIG. **2** and thus omitted here.

(44) FIG. **5** shows a power limiting circuit according to another embodiment of the present invention. The power limiting circuit **10** of FIG. **1** can be implemented by the power limiting circuit **10**C of FIG. **5**. Referring to FIG. **5**, in order to clearly illustrate the operation of the power limiting circuit, FIG. **5** not only shows the power limiting circuit **10**C, but also shows the power device **11** and the transistor **110** coupled to the power limiting circuit **10**C. The power limiting circuit **10**C comprises a control circuit **100**B and a detection circuit **101**A. The control circuit **100** and the detection circuit **101** in FIG. **1** can be implemented by the control circuit **100**B and the detection circuit **101**A in FIG. **5**, respectively. The control circuit **100**B comprises comparison circuits CMP**50** and CMP**51**.

(45) The circuit structure and operation of the power device **11** and the detection circuit **101**A are the same as those in FIG. **2**. For related descriptions, please refer to the relevant paragraphs in FIG. **2**, and the description is omitted here.

(46) Referring to FIG. **5**, the source of the NMOS transistor **22** is coupled to the comparison circuit CMP**50** at a node N**50**, and the current I**21** is provided to the node N**50** of the comparison circuit CMP**50** as an input signal of the control circuit **100**B. The source of the PMOS transistor **25** is coupled to the comparison circuit CMP**51**, and the current Idet is provided to the comparison circuit CMP**51** as another input signal of the control circuit **100**B.

(47) The comparison circuit CMP**50** comprises a comparator OP**50** and a capacitor C**50**. The comparator OP**50** has an inverting input terminal (−), a non-inverting input terminal (+), and an output terminal. The inverting input terminal (−) of the comparator OP**50** is coupled to the node N**50**, and the non-inverting input terminal (+) thereof receives a reference voltage V**51**. The comparison circuit CMP**50** is coupled to the current detection circuit **20**A at the node N**50**. The capacitor C**50** is coupled between the node N**50** and the ground terminal (represented by an inverted triangle in the figures). The output terminal of the comparator OP**50** generates a comparison signal S**50**.

(48) The comparison circuit CMP**51** comprises a comparator OP**51**, switches SW**50**-SW**53**, capacitors C**51** and C**52**, and a current source CS**50**. The comparator OP**51** has an inverting input terminal (−), a non-inverting input terminal (+), and an output terminal. The non-inverting input terminal (+) of the comparator OP**51** is coupled to a node N**51**, and the inverting input terminal (−) thereof is coupled to a node N**52**. The current source CS**50** provides a current I**50**. The input terminal of the switch SW**50** is coupled to the current source CS**50**, and the output terminal thereof is coupled to the node N**51**. The switch SW**50** receives the comparison signal S**50** from the

comparison circuit CMP**50** to determine its on/off state. The switch SW**51** is coupled between the node N**51** and the ground terminal. The capacitor C**51** is coupled between the node N**51** and the ground terminal. The input terminal of the switch SW**52** is coupled to the voltage detection circuit **21**A, and the output terminal thereof is coupled to the node N**52**. The switch SW**52** receives a switching signal S**51** to determine its on/off state. The switch SW**53** is coupled between the node N**52** and the ground terminal. The capacitor C**52** is coupled between the node N**52** and the ground terminal. The control signal S**10** is generated at the output terminal of the comparator OP**21**.

(49) The detailed operation of the power limiting circuit **10**C of FIG. **5** will be described in detail below.

(50) When the electronic device operates, the operations of the NMOS transistor **110**, the current detection circuit **20**A, and the voltage detection circuit **21**A are as described in the embodiment of FIG. **2**, and the detailed description will be omitted below. Referring to FIG. **5** and FIG. **6**A, when the electronic device operates, the current detection circuit **20**A generates the current I**21**. The current I**21** is a detection signal generated by the current detection circuit **20**A, which is provided to the node N**50** of the comparison circuit CMP**50** as one input signal of the control circuit **100**B. In addition, when the electronic device operates, the voltage detection circuit **21**A generates the current Idet. The current Idet is a detection signal generated by the voltage detection circuit **21**A, which is provided to the comparison circuit CMP**51** as another input signal of the control circuit **100**B.

(51) As shown in FIG. **6**A, when the electronic device operates, the current I**21** charges the capacitor C**50**, and an input voltage V**50** is thus generated at the node N**50**. As shown in FIG. **6**A, the input voltage V**50** gradually increases. The comparator OP**50** compares the input voltage V**50** with the reference voltage V**51** to generate a comparison signal S**50** based on the comparison result. When the reference voltage V**51** is greater than the input voltage V**50**, the control signal S**50** is at a high level. Once the reference voltage V**51** becomes less than the input voltage V**50**, the control signal S**50** is switched to a low level.

(52) Referring to FIGS. **5** and **6**A, when the electronic device operates, the switches SW**51** and SW**53** are simultaneously turned on to reset the voltages at the nodes N**51** and N**52**, respectively, and then the switches SW**51** and SW**53** are turned off for a period of time T. The comparison signal S**50** is at the high level during time t**51**, and the switch SW**50** is turned on based on the high level of the comparison signal S**50**. Since the switch SW**50** is turned on, the current I**50** charges capacitor C**51**, and a reference voltage V**52** is thus generated at the node N**51**. As shown in FIG. **6**A, the reference voltage V**52** gradually increases. When the switch SW**50** is turned off based on the low level of the comparison signal S**50** after the time t**51**, the reference voltage V**52** stops increasing and remains at the last reached level (referred to as a “holding level”). When the reference voltage V**52** reaches the above-mentioned holding level, the switch SW**52** is turned on. Since the switch SW**52** is turned on, the current Idet charges capacitor C**52**, and an input voltage V**53** is thus generated at the node N**52**. As shown in FIG. **6**B, the input voltage V**53** gradually increases. In the embodiment, the time when the switch SW**52** is turned on is later than the time when the switch SW**50** is turned on, so that the reference voltage V**52** starts to increase earlier than the voltage V**53**. In another embodiment, the switch SW**52** may be turned on at the same time as the switch SW**50**. The comparator OP**51** compares the input voltage V**53** with the reference voltage V**52** to generate the control signal S**10** based on the comparison result. When the reference voltage V**52** is greater than the input voltage V**53** (that is, the holding level of the reference voltage V**52** is higher than the level of the input voltage V**53**), the control signal S**10** is at the high level. Once the reference voltage V**52** becomes less than the input voltage V**53** (that is, the holding level of the reference voltage V**52** is lower than the level of the input voltage V**53**), the control signal S**10** is switched to the low level. Referring to FIG. **6**B, when the control signal S**10** is at the high level at the time t**52**, the NMOS transistor **110** and the NMOS transistor **22** are turned on based on the high level of the control signal S**10**; when the control signal S**10** is switched to the low level, the NMOS

transistor **110** and the NMOS transistor **22** are turned off.

(53) During the operation of the electronic device, when the cross voltage Vds of the NMOS transistor **110** increases, both the current I**20** and the load current Iload that are generated based on the cross voltage Vds increase. Therefore, the operation power P (P=Iload×Vds) of the NMOS transistor **110** increases. Based on the increase of the load current Iload, the input voltage V**50** at the node N**50** increases more rapidly, that is, the rising slope of the input voltage V**50** is proportional to the load current Iload (V**50**∝Iload). Referring to FIG. **6**A, the rising slope of the input voltage V**50** increases as indicated by the arrow. As the rising slope of the input voltage V**50** increases, the time t**51** when the reference voltage V**51** is greater than the input voltage V**50** is shortened to time t**51**′, so that the period during which the comparison signal S**50** is at the high level is shortened, that is, the duty cycle of the comparison signal S**50** decreases.

(54) As shown in FIGS. **6**A and **6**B, based on the shortened period during which the comparison signal S**50** is at the high level, the capacitor C**51** is charged in a shorter time, so that the holding level of the reference voltage V**52** is lowered, as indicated by the arrow. In addition, since the current Idet increases due to the increase of the cross voltage Vds, the input voltage V**53** at the node N**52** increases more rapidly, that is, the rising slope of the input voltage V**53** is proportional to the cross voltage Vds (V**53**∝Vds). Referring to FIG. **6**B, the level of the input voltage V**53** is raised upward, as indicated by the arrow. Since the holding level of the reference voltage V**52** decreases and the rising slope of the input voltage V**53** increases, the time t**52** when the reference voltage V**52** is greater than the input voltage V**53** is shortened to time t**52**′, so that the period during which the control signal S**10** is at the high level is shortened, that is, the duty cycle of the control signal S**10** decreases.

(55) Based on the decrease of the duty cycle of the control signal S**10**, the on time of the NMOS transistor (power device) **110** is shortened, so that the load current Iload is reduced. Accordingly, the operation power of the NMOS transistor **110** can decreases. According to the embodiment, when the operation power of the NMOS transistor **110** increases, the operation power decreases by shortening the on-time of the NMOS transistor **110** to avoid damage to the NMOS transistor **110** caused by high power.

(56) After the duty cycle of the control signal S**10** is adjusted once, the switches SW**51** and SW**53** are turned on to discharge the capacitors C**51** and C**52** to reset the voltage V**52** at the node N**51** and the voltage V**53** at the node N**52**, respectively.

(57) In the embodiment of the present invention, the power limiting circuit **10**C can limit the operation power of the NMOS transistor **110** to a predetermined value. For example, when the power limiting circuit **10**C detects that the operation power of the NMOS transistor **110** increases, the operation power can decrease to a predetermined value by shortening the on-time of the NMOS transistor **110**. The predetermined value can be determined by the resistance value r**20** of the resistor R**20**, the capacitance value c**50** of the capacitor C**50**, the current I**50**, the reference voltage V**51**, the capacitance value c**51** of the capacitor C**51**, the capacitance value c**52** of the capacitor C**52**, the time T, and the multiple K of the size of the NMOS transistor **22** relative to the size of the NMOS transistor **110**. The detailed analysis is described below.

(58) When the electronic device operates, the current I**21** charges the capacitor C**50** at the time t**51**. The charge quantity Q**50** corresponding to the period t**51** can be expressed as:

$Q50=I21\times t51=KIload\times t51=c50\times V50$ Equation (10)

(59) When the input voltage V**50** is equal to the reference voltage V**51** (V**50**=V**51**), the time t**51** can be obtained:

$t51=c50\times V51/KIload$ Equation (11)

(60) According to Equation (11), when the cross voltage Vds increases, the current I**21** (=KIload) increases accordingly, so that the time t**51** decreases, which shortens the time when the comparison signal S**50** is at the high level. As a result, the time when the capacitor C**51** is charged by the current I**50** is also shortened. The amount of charge Q**51** used to charge the capacitor C**51** can be

expressed as:

$Q51=I50\times t51=c51\times V52$ Equation (12)

(61) The reference voltage V**52** can be obtained according to Equation (12):

$V52=I50\times t51/c51$ Equation (13)

(62) Equation (11) is taken into Equation (13) to obtain:

$V52=(I50/c51)\times c50\times V51/KI\text{load}$ Equation (14)

(63) The current Idet charges the capacitor C**52** at the time T. The amount of charge Q**52** used to charge the capacitor C**52** can be expressed as:

$Q52=c52\times V53=T\times I\text{det}=T\times(V\text{ds}/r20)$ Equation (15)

(64) Based on Equation (15), the input voltage V**53** can be obtained:

$V53=T\times(V\text{ds}/r20)/c52$ Equation (16)

(65) When the reference voltage V**52** is equal to the input voltage V**53**, Equation (17) can be obtained:

$(I50/c51)\times c50\times V51/KI\text{load}=T\times(V\text{ds}/r20)/c52$ Equation (17)

(66) Equation (17) is rewritten as:

$I\text{load}\times V\text{ds}=(I50\times c50\times V51)\times(r20\times c52)/(c51\times T\times K)$ Equation (18)

(67) Equation (18) represents the operation power P of the NMOS transistor **110** (P=load×Vds). Since the parameters I**50**, c**50**, V**51**, r**20**, c**52**, c**51**, T, and K in Equation (19) are all constant values, the predetermined value of the operation power can be determined by adjusting at least one of these parameters.

(68) FIG. **7** shows a power limiting circuit according to another embodiment of the present invention. The power limiting circuit **10** of FIG. **1** can be implemented by the power limiting circuit **10**D of FIG. **7**. The circuit structure of the power limiting circuit **10**D is substantially the same as that of the power limiting circuit **10**C in FIG. **5**. The only difference between the power limiting circuits **10**D and **10**C is that the current I**21** (a detection signal) generated by the current detection circuit **20**A is provided to the comparison circuit CMP**51** as an input signal of the control circuit **100**B and the current Idet (another detection signal) generated by the voltage detection circuit **21**A is provided to the node N**50** of the comparison circuit CMP**50** as another input signal of the control circuit **100**B. The circuit structure and operation of the power limiting circuit **10**D are as described in the embodiment of FIG. **5**, and thus omitted here.

(69) FIG. **8** shows a voltage detection circuit according to another embodiment of the present invention. Referring to FIG. **8**, a voltage detection circuit **21**B can replace the voltage detection circuit **21**A in any one of FIGS. **2**, **4**, **5**, and **7**. Referring to FIG. **8**, the voltage detection circuit **21**B also comprises a resistor R**20** and further comprises an operational amplifier **80** and NMOS transistors **81** and **82**. The operational amplifier **80** has an inverting input terminal (−), a non-inverting input terminal (+), and an output terminal. The first terminal of the resistor R**20** is coupled to the drain of the NMOS transistor **110**, and the second terminal thereof is coupled to the inverting input terminal (−) of the operational amplifier **80**. The non-inverting input terminal (+) of the operational amplifier **80** is coupled to the source of the NMOS transistor **110**. The drain of the NMOS transistor **81** is coupled to the second terminal of the resistor R**20** and the inverting input terminal (−) of the operational amplifier **80**, the source thereof is coupled to the ground terminal, and the gate thereof is coupled to the output terminal of the operational amplifier **80**. The gate of the NMOS transistor **82** is also coupled to the output terminal of the operational amplifier **80**. When the electronic device operates, the voltage detection circuit **21**B generates the current I**20** (I**20**=Vds/r**20**) based on the resistance value r**20** of the resistor R**20** and the cross voltage Vds of the NMOS transistor **110**. Through the operations of the operational amplifier **80** and the NMOS transistors **81** and **82** in the voltage detection circuit **21**B, the mirrored current Idet of the current I**20** is obtained.

(70) FIG. **9** shows a current detection circuit according to another embodiment of the present invention. Referring to FIG. **9**, a current detection circuit **20**B can replace the current detection

circuit **20**A in any one of FIGS. **2**, **4**, **5**, and **7**. Referring to FIG. **9**, the voltage detection circuit **21**B comprises resistors R**90** and R**91**, an operational amplifier **90**, and NMOS transistors **91** and **92**. The operational amplifier **90** has an inverting input terminal (−), a non-inverting input terminal (+), and an output terminal. The first terminal of the resistor R**90** is coupled to the drain of the NMOS transistor **110** and the non-inverting input terminal (+) of the operational amplifier **90**. The first terminal of the resistor R**91** is coupled to the second terminal of the resistor R**90**, and the second terminal thereof is coupled to the inverting input terminal (−) of the operational amplifier **90**. The drain of the NMOS transistor **91** is coupled to the second terminal of the resistor R**91** and the inverting input terminal (−) of the operational amplifier **90**, the source thereof is coupled to the ground terminal, and the gate thereof is coupled to the output terminal of the operational amplifier **90**. The drain of the NMOS transistor **92** is coupled to the second terminal of the resistor R**91** and the inverting input terminal (−) of the operational amplifier **90**, the source thereof is coupled to the ground terminal, and the gate thereof is coupled to the output terminal of the operational amplifier **90**. In the embodiment, the resistance value of the resistor R**91** is 1/K times the resistance value of the resistor R**90**. When the electronic device operates, the load current Iload flows through the resistor R**90** and the NMOS transistor **110**, and a current that is K times the load current Iload flows through the resistor R**91**. Through the operations of the operational amplifier **90** and the NMOS transistors **91** and **92**, the current I**21** that is equal to a predetermined multiple of the load current Iload is obtained.

(71) According to the above various embodiments of the present invention, when the cross voltage between the input terminal and the output terminal of the power device increases, the operation power of the power limiting circuit can decrease to a predetermined value by shortening the time when the power device is enabled or turned on. The power limiting circuit of the present application does not affect the operation of the overcurrent protection circuit coupled to the power device. When the cross voltage between the input terminal and the output terminal of the power device is low or the operation power of the power device does not exceed the above-mentioned predetermined value, the overcurrent protection circuit can be used to achieve the overcurrent protection.

(72) While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

Claims

1. A current limiting circuit for controlling an operation power of a power device during operation, comprising: a detection circuit, coupled to the power device, configured to detect a cross voltage between an input terminal and an output terminal of the power device and generate at least one detection signal associated with the detected cross voltage; and a control circuit, coupled to the detection circuit and the power device, and configured to generate a control signal based on the at least one detection signal, wherein the control circuit adjusts a duty cycle of the control signal based on the at least one detection signal to control the operation power of the power device; wherein the at least one detection signal comprises a first detection signal representing the cross voltage and a second detection signal representing a load current flowing through the power device, and the operation power is determined based on the cross voltage and the load current; wherein the control circuit receives one of the first detection signal and the second detection signal as a first input signal and receives the other of the first detection signal and the second detection signal as a second input signal; and wherein the control circuit comprises: a first comparison circuit

configured to receive the first input signal to generate a first input voltage and compare the first input voltage with a ramp voltage to generate a comparison signal; and a second comparison circuit configured to receive the comparison signal and the second input signal, wherein the second comparison circuit is controlled by the comparison signal to generate a second input voltage based on the second input signal and configured to compare the second input voltage with a reference voltage to generate the control signal, wherein in response to increasing of the operation power, the first comparison circuit increases a duty cycle of the comparison signal, and the second comparison circuit decreases a duty cycle of the control signal, so that the operation power of the power device decreases.

2. The current limiting circuit as claimed in claim 1, wherein the power device is a power metal-oxide-semiconductor (MOS) transistor, a gate of the power metal-oxide-semiconductor transistor receives the control signal, one first drain/source of the power metal-oxide-semiconductor transistor is the input terminal of the power device, and another first drain/source of the power metal-oxide-semiconductor transistor is the output terminal of the power device.

3. The current limiting circuit as claimed in claim 1, wherein the detection circuit comprises: a voltage detection circuit, coupled between the input terminal and the output terminal of the power device, and configured to detect the cross voltage and generate the first detection signal based on the detected cross voltage; and a current detection circuit, coupled to the input terminal of the power device, configured to detect the load current flowing through the power device and generate the second detection signal based on the detected load current, wherein the load current is generated based on the cross voltage.

4. The current limiting circuit as claimed in claim 1, wherein the first comparison circuit comprises: a comparator having an inverting input terminal coupled to a first node, a non-inverting input terminal coupled to a second node, and an output terminal; a capacitor coupled between the first node and a ground terminal; a switch, coupled between the first node and the ground terminal; a resistor coupled between the second node and the ground terminal; and a current source coupled to the first node and configured to provide a first current to the first node, wherein the first input signal is provided to the second node, and the first input voltage is generated at the second node, and wherein the ramp voltage is generated at the first node, and the comparison signal is generated at the output terminal of the comparator.

5. The current limiting circuit as claimed in claim 1, wherein the second comparison circuit comprises: a comparator having an inverting input terminal coupled to a first node, a non-inverting input terminal, and an output terminal; a first switch, controlled by the comparison signal, and having an input terminal for receiving the second input signal and an output terminal coupled to the first node; a capacitor coupled between the first node and a ground terminal; and a second switch, coupled between the first node and the ground terminal, wherein the second input voltage is generated at the first node, and the reference voltage is provided to the non-inverting input terminal of the comparator, and wherein the control signal is generated at the output terminal of the comparator.

6. A current limiting circuit for controlling an operation power of a power device during operation, comprising: a detection circuit, coupled to the power device, configured to detect a cross voltage between an input terminal and an output terminal of the power device and generate at least one detection signal associated with the detected cross voltage; and a control circuit, coupled to the detection circuit and the power device, and configured to generate a control signal based on the at least one detection signal, wherein the control signal is provided to enable or disable the power device to control the operation power of the power device; wherein the at least one detection signal comprises a first detection signal representing the cross voltage and a second detection signal representing a load current flowing through the power device, and the operation power is determined based on the cross voltage and the load current, wherein the control circuit receives one of the first detection signal and the second detection signal as a first input signal and receives the

other of the first detection signal and the second detection signal as a second input signal, and wherein the control circuit comprises: a first comparison circuit configured to receive the first input signal to generate a first input voltage, and compare the first input voltage with a first reference voltage to generate a comparison signal; and a second comparison circuit configured to receive the comparison signal and the second input signal, wherein the second comparison circuit is controlled by the comparison signal to provide a second reference voltage, and the second comparison circuit is configured to generate a second input voltage based on the second input signal and compare the second input voltage with the second reference voltage to generate the control signal, wherein in response to increasing of the operation power, the first comparison circuit increases a duty cycle of the comparison signal, and the second comparison circuit decreases the duty cycle of the control signal, so that the operation power of the power device decreases.

7. The current limiting circuit as claimed in claim 6, wherein the first comparison comprises: a comparator having an inverting input terminal coupled to a first node, a non-inverting input terminal receiving the first reference voltage, and an output terminal; and a capacitor coupled between the first node and a ground terminal, wherein the first input signal is provided to the first node, and the first input voltage is generated at the first node.

8. The current limiting circuit as claimed in claim 6, wherein the second comparison comprises: a comparator having a non-inverting input terminal coupled to a first node, an inverting input terminal coupled to a second node, and an output terminal; a current source providing a first current; a first switch controlled by the comparison signal and having an input terminal receiving the first current and an output terminal coupled to the first node; a first capacitor coupled between the first node and a ground terminal; a second switch coupled between the first node and the ground terminal; a third switch controlled by a switching signal and having an input terminal receiving the second input signal and an output terminal coupled to the second node; a second capacitor coupled between the second node and the ground terminal; and a fourth switch, coupled between the second node and the ground terminal, wherein the second reference voltage is generated at the first node, and the second input voltage is generated at the second node, and wherein the control signal is generated from the output terminal of the comparator.

9. The current limiting circuit as claimed in claim 1, wherein the detection circuit detects the cross voltage to generate the first detection signal and detects the load current flowing through the power device to generate the second detection signal.