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Circuit device

Abstract

Provided is a circuit device that can achieve A/D conversion at a high speed and a high resolution. This circuit device comprises: a gain adjustment circuit that adjusts the gain of an analog output signal outputted from a sensor; an offset adjustment circuit that adjusts the offset voltage of the analog output signal; an A/D converter that converts the analog output signal to a digital signal; and a control unit that sets the gain and the offset voltage of the analog output signal on the basis of the voltage value of a digital signal that was immediately previously converted by the A/D converter.

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References Cited

U.S. PATENT DOCUMENTS

Patent No.	Issued Date	Patentee Name	U.S. Cl.	CPC
2009/0212983	12/2008	Fukuzawa	341/142	H03F 3/45928
2009/0315745	12/2008	McLoughlin	341/118	H03M 1/183
2010/0110231	12/2009	Funabashi	327/321	H04N 5/185
2015/0066159	12/2014	Kubota	341/118	H03M 1/0617

FOREIGN PATENT DOCUMENTS

Patent No.	Application Date	Country	CPC
S61-065533	12/1985	JP	N/A
2000-009792	12/1999	JP	N/A
2002-135118	12/2001	JP	N/A
2003-098002	12/2002	JP	N/A
2012-044347	12/2011	JP	N/A
2014-199181	12/2013	JP	N/A
2019-186626	12/2018	JP	N/A
2013/168284	12/2012	WO	N/A

OTHER PUBLICATIONS

International Search Report issued in PCT/JP2021/028514; mailed Oct. 12, 2021. cited by applicant

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Background/Summary

TECHNICAL FIELD

(1) The present invention relates to a circuit device.

BACKGROUND ART

(2) A circuit device that performs analog-to-digital conversion (hereinafter referred to as A/D conversion) requires an A/D converter having high resolution for a wide measurement range and high-precision measurement (for example, see Patent Document 1). The integrated circuit device described in Patent Document 1 includes an amplifier circuit and an A/D converter that performs A/D conversion on an output signal of the amplifier circuit, and the amplifier circuit is configured by a switched capacitor circuit that cancels an offset voltage of an operational amplifier included in the amplifier circuit.

CITATION LIST

Patent Document

(3) Patent Document 1: Japanese Unexamined Patent Application, Publication No. 2012-44347

DISCLOSURE OF THE INVENTION

Problems to be Solved by the Invention

(4) However, since the A/D converter having high resolution takes a long time for A/D conversion, the analog signal may not be converted into a digital signal within a desired time. Therefore, there is a demand for a circuit device capable of realizing A/D conversion at high speed with high resolution.

Means for Solving the Problems

(5) A circuit device according to an aspect of the present disclosure includes: a gain adjustment circuit that adjusts a gain of an analog output signal outputted from a sensor; an offset adjustment circuit that adjusts an offset voltage of the analog output signal; an A/D converter that converts the analog output signal to a digital signal; and a control unit that sets the gain and the offset voltage of the analog output signal based on a voltage value of the digital signal converted immediately before by the A/D converter.

Effects of the Invention

(6) According to an embodiment of the present invention, it is possible to realize A/D conversion at high speed with high resolution.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) FIG. 1 is a block diagram showing a configuration of a circuit device according to an embodiment of the present embodiment;

(2) FIG. 2 is a flowchart showing processing of the circuit device according to the first embodiment;

(3) FIG. 3 is a diagram showing processing of converting an analog output signal into a digital signal according to the first embodiment;

(4) FIG. 4 is a diagram showing a definition of a gain according to the first embodiment;

(5) FIG. 5 is a flowchart showing processing of a circuit device according to a second embodiment;

(6) FIG. 6 is a flowchart showing processing of calculation of a measured value and setting of gain and offset command values according to the second embodiment; and

(7) FIG. 7 is a diagram showing a relationship between an amount of change of a voltage value of a digital signal and setting of a gain and an offset voltage according to the second embodiment.

PREFERRED MODE FOR CARRYING OUT THE INVENTION

(8) Hereinafter, an example of an embodiment of the present invention will be described. FIG. 1 is a block diagram showing the configuration of a circuit device 1 according to the present embodiment. As shown in FIG. 1, the circuit device 1 includes a sensor 11, a gain adjustment circuit 12, an amplifier circuit 13, an A/D converter 14, an offset adjustment circuit 15, and a microcomputer 16.

(9) The sensor 11 includes a temperature sensor, a pressure sensor, a flow rate sensor, and the like, detects any physical quantity, and outputs an analog output signal as a detection result.

(10) The gain adjustment circuit 12 is electrically connected to the sensor 11, a resistor R2, the amplifier circuit 13, and the microcomputer 16. The gain adjustment circuit 12 includes, for example, a digital potentiometer. The gain adjustment circuit 12 adjusts the gain (amplification factor) of the analog output signal outputted from the sensor 11 by changing the resistance value of a variable resistor R1 using a digital potentiometer based on a gain adjustment command from the microcomputer 16. In the present embodiment, the resistance value is uniquely determined with

respect to the gain.

(11) The amplifier circuit **13** is electrically connected to the gain adjustment circuit **12**, the resistor **R2**, the A/D converter **14**, and the offset adjustment circuit **15**. The amplifier circuit **13** adds the offset voltage adjusted by the offset adjustment circuit **15** to the analog output signal adjusted by the gain adjustment circuit **12**. The amplifier circuit **13** amplifies the analog output signal obtained by adding the offset voltage. The amplifier circuit **13** outputs the amplified analog output signal to the A/D converter **14**. Thus, the variable resistor **R1**, the resistor **R2**, and the amplifier circuit **13** constitute an inverting amplifier circuit, and the gain can be determined from the resistance values of the variable resistor **R1** and the resistor **R2**.

(12) The A/D converter **14** is electrically connected to the amplifier circuit **13** and the microcomputer **16**. The A/D converter **14** converts (A/D conversion) the analog output signal amplified by the amplifier circuit **13** into a digital signal. The A/D converter **14** outputs the A/D converted digital signal to the microcomputer **16**.

(13) The offset adjustment circuit **15** is electrically connected to the amplifier circuit **13** and the microcomputer **16**. The offset adjustment circuit **15** includes, for example, a D/A converter, a digital potentiometer, and the like. The offset adjustment circuit **15** adjusts the voltage division by the D/A converter, the digital potentiometer, or the like, thereby adjusting the offset voltage of the analog output signal based on an offset adjustment command from the microcomputer **16**.

(14) The microcomputer **16** is electrically connected to the gain adjustment circuit **12**, the A/D converter **14**, and the offset adjustment circuit **15**, and executes various control functions. The microcomputer **16** includes a control unit **161** that controls the gain adjustment circuit **12**, the A/D converter **14**, and the offset adjustment circuit **15**.

(15) The control unit **161** sets the gain of the analog output signal in the gain adjustment circuit **12** and the offset voltage in the offset adjustment circuit **15** based on the voltage value of the digital signal converted immediately before by the A/D converter **14**. As described above, the circuit device **1** according to the present embodiment dynamically changes the gain and offset voltage of the analog output signal, and A/D-converts the changed analog output signal, thereby achieving A/D conversion at higher speed and higher resolution than when the gain is fixed. Hereinafter, specific processing of the circuit device **1** according to the first embodiment and the second embodiment will be described.

First Embodiment

(16) FIG. **2** is a flowchart showing processing of the circuit device **1** according to the first embodiment. In Step **S1**, the circuit device **1** adjusts the first gain and the offset voltage.

Specifically, the control unit **161** outputs a gain adjustment command to the gain adjustment circuit **12** so that the first gain $G_{\text{sub.1}}$ of the analog output signal is set to $G_{\text{sub.1}}=1$.

(17) Further, the control unit **161** outputs an offset adjustment command to the offset adjustment circuit **15** so that the first offset voltage $V_{\text{sub.off1}}$ of the analog output signal is set to $V_{\text{sub.off1}}=v_{\text{off_init}}$.

(18) Here, when the gain $G_{\text{sub.1}}$ is 1, the resolution in the A/D conversion becomes a minimum, and the measurement range in the A/D conversion becomes a maximum. $V_{\text{sub.off_init}}$ is, for example, a value set at the time of factory shipment.

(19) Then, the sensor **11** outputs the analog output signal $V_{\text{sub.a}}$, and the gain adjustment circuit **12** adjusts the first gain $G_{\text{sub.1}}$ of the analog output signal $V_{\text{sub.a}}$ based on the gain adjustment command. The offset adjustment circuit **15** adjusts the first offset voltage $V_{\text{sub.off1}}$ based on the offset adjustment command.

(20) In Step **S2**, the circuit device **1** performs the first A/D conversion. Specifically, the amplifier circuit **13** adds the first offset voltage $V_{\text{sub.off1}}$ adjusted by the offset adjustment circuit **15** to the analog output signal having a gain adjusted by the gain adjustment circuit **12**. The amplifier circuit **13** amplifies the analog output signal obtained by adding the first offset voltage $V_{\text{sub.off1}}$. The amplifier circuit **13** outputs the amplified analog output signal to the A/D converter **14**.

(21) The A/D converter **14** converts the analog output signal amplified by the amplifier circuit **13** into a digital signal. The A/D converter **14** outputs the A/D converted first digital signal V.sub.b1 to the microcomputer **16**. Further, the A/D converter **14** may output information on the occurrence of overflow and/or underflow in the A/D conversion to the microcomputer **16**.

(22) In Step S3, the circuit device **1** acquires first measurement information. Specifically, the control unit **161** calculates the first sensor voltage V.sub.d1 in the first measurement based on the first digital signal V.sub.b1 outputted from the A/D converter **14**. The first sensor voltage V.sub.d1 is calculated by using the following equation (1).

[Formula1]

$$(23) \quad V_{d1} = (V_{upper_lim_max} - V_{lower_lim_min}) \cdot \text{Math.} \frac{(V_{b1})_{10}}{2^N} + V_{lower_lim_min} \quad (1)$$

(24) Here, V.sub.upper_lim_max and V.sub.lower_lim_min are the upper limit value and the lower limit value of the measurement range when the gain is a minimum (in a case where the gain and offset voltage are initial values), respectively, and these values are values which can be known in advance. V.sub.b1 is a voltage obtained from the A/D converter **14**, and V.sub.b1 is a binary value. N is the number of bits of V.sub.b1. In equation (1), (V.sub.b1).sub.10 represents a decimal value of V.sub.b1.

(25) FIG. 3 is a diagram showing processing of converting an analog output signal into a digital signal according to the first embodiment. As shown in FIG. 3, the analog output signal V.sub.a is A/D converted by the A/D converter **14**, and the first sensor voltage V.sub.d1 is calculated based on the first digital signal V.sub.b1 outputted from the A/D converter **14**.

(26) Referring back to FIG. 2, in Step S4, the circuit device **1** sets the second gain G.sub.2 and the second offset voltage V.sub.off2 of the A/D conversion. Specifically, the control unit **161** calculates the setting values of the second gain G.sub.2 and the second offset V.sub.off2 in the second measurement based on the first sensor voltage V.sub.d1, and equations (2) and (3).

$$(27) \quad G_2 = 2^K \quad (2) \quad V_{off2} = V_{d1} \quad (3)$$

(28) Equation (2) is a gain setting in a case where the Kbit resolution is higher than the resolution in the first A/D conversion. K is a value determined in advance. Equation (3) sets the second offset voltage V.sub.off2 to the first sensor voltage V.sub.d1. In the second measurement, the measurement range is narrowed while the resolution increases. Therefore, only the voltage near the first sensor voltage V.sub.d1 obtained by the first measurement is measured. Thus, when the original resolution of the A/D converter **14** is N bits, the resolution of the obtained measurement value is N+K bits.

(29) FIG. 4 is a diagram showing a definition of a gain according to the first embodiment. As shown in FIG. 4, the gain G is defined as follows.

$$(30) \quad G \cdot \text{Math.} (V_{upper_lim} - V_{lower_lim}) = \Delta V_{ma} (= \text{constant})$$

(31) As shown in FIG. 4, in the first A/D conversion, the gain is set to G.sub.1=1, and the measurement range is the maximum measurable range (full range) of the A/D converter **14**. In the second A/D conversion, in a case of K=1 in expression (2), the gain is set to G.sub.2=2, the resolution is higher than the resolution in the first A/D conversion, and the measurement range is 1/2 of the measurement range in the first A/D conversion.

(32) Referring back to FIG. 2, in Step S5, the circuit device **1** performs second adjustment of the second gain G.sub.2 and the second offset voltage V.sub.off2. Specifically, the control unit **161** outputs a gain adjustment command to the gain adjustment circuit **12**, and the gain adjustment circuit **12** adjusts the second gain G.sub.2 of the analog output signal to G.sub.2=2.sup.K based on the gain adjustment command. Further, the control unit **161** outputs an offset adjustment command to the offset adjustment circuit **15**, and the offset adjustment circuit **15** adjusts the second offset voltage V.sub.off2 of the analog output signal to V.sub.off2=V.sub.d1 based on the offset adjustment command.

(33) In Step S6, the circuit device **1** performs the second A/D conversion. Specifically, the amplifier circuit **13** adds the second offset voltage $V_{\text{sub.off2}}$ adjusted by the offset adjustment circuit **15** to the analog output signal adjusted to the second gain $G_{\text{sub.2}}$ by the gain adjustment circuit **12**. The amplifier circuit **13** amplifies the analog output signal obtained by adding the second offset voltage $V_{\text{sub.off2}}$. The amplifier circuit **13** outputs the amplified analog output signal to the A/D converter **14**.

(34) The A/D converter **14** converts the analog output signal amplified by the amplifier circuit **13** into a second digital signal $V_{\text{sub.b2}}$. The A/D converter **14** outputs the A/D converted second digital signal $V_{\text{sub.b2}}$ to the microcomputer **16**. The A/D converter **14** outputs information on the occurrence of overflow and/or underflow in the A/D conversion to the microcomputer **16**.

(35) In Step S7, the circuit device **1** acquires the second measurement information. Specifically, in Step S6, the control unit **161** calculates the second sensor voltage $V_{\text{sub.d2}}$ in the second measurement based on the second digital signal $V_{\text{sub.b2}}$ outputted from the A/D converter **14**. The second sensor voltage $V_{\text{sub.d2}}$ is calculated by using the following equations (4) to (6). In equation (4), $(V_{\text{sub.b2}})_{\text{sub.10}}$ represents a decimal value of $V_{\text{sub.b1}}$.

[Formula2]

$$(36) \quad V_{d2} = (V_{\text{upper_lim}} - V_{\text{lower_lim}}) \cdot \text{Math} \cdot \frac{(V_{b2})_{10}}{2^N} + V_{\text{lower_lim}} \quad (4)$$

$$V_{\text{upper_lim}} = V_{\text{off2}} + \frac{V_{\text{upper_lim_max}} - V_{\text{lower_lim_min}}}{2 \cdot \text{Math} \cdot G_2} \quad (5) \quad V_{\text{lower_lim}} = V_{\text{off2}} - \frac{V_{\text{upper_lim_max}} - V_{\text{lower_lim_min}}}{2 \cdot \text{Math} \cdot G_2} \quad (6)$$

(37) Here, $V_{\text{sub.upper_lim}}$ and $V_{\text{sub.lower_lim}}$ are the maximum value and the minimum value of the measurement range in the second A/D conversion, respectively. $V_{\text{sub.upper_lim}}$ is calculated using Equation (5), and $V_{\text{sub.lower_lim}}$ is calculated using Equation (6). As described above, $V_{\text{sub.upper_lim}}$ and $V_{\text{sub.lower_lim}}$ are calculated based on gain $G_{\text{sub.2}}$ and offset $V_{\text{sub.off2}}$ in the second measurement.

(38) In Step S8, the control unit **161** transmits the second sensor voltage $V_{\text{sub.d2}}$ calculated in Step S7, the gain and offset voltage set in the A/D conversion, and information on the occurrence of overflow and/or underflow in the A/D conversion to the host system.

(39) As described above, according to the first embodiment, the control unit **161** sets the first gain $G_{\text{sub.1}}$ and the first offset voltage $V_{\text{sub.off1}}$ of the analog output signal so that the measurement range of the A/D converter **14** matches the voltage range of the analog output signal, and the A/D converter **14** converts the analog output signal adjusted by the first gain $G_{\text{sub.1}}$ and the first offset voltage $V_{\text{sub.off1}}$ into a digital signal.

(40) Then, the control unit **161** calculates the first sensor voltage $V_{\text{sub.d1}}$ based on the first digital signal $V_{\text{sub.b1}}$ converted by the A/D converter, sets the second offset voltage $V_{\text{sub.off2}}$ of the analog output signal in the offset adjustment circuit **15** based on the first sensor voltage $V_{\text{sub.d1}}$, and sets the second gain $G_{\text{sub.2}}$ of the analog output signal in the gain adjustment circuit **12** to a value larger than the first gain $G_{\text{sub.1}}$. The A/D converter **14** converts an analog output signal adjusted by the second gain $G_{\text{sub.2}}$ and the second offset voltage $V_{\text{sub.off2}}$ into a digital signal.

(41) Thus, the circuit device **1** according to the first embodiment converts the analog output signal into a digital signal in the maximum measurement range of the A/D converter **14** in the first A/D conversion by setting the first gain $G_{\text{sub.1}}$ and the first offset voltage $V_{\text{sub.off1}}$. By setting the second gain $G_{\text{sub.2}}$ and the second offset voltage $V_{\text{sub.off2}}$, the circuit device **1** narrows the measurement range of the A/D converter **14** and converts the analog output signal into a digital signal with high resolution in the second A/D conversion.

(42) Therefore, since the circuit device **1** can increase the resolution of the A/D converter **14** and narrow the measurement range in the second A/D conversion, for example, the circuit device **1** can perform A/D conversion over a wide range and high resolution at high speed by using the A/D converter **14** with low resolution and high speed.

(43) The control unit **161** further calculates the second sensor voltage $V_{\text{sub.d2}}$ based on the second

digital signal $V_{sub.b2}$ converted by the A/D converter **14** and the upper limit value $V_{sub.upper_lim}$ and the lower limit value $V_{sub.lower_lim}$ of the measurement range in the A/D converter **14**, and transmits the calculated second sensor voltage $V_{sub.d2}$ to the host device. Thus, the circuit device **1** can calculate the second sensor voltage $V_{sub.d2}$ from the second digital signal $V_{sub.b2}$ obtained by A/D conversion over a wide range and high resolution, and transmit the second sensor voltage $V_{sub.d2}$ to the host device. Therefore, the circuit device **1** can transmit the second sensor voltage $V_{sub.d2}$ measured with high accuracy to the host device.

Second Embodiment

(44) FIG. 5 is a flowchart showing processing of the circuit device **1** according to a second embodiment. The circuit device **1** according to the second embodiment has the same configuration as the circuit device shown in FIG. 1, but differs from the circuit device **1** according to the first embodiment in processing contents. Specifically, the circuit device **1** according to the second embodiment sets a wide measurement range in the A/D conversion when the amount of change in the sensor voltage outputted from the A/D converter **14** is large, and sets a narrow measurement range in the A/D conversion when the amount of change in the sensor voltage outputted from the A/D converter **14** is small.

(45) In Step S11, the circuit device **1** adjusts the gain and offset voltage. Specifically, the control unit **161** outputs a gain adjustment command to the gain adjustment circuit **12**, and the gain adjustment circuit **12** adjusts the gain $G_{sub.1}$ of the analog output signal based on the gain adjustment command.

(46) Further, the control unit **161** outputs an offset adjustment command to the offset adjustment circuit **15**, and the offset adjustment circuit **15** adjusts the offset voltage $V_{sub.off1}$ of the analog output signal based on the offset adjustment command. Here, the gain G and the offset voltage $V_{sub.off}$ are adjusted to the gain and the offset voltage used in the previous measurement (for example, processing corresponding to the processing of Step S4 in FIG. 2).

(47) In Step S12, the circuit device **1** performs A/D conversion. Specifically, the sensor **11** outputs the analog output signal $V_{sub.a}$, and the gain adjustment circuit **12** adjusts the gain of the analog output signal $V_{sub.a}$ based on the gain adjustment command. The amplifier circuit **13** adds the offset voltage adjusted by the offset adjustment circuit **15** to the analog output signal adjusted by the gain adjustment circuit **12**. The amplifier circuit **13** amplifies the analog output signal obtained by adding the offset voltage. The amplifier circuit **13** outputs the amplified analog output signal to the A/D converter **14**.

(48) The A/D converter **14** converts the analog output signal amplified by the amplifier circuit **13** into a digital signal. The A/D converter **14** outputs the A/D converted digital signal $V_{sub.b2}$ to the microcomputer **16**. Further, the A/D converter **14** outputs information on the occurrence of overflow and/or underflow in the A/D conversion to the microcomputer **16** together with the digital signal $V_{sub.b}$.

(49) In Step S13, the circuit device **1** performs calculation of a measured value and sets gain and offset command values. Specifically, the control unit **161** calculates the sensor voltage $V_{sub.d}$, the gain $G_{sub.next}$, and the offset voltage $V_{sub.off_next}$ at the time of the next A/D conversion based on the digital signal $V_{sub.b}$ (binary number) output from the A/D converter **14**.

(50) The processing of Step S13 will be described in detail with reference to FIG. 6. FIG. 6 is a flowchart showing calculation of a measured value and setting of gain and offset command values according to the second embodiment.

(51) In Step S131, the control unit **161** determines whether an overflow has occurred in the A/D conversion. When the overflow occurs (YES), the processing advances to Step S132. On the other hand, when no overflow occurs (NO), the processing advances to Step S133.

(52) In Step S132, the control unit **161** sets the upper limit voltage $V_{sub.upper_lim}$ of the measurement range as the sensor voltage $V_{sub.d}$ as shown in the following Equation (11).

$$(53) \quad V_d = V_{\text{upper_lim}} \quad (11)$$

(54) In Step S133, the control unit **161** determines whether or not underflow has occurred in the A/D conversion. When underflow has occurred (YES), the processing advances to Step S134. On the other hand, when underflow has not occurred (NO), the processing advances to Step S136.

(55) In Step S134, the control unit **161** sets the lower limit voltage $V_{\text{sub.lower_lim}}$ of the measurement range as the sensor voltage $V_{\text{sub.d}}$ as shown in the following Equation (12).

$$(56) \quad V_d = V_{\text{lower_lim}} \quad (12)$$

(57) In Step S135, the control unit **161** calculates the setting values of the gain and offset voltage in the next A/D conversion. When overflow or underflow occurs in the current A/D conversion, the control unit **161** sets the gain $G_{\text{sub.next}}$ and the offset voltage $V_{\text{sub.off_next}}$ to initial values for the next A/D conversion, as shown in the following Equations (13) and (14).

$$(58) \quad G_{\text{next}} = 1 \quad (13) \quad V_{\text{off_next}} = V_{\text{off_init}} \quad (14)$$

(59) In Step S136, the control unit **161** calculates the sensor voltage $V_{\text{sub.d}}$ based on the digital signal $V_{\text{sub.b}}$ (binary number) outputted from the A/D converter **14** and the following Equations (15), (16) and (17). In Equation (15), $(V_{\text{sub.b}})_{\text{sub.10}}$ represents a decimal value of $V_{\text{sub.b}}$.

[Formula3]

$$(60) \quad V_d = \frac{(V_b)_{10}}{2^N} \cdot \text{Math.} (V_{\text{upper_lim}} - V_{\text{lower_lim}}) + V_{\text{lower_lim}} \quad (15)$$

$$V_{\text{upper_lim}} = V_{\text{off}} + \frac{V_{\text{upper_lim_max}} - V_{\text{lower_lim_min}}}{2 \cdot \text{Math.} G} \quad (16) \quad V_{\text{lower_lim}} = V_{\text{off}} - \frac{V_{\text{upper_lim_max}} - V_{\text{lower_lim_min}}}{2 \cdot \text{Math.} G} \quad (17)$$

(61) In Step S137, the control unit **161** calculates the setting values of the gain and offset voltage in the next A/D conversion. The control unit **161** calculates the gain $G_{\text{sub.next}}$ using the following Equation (18).

[Formula4]

$$(62) \quad G_{\text{next}} = \begin{cases} G \times 2 & \text{if } \text{Math.} \frac{V_d - V_{d-1}}{V_{\text{upper_lim}} - V_{\text{lower_lim}}} \cdot \text{Math.} < \alpha \\ G / 2 & \text{elseif } \text{Math.} \frac{V_d - V_{d-1}}{V_{\text{upper_lim}} - V_{\text{lower_lim}}} \cdot \text{Math.} > \beta \\ G & \text{else} \end{cases} \quad (18)$$

(63) That is, the control unit **161** compares the sensor voltage $V_{\text{sub.d-1}}$ in the previous A/D conversion with the sensor voltage $V_{\text{sub.d}}$ in the current A/D conversion. When the amount of change between the sensor voltage $V_{\text{sub.d-1}}$ and the sensor voltage $V_{\text{sub.d}}$ is less than a threshold value α , the control unit **161** sets the gain $G_{\text{sub.next}}$ to a value larger than the previous gain in order to increase the resolution.

(64) On the other hand, when the amount of change between the sensor voltage $V_{\text{sub.d-1}}$ and the sensor voltage $V_{\text{sub.d}}$ exceeds a threshold value β , the control unit **161** sets the gain $G_{\text{sub.next}}$ to a value smaller than the previous gain in order to widen the measurement range. When the amount of change is equal to or greater than the threshold value α or equal to or less than the threshold value β , the control unit **161** maintains the value of the gain $G_{\text{sub.next}}$ at the previous value, i.e., does not change the value of the gain $G_{\text{sub.next}}$. In Equation (18), the coefficients (2 and $\frac{1}{2}$) multiplied by the gain are any values and are not limited to the above values.

(65) Further, the control unit **161** calculates the offset voltage $V_{\text{sub.off_next}}$ using the following Equation (19).

$$V_{\text{sub.off_next}} = V_{\text{sub.d}}(V_{\text{sub.d}} - V_{\text{sub.d-1}}) \quad \text{Equation (19)}$$

That is, the offset voltage $V_{\text{sub.off_next}}$ is a value obtained by adding the difference between the previous sensor voltage $V_{\text{sub.d-1}}$ and the current sensor voltage $V_{\text{sub.d}}$ to the current sensor voltage $V_{\text{sub.d}}$. Thus, when the amount of change of the sensor voltage is constant, the sensor voltage is set to be the center of the measurement range.

(66) In Step S138, the control unit **161** determines whether or not the gain $G_{\text{sub.next}}$ calculated in

Step S137 is within a predetermined range. When the gain G.sub.next is not within the predetermined range, the control unit **161** sets the gain G.sub.next to the upper limit value (G.sub.next=G.sub.max) or the lower limit value (G.sub.next=1) of the gain using the following Equation (20).

[Formula5]

$$(67) \quad G_{\text{next}} = \begin{cases} G_{\text{max}} & \text{if } G_{\text{next}} > G_{\text{max}} \\ 1 & \text{if } G_{\text{next}} < 1 \end{cases} \quad (20)$$

(68) Referring back to FIG. 5, in Step S14, the control unit **161** transmits the sensor voltage V.sub.d calculated in Step S132, Step S134, or Step S136, the gain and offset voltage set at the time of A/D conversion, and information on the occurrence of overflow and/or underflow in A/D conversion to the host system.

(69) Further, the control unit **161** stores the sensor voltage V.sub.d and the gain and offset voltage set at the time of A/D conversion in the storage area of the microcomputer **16** in order to use them for subsequent measurements.

(70) FIG. 7 is a diagram showing a relationship between an amount of change in a voltage value of a digital signal and setting of a gain and an offset voltage according to the second embodiment.

(71) As shown in FIG. 7, when the amount of change is less than the threshold value α , the control unit **161** sets the gain G.sub.next to a value larger than the previous gain. When the amount of change exceeds the threshold value β , the control unit **161** sets the gain G.sub.next to a value smaller than the previous gain in order to widen the measurement range.

(72) When the amount of change is equal to or greater than the threshold value α or equal to or less than the threshold value β , the control unit **161** maintains the value of the gain G.sub.next at the previous value, i.e., does not change the value of the gain G.sub.next. The offset voltage V.sub.off_next is a value obtained by adding the difference between the previous sensor voltage V.sub.d-1 and the current sensor voltage V.sub.d to the current sensor voltage V.sub.d.

(73) As described above, according to the second embodiment, the control unit **161** compares the sensor voltage V.sub.d-1 based on the digital signal obtained by the previous A/D conversion with the sensor voltage V.sub.d based on the digital signal obtained by the current A/D conversion, and when the amount of change from the sensor voltage V.sub.d-1 to the sensor voltage V.sub.d is less than the threshold value α , sets the gain G.sub.next of the analog output signal to a value larger than the gain of the previous time, and when the amount of change exceeds the threshold value β , sets the gain G.sub.next of the analog output signal to a value smaller than the gain of the previous time.

(74) With such a configuration, in the circuit device **1** according to the second embodiment, when the amount of change in the sensor voltage is less than the threshold value α , it is possible to increase the resolution by setting the gain to a value larger than the gain of the previous time. On the other hand, in the circuit device **1**, when the amount of change in the sensor voltage exceeds the threshold value β , it is possible to narrow the resolution by setting the gain to a value smaller than the gain of the previous time. Accordingly, it is possible for the circuit device **1** to set the resolution according to the amount of change in the sensor voltage, and perform A/D conversion in a wide range and high resolution at high speed.

(75) The control unit **161** sets the offset voltage V.sub.off_next of the analog output signal based on the sensor voltage V.sub.d-1 based on the digital signal obtained by the previous A/D conversion and the sensor voltage V.sub.d based on the digital signal obtained by the current A/D conversion. With such a configuration, it is possible for the circuit device **1** to set the sensor voltage to be the center of the measurement range when the amount of change of the sensor voltage is constant.

(76) Further, the A/D converter **14** outputs information on the occurrence of overflow and/or underflow in the A/D conversion together with the digital signal to the control unit **161**. The control unit **161** calculates the sensor voltage V.sub.d as the upper limit of the measurement range of the

A/D converter **14** when overflow occurs in the A/D conversion, calculates the sensor voltage $V_{sub.d}$ as the lower limit of the measurement range of the A/D converter **14** when underflow occurs in the A/D conversion, and sets the gain and offset voltage in the next A/D conversion to the initial values when overflow or underflow occurs in the A/D conversion. With such a configuration, even when overflow and/or underflow occurs, it is possible for the circuit device **1** to set the sensor voltage, the gain, and the offset voltage to appropriate values.

(77) Although the above-described embodiments are preferred embodiments of the present invention, the scope of the present invention is not to be limited to the above-described embodiments, and various modifications can be made without departing from the gist of the present invention.

EXPLANATION OF REFERENCE NUMERALS

(78) **1** circuit device **11** sensor **12** gain adjustment circuit **13** amplifier circuit **14** A/D converter **15** offset adjustment circuit **16** microcomputer **161** control unit

Claims

1. A circuit device comprising: a gain adjustment circuit that adjusts a gain of an analog output signal outputted from a sensor; an offset adjustment circuit that adjusts an offset voltage of the analog output signal; an A/D converter that converts the analog output signal to a digital signal; and a control unit that sets the gain and the offset voltage of the analog output signal based on a voltage value of the digital signal converted immediately before by the A/D converter, wherein the control unit sets a first gain and a first offset voltage of the analog output signal so that a measurement range of the A/D converter matches a voltage range of the analog output signal, and the control unit calculates a first sensor voltage based on a first digital signal converted by the A/D converter, sets a second offset voltage of the analog output signal in the offset adjustment circuit based on the first sensor voltage, and sets a second gain of the analog output signal in the gain adjustment circuit to a value larger than the first gain.
2. The circuit device according to claim 1, wherein the control unit further calculates a second sensor voltage based on a second digital signal converted by the A/D converter, and an upper limit value and a lower limit value for the measurement range in the A/D converter, and transmits the calculated second sensor voltage to a host device.
3. A circuit device comprising: a gain adjustment circuit that adjusts a gain of an analog output signal outputted from a sensor; an offset adjustment circuit that adjusts an offset voltage of the analog output signal; an A/D converter that converts the analog output signal to a digital signal; and a control unit that sets the gain and the offset voltage of the analog output signal based on a voltage value of the digital signal converted immediately before by the A/D converter, wherein the control unit compares a third sensor voltage based on the digital signal obtained by a previous A/D conversion with a fourth sensor voltage based on the digital signal obtained by a current A/D conversion, and when an amount of change from the third sensor voltage to the fourth sensor voltage is less than a first threshold, sets a third gain of the analog output signal to a value larger than a previous gain, and when the amount of change exceeds a second threshold, sets the third gain of the analog output signal to a value smaller than the previous gain.
4. The circuit device according to claim 3, wherein the control unit sets a third offset voltage of the analog output signal based on the third sensor voltage based on the digital signal obtained by the previous A/D conversion, and the fourth sensor voltage based on the digital signal obtained by the current A/D conversion.
5. The circuit device according to claim 3, wherein the A/D converter outputs information on an occurrence of overflow and/or underflow in the A/D conversion to the control unit together with the digital signal, and the control unit calculates the fourth sensor voltage as an upper limit value of a measurement range of the A/D converter when an overflow occurs in the A/D conversion,

calculates the fourth sensor voltage as a lower limit value of the measurement range of the A/D converter when an underflow occurs in the A/D conversion, and sets a gain and offset voltage in a next A/D conversion to initial values when an overflow or underflow occurs in the A/D conversion.
