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Inventor(s)	Cheng; Kai

Semiconductor structure with diffusion blocking layer and preparing method for semiconductor structure

Abstract

Disclosed are a semiconductor structure and a preparing method for a semiconductor structure, which relate to the technical field of microelectronics. The semiconductor structure includes a buffer layer including a diffusion element; a diffusion blocking layer formed on the buffer layer, the diffusion blocking layer including an adsorptive element; and a channel layer formed on the diffusion blocking layer. In this embodiment, the diffusion blocking layer is provided with an adsorptive element that adsorbs the diffusion element, so as to effectively block the diffusion of the diffusion element to the channel layer from the buffer layer. In addition, a change in the composition of the adsorptive element in the diffusion blocking layer is provided to avoid stress release of the diffusion blocking layer.

Inventors: **Cheng; Kai (Suzhou, CN)**

Applicant: **ENKRIS SEMICONDUCTOR, INC.** (Suzhou, CN)

Family ID: **1000008750548**

Assignee: **ENKRIS SEMICONDUCTOR, INC. (Suzhou, CN)**

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References Cited

U.S. PATENT DOCUMENTS

Patent No.	Issued Date	Patentee Name	U.S. Cl.	CPC
5448084	12/1994	Hoke	257/E29.32	H10D 30/4732
8545629	12/2012	Schowalter	117/952	C30B 25/16
9076812	12/2014	Laboutin	N/A	H01L 29/7786
9627489	12/2016	Hung	N/A	H10D 62/357
2004/0169194	12/2003	Noda	257/190	H10D 30/4738
2005/0173728	12/2004	Saxler	257/E29.093	H01L 29/2003
2007/0252135	12/2006	Lee	257/E33.001	H10H 20/825
2008/0093610	12/2007	Lee	257/94	H10H 20/825
2008/0157058	12/2007	Hudait	257/14	H01L 21/0251
2008/0182369	12/2007	Jeong	257/E29.127	H10D 30/015
2008/0203430	12/2007	Simin	257/192	H01L 29/7783
2008/0258135	12/2007	Hoke	257/E29.069	H10D 62/852
2009/0045438	12/2008	Inoue	257/E29.091	H01L 29/155
2009/0072220	12/2008	Lee	257/E21.085	H10H 20/83
2010/0012987	12/2009	Yeh	257/253	G01N 27/414
2010/0117118	12/2009	Dabiran	257/190	H01L 29/7787
2010/0270591	12/2009	Ahn	257/E21.403	H01L 29/7782
2011/0027974	12/2010	Su	257/E21.09	H01L 21/0262
2011/0064103	12/2010	Ohta	372/45.01	H01L 21/0254
2013/0113018	12/2012	Wakita	257/190	H01L 29/205

2013/0189817	12/2012	Peroni	438/172	H01L 29/42316
2013/0316507	12/2012	Saitoh	438/285	H10D 62/8503
2015/0017789	12/2014	Hashimoto	438/503	H10D 30/871
2015/0041825	12/2014	Liu et al.	N/A	N/A
2016/0336314	12/2015	Chou	N/A	H10D 62/343
2017/0125573	12/2016	Lin	N/A	H01L 29/0619
2018/0069086	12/2017	Ishiguro	N/A	H10D 30/015
2019/0020318	12/2018	Ishiguro	N/A	H01L 21/0254
2020/0135445	12/2019	Yamazaki	N/A	H10D 87/00
2021/0183649	12/2020	Dahl	N/A	H01L 21/02458

FOREIGN PATENT DOCUMENTS

Patent No.	Application Date	Country	CPC
1698212	12/2004	CN	N/A
101027791	12/2006	CN	H01L 33/02
101390201	12/2008	CN	N/A
101789446	12/2009	CN	N/A
102265474	12/2010	CN	B82Y 20/00
102931229	12/2012	CN	N/A
103107190	12/2012	CN	H01L 29/778
104600109	12/2014	CN	N/A
106887494	12/2016	CN	N/A
107146832	12/2016	CN	H01L 33/007
108140563	12/2017	CN	C23C 16/303
108511522	12/2017	CN	H01L 29/267
108807527	12/2017	CN	H01L 21/8252
109638074	12/2018	CN	H01L 29/0603
109671815	12/2018	CN	N/A
2358736	12/2000	GB	H01L 21/02395
2009026975	12/2008	JP	H01L 21/338
2015122482	12/2014	JP	H01L 21/338
WO-0007248	12/1999	WO	H01L 21/28587
WO-0191188	12/2000	WO	H01L 21/28587
2018180021	12/2017	WO	N/A
2019097963	12/2018	WO	N/A

OTHER PUBLICATIONS

International Search Report issued in corresponding PCT Application No. PCT/CN2019/090554, dated Mar. 3, 2020. cited by applicant
Written Opinion issued in corresponding PCT Application No. PCT/CN2019/090554, dated Mar. 3, 2020. cited by applicant

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Primary Examiner: Geyer; Scott B

Attorney, Agent or Firm: Westbridge IP LLC

Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS (1) This application is a continuation of International Application No. PCT/CN2019/090554, filed on Jun. 10, 2019, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

(1) Embodiments of this application relates to the field of microelectronics technology, in particular to a semiconductor structure and a preparing method for a semiconductor structure.

BACKGROUND

(2) Currently, epitaxy is often used in the semiconductor industry. For example, a chemical vapor deposition (CVD) method is often used as an epitaxial method to form an epitaxial layer on a substrate. During the growth process, the epitaxial layer can be doped with impurities to control the electrical properties of the layer. For example, Be, Mg, C, Fe, and the like are commonly used as acceptor dopants in nitride semiconductor layers. However, among these elements, the use of Mg, Fe, etc. can cause the problem of “memory effect”, thereby adversely affecting the performance of the semiconductor devices.

SUMMARY

(3) In view of this, the present application provides a semiconductor structure and a preparing method for a semiconductor structure to avoid the memory effect of diffused element in the prior art.

(4) One aspect of the present application provides a semiconductor structure, including: a buffer layer, the buffer layer including a diffusion element; a diffusion blocking layer formed on the buffer layer, the diffusion blocking layer including an adsorptive element; and a channel layer on the diffusion blocking layer.

(5) In an embodiment of the present application, the diffusion element in the buffer layer includes a metal element.

(6) In an embodiment of the present application, the material used for the diffusion blocking layer includes a group III-V compound, and a group III element in the group III-V compound may be the adsorptive element.

(7) In an embodiment of the present application, the III-V compound includes a compound of In.

(8) In an embodiment of the present application, the compound of In includes InGaN.

(9) In an embodiment of the present application, the compound of In includes AlInGaN, wherein an Al composition is less than an In composition.

(10) In an embodiment of the present application, a composition of the adsorptive element in the diffusion blocking layer decreases along an epitaxial direction of the diffusion blocking layer.

(11) Another aspect of the present application provides a preparing method for a semiconductor structure, including: forming a buffer layer including a diffusion element; forming a diffusion blocking layer on the buffer layer, the diffusion blocking layer including an adsorptive element; forming a channel layer on the diffusion blocking layer.

(12) In an embodiment of the present application, the diffusion blocking layer includes a III-V compound, and a group III element in the III-V compound is the adsorptive element.

(13) In an embodiment of the present application, the III-V compound includes a compound of In.

(14) In an embodiment of the present application, the compound of In includes InGaN.

(15) In an embodiment of the present application, the compound of In includes AlInGaN, wherein an Al composition is less than an In composition.

(16) In an embodiment of the present application, a composition of the adsorptive element in the

diffusion blocking layer decreases, along an epitaxial direction of the diffusion blocking layer.
(17) In an embodiment of the present application, the diffusion element includes a metal element.
(18) In an embodiment of the present application, a formation temperature of the diffusion blocking layer does not exceed 900° C.
(19) In the embodiments, the diffusion blocking layer is provided with an adsorptive element that adsorbs the diffusion element, thereby effectively blocking the diffusion of the diffusion element to the channel layer from the buffer layer. In addition, the stress release of the diffusion blocking layer is avoided by setting the composition change of the adsorptive element in the diffusion blocking layer.

Description

BRIEF DESCRIPTION OF DRAWINGS
(1) In order to explain the technical solutions of the embodiments of the present application more clearly, the following will briefly introduce the drawings that need to be used in the embodiments. It should be understood that the following drawings only show certain embodiments of the present application, and therefore they should not be regarded as a limitation of the scope. For those of ordinary skill in the art, other related drawings can be obtained from these drawings without creative work.
(2) FIG. **1** is a schematic structural diagram of a semiconductor structure according to an embodiment of the present application.
(3) FIG. **2** to FIG. **5** are schematic diagrams of the composition changes of the adsorptive element in the diffusion blocking layer according to an embodiment of the present application, respectively.
(4) FIG. **6** is a schematic flowchart of a preparing method for a semiconductor structure according to an embodiment of the present application.
(5) FIG. **7** illustrates a high electron mobility transistor (HEMT) semiconductor device formed by a semiconductor structure.
(6) FIG. **8** and FIG. **9** are energy band structure diagrams of corresponding semiconductor devices.
DETAILED DESCRIPTION OF THE EMBODIMENTS
(7) With reference to the drawings in the embodiments of the present application, the technical solutions in the embodiments of the present application are clearly and completely described as follows. Apparently, the described embodiments are only a part of the embodiments of the present application, rather than all the embodiments. Based on the embodiments in this application, all other embodiments obtained by those of ordinary skill in the art without creative work shall fall within the protection scope of this application.
(8) Where possible, the same or similar parts in the drawings have the same reference signs.
(9) FIG. **1** is a schematic structural diagram of a semiconductor structure according to an embodiment of the present application, and the arrow direction in the figure is the epitaxial direction of the semiconductor structure.
(10) As shown in FIG. **1**, the semiconductor structure includes a buffer layer **1**, a diffusion blocking layer **2** and a channel layer **3**. The buffer layer **1** includes a diffusion element. The diffusion blocking layer **2** is formed on the buffer layer **1**, and includes an adsorptive element for preventing diffusion of the diffusion element. The channel layer **3** is formed on the diffusion blocking layer **2**.
(11) In this embodiment, the semiconductor structure also includes a substrate **0**, and the buffer layer **1** may be formed on the substrate **0**.
(12) Specifically, the diffusion element in the buffer layer **1** may be realized by intentional doping or may be inevitable in the epitaxial growth environment of the semiconductor structure. The diffusion element may include a metal element, for example, Fe, Mg, and the like. It is understandable that intentional doping of a diffusion element in the buffer layer **1** can increase the

electric resistivity of the buffer layer **1** and effectively increase the breakdown voltage of the semiconductor structure. However, a diffusion element generally has memory effect problems, that is, even if the doping of the diffusion element has been stopped during the growth of the buffer layer **1**, the diffusion element may still diffuse into the channel layer **3**, affecting the performance of the entire semiconductor device. Therefore, the diffusion blocking layer **2** is arranged to effectively block the diffusion element from diffusing to the channel layer **3** from the buffer layer **1**.

(13) Further, the diffusion blocking layer **2** includes an adsorptive element, and the composition of the adsorptive element in the diffusion blocking layer **2** varies, specifically, in the direction from the buffer layer **1** to the channel layer **3**, i.e., in the direction of semiconductor epitaxial growth, the composition of the adsorptive element in the diffusion blocking layer **2** decreases.

(14) Further, the diffusion blocking layer **2** may include a III-V compound, where the group III element may be used as an adsorptive element. For example, the III-V compound may include a compound of In, and the compound of In may include In.sub.xGa.sub.yN, where x+y=1.

(15) In the diffusion blocking layer **2** composed of In.sub.xGa.sub.yN, In in In.sub.xGa.sub.yN may be an adsorptive element, and the composition of In in In.sub.xGa.sub.yN decreases along the epitaxial growth direction, where the composition variation range of In is $0<x\leq 1$.

(16) Specifically, during the epitaxial growth of the diffusion blocking layer **2** composed of In.sub.xGa.sub.yN, the aforementioned In composition gradation can be realized by adjusting the growth temperature or the ratio of the indium source and the gallium source. For example, for the method of adjusting the growth temperature, the growth temperature may not exceed 900° C. Further, it may not exceed 850° C.

(17) In other embodiments, the diffusion blocking layer **2** may also be Al.sub.zIn.sub.xGa.sub.yN, where x+y+z=1, and the composition of Al is less than that of In, i.e. $z<x$, to ensure that the lattice constant of AlInGaN matches GaN better, thereby improving the quality of epitaxial growth.

(18) Further, the buffer layer **1** and the channel layer **3** include a nitride semiconductor layer, for example, a GaN-based material. The so-called GaN-based material is a semiconductor material that includes at least Ga atoms and N atoms, such as GaN, AlGaN, InGaN, AlInGaN, etc.

(19) Specifically, when the buffer layer **1** includes GaN and the diffusion blocking layer **2** includes InGaN, since the thermal mismatch and lattice mismatch between GaN and InGaN are relatively large, the diffusion blocking layer **2** will experience stress release, resulting in decreased quality of the semiconductor structure. By adjusting the In composition of InGaN in the diffusion blocking layer **2**, it is equivalent to multiple InGaN diffusion blocking layers **2** with different compositions, which can effectively avoid the stress release of the diffusion blocking layer **2**.

(20) In this embodiment, the diffusion blocking layer **2** is provided with an adsorptive element that adsorbs the diffusion element, so as to effectively block the diffusion of the diffusion element from the buffer layer **1** to the channel layer **3**. In addition, the stress release of the diffusion blocking layer **2** is avoided by setting changes in the composition of the adsorptive elements in the diffusion blocking layer **2**.

(21) FIG. **2** to FIG. **5** are schematic diagrams of the composition changes of the adsorptive elements in the diffusion blocking layer **2** according to an embodiment of the present application, respectively. The ordinate represents the component content of the adsorptive element in the diffusion blocking layer **2**, and the abscissa represents the epitaxial direction. It can be seen from FIG. **2** to FIG. **5** that the composition content of the adsorptive element in the diffusion blocking layer **2** decreases along the epitaxial direction.

(22) Specifically, in an embodiment of the present application, as shown in FIG. **2** and FIG. **5**, the composition content of the adsorptive element in the diffusion blocking layer **2** decreases along the epitaxial direction of the diffusion blocking layer **2**. Under such changes in the adsorptive element, a relatively flat quantum well structure can be realized.

(23) Or, as shown in FIG. **3** and FIG. **4**, the adsorptive element may gradually decrease in a

stepwise manner along the epitaxial direction of the diffusion blocking layer **2**. Under such changes in the adsorptive element, a multi-channel effect can be obtained, thereby reducing the spatial concentration of two-dimensional electron gas (**2**DEG) and increasing the mobility rate of carriers.
(24) Here, the epitaxial direction of the diffusion blocking layer **2** may refer to the epitaxial growth direction of the diffusion blocking layer **2** during preparation. When the diffusion blocking layer **2** includes In.sub.xGa.sub.yN, the In component may be an adsorptive element. Along the epitaxial direction of the diffusion blocking layer **2**, the In composition may decrease or reduce in a stepwise manner, that is, the X value decreases or reduces in a stepwise manner.
(25) Specifically, as shown in FIG. **2** to FIG. **5**, along the epitaxial direction of the diffusion blocking layer **2**, the adsorptive element composition in the diffusion blocking layer **2**, such as the In composition content, decreases in the direction of epitaxial growth. The content of the In component may reduce linearly, as shown in FIG. **2**; it may also reduce non-linearly, as shown in FIG. **5**. The content of the In component may reduce in a stepwise period, as shown in FIG. **3** to FIG. **4**; it may also reduce in other non-periodical manners. In this case, the manner in which the component of the adsorptive element decreases along the epitaxial growth direction is not limited, as long as the component of the adsorptive element in the diffusion blocking layer **2** shows a decreasing trend along the epitaxial growth direction.
(26) The semiconductor structure according to an embodiment of the present application is described above, and a preparing method for a semiconductor structure according to an embodiment of the present application is described below with reference to FIG. **6**.
(27) FIG. **6** is a schematic flowchart of a preparing method for a semiconductor structure according to an embodiment of the present application.
(28) As shown in FIG. **6**, the preparing method for a semiconductor structure may include the following steps.
(29) Step **510**, preparing a buffer layer **1** including a diffusion element.
(30) Specifically, the diffusion element in the buffer layer **1** may be realized by intentional doping or may be inevitable in the epitaxial growth environment of the semiconductor structure. The diffusion element may include a metal element, for example, Fe, Mg, and the like. It is understandable that intentional doping of a diffusion element in the buffer layer **1** can increase the electric resistivity of the buffer layer **1** and effectively increase the breakdown voltage of the semiconductor structure. However, a diffusion element generally has memory effect problems, that is, even if the doping of the diffusion elements has been stopped during the growth of the buffer layer **1**, the diffusion elements may still diffuse into the channel layer **3**, affecting the performance of the entire semiconductor device. Therefore, the diffusion blocking layer **2** is arranged to effectively block the diffusion elements from diffusing to the channel layer **3** from the buffer layer **1**.
(31) Step **520**, preparing a diffusion blocking layer **2** on the buffer layer **1**, where the diffusion blocking layer **2** includes an adsorptive element.
(32) Further, the diffusion blocking layer **2** includes an adsorptive element, and the composition of the adsorptive element in the diffusion blocking layer **2** varies, specifically, in the direction from the buffer layer **1** to the channel layer **3**, i.e., in the direction of semiconductor epitaxial growth, the composition of the adsorptive element in the diffusion blocking layer **2** decreases.
(33) In this embodiment, the epitaxial direction of the diffusion blocking layer **2** may refer to the epitaxial growth direction of the diffusion blocking layer **2** during preparation. When the diffusion blocking layer **2** is In.sub.xGa.sub.yN, the In component may be an adsorptive element. Along the epitaxial direction of the diffusion blocking layer **2**, the In composition can be reduced or stepped down, that is, the X value decrease or reduce in a stepwise manner. A relatively flat quantum well structure can be achieved, and an effect of a multi-channel structure can be obtained, thereby reducing the spatial concentration of two-dimensional electron gas (2DEG) and increasing the mobility rate of carriers.

(34) Further, the diffusion blocking layer **2** may include a III-V compound, where the group III element may be used as an adsorptive element. For example, the III-V compound may include a compound of In, and the compound of In may include In.sub.xGa.sub.yN, where x+y=1.
(35) In the diffusion blocking layer **2** composed of In.sub.xGa.sub.yN, In in In.sub.xGa.sub.yN may be an adsorptive element, and the composition of In in In.sub.xGa.sub.yN decreases along the epitaxial growth direction, where the composition variation range of In is $0<x\leq 1$.
(36) Specifically, during the epitaxial growth of the diffusion blocking layer **2** composed of In.sub.xGa.sub.yN, the aforementioned In composition gradation can be realized by adjusting the growth temperature or the ratio of the indium source and the gallium source. For example, for the method of adjusting the growth temperature, the growth temperature may be limited to not more than 900° C. Further, it may not exceed 850° C.
(37) Step **530**, preparing a channel layer **3** on the diffusion blocking layer **2**.
(38) Further, the buffer layer **1** and the channel layer **3** include a nitride semiconductor layer, for example, a GaN-based material. The so-called GaN-based material is a semiconductor material that includes at least Ga atoms and N atoms, such as GaN, AlGaN, InGaN, AlInGaN, etc.
(39) Specifically, when the buffer layer **1** includes GaN and the diffusion blocking layer **2** includes InGaN, since the thermal mismatch and lattice mismatch between GaN and InGaN are relatively large, resulting in stress release of the diffusion blocking layer **2**, resulting in decreased quality of the semiconductor structure. By adjusting the In composition of InGaN in the diffusion blocking layer **2**, it is equivalent to multiple InGaN diffusion blocking layers **2** with different compositions, which can effectively avoid the stress release of the diffusion blocking layer **2**.
(40) In this embodiment, the diffusion blocking layer **2** is provided with an adsorptive element that adsorbs the diffusion element, so as to effectively block the diffusion of the diffusion element from the buffer layer **1** to the channel layer **3**. In addition, the stress release of the diffusion blocking layer **2** is avoided by setting changes in the composition of the adsorptive elements in the diffusion blocking layer **2**.
(41) Further, when the semiconductor structure forms a semiconductor device such as an HEMT, as shown in FIG. **7**, it includes a substrate **0**, the buffer layer **1** formed on the substrate **0**, the diffusion blocking layer **2** formed on the buffer layer **1**, and the channel layer on the diffusion blocking layer **2**, a barrier layer **4** formed on the channel layer **3**, and a gate electrode **5**, a source electrode **6** and a drain electrode **7** formed on the barrier layer **4**.
(42) In this embodiment, the substrate **0** may include Si, SiC, sapphire, etc. The buffer layer **1** may include a metal element, for example, Fe, Mg, etc. The diffusion blocking layer **2** may include InGaN, where In is an adsorptive element that is used to block the metal element in the buffer layer **1** from diffusing to the channel layer **3** and affecting the performance of the device. The channel layer **3** can include GaN, and the barrier layer **4** can include AlGaN. The channel layer **3** just needs to form a heterojunction with the barrier layer **4**, and a quantum well is formed at its interface to confine the carriers in the quantum well to form a two-dimensional electron gas channel.
(43) FIG. **8** and FIG. **9** are energy band structure diagrams of corresponding semiconductor devices. FIG. **8** corresponds to the situation in which the adsorptive element In composition in the diffusion blocking layer **2** becomes smaller along the direction of the epitaxial layer. FIG. **9** corresponds to the situation in which the composition of the adsorptive element In in the diffusion blocking layer **2** remains unchanged.
(44) The diffusion blocking layer **2** is provided with an adsorptive element that adsorbs the diffusion element, thereby effectively blocking the diffusion of the diffusion element to the channel layer **3** from the buffer layer **1**. In addition, the stress release of the diffusion blocking layer **2** is avoided by setting changes in the composition of the adsorptive element in the diffusion blocking layer **2**.
(45) The above are only preferred embodiments of the present application and are not used to limit the protection scope of the present application. Any modification, equivalent replacement,

improvement, etc. made within the spirit and principle of this application shall be included in the protection scope of this application.

Claims

1. A semiconductor structure, including: a buffer layer including a diffusion element; a diffusion blocking layer formed on the buffer layer, the diffusion blocking layer including an adsorptive element; and a channel layer formed on the diffusion blocking layer; wherein a composition of the adsorptive element in the diffusion blocking layer decreases along an epitaxial growth direction of the diffusion blocking layer.
2. The semiconductor structure according to claim 1, wherein the diffusion blocking layer includes a III-V compound, and a group III element in the III-V compound is the adsorptive element.
3. The semiconductor structure according to claim 2, wherein the III-V compound includes a compound of In.
4. The semiconductor structure according to claim 3, wherein the compound of In includes InGaN.
5. The semiconductor structure according to claim 3, wherein the compound of In includes AlInGaN, and an Al composition is less than an In composition.
6. The semiconductor structure according to claim 1, wherein the composition of the adsorptive element in the diffusion blocking layer decreases in a stepwise period along the epitaxial growth direction of the diffusion blocking layer.
7. The semiconductor structure according to claim 1, wherein the composition of the adsorptive element in the diffusion blocking layer decreases in a non-periodical manner along the epitaxial growth direction of the diffusion blocking layer.
8. The semiconductor structure according to claim 1, wherein the composition of the adsorptive element in the diffusion blocking layer decreases linearly or non-linearly along the epitaxial growth direction of the diffusion blocking layer.
9. The semiconductor structure according to claim 1, wherein the diffusion element includes a metal element.
10. A preparing method for a semiconductor structure, comprising: forming a buffer layer including a diffusion element; forming a diffusion blocking layer on the buffer layer, the diffusion blocking layer including an adsorptive element; and forming a channel layer on the diffusion blocking layer; wherein a composition of the adsorptive element in the diffusion blocking layer decreases along an epitaxial growth direction of the diffusion blocking layer.
11. The method according to claim 10, wherein the diffusion blocking layer includes a III-V compound, and a group III element in the III-V compound is the adsorptive element.
12. The method according to claim 11, wherein the III-V compound includes a compound of In.
13. The method according to claim 12, wherein the compound of In includes InGaN.
14. The method according to claim 12, wherein the In compound comprises AlInGaN, and an Al composition is less than an In composition.
15. The method according to claim 10, wherein the composition of the adsorptive element in the diffusion blocking layer decreases in a stepwise period or in a non-periodical manner along the epitaxial growth direction of the diffusion blocking layer.
16. The method according to claim 10, wherein the composition of the adsorptive element in the diffusion blocking layer decreases linearly or non-linearly along the epitaxial growth direction of the diffusion blocking layer.
17. The method according to claim 10, wherein the diffusion element includes a metal element.
18. The method according to claim 10, wherein a formation temperature of the diffusion blocking layer does not exceed 900° C.