United States Patent	12388446
Kind Code	B2
Date of Patent	August 12, 2025
Inventor(s)	Choi; Woo Sick

Memory system and memory controller

Abstract

Embodiments of the present disclosure relate to a memory system and a memory controller, in which data input/output terminals in different data input/output terminal groups corresponding to different channels may be arranged adjacent to each other, thereby preventing skew of a signal occurring during data input/output operations and interference between different signals and reducing the cost required for implementing the memory system.

Inventors:	**Choi; Woo Sick (Seoul, KR)**
Applicant:	**SK hynix Inc.** (Gyeonggi-do, KR)
Family ID:	**1000008748492**
Assignee:	**SK hynix Inc. (Gyeonggi-do, KR)**
Appl. No.:	**17/941801**
Filed:	**September 09, 2022**

Prior Publication Data

Document Identifier	Publication Date
US 20230006673 A1	Jan. 05, 2023

Foreign Application Priority Data

KR	10-2019-0171464	Dec. 20, 2019

Related U.S. Application Data

continuation-in-part parent-doc US 16884631 20200527 US 11474740 child-doc US 17941801

Publication Classification

References Cited

U.S. PATENT DOCUMENTS

Patent No.	Issued Date	Patentee Name	U.S. Cl.	CPC
2005/0005184	12/2004	Lindt	713/500	G11C 29/50012
2014/0312930	12/2013	Lee	N/A	N/A
2019/0121696	12/2018	Chen et al.	N/A	N/A
2019/0355407	12/2018	Lee et al.	N/A	N/A

FOREIGN PATENT DOCUMENTS

Patent No.	Application Date	Country	CPC
10-2014-0017034	12/2013	KR	N/A
10-2014-0126145	12/2013	KR	N/A
10-2017-0068719	12/2016	KR	N/A
10-2018-0008951	12/2017	KR	N/A

OTHER PUBLICATIONS

Office Action for the U.S. Appl. No. 16/884,631 issued by the USPTO on Aug. 4, 2021. cited by applicant

---

Background/Summary

CROSS REFERENCE TO RELATED APPLICATION (1) The present application is a continuation-in-part application of U.S. patent application Ser. No. 16/884,631 filed on May 27, 2020, which claims priority under 35 U.S.C. 119(a) to Korean patent application number 10-2019-0171464, filed on Dec. 20, 2019. The entire disclosure of each of the foregoing applications is incorporated herein by reference in its entirety.

BACKGROUND
1. Field of the Invention
(1) Embodiments of the present disclosure relate to a memory system and a memory controller.
2. Description of the Prior Art
(2) A memory system, e.g., a storage device, stores data on the basis of a request from a host, such

as a computer, a mobile terminal (for example, a smartphone or a tablet), or any of various other electronic devices. The memory system may be a device configured to store data in a magnetic disk such as a hard disk drive (HDD), or a device configured to store data in a nonvolatile memory such as a solid state drive (SSD), a universal flash storage device (UFS), or an embedded MMC (eMMC) device.

(3) The memory system may further include a memory controller for controlling the memory device. The memory controller may receive a command input from the host and on the basis of the received command, may execute or control operations for reading, writing, or erasing data in a volatile memory or a nonvolatile memory included in the memory system. The memory controller may drive firmware for performing a logical operation for executing or controlling such operations.

(4) When the memory system reads or writes data at high speed, skew may occur in a signal transmitted through a signal line connected to a terminal through which data is input/output in the memory system. In addition, there is a possibility that interference between signals transmitted through different signal lines occurs.

SUMMARY

(5) Embodiments of the present disclosure may provide a memory system and a memory controller which can prevent skew of a signal occurring during data input/output operations and interference between different signals.

(6) In one aspect, embodiments of the present disclosure may provide a memory system including a plurality of memory dies and a memory controller that controls the plurality of memory dies.

(7) The memory controller may include a physical interface circuit including a plurality of data input/output terminals. The data input/output terminal is a path through which data for N channels (N is a natural number of two or more) is input/output.

(8) K data input/output terminals (K is a natural number of two or more) in a first data input/output terminal group among the plurality of data input/output terminals may correspond to a first channel of the N channels.

(9) K data input/output terminals in a second data input/output terminal group among the plurality of data input/output terminals may correspond to a second channel of the N channels.

(10) The data input/output terminal in the first data input/output terminal group may be arranged adjacent to one or more of the data input/output terminals in the second data input/output terminal group.

(11) Each data input/output terminal is connected to one of a plurality of package terminals connected to one or more of the plurality of memory dies.

(12) A first package terminal among the package terminals corresponding to a L-th bit of the first channel (L is an integer greater than or equal to 0) is arranged adjacent to a second package terminals among the package terminals corresponding to a L-th bit of the second channel.

(13) For example, the data input/output terminal corresponding to data of an I-th bit among the K data input/output terminals in the first data input/output terminal group, and the data input/output terminal corresponding to data of an I-th bit among the K data input/output terminals in the second data input/output terminal group may be arranged adjacent to each other.

(14) In another aspect, embodiments of the present disclosure may provide a memory controller including a plurality of memory dies and a control circuit for controlling the plurality of memory dies.

(15) The control circuit may include a physical interface circuit including a plurality of data input/output terminals. The data input/output terminal is a path through which data for N channels (N is a natural number of two or more) is input/output.

(16) K data input/output terminals (K is a natural number of two or more) in a first data input/output terminal group among the plurality of data input/output terminals may correspond to a first channel of the N channels.

(17) K data input/output terminals in a second data input/output terminal group among the plurality

of data input/output terminals may correspond to a second channel of the N channels.

(18) The data input/output terminal in the first data input/output terminal group may be arranged adjacent to one or more of the data input/output terminals included in the second data input/output terminal group.

(19) Each data input/output terminal is connected to one of a plurality of package terminals connected to one or more of the plurality of memory dies.

(20) A first package terminal among the package terminals corresponding to a L-th bit of the first channel (L is an integer greater than or equal to 0) is arranged adjacent to a second package terminals among the package terminals corresponding to a L-th bit of the second channel.

(21) For example, the data input/output terminal corresponding to data of an I-th bit among the K data input/output terminals in the first data input/output terminal group, and the data input/output terminal corresponding to data of an I-th bit among the K data input/output terminals in the second data input/output terminal group may be arranged adjacent to each other.

(22) In another aspect, embodiments of the present disclosure may provide a system including master and slave circuits each including N groups each having K terminals.

(23) The master and slave circuits communicate with each other through the terminals transferring signals of N channels each having a bandwidth of K bits. The N groups respectively correspond to the N channels. The K terminals respectively correspond to the K bits.

(24) The K terminals within each of the N groups are sequentially disposed at each of the master and slave circuits.

(25) The K terminals of the same sequence within the respective N groups are alternately disposed at each of the master and slave circuits.

(26) In another aspect, embodiments of the present disclosure may provide a system including master and slave circuits each including N groups each having K terminals.

(27) The master and slave circuits communicate with each other through the terminals transferring signals of N channels each having a bandwidth of K bits. The N groups respectively correspond to the N channels. The K terminals respectively correspond to the K bits.

(28) Arrangements of the terminals within the respective master and slave circuits are the same as each other.

(29) According to embodiments of the present disclosure, it is possible to prevent skew of a signal occurring during data input/output operation and interference between different signals.

(30) In addition, according to embodiments of the present disclosure, it is possible to reduce the cost of implementing a memory system.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) The above and other aspects, features and advantages of the present disclosure will be more apparent from the following detailed description taken in conjunction with the accompanying drawings.

(2) FIG. **1** is a schematic diagram illustrating a configuration of a memory system according to an embodiment of the present disclosure.

(3) FIG. **2** is a block diagram schematically illustrating a memory device according to an embodiment of the present disclosure.

(4) FIG. **3** is a diagram schematically illustrating a memory block of a memory device according to an embodiment of the present disclosure.

(5) FIG. **4** is a diagram illustrating the structure of word lines and bit lines of a memory device according to an embodiment of the present disclosure.

(6) FIG. **5** is a schematic diagram illustrating a structure of a memory system according to an

embodiment of the present disclosure.

(7) FIG. **6** is a diagram illustrating an example of a correspondence relationship between a channel and a data input/output terminal in a memory system according to an embodiment of the present disclosure.

(8) FIG. **7** is a diagram illustrating an example in which a data input/output terminal is arranged in a memory system according to an embodiment of the present disclosure.

(9) FIG. **8** is a diagram illustrating an example of a configuration of a signal line between a data input/output terminal and a package terminal in FIG. **7**.

(10) FIG. **9** is a diagram illustrating another example in which a data input/output terminal is arranged in a memory system according to an embodiment of the present disclosure.

(11) FIG. **10** is a diagram illustrating an example of a configuration of a signal line between a data input/output terminal and a package terminal in FIG. **9**.

(12) FIG. **11** is a diagram illustrating an example in which data is transmitted to a memory die through a first channel, such as that in FIG. **10**.

(13) FIG. **12** is a diagram illustrating an example in which data is transmitted to a memory die through a second channel, such as that in FIG. **10**.

(14) FIG. **13** is a diagram illustrating an example of each of a first memory die group and a second memory die group.

(15) FIG. **14** is a diagram illustrating a configuration of a computing system according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

(16) Hereinafter, embodiments of the present disclosure are described in detail with reference to the accompanying drawings. Throughout the specification, reference to "an embodiment," "another embodiment" or the like is not necessarily to only one embodiment, and different references to any such phrase are not necessarily to the same embodiment(s).

(17) FIG. **1** is a schematic diagram illustrating a configuration of a memory system **100** according to an embodiment of the present disclosure.

(18) Referring to FIG. **1**, the memory system **100** may include a memory device **110** configured to store data, and a memory controller **120** configured to control the memory device **110**.

(19) The memory device **110** may include multiple memory blocks. The memory device **110** may be configured to operate in response to control signals received from the memory controller **120**. Operations of the memory device **110** may include, for example, a read operation, a program operation (also referred to as a "write operation"), an erasure operation, and the like.

(20) The memory device **110** may include a memory cell array including multiple memory cells (also simply referred to as "cells") configured to store data. The memory cell array may exist inside a memory block.

(21) For example, the memory device **110** may be implemented as any of various types of memories, such as a double data rate synchronous dynamic random access memory (DDR SDRAM), a low power double data rate4 (LPDDR4) SDRAM, a graphics double data rate (GDDR) SDRAM, a low power DDR (LPDDR), a rambus dynamic random access memory (RDRAM), a NAND flash memory, a vertical NAND flash memory, a NOR flash memory, a resistive random access memory (RRAM), a phase-change memory (PRAM), a magnetoresistive random access memory (MRAM), a ferroelectric random access memory (FRAM), or a spin transfer torque random access memory (STT-RAM).

(22) The memory device **110** may be implemented in a three-dimensional array structure. Embodiments of the present disclosure are applicable not only to a flash memory device having an electric charge storage layer configured as a conductive floating gate, but also to a flash memory device having a charge trap flash (CTF) having an electric charge storage layer configured as an insulating film.

(23) The memory device **110** may be configured to receive a command and an address from the

memory controller **120** and to access an area of the memory cell array, which is selected by the address. That is, the memory device **110** may perform an operation corresponding to the received command in a memory area of the memory device having a physical address corresponding to the received address from the controller.

(24) For example, the memory device **110** may perform a program operation, a read operation, an erasure operation, and the like. In relation thereto, during the program operation, the memory device **110** may program data in the area selected by the address. During the read operation, the memory device **110** may read data from the area selected by the address. During the erasure operation, the memory device **110** may erase data stored in the area selected by the address.

(25) The memory controller **120** may control write (program), read, erasure, and background operations with regard to the memory device **110**. The background operation may include, for example, at least one among a garbage collection operation (GC), a wear leveling (WL) operation, and a bad block management (BBM) operation.

(26) The memory controller **120** may control the operation of the memory device **110** at the request of a host. Alternatively, the memory controller **120** may control the operation of the memory device **110** without a corresponding request of the host, such as, for example, when the memory controller **120** directs the memory device **110** to perform one or more background operations.

(27) The memory controller **120** and the host may be separate devices. In another embodiment, the memory controller **120** and the host may be integrated and implemented as a single device. In the following description, the memory controller **120** and the host are separate devices.

(28) Referring to FIG. **1**, the memory controller **120** may include a memory interface **122**, a control circuit **123**, and a host interface **121**.

(29) The host interface **121** may be configured to provide an interface for communication with the host.

(30) When receiving a command from the host (HOST), the control circuit **123** may receive the command through the host interface **121** and may perform an operation of processing the received command.

(31) The memory interface **122** may be connected to the memory device **110** to provide an interface for communication with the memory device **110**. That is, the memory interface **122** may be configured to provide the memory device **110** and the memory controller **120** with an interface in response to a control of the control circuit **123**.

(32) The control circuit **123** may be configured to control the operation of the memory device **110** by performing operations for overall control of the memory controller **120**. For example, the control circuit **123** may include a processor **124** and a working memory **125**. The control circuit **123** may further include an error detection/correction circuit (ECC circuit) **126** and the like.

(33) The processor **124** may control the overall operation of the memory controller **120**. The processor **124** may perform a logical operation. The processor **124** may communicate with the host through the host interface **121**. The processor **124** may communicate with the memory device **110** through the memory interface **122**.

(34) The processor **124** may perform a function of a flash translation layer (FTL). The processor **124** may translate a logical block address (LBA) provided by the host into a physical block address (PBA) through the FTL. The FTL may receive the LBA and translate the LBA into the PBA by using a mapping table.

(35) There are various address mapping methods which may be employed by the FTL, according to the mapping unit. Typical address mapping methods include a page mapping method, a block mapping method, and a hybrid mapping method.

(36) The processor **124** may be configured to randomize data received from the host. For example, the processor **124** may randomize data received from the host by using a randomizing seed. The randomized data is provided to the memory device **110** as data to be stored, and is programmed in the memory cell array.

(37) The processor **124** may be configured to derandomize data received from the memory device **110** during a read operation. For example, the processor **124** may derandomize data received from the memory device **110** by using a derandomizing seed. The derandomized data may be output to the host.

(38) The processor **124** may execute firmware (FW) so as to control the operation of the memory controller **120**. In other words, the processor **124** may control the overall operation of the memory controller **120** and, in order to perform a logical operation, may execute (drive) firmware loaded into the working memory **125** during booting.

(39) The firmware refers to a program executed inside the memory system **100**, and may include various functional layers.

(40) For example, the firmware may include a flash translation layer (FTL) configured to translate between a logical address that the host requests the memory system **100** to provide and a physical address of the memory device **110**, a host interface layer (HIL) configured to interpret a command that the host issues to the memory system **100** (storage device) and to deliver the same to the FTL, and/or a flash interface layer (FIL) configured to deliver a command issued by the FTL to the memory device **110**.

(41) For example, the firmware may be stored in the memory device **110**, then loaded into the working memory **125**.

(42) The working memory **125** may store firmware, program codes, commands, or pieces of data to drive the memory controller **120**. The working memory **125** may be a volatile memory, for example, a static RAM (SRAM), a dynamic RAM (DRAM), or a synchronous RAM (SDRAM).

(43) The error detection/correction circuit **126** may be configured to detect an error bit of target data by using an error correction code, and to correct the detected error bit. For example, the target data may be data stored in the working memory **125**, data retrieved from the memory device **110**, or the like.

(44) The error detection/correction circuit **126** may be implemented to decode data by using the error correction code. The error detection/correction circuit **126** may be implemented by using various code decoders. For example, a decoder that performs nonsystematic code decoding or a decoder that performs systematic code decoding may be used.

(45) For example, the error detection/correction circuit **126** may detect an error bit, sector by sector, with regard to each piece of read data. That is, each piece of read data may include multiple sectors. As used herein, a sector may refer to a data unit smaller than the read unit (page) of a flash memory. Sectors constituting each piece of read data may correspond to each other via an address.

(46) The error detection/correction circuit **126** may calculate a bit error rate (BER) and determine whether or not correction can be made sector by sector. For example, if the BER is higher than a reference value, the error detection/correction circuit **126** may determine that the corresponding sector is uncorrectable or "a fail". If the BER is lower than the reference value, the error detection/correction circuit **126** may determine that the corresponding sector is correctable or "a pass".

(47) The error detection/correction circuit **126** may perform error detection and correction operations successively with regard to all pieces of read data. When a sector included in the read data is correctable, the error detection/correction circuit **126** may omit the error detection and correction operations related to the corresponding sector with regard to the next piece of read data. After finishing error detection and correction operations with regard to all pieces of read data in this manner, the error detection/correction circuit **126** may detect one or more sectors deemed uncorrectable in the read data. The error detection/correction circuit **126** may deliver information (for example, address information) regarding the sector(s) deemed uncorrectable to the processor **124**.

(48) The bus **127** may be configured to provide a channel between the constituent elements **121**, **122**, **124**, **125**, and **126** of the memory controller **120**. The bus **127** may include, for example, a

control bus for delivering various kinds of control signals and commands, and a data bus for delivering various kinds of data.

(49) The above-mentioned constituent elements **121**, **122**, **124**, **125**, and **126** of the memory controller **120** are only provided as examples. One or more of these elements may be omitted, or two or more may be integrated into a single element. Of course, as those skilled in the art will understand, the memory controller **120** may include more components than those illustrated in FIG. **1**.

(50) Hereinafter, the memory device **110** is described in more detail with reference to FIG. **2**.

(51) FIG. **2** is a block diagram schematically illustrating a memory device **110** according to an embodiment of the present disclosure.

(52) Referring to FIG. **2**, the memory device **110** may include a memory cell array **210**, an address decoder **220**, a read/write circuit **230**, control logic **240**, and a voltage generation circuit **250**.

(53) The memory cell array **210** may include multiple memory blocks BLK**1**-BLKz (z is a natural number equal to or larger than 2).

(54) In the multiple memory blocks BLK**1**-BLKz, multiple word lines WL and multiple bit lines BL may be disposed in an intersecting arrangement, and multiple memory cells MC may be formed at the respective intersections.

(55) The multiple memory blocks BLK**1**-BLKz may be connected to the address decoder **220** through the multiple word lines WL. The multiple memory blocks BLK**1**-BLKz may be connected to the read/write circuit **230** through the multiple bit lines BL.

(56) Each of the multiple memory blocks BLK**1**-BLKz may include multiple memory cells. For example, the multiple memory cells are nonvolatile memory cells, which may have a vertical channel structure.

(57) The memory cell array **210** may be configured as a memory cell array having a two-dimensional structure and, in some cases, may be configured as a memory cell array having a three-dimensional structure.

(58) Each of the multiple memory cells in the memory cell array **210** may store at least one bit of data. For example, each of the multiple memory cells in the memory cell array **210** may be a single-level cell (SLC) configured to store one bit of data, a multi-level cell (MLC) configured to store two bits of data, or a triple-level cell (TLC) configured to store three bits of data. Higher storage capacity memory cells may also be used. To that end, each of the multiple memory cells in the memory cell array **210** may be a quad-level cell (QLC) configured to store four bits of data or a memory cell configured to store at least five bits of data.

(59) Referring to FIG. **2**, the address decoder **220**, the read/write circuit **230**, the control logic **240**, and the voltage generation circuit **250** may collectively operate as a peripheral circuit configured to drive the memory cell array **210**.

(60) The address decoder **220** may be connected to the memory cell array **210** through the multiple word lines WL.

(61) The address decoder **220** may be configured to operate in response to a control of the control logic **240**.

(62) The address decoder **220** may receive addresses through an input/output buffer inside the memory device **110**. The address decoder **220** may be configured to decode a block address among the received addresses. The address decoder **220** may select at least one memory block according to the decoded block address.

(63) The address decoder **220** may receive a read voltage Vread and a pass voltage Vpass from the voltage generation circuit **250**.

(64) The address decoder **250** may apply the read voltage Vread to a selected word line WL inside a selected memory block, during an operation of applying the read voltage during a read operation, and may apply the pass voltage Vpass to the remaining non-selected word lines WL.

(65) The address decoder **220** may apply a verification voltage generated by the voltage generation

circuit **250** to a selected word line WL inside a selected memory block, during a program verification operation, and may apply the pass voltage Vpass to the remaining non-selected word lines WL.

(66) The address decoder **220** may be configured to decode a column address among the received addresses. The address decoder **220** may transmit the decoded column address to the read/write circuit **230**.

(67) The memory device **110** may perform the read operation and the program operation page by page. Addresses received when the read operation and the program operation are requested may include at least one of a block address, a row address, and a column address.

(68) The address decoder **220** may select one memory block and one word line according to the block address and the row address. The column address may be decoded by the address decoder **220** and provided to the read/write circuit **230**.

(69) The address decoder **220** may include at least one of a block decoder, a row decoder, a column decoder, and an address buffer.

(70) The read/write circuit **230** may include multiple page buffers PB. The read/write circuit **230** may operate as a "read circuit" when the memory cell array **210** performs a read operation, and may operate as a "write circuit" when the memory cell array **210** performs a write operation.

(71) The above-mentioned read/write circuit **230** is also referred to as a page buffer circuit including multiple page buffers PB, or a data register circuit. The read/write circuit **230** may include a data buffer that participates in a data processing function and, in some cases, may further include a cache buffer in charge of a caching function.

(72) The multiple page buffers PB may be connected to the memory cell array **210** through the multiple bit lines BL. In order to sense the threshold voltage Vth of the memory cells during a read operation and a program verification operation, the multiple page buffers PB may continuously supply a sensing current to the bit lines BL connected to the memory cells, may sense, through a sensing node, a change in the amount of current that flows according to the program state of a corresponding memory cell, and may latch the same as sensing data.

(73) The read/write circuit **230** may operate in response to page buffer control signals output from the control logic **240**.

(74) During a read operation, the read/write circuit **230** senses data in a memory cell, temporarily stores the retrieved data, and outputs the data DATA to the input/output buffer of the memory device **110**. In an embodiment, the read/write circuit **230** may include a column selection circuit, in addition to the page buffers PB or page registers.

(75) The control logic **240** may be connected to the address decoder **220**, the read/write circuit **230**, and the voltage generation circuit **250**. The control logic **240** may receive a command CMD and a control signal CTRL through the input/output buffer of the memory device **110**.

(76) The control logic **240** may be configured to control the overall operation of the memory device **110** in response to the control signal CTRL. The control logic **240** may output a control signal for adjusting the pre-charge potential level of sensing nodes of multiple page buffers PB.

(77) The control logic **240** may control the read/write circuit **230** to perform a read operation in the memory cell array **210**. The voltage generation circuit **250** may generate a read voltage Vread and a pass voltage Vpass, which are used during the read operation, in response to a voltage generation circuit control signal output from the control logic **240**.

(78) FIG. **3** is a diagram schematically illustrating a memory block BLK of a memory device **110** according to an embodiment of the present disclosure.

(79) Referring to FIG. **3**, a memory block BLK included in the memory device **110** may be arranged and configured in such direction that multiple pages PG and multiple strings TTR intersect.

(80) The multiple pages PG correspond to multiple word lines WL, and the multiple strings STR correspond to multiple bit lines BL.

(81) In the memory block BLK, multiple word lines WL and multiple bit lines BL may be arranged to intersect. For example, each of the multiple word lines WL may be arranged in the row direction, and each of the multiple bit lines BL may be arranged in the column direction. As another example, each of the multiple word lines WL may be arranged in the column direction, and each of the multiple bit lines BL may be arranged in the row direction.

(82) The multiple word lines WL and the multiple bit lines BL may intersect with each other, thereby defining multiple memory cells MC. Each memory cell MC may have a transistor TR arranged therein.

(83) For example, the transistor TR arranged in each memory cell MC may include a drain, a source, and a gate. The drain (or source) of the transistor TR may be connected to the corresponding bit line BL directly or via another transistor TR. The source (or drain) of the transistor TR may be connected to the source line (which may be the ground) directly or via another transistor TR. The gate of the transistor TR may include a floating gate (FG) surrounded by an insulator, and a control gate (CG) to which a gate voltage is applied from a word line WL.

(84) In each of the multiple memory blocks BLK**1**-BLKz, a first selection line (also referred to as a source selection line or a drain selection line) may be additionally arranged outside the first outermost word line, which is closer to the read/write circuit **230** among two outermost word lines, and a second selection line (also referred to as a drain selection line or a source selection line) may be additionally arranged outside the other second outermost word line.

(85) In some cases, at least one dummy word line may be additionally arranged between the first outermost word line and the first selection line. In addition, at least one dummy word line may be additionally arranged between the second outermost word line and the second selection line.

(86) In the case of a memory block structure as illustrated in FIG. **3**, a read operation and a program operation (write operation) may be performed page by page, and an erasure operation may be performed memory block by memory block.

(87) FIG. **4** is a diagram illustrating a structure of word lines WL and bit lines BL of a memory device **110** according to an embodiment of the present disclosure.

(88) Referring to FIG. **4**, the memory device **110** has a core area in which memory cells MC are concentrated, and an auxiliary area which corresponds to the remaining (i.e., non-core) area. The auxiliary area supports the operations of the memory cell array **210**.

(89) The core area may include pages PG and strings STR. In the core area, multiple word lines WL**1**-WL**9** and multiple bit lines BL are arranged to intersect.

(90) The word lines WL**1**-WL**9** may be connected to a row decoder **410**. The bit lines BL may be connected to a column decoder **420**. A data register **430**, which corresponds to the read/write circuit **230** of FIG. **2**, may exist between the multiple bit lines BL and the column decoder **420**.

(91) The multiple word lines WL**1**-WL**9** may correspond to multiple pages PG.

(92) For example, each of the multiple word lines WL**1**-WL**9** may correspond to one page PG as illustrated in FIG. **4**. In contrast, when each of the multiple word lines WL**1**-WL**9** has a large size, each of the multiple word lines WL**1**-WL**9** may correspond to at least two (for example, two or four) pages PG. Each page PG is the smallest unit in connection with conducting a program operation and a read operation, and all memory cells MC within the same page PG may perform simultaneous operations when conducting a program operation and a read operation.

(93) The multiple bit lines BL may be connected to the column decoder **420** while being distinguished between odd-numbered bit lines BL and even-numbered bit lines BL.

(94) For accessing a memory cell MC, the address may be entered to the core area first through the input/output end and then through the row decoder **410** and the column decoder **420** such that a corresponding target memory cell can be designated. As used herein, designating a target memory cell refers to accessing one of the memory cells MC at the sites of intersection between the word lines WL**1**-WL**9** connected to the row decoder **410** and the bit lines BL connected to the column decoder **420**, for programming data therein or for reading programmed data therefrom.

(95) Pages PG in a first direction (for example, X-axis direction) are bound by a commonly used line referred to as a word line WL, and strings STR in a second direction (for example, Y-axis direction) are bound (connected) by a common line referred to as a bit line BL. As used herein, being commonly bound refers to being structurally connected by the same material and simultaneously receiving the same voltage during voltage application. The voltage applied to a memory cell MC in positions among memory cells MC connected in series may differ slightly, due to the voltage drop across the preceding memory cell MC.

(96) The data register **430** plays an integral role because all data processing by the memory device **110**, including program and read operations, occurs via the data register **430**. If data processing by the data register **430** is delayed, all the other areas need to wait until the data register **430** finishes the data processing. In addition, degradation of performance of the data register **430** may degrade the overall performance of the memory device **110**.

(97) Referring to the example illustrated in FIG. **4**, in one string STR, multiple transistors TR**1**-TR**9** connected to multiple word lines WL**1**-WL**9** may exist. The areas in which the multiple transistor TR**1**-TR**9** exist correspond to memory cells MC. As used herein, the multiple transistors TR**1**-TR**9** refer to transistors including control gates CG and floating gates FG.

(98) The multiple word lines WL**1**-WL**9** include two outermost word lines WL**1** and WL**9**. A first selection line DSL may be additionally arranged outside the first outermost word line WL**1**, which is closer to the data register **430** in terms of the signal path among the two outermost word lines WL**1** and WL**9**, and a second selection line SSL may be additionally arranged outside the other second outermost word line WL**9**.

(99) The first selection transistor D-TR, which is controlled to turn on/off by the first selection line DSL, has a gate electrode connected to the first selection line DSL, but includes no floating gate FG. The second selection transistor S-TR, which is controlled to turn on/off by the second selection line SSL, has a gate electrode connected to the second selection line SSL, but includes no floating gate FG.

(100) The first selection transistor D-TR plays the role of a switch that turns on or off the connection between the corresponding string STR and the data register **430**. The second selection transistor S-TR plays the role of a switch that turns on or off the connection between the corresponding string STR and the source line SL. That is, the first selection transistor D-TR and the second selection transistor S-TR play the role of gatekeepers which are positioned on both ends of the corresponding string STR and deliver/block signals.

(101) The memory system **100** needs to fill the target memory cell MC of the bit line BL to be programmed with electrons during a program operation. Accordingly, the memory system **100** applies a turn-on voltage Vcc to the gate electrode of the first selection transistor D-TR, thereby turning on the first selection transistor D-TR, and applies a turn-off voltage (for example, 0V) to the gate electrode of the second selection transistor S-TR, thereby turning off the second selection transistor S-TR.

(102) The memory system **100** turns on both the first selection transistor D-TR and the second selection transistor S-TR during a read operation or a verification operation. Accordingly, an electric current may flow through the corresponding string STR and drain to the source line SL, which corresponds to the ground, such that the voltage level of the bit line BL can be measured. However, during a read operation, there may be a time difference in on/off timing between the first selection transistor D-TR and the second selection transistor S-TR.

(103) The memory system **100** may supply a voltage (for example, +20V) to the substrate through a source line SL during an erasure operation. The memory system **100** floats both the first selection transistor D-TR and the second selection transistor S-TR during an erasure operation, thereby generating an infinite resistance. As a result, the role of the first selection transistor D-TR and that of the second selection transistor S-TR may be removed, and electrons may operate only between the floating gate FG and the substrate due to the potential difference.

(104) FIG. **5** is a diagram illustrating a schematic structure of the memory system **100** according to an embodiment of the present disclosure.

(105) Referring to FIG. **5**, the memory controller **120** may include a physical interface circuit PHY_INF_BLK. The physical interface circuit PHY_INF_BLK may include a plurality of data input/output terminals IO_TERM. The physical interface circuit PHY_INF_BLK may be referred to as physical interface block.

(106) The data input/output terminals IO_TERM are paths through which data for N channels CH_**1** to CH_N is transferred. For example, the data input/output terminal IO_TERM may be a pin.

(107) The channel refers to a path for data communication between the memory controller **120** and a plurality of memory dies DIE included in the memory system **100**. The memory controller **120** may transmit and receive data through different channels in parallel.

(108) Data may be transferred to and from the plurality of memory dies DIE included in the memory system **100**. The plurality of memory dies DIE may be located on a package included in the memory system **100**.

(109) The physical interface circuit PHY_INF_BLK may correspond to the plurality of channels CH_**1** to CH_N, where n is a natural number of 2 or more.

(110) In embodiments of the present disclosure, the value of N may be variously determined. For example, the value of N may be determined to be 2.sup.m (m is a natural number). This is because the number of channels that can be represented using m bits is 2.sup.m. That is, N=2, 4, 8, 16 . . . .

(111) Hereinafter, a correspondence relationship between the N channels CH_**1** to CH_N and the plurality of data input/output terminals IO_TERM is described by way of example.

(112) FIG. **6** is a diagram illustrating an example of a correspondence relationship between a channel and a data input/output terminal in the memory system **100** according to an embodiment of the present disclosure.

(113) Referring to FIG. **6**, K data input/output terminals in a first data input/output terminal group IO_TERM_GRP_**1**, among the plurality of data input/output terminals IO_TERM in the physical interface circuit PHY_INF_BLK, correspond to a first channel CH_**1** of the N channels. In this case, that the data input/output terminal corresponds to the first channel CH_**1** means that data for the first channel CH_**1** can be transferred through the corresponding data input/output terminal.

(114) K data input/output terminals in a second data input/output terminal group IO_TERM_GRP_**2**, among the plurality of data input/output terminals IO_TERM in the physical interface circuit PHY_INF_BLK, correspond to a second channel CH_**2** of the N channels. That the data input/output terminal corresponds to the second channel CH_**2** means that data for the second channel CH_**2** can be transferred through the corresponding data input/output terminal. CH_**2** is different than CH_**1**.

(115) K is a natural number of 2 or more.

(116) Hereinafter, a case where K=8, that is, a case where eight data input/output terminals correspond to the first channel CH_**1** and the second channel CH_**2**, respectively, is described by way of example.

(117) FIG. **7** is a diagram illustrating an example in which the data input/output terminal IO_TERM is arranged in the memory system **100** according to an embodiment of the present disclosure.

(118) Referring to FIG. **7**, the data input/output terminals in the first data input/output terminal group IO_TERM_GRP_**1**, among the plurality of data input/output terminals IO_TERM in the physical interface circuit PHY_INF_BLK, may be arranged adjacent to each other. In addition, the data input/output terminals included in the second data input/output terminal group IO_TERM_GRP_**2** may be arranged adjacent to each other.

(119) The data input/output terminal IO_TERM may be connected to a package terminal PKG_TERM inside the memory system **100**.

(120) The package terminal PKG_TERM is a terminal located on a package included in the

memory system **100** and may be connected to one or more of the plurality of memory dies DIE inside the memory system **100**. The package terminal PKG_TERM may be a package ball.

(121) The arrangement of the package terminals PKG_TERM inside the memory system **100** may be determined as follows. First, a package terminal CH_**1**_BIT_**0** corresponding to a 0-th bit of the first channel CH_**1** and a package terminal CH_**2**_BIT_**0** corresponding to a 0-th bit of the second channel CH_**2** may be arranged adjacent to each other. A package terminal CH_**1**_BIT_**1** corresponding to a first bit of the first channel CH_**1** and a package terminal CH_**2**_BIT_**1** corresponding to a first bit of the second channel CH_**2** may be arranged adjacent to each other.

(122) A package terminal CH_**1**_BIT 2 corresponding to a second bit of the first channel CH_**1** and a package terminal CH_**2**_BIT_**2** corresponding to a second bit of the second channel CH_**2** may be arranged adjacent to each other. In this pattern, a package terminal CH_**1**_BIT_**7** corresponding to a seventh bit of the first channel CH_**1** and a package terminal CH_**2**_BIT_**7** corresponding to a seventh bit of the second channel CH_**2** may be arranged adjacent to each other.

(123) In order for data to be transferred through the data input/output terminal IO_TERM, the data input/output terminal IO_TERM and the package terminal PKG_TERM are required to be connected to each other. In order to connect the data input/output terminal IO_TERM to the package terminal PKG_TERM, a pad and a signal line may be disposed between the data input/output terminal IO_TERM and the package terminal PKG_TERM.

(124) Hereinafter, an example of a signal line between the data input/output terminal IO_TERM and the package terminal PKG_TERM for connecting the data input/output terminal IO_TERM and the package terminal PKG_TERM is described.

(125) FIG. **8** is a diagram illustrating an example of a configuration of a signal line between the data input/output terminal IO_TERM and the package terminal PKG_TERM in FIG. **7**.

(126) Referring to FIG. **8**, there is an intersection point {circle around (1)} between a signal line connecting a data input/output terminal corresponding to a first bit of the first channel CH_**1** and a package terminal CH_**1**_BIT_**1** corresponding to the first bit of the first channel CH_**1** and a signal line connecting a data input/output terminal corresponding to a 0-th bit of the second channel CH_**2** and a package terminal CH_**2**_BIT_**0** corresponding to the 0-th bit of the second channel CH_**2**.

(127) In addition, there is an intersection point {circle around (2)} between a signal line connecting a data input/output terminal corresponding to a second bit of the first channel CH_**1** and a package terminal CH_**1**_BIT_**2** corresponding to the second bit of the first channel CH_**1** and the signal line connecting the data input/output terminal corresponding to the 0-th bit of the second channel CH_**2** and the package terminal CH_**2**_BIT_**0** corresponding to the 0-th bit of the second channel CH_**2**.

(128) In this manner, at a point where different signal lines intersect, skew may occur in a signal transmitted through the signal line or interference may occur between signals transmitted through each signal line. Short may also occur at the point where different signal lines intersect with each other.

(129) Therefore, in order to prevent such a problem, a separate package layer may be added at the intersection point of the signal lines. However, this solution may increase the cost of implementing the memory system **100**.

(130) In accordance with an embodiment of the present invention, the data input/output terminals IO_TERM and the package terminals PKG_TERM may be arranged to prevent the signal lines connecting the data input/output terminal IO_TERM and the package terminal PKG_TERM from intersecting with each other.

(131) FIG. **9** is a diagram illustrating another example in which the data input/output terminal IO_TERM is arranged in the memory system **100** according to an embodiment of the present disclosure.

(132) Among the data input/output terminals IO_TERM in the physical interface circuit PHY_INF_BLK, the data input/output terminals in the first data input/output terminal group IO_TERM_GRP_**1** may be arranged adjacent to one or more of the data input/output terminals in

the second data input/output terminal group IO_TERM_GRP_**2**.

(133) Referring to 9, the data input/output terminal in the second data input/output terminal group IO_TERM_GRP_**2** may be arranged next to the data input/output terminal in the first data input/output terminal group IO_TERM_GRP_**1**, and the data input/output terminal in the first data input/output terminal group IO_TERM_GRP_**1** may be arranged next to the data input/output terminal in the second data input/output terminal group IO_TERM_GRP_**2**.

(134) Meanwhile, the physical interface circuit PHY_INF_BLK may further include an interface port INT_PORT connected to the data input/output terminals IO_TERM. Data input to the data input/output terminals IO_TERM and data output from the data input/output terminals IO_TERM may pass through the interface port INT_PORT.

(135) In this case, a plurality of signal conversion circuits SCC may exist between the interface port INT_PORT and the data input/output terminals IO_TERM optionally. That is, Data input to the data input/output terminals IO_TERM and data output from the data input/output terminals IO_TERM may pass through the interface port INT_PORT via the signal conversion circuits SCC.

(136) In order for the memory controller **120** to communicate with the plurality of memory dies DIE through the physical interface circuit PHY_INF_BLK, signals transmitted from the physical interface circuit PHY_INF_BLK need to be converted into Tx or Rx signals. The signal conversion circuits SCC may convert data input to the data input/output terminals IO_TERMS or data output from the data input/output terminals IO_TERM into Tx or Rx signals, so that a signal may be smoothly transmitted from the memory controller **120** to the plurality of memory dies DIE or from the plurality of memory dies DIE to the memory controller **120**.

(137) On the other hand, data input to the data input/output terminals IO_TERM and data output from the plurality of data input/output terminals IO_TERM may be directly passed through the interface port INT_PORT without the signal conversion circuits SCC.

(138) For example, the physical interface circuit PHY_INF_BLK may receive data for a channel from the memory controller **120** through the interface port INT_PORT, and may transmit the received data to the data input/output terminal corresponding to the channel. And the physical interface circuit PHY_INF_BLK may transmit data received from the data input/output terminal corresponding to a channel to the memory controller **120** through the interface port INT_PORT.

(139) The interface port INT_PORT and the data input/output terminals IO_TERM included in the physical interface circuit PHY_INF_BLK may be electrically connected to each other through signal lines. In this case, the length of the signal line between the interface port INT_PORT and each of the data input/output terminals IO_TERM may be different for each data input/output terminal. In this case, the timing at which data is transmitted between the interface port INT_PORT and the data input/output terminals IO_TERM may be different for each data input/output terminal, and thus skew may occur.

(140) Therefore, the signal line connecting the interface port INT_PORT and the data input/output terminals IO_TERM may be configured such that the time for data transfer between the interface port INT_PORT and each data input/output terminal is included within a reference time period. In this case, the reference time point may be set based on a time X during which data is transmitted through the longest signal line among the signal lines connecting the interface port INT_PORT and the data input/output terminals. For example, the reference time period may be set from X−α to X+α (α is an arbitrary time value, e.g. 20˜100 ps).

(141) For example, in FIG. **9**, a first line LINE_**1** is the longest among the signal lines connecting the interface port INT_PORT and the data input/output terminals IO_TERM. And, among the signal lines connecting the interface port INT_PORT and the data input/output terminals IO_TERM, the second line LINE_**2** is shorter than the first line LINE_**1**.

(142) Meanwhile, when the signal conversion circuits SCC exist between the interface port INT_PORT and the data input/output terminals IO_TERM, the length of the signal lines connecting the interface port INT_PORT and the data input/output terminals IO_TERM may be determined

based on the lengths of signal lines connecting the interface port INT_PORT and the signal conversion circuits SCC. This is because the lengths of the signal lines connecting the data input/output terminals IO_TERM and the signal conversion circuits SCC are uniform.

(143) In this case, the reference time period may be set based on the time data is transmitted from the interface port INT_PORT to data input/output terminal through the first line LINE_**1**. In addition, one or more elements for delaying the data transmission time may be applied to the second line LINE_**2** so that the data transmission time through the second line LINE_**2** is included within the reference time period.

(144) For example, one or more delay elements DE capable of delaying a data transmission time may be added to the second line LINE_**2**. The delay elements DE may be, for example, a transistor or an electronic component including a transistor (e.g. an inverter). As another example, wire included in the second line LINE_**2** may have a detour shape.

(145) Through this, the timing at which data is transmitted between the interface port INT_PORT and the data input/output terminals IO_TERM may be set as uniformly as possible.

(146) Hereinafter, a configuration of a signal line between the data input/output terminal IO_TERM and the package terminal PKG_TERM when the data input/output terminal IO_TERM is arranged as shown in FIG. **9** is described.

(147) FIG. **10** is a diagram illustrating an example of a configuration of a signal line between the data input/output terminal IO_TERM and the package terminal in FIG. **9**.

(148) Referring to FIG. **10**, a data input/output terminal corresponding to data of an I-th bit, among eight data input/output terminals in the first data input/output terminal group IO_TERM_GRP_**1**, and a data input/output terminal corresponding to data of an I-th bit among eight data input/output terminals in the second data input/output terminal group IO_TERM_GRP_**2**, may be arranged adjacent to each other. The value of I is a positive integer less than 8 (0 to 7).

(149) First, a data input/output terminal corresponding to data of a 0-th bit, among the data input/output terminals in the second data input/output terminal group IO_TERM_GRP_**2**, may be arranged after a data input/output terminal corresponding to data of a 0-th bit among the data input/output terminals in the first data input/output terminal group IO_TERM_GRP_**1**.

(150) Next, a data input/output terminal corresponding to data of a first bit, among the data input/output terminals in the second data input/output terminal group IO_TERM_GRP_**2**, may be arranged after a data input/output terminal corresponding to data of a first bit, among the data input/output terminals in the first data input/output terminal group IO_TERM_GRP_**1**.

(151) In this pattern, a data input/output terminal corresponding to data of a seventh bit, among the data input/output terminals in the second data input/output terminal group IO_TERM_GRP_**2**, may be arranged after a data input/output terminal corresponding to data of a seventh bit, among the data input/output terminals in the first data input/output terminal group IO_TERM_GRP_**1**.

(152) When the data input/output terminal IO_TERM and the package terminal PKG_TERM are arranged as described above, there is no point where signal lines between the data input/output terminal IO_TERM and the package terminal PKG_TERM intersect with each other. Unlike FIG. **8**, this is because a pattern of the order in which the data input/output terminals IO_TERM are arranged inside the physical interface circuit PHY_INF_BLK and a pattern of the order in which the package terminals PKG_TERM are arranged according to channels and bits coincide with each other. That is, the signal lines between the data input/output terminals IO_TERM and the package terminals PKG_TERM may be configured not to cross one another.

(153) Thus, it is possible to prevent a situation in which skew of a signal transmitted through each signal line or interference between different signals occurs. Therefore, it is not necessary to add a separate package layer to prevent a problem caused by different signal lines intersecting with each other as shown in FIG. **8**. As a result, the cost of implementing the memory system **100** may be reduced.

(154) Hereinafter, an example in which data is transmitted to the memory die DIE through each

channel when a signal line between the data input/output terminal IO_TERM and the package terminal PKG_TERM is arranged as shown in FIG. **10** is described.

(155) The memory controller **120** of the memory system **100** may transmit or receive data in units of K bits of a data segment through K data input/output terminals in the first data input/output terminal group IO_TERM_GRP_**1**. The memory controller **120** may transmit or receive data in units of K bits of data segment through K data input/output terminals in the second data input/output terminal group IO_TERM_GRP_**2**.

(156) FIG. **11** is a diagram illustrating an example in which data is transmitted to the memory die DIE through the first channel CH_**1** in FIG. **10**.

(157) In FIG. **11**, it is assumed that an 8-bit data segment of 0b01011011 is transmitted to the memory die DIE through the first channel CH_**1**.

(158) In this case, through a data input/output terminal corresponding to a 0-th bit of the first channel CH_**1** in which a bit value corresponding to a 0-th bit of 0b01011011 is 1, the 8-bit data segment 0b01011011 may be transmitted to a package terminal CH_**1**_BIT_**0** corresponding to the 0-th bit of the first channel CH_**1**.

(159) At the same time, through a data input/output terminal corresponding to a first bit of the first channel CH_**1** in which a bit value corresponding to a first bit of 0b01011011 is 1, the 8-bit data segment 0b01011011 may be transmitted to a package terminal CH_**1**_BIT_**1** corresponding to the first bit of the first channel CH_**1**.

(160) At the same time, through a data input/output terminal corresponding to a second bit of the first channel CH_**1** in which a bit value corresponding to a second bit of 0b01011011 is 0, the 8-bit data segment 0b01011011 may be transmitted to a package terminal CH_**1**_BIT 2 corresponding to the second bit of the first channel CH_**1**.

(161) In the above-described pattern, through a data input/output terminal corresponding to a seventh bit of the first channel CH_**1** in which a bit value corresponding to a seventh bit of 0b01011011 is 0, the 8-bit data segment 0b01011011 may be transmitted to a package terminal CH_**1**_BIT_**7** corresponding to the seventh bit of the first channel CH_**1**.

(162) In this manner, each bit value of the data segment transmitted to the package terminal may be transmitted to any one of the plurality of memory dies DIE.

(163) FIG. **12** is a diagram illustrating an example in which data is transmitted to the memory die DIE through the second channel CH_**2** in FIG. **10**.

(164) In FIG. **12**, it is assumed that an 8-bit data segment of 0b10100010 is transmitted to the memory die DIE through the second channel CH_**2**.

(165) In this case, through a data input/output terminal corresponding to a 0-th bit of the second channel CH_**2** in which a bit value corresponding to a 0-th bit of 0b10100010 is 0, the 8-bit data segment 0b10100010 may be transmitted to a package terminal CH_**2**_BIT 0 corresponding to the 0-th bit of the second channel CH_**2**.

(166) At the same time, through a data input/output terminal corresponding to a first bit of the second channel CH_**2** in which a bit value corresponding to a first bit of 0b10100010 is 1, the 8-bit data segment 0b10100010 may be transmitted to a package terminal CH_**2**_BIT 1 corresponding to the first bit of the second channel CH_**2**.

(167) At the same time, through a data input/output terminal corresponding to a second bit of the second channel CH_**2** in which a bit value corresponding to a second bit of 0b10100010 is 0, the 8-bit data segment 0b10100010 may be transmitted to a package terminal CH_**2**_BIT 2 corresponding to the second bit of the second channel CH 2.

(168) In the above-described pattern, through a data input/output terminal corresponding to a seventh bit of the second channel CH_**2** in which a bit value corresponding to a seventh bit of 0b10100010 is 1, the 8-bit data segment 0b10100010 may be transmitted to a package terminal CH_**2**_BIT_**7** corresponding to the seventh bit of the second channel CH_**2**.

(169) In this manner, each bit value of the data segment transmitted to the package terminal may be

transmitted to any one of the plurality of memory dies DIE.

(170) FIG. **13** is a diagram illustrating an example of each of a first memory die group DIE_GRP_**1** and a second memory die group DIE_GRP_**2** in FIG. **10**.

(171) Referring to FIG. **13**, a data input/output terminal in the first data input/output terminal group IO_TERM_GRP_**1** may be connected to a memory die in a first memory die group DIE_GRP_**1** among the plurality of memory dies DIE in the memory system **100**.

(172) In FIG. **13**, the data input/output terminal corresponding to a 0-th bit among the data input/output terminals in the first data input/output terminal group IO_TERM_GRP_**1** may be connected to a memory die in the first memory die group DIE_GRP_**1** through a package terminal CH_**1**_BIT_**0** corresponding to the 0-th bit of the first channel CH_**1**. In this pattern, the data input/output terminal corresponding to an I-th bit (I is a natural number of 7 or less) among the data input/output terminals in the first data input/output terminal group IO_TERM_GRP_**1** may be connected to a memory die included in the first memory die group DIE_GRP_**1** through a package terminal corresponding to the I-th bit of the first channel CH_**1**.

(173) The data input/output terminal in the second data input/output terminal group IO_TERM_GRP_**2** may be connected to the memory die in the second memory die group DIE_GRP_**2** among the plurality of memory dies DIE in the memory system **100**.

(174) In FIG. **13**, the data input/output terminal corresponding to a 0-th bit of the data input/output terminals in the second data input/output terminal group IO_TERM_GRP_**2** may be connected to a memory die in the second memory die group DIE_GRP_**2** through the package terminal CH_**2**_BIT_**0** corresponding to a 0-th bit of the second channel CH_**2**. In this pattern, the data input/output terminal corresponding to an I-th bit (I is a natural number of 7 or less) among the data input/output terminals in the second data input/output terminal group IO_TERM_GRP_**2** may be connected to a memory die in the second memory die group DIE_GRP_**2** through a package terminal corresponding to an I-th bit of the second channel CH_**2**.

(175) The above-described operation of the memory controller **120** may be controlled by the control circuit **123**, and the processor **124** may be performed in a manner in which various operations of the memory controller **120** execute (drive) programmed firmware.

(176) FIG. **14** is a diagram illustrating the configuration of a computing system **1400** according to an embodiment of the present disclosure.

(177) Referring to FIG. **14**, the computing system **1400** may include: a memory system **100** electrically connected to a system bus **1460**; a CPU **1410** configured to control the overall operation of the computing system **1400**; a RAM **1420** configured to store data and information related to operations of the computing system **1400**; a user interface/user experience (UI/UX) module **1430** configured to provide the user with a user environment; a communication module **1440** configured to communicate with an external device in a wired and/or wireless type; and a power management module **1450** configured to manage power used by the computing system **1400**.

(178) The computing system **1400** may be a personal computer (PC) or may include a mobile terminal such as a smartphone, a tablet or any of various other electronic devices.

(179) The computing system **1400** may further include a battery for supplying an operating voltage, and may further include an application chipset, a graphic-related module, a camera image processor (CIS), and a DRAM. The computer system **1400** may include other elements as those skilled in the art understand.

(180) The memory system **100** may be a device configured to store data in a magnetic disk such as a hard disk drive (HDD), or a device configured to store data in a nonvolatile memory such as a solid state drive (SSD), a universal flash storage device, or an embedded MMC (eMMC) device. The non-volatile memory may include a read only memory (ROM), a programmable ROM (PROM), an electrically programmable ROM (EPROM), an electrically erasable and programmable ROM (EEPROM), a flash memory, a phase-change RAM (PRAM), a magnetic

RAM (MRAM), a resistive RAM (RRAM), a ferroelectric RAM (FRAM), and the like. In addition, the memory system **100** may be implemented as any of various storage devices of various types, which may be mounted within various electronic devices.

(181) According to embodiments of the present disclosure described above, operation delay time of the memory system may be minimized. In addition, according to an embodiment of the present disclosure, overhead occurring in the process of calling a specific function may be minimized. Although various embodiments of the present disclosure have been illustrated and described, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as set forth in the accompanying claims. That is, the present invention encompasses all modifications and variations of any of the disclosed embodiments that fall within the scope of the claims.

Claims

1. A memory system comprising: a plurality of memory dies; and a memory controller configured to control the plurality of memory dies, wherein: the memory controller comprises a physical interface circuit including a plurality of data input/output terminals which are paths through which data for a plurality of channels is input/output and an interface port electrically connected to the plurality of data input/output terminals through a plurality of signal lines, data input to the data input/output terminals and data output from the data input/output terminals pass through the interface port, a plurality of first data input/output terminals among the plurality of data input/output terminals correspond to a first channel among the plurality of channels, a plurality of second data input/output terminals among the plurality of data input/output terminals correspond to a second channel among the plurality of channels, each of the plurality of first data input/output terminals is arranged adjacent to at least one of the plurality of second data input/output terminals, each of the plurality of data input/output terminals is connected to one of a plurality of package terminals connected to at least one of the plurality of memory dies, a first package terminal among the plurality of package terminals corresponding to a L-th bit of the first channel is arranged adjacent to a second package terminal among the plurality of package terminals corresponding to a L-th bit of the second channel, the plurality of data input/output terminals and the plurality of package terminals are arranged to prevent signal lines from intersecting with each other, at least one of the plurality of signal lines between the interface port and the plurality of data input/output terminals includes at least one delay element to delay a data transmission time, a plurality of signal conversion circuits, which convert data input to the data input/output terminals or data output from the data input/output terminals into Tx or Rx signals, is located between the interface port and the plurality of data input/output terminals.

2. The memory system of claim 1, wherein a data input/output terminal corresponding to data of an I-th bit among the first data input/output terminals is arranged adjacent to a data input/output terminal corresponding to data of an I-th bit among the second data input/output terminals.

3. The memory system of claim 2, wherein the memory controller exchanges data in units of data segments through the first data input/output terminals, and exchanges data in units of data segments through the second data input/output terminals.

4. The memory system of claim 3, wherein: each of the first data input/output terminals is connected to a memory die in a first memory die group among the plurality of memory dies, and each of the second data input/output terminals is connected to a memory die in a second memory die group among the plurality of memory dies.

5. A memory controller comprising: a memory interface configured to communicate with a plurality of memory dies; and a control circuit configured to control the plurality of memory dies, wherein: the control circuit controls a physical interface circuit including a plurality of data input/output terminals which are paths through which data for a plurality of channels is

input/output and an interface port electrically connected to the plurality of data input/output terminals through a plurality of signal lines, data input to the data input/output terminals and data output from the data input/output terminals pass through the interface port, a plurality of first data input/output terminals among the plurality of data input/output terminals correspond to a first channel among the plurality of channels, a plurality of second data input/output terminals among the plurality of data input/output terminals correspond to a second channel among the plurality of channels, each of the plurality of first data input/output terminals is arranged adjacent to at least one of the plurality of second data input/output terminals, each of the plurality of data input/output terminals is connected to one of a plurality of package terminals connected to at least one of the plurality of memory dies, a first package terminal among the plurality of package terminals corresponding to a L-th bit of the first channel is arranged adjacent to a second package terminal among the plurality of package terminals corresponding to a L-th bit of the second channel, the plurality of data input/output terminals and the plurality of package terminals are arranged to prevent signal lines from intersecting with each other, at least one of the plurality of signal lines between the interface port and the plurality of data input/output terminals include at least one delay element to delay a data transmission time, a plurality of signal conversion circuits, which convert data input to the data input/output terminals or data output from the data input/output terminals into Tx or Rx signals, is located between the interface port and the plurality of data input/output terminals.

6. The memory controller of claim 5, wherein a data input/output terminal corresponding to data of an I-th bit among the first data input/output terminals is arranged adjacent to a data input/output terminal corresponding to data of an I-th bit among the second data input/output terminals.

7. The memory controller of claim 6, wherein the control circuit transmits or receives data in units of data segments through the first data input/output terminals, and transmits or receives data in units of data segments through the second data input/output terminals.

8. The memory controller of claim 7, wherein each of the first data input/output terminals is connected to a memory die in a first memory die group among the plurality of memory dies, and each of the second data input/output terminals is connected to a memory die in a second memory die group among the plurality of memory dies.