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High connectivity device stacking

Abstract

The present disclosure generally relates to stacked miniaturized electronic devices and methods of forming the same. More specifically, embodiments described herein relate to semiconductor device spacers and methods of forming the same. The semiconductor device spacers described herein may be utilized to form stacked semiconductor package assemblies, stacked PCB assemblies, and the like.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS (1) This application is a divisional of U.S. Nonporivisional Patent application Ser. No. 17/578,271, filed Jan. 18, 2022, which is a divisional of U.S. Nonprovisional patent application Ser. No. 16/814,785, filed Mar. 10, 2020, which is herein incorporated by reference in its entirety.

BACKGROUND
Field
(1) Embodiments of the present disclosure generally relate to stacked miniaturized electronic devices and methods of forming the same. More specifically, embodiments described herein relate to PCB and package spacers and methods of forming the same.
Description of the Related Art
(2) Due to an ever-increasing demand for miniaturized electronic devices with reduced footprint, electronic devices have evolved into complex 2.5D and 3D stacked devices. The evolution of stacked electronic device design has resulted in greater circuit densities in efforts to improve speed and processing capabilities and has also imposed corresponding demands on the materials, components, and processes used in the fabrication of such electronic devices.
(3) Conventionally, components of miniaturized electronic devices have been vertically stacked with spacers disposed between the individual device components to provide physical separation therebetween. These spacers are typically formed of a molding compound (e.g., epoxy molding compound, FR-4 and FR-5 grade woven fiberglass cloth with epoxy resin binders, and the like) and are patterned via mechanical processes to enable electrical connectivity of the device components. However, the materials utilized for the molding compound, as well as the patterning processes for the spacers, have several limitations that impede electronic device scaling and overall device performance.
(4) In particular, as a result of the thermal properties of current molding compound materials, coefficient of thermal expansion (CTE) mismatch may occur between the device components and adjacent spacers, thus necessitating larger solder bumps with greater spacing to mitigate any warpage of the device components or the spacers caused by the CTE mismatch. Furthermore, the intrinsic properties of these molding compound materials also cause difficulty in patterning fine (e.g., less than 50 μm) features in the spacers, which is magnified by the resolution limitations of the mechanical structuring processes themselves. Therefore, spacers utilizing conventional molding compound materials may create a bottleneck in the fabrication of stacked miniaturized electronic devices with reduced footprint.
(5) Therefore, what is needed in the art are improved spacers and structures for stacked miniaturized electronic devices and methods of forming the same.
SUMMARY
(6) The present disclosure generally relates to stacked miniaturized electronic devices and methods of forming the same. More specifically, embodiments described herein relate to semiconductor device spacers and methods of forming the same.
(7) In one embodiment, a semiconductor device spacer is provided. The semiconductor device spacer includes a frame having a first surface opposite a second surface, a frame material including a polymer-based dielectric material with spherical ceramic fillers, and a via including a via surface defining an opening extending through the frame from the first surface to the second surface. The via has a diameter between about 10 μm and about 150 μm. An electrical interconnection is further disposed within the via on the via surface.
(8) In one embodiment, a semiconductor device assembly is provided. The semiconductor device assembly includes a first printed circuit board (PCB) having a first glass fiber reinforced epoxy

resin material and a first electrical distribution layer formed on the first glass fiber reinforced epoxy resin material. The semiconductor device assembly further includes a second PCB having a second glass fiber reinforced epoxy resin material and a second electrical distribution layer formed on the second glass fiber reinforced epoxy resin material. The semiconductor device assembly also includes a device spacer interposed between the first PCB and the second PCB to facilitate a physical space therebetween. The device spacer includes a frame having a first surface opposite a second surface, a frame material including a polymer-based dielectric material with spherical ceramic fillers, and a via including a via surface defining an opening extending through the frame from the first surface to the second surface. The via has a diameter between about 10 μm and about 150 μm. An electrical interconnection is further disposed within the via on the via surface to form at least part of a conductive path extending between at least a portion of the first and second electrical distribution layers.

(9) In one embodiment, a semiconductor device assembly is provided. The semiconductor device assembly includes a printed circuit board (PCB) having a first glass fiber reinforced epoxy resin material and a first electrical distribution layer formed on the first glass fiber reinforced epoxy resin material. The semiconductor device assembly further includes a silicon substrate having a silicon cure structure with a thickness less than about 1000 μm and a second electrical distribution layer formed on the silicon core structure. The semiconductor device assembly also includes a device spacer interposed between the PCB and the silicon substrate to facilitate a physical space therebetween. The device spacer includes a frame having a first surface opposite a second surface and a thickness between about 400 μm and about 1600 μm, a frame material including a polymer-based dielectric material with spherical ceramic fillers, and a via including a via surface defining an opening extending through the frame from the first surface to the second surface. The thickness of the frame is substantially similar to a height of the physical space and the via has a diameter between about 10 μm and about 150 μm. An electrical interconnection is further disposed within the via on the via surface to form at least part of a conductive path extending between at least a portion of the first and second electrical distribution layers. A ratio of an area of the device spacer relative to an area of a surface of the PCB or the silicon substrate is between about 0.15 and about 0.85.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary embodiments and are therefore not to be considered limiting of its scope, and may admit to other equally effective embodiments.

(2) FIGS. **1**A and **1**B schematically illustrate cross-sectional views of semiconductor device spacers, according to embodiments described herein.

(3) FIG. **1**C illustrates an enlarged cross-sectional view of a portion of a semiconductor device spacer, according to embodiments described herein.

(4) FIGS. **2**A and **2**B schematically illustrate cross-sectional views of semiconductor device spacers, according to embodiments described herein.

(5) FIGS. **3**A and **3**B schematically illustrate top-down views of semiconductor device spacers, according to embodiments described herein.

(6) FIG. **4** is a flow diagram that illustrates a process for fabricating the semiconductor device spacers of FIGS. **1**-**3**B, according to embodiments described herein.

(7) FIGS. **5**A-**5**J schematically illustrate cross-sectional views of a semiconductor device spacer at different stages of the process depicted in FIG. **4**, according to embodiments described herein.
(8) FIG. **6** is a flow diagram that illustrates a process for fabricating a frame for utilization in a semiconductor device spacer, according to embodiments described herein.
(9) FIGS. **7**A-**7**E schematically illustrate cross-sectional views of a frame at different stages of the process depicted in FIG. **6**, according to embodiments described herein.
(10) FIG. **8** schematically illustrates a cross-sectional view of a stacked semiconductor device, according to embodiments described herein.
(11) FIG. **9** schematically illustrates a cross-sectional view of a stacked semiconductor device, according to embodiments described herein.
(12) FIG. **10** schematically illustrates a cross-sectional view of a stacked semiconductor device, according to embodiments described herein.
(13) FIGS. **11**A-**11**E schematically illustrate top views of semiconductor device spacer arrangements, according to embodiments described herein.
(14) To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the Figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

(15) The present disclosure generally relates to stacked miniaturized electronic devices and methods of forming the same. More specifically, embodiments described herein relate to semiconductor device spacers and methods of forming the same. The semiconductor device spacers described herein may be utilized to form stacked semiconductor package assemblies, stacked PCB assemblies, and the like.
(16) The stacked semiconductor devices and semiconductor device spacers disclosed herein are intended to replace more conventional semiconductor PCB and package assemblies utilizing spacers fabricated from molding compound materials (e.g., epoxy molding compound, FR-4 and FR-5 grade woven fiberglass cloth with epoxy resin binders, and the like). Generally, the scalability of stacked PCBs and package assemblies is limited in part by the intrinsic properties of the molding compound materials utilized to form these spacers. For example, the rigidity of these materials causes difficulty in patterning fine (e.g., micron scale) features in the spacers for interconnectivity of the individual device components within a stacked assembly. Furthermore, as a result of the thermal properties of currently-utilized molding compound materials, coefficient of thermal expansion (CTE) mismatch may occur between the spacers and any device components disposed adjacent thereto. Therefore, current PCB and package assemblies necessitate larger solder bumps with greater spacing to mitigate the effect of any warpage caused by CTE mismatch. Accordingly, conventional semiconductor PCB and package assemblies are characterized by low through-structure electrical bandwidths resulting in decreased overall power and efficiency. The methods and apparatus disclosed herein provide semiconductor device spacers that overcome many of the disadvantages associated with conventional PCB and package assemblies described above.
(17) FIGS. **1**A-**1**C, **2**A, and **2**B illustrate cross-sectional views of a semiconductor device spacer **100** according to some embodiments. The semiconductor device spacer **100** may be utilized for physical separation, structural support, and electrical interconnection of semiconductor devices and components mounted thereto. The semiconductor device spacer **100** may also be employed for stacking semiconductor packaging substrates, thus enabling economical space utilization in small electronic products and/or enhanced I/O connections and bandwidth between multiple packaging substrates. The semiconductor device spacer **100** also minimizes track length between different inter-operating parts to shorten routing of interconnections between substrates.
(18) The semiconductor device spacer **100** generally includes a frame **102** having one or more holes or vias **103** formed therethrough. In one embodiment, the frame **102** is formed of polymer-

based dielectric materials. For example, the frame **102** is formed from a flowable build-up material. In further embodiments, the frame **102** is formed of an epoxy resin material having ceramic fillers **130** (shown in FIG. **1**C), such as silica (SiO.sub.2) particles. Other examples of ceramic fillers **130** that may be utilized to form the frame **102** include aluminum nitride (AlN), aluminum oxide (Al.sub.2O.sub.3), silicon carbide (SiC), silicon nitride (Si.sub.3N.sub.4), Sr.sub.2Ce.sub.2Ti.sub.5O.sub.16, zirconium silicate (ZrSiO.sub.4), wollastonite (CaSiO.sub.3), beryllium oxide (BeO), cerium dioxide (CeO.sub.2), boron nitride (BN), calcium copper titanium oxide (CaCu.sub.3Ti.sub.4O.sub.12), magnesium oxide (MgO), titanium dioxide (TiO.sub.2), zinc oxide (ZnO) and the like.
(19) The ceramic fillers **130** are generally spherical in shape or morphology as depicted in the enlarged cross-sectional view of the frame **102** in FIG. **1**C. As utilized herein, the term “spherical” refers to any round, ellipsoid, or spheroid shape. For example, in some embodiments, the ceramic fillers **130** may have an elliptic shape, an oblong oval shape, or other similar round shape. However, other morphologies are also contemplated. In some examples, the ceramic fillers **130** utilized to form the frame **102** include particles ranging in diameter between about 40 nm and about 150 nm, such as between about 80 nm and about 100 nm. For example, the ceramic fillers **130** include particles ranging in diameter between about 200 nm and about 800 nm, such as between about 300 nm and about 600 nm. In some examples, the ceramic fillers **130** include particles having a substantially uniform diameter. In other examples, the ceramic fillers **130** include particles differing in diameter. The particles of the ceramic fillers **130** have a packing density (e.g., fraction of the solid volume of the frame **102** made up by the volume of the ceramic fillers **130**) between about 0.02 and about 0.99, such as a packing density between about 0.1 and about 0.98. For example, the ceramic fillers **130** in the frame **102** may have a packing density between about 0.2 and about 0.96, such as a packing density between about 0.5 and about 0.95.
(20) The frame **102** may have any desired morphology and dimensions. In some embodiments, the frame **102** has a polygonal morphology. For example, the frame **102** has a substantially rectangular shape with lateral dimensions between about 5 mm and about 100 mm, such as between about 10 mm and about 80 mm, for example between about 15 mm and about 50 mm. Generally the frame **102** has a thickness T.sub.0 between about 45 μm and about 5000 μm, such as a thickness T.sub.0 between about 100 μm and about 3000 μm. For example, the frame **102** has a thickness T.sub.0 between about 200 μm and about 2000 μm, such as a thickness T.sub.0 between about 400 μm and about 1600 μm.
(21) In some embodiments, the frame **102** is formed of one or more layers **110** of polymer-based dielectric materials that are laminated and cured together to form a single, integral body (e.g., block) for the frame **102**. For example, the frame **102** is formed of stacked individual layers **110***a-c* that are laminated and cured together to form a single, integral body. In such an example, the thickness T.sub.0 of the frame **102** is the sum of the thicknesses T.sub.A-C of the individual layers **110***a*-**110***c*, respectively. Each individual layer **110***a*-**110***c* utilized for the frame **102** has a thickness T.sub.A-B between about 10 um and about 150 um, such as between about 25 um and about 125 um, for example between about 50 um and about 100 um.
(22) The holes or vias **103** (hereinafter referred to as “vias”) are formed in the frame **102** to enable conductive electrical interconnections **104** to be routed through the frame **102**. For example, the vias **103** extend from a first surface **105** of the frame **102** to an opposing second surface **107**. Generally, the one or more vias **103** are substantially cylindrical in shape. However, other suitable morphologies for the vias **103** are also contemplated. The vias **103** may be formed as singular and isolated vias **103** through the frame **102** or in one or more groupings or arrays. In one embodiment, the vias **103** have a minimum pitch P.sub.0 less than about 1200 μm, such as a minimum pitch P.sub.0 between about 50 μm and about 1000 μm, such as between about 100 μm and about 800 μm. For example, the minimum pitch P.sub.0 is between about 150 μm and about 600 μm. For clarity, “pitch” refers to the distance between centers of adjacent vias **103**.

(23) In the embodiment depicted in FIG. **1**A, each of the one or more vias **103** has a substantially uniform diameter through the frame **102**. For example, each of the one or more vias **103** has a uniform diameter V.sub.1 less than about 500 μm throughout, such as a uniform diameter V.sub.1 between about 10 μm and about 200 μm throughout. In a further example, each of the vias **103** has a uniform diameter V.sub.1 between about 10 μm and about 180 μm throughout, such as a uniform diameter V.sub.1 between about 10 μm and about 150 μm throughout.
(24) Alternatively, in the embodiment depicted in FIG. **1**B, each of the one or more vias **103** has a tapering diameter through the frame **102**. For example, each of the one or more vias has a first diameter V.sub.1A at a first surface **105** that widens or expands to a second diameter V.sub.1B at a second surface **107**. Thus, it may be said that each via **103** tapers from the diameter V.sub.1B to the diameter V.sub.1A. In one example, the diameter V.sub.1B is less than about 500 μm, such between about 10 μm and about 200 μm, such as between about 10 μm and about 180 μm, such as between about 10 μm and about 150 μm. In one example, the diameter V.sub.1A is less than about 400 μm, such as between about 10 μm and about 130 μm, such as between about 10 μm and about 120 μm, such as between about 10 μm and about 100 μm.
(25) The vias **103** provide channels through which one or more electrical interconnections **104** are formed in the semiconductor device spacer **100**. In one embodiment, the vias **103** and the electrical interconnections **104** are formed through the entire thickness T.sub.0 of the semiconductor device spacer **100** (i.e. from the first surface **105** to the second surface **107** of the semiconductor device spacer **100**). For example, the electrical interconnections **104** have a longitudinal length L corresponding to the thickness T.sub.0 of the semiconductor device spacer **100** between about 45 μm and about 5000 μm, such as a longitudinal length L between about 100 μm and about 3000 μm. In one example, the electrical interconnections **144** have a longitudinal length L between about 200 μm and about 2000 μm, such as a longitudinal length L between about 400 μm and about 1600 μm. In another embodiment, the vias **103** and/or electrical interconnections **104** are only formed through a portion of the thickness T.sub.0 of the semiconductor device spacer **100**. In further embodiments, the electrical interconnections **104** protrude from one or more surfaces of the semiconductor device spacer **100**, such as the surfaces **105**, **107** as depicted in FIGS. **1**A and **1**B. The electrical interconnections **104** are formed of any conductive materials used in the field of microelectronic devices, integrated circuits, circuit boards, and the like. For example, the electrical interconnections **104** are formed of a metallic material, such as copper, aluminum, gold, nickel, silver, palladium, tin, or the like.
(26) In the embodiments depicted in FIGS. **1**A-**2**B, the electrical interconnections **104** fill the vias **103**. However, in some embodiments, the electrical interconnections **104** only line the surfaces of the sidewalls **113** of the vias **103** and do not fully fill (e.g., completely occupy) the vias **103**. Thus, the interconnections **104** may have hollow cores therethrough.
(27) Furthermore, in FIGS. **1**A and **1**B, the electrical interconnections **104** have a diameter equal to the diameter of the vias **103** in which they are formed. In further embodiments, such as depicted in FIGS. **2**A and **2**B, the semiconductor device spacer **100** further includes an adhesion layer **112** and/or a seed layer **114** formed thereon for electrical isolation of the electrical interconnections **104**. In one embodiment, the adhesion layer **112** is formed on surfaces of the semiconductor device spacer **100** adjacent to the electrical interconnections **104**, including the sidewalls **113** of the vias **103**. Thus, as depicted in FIGS. **2**A and **2**B, the electrical interconnections **104** have a diameter less than the diameter of the vias **103** in which they are formed. For example, in FIG. **2**A, the electrical interconnections have a uniform diameter V.sub.2 less than the diameter V.sub.1 of the vias **103**. In FIG. **2**B, the electrical interconnections have a first diameter V.sub.2A less than the diameter V.sub.1A that tapers to a second diameter V.sub.2B less than a diameter V.sub.1B.
(28) The adhesion layer **112** is formed of any suitable materials, including but not limited to titanium, titanium nitride, tantalum, tantalum nitride, manganese, manganese oxide, molybdenum, cobalt oxide, cobalt nitride, silicon nitride and the like. In one embodiment, the adhesion layer **112**

has a thickness between about 10 nm and about 300 nm, such as between about 50 nm and about 150 nm. For example, the adhesion layer **112** has a thickness between about 75 nm and about 125 nm, such as about 100 nm.
(29) The optional seed layer **114** comprises a conductive material, including but not limited to copper, tungsten, aluminum, silver, gold, or any other suitable materials or combinations thereof. The seed layer **114** is formed on the adhesion layer **112** or directly on the sidewalls **113** of the vias **103** (on the frame **102**). In one embodiment, the seed layer **114** has a thickness between about 50 nm and about 2000 nm, such as between about 100 nm and about 1000 nm. For example, the seed layer **112** has a thickness between about 150 nm and about 800 nm, such as about 500 nm.
(30) FIGS. **3**A and **3**B illustrate schematic top-down views of the semiconductor device spacer **100** with exemplary arrangements of vias **103** formed therein. As described above, the vias **103** are generally cylindrical in shape and thus, appear circular in FIGS. **3**A and **3**B. Other morphologies for the vias **103**, however, are also contemplated. FIGS. **3**A and **3**B further depict the adhesion layer **112** and the seed layer **114** formed within each via **103**. The adhesion layer **112** is formed on the sidewalls **113** of each via **103** and the seed layer **114** is formed on the adhesion layer **112**. However, in some embodiments, the interconnections **104** may be formed through the vias **103** without the utilization of the adhesion layer **112** and/or the seed layer **114**. In other embodiments, the seed layer **114** may be formed on the sidewalls **113** of the vias **103** without the utilization of the adhesion layer **112** prior to formation of the interconnections **104**.
(31) The vias **103** are formed in any suitable arrangement and number through the frame **102**. As depicted in FIG. **3**A, six vias **103** are formed through the frame **102** in a linear arrangement having two columns and three rows of vias **103**, wherein the vias **103** in each column and in each row are aligned with one another. A first pitch P.sub.1 is depicted between adjacent vias **103** aligned in each row, a second pitch P.sub.2 is depicted between adjacent vias **103** aligned in each column, and a third pitch P.sub.3 is depicted between adjacent and diagonal vias **103** across the two columns. At least two of the pitches P.sub.1, P.sub.2, or P.sub.3 may be different from one another in length.
(32) FIG. **3**B illustrates an alternative arrangement also having two columns and three rows of vias **103**, wherein only the vias **103** in each column are aligned. Accordingly, the pitch between all adjacent vias **103** is substantially the same in length, represented in FIG. **3**B by the pitch P.sub.1. As described above, “pitch” refers to the distance between centers of adjacent vias **103**. Although two arrangements of vias **103** are depicted, FIGS. **3**A and **3**B are only exemplary and any suitable number and arrangement of vias **103** may be formed in the frame **102** of the semiconductor device spacer **100**.
(33) FIG. **4** illustrates a flow diagram of a representative method **400** of forming a semiconductor device spacer **500**. The method **400** has multiple operations **402-416** The method may include one or more additional operations which are carried out before any of the defined operations, between two of the defined operations, or after all of the defined operations (except where the context excludes the possibility). FIGS. **5**A-**5**J schematically illustrate cross-sectional views of a semiconductor device spacer **500** at various stages of the method **400** represented in FIG. **4**. Therefore, FIG. **4** and FIGS. **5**A-**5**J are herein described together for clarity.
(34) The method **400** beings at optional operation **402** and corresponding FIG. **5**A, wherein one or more protective films **501** are removed from each of two or more device spacer precursor layers **510***a*, **510***b*. The precursor layers **510***a*, **510***b* act as building blocks for formation of the frame **102** of the semiconductor device spacer **500** and thus, the precursor layers **510***a*, **510***b* are formed of a polymer-based dielectric material as described above with reference to the frame **102**. For example, the precursor layers **510***a*, **510***b* are formed of flowable build-up materials. In one embodiment, the precursor layers **510***a*, **510***b* are formed of a ceramic-filler-containing epoxy resin, such as an epoxy resin filled with (e.g., containing) silica (SiO.sub.2) particles. Other examples of ceramic fillers **130** that may be utilized in the precursor layers **510***a*, **510***b* include aluminum nitride (AlN), aluminum oxide (Al.sub.2O.sub.3), silicon carbide (SiC), silicon nitride (Si.sub.3N.sub.4),

Sr.sub.2Ce.sub.2Ti.sub.5O.sub.16, zirconium silicate (ZrSiO.sub.4), wollastonite (CaSiO.sub.3), beryllium oxide (BeO), cerium dioxide (CeO.sub.2), boron nitride (BN), calcium copper titanium oxide (CaCu.sub.3Ti.sub.4O.sub.12), magnesium oxide (MgO), titanium dioxide (TiO.sub.2), zinc oxide (ZnO) and the like. Generally, each precursor layer **510**_a_, **510**_b_ has a thickness TL less than about 150 μm, such as a thickness TL between about 10 μm and about 150 μm, such as between about 25 μm and about 125 μm, for example between about 50 μm and about 100 μm. Any suitable amount of precursor layers **510**_a_, **510**_b_ may utilized during the method **400** to form a semiconductor device spacer **100** having any desired dimensions.

(35) In some embodiments, each precursor layer **510**_a_, **510**_b_ is coupled to one or more protective films **501** that are configured to protect the precursor layers **510**_a_, **510**_b_ during handling and storage thereof. Thus, at operation **402**, the one or more protective films **501** are removed from each precursor layer **510**_a_, **510**_b_ to expose one or more major surfaces of each precursor layer **510**. As depicted in FIG. **5**A, a single protective film **501** is removed from each of the two precursor layers **510**_a_, **510**_b_ to expose surfaces **505**, **507** thereof for coupling of the precursor layers **510**_a_, **510**_b_ at operation **404**.

(36) At operation **404**, the one or more precursor layers **510** are coupled together (e.g., placed against one another) at the exposed surfaces thereof and laminated. Coupling and lamination of the surfaces **505**, **507** of the precursor layers **510**_a_, **510**_b_ is depicted in FIGS. **5**B and **5**C. Upon placement of the precursor layers **510**_a_, **510**_b_ together, a vacuum pressure is applied to draw out any air captured between the major surfaces **505**, **507** during the coupling thereof, as shown in FIG. **5**B. Accordingly, at least a portion of operation **404** may be carried out in a vacuum laminator or vacuum bonder or any other suitable vessel for application of vacuum pressure. In one embodiment, the vacuum pressure is ramped up to about 1 hPa or less during an interval (e.g., time period) between about 10 seconds and about 90 seconds, such as an interval between about 30 seconds and about 60 seconds, such as an interval of about 45 seconds. Upon reaching a desired vacuum pressure level, the vacuum pressure may be maintained for an interval between about 50 seconds and 300 seconds, such as an interval between about 100 seconds and 200 seconds. In one example, the vacuum pressure is maintained at about 1 hPa or less for an interval of about 150 seconds to ensure removal of any air gaps between the precursor layers **510**. During the application of vacuum pressure, the temperature is maintained within a range between about 60° C. and about 100° C., such as between about 70° C. and about 90° C. For example, the temperature is maintained at about 80° C. during the application of vacuum pressure at operation **404**.

(37) In FIG. **5**C, the coupled precursor layers **510**_a_, **510**_b_ are fused (e.g., laminated) together by application of pressure upon one or more outer surfaces of the precursor layers **510**_a_, **510**_b_. In one embodiment, a single-sided pressure is applied to the coupled precursor layers **510**_a_, **510**_b_ as the coupled precursor layers **510**_a_, **510**_b_ are supported upon a supporting diaphragm or platen (e.g., platform) (not shown). For example, pressure may be applied to a single side **517** of the coupled precursor layers **510**_a_, **510**_b_ as the coupled precursor layers **510**_a_, **510**_b_ are supported by a platen on an opposing side **515**. In other embodiments, a double-sided pressure is applied to the coupled precursor layers **510**_a_, **510**_b_. For example, pressure is applied to both sides **515**, **517** by mechanical devices, such as a mechanical press or vice, or by pneumatic devices, such as pneumatic devices using compressed air. In some embodiments, lamination of the precursor layers **510**_a_, **510**_b_ is carried out in the same vessel as the application of vacuum depicted in FIG. **5**B. For example, lamination is carried out in a vacuum laminator or vacuum bonder.

(38) During the lamination of the precursor layers **510**_a_, **510**_b_, a temperature is maintained within a range between about 50° C. and about 150° C., such as between about 75° C. and about 125° C., such as about 100° C. Exposing the precursor layers **510**_a_, **510**_b_ to elevated temperatures may soften the precursor layers **510**_a_, **510**_b_ and promote adhesion therebetween. In some embodiments, a pressure applied to the precursor layers **510**_a_, **510**_b_ during lamination is between about 0.3 kg/cm.sup.2 and about 1 kg/cm.sup.2, such as between about 0.4 kg/cm.sup.2 and about 0.8

kg/cm.sup.2, such as about 0.5 kg/cm.sup.2 or about 0.6 kg/cm.sup.2.

(39) Upon completion of operation **404**, the operations **402** and **404** may be repeated to couple and fuse additional precursor layers **510** to the already fused precursor layers **510***a*, **510***b*, or the fused precursor layers **510***a*, **510***b* may be exposed to a cure process at operation **406** to form a frame **502** in preparation for further structuring. For example, one or more additional precursor layers **510** may be coupled to and fused with the side **515** and/or the side **517** of the fused precursor layers **510***a*, **510***b* until a desired thickness of precursor material (corresponding to a final thickness of the frame **102**) is achieved. Thus, one or more remaining protective films **501** coupled to the fused precursor layers **510***a*, **510***b* are removed therefrom in preparation for the attachment of additional precursor layers **510**, in addition to any protective films **501** coupled to the additional precursor layers **510** themselves. As depicted in FIG. **5**D, a single protective film **501** is removed from the side **517** of the fused precursor layers **510***a*, **510***b* in preparation for the coupling of a third precursor layer **510***c* thereto.

(40) In other examples, a protective film **501** is removed from each side **515**, **517** of the fused precursor layers **510***a*, **510***b* in preparation for the coupling of an additional third and fourth precursor layer (not shown) to the sides **515**, **517** of the fused precursor layers **510***a*, **510***b*. Thus, the number of protective films **501** removed from the fused precursor layers **510***a*, **510***b* may be dependent upon the number of additional precursor layers **510** to be added thereto. If no additional precursor layers **510** are desired to be added to the fused precursor layers **510***a*, **510***b* and the fused precursor layers **510***a*, **510***b* are ready for curing, one or more protective films **501** coupled to both sides **515**, **517** may be removed before exposure of the fused precursor layers **510***a*, **510***b* to the cure process at operation **406** depicted in FIG. **5**E.

(41) At operation **406**, the fused precursor layers **510***a*, **510***b* are exposed to the cure process to partially or fully cure (i.e., harden through chemical reactions and cross-linking) the polymer-based dielectric material of the fused precursor layers **510***a*, **510***b* and form the frame **502**. In some embodiments, the cure process is performed at high temperatures to fully cure the frame **502**. In further embodiments, the cure process is performed at or near ambient (e.g., atmospheric) pressure conditions. During the cure process, the fused precursor layers **510***a*, **510***b* are placed on a first platen **520***a* within a vacuum oven, vacuum bonder, vacuum laminator or any other suitable vessel for application of vacuum pressure. The first platen **520***a* includes an anti-stick layer **522** disposed on a side thereof that is configured to contact and support the fused precursor layers **510***a*, **510***b* during curing. The anti-stick layer **522** is formed of any suitable non-stick materials having a low roughness value such as Teflon, PDMS, polyimide, fluorinated ethylene propylene, and the like.

(42) Upon placement of the fused precursor layers **510***a*, **510***b* on the first platen **520***a*, a temperature and pressure within the vacuum chamber is ramped up to a first curing pressure of about 0.001 hPa and a first curing temperature of about 110° C. For example, the first curing pressure within the vacuum chamber is ramped up to between about 0.001 hPa and about 10 hPa, such as between about 0.001 hPa and about 1 hPa. In one example, the first curing temperature within the vacuum chamber is ramped up to between about 60° C. and about 110° C., such as between about 100° C. and about 110° C. Ramping of the temperature and/or the pressure within the vacuum chamber may be carried out over an interval between about 15 minutes and about 45 minutes, such as an interval between about 20 minutes and about 40 minutes. In one example, the temperature and/or pressure are ramped up over an interval of about 30 minutes upon placement of the fused precursor layers **510***a*, **510***b* on the first platen **520***a*.

(43) Upon reaching a desired first curing temperature and/or first curing pressure within the vacuum chamber, a second platen **520***b* is pressed against a side of the fused precursor layers **510***a*, **510***b* opposite the first platen **520***a* to clamp or secure the fused precursor layers **510***a*, **510***b* in place. Similar to the first platen **520***a*, the second platen **520***b* also includes an anti-stick layer **522** disposed on a side thereof that is configured to contact the fused precursor layers **510***a*, **510***b*. Once the fused precursor layers **510***a*, **510***b* are secured between the two platens **520***a*, **520***b*, the fused

precursor layers **510***a*, **510***b* are held in place for an interval between about 45 minutes and about 75 minutes and at the first curing temperature and first curing pressure. For example, the fused precursor layers **510***a*, **510***b* may be held between the two platens **520***a*, **520***b* at a temperature of about 110° C. and a pressure of about 0.01 MPa for a period of about 60 minutes.

(44) In some embodiments, after holding the fused precursor layers **510***a*, **510***b* between the two platens **520***a*, **520***b* for a desired amount of time at the first curing temperature and the first curing pressure, the first curing temperature is again ramped up to a second curing temperature while the first curing pressure is maintained. For example, the first curing temperature is ramped up again to a second curing temperature between about 150° C. and about 180° C., such as between about 170° C. and about 180° C. In one example, the second curing temperature is about 180° C. The fused precursor layers **510***a*, **510***b* may then be held between the two platens **520***a*, **520***b* at the second curing temperature and the first curing pressure for an interval between about 15 minutes and about 45 minutes, such as between 20 minutes and about 40 minutes, such as about 30 minutes. After exposing the fused precursor layers **510***a*, **510***b* to the second curing temperature, the curing process may be completed and the cured frame **502** is cooled and removed from the platens **520***a*, **520***b*.

(45) At operation **408** and FIG. **5**F, the cured frame **502** is exposed to a laser ablation process (e.g., direct laser patterning) to form one or more vias **503** therein. Any suitable laser ablation system may be utilized to form the one or more vias **503**. In some examples, the laser ablation system utilizes an infrared (IR) laser source. In some examples, the laser source is a nanosecond or picosecond ultraviolet (UV) laser. In other examples, the laser is a femtosecond UV laser. In still other examples, the laser source is a femtosecond green laser.

(46) The laser source of the laser ablation system generates a continuous or pulsed laser beam for patterning of the frame **502**. For example, the laser source generates a pulsed laser beam having a frequency between 5 kHz and 1000 kHz, such as between 10 kHz and about 200 kHz, such as between 15 kHz and about 100 kHz. In one embodiment, the laser source is configured to deliver a pulsed laser beam at a wavelength between about 200 nm and about 1200 nm and a pulse duration between about 10 ns and about 5000 ns with an output power between about 10 Watts and about 100 Watts. In one embodiment, the laser source is configured to deliver a pulsed laser beam at fluctuating time intervals. For example, the laser source delivers one or more rounds of pulses having between about 1 pulse and about 20 pulses with time delays therebetween. Pulse-timing fluctuations may reduce the overall thermal impact of the laser beam on the formation of the vias **503** and any other features in the frame **502**. Generally, the laser source is configured to form any desired pattern of vias **503** in the frame **502**, such as individual vias **503** or arrays of vias **503**.

(47) In some embodiments, the vias **503** are formed having substantially uniform diameters throughout lengths thereof (for example, between a first surface **424** and a second surface **527** of the frame **502**). The vias **503** of uniform diameters may be formed by first piercing a hole into the frame **502** with a laser beam generated by the laser source and then moving the laser beam in a spiraling (e.g., circular, corkscrew) motion relative to the central axis of each of the vias **503**. The laser beam may also be angled using a motion system to form the uniform vias **503**. In other embodiments, the vias **503** are formed having a tapering diameters throughout lengths thereof. The tapering of vias **503** may be formed by using the same method described above, or by pulsing the laser beam generated by the laser source at a single location in the frame **502** continuously.

(48) After formation of the vias **503**, the cured and patterned frame **502** is exposed to a de-smear process. During the de-smear process, any unwanted residues and/or debris caused by laser ablation during the formation of the vias **503** are removed therefrom. The de-smear process thus cleans the vias **503** for subsequent metallization. In one embodiment, the de-smear process is a wet de-smear process. Any suitable solvents, etchants, and/or combinations thereof are utilized for the wet de-smear process. In one example, methanol is utilized as a solvent and copper (II) chloride dihydrate (CuCl.sub.2.Math.H.sub.2O) as an etchant. Depending on the residue thickness, exposure duration

of the frame **502** to the wet de-smear process is varied. In another embodiment, the de-smear process is a dry de-smear process. For example, the de-smear process is a plasma de-smear process with an O.sub.2/CF.sub.4 mixture gas. The plasma de-smear process may include generating a plasma by applying a power of about 700 W and flowing O.sub.2:CF.sub.4 at a ratio of about 10:1 (e.g., 100:10 sccm) for a time period between about 60 seconds and about 120 seconds. In further embodiments, the de-smear process is a combination of wet and dry processes.

(49) Following the de-smear process, the frame **502** is ready for formation of conductive interconnections therein. At optional operation **410** and corresponding FIG. **5**G, an adhesion layer **512** and/or a seed layer **514** are formed on the frame **502**. The adhesion layer **512** is formed on desired surfaces of the frame **502**, such as surfaces **525**, **527** as well as sidewalls **513** of the vias **503**, to assist in promoting adhesion and blocking diffusion of the subsequently formed seed layer **514** and electrical interconnections **504**. Thus, in one embodiment, the adhesion layer **512** acts as an adhesion layer; in another embodiment, the adhesion layer **512** acts as a barrier layer. In both embodiments, however, the adhesion layer **512** will be described as an "adhesion layer."

(50) In one embodiment, the adhesion layer **512** is formed of titanium, titanium nitride, tantalum, tantalum nitride, manganese, manganese oxide, molybdenum, cobalt oxide, cobalt nitride, silicon nitride, or any other suitable materials or combinations thereof. In one embodiment, the adhesion layer **512** has a thickness between about 10 nm and about 300 nm, such as between about 50 nm and about 150 nm. For example, the adhesion layer **512** has a thickness between about 75 nm and about 125 nm, such as about 100 nm. The adhesion layer **512** is formed by any suitable deposition process, including but not limited to chemical vapor deposition (CVD), physical vapor deposition (PVD), plasma enhanced CVD (PECVD), atomic layer deposition (ALD), or the like.

(51) The seed layer **514** may be formed on the adhesion layer **512** or directly on the frame **502** (e.g., without the formation of the adhesion layer **512**). In some embodiments, the seed layer **514** is formed on all surfaces of the frame **502** while the adhesion layer **512** is only formed on desired surfaces or desired portions of surfaces of the frame **502**. For example, the adhesion layer **512** is formed on the surfaces **525**, **527** and not on the sidewalls **513** of the vias **503** while the seed layer **514** is formed on the surfaces **525**, **527** as well as sidewalls **513** of the vias **503**. The seed layer **514** is formed of a conductive material such as copper, tungsten, aluminum, silver, gold, or any other suitable materials or combinations thereof. In one embodiment, the seed layer **514** has a thickness between about 0.05 μm and about 0.5 μm, such as a thickness between about 0.1 μm and about 0.3 μm. For example, the seed layer **514** has a thickness between about 0.15 μm and about 0.25 μm, such as about 0.2 μm. In one embodiment, the seed layer **514** has a thickness between about 0.1 μm and about 1.5 μm.

(52) Similar to the adhesion layer **512**, the seed layer **514** is formed by any suitable deposition process, such as CVD, PVD, PECVD, ALD dry processes, wet electroless plating processes, or the like. In one embodiment, a copper seed layer **514** is formed on a molybdenum adhesion layer **512** on the frame **502**. The molybdenum adhesion and copper seed layer combination enables improved adhesion with the surfaces of the frame **502** and reduces undercut of conductive interconnect lines during a subsequent seed layer etch process.

(53) At operation **412**, corresponding to FIG. **5**H, a spin-on/spray-on or dry resist film **550**, such as a photoresist, is applied over surfaces **525**, **527** of the frame **502** and subsequently patterned. In one embodiment, the resist film **550** is patterned via selective exposure to UV radiation. In one embodiment, an adhesion promoter (not shown) is applied to the frame **502** prior to formation of the resist film **550**. The adhesion promoter improves adhesion of the resist film **550** to the frame **502** by producing an interfacial bonding layer for the resist film **550** and by removing any moisture from the surface of the frame **502**. In some embodiments, the adhesion promoter is formed of bis(trimethylsilyl)amine or hexamethyldisilizane (HMDS) and propylene glycol monomethyl ether acetate (PGMEA).

(54) Upon application of the resist film **550**, the frame **502** is exposed to a resist film development

process. The development of the resist film **550** results in exposure of the vias **503** (shown in FIG. **5**H), which may now have an adhesion layer **512** and/or a seed layer **514** formed thereon. In one embodiment, the film development process is a wet process, such as a wet process that includes exposing the resist film **550** to a solvent. In one embodiment, the film development process is a wet etch process utilizing an aqueous etch process. For example, the film development process is a wet etch process utilizing a buffered etch process selective for a desired material. Any suitable wet solvents or combination of wet etchants are used for the resist film development process.

(55) At operation **414** and FIG. **5**I, electrical interconnections **504** are formed through the exposed vias **503** and the resist film **550** is thereafter removed. The interconnections **504** are formed by any suitable methods, including electroplating and electroless plating. In one embodiment, the resist film **550** is removed via a wet process. As depicted in FIG. **5**I, the electrical interconnections **504** completely fill the vias **503** and protrude from the surfaces **525**, **527** of the frame **502** upon removal of the resist film **550**. In some embodiments, the electrical interconnections **504** only line the sidewalls **513** of the vias **503** without completely filling the vias **503**. In one embodiment, the electrical interconnections **504** are formed of copper. In other embodiments, the electrical interconnections **504** are formed of any suitable conductive material including but not limited to aluminum, gold, nickel, silver, palladium, tin, or the like.

(56) At operation **416** and FIG. **5**J, the frame **502** having electrical interconnections **504** formed therein is exposed to a seed layer etch process to remove the exposed adhesion layer **512** and/or seed layer **514** on external surfaces thereof (e.g., surfaces **525**, **527**). Upon completion of the seed layer etch process at operation **416**, the frame **502** is ready to be utilized as a semiconductor device spacer **500**. In some embodiments, the adhesion layer **512** and/or seed layer **514** formed between the electrical interconnections **504** and the sidewalls **513** of the vias **503** remain after the seed layer etch process. In one embodiment, the seed layer etch is a wet etch process including a rinse and drying of the frame **502**. In one embodiment, the seed layer etch process is a buffered etch process selective for a desired material such as copper, tungsten, aluminum, silver, or gold. In other embodiments, the etch process is an aqueous etch process. Any suitable wet etchant or combination of wet etchants are used for the seed layer etch process.

(57) As discussed above, FIG. **4** and FIGS. **5**A-**5**J illustrate a representative method **400** for forming a semiconductor device spacer **500**. FIG. **6** and FIGS. **7**A-**7**E illustrate an alternative method **600** for forming the frame **502** at operation **406**. The method **600** generally includes five operations **602-610**, and optional operation **602** (corresponding to FIG. **7**A) is substantially similar to operation **402** of the method **400**. Thus, method **600** will be described starting with operation **604** for clarity.

(58) Accordingly, after peeling of protective films **501** from the precursor layers **510***a*, **510***b*, the precursor layers **510***a*, **510***b* are laminated together at operation **604** and FIG. **7**B. Similar to operation **404**, the precursor layers **510***a*, **510***b* are placed against one another at exposed surfaces **505**, **507** thereof, after which a vacuum pressure is applied to draw out any air captured between the coupled surfaces **505**, **507**. In one embodiment, the precursor films **510***a*, **510***b* are exposed to a vacuum pressure between about 0.001 hPa and about 100 hPa. For example, the precursor films **510***a*, **510***b* are exposed to a vacuum pressure between about 0.001 hPa and about 10 hPa, such as a vacuum pressure between about 0.001 hPa and about 1 hPa. The vacuum pressure is applied for an interval between about 10 seconds and about 60 seconds, such as an interval between about 15 seconds and about 45 seconds, such as about 30 seconds. During application of vacuum pressure, the temperature is maintained within a range between about 60° C. and about 100° C., such as between about 70° C. and about 90° C., such as about 80° C.

(59) After exposing the precursor films **510***a*, **510***b* to a vacuum pressure, the precursor films **510***a*, **510***b* are laminated together by application of a positive pressure to one of more outer surfaces of the precursor layers **510***a*, **510***b*. As described above, the applied pressure may be single-sided or double-sided and applied by mechanical or pneumatic processes. In one embodiment, a pressure

between about 0.3 and about 1 kg/cm.sup.2 is applied to one or more outer surfaces of the precursor layers **510***a*, **510***b*. For example, the precursor films **510***a*, **510***b* are exposed to a positive pressure between about 0.3 and about 0.8 kg/cm.sup.2, such as a pressure of about 0.5 kg/cm.sup.2. The positive pressure is applied for an interval between about 10 seconds and about 60 seconds, such as an interval between about 15 seconds and about 45 seconds, such as about 30 seconds. During the application of positive pressure, the temperature is maintained within a range between about 60° C. and about 100° C., such as between about 70° C. and about 90° C., such as about 80° C.

(60) After fusing the precursor layers **510***a*, **510***b* together, the precursor layers **510***a*, **510***b* are then laminated to a substrate **620** at operation **606** and FIG. **7**C. The substrate **620** is any suitable type of substrate having an anti-stick layer **622** disposed on a side thereof that is configured to contact and support the fused precursor layers **510***a*, **510***b*. In some embodiments, the substrate **620** comprises a metal or ceramic material and has a thickness between about 0.5 mm and about 1 mm. For example, the substrate **620** has a thickness between about 0.6 mm and about 0.8 mm, such as about 0.7 mm or about 0.75 mm. In some embodiments, the lateral dimensions of the substrate **620** exceed the dimensions of the precursor layers **510***a*, **510***b* such that an entire lateral area of the precursor layers **510***a*, **510***b* is supported upon the substrate **620**. The anti-stick layer **622** is formed of any suitable non-stick materials having a low roughness value, such as Teflon, PDMS, polyimide, fluorinated ethylene propylene, and the like.

(61) Similar to operation **604**, lamination of the fused precursor layers **510***a*, **510***b* to the substrate **620** includes coupling the fused precursor layers **510***a*, **510***b* to the anti-stick layer **622** and exposing the precursor layers **510***a*, **510***b* and substrate **620** to vacuum followed by a positive pressure. In one embodiment, the vacuum pressure is between about 0.001 hPa and about 100 hPa. For example, the coupled precursor films **510***a*, **510***b* and substrate **620** are exposed to a vacuum pressure between about 0.001 hPa and about 10 hPa, such as a vacuum pressure between about 0.001 hPa and about 1 hPa. The vacuum pressure is applied for an interval between about 10 seconds and about 60 seconds, such as an interval between about 15 seconds and about 45 seconds, such as about 30 seconds. During application of vacuum pressure, the temperature is maintained within a range between about 60° C. and about 120° C., such as between about 70° C. and about 110° C., such as about 80° C.

(62) After vacuum, a positive pressure is applied to one of more outer surfaces of the coupled precursor layers **510***a*, **510***b* and/or the substrate **620**. In one embodiment, the positive pressure is between about 0.3 and about 1 kg/cm.sup.2, such as between about 0.4 and about 0.8 kg/cm.sup.2, such as a pressure of about 0.5 kg/cm.sup.2. The positive pressure is applied for an interval between about 10 seconds and about 60 seconds, such as an interval between about 15 seconds and about 45 seconds, such as about 30 seconds. During the application of positive pressure, the temperature is maintained within a range between about 60° C. and about 120° C., such as between about 70° C. and about 110° C., such as about 80° C.

(63) Upon completion of operation **606**, the operations **602** and **604** may be repeated to couple and fuse additional precursor layers **510** to the precursor layers **510***a*, **510***b* already fused together with the substrate **620**, or the precursor layers **510***a*, **510***b* may be exposed to a cure process at operation **608** and FIG. **7**D to form the frame **502**. Prior to the cure process, any remaining protective films **501** on the fused precursor layers **510***a*, **510***b* are removed therefrom. In one embodiment, the cure process at operation **608** includes exposing the fused precursor layers **510***a*, **510***b* and substrate **620** to a constant temperature between about 150° C. and about 200° C. for an interval between about 15 minutes and about 90 minutes. For example, the fused precursor layers **510***a*, **510***b* and the substrate **620** are exposed to a temperature of about 180° C. for an interval of about 30 minutes.

(64) In another embodiment, the cure process includes exposing the fused precursor layers **510***a*, **510***b* and the substrate **620** to a variable temperature. For example, the fused precursor layers **510***a*, **510***b* and the substrate **620** are exposed to a first temperature between about 80° C. and about 120°

C. for an interval between about 45 minutes and about 75 minutes, followed by exposure to a second temperature between about 160° C. and about 200° C. for an interval between about 15 minutes and about 45 minutes. For example, the fused precursor layers **510**_a_, **510**_b_ and the substrate **620** are exposed to a first temperature of about 100° C. for an interval of about 60 minutes, followed by exposure to a second temperature of about 180° C. for an interval of about 30 minutes. After curing, the cured precursor frame **502** is removed from the substrate **620** for further structuring at operation **610** and FIG. **7**E.

(65) The semiconductor device spacers **100**, **500** may be utilized in any suitable stacked PCB assembly, stacked package assembly, or other suitable stacked electronic device. In one exemplary embodiment depicted in FIG. **8**, two semiconductor device spacers **100** are utilized within a PCB assembly **800**. As shown, the semiconductor device spacers **100** are disposed between two PCB's **850**_a_, **850**_b_ and are configured to position the first PCB **850**_a_ relative to the second PCB **850**_b_ such that a physical space **820** remains between the first PCB's **850**_a_, **850**_b_ while they are conductively connected through the semiconductor device spacers **100**. Accordingly, the semiconductor device spacers **100** prevent the PCB's **850**_a_, **850**_b_ from contacting one another, and thus, reduce the risk of shorting thereof. Additionally, interposition of the semiconductor device spacers **100** between the PCB's **850**_a_, **850**_b_ may assure proper and easy placement of the PCB's **850**_a_, **850**_b_ relative to one another, enabling proper alignment of contacts and holes therebetween. Furthermore, the interposition of the semiconductor device spacers **100** between adjacent PCB's **850**_a_, **850**_b_ reduces the risk of overheating and burning of the PCB's **850**_a_, **850**_b_ since the facilitation of the physical space **820** reduces the amount of heat trapped therebetween. Although only two PCBs **850**_a_, **850**_b_ are shown in FIG. **8**, it is contemplated the semiconductor device spacers **100** may be utilized to stack and interconnect two or more PCB's in parallel.

(66) The PCB's **850**_a_, **850**_b_ are formed of any suitable dielectric material. For example, the PCB's **850**_a_, **850**_b_ are formed of a glass fiber reinforced epoxy resin (e.g., FR-1, FR-2, FR-4, halogen-free FR-4, high T.sub.g FR-4, and FR-5). Other suitable examples of dielectric materials include resin copper-clad (RCC), polyimide, polytetrafluoroethylene (PTFE), CEM-3, and the like. The PCB's **850**_a_, **850**_b_ may be single-sided or double-sided circuit boards. In some embodiments, at least one of the PCB's **850**_a_, **850**_b_ includes an electrical distribution layer **870** formed thereon and conductively connected with interconnections **104** of the semiconductor device spacers **100**. For example, as depicted in FIG. **8**, both PCB's **850**_a_, **850**_b_ include electrical distribution layers **870**_a_, **870**_b_ formed thereon and adjacent the physical space **820**, respectively. The electrical distribution layers **870**_a_, **870**_b_ are formed of any suitable conductive material such as copper, tungsten, aluminum, silver, gold, or any other suitable materials or combinations thereof. Each electrical distribution layer **870**_a_, **870**_b_ has a thickness between about 40 μm and about 100 μm, such as a thickness between about 60 μm and about 80 μm. For example, each electrical distribution layer **870**_a_, **870**_b_ has a thickness of about 70 μm. The electrical distribution layers **870**_a_, **870**_b_ may have similar or different thicknesses relative to one another. Furthermore, although two electrical distribution layers **870**_a_, **870**_b_ are depicted, each PCB **850**_a_, **850**_b_ may have more or fewer electrical distribution layers formed on surfaces thereof. In other embodiments, the PCB's **850**_a_, **850**_b_ include conductive pads or other suitable electrical contacts for interconnection through the semiconductor device spacers **100**.

(67) The PCB's **850**_a_, **850**_b_ are conductively coupled to the semiconductor device spacers **100** by one or more solder bumps **840** disposed between the electrical contacts of the PCB's **850**_a_, **850**_b_ (e.g., electrical distribution layers **870**_a_, **870**_b_) and the interconnections **104** of the semiconductor device spacers **100**. In one embodiment, the solder bumps **840** are formed of a substantially similar material to that of the interconnections **104** and/or the electrical distribution layers **870**_a_, **870**_b_. For example, the solder bumps **840** are formed of a conductive material such as copper, tungsten, aluminum, silver, gold, or any other suitable materials or combinations thereof. Generally, the solder bumps **840** have a height B less than about 50 μm, such as a height B between about 5 μm

and about 45 μm, such as a height B between about 10 μm and about 30 μm. For example, the solder bumps **840** have a height B about 20 μm. Altogether, the semiconductor device spacers **100** with the solder bumps **840** create the physical space **820** with a height S between about 95 μm and about 5040 μm. Generally, the physical space **820** has a height S substantially similar to a thickness of the frame **102** of the semiconductor device spacers **100**.

(68) In one embodiment, the solder bumps **840** include C4 solder bumps. In a further embodiment, the solder bumps **840** include C2 (Cu-pillar with a solder cap) solder bumps. Utilization of C2 solder bumps may enable smaller pitch lengths and improved thermal and/or electrical properties for the PCB assembly **800**. The solder bumps **840** are formed by any suitable bumping processes, including but not limited to electrochemical deposition (ECD) electroplating, and metal diffusion bonding (e.g., gold to gold).

(69) In one embodiment, voids between the semiconductor device spacers **100** and the PBC's **850***a*, **850***b* are filled with an encapsulation material **848** to enhance the reliability of the solder bumps **840** disposed therein. The encapsulation material **848** is any suitable type of encapsulant or underfill and substantially surrounds the solder bumps **840**. In one example, the encapsulation material **848** includes a pre-assembly underfill material, such as a no-flow underfill (NUF) material, a nonconductive paste (NCP) material, and a nonconductive film (NCF) material. In one example, the encapsulation material **848** includes a post-assembly underfill material, such as a capillary underfill (CUF) material and a molded underfill (MUF) material. In one embodiment, the encapsulation material **848** includes a low-expansion-filler-containing resin, such as an epoxy resin filled with (e.g., containing) SiO.sub.2, AlN, Al.sub.2O.sub.3, SiC, Si.sub.3N.sub.4, Sr.sub.2Ce.sub.2Ti.sub.5O.sub.16, ZrSiO.sub.4, CaSiO.sub.3, BeO, CeO.sub.2, BN, CaCu.sub.3Ti.sub.4O.sub.12, MgO, TiO.sub.2, ZnO and the like.

(70) In another exemplary embodiment depicted in FIG. **9**, the semiconductor device spacers **100** are utilized in a PCB assembly **900**. The PCB assembly **900** is substantially similar to PCB assembly **800**, but includes a substrate **950** in place of one of the PCB's **850***a*, **850***b* described above. Thus, the semiconductor device spacers **100** may be utilized to interconnect and stack a single PCB **850** with the substrate **950**. Although only a single PCB **850** and a single substrate **950** are shown in FIG. **9**, it is contemplated the semiconductor device spacers **100** may be utilized to stack and interconnect any quantity and combination of PCB's **850** and/or substrates **950** in parallel. In some embodiments, two or more substrates **950** may be stacked and interconnected without the inclusion of a PCB **850**.

(71) The substrate **950** is any suitable type of substrate for use with electronic devices. In one embodiment, the substrate **950** is configured to function as a core structure for a semiconductor package, an interposer, an intermediate bridging connector, a PCB spacer, a chip carrier, or the like. Accordingly, the substrate **950** is formed of any suitable substrate material including but not limited to a III-V compound semiconductor material, silicon, crystalline silicon (e.g., Si<100> or Si<111>), silicon oxide, silicon germanium, doped or undoped silicon, doped or undoped polysilicon, silicon nitride, quartz, glass material (e.g., borosilicate glass), sapphire, alumina, and/or ceramic material. In one embodiment, the substrate **950** is a monocrystalline p-type or n-type silicon substrate. In one embodiment, the substrate **950** is a multicrystalline p-type or n-type silicon substrate. In another embodiment, the substrate **950** is a p-type or an n-type silicon solar substrate.

(72) In further embodiments, the substrate **950** further includes an optional passivating layer **905** formed on desired surfaces thereof, such as an oxide passivating layer **905**. For example, the substrate **950** may include a silicon oxide passivating layer **905** formed on substantially all surfaces thereof and thus, the passivating layer **905** substantially surrounds the substrate **950**. The passivating layer **905** provides a protective outer barrier for the substrate **950** against corrosion and other forms of damage. In some examples, the passivating layer **905** has a thickness between about 100 nm and about 3 μm, such as a thickness between about 200 nm and about 2.5 μm. In one example, the passivating layer **905** has a thickness between about 300 nm and about 2 μm, such as

a thickness of about 1.5 μm.

(73) The substrate **950** may further have a polygonal or circular shape. For example, the substrate **950** includes a substantially square silicon substrate having lateral dimensions between about 140 mm and about 180 mm, with or without chamfered edges. In another example, the substrate **950** includes a circular silicon containing wafer having a diameter between about 20 mm and about 700 mm, such as between about 100 mm and about 500 mm, for example about 300 mm. Unless otherwise noted, embodiments and examples described herein are conducted on substrates **950** having a thickness between about 50 μm and about 1000 μm, such as a thickness between about 90 μm and about 780 μm. For example, the substrate **950** has a thickness between about 100 μm and about 300 μm, such as a thickness between about 110 μm and about 200 μm.

(74) In some embodiments, the substrate **950** is a patterned substrate and includes one or more vias **903** formed therein to enable conductive electrical interconnections **904** to be routed therethrough. The vias **903** are formed as singular and isolated vias **903** through the substrate **950** or in one or more groupings or arrays, as depicted in FIG. **9**. In one embodiment, a minimum pitch between each via **903** is less than about 1000 μm, such as between about 25 μm and about 200 μm. For example, the pitch between vias **903** is between about 40 μm and about 150 μm.

(75) Generally, the one or more vias **903** are substantially cylindrical in shape. However, other suitable morphologies for the vias **903** are also contemplated. In one embodiment, the vias **903** and thus any interconnections **904** formed therein, have a diameter less than about 500 μm, such as a diameter less than about 250 μm. For example, the vias **903** and/or the interconnections **904** have a diameter between about 25 μm and about 100 μm, such as a diameter between about 30 μm and about 60 μm. In one embodiment, the vias **903** and/or the interconnections **904** have a diameter of about 40 μm.

(76) In one embodiment, the vias **903** and/or the interconnections **904** are formed through the entire thickness of the substrate **950**. For example, the vias **903** and/or the interconnections **904** have a longitudinal length corresponding to a total thickness of the substrate **950** between about 50 μm and about 1000 μm, such as a longitudinal length between about 200 μm and about 800 μm. In one example, the vias **903** and/or the interconnections **904** have a longitudinal length of between about 400 μm and about 600 μm, such as longitudinal length of about 500 μm. In another embodiment, the vias **903** and/or the interconnections **904** are only formed through a portion of the thickness of the substrate **950**. In further embodiments, the interconnections **904** protrude from one or more surfaces of the substrate **950**, as depicted in FIG. **9**. Similar to the interconnections **104**, the interconnections **904** are formed of any conductive materials used in the field of microelectronic devices, integrated circuits, circuit boards, and the like. For example, the interconnections **904** are formed of a metallic material, such as copper, aluminum, gold, nickel, silver, palladium, tin, or the like.

(77) In some embodiments, the substrate **950** further includes an adhesion layer **912** and/or a seed layer **914** formed over desired surfaces of the substrate **950** upon which the interconnections **904** are formed. For example, the adhesion layer **912** and/or the seed layer **914** are formed on the sidewalls **913** of the vias **903**. Generally, the adhesion layer **912** and/or the seed layer **914** are substantially similar in material and morphology to the adhesion layers **112**, **512** and the seed layers **114**, **514**. In some embodiments, the adhesion layer **912** and/or the seed layer **914** are formed over the passivating layer **905**, which is formed over the sidewalls **913** of the vias **903**.

(78) In some embodiments, the substrate **950** further includes one or more optional electrical distribution layers **970** disposed on desired surfaces thereof. In FIG. **9**, the electrical distribution layer **970** is disposed on a surface adjacent the physical space **820**, opposite the optional electrical distribution layer **870**, and in contact with the interconnections **904**. The electrical distribution layer **970** is formed of any suitable conductive material such as copper, tungsten, aluminum, silver, gold, or any other suitable materials or combinations thereof. In further embodiments, the substrate **950** may include conductive pads or other suitable electrical contacts for interconnection with the PCB

850 through the semiconductor device spacers **100**.
(79) In another exemplary embodiment depicted in FIG. **10**, the semiconductor device spacers **100** are utilized in a PCB assembly **1000**. The PCB assembly **1000** is substantially similar to PCB assembly **900**, but includes a semiconductor core assembly **1050** in place of the substrate **950** described above. Thus, the semiconductor device spacers **100** may be utilized to interconnect and stack a single PCB **850** with the semiconductor core assembly **1050**. Although only a single PCB **850** and a single semiconductor core assembly **1050** are shown in FIG. **10**, it is contemplated the semiconductor device spacers **100** may be utilized to stack and interconnect any quantity and combination of PCB's **850** and/or semiconductor core assemblies **1050** in parallel. In some embodiments, two or more semiconductor core assemblies **1050** may be stacked and interconnected without the inclusion of a PCB **850**.
(80) The semiconductor core assembly **1050** may be utilized for structural support and electrical interconnection of semiconductor packages. In other examples, the semiconductor core assembly **1050** may be utilized as a carrier structure for a surface-mounted device, such as a chip or graphics card. The semiconductor core assembly **1050** generally includes a core structure **1002**, an optional passivating layer **1005**, and an insulating layer **1016**.
(81) In one embodiment, the core structure **1002** includes a patterned (e.g., structured) substrate formed of any suitable substrate material. For example, the core structure **1002** includes a substrate formed from any of the materials described above with reference to substrate **950**. The substrate utilized to form the core structure **1002** may further have a polygonal or circular shape. For example, the core structure **1002** includes a substantially square silicon substrate having lateral dimensions between about 120 mm and about 180 mm, with or without chamfered edges. In another example, the core structure **1002** includes a circular silicon-containing wafer having a diameter between about 20 mm and about 700 mm, such as between about 100 mm and about 50 mm, for example about 300 mm. Unless otherwise noted, embodiments and examples described herein are conducted on substrates having a thickness between about 50 μm and about 1000 μm, such as a thickness between about 90 μm and about 780 μm. For example, the substrate utilized for the core structure **1002** has a thickness between about 100 μm and about 300 μm, such as a thickness between about 110 μm and about 200 μm.
(82) Similar to the substrate **950**, the core structure **1002** further includes one or more core vias **1003** formed therein to enable conductive electrical interconnections to be routed through the core structure **1002**. The core vias **1003** are formed as singular and isolated core vias **1003** through the core structure **1002** or in one or more groupings or arrays. In one embodiment, a minimum pitch between each core via **1003** is less than about 1000 μm, such as between about 25 μm and about 200 μm. For example, the pitch is between about 40 μm and about 150 μm. In one embodiment, the one or more core vias **1003** have a diameter less than about 500 μm, such as a diameter less than about 250 μm. For example, the core vias **1003** have a diameter between about 25 μm and about 100 μm, such as a diameter between about 30 μm and about 60 μm. In one embodiment, the core vias **1003** have a diameter of about 40 μm.
(83) The optional passivating layer **1005** is similar to the passivating layer **905** and is formed on one or more surfaces of the core structure **1002**, including the one or more sidewalls **1013** of the core vias **1003**. In one embodiment, the passivating layer **1005** is formed on substantially all exterior surfaces of the core structure **1002** such that the passivating layer **1005** substantially surrounds the core structure **1002**. In one embodiment, the passivating layer **1005** is formed of an oxide film or layer, such as a thermal oxide layer. For example, the passivating layer **1005** may be a silicon oxide layer. In some examples, the passivating layer **1005** has a thickness between about 100 nm and about 3 μm, such as a thickness between about 200 nm and about 2.5 μm. In one example, the passivating layer **1005** has a thickness between about 300 nm and about 2 μm, such as a thickness of about 1.5 μm.
(84) The insulating layer **1016** is formed on one or more surfaces of the core structure **1002** or the

passivating layer **1005** and substantially encases the passivating layer **1005** and/or the core structure **1002**. Thus, the insulating layer **1016** extends into the core vias **803** and coat the passivating layer **1005** formed on the sidewalls **1013** thereof or directly coat the core structure **1002**. In one embodiment, the insulating layer **1016** has a thickness from an outer surface of the core structure **1002** or the passivating layer **1005** to an adjacent outer surface of the insulating layer **1016** that is less than about 50 μm, such as a thickness less than about 20 μm. For example, the insulating layer **1016** has thickness between about 5 μm and about 10 μm.

(85) In one embodiment, the insulating layer **1016** is formed of polymer-based dielectric materials, similar to the frame **102** of semiconductor device spacers **100**. For example, the insulating layer **1016** is formed from a flowable build-up material. Accordingly, although hereinafter referred to as an "insulating layer," the insulating layer **1016** may also be described as a dielectric layer. In a further embodiment, the insulating layer **1016** is formed of an epoxy resin material having a ceramic filler, such as silica (SiO.sub.2) particles. Other examples of ceramic fillers that may be utilized to form the insulating layer **1016** include aluminum nitride (AlN), aluminum oxide (Al.sub.2O.sub.3), silicon carbide (SiC), silicon nitride (Si.sub.3N.sub.4), Sr.sub.2Ce.sub.2Ti.sub.5O.sub.16, zirconium silicate (ZrSiO.sub.4), wollastonite (CaSiO.sub.3), beryllium oxide (BeO), cerium dioxide (CeO.sub.2), boron nitride (BN), calcium copper titanium oxide (CaCu.sub.3Ti.sub.4O.sub.12), magnesium oxide (MgO), titanium dioxide (TiO.sub.2), zinc oxide (ZnO) and the like. In some examples, the ceramic fillers utilized to form the insulating layer **1016** have particles ranging in diameter between about 40 nm and about 1.5 μm, such as between about 80 nm and about 1 μm. For example, the ceramic fillers have particles with a diameter between about 200 nm and about 800 nm, such as between about 300 nm and about 600 nm. In some embodiments, the ceramic fillers include particles having a diameter less than about 10% of the width or diameter of adjacent core vias **1003** in the core structure **1002**, such as a diameter less than about 5% of the width or diameter of the core vias **1003**.

(86) One or more through-assembly vias **1023** are formed through the insulating layer **1016** where the insulating layer **1016** extends into the core vias **1003** to enable electrical interconnections **1004** to be routed therethrough. For example, the through-assembly vias **1023** are centrally formed within the core vias **1003** having the insulating layer **1016** disposed therein. Accordingly, the insulating layer **1016** forms one or more sidewalls of the through-assembly vias **1023**, wherein the through-assembly vias **1023** have a diameter lesser than the diameter of the core vias **1003**. In one embodiment, the through-assembly vias **1023** have a diameter less than about 100 μm, such as less than about 75 μm. For example, the through-assembly vias **1023** have a diameter less than about 50 μm, such as less than about 35 μm. In one embodiment, the through-assembly vias **1023** have a diameter of between about 25 μm and about 50 μm, such as a diameter of between about 35 μm and about 40 μm.

(87) In one embodiment, the interconnections **1004**, and thus the through-assembly vias **1023** and the core vias **1003**, are formed through the entire thickness of the semiconductor core assembly **1050**. For example, the interconnections **1004** and/or the through-assembly vias **1023** and/or the core vias **1003** have a longitudinal length corresponding to a total thickness of the semiconductor core assembly **1050** between about 50 μm and about 1000 μm, such as a longitudinal length between about 200 μm and about 800 μm. In one example, the interconnections **1004** and/or the through-assembly vias **1023** and/or the core vias **1003** have a longitudinal length of between about 400 μm and about 600 μm, such as longitudinal length of about 500 μm. In another embodiment, the interconnections **1004** and/or the through-assembly vias **1023** and/or the core vias **1003** are only formed through a portion of the thickness of the semiconductor core assembly **1050**. In further embodiments, the interconnections **1004** protrude from one or more surfaces of the semiconductor core assembly **1050**, as depicted in FIG. **10**. Similar to the interconnections described above, the interconnections **1004** are formed of any conductive materials used in the field of integrated circuits, circuit boards, chip carriers, and the like. For example, the electrical interconnections **1004**

are formed of a metallic material, such as copper, aluminum, gold, nickel, silver, palladium, tin, or the like.

(88) In some embodiments, the semiconductor core assembly **1050** further includes an adhesion layer **1012** and/or a seed layer **1014** formed on desired surfaces of the insulating layer **1016** upon which the interconnections **1004** are formed. For example, the adhesion layer **1012** and/or the seed layer **1014** are formed on the sidewalls of the through-assembly vias **1003**. Generally, the adhesion layer **1012** and/or the seed layer **1014** are substantially similar in material and morphology to the adhesion layers **112**, **512** and the seed layers **114**, **514**.

(89) In some embodiments, the semiconductor core assembly **1050** further includes one or more optional electrical distribution layers **1070** disposed on desired surfaces thereof. In FIG. **10**, the electrical distribution layer **1070** is disposed on a surface adjacent the physical space **820**, opposite the optional electrical distribution layer **870**, and in contact with the interconnections **1004** and solder bumps **840**. The electrical distribution layer **1070** are formed of any suitable conductive material such as copper, tungsten, aluminum, silver, gold, or any other suitable materials or combinations thereof. In further embodiments, the semiconductor core assembly **1050** may include conductive pads or other suitable electrical contacts for interconnection with the PCB **850** through the semiconductor device spacers **100**.

(90) FIGS. **11**A-**11**E schematically illustrate top views of possible arrangements of the semiconductor device spacers **100** when coupled to at least a single device, such as the PCB **850**, according to the descriptions of FIGS. **8-10** above. Generally, the semiconductor device spacers **100** may be disposed between adjacent PCB's or other devices in any suitable quantity and arrangement. As depicted in FIG. **11**A, two semiconductor device spacers **100** are disposed on a top surface of the PCB **850** along edges of opposing ends thereof. FIG. **11**B illustrates three semiconductor device spacers **100** disposed along three edges of the top surface of PCB **850** and FIG. **11**C illustrates four semiconductor device spacers **100** disposed along all four edges of the top surface of PCB **850**. In an alternative example, FIG. **11**D illustrates a single semiconductor device spacer **100** medially disposed along the top surface of the PCB **850** and extending from one edge to an opposing edge thereof.

(91) FIGS. **11**A-**11**D depict exemplary arrangements wherein one or more semiconductor device spacers **100** have a lateral dimension spanning the length of one or more edges (e.g., sides) of an adjacent device. FIG. **11**E depicts an alternative exemplary arrangement wherein one or more semiconductor device spacers **100** have dimensions less than the lengths of the sides of the adjacent device. As shown in FIG. **11**E, two semiconductor device spacers **100** are medially disposed along the top surface of the PCB **850**, each semiconductor device spacer **100** having a lateral dimensions substantially less than lengths of the sides of PCB **850**. In some embodiments, the ratio of area of the semiconductor device spacers **100** relative to the area of the PCB **850** is between about 0.01 and about 0.99, such as between about 0.05 and about 0.95. For example, the ratio of area of the semiconductor device spacers **100** relative to the area of the PCB **850** is between about 0.1 and about 0.9, such as between about 0.15 and about 0.85.

(92) The utilization of the semiconductor device spacers **100** in the embodiments shown above provides multiple advantages over the spacers utilized in conventional stacked package, PCB, and chip carrier structures. Such benefits include improved thermal management for improved electrical performance and reliability of stacked device architectures. The improved thermal conductivity of these spacers, as well as the ability to pattern fine features therein, further enables thin-form-factor structures with greater **1**/O scaling to meet the ever-increasing bandwidth and power efficiency demands of artificial intelligence (AI) and high performance computing (HPC). Additionally, the fabrication methods for the semiconductor device spacers described herein provide high performance and flexibility for 3D integration with relatively low manufacturing costs as compared to conventional spacer and stacking technologies.

(93) While the foregoing is directed to embodiments of the present disclosure, other and further

embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

Claims

1. A semiconductor device assembly, comprising: a first printed circuit board (PCB) comprising: a first glass fiber reinforced epoxy resin material; and a first electrical distribution layer formed on the first glass fiber reinforced epoxy resin material; a second PCB comprising: a second glass fiber reinforced epoxy resin material; and a second electrical distribution layer formed on the second glass fiber reinforced epoxy resin material; and a device spacer interposed between the first PCB and the second PCB to facilitate a physical space therebetween, the device spacer further comprising: a frame having a first surface opposite a second surface, the frame further comprising: a frame material comprising a polymer-based dielectric material having ceramic filler particles; and a via comprising a via surface that defines an opening extending through the frame from the first surface to the second surface, the via having a first diameter of about 10 μm and about 150 μm; an electrical interconnection disposed within the via on the via surface to form at least part of a conductive path extending between at least a portion of the first and second electrical distribution layers; and solder bumps conductively coupling the electrical interconnection with the first and second electrical distribution layers.
2. The semiconductor device assembly of claim 1, wherein the ceramic filler particles comprise silica particles having a maximum diameter of about 0.6 μm.
3. The semiconductor device assembly of claim 2, wherein a packing density of the silica particles is between about 0.5 and about 0.95 by volume.
4. The semiconductor device assembly of claim 1, wherein the frame has a thickness between about 400 μm and about 1600 μm.
5. The semiconductor device assembly of claim 1, wherein the solder bumps have a maximum height of about 50 μm.
6. The semiconductor device assembly of claim 1, further comprising an encapsulation material substantially surrounding the solder bumps.
7. The semiconductor device assembly of claim 1, wherein a ratio of an area of the device spacer relative to an area of a surface of the first or second PCB is between about 0.15 and about 0.85.
8. The semiconductor device assembly of claim 1, further comprising a silicon substrate comprising a silicon core structure, the silicon core structure having a thickness less than 1000 μm.
9. The semiconductor device assembly of claim 8, wherein the second electrical distribution layer is formed on the silicon core structure and surrounds the silicon core structure.
10. The semiconductor device assembly of claim 1, wherein the frame further comprises a lateral dimension that is less than a lateral dimension of the first PCB and the second PCB.
11. The semiconductor device assembly of claim 1, further comprising a barrier layer lining the via surface and disposed between the via surface and the electrical interconnection.
12. The semiconductor device assembly of claim 11, wherein the barrier layer comprises molybdenum.
13. The semiconductor device assembly of claim 1, wherein the via is tapered from a second diameter to the first diameter.
14. The semiconductor device assembly of claim 13, wherein the second diameter is between about 0 μm and about 100 μm.
15. The semiconductor device assembly of claim 1, wherein the device spacer further comprises an array of vias defining openings extending through the frame from the first surface to the second surface.

16. The semiconductor device assembly of claim 15, wherein a pitch between each via of the array of vias is between about 150 μm and about 600 μm.