

(54) **SELECTIVE ETCHING OF SILICON-AND-GERMANIUM-CONTAINING MATERIALS WITH REDUCED UNDER LAYER LOSS**

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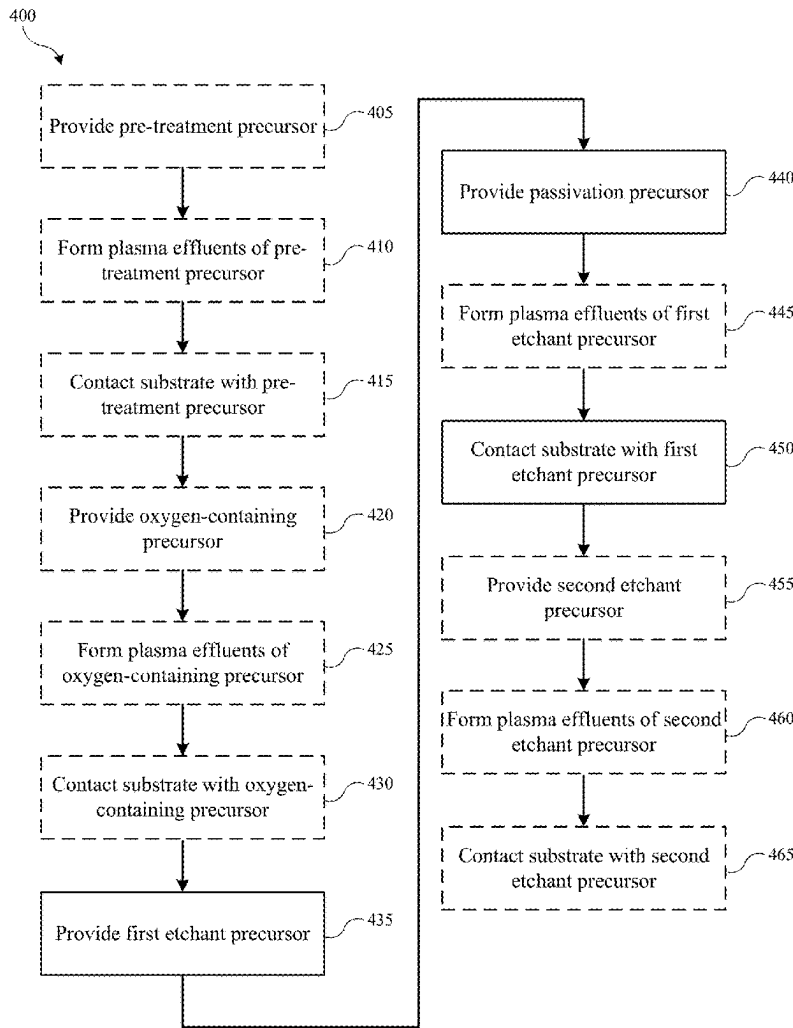
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(57) **ABSTRACT**

Exemplary semiconductor processing methods may include providing a first etchant precursor to a processing region of a semiconductor processing chamber. A substrate may be housed within the processing region. A first layer of silicon-and-germanium-containing material, a second layer of silicon-and-germanium-containing material, and a layer of silicon-containing material may be disposed on the substrate. The methods may include providing a passivation precursor to the processing region. The methods may include contacting the substrate with the first etchant precursor and the passivation precursor. The contacting may selectively etch the first layer of silicon-and-germanium-containing material. The contacting may form a passivation material on the substrate.



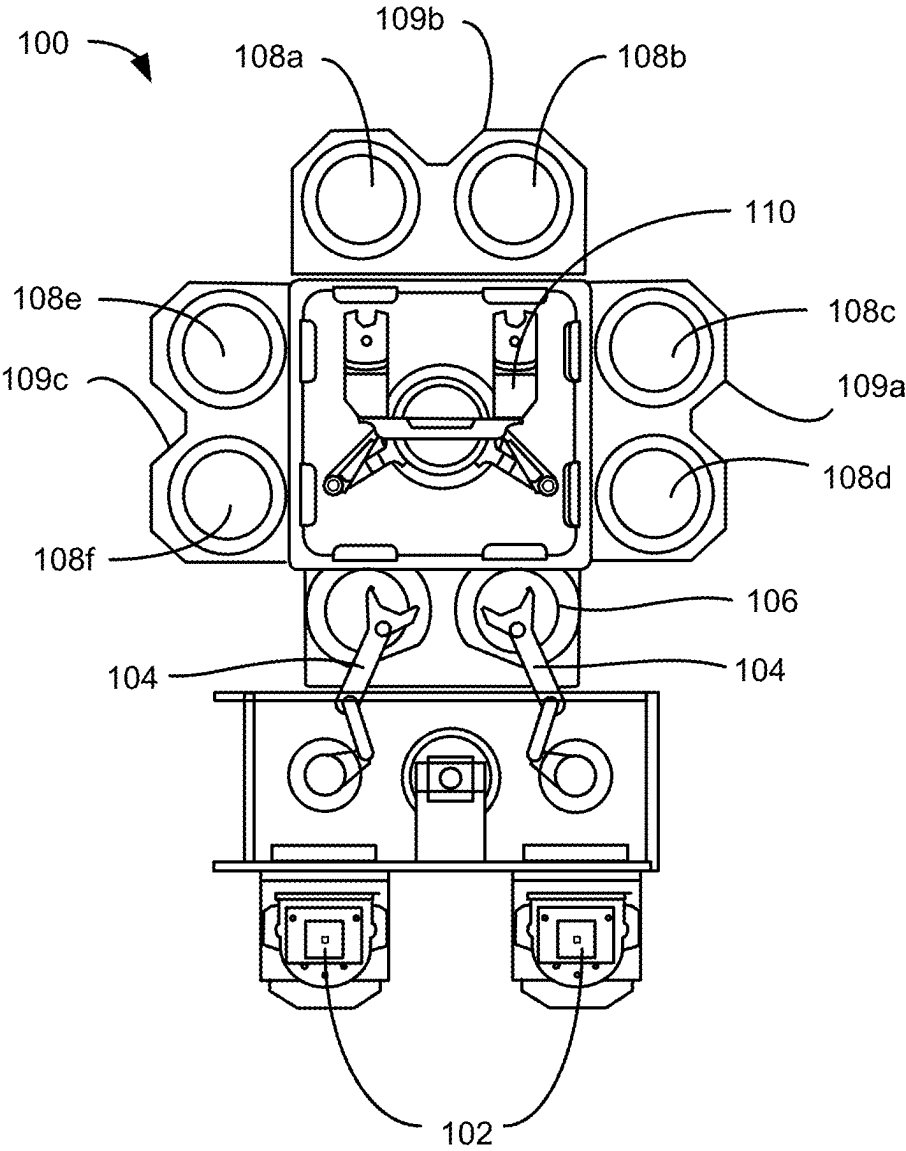
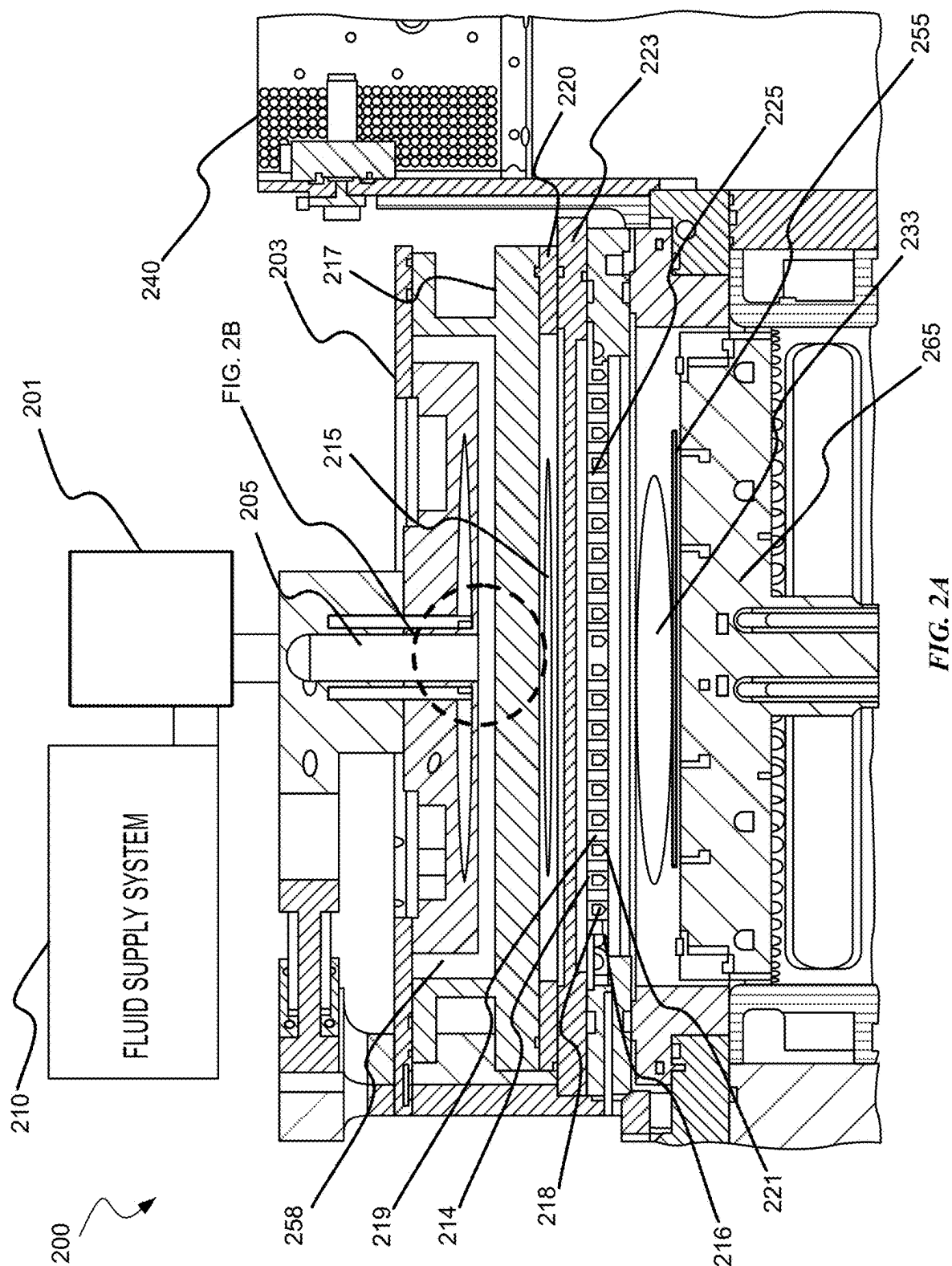


FIG. 1



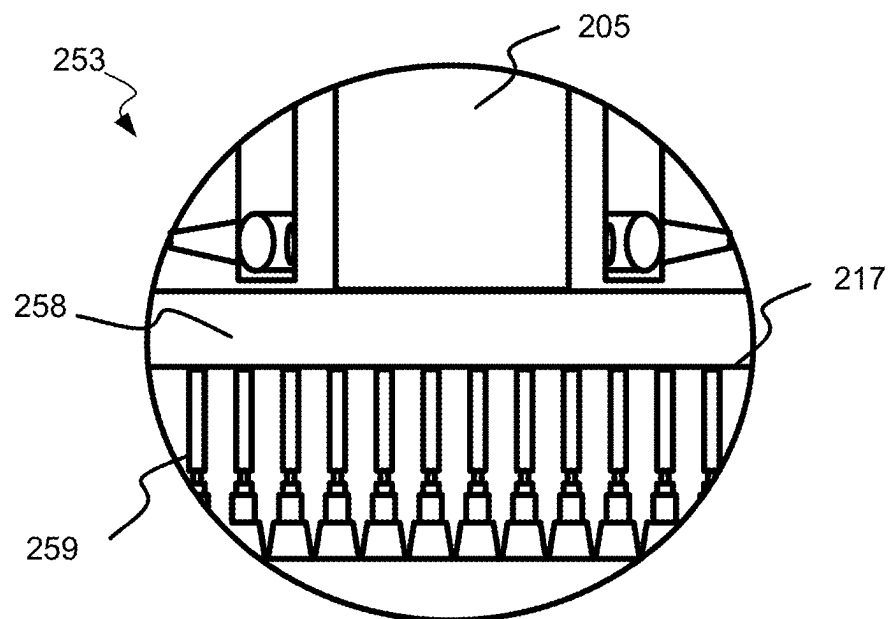


FIG. 2B

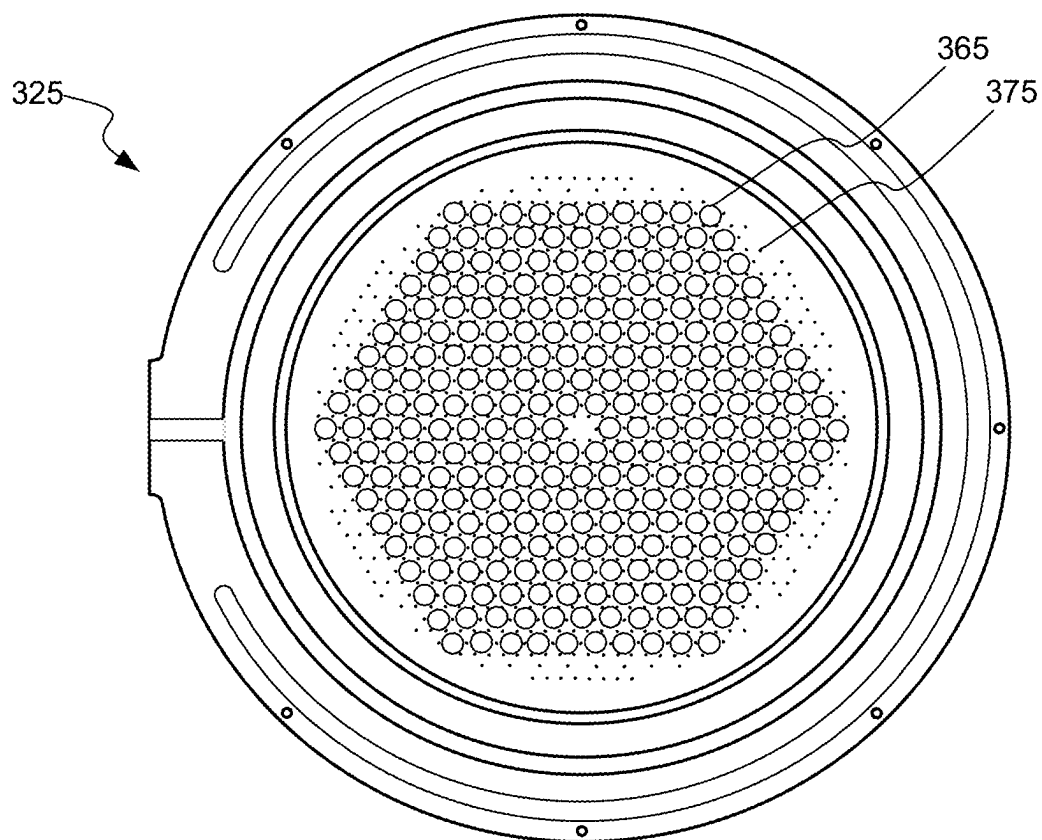


FIG. 3

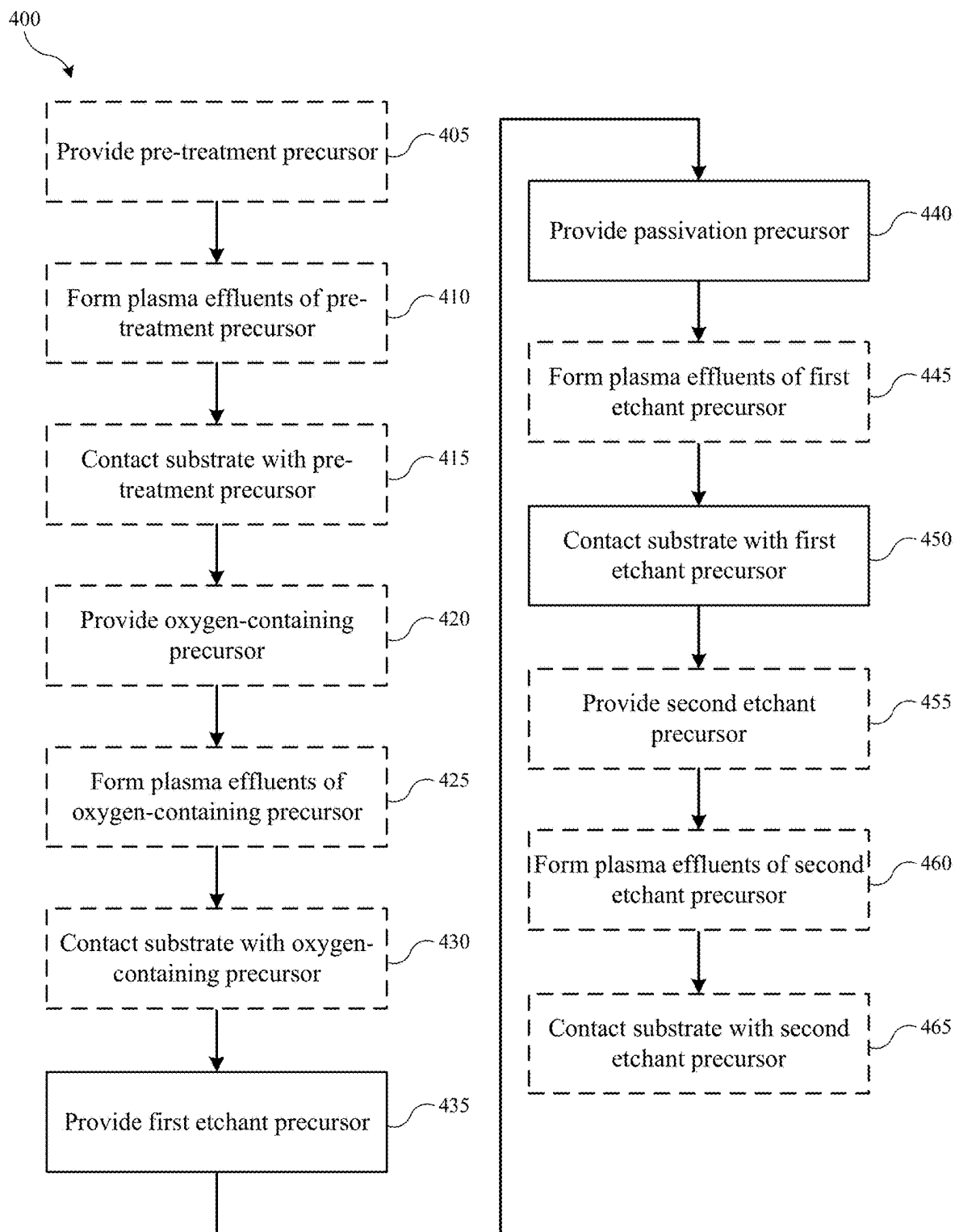


FIG. 4

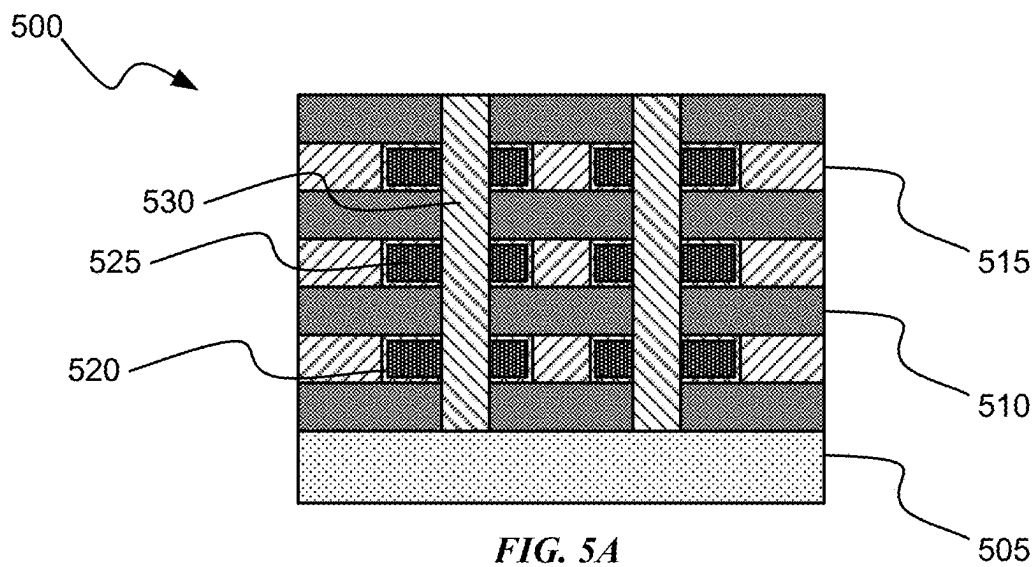


FIG. 5A

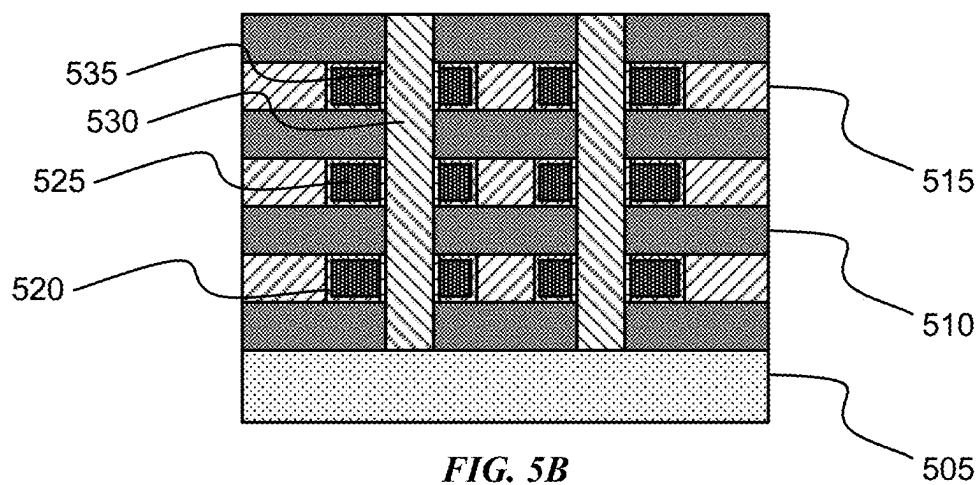
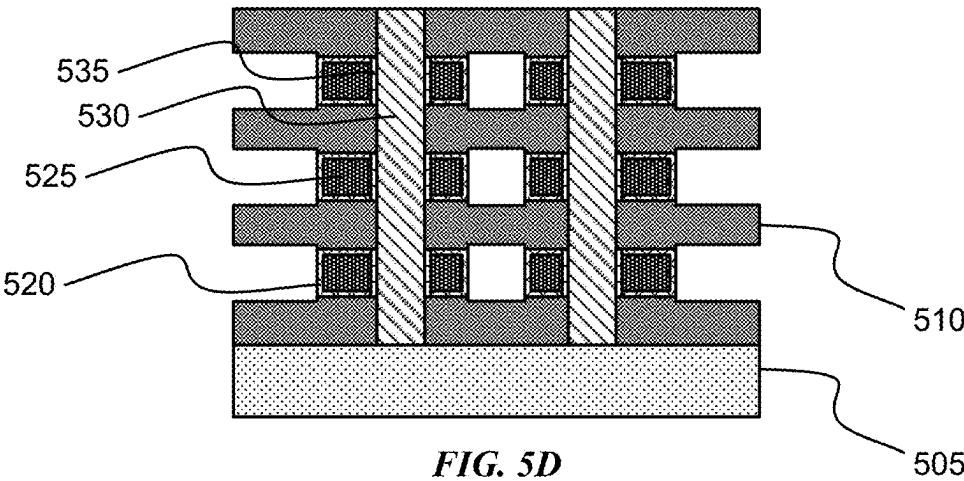
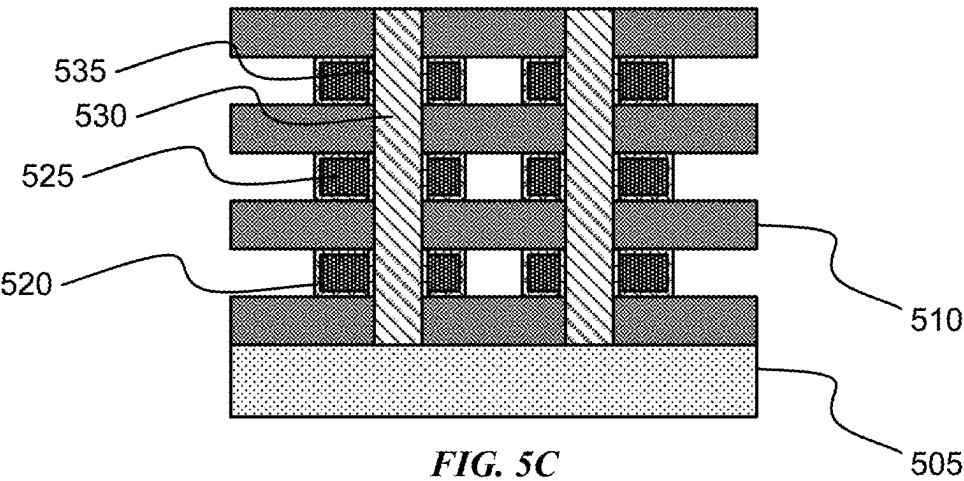


FIG. 5B



**SELECTIVE ETCHING OF  
SILICON-AND-GERMANIUM-CONTAINING  
MATERIALS WITH REDUCED UNDER  
LAYER LOSS**

**CROSS-REFERENCE TO RELATED  
APPLICATIONS**

**[0001]** This application claims the benefit of, and priority to U.S. Provisional Application Ser. No. 63/552,548, filed Feb. 12, 2024, which is hereby incorporated by reference in its entirety for all purposes.

**TECHNICAL FIELD**

**[0002]** The present technology relates to semiconductor processes and equipment. More specifically, the present technology relates to selectively etching silicon-and-germanium-containing material in vertical structures.

**BACKGROUND**

**[0003]** Integrated circuits are made possible by processes which produce intricately patterned material layers on substrate surfaces. Producing patterned material on a substrate requires controlled methods for removal of exposed material. Chemical etching is used for a variety of purposes including transferring a pattern in photoresist into underlying layers, thinning layers, or thinning lateral dimensions of features already present on the surface. Often it is desirable to have an etch process that etches one material faster than another facilitating, for example, a pattern transfer process. Such an etch process is said to be selective to the first material. As a result of the diversity of materials, circuits, and processes, etch processes have been developed with a selectivity towards a variety of materials.

**[0004]** Etch processes may be termed wet or dry based on the materials used in the process. A wet HF etch preferentially removes silicon oxide over other dielectrics and materials. However, wet processes may have difficulty penetrating some constrained trenches and also may sometimes deform the remaining material. Dry etches produced in local plasmas formed within the substrate processing region can penetrate more constrained trenches and exhibit less deformation of delicate remaining structures. However, local plasmas may damage the substrate through the production of electric arcs as they discharge.

**[0005]** Thus, there is a need for improved systems and methods that can be used to produce high quality devices and structures. These and other needs are addressed by the present technology.

**SUMMARY**

**[0006]** Exemplary semiconductor processing methods may include providing a first etchant precursor to a processing region of a semiconductor processing chamber. A substrate may be housed within the processing region. A first layer of silicon-and-germanium-containing material, a second layer of silicon-and-germanium-containing material, and a layer of silicon-containing material may be disposed on the substrate. The methods may include providing a passivation precursor to the processing region. The methods may include contacting the substrate with the first etchant precursor and the passivation precursor. The contacting may

selectively etch the first layer of silicon-and-germanium-containing material. The contacting may form a passivation material on the substrate.

**[0007]** In some embodiments, the first layer of silicon-and-germanium-containing material may be characterized by a first germanium concentration. The second layer of silicon-and-germanium-containing material may be characterized by a second germanium concentration. The first germanium concentration may be less than the second germanium concentration. The passivation precursor may be or include a fluorine-and-carbon-containing precursor. The passivation precursor may be or include perfluoropentane ( $C_5F_{12}$ ). The methods may include forming plasma effluents of the first etchant precursor, the passivation precursor, or both. The first etchant precursor may be or include a fluorine-containing precursor. The methods may include providing an inert gas with the first etchant precursor, the passivation precursor, or both. The passivation precursor may be characterized by a boiling point of less than or about  $100^\circ\text{C}$ . The passivation precursor may be characterized by a vapor pressure at  $25^\circ\text{C}$ . of less than or about 100 kPa. A pressure in the processing region may be maintained at less than or about 30 Torr. A temperature in the processing region may be maintained at less than or about  $150^\circ\text{C}$ .

**[0008]** Some embodiments of the present technology may encompass semiconductor processing methods. The methods may include providing an oxygen-containing precursor to a processing region of a semiconductor processing chamber. A substrate may be housed within the processing region. A first layer of silicon-and-germanium-containing material, a second layer of silicon-and-germanium-containing material, and a layer of silicon-containing material may be disposed on the substrate. The first layer of silicon-and-germanium-containing material may be characterized by a lesser germanium concentration than the second layer of silicon-and-germanium-containing material. The methods may include contacting the substrate with the oxygen-containing precursor. The contacting may oxidize at least a portion of the second layer of silicon-and-germanium-containing material. The methods may include providing a first fluorine-containing precursor to the processing region. The methods may include providing a fluorine-and-carbon-containing precursor to the processing region. The methods may include contacting the substrate with the first fluorine-containing precursor and the fluorine-and-carbon-containing precursor. The contacting may etch the first layer of silicon-and-germanium-containing material relative to the second layer of silicon-and-germanium-containing material while preventing etching of the second layer of silicon-and-germanium-containing material.

**[0009]** In some embodiments, the fluorine-and-carbon-containing precursor may be or include perfluoropentane ( $C_5F_{12}$ ). A flow rate of the fluorine-and-carbon-containing precursor may be less than a flow rate of the first fluorine-containing precursor. A flow rate of the fluorine-and-carbon-containing precursor may be less than or about 1,000 sccm. The methods may include forming plasma effluents of the first fluorine-containing precursor. The contacting may etch the first layer of silicon-and-germanium-containing material relative to the second layer of silicon-and-germanium-containing material at a selectivity of greater than or about 40:1.

**[0010]** Some embodiments of the present technology may encompass semiconductor processing methods. The methods may include providing a first fluorine-containing pre-



cursor to a processing region of a semiconductor processing chamber. A substrate may be housed within the processing region. A first layer of silicon-and-germanium-containing material, a second layer of silicon-and-germanium-containing material, and a layer of silicon-containing material may be disposed on the substrate. The first layer of silicon-and-germanium-containing material may be characterized by a lesser germanium concentration than the second layer of silicon-and-germanium-containing material. The methods may include providing a fluorine-and-carbon-containing precursor to the processing region. The methods may include contacting the substrate with the first fluorine-containing precursor and the fluorine-and-carbon-containing precursor. The contacting may selectively etch the first layer of silicon-and-germanium-containing material while preventing etching of the second layer of silicon-and-germanium-containing material. The methods may include providing a second fluorine-containing precursor and a hydrogen-containing precursor to the processing region. The methods may include forming plasma effluents of the second fluorine-containing precursor and the hydrogen-containing precursor. The methods may include contacting the substrate with the plasma effluents of the second fluorine-containing precursor and the hydrogen-containing precursor. The contacting may etch a portion of the layer of silicon-containing material.

**[0011]** In some embodiments, a flow rate ratio of the first fluorine-containing precursor to the fluorine-and-carbon-containing precursor may be greater than or about 1:1. The fluorine-and-carbon-containing precursor may be or include perfluoropentane ( $C_5F_{12}$ ).

**[0012]** Such technology may provide numerous benefits over conventional systems and techniques. For example, the processes may selectively etch one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material. Additionally, the presence of a passivation precursor may serve as a blocking agent to prevent undesired etching of material(s) underlying the silicon-and-germanium-containing material to be etched. These and other embodiments, along with many of their advantages and features, are described in more detail in conjunction with the below description and attached figures.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0013]** A further understanding of the nature and advantages of the disclosed technology may be realized by reference to the remaining portions of the specification and the drawings.

**[0014]** FIG. 1 shows a top plan view of one embodiment of an exemplary processing system according to embodiments of the present technology.

**[0015]** FIG. 2A shows a schematic cross-sectional view of an exemplary processing chamber according to embodiments of the present technology.

**[0016]** FIG. 2B shows a detailed view of a portion of the processing chamber illustrated in FIG. 2A according to embodiments of the present technology.

**[0017]** FIG. 3 shows a bottom plan view of an exemplary showerhead according to embodiments of the present technology.

**[0018]** FIG. 4 shows exemplary operations in a method according to embodiments of the present technology.

**[0019]** FIGS. 5A-5D show cross-sectional views of substrates being processed according to embodiments of the present technology.

**[0020]** Several of the figures are included as schematics. It is to be understood that the figures are for illustrative purposes, and are not to be considered of scale unless specifically stated to be of scale. Additionally, as schematics, the figures are provided to aid comprehension and may not include all aspects or information compared to realistic representations, and may include superfluous or exaggerated material for illustrative purposes.

**[0021]** In the appended figures, similar components and/or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a letter that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the letter.

#### DETAILED DESCRIPTION

**[0022]** In transitioning to gate-all-around (GAA) transistors, many process operations are modified from more conventional fin field-effect (FinFET) transistors. Additionally, as structures continue to reduce in size, the thicknesses of material layers reduce and the aspect ratios of memory holes and other structures increase, sometimes dramatically.

**[0023]** During GAA processing, alternating layers of material are deposited on a substrate, such as alternating layers of silicon-containing material and silicon-and-germanium-containing material. In forming the transistor, memory holes or trenches may be formed through the alternating layers of material. During GAA processing, the silicon-and-germanium-containing material may be recessed from within the memory holes or trenches to form material that will serve as nanowires/nanosheets. Subsequent recessing one or more materials, including another silicon-and-germanium-containing material, may be formed within the recesses and/or memory holes or trenches.

**[0024]** Because of the similar materials in some GAA transistors, selectively removing one material relative to another material may become increasingly difficult. For example, multiple silicon-containing materials, including multiple silicon-and-germanium-containing materials may be used in GAA processing. In some operations, it may be desirable to remove one silicon-and-germanium-containing material, such as silicon-and-germanium-containing nanowires, relative to epitaxial silicon-and-germanium-containing material and other silicon-containing materials. Conventional technologies have struggled with selectively removing one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material. The non-selective removal may result in undesirable etching of some material, such as epitaxial silicon-and-germanium-containing material.

**[0025]** The present technology may overcome these issues by performing a selective oxidation prior to etching silicon-and-germanium-containing material, such as the silicon-and-germanium-containing nanowires. The selective oxidation may preferentially oxidize silicon-and-germanium-containing material characterized by a higher germanium concentration, such as the epitaxial silicon-and-germanium-containing material. The oxidized silicon-and-germanium-containing material may be more resistant to etching com-

pared to the non-oxidized silicon-and-germanium-containing material. Therefore, a subsequent etching operation to remove the silicon-and-germanium-containing material characterized by a lower germanium concentration may selectively remove the lower concentration material relative to the higher concentration material. The present technology may also overcome these issues by providing a passivation precursor with the etchant precursor. The passivation precursor may prevent etchant species from reaching material(s), such as the silicon-and-germanium-containing material to be maintained, underlying the silicon-and-germanium material to be etched. Thus, the etching operations of the present technology may successfully remove one silicon-and-germanium-containing material while maintaining another silicon-and-germanium-containing material in addition to other silicon-containing materials.

[0026] Although the remaining disclosure will routinely identify specific etching processes utilizing the disclosed technology, it will be readily understood that the systems and methods are equally applicable to etching processes as may occur in the described chambers. Accordingly, the technology should not be considered to be so limited as for use with etching processes or chambers alone. Moreover, although an exemplary chamber is described to provide foundation for the present technology, it is to be understood that the present technology can be applied to virtually any semiconductor processing chamber that may allow the operations described.

[0027] FIG. 1 shows a top plan view of one embodiment of a processing system 100 of deposition, etching, baking, and curing chambers according to embodiments. In the figure, a pair of front opening unified pods (FOUPs) 102 supply substrates of a variety of sizes that are received by robotic arms 104 and placed into a low pressure holding area 106 before being placed into one of the substrate processing chambers 108a-f, positioned in tandem sections 109a-c. A second robotic arm 110 may be used to transport the substrate wafers from the holding area 106 to the substrate processing chambers 108a-f and back. Each substrate processing chamber 108a-f, can be outfitted to perform a number of substrate processing operations including the dry etch processes described herein in addition to cyclical layer deposition (CLD), atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), etch, pre-clean, degas, orientation, and other substrate processes.

[0028] The substrate processing chambers 108a-f may include one or more system components for depositing, annealing, curing and/or etching a dielectric film on the substrate wafer. In one configuration, two pairs of the processing chambers, e.g., 108c-d and 108e-f, may be used to deposit dielectric material on the substrate, and the third pair of processing chambers, e.g., 108a-b, may be used to etch the deposited dielectric. In another configuration, all three pairs of chambers, e.g., 108a-f, may be configured to etch a dielectric film on the substrate. Any one or more of the processes described may be carried out in chamber(s) separated from the fabrication system shown in different embodiments. It will be appreciated that additional configurations of deposition, etching, annealing, and curing chambers for dielectric films are contemplated by system 100.

[0029] FIG. 2A shows a cross-sectional view of an exemplary process chamber system 200 with partitioned plasma generation regions within the processing chamber. During

film etching, e.g., titanium nitride, tantalum nitride, tungsten, silicon, polysilicon, silicon oxide, silicon nitride, silicon oxynitride, silicon oxycarbide, etc., a process gas may be flowed into the first plasma region 215 through a gas inlet assembly 205. A remote plasma system (RPS) 201 may optionally be included in the system, and may process a first gas which then travels through gas inlet assembly 205. The inlet assembly 205 may include two or more distinct gas supply channels where the second channel (not shown) may bypass the RPS 201, if included.

[0030] A cooling plate 203, faceplate 217, ion suppressor 223, showerhead 225, and a pedestal 265, having a substrate 255 disposed thereon, are shown and may each be included according to embodiments. The pedestal 265 may have a heat exchange channel through which a heat exchange fluid flows to control the temperature of the substrate, which may be operated to heat and/or cool the substrate or wafer during processing operations. The wafer support platter of the pedestal 265, which may comprise aluminum, ceramic, or a combination thereof, may also be resistively heated in order to achieve relatively high temperatures, such as from up to or about 100° C. to above or about 1100° C., using an embedded resistive heater element.

[0031] The faceplate 217 may be pyramidal, conical, or of another similar structure with a narrow top portion expanding to a wide bottom portion. The faceplate 217 may additionally be flat as shown and include a plurality of through-channels used to distribute process gases. Plasma generating gases and/or plasma excited species, depending on use of the RPS 201, may pass through a plurality of holes, shown in FIG. 2B, in faceplate 217 for a more uniform delivery into the first plasma region 215.

[0032] Exemplary configurations may include having the gas inlet assembly 205 open into a gas supply region 258 partitioned from the first plasma region 215 by faceplate 217 so that the gases/species flow through the holes in the faceplate 217 into the first plasma region 215. Structural and operational features may be selected to prevent significant backflow of plasma from the first plasma region 215 back into the supply region 258, gas inlet assembly 205, and fluid supply system 210. The faceplate 217, or a conductive top portion of the chamber, and showerhead 225 are shown with an insulating ring 220 located between the features, which allows an AC potential to be applied to the faceplate 217 relative to showerhead 225 and/or ion suppressor 223. The insulating ring 220 may be positioned between the faceplate 217 and the showerhead 225 and/or ion suppressor 223 enabling a capacitively coupled plasma (CCP) to be formed in the first plasma region. A baffle (not shown) may additionally be located in the first plasma region 215, or otherwise coupled with gas inlet assembly 205, to affect the flow of fluid into the region through gas inlet assembly 205.

[0033] The ion suppressor 223 may comprise a plate or other geometry that defines a plurality of apertures throughout the structure that are configured to suppress the migration of ionically-charged species out of the first plasma region 215 while allowing uncharged neutral or radical species to pass through the ion suppressor 223 into an activated gas delivery region between the suppressor and the showerhead. In embodiments, the ion suppressor 223 may comprise a perforated plate with a variety of aperture configurations. These uncharged species may include highly reactive species that are transported with less reactive carrier gas through the apertures. As noted above, the migration of

ionic species through the holes may be reduced, and in some instances completely suppressed. Controlling the amount of ionic species passing through the ion suppressor **223** may advantageously provide increased control over the gas mixture brought into contact with the underlying wafer substrate, which in turn may increase control of the deposition and/or etch characteristics of the gas mixture. For example, adjustments in the ion concentration of the gas mixture can significantly alter its etch selectivity, e.g.,  $\text{SiGe}_x\text{:SiO}_x$  etch ratios,  $\text{SiGe}_x\text{:Si}$  etch ratios, etc. In alternative embodiments in which deposition is performed, it can also shift the balance of conformal-to-flowable style depositions for dielectric materials.

**[0034]** The plurality of apertures in the ion suppressor **223** may be configured to control the passage of the activated gas, i.e., the ionic, radical, and/or neutral species, through the ion suppressor **223**. For example, the aspect ratio of the holes, or the hole diameter to length, and/or the geometry of the holes may be controlled so that the flow of ionically-charged species in the activated gas passing through the ion suppressor **223** is reduced. The holes in the ion suppressor **223** may include a tapered portion that faces the plasma region **215**, and a cylindrical portion that faces the showerhead **225**. The cylindrical portion may be shaped and dimensioned to control the flow of ionic species passing to the showerhead **225**. An adjustable electrical bias may also be applied to the ion suppressor **223** as an additional means to control the flow of ionic species through the suppressor.

**[0035]** The ion suppressor **223** may function to reduce or eliminate the amount of ionically charged species traveling from the plasma generation region to the substrate. Uncharged neutral and radical species may still pass through the openings in the ion suppressor to react with the substrate. It should be noted that the complete elimination of ionically charged species in the reaction region surrounding the substrate may not be performed in embodiments. In certain instances, ionic species are intended to reach the substrate in order to perform the etch and/or deposition process. In these instances, the ion suppressor may help to control the concentration of ionic species in the reaction region at a level that assists the process.

**[0036]** Showerhead **225** in combination with ion suppressor **223** may allow a plasma present in first plasma region **215** to avoid directly exciting gases in substrate processing region **233**, while still allowing excited species to travel from chamber plasma region **215** into substrate processing region **233**. In this way, the chamber may be configured to prevent the plasma from contacting a substrate **255** being etched. This may advantageously protect a variety of intricate structures and films patterned on the substrate, which may be damaged, dislocated, or otherwise warped if directly contacted by a generated plasma. Additionally, when plasma is allowed to contact the substrate or approach the substrate level, the rate at which materials may be etched increase. Accordingly, an exposed region of material may be further protected by maintaining the plasma remotely from the substrate.

**[0037]** The processing system may further include a power supply **240** electrically coupled with the processing chamber to provide electric power to the faceplate **217**, ion suppressor **223**, showerhead **225**, and/or pedestal **265** to generate a plasma in the first plasma region **215** or processing region **233**. The power supply may be configured to deliver an adjustable amount of power to the chamber depending on

the process performed. Such a configuration may allow for a tunable plasma to be used in the processes being performed. Unlike a remote plasma unit, which is often presented with on or off functionality, a tunable plasma may be configured to deliver a specific amount of power to the plasma region **215**. This in turn may allow development of particular plasma characteristics such that precursors may be dissociated in specific ways to enhance the etching profiles produced by these precursors.

**[0038]** A plasma may be ignited either in chamber plasma region **215** above showerhead **225** or substrate processing region **233** below showerhead **225**. Plasma may be present in chamber plasma region **215** to produce the radical precursors from an inflow of, for example, a fluorine-containing precursor or other precursor. An AC voltage typically in the radio frequency (RF) range may be applied between the conductive top portion of the processing chamber, such as faceplate **217**, and showerhead **225** and/or ion suppressor **223** to ignite a plasma in chamber plasma region **215** during deposition. An RF power supply may generate a high RF frequency of 13.56 MHz but may also generate other frequencies alone or in combination with the 13.56 MHz frequency.

**[0039]** FIG. 2B shows a detailed view **253** of the features affecting the processing gas distribution through faceplate **217**. As shown in FIGS. 2A and 2B, faceplate **217**, cooling plate **203**, and gas inlet assembly **205** intersect to define a gas supply region **258** into which process gases may be delivered from gas inlet **205**. The gases may fill the gas supply region **258** and flow to first plasma region **215** through apertures **259** in faceplate **217**. The apertures **259** may be configured to direct flow in a substantially unidirectional manner such that process gases may flow into processing region **233**, but may be partially or fully prevented from backflow into the gas supply region **258** after traversing the faceplate **217**.

**[0040]** The gas distribution assemblies such as showerhead **225** for use in the processing chamber section **200** may be referred to as dual channel showerheads (DCSH) and are additionally detailed in the embodiments described in FIG. 3. The dual channel showerhead may provide for etching processes that allow for separation of etchants outside of the processing region **233** to provide limited interaction with chamber components and each other prior to being delivered into the processing region.

**[0041]** The showerhead **225** may comprise an upper plate **214** and a lower plate **216**. The plates may be coupled with one another to define a volume **218** between the plates. The coupling of the plates may be so as to provide first fluid channels **219** through the upper and lower plates, and second fluid channels **221** through the lower plate **216**. The formed channels may be configured to provide fluid access from the volume **218** through the lower plate **216** via second fluid channels **221** alone, and the first fluid channels **219** may be fluidly isolated from the volume **218** between the plates and the second fluid channels **221**. The volume **218** may be fluidly accessible through a side of the showerhead **225**.

**[0042]** FIG. 3 is a bottom view of a showerhead **325** for use with a processing chamber according to embodiments. Showerhead **325** may correspond with the showerhead **225** shown in FIG. 2A. Through-holes **365**, which show a view of first fluid channels **219**, may have a plurality of shapes and configurations in order to control and affect the flow of precursors through the showerhead **225**. Small holes **375**,

which show a view of second fluid channels 221, may be distributed substantially evenly over the surface of the showerhead, even amongst the through-holes 365, and may help to provide more even mixing of the precursors as they exit the showerhead than other configurations.

**[0043]** The chambers discussed previously may be used in performing exemplary methods including etching methods. Turning to FIG. 4 is shown exemplary operations in a method 400 according to embodiments of the present technology. Prior to the first operation of the method a substrate may be processed in one or more ways before being placed within a processing region of a chamber in which method 400 may be performed. For example, alternating layers of material may be formed on the substrate and then one or more memory holes or trenches may be formed through the alternating layers. The alternating layers may include any number of materials, and may include alternating layers of a silicon-containing material and a silicon-and-germanium-containing material. Although the remaining disclosure will discuss silicon-containing material and silicon-and-germanium-containing material, any other known materials used in these two layers may be substituted for one or more of the layers. One material in the alternating layers, such as the silicon-and-germanium-containing material may be recessed. In the recess, an oxygen-containing material may be formed followed by a spacer material. Further, an epitaxial material, such as a second silicon-and-germanium-containing material, may be formed in the one or more memory holes or trenches. Some or all of these operations may be performed in chambers or system tools as previously described, or may be performed in different chambers on the same system tool, which may include the chamber in which the operations of method 400 are performed.

**[0044]** The method 400 may include providing a treatment precursor, such as a pre-treatment precursor or pre-etching precursor, to a semiconductor processing chamber at optional operation 405. In some embodiments, an inert precursor may be provided with the treatment precursor. An exemplary chamber may be chamber 200 previously described, which may include one or both of the RPS unit 201 or first plasma region 215. A plasma may be formed at optional operation 410, which may form plasma effluents of the treatment precursor. The substrate may be contacted with the treatment precursor or, if formed, the plasma effluents of the treatment precursor at optional operation 415. The contacting at optional operation 415 may remove a native oxide that is present on the first layer of silicon-and-germanium-containing material and the second layer of silicon-and-germanium-containing material on the substrate. The operations to develop the structure may include removing or etching one or more materials. To increase selectivity during the removal or etching, the method 400 may include providing an oxygen-containing precursor to the processing region at optional operation 420, optionally forming plasma effluents of the oxygen-containing precursor at optional operation 425, and contacting the substrate with the oxygen-containing precursor, or plasma effluents thereof, at optional operation 430. The contacting at optional operation 430 may oxidize at least a portion of the second layer of silicon-and-germanium-containing material, which may be epitaxial silicon-and-germanium-containing material. Subsequent an amount of oxidation, method 400 may include providing a first etchant precursor to the processing region at operation 435, providing a passivation precursor to the processing

region at operation 440, optionally forming plasma effluents of the first etchant precursor and/or passivation precursor at optional operation 445, and contacting the substrate with the first etchant precursor and passivation precursor at operation 450. The contacting at operation 450 may selectively etch the first layer of silicon-and-germanium-containing material, which may be a silicon-and-germanium-containing material nanowire in a GAA transistor. The contacting may also form a passivation material on material(s) underlying the first layer of silicon-and-germanium-containing material to be etched. The passivation material may prevent pitting of material(s) underlying the first layer of silicon-and-germanium-containing material. Method 400 may include providing a second etchant precursor to the processing region at operation 435, optionally forming plasma effluents of the second etchant precursor at optional operation 455, and contacting the substrate with the second etchant precursor at optional operation 460. The second etchant precursor may remove a portion of the silicon-containing material, such as silicon-containing material with germanium residue. Reducing and/or removing germanium residue may increase final device performance due to improve electron mobility.

**[0045]** Method 400 may involve selectively oxidizing one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material. The one silicon-and-germanium-containing material may be selectively oxidized to a greater degree relative to another silicon-and-germanium-containing material due to the germanium concentrations of the materials. The silicon-and-germanium-containing material to be oxidized may be characterized by a higher germanium concentration, and therefore may preferentially oxidize over the other silicon-and-germanium-containing material. By selectively oxidizing one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material, a subsequent etch operation may selectively remove the silicon-and-germanium-containing material that remains unoxidized or less oxidized than the other silicon-and-germanium-containing material. Accordingly, in GAA transistors, for example, the lower germanium-containing silicon-and-germanium-containing nanowire may be etched or released selectively to the higher germanium-containing silicon-and-germanium-containing epitaxial material. The method 400 may allow for the selective oxidation and subsequent selective removal of one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material.

**[0046]** Precursors provided to the processing region in the method 400 at optional operation 405 may include a treatment precursor, such as a pre-treatment precursor or pre-etching precursor, as well as optionally an inert precursor. An exemplary treatment precursor may be a hydrogen-containing precursor, a nitrogen-containing precursor, or combinations thereof, which may be flowed into the processing region. The hydrogen-containing precursor may be or include, for example, molecular hydrogen ( $H_2$ ), ammonia ( $NH_3$ ), or any other hydrogen-containing precursor used or useful in semiconductor processing. The nitrogen-containing precursor may be or include, for example, molecular nitrogen ( $N_2$ ), ammonia ( $NH_3$ ), or any other nitrogen-containing precursor used or useful in semiconductor processing. The treatment precursor may be provided with an inert precursor in some embodiments. The inert precursor may be or include, for example, argon, helium, xenon, or

other noble, inert, or useful precursors. The inert precursor may be used to dilute the treatment precursor or to assist in distributing the treatment precursor throughout the processing region.

**[0047]** If formed at optional operation **410**, the plasma effluents of the treatment precursor and the inert precursor, if present, may be generated at a plasma power of less than or about 5,000 W, and may be generated at less than or about 4,750 W, less than or about 4,500 W, less than or about 4,250 W, less than or about 4,000 W, less than or about 3,750 W, less than or about 3,500 W, less than or about 3,250 W, less than or about 3,000 W, less than or about 2,750 W, less than or about 2,500 W, less than or about 2,250 W, less than or about 2,000 W, less than or about 1,750 W, less than or about 1,500 W, less than or about 1,250 W, less than or about 1,000 W, less than or about 750 W, less than or about 500 W, less than or about 250 W, or less.

**[0048]** The substrate may be contacted with the plasma effluents of the treatment precursor at optional operation **415** for a sufficient period of time to remove native oxide on the silicon-and-germanium-containing material. In embodiments, the period of time may be greater than or about 3 seconds, greater than or about 5 seconds, greater than or about 10 seconds, greater than or about 20 seconds, greater than or about 30 seconds, greater than or about 40 seconds, greater than or about 50 seconds, greater than or about 1 minute, greater than or about 2 minutes, greater than or about 3 minutes, greater than or about 5 minutes, or higher. The period of time may be sufficient to remove greater than or about 85% of the native oxide from the silicon-and-germanium-containing material, and greater than or about 90%, greater than or about 95%, greater than or about 97%, greater than or about 99%, greater than or about 99.9%, or higher, or all of the native oxide may be removed from the silicon-and-germanium-containing material.

**[0049]** In embodiments, method **400** may include providing an oxygen-containing precursor to the processing region of the semiconductor processing chamber at optional operation **420**. In some embodiments, an inert precursor may be provided with the oxygen-containing precursor. The oxygen-containing precursor may be or include, for example, molecular oxygen ( $O_2$ ), steam ( $H_2O$ ), hydrogen peroxide ( $H_2O_2$ ), or any other oxygen-containing precursor used or useful in semiconductor processing. The inert precursor may be or include, for example, argon, helium, xenon, or other noble, inert, or useful precursors. The inert precursor may be used to dilute the oxygen-containing precursor, which may further reduce oxidation rates to control the oxidation and the selectivity of the oxidation, or to assist in distributing the oxygen-containing precursor throughout the processing region. Additionally, a flow rate ratio of the oxygen-containing precursor and, if present, the inert precursor may be adjusted to tune oxidative effect of the oxygen-containing precursor and/or oxidation selectivity.

**[0050]** A flow rate of the oxygen-containing precursor and the inert precursor, if present, may be sufficient to selectively oxidize one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material. In embodiments, a flow rate of the oxygen-containing precursor to the processing region may be greater than or about 1 sccm, and may be greater than or about 10 sccm, greater than or about 50 sccm, greater than or about 100 sccm, greater than or about 250 sccm, greater than or about 500 sccm, greater than or about 1,000 sccm, greater than or

about 1,500 sccm, greater than or about 2,000 sccm, greater than or about 2,500 sccm, greater than or about 3,000 sccm, greater than or about 3,500 sccm, greater than or about 4,000 sccm, or higher. Additionally, a flow rate of the inert precursor, which may dilute and/or distribute the oxygen-containing precursor or plasma effluents thereof may be greater than or about 100 sccm, and may be greater than or about 250 sccm, greater than or about 500 sccm, greater than or about 750 sccm, greater than or about 1,000 sccm, greater than or about 2,500 sccm, greater than or about 5,000 sccm, greater than or about 7,500 sccm, greater than or about 10,000 sccm, or higher.

**[0051]** In some embodiments, plasma effluents of the oxygen-containing precursor may be generated at optional operation **425**. As discussed, the plasma effluents may be generated in the processing region. However, it is contemplated that plasma effluents may not be formed of the oxygen-containing precursor and a plasma-free or thermal oxidation may be performed. For example, when the oxygen-containing precursor is  $O_2$  or  $H_2O$ , the plasma effluents may oxidize all silicon-and-germanium-containing materials on the substrate. Accordingly, a subsequent etch to remove one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material may not be able to etch any of the oxidized silicon-and-germanium-containing material. In embodiments where plasma effluents of the oxygen-containing precursor are formed, the plasma effluents of the oxygen-containing precursor and the inert precursor, if present, may be generated at a plasma power of less than or about 5,000 W, and may be generated at less than or about 4,750 W, less than or about 4,500 W, less than or about 4,250 W, less than or about 4,000 W, less than or about 3,750 W, less than or about 3,500 W, less than or about 3,250 W, less than or about 3,000 W, less than or about 2,750 W, less than or about 2,500 W, less than or about 2,250 W, less than or about 2,000 W, less than or about 1,750 W, less than or about 1,500 W, less than or about 1,250 W, less than or about 1,000 W, less than or about 750 W, less than or about 500 W, less than or about 250 W, or less. Compared to the pre-treatment precursor, plasma effluents of the oxygen-containing precursor may be generated at a lower plasma power. By generating plasma effluents of the post-treatment at a lower plasma power, oxidation may be better controlled and bombardment/damage to the substrate and materials deposited thereon may be limited.

**[0052]** Method **400** may include contacting the substrate with the oxygen-containing precursor, or plasma effluents thereof, at optional operation **430**. The contacting may continue for a sufficient period of time to oxidize at least one of the multiple silicon-and-germanium-containing materials on the substrate. In embodiments, the period of time may be greater than or about 3 seconds, greater than or about 5 seconds, greater than or about 10 seconds, greater than or about 20 seconds, greater than or about 30 seconds, greater than or about 40 seconds, greater than or about 50 seconds, greater than or about 1 minute, greater than or about 2 minutes, greater than or about 3 minutes, greater than or about 5 minutes, or higher. Similarly, the period of time may be less than or about 5 minutes, less than or about 3 minutes, less than or about 2 minutes, less than or about 1 minute, less than or about 50 seconds, less than or about 40 seconds, less than or about 30 seconds, less than or about 20 seconds, less than or about 10 seconds, less than or about 5 seconds, less than or about 3 seconds, or less.

**[0053]** By contacting the substrate with the oxygen-containing precursor, germanium and/or silicon in silicon-and-germanium-containing material may bond with oxygen to oxidize a portion of the silicon-and-germanium-containing material. Without being bound by any particular theory, it is believed that germanium may more readily bond with oxygen, and silicon-and-germanium-containing material with a higher germanium concentration may oxidize easier than neighboring silicon-and-germanium-containing material with a lower germanium concentration. Additionally, it is believed Si—Ge bonds in the silicon-and-germanium-containing material may break easier than Si—Si bonds in neighboring silicon-containing material, and the silicon-and-germanium-containing material may oxidize easier than neighboring silicon-containing material. Additionally, by operating at temperature and/or pressure ranges discussed below, the silicon-and-germanium-containing material with a higher germanium concentration may be more readily oxidized.

**[0054]** At operation 435, method 400 may include providing a first etchant precursor to the processing region of the semiconductor processing chamber. The first etchant precursor may be a halogen-containing precursor or any other precursor able to selectively etch silicon-and-germanium-containing material. The first etchant precursor may be or include, for example, diatomic fluorine ( $F_2$ ), nitrogen trifluoride ( $NF_3$ ), hydrogen fluoride (HF), or any other fluorine-containing precursor used or useful in semiconductor processing.

**[0055]** At operation 440, method 400 may include providing a passivation precursor to the processing region of the semiconductor processing chamber. The passivation precursor may be provided with the first etchant precursor. However, it is also contemplated that the passivation precursor and the first etchant precursor may be provided sequentially. The passivation precursor may be a carbon-containing precursor or any other precursor able to selectively passivate material(s) underlying the silicon-and-germanium-containing material to be etched.

**[0056]** More specifically, the passivation precursor may block pitting holes in material(s) underlying the silicon-and-germanium-containing material to be etched, such as a spacer material (e.g., low dielectric constant material).

**[0057]** The passivation precursor may be characterized by a boiling point and/or vapor pressure that promotes condensation of the passivation precursor as passivation material in pitting holes in material(s) underlying the silicon-and-germanium-containing material to be etched. For example, the passivation precursor may be characterized by a boiling point of less than or about  $100^\circ C.$ , such as less than or about  $90^\circ C.$ , less than or about  $80^\circ C.$ , less than or about  $70^\circ C.$ , less than or about  $60^\circ C.$ , less than or about  $50^\circ C.$ , less than or about  $45^\circ C.$ , less than or about  $40^\circ C.$ , less than or about  $35^\circ C.$ , less than or about  $30^\circ C.$ , less than or about  $25^\circ C.$ , less than or about  $20^\circ C.$ , less than or about  $15^\circ C.$ , less than or about  $10^\circ C.$ , less than or about  $5^\circ C.$ , or less. The passivation precursor may be characterized by a vapor pressure at  $25^\circ C.$  of less than or about 100 kPa, less than or about 95 kPa, less than or about 90 kPa, less than or about 85 kPa, less than or about 80 kPa, less than or about 75 kPa, less than or about 70 kPa, less than or about 65 kPa, less than or about 60 kPa, less than or about 55 kPa, or less. In embodiments, the passivation precursor may be a fluorine-and-carbon-containing precursor (i.e., fluorocarbon). The

passivation precursor may be or include, for example, perfluoropentane ( $C_5F_{12}$ ), or any other fluorine-and-carbon-containing precursor used or useful in semiconductor processing.

**[0058]** In some embodiments, an inert precursor may be provided with the first etchant precursor and/or the passivation precursor. The inert precursor may be or include, for example, argon, helium, xenon, or other noble, inert, or useful precursors. The inert precursor may be used to dilute the first etchant precursor and/or the passivation precursor, which may further reduce etching rates to control the etch and the selectivity of the etch, or to assist in distributing the first etchant precursor and/or the passivation precursor throughout the processing region. Additionally, a flow rate ratio of the first etchant precursor, the passivation precursor, and, if present, the inert precursor may be adjusted to tune etching selectivity.

**[0059]** A flow rate of the first etchant precursor may be sufficient to selectively etch one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material. In embodiments, a flow rate of the first etchant precursor to the processing region may be greater than or about 1 sccm, and may be greater than or about 10 sccm, greater than or about 50 sccm, greater than or about 100 sccm, greater than or about 250 sccm, greater than or about 500 sccm, greater than or about 1,000 sccm, greater than or about 1,500 sccm, greater than or about 2,000 sccm, greater than or about 2,500 sccm, greater than or about 3,000 sccm, greater than or about 3,500 sccm, greater than or about 4,000 sccm, or higher.

**[0060]** A flow rate of the passivation precursor may be sufficient to passivate material(s) underlying the silicon-and-germanium-containing material to be etched. Additionally, a flow rate of the passivation precursor may be minimized to reduce any impact on the desired etching. In embodiments, a flow rate of the passivation precursor to the processing region may be less than or about 1,000 sccm, and may be less than or about 900 sccm, less than or about 800 sccm, less than or about 700 sccm, less than or about 600 sccm, less than or about 500 sccm, less than or about 400 sccm, less than or about 300 sccm, less than or about 200 sccm, less than or about 100 sccm, less than or about 90 sccm, less than or about 80 sccm, less than or about 70 sccm, less than or about 60 sccm, less than or about 50 sccm, less than or about 40 sccm, less than or about 30 sccm, less than or about 20 sccm, less than or about 10 sccm, or less.

**[0061]** Additionally, a flow rate ratio of the first etchant precursor to the passivation precursor may be maintained to reduce any impact on the desired etching. In embodiments, the flow rate ratio of the first etchant precursor to the passivation precursor may be greater than or about 1:1, and may be greater than or about 1.2:1, greater than or about 1.4:1, greater than or about 1.6:1, greater than or about 1.8:1, greater than or about 2:1, greater than or about 2.5:1, or more. A relatively low flow rate of the passivation precursor may ensure passivation material is formed to block pitting holes in material(s) underlying the silicon-and-germanium-containing material to be etched while not disrupting the desired etch of the silicon-and-germanium-containing material. If the flow rate of the passivation precursor relative to the first etchant precursor is too high, the etch rate of the silicon-and-germanium-containing material may be reduced.

[0062] Additionally, a flow rate of the inert precursor, which may dilute and/or distribute the first etchant precursor, the passivation precursor, or plasma effluents thereof may be greater than or about 100 sccm, and may be greater than or about 250 sccm, greater than or about 500 sccm, greater than or about 750 sccm, greater than or about 1,000 sccm, greater than or about 2,500 sccm, greater than or about 5,000 sccm, greater than or about 7,500 sccm, greater than or about 10,000 sccm, or higher.

[0063] In some embodiments, plasma effluents of the first etchant precursor and/or the passivation precursor may be generated at optional operation 445. As discussed, the plasma effluents may be generated in the processing region. In embodiments plasma effluents of the first etchant precursor, the passivation precursor, and the inert precursor, if present, may be generated at a plasma power of less than or about 5,000 W, and may be generated at less than or about 4,750 W, less than or about 4,500 W, less than or about 4,250 W, less than or about 4,000 W, less than or about 3,750 W, less than or about 3,500 W, less than or about 3,250 W, less than or about 3,000 W, less than or about 2,750 W, less than or about 2,500 W, less than or about 2,250 W, less than or about 2,000 W, less than or about 1,750 W, less than or about 1,500 W, less than or about 1,250 W, less than or about 1,000 W, less than or about 750 W, less than or about 500 W, less than or about 250 W, or less.

[0064] Method 400 may include contacting the substrate with the first etchant precursor and passivation precursor, or plasma effluents thereof, at operation 450. The contacting may continue for a sufficient period of time to etch at least one of the multiple silicon-and-germanium-containing materials on the substrate. In embodiments, the period of time may be greater than or about 3 seconds, greater than or about 5 seconds, greater than or about 10 seconds, greater than or about 20 seconds, greater than or about 30 seconds, greater than or about 40 seconds, greater than or about 50 seconds, greater than or about 1 minute, greater than or about 2 minutes, greater than or about 3 minutes, greater than or about 5 minutes, or higher. Similarly, the period of time may be less than or about 5 minutes, less than or about 3 minutes, less than or about 2 minutes, less than or about 1 minute, less than or about 50 seconds, less than or about 40 seconds, less than or about 30 seconds, less than or about 20 seconds, less than or about 10 seconds, less than or about 5 seconds, less than or about 3 seconds, or less.

[0065] By contacting the substrate with the first etchant precursor, the non-oxidized silicon-and-germanium-containing material may be selectively removed relative to other materials on the substrate, including the oxidized silicon-and-germanium-containing material. Without being bound by any particular theory, it is believed that the oxidized silicon-and-germanium-containing material may be more resistant to the first etchant precursor compared to the non-oxidized silicon-and-germanium-containing material. Therefore, the non-oxidized silicon-and-germanium-containing material may be selectively removed compared to the oxidized silicon-and-germanium-containing material. As such, in GAA transistors, the non-oxidized and lower germanium concentration silicon-and-germanium-containing material, such as SiGe nanowires, may be selectively removed relative to the oxidized and higher germanium concentration silicon-and-germanium-containing material, such as epitaxial SiGe material. Additionally, the passivation precursor may condense on material(s) underlying the sili-

con-and-germanium-containing material to be etched. The condensation of the passivation precursor may form a passivation material. The passivation material may block pitting holes (i.e., pores) in material(s) underlying the silicon-and-germanium-containing material.

[0066] The contacting at operation 450 may etch one layer of silicon-and-germanium-containing material relative to another layer of silicon-and-germanium-containing material at a selectivity of greater than or about 40:1. For example, the non-oxidized layer of silicon-and-germanium-containing material may be etched at a selectivity of greater than or about 42:1 relative to the oxidized layer of silicon-and-germanium-containing material, such as greater than or about 44:1, greater than or about 46:1, greater than or about 48:1, greater than or about 50:1, greater than or about 52:1, greater than or about 54:1, greater than or about 56:1, greater than 58:1, or more. In embodiments, an etch rate, such as of the non-oxidized layer of silicon-and-germanium-containing material, may be greater than or about 5.0 Å/s, and may be greater than or about 10.0 Å/s, greater than or about 15.0 Å/s, greater than or about 16.0 Å/s, greater than or about 17.0 Å/s, greater than or about 18.0 Å/s, greater than or about 19.0 Å/s, greater than or about 20.0 Å/s, greater than or about 22.0 Å/s, greater than or about 24.0 Å/s, greater than or about 26.0 Å/s, greater than or about 28.0 Å/s, greater than or about 30.0 Å/s, greater than or about 35.0 Å/s, greater than or about 40.0 Å/s, or more.

[0067] After etching the non-oxidized silicon-and-germanium-containing material selectively to other materials on the substrate, some germanium residue may remain on some surfaces. For example, some germanium residue may be present on the silicon-containing material, such as Si nanowires. If left untreated or not removed from the surface of the silicon-containing material, the residue may impact electron mobility in final devices. Accordingly, the presence of germanium residue, such as on the silicon-containing material, may degrade final device performance. The present technology may address this issue by selectively removing an amount of the silicon-containing material to reduce the presence of germanium residue.

[0068] At optional operation 455, method 400 may include providing a second etchant precursor to the processing region of the semiconductor processing chamber. In some embodiments, a hydrogen-containing precursor and/or an inert precursor may be provided with the second etchant precursor. The second etchant precursor may be a halogen-containing precursor or any other precursor able to selectively etch silicon-containing material. The second etchant precursor may be or include, for example, diatomic fluorine ( $F_2$ ), nitrogen trifluoride ( $NF_3$ ), hydrogen fluoride (HF), carbon tetrafluoride ( $CF_4$ ), xenon difluoride ( $XeF_2$ ), or any other fluorine-containing precursor used or useful in semiconductor processing. The hydrogen-containing precursor may be or include, for example, diatomic hydrogen ( $H_2$ ), ammonia ( $NH_3$ ), a hydrocarbon, or any other hydrogen-containing precursor used or useful in semiconductor processing. The inert precursor may be or include, for example, argon, helium, nitrogen, xenon, or other noble, inert, or useful precursors. The inert precursor may be used to dilute the second etchant precursor, which may further reduce etching rates to control the etch and the selectivity of the etch, or to assist in distributing the second etchant precursor throughout the processing region. Additionally, a flow rate

ratio of the second etchant precursor and, if present, the inert precursor may be adjusted to tune etching selectivity.

**[0069]** A flow rate of the second etchant precursor and the inert precursor, if present, may be sufficient to selectively etch one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material. In embodiments, a flow rate of the second etchant precursor to the processing region may be greater than or about 1 sccm, and may be greater than or about 10 sccm, greater than or about 50 sccm, greater than or about 100 sccm, greater than or about 250 sccm, greater than or about 500 sccm, greater than or about 1,000 sccm, greater than or about 1,500 sccm, greater than or about 2,000 sccm, greater than or about 2,500 sccm, greater than or about 3,000 sccm, greater than or about 3,500 sccm, greater than or about 4,000 sccm, or higher. Additionally, a flow rate of the inert precursor, which may dilute and/or distribute the second etchant precursor or plasma effluents thereof may be greater than or about 100 sccm, and may be greater than or about 250 sccm, greater than or about 500 sccm, greater than or about 750 sccm, greater than or about 1,000 sccm, greater than or about 2,500 sccm, greater than or about 5,000 sccm, greater than or about 7,500 sccm, greater than or about 10,000 sccm, or higher.

**[0070]** In embodiments, an atomic flow ratio of hydrogen relative to fluorine may be greater than 1:1, greater than or about 1.2:1, greater than or about 1.4:1, greater than or about 1.6:1, greater than or about 1.8:1, greater than or about 2:1 or greater than or about 4:1, or more. Higher atomic flow ratios hydrogen relative to fluorine may increase the silicon selectivity in embodiments. Some precursors may contain both fluorine and hydrogen, in which case the atomic flow rate of all contributions are included when calculating the atomic flow ratio described herein. Additionally, the atomic flow ratio of argon, or any other inert material, relative to fluorine may be greater than or about 100:1, greater than or about 150:1 or greater than or about 200:1, or more.

**[0071]** In some embodiments, plasma effluents of the second etchant precursor may be generated at optional operation 460. The plasma effluents may be generated in the processing region or in an RPS. In embodiments plasma effluents of the second etchant precursor and the hydrogen-containing precursor and/or inert precursor, if present, may be generated at a plasma power of less than or about 5,000 W, and may be generated at less than or about 4,750 W, less than or about 4,500 W, less than or about 4,250 W, less than or about 4,000 W, less than or about 3,750 W, less than or about 3,500 W, less than or about 3,250 W, less than or about 3,000 W, less than or about 2,750 W, less than or about 2,500 W, less than or about 2,250 W, less than or about 2,000 W, less than or about 1,750 W, less than or about 1,500 W, less than or about 1,250 W, less than or about 1,000 W, less than or about 750 W, less than or about 500 W, less than or about 250 W, or less.

**[0072]** Method 400 may include contacting the substrate with the second etchant precursor, or plasma effluents thereof, at optional operation 465. The contacting may continue for a sufficient period of time to etch a portion of the silicon-containing material on the substrate. In embodiments, the period of time may be greater than or about 3 seconds, greater than or about 5 seconds, greater than or about 10 seconds, greater than or about 20 seconds, greater than or about 30 seconds, greater than or about 40 seconds, greater than or about 50 seconds, greater than or about 1 minute, greater than or about 2 minutes, greater than or

about 3 minutes, greater than or about 5 minutes, or higher. Similarly, the period of time may be less than or about 5 minutes, less than or about 3 minutes, less than or about 2 minutes, less than or about 1 minute, less than or about 50 seconds, less than or about 40 seconds, less than or about 30 seconds, less than or about 20 seconds, less than or about 10 seconds, less than or about 5 seconds, less than or about 3 seconds, or less. Shorter durations may be preferable to remove only a small amount of the silicon-containing material, such as the silicon-containing material with germanium residue.

**[0073]** The contacting may etch less than or about 10 nm of the silicon-containing material to maintain as much of the silicon-containing material as possible while reducing germanium residue. In embodiments, the contacting may etch less than or about 9 nm of the silicon-containing material, such as less than or about 8 nm, less than or about 7 nm, less than or about 6 nm, less than or about 5 nm, less than or about 4 nm, less than or about 3 nm, less than or about 2 nm, or less, such as between about 2 nm and about 5 nm of the of silicon-containing material.

**[0074]** The contacting at operation 450 may etch one layer of silicon-containing material relative to any other material on the substrate at a selectivity of greater than or about 40:1. For example, the silicon-containing material may be etched at a selectivity of greater than or about 50:1 relative to any other material on the substrate, such as greater than or about 60:1, greater than or about 70:1, greater than or about 80:1, greater than or about 90:1, greater than or about 100:1, greater than or about 125:1, greater than or about 150:1, or more.

**[0075]** Subsequent contacting the substrate with the second etchant precursor, a surface of the silicon-containing material may be characterized by a germanium concentration of less than or about 1.5 at. %, and may be characterized by a germanium concentration of less than or about 1.4 at. %, less than or about 1.3 at. %, less than or about 1.2 at. %, less than or about 1.1 at. %, less than or about 1.1 at. %, less than or about 0.9 at. %, less than or about 0.8 at. %, less than or about 0.7 at. %, less than or about 0.6 at. %, less than or about 0.5 at. %, less than or about 0.4 at. %, less than or about 0.3 at. %, less than or about 0.2 at. %, or less.

**[0076]** In embodiments, operations 405-415 may be performed in the same semiconductor processing chamber as operations 420-430, or the substrate may be transferred to a second processing region of a second semiconductor processing chamber to selectively oxidize one silicon-and-germanium-containing material on the substrate at operations 420-430. However, the second semiconductor processing chamber may be on the same processing system or mainframe, such as processing system 100, as the semiconductor processing chamber used during operations 405-415. Additionally, operations 435-450 may be performed in the same semiconductor processing chamber as operations 405-415 and/or operations 420-430, or the substrate may be transferred to a third processing region of a third semiconductor processing chamber to selectively etch one silicon-and-germanium-containing material on the substrate at operations 435-450. However, the third semiconductor processing chamber may be on the same processing system or mainframe, such as processing system 100, as the semiconductor processing chamber(s) used during operations 405-415 and/or operations 420-430. Further, optional operations 455-465 may be performed in the same semiconductor



processing chamber as operations **405-415**, operations **420-430** and/or operations **435-450**, or the substrate may be transferred to a fourth processing region of a fourth semiconductor processing chamber to selectively etch the silicon-containing material on the substrate at optional operations **455-465** to reduce and/or remove germanium residue. However, the fourth semiconductor processing chamber may be on the same processing system or mainframe, such as processing system **100**, as the semiconductor processing chamber(s) used during operations **405-415**, operations **420-430** and/or operations **435-450**. Accordingly, contacting the substrate with the pre-treatment precursor, contacting the substrate with the oxygen-containing precursor, contacting the substrate with the first etchant precursor, and contacting the substrate with the second etchant precursor may be performed on a single mainframe.

**[0077]** Process conditions may also impact the operations performed in method **400** as well as other etching methods according to the present technology. Each of the operations of method **400** may be performed during a constant temperature in embodiments, while in some embodiments the temperature may be adjusted during different operations. For example, the substrate, pedestal, or chamber temperature may be maintained between about 0° C. and about 500° C. in embodiments. The temperature may also be maintained at less than or about 480° C., less than or about 460° C., less than or about 440° C., less than or about 420° C., less than or about 400° C., less than or about 380° C., less than or about 360° C., less than or about 350° C., less than or about 340° C., less than or about 330° C., less than or about 320° C., less than or about 310° C., less than or about 300° C., less than or about 280° C., less than or about 260° C., less than or about 240° C., less than or about 220° C., less than or about 200° C., less than or about 150° C., less than or about 100° C., less than or about 75° C., less than or about 50° C., less than or about 25° C., or less. In embodiments, the temperature may also be maintained at greater than or about 0° C., greater than or about 25° C., greater than or about 50° C., greater than or about 75° C., greater than or about 100° C., greater than or about 120° C., greater than or about 140° C., greater than or about 150° C., greater than or about 160° C., greater than or about 180° C., greater than or about 200° C., greater than or about 220° C., greater than or about 240° C., greater than or about 260° C., greater than or about 280° C., greater than or about 300° C., greater than or about 320° C., greater than or about 340° C., greater than or about 360° C., greater than or about 380° C., greater than or about 400° C., greater than or about 420° C., greater than or about 440° C., greater than or about 460° C., greater than or about 480° C., greater than or about 500° C., or higher. Temperature may affect the quality of the oxidation process, and higher temperature may allow for better oxidation of the silicon-and-germanium-containing material. Higher temperature may also produce higher reactivity between the etchant precursor and the silicon-and-germanium-containing material. Similarly, lower temperatures may slow the removal of the silicon-and-germanium-containing material due to poor reactivity. However, higher temperature may reduce effectiveness of the passivation precursor. Thus, in some embodiments, maintaining a temperature at between about 0° C. and about 150° C. may provide better oxidation, increased removal of the silicon-and-germanium-containing material, and/or increased effectiveness of the passivation precursor.

**[0078]** The pressure within the chamber may also affect the operations performed, and in embodiments the pressure within the semiconductor processing chamber may be maintained at greater than about 1 Torr, greater than or about 2 Torr, greater than or about 3 Torr, greater than or about 4 Torr, greater than or about 5 Torr, greater than or about 7.5 Torr, greater than or about 10 Torr, greater than or about 12.5 Torr, greater than or about 15 Torr, greater than or about 17.5 Torr, greater than or about 20 Torr, or more. Each of the operations of method **400** may be performed during a constant pressure in embodiments, while in some embodiments the pressure may be adjusted during different operations. In embodiments a pressure greater or about 1 Torr may result in stronger oxidation of one silicon-and-germanium-containing material relative to another silicon-and-germanium-containing material. Accordingly, a lower pressure may result in weaker oxidation and, therefore, may require additional time for sufficient or desired oxidation. However, to maintain precise selectivity of the oxidation, the pressure within the chamber may also be maintained at less than or about 30 Torr, and may be maintained at less than or about 28 Torr, less than or about 26 Torr, less than or about 24 Torr, less than or about 22 Torr, less than or about 20 Torr, less than or about 18 Torr, less than or about 16 Torr, less than or about 14 Torr, less than or about 12 Torr, less than or about 10 Torr, or less.

**[0079]** Turning to FIGS. **5A-5D** are shown cross-sectional views of structure **500** being processed according to embodiments of the present technology. As illustrated in FIG. **5A**, structure **500** may include a substrate **505** that may have a plurality of stacked layers overlying the substrate, which may be silicon-containing material, silicon-and-germanium-containing material, or other substrate materials. The alternating layers of material may include materials suitable for GAA transistors, such as silicon-containing material **510** alternating with first silicon-and-germanium-containing material **515**. The first silicon-and-germanium-containing material **515** may be or include material that will be recessed and/or removed to produce nanowires/nanosheets in GAA transistors. Although illustrated with only 7 layers of material, exemplary structures may include any number of layers. Memory holes or trenches may be defined through the stacked structure to the level of substrate **505**. Memory holes or trenches may be defined by sidewalls that may be composed of the alternating layers of silicon-containing material **510** and first silicon-and-germanium-containing material **515**. After recessing the first silicon-and-germanium-containing material **515**, an oxygen-containing material **520** and a spacer material **525** may be formed in the recesses. As illustrated in FIG. **5A**, the oxygen-containing material **520** may line the silicon-containing material **510** and the first silicon-and-germanium-containing material **515** defining the recess. The spacer material **525** may then be deposited in the remaining area where the first silicon-and-germanium-containing material **515** was previously. A second silicon-and-germanium-containing material **530** may then be formed in the memory holes or trenches defined through the stacked structure.

**[0080]** In embodiments, the second silicon-and-germanium-containing material **530**, which may be epitaxially grown, may be characterized by a germanium concentration greater than the first silicon-and-germanium-containing material **515**. For example, the first silicon-and-germanium-containing material **515** may be characterized by a germa-

nium concentration of less than or about 35 at. %, and may be characterized by a germanium concentration of less than or about 32.5 at. %, less than or about 30 at. %, less than or about 27.5 at. %, less than or about 25 at. %, less than or about 22.5 at. %, less than or about 20 at. %, less than or about 17.5 at. %, less than or about 15 at. %, or less. Conversely, the second silicon-and-germanium-containing material **530** may be characterized by a germanium concentration greater than or about 35 at. %, and may be characterized by a germanium concentration of greater than or about 37.5 at. %, greater than or about 40 at. %, greater than or about 42.5 at. %, greater than or about 45 at. %, greater than or about 47.5 at. %, greater than or about 50 at. %, greater than or about 52.5 at. %, greater than or about 55 at. %, greater than or about 57.5 at. %, greater than or about 60 at. %, or more. Additionally, the second silicon-and-germanium-containing material **530** may be a doped material. In embodiments, the second silicon-and-germanium-containing material **530** may be doped with, for example, boron.

**[0081]** FIG. 5B may illustrate the structure after some operations of methods according to the present technology have been performed, such as discussed with respect to FIG. 4 above. Contacting the substrate with the oxygen-containing precursor, such as at optional operation **430** of method **400**, may oxidize at least a portion of the second layer of silicon-and-germanium-containing material **535**. The portion of the second layer of silicon-and-germanium-containing material **535** may be an oxidized silicon-and-germanium-containing material. The portion of the second layer of silicon-and-germanium-containing material **535** may be in contact with the oxygen-containing material **520** and/or the spacer material **525**. As previously discussed with regard to methods according to the present technology, such as discussed with respect to FIG. 4 above, the second layer of silicon-and-germanium-containing material **530** may selectively oxidize relative to the first layer of silicon-and-germanium-containing material **515** due to the increased germanium concentration of the second layer of silicon-and-germanium-containing material **530**. The spacer material **525** may be porous. Accordingly, during a subsequent etch to remove the first silicon-and-germanium-containing material **515**, etchant species may penetrate the spacer material **525** and reach the second layer of silicon-and-germanium-containing material **530**. Without the portion of the second layer of silicon-and-germanium-containing material **535** blocking the etchant species, some of the second layer of silicon-and-germanium-containing material **530** may be etched.

**[0082]** FIG. 5C illustrates the structure after further operations of methods according to the present technology have been performed, such as discussed with respect to FIG. 4 above. An etching operation may be performed to remove the silicon-and-germanium-containing material **515**. The etching may remove the first silicon-and-germanium-containing material **515** to form nanowires/nanosheets of the silicon-containing material **510** useful in GAA applications. Structure **500** may show minimal or zero etching of the second layer of silicon-and-germanium-containing material **530** due to the selective oxidation of the portion of the second layer of silicon-and-germanium-containing material **535** as well as the presence of the passivation precursor to block pitting holes in material(s) underlying the first silicon-and-germanium-containing material **515**.

**[0083]** FIG. 5D illustrates the structure after further operations of methods according to the present technology have been performed, such as discussed with respect to FIG. 4 above. An etching operation may be performed to remove a portion of the silicon-containing material **510**. The etching may remove a portion of the silicon-containing material **510** to reduce and/or remove germanium residue from nanowires/nanosheets of the first silicon-and-germanium-containing material **515** previously removed. A minimal portion of the silicon-containing material **510** may be removed to reduce germanium residue while maintaining as much of the silicon-containing material **510** as possible.

**[0084]** In the preceding description, for the purposes of explanation, numerous details have been set forth in order to provide an understanding of various embodiments of the present technology. It will be apparent to one skilled in the art, however, that certain embodiments may be practiced without some of these details, or with additional details.

**[0085]** Having disclosed several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the embodiments. Additionally, a number of well-known processes and elements have not been described in order to avoid unnecessarily obscuring the present technology. Accordingly, the above description should not be taken as limiting the scope of the technology. Additionally, methods or processes may be described as sequential or in steps, but it is to be understood that the operations may be performed concurrently, or in different orders than listed.

**[0086]** Where a range of values is provided, it is understood that each intervening value, to the smallest fraction of the unit of the lower limit, unless the context clearly dictates otherwise, between the upper and lower limits of that range is also specifically disclosed. Any narrower range between any stated values or unstated intervening values in a stated range and any other stated or intervening value in that stated range is encompassed. The upper and lower limits of those smaller ranges may independently be included or excluded in the range, and each range where either, neither, or both limits are included in the smaller ranges is also encompassed within the technology, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included.

**[0087]** As used herein and in the appended claims, the singular forms “a”, “an”, and “the” include plural references unless the context clearly dictates otherwise. Thus, for example, reference to “a precursor” includes a plurality of such precursors, and reference to “the material” includes reference to one or more materials and equivalents thereof known to those skilled in the art, and so forth.

**[0088]** Also, the words “comprise(s)”, “comprising”, “contain(s)”, “containing”, “include(s)”, and “including”, when used in this specification and in the following claims, are intended to specify the presence of stated features, integers, components, or operations, but they do not preclude the presence or addition of one or more other features, integers, components, operations, acts, or groups.

1. A semiconductor processing method comprising: providing a first etchant precursor to a processing region of a semiconductor processing chamber, wherein a substrate is housed within the processing region, and wherein a first layer of silicon-and-germanium-contain-

- ing material, a second layer of silicon-and-germanium-containing material, and a layer of silicon-containing material are disposed on the substrate;  
 providing a passivation precursor to the processing region; and  
 contacting the substrate with the first etchant precursor and the passivation precursor, wherein the contacting selectively etches the first layer of silicon-and-germanium-containing material, and wherein the contacting forms a passivation material on the substrate.
2. The semiconductor processing method of claim 1, wherein:  
 the first layer of silicon-and-germanium-containing material is characterized by a first germanium concentration; the second layer of silicon-and-germanium-containing material is characterized by a second germanium concentration; and  
 the first germanium concentration is less than the second germanium concentration.
3. The semiconductor processing method of claim 1, wherein the passivation precursor comprises a fluorine-and-carbon-containing precursor.
4. The semiconductor processing method of claim 1, wherein the passivation precursor comprises perfluoropentane ( $C_5F_{12}$ ).
5. The semiconductor processing method of claim 1, further comprising:  
 forming plasma effluents of the first etchant precursor, the passivation precursor, or both.
6. The semiconductor processing method of claim 1, wherein the first etchant precursor comprises a fluorine-containing precursor.
7. The semiconductor processing method of claim 1, further comprising:  
 providing an inert gas with the first etchant precursor, the passivation precursor, or both.
8. The semiconductor processing method of claim 1, wherein the passivation precursor is characterized by a boiling point of less than or about  $100^\circ\text{C}$ .
9. The semiconductor processing method of claim 1, wherein the passivation precursor is characterized by a vapor pressure at  $25^\circ\text{C}$ . of less than or about 100 kPa.
10. The semiconductor processing method of claim 1, wherein a pressure in the processing region is maintained at less than or about 30 Torr.
11. The semiconductor processing method of claim 1, wherein a temperature in the processing region is maintained at less than or about  $150^\circ\text{C}$ .
12. A semiconductor processing method comprising:  
 providing an oxygen-containing precursor to a processing region of a semiconductor processing chamber, wherein a substrate is housed within the processing region, wherein a first layer of silicon-and-germanium-containing material, a second layer of silicon-and-germanium-containing material, and a layer of silicon-containing material are disposed on the substrate, and wherein the first layer of silicon-and-germanium-containing material is characterized by a lesser germanium concentration than the second layer of silicon-and-germanium-containing material;  
 contacting the substrate with the oxygen-containing precursor, wherein the contacting oxidizes at least a portion of the second layer of silicon-and-germanium-containing material;
- providing a first fluorine-containing precursor to the processing region;  
 providing a fluorine-and-carbon-containing precursor to the processing region; and  
 contacting the substrate with the first fluorine-containing precursor and the fluorine-and-carbon-containing precursor, wherein the contacting etches the first layer of silicon-and-germanium-containing material relative to the second layer of silicon-and-germanium-containing material while preventing etching of the second layer of silicon-and-germanium-containing material.
13. The semiconductor processing method of claim 12, wherein the fluorine-and-carbon-containing precursor comprises perfluoropentane ( $C_5F_{12}$ ).
14. The semiconductor processing method of claim 12, wherein a flow rate of the fluorine-and-carbon-containing precursor is less than a flow rate of the first fluorine-containing precursor.
15. The semiconductor processing method of claim 12, wherein a flow rate of the fluorine-and-carbon-containing precursor is less than or about 1,000 sccm.
16. The semiconductor processing method of claim 12, further comprising:  
 forming plasma effluents of the first fluorine-containing precursor.
17. The semiconductor processing method of claim 12, wherein the contacting etches the first layer of silicon-and-germanium-containing material relative to the second layer of silicon-and-germanium-containing material at a selectivity of greater than or about 40:1.
18. A semiconductor processing method comprising:  
 providing a first fluorine-containing precursor to a processing region of a semiconductor processing chamber, wherein a substrate is housed within the processing region, wherein a first layer of silicon-and-germanium-containing material, a second layer of silicon-and-germanium-containing material, and a layer of silicon-containing material are disposed on the substrate, and wherein the first layer of silicon-and-germanium-containing material is characterized by a lesser germanium concentration than the second layer of silicon-and-germanium-containing material;  
 providing a fluorine-and-carbon-containing precursor to the processing region;  
 contacting the substrate with the first fluorine-containing precursor and the fluorine-and-carbon-containing precursor, wherein the contacting selectively etches the first layer of silicon-and-germanium-containing material while preventing etching of the second layer of silicon-and-germanium-containing material;  
 providing a second fluorine-containing precursor and a hydrogen-containing precursor to the processing region;  
 forming plasma effluents of the second fluorine-containing precursor and the hydrogen-containing precursor; and  
 contacting the substrate with the plasma effluents of the second fluorine-containing precursor and the hydrogen-containing precursor, wherein the contacting etches a portion of the layer of silicon-containing material.
19. The semiconductor processing method of claim 18, wherein a flow rate ratio of the first fluorine-containing precursor to the fluorine-and-carbon-containing precursor is greater than or about 1:1.

20. The semiconductor processing method of claim 18, wherein the fluorine-and-carbon-containing precursor comprises perfluoropentane ( $C_5F_{12}$ ).

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