Design Considerations for Mixed-Signal PCB Layout

Application Note

1. Introduction

This application note aims at providing you with some recommendations to achieve better performance from the ADC.

The initial assumptions are the following:

- Proper grounding and routing of all signals is essential to ensure accurate signal conversion
- Eliminate the loop area return by using both separate ground plane and power plane
- Circuitry placement on mixed-signal PCBs is a crucial design point

In many cases, engineers have preconceived notions about mixed-signal designs and how analog and digital placement, partitioning and associated design should be performed.

When laying out components for a mixed-signal PCB, certain considerations are critical to achieve optimum performance. Mixed-signal PCB's are particularly tricky to design since analog devices possess different characteristics compared to digital components: different power rating, current, voltage and heat dissipation requirements, to name a few.

This study shows how to prevent digital logic ground currents from contaminating analog circuitry on a mixed-signal PCB and particularly ADC component.

In our attempt to answer this question, let's keep in mind two basic principles of electromagnetic compatibility. One is that currents should be returned to their source as locally and compactly as possible, through the smallest possible loop area. The second is that a system should have only one reference plane, if not we would create a dipole antenna.

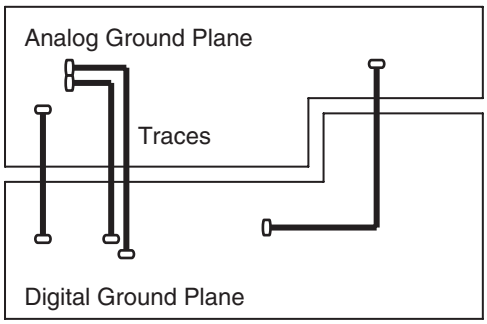
0999B–BDC–08/10

2. Ground Plane Rules and Layout

2.1 Current Loop Area and Ground Plane

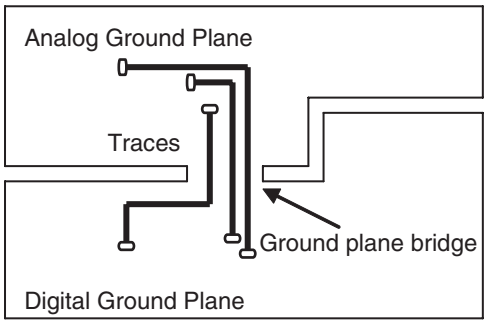
The most interesting aspect to board level designers, is the common return currents of individual components. Any signal running on a PCB trace creates a return current, which flows through the ground connection. This return current follows the route of minimum impedance; it would prefer to run directly under the signal trace.

Figure 2-1. Signal Traces Crossing Over a Slit in the Ground Plane



Bad

Figure 2-2. Analog and Digital Ground Planes Connected Together at a Single Location.



Correct

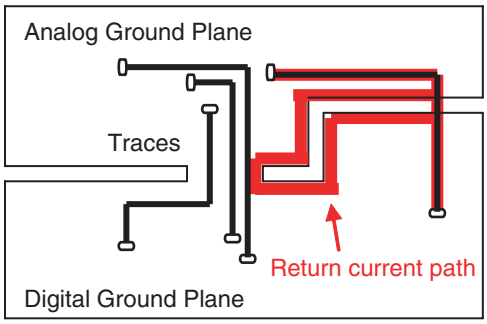
If you have to slit the ground plane and run traces across the slit as shown in Figure 2-1, there would be no return path near the trace and the current would have to flow through a large loop. High-frequency currents flowing in large loops produce radiation and high ground inductance. Low-level analog currents flowing in large loops are susceptible to interference.

The key to determining the optimum mixed-signal board layout is to understand how and where the ground return currents actually flow.

If you need to split the ground plane and run traces across the split, you should first connect the planes together at one location, thus forming a bridge, as shown in Figure 2-2.

Then, by routing all the traces so that they cross at this bridge, you will provide a current return path directly underneath each of the traces, thereby producing a very small loop area. Hence the digital ground currents do not flow in the analog section of the ground plane.

Figure 2-3. When Currents Diverge, a Loop Area is Created



In practice, the current returns must consist of large area ground planes for low impedance to high frequency currents. Without a low-impedance ground plane, it is therefore almost impossible to avoid parasitic resistance and inductance, especially at high frequencies.

Each PCB in the system should have at least one complete layer dedicated to the ground plane. Ideally, a double-sided board should have one side completely dedicated to ground and the other side for interconnections. In practice, it is not always possible, since some of the ground place will certainly have to be removed to allow for signal and power crossovers, vias, and through-holes. Nevertheless, as much area as possible should be preserved, and at least 75% should remain.

2.2 How to Stack-up Properly?

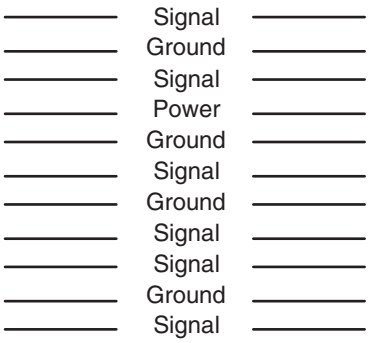
As each PCBs generate EMI, we should take some precautions such as minimizing crosstalk, proper grounding and namely proper layer stack-up which will significantly reduce ElectroMagnetic Interference (EMI) problems.

An ideal stack-up will be a ground plane under each other plane (signal or power). In this case, a signal should not be disrupted by the return current of another signal.

If it is not possible for cost reasons, place each signal layer in between the ground plane and power (or ground) plane. Inductance is directly proportional to the distance an electric charge has to cover from the source of an electric charge to the ground. As the distance gets shorter, the inductance becomes smaller.

Therefore, placing the ground planes close to a signal source reduces inductance and helps contain EMI.

Figure 2-4. Eleven-layer Stack-up



This is an example of an eleven-layer stack-up PCB. In the stack-up, the stripline signal layers are the quietest because they are centered by power and GND planes. A solid ground plane next to the power plane creates a set of low Equivalent Series Resistances (ESR) capacitors. With integrated circuit edge rates becoming faster and faster, these techniques help to contain EMI.

To reduce the number of layers, you might use this configuration: “Ground - Signal - Signal - Ground” instead of “Ground - Signal - Ground - Signal – Ground” (one layer less).

Note: This solution can be used if the signals are differentials.

When two signal layers are side by side, you must route the signals of layer N orthogonal to signals of layer N+1 to minimize crosstalk and parasitic capacitance.

Component selection and proper placement on the board is important to controlling EMI, so be careful about these points:

- Select low-inductance components, such as surface mount capacitors and effective series inductance
- Use solid ground planes next to power planes

2.3 Power Plane (Analog and Digital)

For performance reasons it is always recommended to use separate supplies for digital and analog circuitry.

The digital supply should only be used for parts placed over the digital ground plane, (that is, all pure digital parts). The analog supply is used for all analog and mixed-signal parts.

It is important that a digital power plane does not overlap an analog power plane as shown on Figure 2-5: Bad. This will produce capacitance between the overlapping areas, which is likely to cause RF emissions to pass from one plane to another.

Figure 2-5. Overlapping Analog and Digital Planes

Power planes are designed using the same rules as ground planes. Keep the analog supply plane entirely under the analog ground plane, see on Figure 2-5: Correct. This gives an analog supply plane over the analog ground plane and a digital supply plane over the digital ground plane. In this case, it could not cause unwanted capacitance between the two planes.

Moreover, power supply pins should be decoupled directly to the ground plane. The ceramic capacitor should be located as close as possible to the IC power pins.

Separate power supplies for analog and digital circuits are also highly desirable, even if the voltages are the same. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin, it should be powered from a separate analog supply. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane.

The sampling clock generation circuitry should be treated like analog circuitry and also be grounded and heavily-decoupled to the analog ground plane. It should also be isolated from noisy digital circuits.

Therefore, the ground plane not only acts as a low impedance return path for decoupling high frequency currents but also minimizes RF emissions. Because of the shielding action of the ground plane, the circuits' susceptibility to external RF is also reduced.

3. Board Partitioning

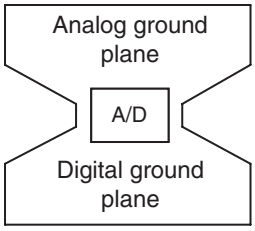
As shown in Section 2.1 "Current Loop Area and Ground Plane" on page 2, the digital ground currents must not flow in the analog section of the ground plane, therefore a specific block architecture is required for the placement of the components.

Correct component placement is very important. This an essential step to ensure how correct analog circuitry signals flow through the PCB, as well as how the planes are split to keep analog functionality separate from the digital section.

For highest system performance, it is important to arrange the different blocks as to ensure that interaction between the potentially noisy circuit blocks and sensitive analog circuits is minimized. For example, short trace lengths reduce the amount of distributed capacitance and mutual inductance between signal routes.

If the system contains only one A/D converter, you can split the ground plane and connect the analog and digital sections together at one place, under the A/D converter and remember that no traces can be routed across the split in the plane. (special care should be taken with the routing).

Figure 3-1. Acceptable Layout of Mixed-signal Board with a Single A/D Converter and a Split Ground Plane



The system star ground occurs where the analog and digital ground planes are joined together at the mixed signal device. While this approach will generally work in a simple system with a single PCB and a single ADC/DAC, it is not optimum for multicard mixed-signal systems.

Additionally, ground planes should be spaced as far apart as possible from each other to avoid coupling issues.

This is an example with a system which contains three devices.

Figure 3-2. Separate Analog and Digital Ground Plane Regions

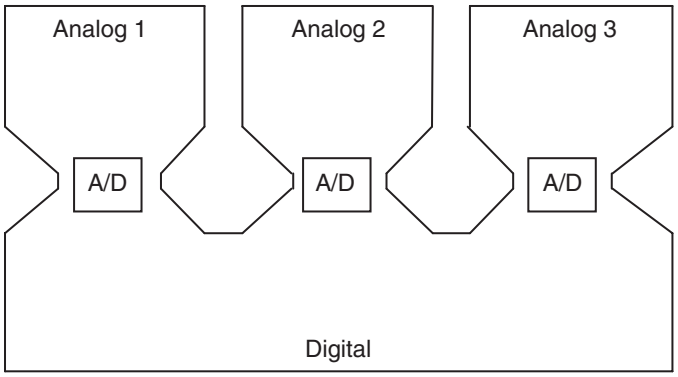


Figure 3-2 shows the best placement method, using an analog-to-digital converter (ADC). One side of the A/D has analog pins resting directly on top of the analog plane, while the other side's digital pins are squarely on the digital plane.

This configuration is ideal but the evaluation board is more and more complex now and some analog signals could be required to go to all ADCs.

For example with the clock input signal:

- This signal is critical and should not be noisy, it should also have very low Jitter and very low noise floor
- It is why the clock buffer must be put on the Analog part of evaluation board
- In systems you have one clock (master clock) for several ADCs
- In this case the clock signal must cross the Analog1, Analog 2 and Analog 3 sections

Figure 3-3. Clock Distribution Bad Configuration

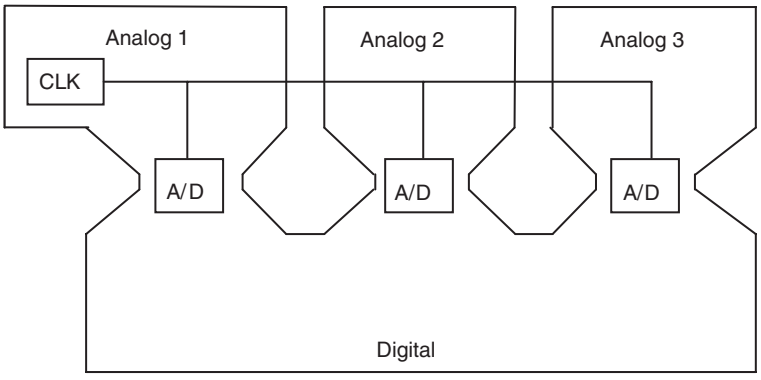
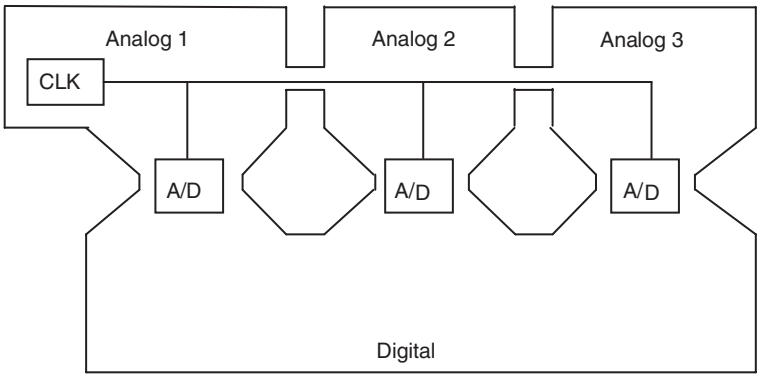


Figure 3-3 shows a bad configuration with the clock signal tracked across the slit. You should first connect the planes Analog1 and Analog 2 together at one location, thus forming a bridge and you must route all trace on this bridge. Figure 3-4 shows a better configuration.

Figure 3-4. Clock Distribution Correct Configuration

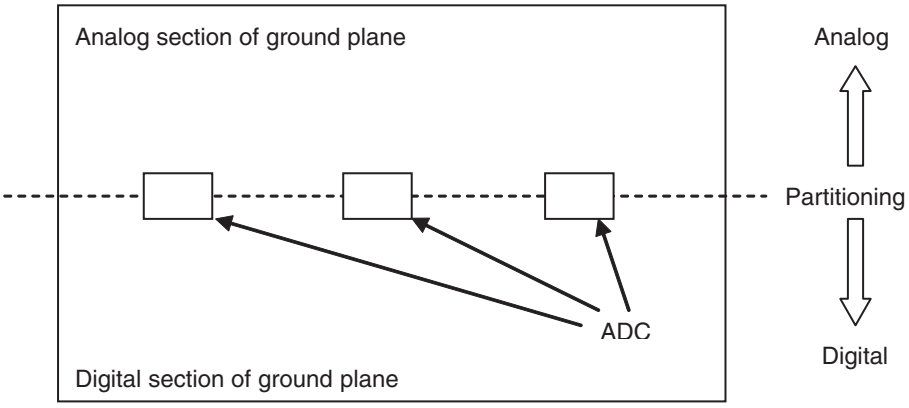


The analog ground plane is therefore not split and is connected by a bridge.

If you have any other signal on the analog partition which must go to ADC 1, ADC 2 and ADC 3 you must use the same method and create a bridge across the split otherwise this method might be difficult to implement on your PCB because of area and layer limitations.

In fact when you have several connections between each analog partition, the best method is to have a single ground plane. Figure 3-5 is not optimal but is easier to implement, it is a good compromise and it is adapted for complex PCBs with multiple layers.

Figure 3-5. Partitioned mixed-signal Board with Multiple A/D Converters and Single Ground Plane



4. Board decoupling capacitors

As indicated in Section 2.3, the effect of power plane configuration and separation between analog part and digital part is very important. Additionally an important point for PCB layout is the decoupling capacitors and decoupling strategy. The capacitors must be soldered at the right position to be efficient.

Usually, the ADC is decoupled following a four-level decoupling capacitors strategy, providing adequate decoupling over frequency taking into account the external decoupling of the evaluation board

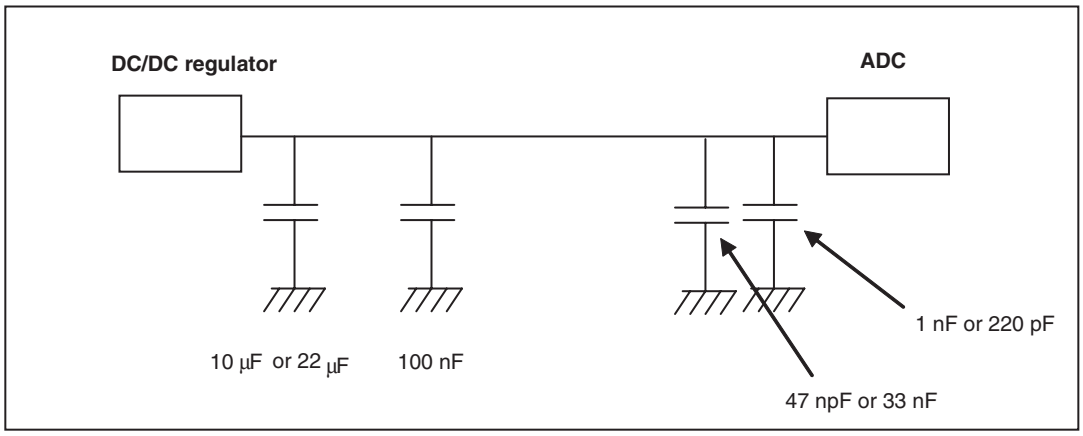
ADC external decoupling: typical values

- At DC/DC regulator level: (1st level and 2nd level): ~ 10 µF or 20 µF (tantalum) in parallel with ~ 100nF capacitor.
- Close to Package: (3rd level and 4th level): ~ 47nF or 33nF chip capacitor in parallel with ~ 1nF or ~ 200pF capacitor depend of ADC.

It is recommended to decouple all power supplies to ground as close as possible to the device balls

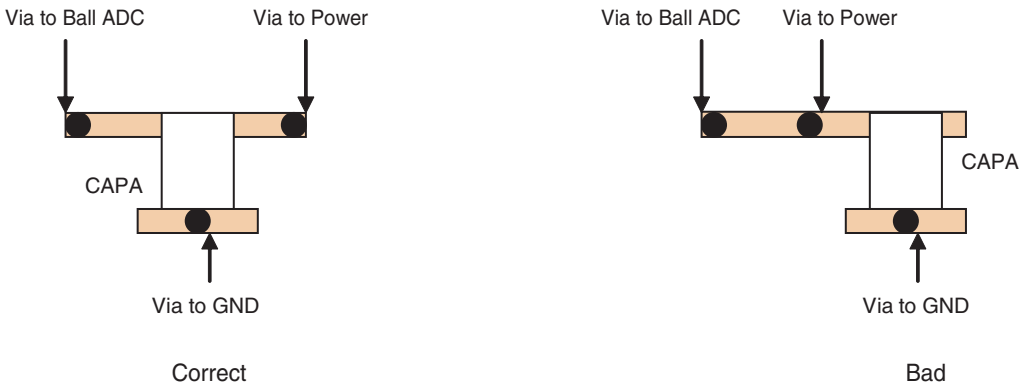
The capacitor strategy could be summarized as; the higher values must be put close to the DC/DC regulator and the lower values must be put close to ADC.

Figure 4-1. Four-row Decoupling Capacitors Lane ADC



Another important point is the position of decoupling capacitor and the power supply. The decoupling capacitor must be put between power supply (via) and ADC ball or ADC pin.

Figure 4-2. Decoupled Capacitor Position



5. Conclusion

This study shows that it is essential to respect the following design rules:

- Do not split the ground plane; use one solid plane under both analog and digital sections of the board
- Use large area ground planes for low impedance current return paths
- Keep over 75% board area for the ground plane
- Separate analog and digital power planes
- Use solid ground planes next to power planes
- Locate all analogue components and lines over the analogue power plane and all digital components and lines over the digital power plane
- Do not route traces over the split in the power planes, unless if traces that must go over the power plane split must be on layers adjacent to the solid ground plane
- Think about where and how the ground return currents are actually flowing
- Partition your PCB with separate analog and digital sections
- Place components properly

If these simple rules are followed, the design should avoid some important mistakes. To conclude, component placement and partitioning, combined with routing discipline, are the keys to success in layout a mixed-signal PCB, not the isolation of the ground planes.

How to reach us

Home page: www.e2v.com

Sales offices:

Europe Regional sales office

e2v ltd

106 Waterhouse Lane

Chelmsford Essex CM1 2QU

England

Tel: +44 (0)1245 493493

Fax: +44 (0)1245 492492

mailto: enquiries@e2v.com

e2v sas

16 Burospace

F-91572 Bièvres Cedex

France

Tel: +33 (0) 16019 5500

Fax: +33 (0) 16019 5529

mailto: enquiries-fr@e2v.com

e2v gmbh

Industriestraße 29

82194 Gröbenzell

Germany

Tel: +49 (0) 8142 41057-0

Fax: +49 (0) 8142 284547

mailto: enquiries-de@e2v.com

Americas

e2v inc

520 White Plains Road

Suite 450 Tarrytown, NY 10591

USA

Tel: +1 (914) 592 6050 or 1-800-342-5338,

Fax: +1 (914) 592-5148

mailto: enquiries-na@e2v.com

Asia Pacific

e2v ltd

11/F.,

Onfem Tower,

29 Wyndham Street,

Central, Hong Kong

Tel: +852 3679 364 8/9

Fax: +852 3583 1084

mailto: enquiries-ap@e2v.com

Product Contact:

e2v

Avenue de Rochepleine

BP 123 - 38521 Saint-Egrève Cedex

France

Tel: +33 (0)4 76 58 30 00

Hotline:

mailto: hotline-bdc@e2v.com