FPGA for POP timing control

Extract from S4.2 of Stuart Kenny’s thesis - Development of a Pulsed Optical Pumped Rubidium Clock

An external 10MHz source is divided (by the internal PLL) to produce a 2.5MHz clock for a 16-bit counter; providing a 400ns tick, for a cycle time of up to 26.2ms.

A screenshot of a computer

Description automatically generated

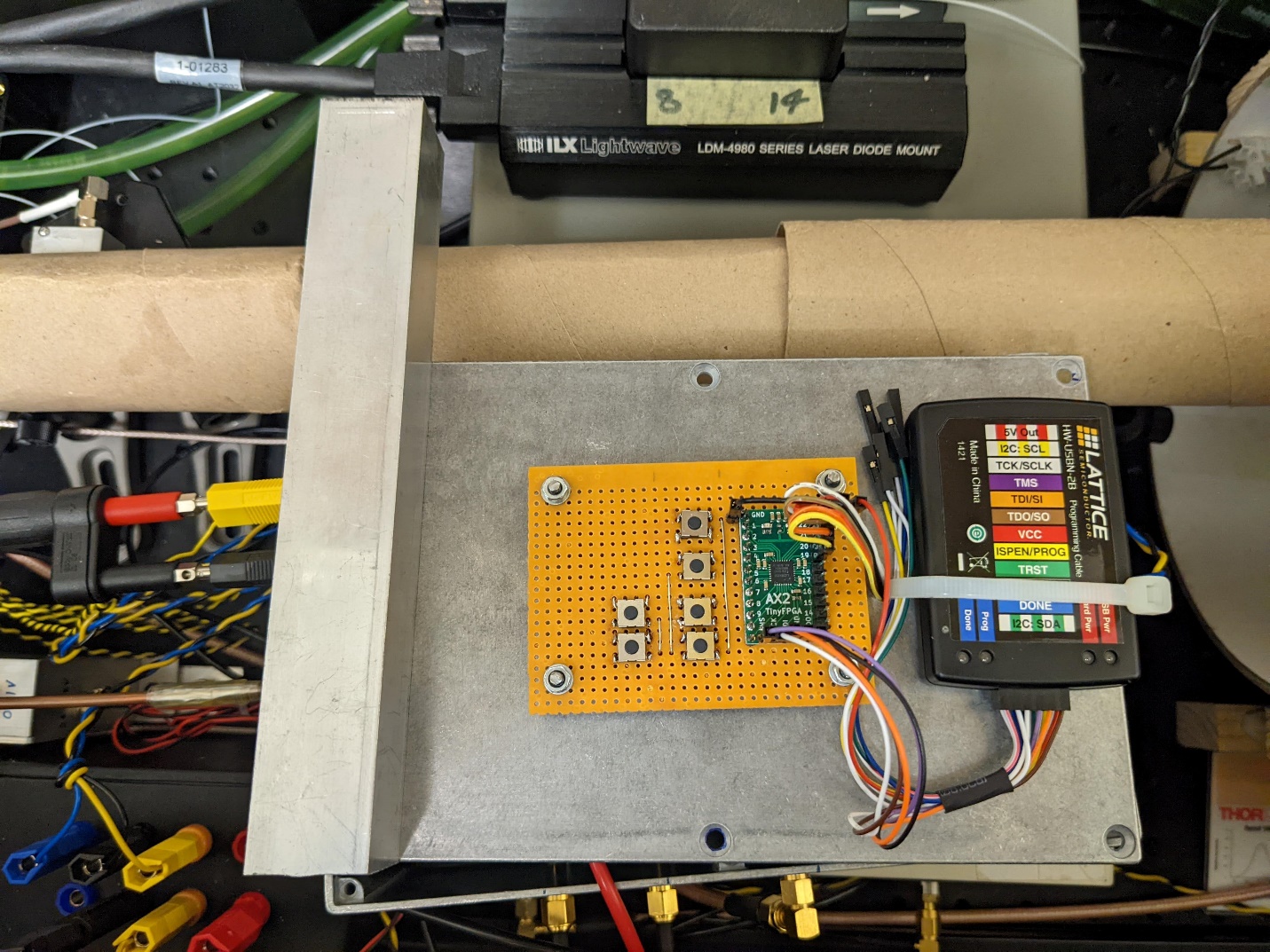
Figure 56. FPGA-based POP cycle timing generation

This timing mechanism is then fed into a state machine with outputs as specified in Table 10. This permits fast changes between laser alignment and POP, and provides other modes useful for experimentation and calibration of the clock.

Table 10. POP timing Field Programmable Gate Array (FPGA) state machine

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | **Outputs** | | | | |
| **Mode** | **Description** | **Pump** | **Probe** | **MW** | **Sample** | **LED** |
| 0 | MCU control | POP cycle timing / laser frequency setup | | | | Control status |
| 1 | Laser frequency setup | 0 | 1 | 0 | 1 | Slow flash |
| 2 | POP cycle | POP cycle timing | | | | On |
| 3 | Dark | 0 | 0 | 0 | 1 | Fast flash |
| 4 | Pump beam calibration | 1 | 0 | 0 | 0 | Off |
| 5 | Double resonance | 0 | 1 | 1 | 1 | 4 quick flashes |
| 6 | Probe with pulsing MW | 0 | 1 | Pulsed | 1 | 3 dots & 1 dash |
| 7 | POP with continuous sample | POP cycle timing | | | 1 | 2 quick flashes |

Mode 0 is the power-on default and allows the MCU to select between laser calibration and POP. It additionally allows the MCU to suppress the sample output, e.g. when the MW frequency is changing, and the output of the Physics Package is not valid. 6 pushbuttons were added as per Figure 57, allowing fast adjustment of functionality and timing.



Mode

Load defaults

{

Adjust

π/2

}

Adjust

free precessing time

Figure 57. Mach X02 1200HC FPGA and JTAG programmer/debugger.

After debugging, the FPGA’s behaviour was verified and the control sequence necessary for one POP cycle is shown in the outputs seen in Figure 58.

A screen shot of a computer

Description automatically generated

Figure 58. FPGA outputs as used to control a single POP cycle.

All of the RTL (Verilog) and testbenches for the FPGA were written from scratch, and are available on the Github online software repository - [POP\_timing\_FPGA](https://github.com/StuartKenny/POP_timing_FPGA).