β

CHAPTER

3 Bipolar Junction Transistors

3.1 INTRODUCTION

During the period 1904–1947, the vacuum tube was undoubtedly the electronic device of interest and development. In 1904, the vacuum-tube diode was introduced by J. A. Fleming. Shortly thereafter, in 1906, Lee De Forest added a third element, called the *control grid*, to the vacuum diode, resulting in the first amplifier, the *triode*. In the following years, radio and television provided great stimulation to the tube industry. Production rose from about 1 million tubes in 1922 to about 100 million in 1937. In the early 1930s the four-element tetrode and five-element pentode gained prominence in the electron-tube industry. In the years to follow, the industry became one of primary importance and rapid advances were made in design, manufacturing techniques, high-power and high-frequency applications, and miniaturization.

On December 23, 1947, however, the electronics industry was to experience the advent of a completely new direction of interest and development. It was on the afternoon of this day that Walter H. Brattain and John Bardeen demonstrated the amplifying action of the first transistor at the Bell Telephone Laboratories. The original transistor (a point-contact transistor) is shown in Fig. 3.1. The advantages of this three-terminal solid-state device over the tube were immediately obvious: It was smaller

Co-inventors of the first transistor at Bell Laboratories: Dr. William Shockley (seated); Dr. John Bardeen (left); Dr. Walter H. Brattain. (Courtesy of AT&T Archives.)

Dr. Shockley Born: London, England, 1910
PhD Harvard, 1936

Dr. Bardeen Born: Madison, Wisconsin, 1908
PhD Princeton, 1936

Dr. Brattain Born: Amoy, China, 1902
PhD University of Minnesota, 1928

All shared the Nobel Prize in 1956 for this contribution.

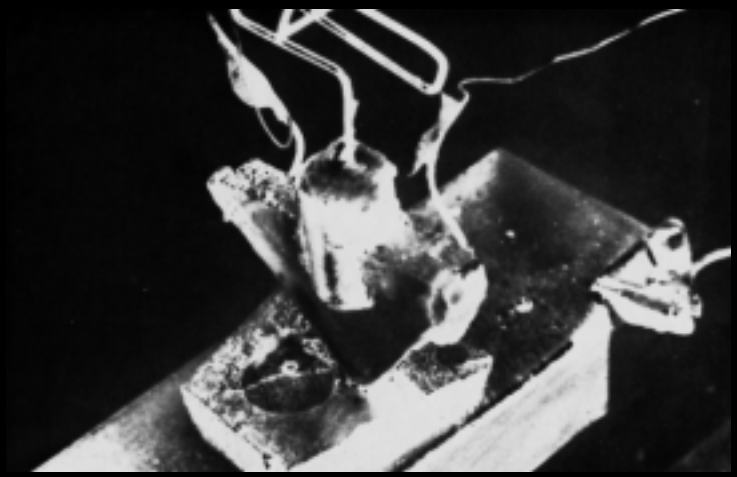


Figure 3.1 The first transistor. (Courtesy Bell Telephone Laboratories.)

and lightweight; had no heater requirement or heater loss; had rugged construction; and was more efficient since less power was absorbed by the device itself; it was instantly available for use, requiring no warm-up period; and lower operating voltages were possible. Note in the discussion above that this chapter is our first discussion of devices with three or more terminals. You will find that all amplifiers (devices that increase the voltage, current, or power level) will have at least three terminals with one controlling the flow between two other terminals.

3.2 TRANSISTOR CONSTRUCTION

The transistor is a three-layer semiconductor device consisting of either two *n*- and one *p*-type layers of material or two *p*- and one *n*-type layers of material. The former is called an *npn transistor,* while the latter is called a *pnp transistor.* Both are shown in Fig. 3.2 with the proper dc biasing. We will find in Chapter 4 that the dc biasing is necessary to establish the proper region of operation for ac amplification. The emitter layer is heavily doped, the base lightly doped, and the collector only lightly doped. The outer layers have widths much greater than the sandwiched *p*- or *n*-type material. For the transistors shown in Fig. 3.2 the ratio of the total width to that of the center layer is 0.150/0.001 = 150 : 1. The doping of the sandwiched layer is also considerably less than that of the outer layers (typically, 10 : 1 or less). This lower doping level decreases the conductivity (increases the resistance) of this material by limiting the number of "free" carriers.

For the biasing shown in Fig. 3.2 the terminals have been indicated by the capital letters *E* for *emitter, C* for *collector,* and *B* for *base.* An appreciation for this choice of notation will develop when we discuss the basic operation of the transistor. The abbreviation BJT, from *bipolar junction transistor,* is often applied to this three-terminal device. The term *bipolar* reflects the fact that holes *and* electrons participate in the injection process into the oppositely polarized material. If only one carrier is employed (electron or hole), it is considered a *unipolar* device. The Schottky diode of Chapter 20 is such a device.

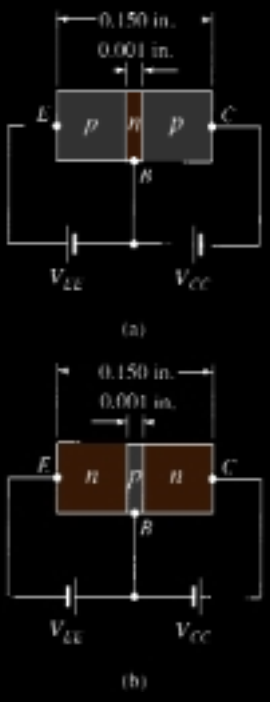


Figure 3.2 Types of transistors: (a) *pnp*; (b) *npn*.

3.3 TRANSISTOR OPERATION

The basic operation of the transistor will now be described using the *pnp* transistor of Fig. 3.2a. The operation of the *npn* transistor is exactly the same if the roles played by the electron and hole are interchanged. In Fig. 3.3 the *pnp* transistor has been redrawn without the base-to-collector bias. Note the similarities between this situation and that of the *forward-biased* diode in Chapter 1. The depletion region has been reduced in width due to the applied bias, resulting in a heavy flow of majority carriers from the *p*- to the *n*-type material.

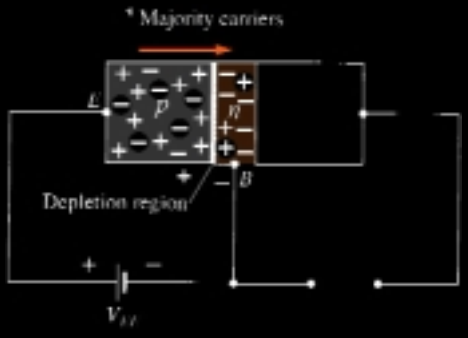


Figure 3.3 Forward-biased junction of a *pnp* transistor.

β

Let us now remove the base-to-emitter bias of the *pnp* transistor of Fig. 3.2a as shown in Fig. 3.4. Consider the similarities between this situation and that of the *reverse-biased* diode of Section 1.6. Recall that the flow of majority carriers is zero, resulting in only a minority-carrier flow, as indicated in Fig. 3.4. In summary, therefore:

One p-n junction of a transistor is reverse biased, while the other is forward biased.

In Fig. 3.5 both biasing potentials have been applied to a *pnp* transistor, with the resulting majority- and minority-carrier flow indicated. Note in Fig. 3.5 the widths of the depletion regions, indicating clearly which junction is forward-biased and which is reverse-biased. As indicated in Fig. 3.5, a large number of majority carriers will diffuse across the forward-biased *p-n* junction into the *n*-type material. The question then is whether these carriers will contribute directly to the base current I_B or pass directly into the *p*-type material. Since the sandwiched *n*-type material is very thin and has a low conductivity, a very small number of these carriers will take this path of high resistance to the base terminal. The magnitude of the base current is typically on the order of microamperes as compared to milliamperes for the emitter and collector currents. The larger number of these majority carriers will diffuse across the reverse-biased junction into the *p*-type material connected to the collector terminal as indicated in Fig. 3.5. The reason for the relative ease with which the majority carriers can cross the reverse-biased junction is easily understood if we consider that for the reverse-biased diode the injected majority carriers will appear as minority carriers in the *n*-type material. In other words, there has been an *injection* of minority carriers into the *n*-type base region material. Combining this with the fact that all the minority carriers in the depletion region will cross the reverse-biased junction of a diode accounts for the flow indicated in Fig. 3.5.

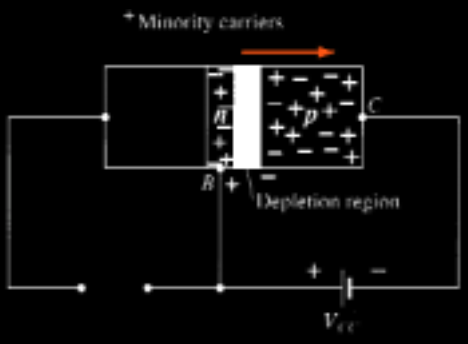


Figure 3.4 Reverse-biased junction of a *pnp* transistor.

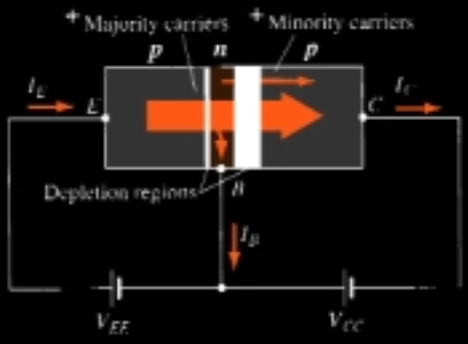


Figure 3.5 Majority and minority carrier flow of a *pnp* transistor.

Applying Kirchhoff's current law to the transistor of Fig. 3.5 as if it were a single node, we obtain

$$I_E = I_C + I_B \tag{3.1}$$

and find that the emitter current is the sum of the collector and base currents. The collector current, however, is comprised of two components—the majority and minority carriers as indicated in Fig. 3.5. The minority-current component is called the *leakage current* and is given the symbol I_{CO} (I_C current with emitter terminal *O*pen). The collector current, therefore, is determined in total by Eq. (3.2).

$$I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}} \tag{3.2}$$

For general-purpose transistors, I_C is measured in milliamperes, while I_{CO} is measured in microamperes or nanoamperes. I_{CO}, like I_s for a reverse-biased diode, is temperature sensitive and must be examined carefully when applications of wide temperature ranges are considered. It can severely affect the stability of a system at high temperature if not considered properly. Improvements in construction techniques have resulted in significantly lower levels of I_{CO}, to the point where its effect can often be ignored.

3.4 COMMON-BASE CONFIGURATION

The notation and symbols used in conjunction with the transistor in the majority of texts and manuals published today are indicated in Fig. 3.6 for the common-base configuration with *pnp* and *npn* transistors. The common-base terminology is derived from the fact that the base is common to both the input and output sides of the configuration. In addition, the base is usually the terminal closest to, or at, ground potential. Throughout this book all current directions will refer to conventional (hole) flow rather than electron flow. This choice was based primarily on the fact that the vast amount of literature available at educational and industrial institutions employs conventional flow and the arrows in all electronic symbols have a direction defined by this convention. Recall that the arrow in the diode symbol defined the direction of conduction for conventional current. For the transistor:

The arrow in the graphic symbol defines the direction of emitter current (conventional flow) through the device.

All the current directions appearing in Fig. 3.6 are the actual directions as defined by the choice of conventional flow. Note in each case that $I_E = I_C + I_B$. Note also that the applied biasing (voltage sources) are such as to establish current in the direction indicated for each branch. That is, compare the direction of I_E to the polarity or V_{EE} for each configuration and the direction of I_C to the polarity of V_{CC}.

To fully describe the behavior of a three-terminal device such as the common-base amplifiers of Fig. 3.6 requires two sets of characteristics—one for the *driving point* or *input* parameters and the other for the *output* side. The input set for the common-base amplifier as shown in Fig. 3.7 will relate an input current (I_E) to an input voltage (V_{BE}) for various levels of output voltage (V_{CB}).

The output set will relate an output current (I_C) to an output voltage (V_{CB}) for various levels of input current (I_E) as shown in Fig. 3.8. The output or *collector* set of characteristics has three basic regions of interest, as indicated in Fig. 3.8: the *active*,

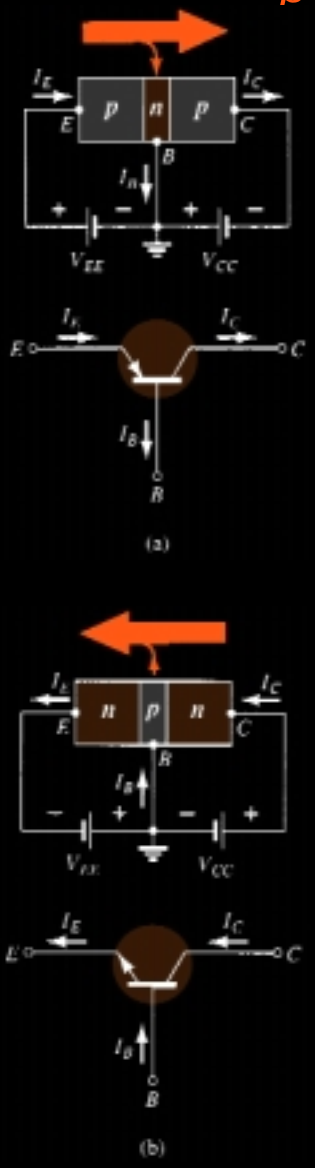


Figure 3.6 Notation and symbols used with the common-base configuration: (a) *pnp* transistor; (b) *npn* transistor.

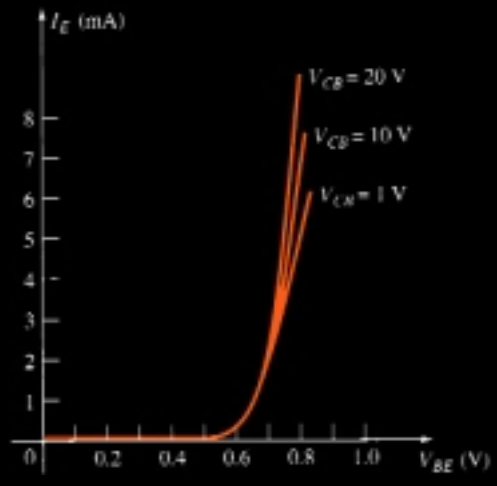


Figure 3.7 Input or driving point characteristics for a common-base silicon transistor amplifier.

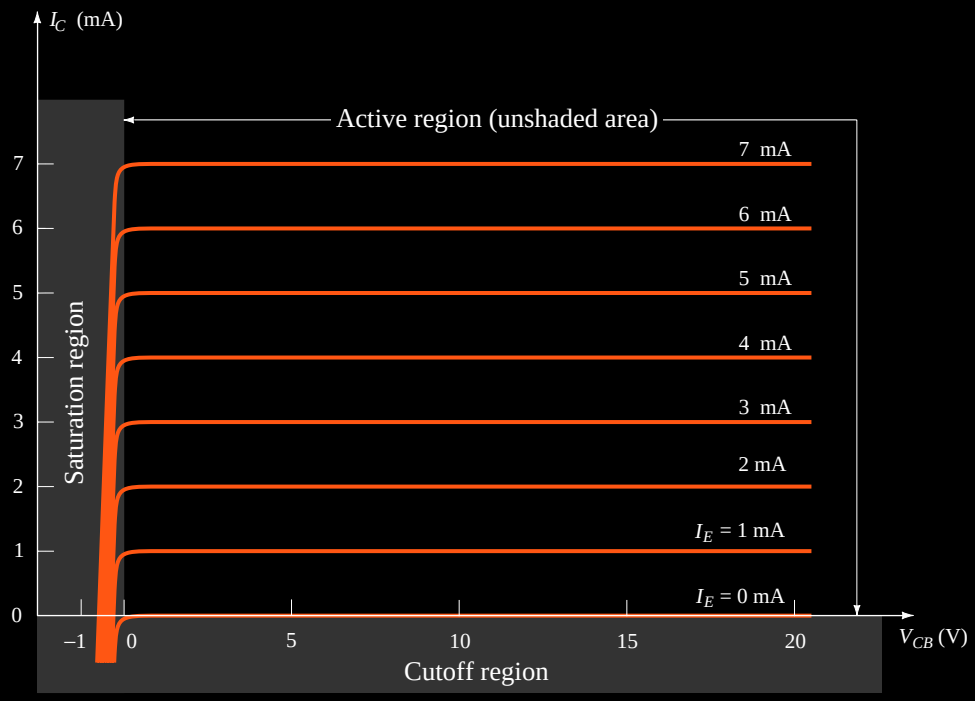


Figure 3.8 Output or collector characteristics for a common-base transistor amplifier.

cutoff, and *saturation* regions. The active region is the region normally employed for linear (undistorted) amplifiers. In particular:

In the active region the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.

The active region is defined by the biasing arrangements of Fig. 3.6. At the lower end of the active region the emitter current (I_E) is zero, the collector current is simply that due to the reverse saturation current I_{CO}, as indicated in Fig. 3.8. The current I_{CO} is so small (microamperes) in magnitude compared to the vertical scale of I_C (milliamperes) that it appears on virtually the same horizontal line as $I_C = 0$. The circuit conditions that exist when $I_E = 0$ for the common-base configuration are shown in Fig. 3.9. The notation most frequently used for I_{CO} on data and specification sheets is, as indicated in Fig. 3.9, I_{CBO}. Because of improved construction techniques, the level of I_{CBO} for general-purpose transistors (especially silicon) in the low- and mid-power ranges is usually so low that its effect can be ignored. However, for higher power units I_{CBO} will still appear in the microampere range. In addition, keep in mind that I_{CBO}, like I_s, for the diode (both reverse leakage currents) is temperature sensitive. At higher temperatures the effect of I_{CBO} may become an important factor since it increases so rapidly with temperature.

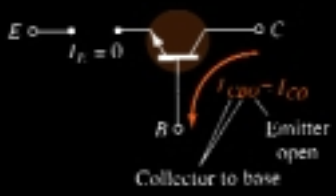


Figure 3.9 Reverse saturation current.

Note in Fig. 3.8 that as the emitter current increases above zero, the collector current increases to a magnitude essentially equal to that of the emitter current as determined by the basic transistor-current relations. Note also the almost negligible effect of V_{CB} on the collector current for the active region. The curves clearly indicate that *a first approximation to the relationship between I_E and I_C in the active region is given by*

$$I_C \cong I_E \tag{3.3}$$

As inferred by its name, the cutoff region is defined as that region where the collector current is 0 A, as revealed on Fig. 3.8. In addition:

In the cutoff region the collector-base and base-emitter junctions of a transistor are both reverse-biased.

The saturation region is defined as that region of the characteristics to the left of $V_{CB} = 0$ V. The horizontal scale in this region was expanded to clearly show the dramatic change in characteristics in this region. Note the exponential increase in collector current as the voltage V_{CB} increases toward 0 V.

In the saturation region the collector-base and base-emitter junctions are forward-biased.

The input characteristics of Fig. 3.7 reveal that for fixed values of collector voltage (V_{CB}), as the base-to-emitter voltage increases, the emitter current increases in a manner that closely resembles the diode characteristics. In fact, increasing levels of V_{CB} have such a small effect on the characteristics that as a first approximation the change due to changes in V_{CB} can be ignored and the characteristics drawn as shown in Fig. 3.10a. If we then apply the piecewise-linear approach, the characteristics of Fig. 3.10b will result. Taking it a step further and ignoring the slope of the curve and therefore the resistance associated with the forward-biased junction will result in the characteristics of Fig. 3.10c. For the analysis to follow in this book the equivalent model of Fig. 3.10c will be employed for all dc analysis of transistor networks. That is, once a transistor is in the "on" state, the base-to-emitter voltage will be assumed to be the following:

$$V_{BE} = 0.7 \text{ V} \tag{3.4}$$

In other words, the effect of variations due to V_{CB} and the slope of the input characteristics will be ignored as we strive to analyze transistor networks in a manner that will provide a good approximation to the actual response without getting too involved with parameter variations of less importance.

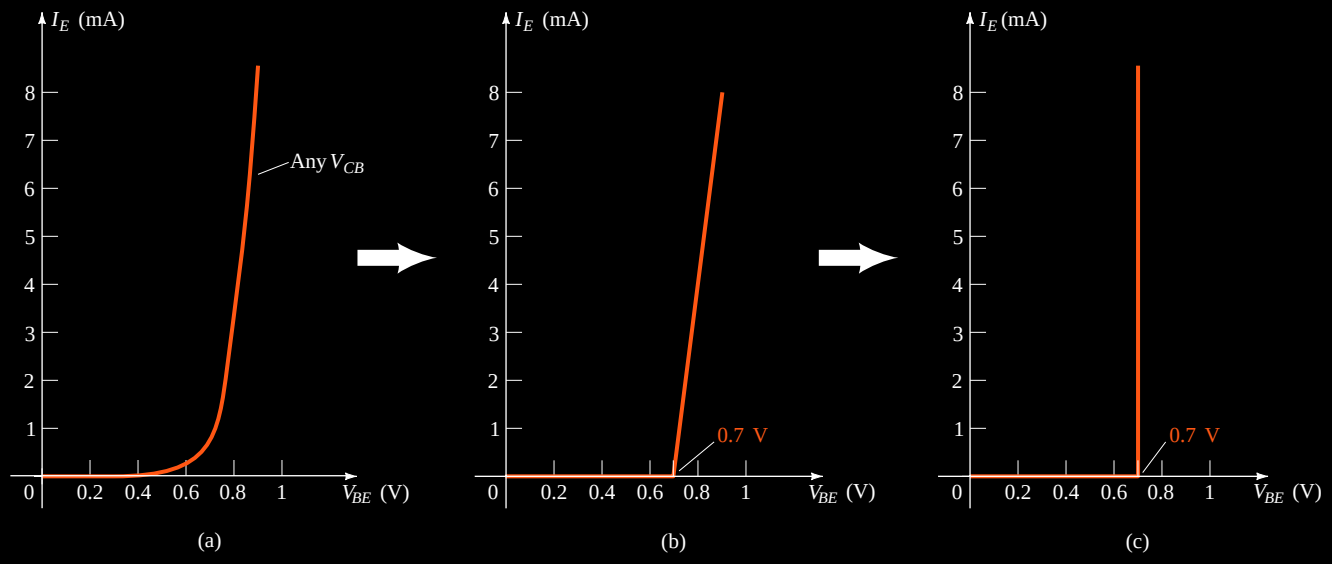


Figure 3.10 Developing the equivalent model to be employed for the base-to-emitter region of an amplifier in the dc mode.

It is important to fully appreciate the statement made by the characteristics of Fig. 3.10c. They specify that with the transistor in the "on" or active state the voltage from base to emitter will be 0.7 V at *any* level of emitter current as controlled by the external network. In fact, at the first encounter of any transistor configuration in the dc mode, one can now immediately specify that the voltage from base to emitter is 0.7 V if the device is in the active region—a very important conclusion for the dc analysis to follow.

EXAMPLE 3.1

(a) Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_E = 3$ mA and $V_{CB} = 10$ V.
(b) Using the characteristics of Fig. 3.8, determine the resulting collector current if I_E remains at 3 mA but V_{CB} is reduced to 2 V.
(c) Using the characteristics of Figs. 3.7 and 3.8, determine V_{BE} if $I_C = 4$ mA and $V_{CB} = 20$ V.
(d) Repeat part (c) using the characteristics of Figs. 3.8 and 3.10c.

Solution

(a) The characteristics clearly indicate that $I_C \cong I_E = \mathbf{3\ mA}$.
(b) The effect of changing V_{CB} is negligible and I_C continues to be **3 mA.**
(c) From Fig. 3.8, $I_E \cong I_C = 4$ mA. On Fig. 3.7 the resulting level of V_{BE} is about **0.74 V.**
(d) Again from Fig. 3.8, $I_E \cong I_C = 4$ mA. However, on Fig. 3.10c, V_{BE} is **0.7 V** for any level of emitter current.

Alpha (α)

In the dc mode the levels of I_C and I_E due to the majority carriers are related by a quantity called *alpha* and defined by the following equation:

$$\alpha_{\text{dc}} = \frac{I_C}{I_E} \tag{3.5}$$

where I_C and I_E are the levels of current at the point of operation. Even though the characteristics of Fig. 3.8 would suggest that $\alpha = 1$, for practical devices the level of alpha typically extends from 0.90 to 0.998, with most approaching the high end of the range. Since alpha is defined solely for the majority carriers, Eq. (3.2) becomes

$$I_C = \alpha I_E + I_{CBO} \tag{3.6}$$

For the characteristics of Fig. 3.8 when $I_E = 0$ mA, I_C is therefore equal to I_{CBO}, but as mentioned earlier, the level of I_{CBO} is usually so small that it is virtually undetectable on the graph of Fig. 3.8. In other words, when $I_E = 0$ mA on Fig. 3.8, I_C also appears to be 0 mA for the range of V_{CB} values.

For ac situations where the point of operation moves on the characteristic curve, an ac alpha is defined by

$$\alpha_{\text{ac}} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}\ =\ \text{constant}} \tag{3.7}$$

The ac alpha is formally called the *common-base, short-circuit, amplification factor,* for reasons that will be more obvious when we examine transistor equivalent circuits in Chapter 7. For the moment, recognize that Eq. (3.7) specifies that a relatively small change in collector current is divided by the corresponding change in I_E with the collector-to-base voltage held constant. For most situations the magnitudes of α_{ac} and α_{dc} are quite close, permitting the use of the magnitude of one for the other. The use of an equation such as (3.7) will be demonstrated in Section 3.6.

Biasing

The proper biasing of the common-base configuration in the active region can be determined quickly using the approximation $I_C \cong I_E$ and assuming for the moment that

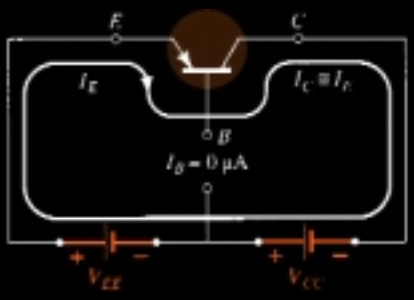


Figure 3.11 Establishing the proper biasing management for a common-base *pnp* transistor in the active region.

$I_B \cong 0\ \mu A$. The result is the configuration of Fig. 3.11 for the *pnp* transistor. The arrow of the symbol defines the direction of conventional flow for $I_E \cong I_C$. The dc supplies are then inserted with a polarity that will support the resulting current direction. For the *npn* transistor the polarities will be reversed.

Some students feel that they can remember whether the arrow of the device symbol in pointing in or out by matching the letters of the transistor type with the appropriate letters of the phrases "pointing in" or "not pointing in." For instance, there is a match between the letters *npn* and the italic letters of *n*ot *p*ointing i*n* and the letters *pnp* with *p*ointing i*n*.

3.5 TRANSISTOR AMPLIFYING ACTION

Now that the relationship between I_C and I_E has been established in Section 3.4, the basic amplifying action of the transistor can be introduced on a surface level using the network of Fig. 3.12. The dc biasing does not appear in the figure since our interest will be limited to the ac response. For the common-base configuration the ac input resistance determined by the characteristics of Fig. 3.7 is quite small and typically varies from 10 to 100 Ω. The output resistance as determined by the curves of Fig. 3.8 is quite high (the more horizontal the curves the higher the resistance) and typically varies from 50 kΩ to 1 MΩ (100 kΩ for the transistor of Fig. 3.12). The difference in resistance is due to the forward-biased junction at the input (base to emitter) and the reverse-biased junction at the output (base to collector). Using a common value of 20 Ω for the input resistance, we find that

$$I_i = \frac{V_i}{R_i} = \frac{200\ \text{mV}}{20\ \Omega} = \mathbf{10\ mA}$$

If we assume for the moment that $\alpha_{ac} = 1$ ($I_c = I_e$),

$$I_L = I_i = 10\ \text{mA}$$

and

$$V_L = I_L R$$
$$= (10\ \text{mA})(5\ \text{k}\Omega)$$
$$= \mathbf{50\ V}$$

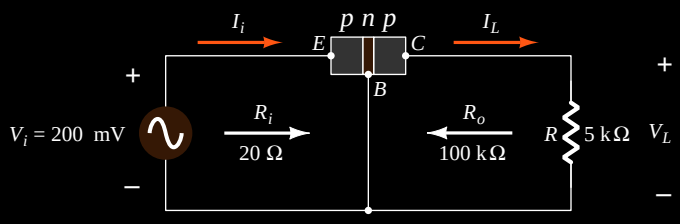


Figure 3.12 Basic voltage amplification action of the common-base configuration.

β

The voltage amplification is

$$A_v = \frac{V_L}{V_i} = \frac{50\text{ V}}{200\text{ mV}} = \mathbf{250}$$

Typical values of voltage amplification for the common-base configuration vary from 50 to 300. The current amplification (I_C/I_E) is always less than 1 for the common-base configuration. This latter characteristic should be obvious since $I_C = \alpha I_E$ and α is always less than 1.

The basic amplifying action was produced by transferring a current I from a low- to a high-*resistance* circuit. The combination of the two terms in italics results in the label *transistor;* that is,

$$\textit{trans}\text{fer} + \text{res}\textit{istor} \rightarrow \textit{transistor}$$

3.6 COMMON-EMITTER CONFIGURATION

The most frequently encountered transistor configuration appears in Fig. 3.13 for the *pnp* and *npn* transistors. It is called the *common-emitter configuration* since the emitter is common or reference to both the input and output terminals (in this case common to both the base and collector terminals). Two sets of characteristics are again necessary to describe fully the behavior of the common-emitter configuration: one for the *input* or *base-emitter* circuit and one for the *output* or *collector-emitter* circuit. Both are shown in Fig. 3.14.

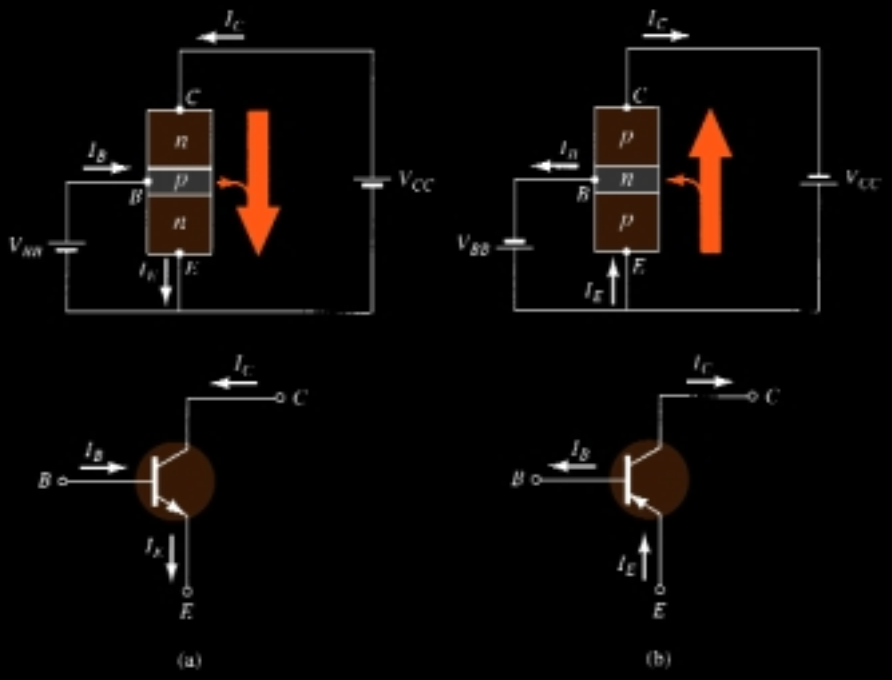


Figure 3.13 Notation and symbols used with the common-emitter configuration: (a) *npn* transistor; (b) *pnp* transistor.

The emitter, collector, and base currents are shown in their actual conventional current direction. Even though the transistor configuration has changed, the current relations developed earlier for the common-base configuration are still applicable. That is, $I_E = I_C + I_B$ and $I_C = \alpha I_E$.

For the common-emitter configuration the output characteristics are a plot of the output current (I_C) versus output voltage (V_{CE}) for a range of values of input current (I_B). The input characteristics are a plot of the input current (I_B) versus the input voltage (V_{BE}) for a range of values of output voltage (V_{CE}).

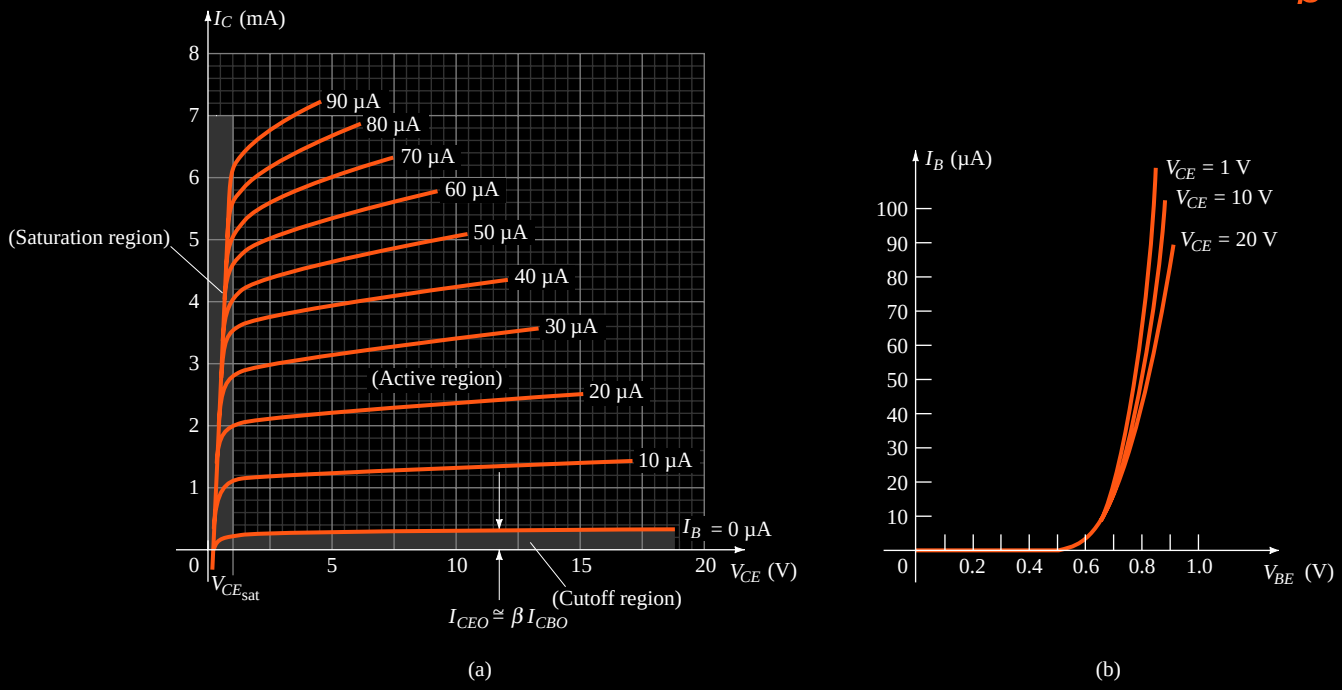


Figure 3.14 Characteristics of a silicon transistor in the common-emitter configuration: (a) collector characteristics; (b) base characteristics.

Note that on the characteristics of Fig. 3.14 the magnitude of I_B is in microamperes, compared to milliamperes of I_C. Consider also that the curves of I_B are not as horizontal as those obtained for I_E in the common-base configuration, indicating that the collector-to-emitter voltage will influence the magnitude of the collector current.

The active region for the common-emitter configuration is that portion of the upper-right quadrant that has the greatest linearity, that is, that region in which the curves for I_B are nearly straight and equally spaced. In Fig. 3.14a this region exists to the right of the vertical dashed line at $V_{CE_{sat}}$ and above the curve for I_B equal to zero. The region to the left of $V_{CE_{sat}}$ is called the saturation region.

In the active region of a common-emitter amplifier the collector-base junction is reverse-biased, while the base-emitter junction is forward-biased.

You will recall that these were the same conditions that existed in the active region of the common-base configuration. The active region of the common-emitter configuration can be employed for voltage, current, or power amplification.

The cutoff region for the common-emitter configuration is not as well defined as for the common-base configuration. Note on the collector characteristics of Fig. 3.14 that I_C is not equal to zero when I_B is zero. For the common-base configuration, when the input current I_E was equal to zero, the collector current was equal only to the reverse saturation current I_{CO}, so that the curve $I_E = 0$ and the voltage axis were, for all practical purposes, one.

The reason for this difference in collector characteristics can be derived through the proper manipulation of Eqs. (3.3) and (3.6). That is,

$$\text{Eq. (3.6):} \quad I_C = \alpha I_E + I_{CBO}$$

Substitution gives $\quad \text{Eq. (3.3):} \quad I_C = \alpha(I_C + I_B) + I_{CBO}$

Rearranging yields

$$I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_{CBO}}{1 - \alpha} \tag{3.8}$$

If we consider the case discussed above, where $I_B = 0$ A, and substitute a typical value of α such as 0.996, the resulting collector current is the following:

$$I_C = \frac{\alpha(0\text{ A})}{1-\alpha} + \frac{I_{CBO}}{1-0.996}$$

$$= \frac{I_{CBO}}{0.004} = 250I_{CBO}$$

If I_{CBO} were 1 μA, the resulting collector current with $I_B = 0$ A would be 250(1 μA) = 0.25 mA, as reflected in the characteristics of Fig. 3.14.

For future reference, the collector current defined by the condition $I_B = 0$ μA will be assigned the notation indicated by Eq. (3.9).

$$I_{CEO} = \left.\frac{I_{CBO}}{1-\alpha}\right|_{I_B = 0\ \mu A} \tag{3.9}$$

In Fig. 3.15 the conditions surrounding this newly defined current are demonstrated with its assigned reference direction.

For linear (least distortion) amplification purposes, cutoff for the common-emitter configuration will be defined by $I_C = I_{CEO}$.

In other words, the region below $I_B = 0$ μA is to be avoided if an undistorted output signal is required.

When employed as a switch in the logic circuitry of a computer, a transistor will have two points of operation of interest: one in the cutoff and one in the saturation region. The cutoff condition should ideally be $I_C = 0$ mA for the chosen V_{CE} voltage. Since I_{CEO} is typically low in magnitude for silicon materials, *cutoff will exist for switching purposes when $I_B = 0$ μA or $I_C = I_{CEO}$ for silicon transistors only. For germanium transistors, however, cutoff for switching purposes will be defined as those conditions that exist when $I_C = I_{CBO}$*. This condition can normally be obtained for germanium transistors by reverse-biasing the base-to-emitter junction a few tenths of a volt.

Recall for the common-base configuration that the input set of characteristics was approximated by a straight-line equivalent that resulted in $V_{BE} = 0.7$ V for any level of I_E greater than 0 mA. For the common-emitter configuration the same approach can be taken, resulting in the approximate equivalent of Fig. 3.16. The result supports our earlier conclusion that for a transistor in the "on" or active region the base-to-emitter voltage is 0.7 V. In this case the voltage is fixed for any level of base current.

Figure 3.15 Circuit conditions related to I_{CEO}.

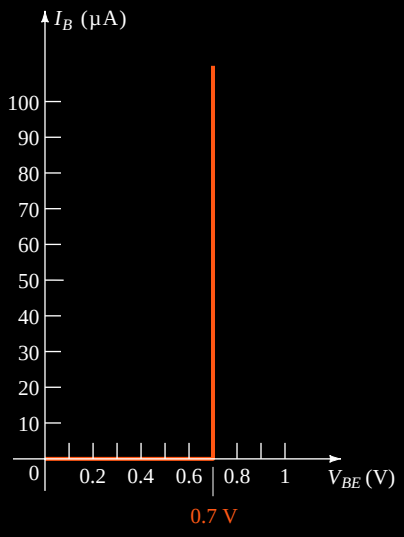


Figure 3.16 Piecewise-linear equivalent for the diode characteristics of Fig. 3.14b.

EXAMPLE 3.2

(a) Using the characteristics of Fig. 3.14, determine I_C at $I_B = 30\ \mu A$ and $V_{CE} = 10$ V.
(b) Using the characteristics of Fig. 3.14, determine I_C at $V_{BE} = 0.7$ V and $V_{CE} = 15$ V.

Solution

(a) At the intersection of $I_B = 30\ \mu A$ and $V_{CE} = 10$ V, $I_C = \mathbf{3.4\ mA}$.
(b) Using Fig. 3.14b, $I_B = 20\ \mu A$ at $V_{BE} = 0.7$ V. From Fig. 3.14a we find that $I_C = \mathbf{2.5\ mA}$ at the intersection of $I_B = 20\ \mu A$ and $V_{CE} = 15$ V.

Beta (β)

In the dc mode the levels of I_C and I_B are related by a quantity called *beta* and defined by the following equation:

$$\beta_{dc} = \frac{I_C}{I_B} \tag{3.10}$$

where I_C and I_B are determined at a particular operating point on the characteristics. For practical devices the level of β typically ranges from about 50 to over 400, with most in the midrange. As for α, β certainly reveals the relative magnitude of one current to the other. For a device with a β of 200, the collector current is 200 times the magnitude of the base current.

On specification sheets β_{dc} is usually included as h_{FE} with the h derived from an ac *h*ybrid equivalent circuit to be introduced in Chapter 7. The subscripts *FE* are derived from *f*orward-current amplification and common-*e*mitter configuration, respectively.

For ac situations an ac beta has been defined as follows:

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} \tag{3.11}$$

The formal name for β_{ac} is *common-emitter, forward-current, amplification factor.* Since the collector current is usually the output current for a common-emitter configuration and the base current the input current, the term *amplification* is included in the nomenclature above.

Equation (3.11) is similar in format to the equation for α_{ac} in Section 3.4. The procedure for obtaining α_{ac} from the characteristic curves was not described because of the difficulty of actually measuring changes of I_C and I_E on the characteristics. Equation (3.11), however, is one that can be described with some clarity, and in fact, the result can be used to find α_{ac} using an equation to be derived shortly.

On specification sheets β_{ac} is normally referred to as h_{fe}. Note that the only difference between the notation used for the dc beta, specifically, $\beta_{dc} = h_{FE}$, is the type of lettering for each subscript quantity. The lowercase letter h continues to refer to the hybrid equivalent circuit to be described in Chapter 7 and the *fe* to the *f*orward current gain in the common-*e*mitter configuration.

The use of Eq. (3.11) is best described by a numerical example using an actual set of characteristics such as appearing in Fig. 3.14a and repeated in Fig. 3.17. Let us determine β_{ac} for a region of the characteristics defined by an operating point of $I_B = 25\ \mu A$ and $V_{CE} = 7.5$ V as indicated on Fig. 3.17. The restriction of $V_{CE} =$ constant requires that a vertical line be drawn through the operating point at $V_{CE} = 7.5$ V. At any location on this vertical line the voltage V_{CE} is 7.5 V, a constant. The change

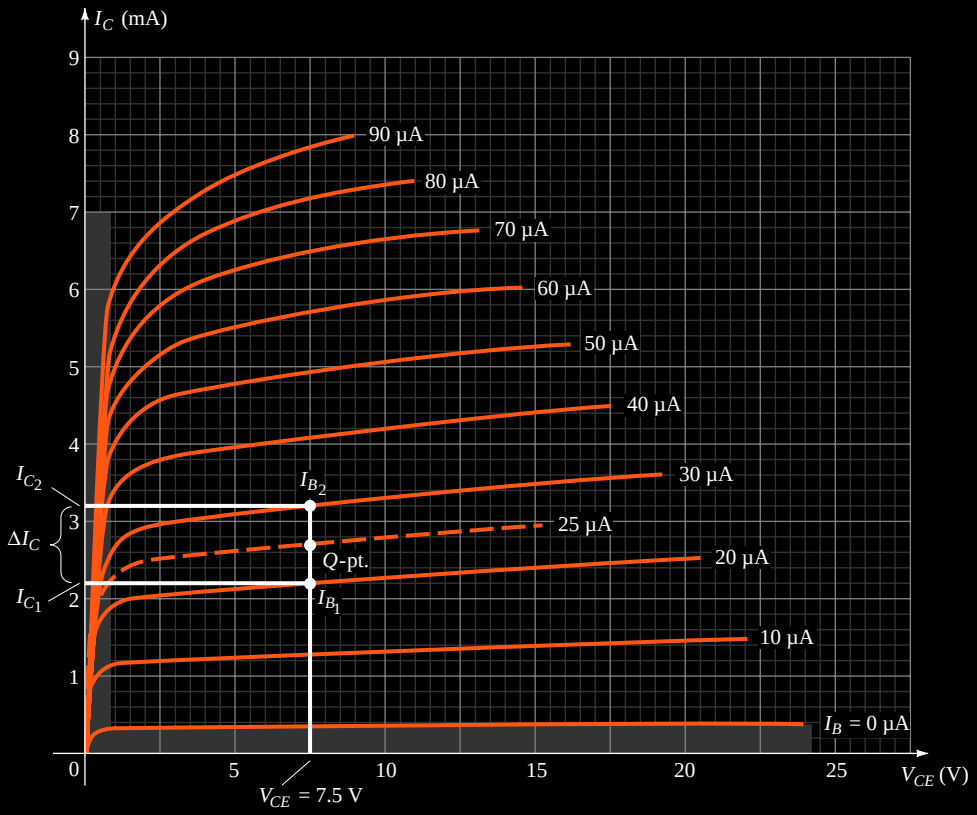


Figure 3.17 Determining β_{ac} and β_{dc} from the collector characteristics.

in I_B (ΔI_B) as appearing in Eq. (3.11) is then defined by choosing two points on either side of the *Q*-point along the vertical axis of about equal distances to either side of the *Q*-point. For this situation the $I_B = 20\ \mu A$ and $30\ \mu A$ curves meet the requirement without extending too far from the *Q*-point. They also define levels of I_B that are easily defined rather than have to interpolate the level of I_B between the curves. It should be mentioned that the best determination is usually made by keeping the chosen ΔI_B as small as possible. At the two intersections of I_B and the vertical axis, the two levels of I_C can be determined by drawing a horizontal line over to the vertical axis and reading the resulting values of I_C. The resulting β_{ac} for the region can then be determined by

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}}$$

$$= \frac{3.2\ \text{mA} - 2.2\ \text{mA}}{30\ \mu A - 20\ \mu A} = \frac{1\ \text{mA}}{10\ \mu A}$$

$$= \mathbf{100}$$

The solution above reveals that for an ac input at the base, the collector current will be about 100 times the magnitude of the base current.

If we determine the dc beta at the *Q*-point:

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{2.7\ \text{mA}}{25\ \mu A} = \mathbf{108}$$

Although not exactly equal, the levels of β_{ac} and β_{dc} are usually reasonably close and are often used interchangeably. That is, if β_{ac} is known, it is assumed to be about the same magnitude as β_{dc}, and vice versa. Keep in mind that in the same lot, the value of β_{ac} will vary somewhat from one transistor to the next even though each transistor has the same number code. The variation may not be significant but for the majority of applications, it is certainly sufficient to validate the approximate approach above. Generally, the smaller the level of I_{CEO}, the closer the magnitude of the two betas. Since the trend is toward lower and lower levels of I_{CEO}, the validity of the foregoing approximation is further substantiated.

If the characteristics had the appearance of those appearing in Fig. 3.18, the level of β_{ac} would be the same in every region of the characteristics. Note that the step in I_B is fixed at 10 μA and the vertical spacing between curves is the same at every point in the characteristics—namely, 2 mA. Calculating the β_{ac} at the Q-point indicated will result in

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} = \frac{9\ \text{mA} - 7\ \text{mA}}{45\ \mu\text{A} - 35\ \mu\text{A}} = \frac{2\ \text{mA}}{10\ \mu\text{A}} = \mathbf{200}$$

Determining the dc beta at the same Q-point will result in

$$\beta_{dc} = \frac{I_C}{I_B} = \frac{8\ \text{mA}}{40\ \mu\text{A}} = \mathbf{200}$$

revealing that if the characteristics have the appearance of Fig. 3.18, the magnitude of β_{ac} and β_{dc} *will be the same* at every point on the characteristics. In particular, note that $I_{CEO} = 0\ \mu$A.

Although a true set of transistor characteristics will never have the exact appearance of Fig. 3.18, it does provide a set of characteristics for comparison with those obtained from a curve tracer (to be described shortly).

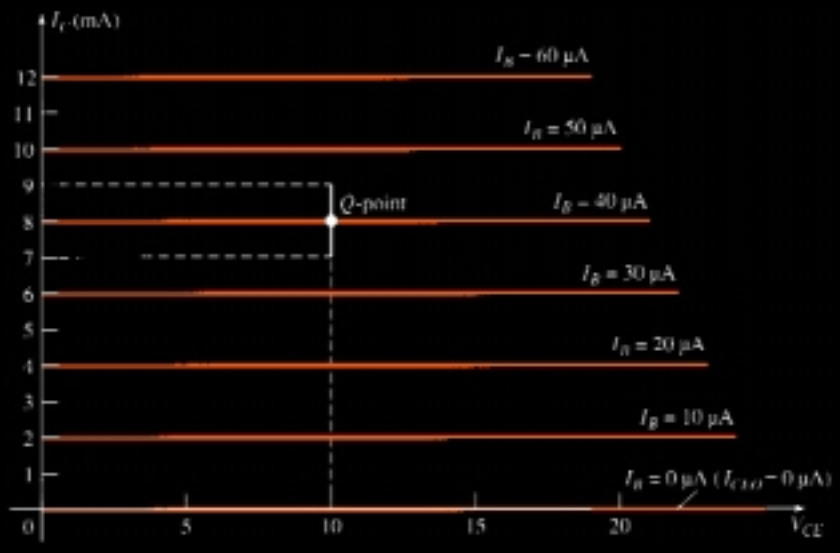


Figure 3.18 Characteristics in which β_{ac} is the same everywhere and $\beta_{ac} = \beta_{dc}$.

For the analysis to follow the subscript dc or ac will not be included with β to avoid cluttering the expressions with unnecessary labels. For dc situations it will simply be recognized as β_{dc} and for any ac analysis as β_{ac}. If a value of β is specified for a particular transistor configuration, it will normally be used for both the dc and ac calculations.

β

A relationship can be developed between β and α using the basic relationships introduced thus far. Using $\beta = I_C/I_B$ we have $I_B = I_C/\beta$, and from $\alpha = I_C/I_E$ we have $I_E = I_C/\alpha$. Substituting into

$$I_E = I_C + I_B$$

we have

$$\frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

and dividing both sides of the equation by I_C will result in

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

or

$$\beta = \alpha\beta + \alpha = (\beta + 1)\alpha$$

so that

$$\boxed{\alpha = \frac{\beta}{\beta + 1}} \tag{3.12a}$$

or

$$\boxed{\beta = \frac{\alpha}{1-\alpha}} \tag{3.12b}$$

In addition, recall that

$$I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$$

but using an equivalence of

$$\frac{1}{1 - \alpha} = \beta + 1$$

derived from the above, we find that

$$I_{CEO} = (\beta + 1)I_{CBO}$$

or

$$\boxed{I_{CEO} \cong \beta I_{CBO}} \tag{3.13}$$

as indicated on Fig. 3.14a. Beta is a particularly important parameter because it provides a direct link between current levels of the input and output circuits for a common-emitter configuration. That is,

$$\boxed{I_C = \beta I_B} \tag{31.4}$$

and since

$$I_E = I_C + I_B$$
$$= \beta I_B + I_B$$

we have

$$\boxed{I_E = (\beta + 1)I_B} \tag{3.15}$$

Both of the equations above play a major role in the analysis in Chapter 4.

Biasing

The proper biasing of a common-emitter amplifier can be determined in a manner similar to that introduced for the common-base configuration. Let us assume that we are presented with an *npn* transistor such as shown in Fig. 3.19a and asked to apply the proper biasing to place the device in the active region.

The first step is to indicate the direction of I_E as established by the arrow in the transistor symbol as shown in Fig. 3.19b. Next, the other currents are introduced as

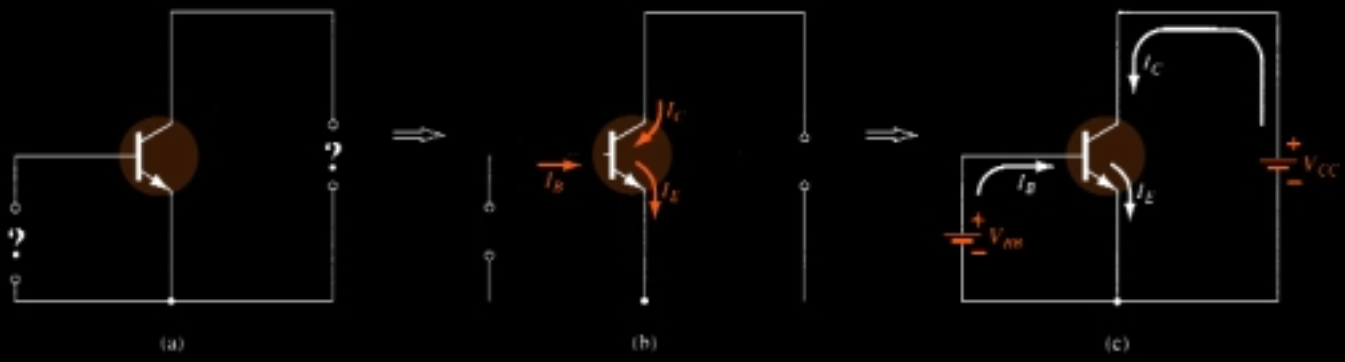


Figure 3.19 Determining the proper biasing arrangement for a common-emitter *npn* transistor configuration.

shown, keeping in mind the Kirchhoff's current law relationship: $I_C + I_B = I_E$. Finally, the supplies are introduced with polarities that will support the resulting directions of I_B and I_C as shown in Fig. 3.19c to complete the picture. The same approach can be applied to *pnp* transistors. If the transistor of Fig. 3.19 was a *pnp* transistor, all the currents and polarities of Fig. 3.19c would be reversed.

3.7 COMMON-COLLECTOR CONFIGURATION

The third and final transistor configuration is the *common-collector configuration*, shown in Fig. 3.20 with the proper current directions and voltage notation. The common-collector configuration is used primarily for impedance-matching purposes since it has a high input impedance and low output impedance, opposite to that of the common-base and common-emitter configurations.

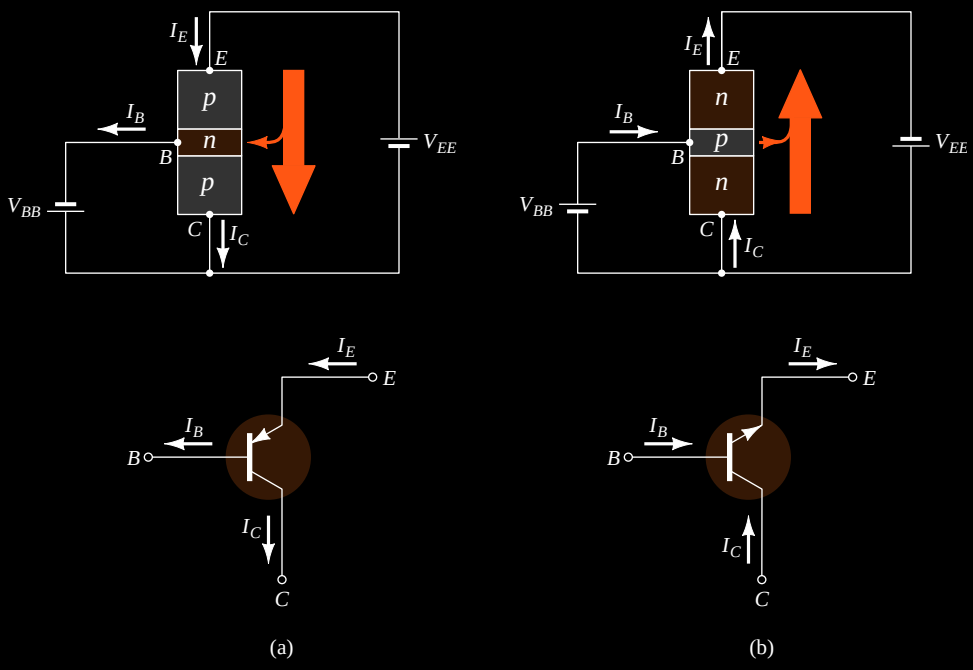


Figure 3.20 Notation and symbols used with the common-collector configuration: (a) *pnp* transistor; (b) *npn* transistor.

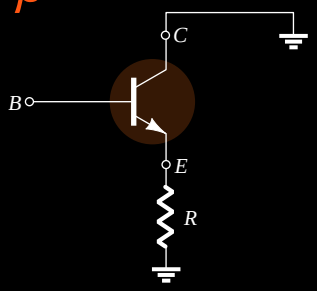


Figure 3.21 Common-collector configuration used for impedance-matching purposes.

A common-collector circuit configuration is provided in Fig. 3.21 with the load resistor connected from emitter to ground. Note that the collector is tied to ground even though the transistor is connected in a manner similar to the common-emitter configuration. From a design viewpoint, there is no need for a set of common-collector characteristics to choose the parameters of the circuit of Fig. 3.21. It can be designed using the common-emitter characteristics of Section 3.6. For all practical purposes, the output characteristics of the common-collector configuration are the same as for the common-emitter configuration. For the common-collector configuration the output characteristics are a plot of I_E versus V_{EC} for a range of values of I_B. The input current, therefore, is the same for both the common-emitter and common-collector characteristics. The horizontal voltage axis for the common-collector configuration is obtained by simply changing the sign of the collector-to-emitter voltage of the common-emitter characteristics. Finally, there is an almost unnoticeable change in the vertical scale of I_C of the common-emitter characteristics if I_C is replaced by I_E for the common-collector characteristics (since $\alpha \cong 1$). For the input circuit of the common-collector configuration the common-emitter base characteristics are sufficient for obtaining the required information.

3.8 LIMITS OF OPERATION

For each transistor there is a region of operation on the characteristics which will ensure that the maximum ratings are not being exceeded and the output signal exhibits minimum distortion. Such a region has been defined for the transistor characteristics of Fig. 3.22. All of the limits of operation are defined on a typical transistor specification sheet described in Section 3.9.

Some of the limits of operation are self-explanatory, such as maximum collector current (normally referred to on the specification sheet as *continuous* collector current) and maximum collector-to-emitter voltage (often abbreviated as V_{CEO} or $V_{(BR)CEO}$ on the specification sheet). For the transistor of Fig. 3.22, $I_{C_{max}}$ was specified as 50 mA and V_{CEO} as 20 V. The vertical line on the characteristics defined as $V_{CE_{sat}}$ specifies

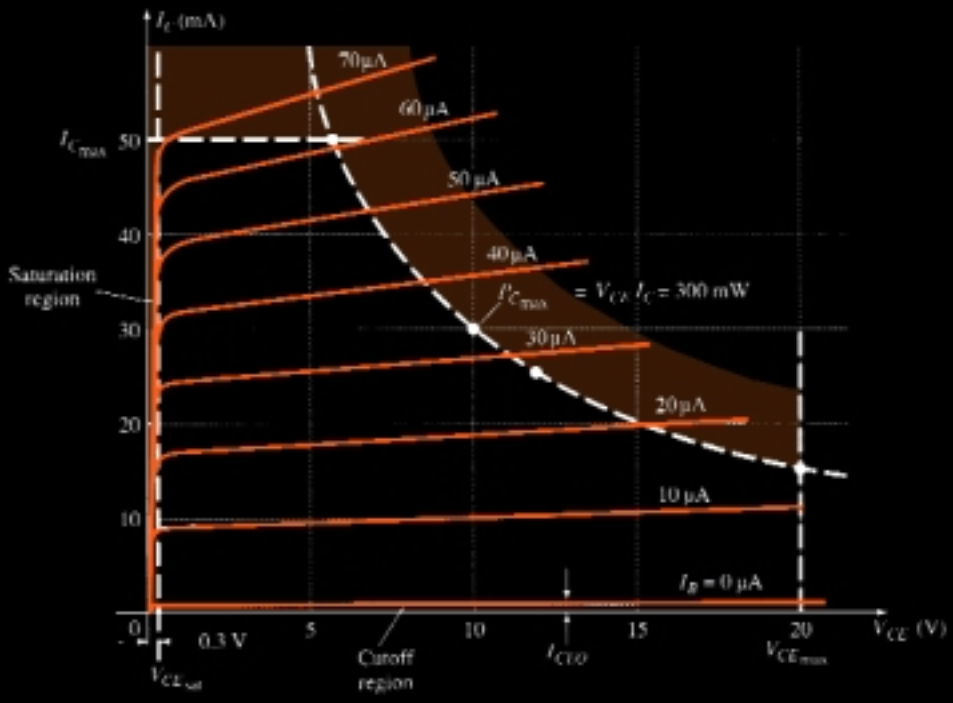


Figure 3.22 Defining the linear (undistorted) region of operation for a transistor.

the minimum V_{CE} that can be applied without falling into the nonlinear region labeled the *saturation* region. The level of $V_{CE_{sat}}$ is typically in the neighborhood of the 0.3 V specified for this transistor.

The maximum dissipation level is defined by the following equation:

$$P_{C_{max}} = V_{CE}I_C \tag{3.16}$$

For the device of Fig. 3.22, the collector power dissipation was specified as 300 mW. The question then arises of how to plot the collector power dissipation curve specified by the fact that

$$P_{C_{max}} = V_{CE}I_C = 300 \text{ mW}$$

or

$$V_{CE}I_C = 300 \text{ mW}$$

At any point on the characteristics the product of V_{CE} and I_C must be equal to 300 mW. If we choose I_C to be the maximum value of 50 mA and substitute into the relationship above, we obtain

$$V_{CE}I_C = 300 \text{ mW}$$

$$V_{CE}(50 \text{ mA}) = 300 \text{ mW}$$

$$V_{CE} = \frac{300 \text{ mW}}{50 \text{ mA}} = \mathbf{6\ V}$$

As a result we find that if $I_C = 50$ mA, then $V_{CE} = 6$ V on the power dissipation curve as indicated in Fig. 3.22. If we now choose V_{CE} to be its maximum value of 20 V, the level of I_C is the following:

$$(20 \text{ V})I_C = 300 \text{ mW}$$

$$I_C = \frac{300 \text{ mW}}{20 \text{ V}} = \mathbf{15\ mA}$$

defining a second point on the power curve.

If we now choose a level of I_C in the midrange such as 25 mA, and solve for the resulting level of V_{CE}, we obtain

$$V_{CE}(25 \text{ mA}) = 300 \text{ mW}$$

and

$$V_{CE} = \frac{300 \text{ mW}}{25 \text{ mA}} = \mathbf{12\ V}$$

as also indicated on Fig. 3.22.

A rough estimate of the actual curve can usually be drawn using the three points defined above. Of course, the more points you have, the more accurate the curve, but a rough estimate is normally all that is required.

The *cutoff* region is defined as that region below $I_C = I_{CEO}$. This region must also be avoided if the output signal is to have minimum distortion. On some specification sheets only I_{CBO} is provided. One must then use the equation $I_{CEO} = \beta I_{CBO}$ to establish some idea of the cutoff level if the characteristic curves are unavailable. Operation in the resulting region of Fig. 3.22 will ensure minimum distortion of the output signal and current and voltage levels that will not damage the device.

If the characteristic curves are unavailable or do not appear on the specification sheet (as is often the case), one must simply be sure that I_C, V_{CE}, and their product $V_{CE}I_C$ fall into the range appearing in Eq. (3.17).

β

$$I_{CEO} \leqq \boldsymbol{I_C} \leqq I_{C_{max}}$$
$$V_{CE_{sat}} \leqq \boldsymbol{V_{CE}} \leqq V_{CE_{max}} \tag{3.17}$$
$$\boldsymbol{V_{CE}I_C} \leqq P_{C_{max}}$$

For the common-base characteristics the maximum power curve is defined by the following product of output quantities:

$$P_{C_{max}} = V_{CB}I_C \tag{3.18}$$

3.9 TRANSISTOR SPECIFICATION SHEET

Since the specification sheet is the communication link between the manufacturer and user, it is particularly important that the information provided be recognized and correctly understood. Although all the parameters have not been introduced, a broad number will now be familiar. The remaining parameters will be introduced in the chapters that follow. Reference will then be made to this specification sheet to review the manner in which the parameter is presented.

The information provided as Fig. 3.23 is taken directly from the *Small-Signal Transistors, FETs, and Diodes* publication prepared by Motorola Inc. The 2N4123 is a general-purpose *npn* transistor with the casing and terminal identification appearing in the top-right corner of Fig. 3.23a. Most specification sheets are broken down into *maximum ratings, thermal characteristics, and electrical characteristics.* The electrical characteristics are further broken down into "on," "off," and small-signal characteristics. The "on" and "off" characteristics refer to dc limits, while the small-signal characteristics include the parameters of importance to ac operation.

Note in the maximum rating list that $V_{CE_{max}} = V_{CEO} = 30$ V with $I_{C_{max}} = 200$ mA. The maximum collector dissipation $P_{C_{max}} = P_D = 625$ mW. The derating factor under the maximum rating specifies that the maximum rating must be decreased 5 mW for every 1° rise in temperature above 25°C. In the "off" characteristics I_{CBO} is specified as 50 nA and in the "on" characteristics $V_{CE_{sat}} = 0.3$ V. The level of h_{FE} has a range of 50 to 150 at $I_C = 2$ mA and $V_{CE} = 1$ V and a minimum value of 25 at a higher current of 50 mA at the same voltage.

The limits of operation have now been defined for the device and are repeated below in the format of Eq. (3.17) using $h_{FE} = 150$ (the upper limit) and $I_{CEO} \cong \beta I_{CBO} = (150)(50\text{ nA}) = 7.5\ \mu$A. Certainly, for many applications the 7.5 μA = 0.0075 mA can be considered to be 0 mA on an approximate basis.

Limits of Operation

$$7.5\ m\text{A} \leqq \boldsymbol{I_C} \leqq 200\text{ mA}$$
$$0.3\text{ V} \leqq \boldsymbol{V_{CE}} \leqq 30\text{ V}$$
$$\boldsymbol{V_{CE}I_C} \leqq 650\text{ mW}$$

In the small-signal characteristics the level of h_{fe} (β_{ac}) is provided along with a plot of how it varies with collector current in Fig. 3.23f. In Fig. 3.23j the effect of temperature and collector current on the level of h_{FE} (β_{ac}) is demonstrated. At room temperature (25°C), note that h_{FE} (β_{dc}) is a maximum value of 1 in the neighborhood of about 8 mA. As I_C increased beyond this level, h_{FE} drops off to one-half the value with I_C equal to 50 mA. It also drops to this level if I_C decreases to the low level of 0.15 mA. Since this is a *normalized* curve, if we have a transistor with $\beta_{dc} = h_{FE} = 50$ at room temperature, the maximum value at 8 mA is 50. At $I_C = 50$ mA it has dropped to 50/2 = 25. In other words, normalizing reveals that the actual level of h_{FE}

at any level of I_C has been divided by the maximum value of h_{FE} at that temperature and $I_C = 8$ mA. Note also that the horizontal scale of Fig. 3.23j is a log scale. Log scales are examined in depth in Chapter 11. You may want to look back at the plots of this section when you find time to review the first few sections of Chapter 11.

MAXIMUM RATINGS

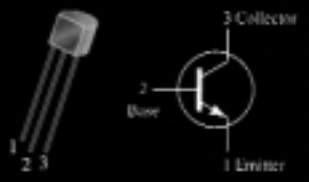
Rating	Symbol	2N4123	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5.0	mW mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

2N4123

CASE 29-04, STYLE 1
TO-92 (TO-226AA)



GENERAL PURPOSE TRANSISTOR
NPN SILICON

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0$ mAdc, $I_B = 0$)	$V_{(BR)CEO}$	30		Vdc
Collector-Base Breakdown Voltage ($I_C = 10$ µAdc, $I_E = 0$)	$V_{(BR)CBO}$	40		Vdc
Emitter-Base Breakdown Voltage ($I_E = 10$ µAdc, $I_C = 0$)	$V_{(BR)EBO}$	5.0		Vdc
Collector Cutoff Current ($V_{CB} = 20$ Vdc, $I_E = 0$)	I_{CBO}	–	50	nAdc
Emitter Cutoff Current ($V_{EB} = 3.0$ Vdc, $I_C = 0$)	I_{EBO}	–	50	nAdc
ON CHARACTERISTICS				
DC Current Gain(1) ($I_C = 2.0$ mAdc, $V_{CE} = 1.0$ Vdc) ($I_C = 50$ mAdc, $V_{CE} = 1.0$ Vdc)	h_{FE}	50 25	150 –	–
Collector-Emitter Saturation Voltage(1) ($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)	$V_{CE(sat)}$	–	0.3	Vdc
Base-Emitter Saturation Voltage(1) ($I_C = 50$ mAdc, $I_B = 5.0$ mAdc)	$V_{BE(sat)}$		0.95	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Current-Gain – Bandwidth Product ($I_C = 10$ mAdc, $V_{CE} = 20$ Vdc, $f = 100$ MHz)	f_T	250		MHz
Output Capacitance ($V_{CB} = 5.0$ Vdc, $I_E = 0$, $f = 100$ MHz)	C_{obo}		4.0	pF
Input Capacitance ($V_{EB} = 0.5$ Vdc, $I_C = 0$, $f = 100$ kHz)	C_{ibo}		8.0	pF
Collector Base Capacitance ($I_E = 0$, $V_{CB} = 5.0$ V, $f = 100$ kHz)	C_{cb}	–	4.0	pF
Small-Signal Current Gain ($I_C = 2.0$ mAdc, $V_{CE} = 10$ Vdc, $f = 1.0$ kHz)	h_{fe}	50	200	–
Current Gain – High Frequency ($I_C = 10$ mAdc, $V_{CE} = 20$ Vdc, $f = 100$ MHz) ($I_C = 2.0$ mAdc, $V_{CE} = 10$ V, $f = 1.0$ kHz)	h_{fe}	2.5 50	– 200	–
Noise Figure ($I_C = 100$ µAdc, $V_{CE} = 5.0$ Vdc, $R_S = 1.0$ k ohm, $f = 1.0$ kHz)	NF		6.0	dB

(1) Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2.0%

(a)

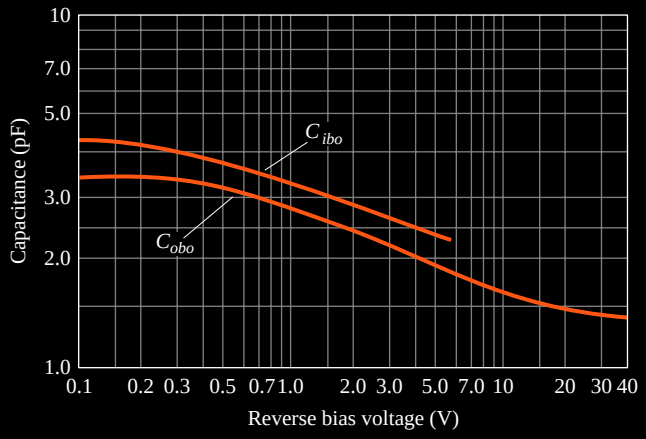
Figure 3.23 Transistor specification sheet.

β

Before leaving this description of the characteristics, take note of the fact that the actual collector characteristics are not provided. In fact, most specification sheets as provided by the range of manufacturers fail to provide the full characteristics. It is expected that the data provided are sufficient to use the device effectively in the design process.

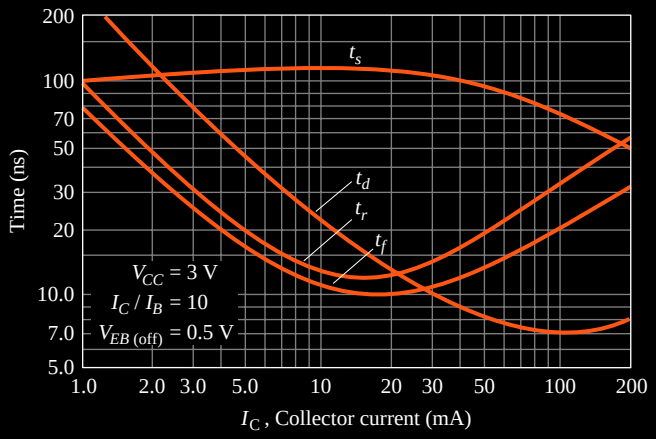
As noted in the introduction to this section, all the parameters of the specification sheet have not been defined in the preceding sections or chapters. However, the specification sheet provided in Fig. 3.23 will be referenced continually in the chapters to follow as parameters are introduced. The specification sheet can be a very valuable tool in the design or analysis mode, and every effort should be made to be aware of the importance of each parameter and how it may vary with changing levels of current, temperature, and so on.

Figure 1 – Capacitance



(b)

Figure 2 – Switching Times



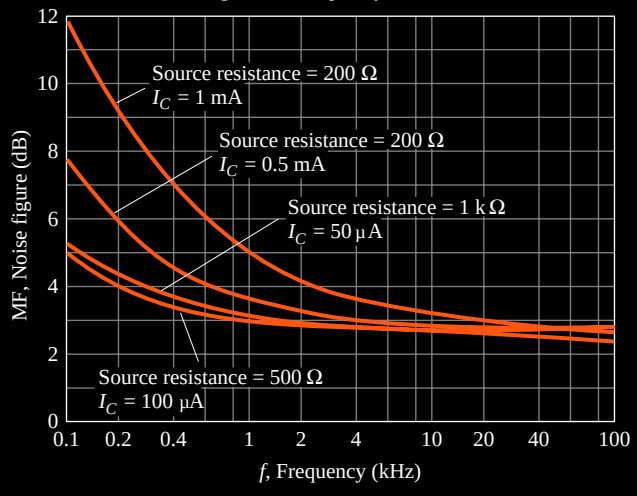
(c)

AUDIO SMALL SIGNAL CHARACTERISTICS

NOISE FIGURE

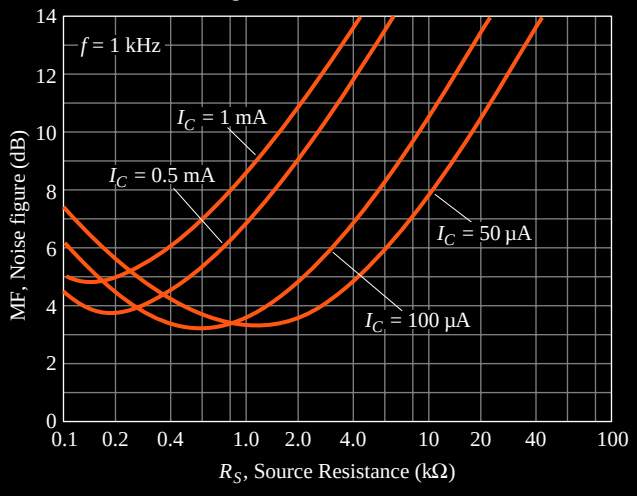
(V_{CE} = 5 Vdc, T_A = 25°C)
Bandwidth = 1.0 Hz

Figure 3 – Frequency Variations



(d)

Figure 4 – Source Resistance



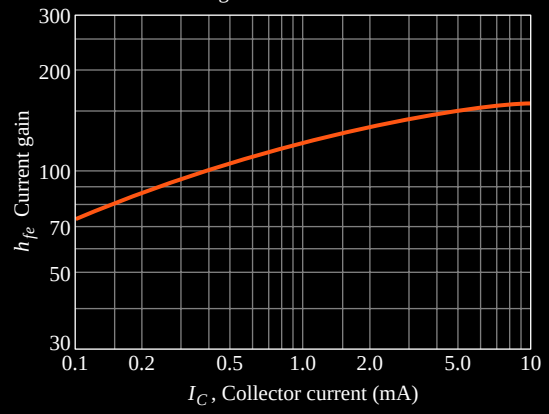
(e)

Figure 3.23 Continued.

_h_ PARAMETERS

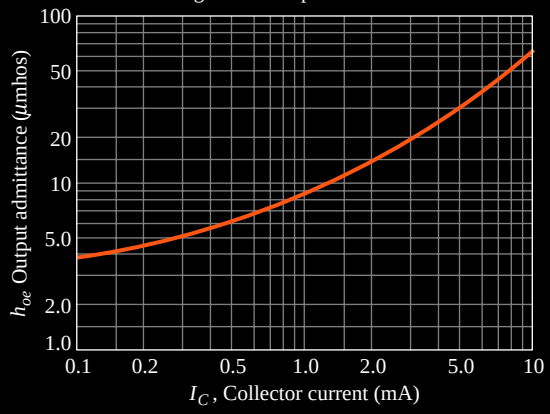
V_{CE} = 10 V, f = 1 kHz, T_A = 25°C

Figure 5 – Current Gain



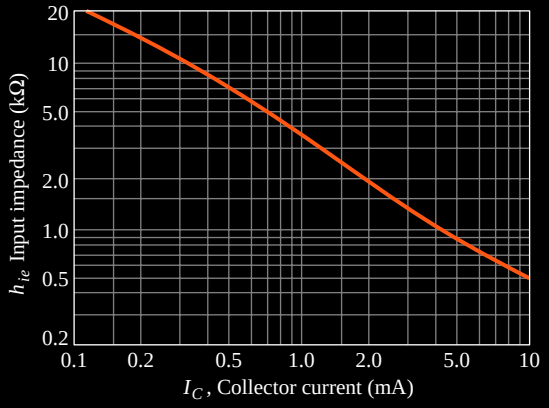
(f)

Figure 6 – Output Admittance



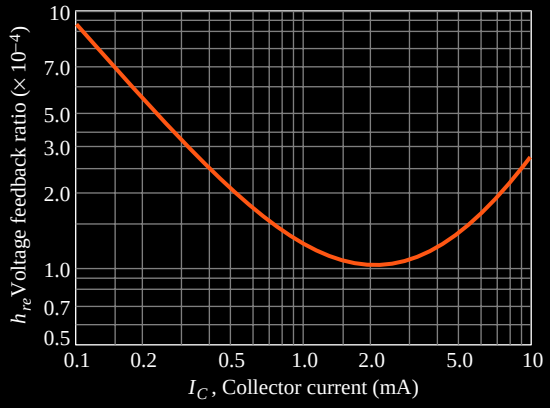
(g)

Figure 7 – Input Impedance



(h)

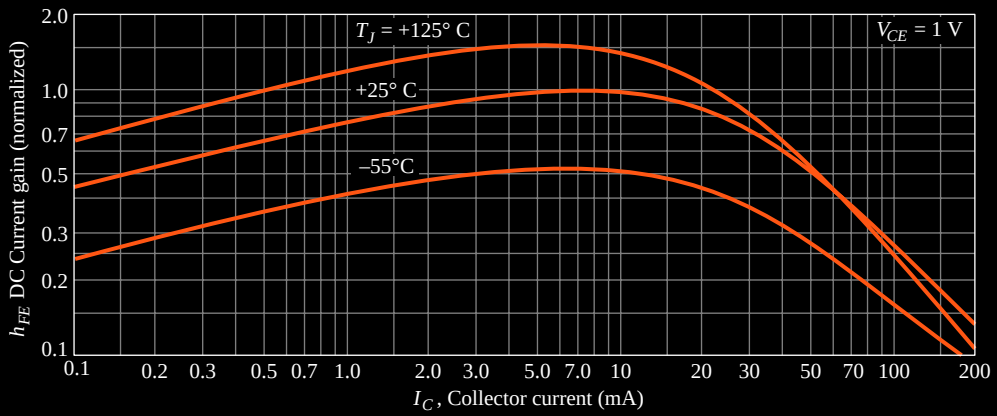
Figure 8 – Voltage Feedback Ratio



(i)

STATIC CHARACTERISTICS

Figure 9 – DC Current Gain



(j)

Figure 3.23 Continued.

3.10 TRANSISTOR TESTING

As with diodes, there are three routes one can take to check a transistor: *curve tracer, digital meter,* and *ohmmeter.*

Curve Tracer

The curve tracer of Fig. 1.45 will provide the display of Fig. 3.24 once all the controls have been properly set. The smaller displays to the right reveal the scaling to be applied to the characteristics. The vertical sensitivity is 2 mA/div, resulting in the scale shown to the left of the monitor's display. The horizontal sensitivity is 1 V/div, resulting in the scale shown below the characteristics. The step function reveals that the curves are separated by a difference of 10 μA, starting at 0 μA for the bottom curve. The last scale factor provided can be used to quickly determine the β_{ac} for any region of the characteristics. Simply multiply the displayed factor by the number of divisions between I_B curves in the region of interest. For instance, let us determine β_{ac} at a Q-point of $I_C = 7$ mA and $V_{CE} = 5$ V. In this region of the display, the distance between I_B curves is $\frac{9}{10}$ of a division, as indicated on Fig. 3.25. Using the factor specified, we find that

$$\beta_{ac} = \frac{9}{10}\ \text{div}\left(\frac{200}{\text{div}}\right) = \mathbf{180}$$

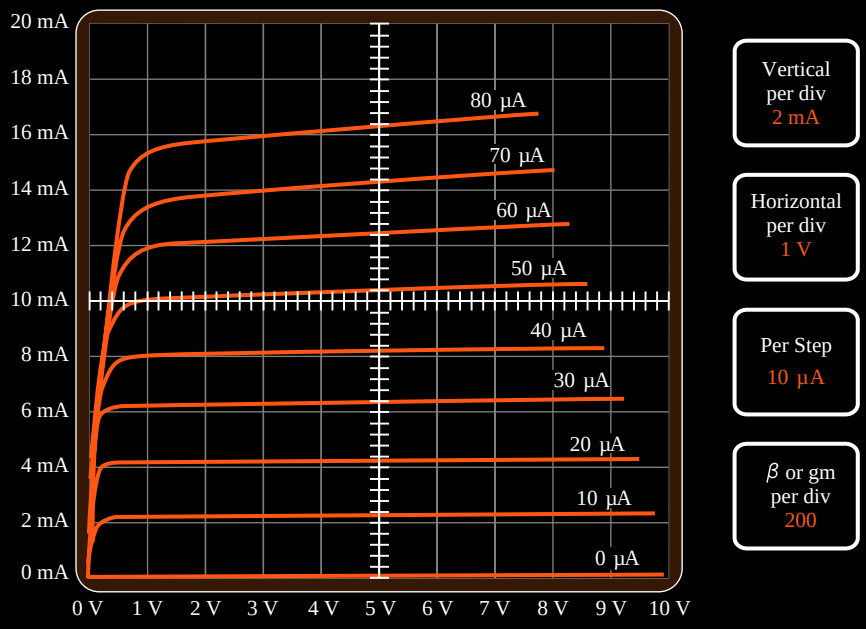


Figure 3.24 Curve tracer response to 2N3904 *npn* transistor.

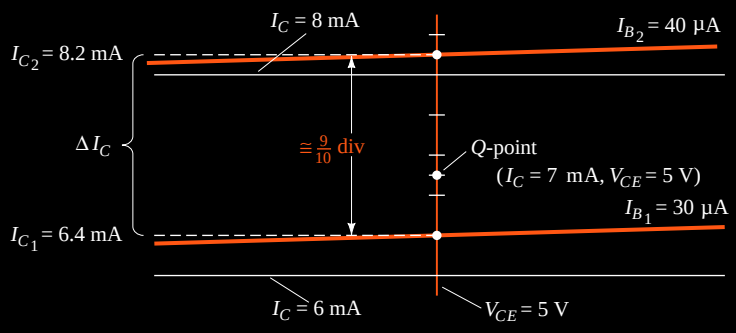


Figure 3.25 Determining β_{ac} for the transistor characteristics of Fig. 3.24 at $I_C = 7$ mA and $V_{CE} = 5$ V.

Using Eq. (3.11) gives us

$$\beta_{ac} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE}\ =\ \text{constant}} = \frac{I_{C_2} - I_{C_1}}{I_{B_2} - I_{B_1}} = \frac{8.2\ \text{mA} - 6.4\ \text{mA}}{40\ \mu\text{A} - 30\ \mu\text{A}}$$

$$= \frac{1.8\ \text{mA}}{10\ \mu\text{A}} = \mathbf{180}$$

verifying the determination above.

Advanced Digital Meters

Advanced digital meters such as that shown in Fig. 3.26 are now available that can provide the level of h_{FE} using the lead sockets appearing at the bottom left of the dial. Note the choice of *pnp* or *npn* and the availability of two emitter connections to handle the sequence of leads as connected to the casing. The level of h_{FE} is determined at a collector current of 2 mA for the Testmate 175A, which is also provided on the digital display. Note that this versatile instrument can also check a diode. It can measure capacitance and frequency in addition to the normal functions of voltage, current, and resistance measurements.

In fact, in the diode testing mode it can be used to check the *p-n* junctions of a transistor. With the collector open the base-to-emitter junction should result in a low voltage of about 0.7 V with the red (positive) lead connected to the base and the black (negative) lead connected to the emitter. A reversal of the leads should result in an OL indication to represent the reverse-biased junction. Similarly, with the emitter open, the forward- and reverse-bias states of the base-to-collector junction can be checked.

Figure 3.26 Transistor tester. (Courtesy Computronics Technology, Inc.)

Ohmmeter

An ohmmeter or the resistance scales of a DMM can be used to check the state of a transistor. Recall that for a transistor in the active region the base-to-emitter junction is forward-biased and the base-to-collector junction is reverse-biased. Essentially, therefore, the forward-biased junction should register a relatively low resistance while the reverse-biased junction shows a much higher resistance. For an *npn* transistor, the forward-biased junction (biased by the internal supply in the resistance mode) from base to emitter should be checked as shown in Fig. 3.27 and result in a reading that will typically fall in the range of 100 Ω to a few kilohms. The reverse-biased base-to-collector junction (again reverse-biased by the internal supply) should be checked as shown in Fig. 3.28 with a reading typically exceeding 100 kΩ. For a *pnp* transistor the leads are reversed for each junction. Obviously, a large or small resistance in both directions (reversing the leads) for either junction of an *npn* or *pnp* transistor indicates a faulty device.

If both junctions of a transistor result in the expected readings the type of transistor can also be determined by simply noting the polarity of the leads as applied to the base-emitter junction. If the positive (+) lead is connected to the base and the negative lead (−) to the emitter a low resistance reading would indicate an *npn* transistor. A high resistance reading would indicate a *pnp* transistor. Although an ohmmeter can also be used to determine the leads (base, collector and emitter) of a transistor it is assumed that this determination can be made by simply looking at the orientation of the leads on the casing.

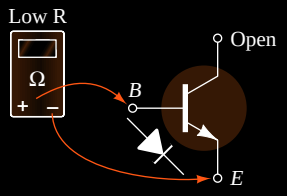


Figure 3.27 Checking the forward-biased base-to-emitter junction of an *npn* transistor.

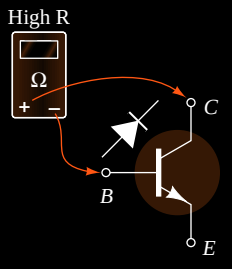


Figure 3.28 Checking the reverse-biased base-to-collector junction of an *npn* transistor.

β

3.11 TRANSISTOR CASING AND TERMINAL IDENTIFICATION

After the transistor has been manufactured using one of the techniques described in Chapter 12, leads of, typically, gold, aluminum, or nickel are then attached and the entire structure is encapsulated in a container such as that shown in Fig. 3.29. Those with the heavy duty construction are high-power devices, while those with the small can (top hat) or plastic body are low- to medium-power devices.

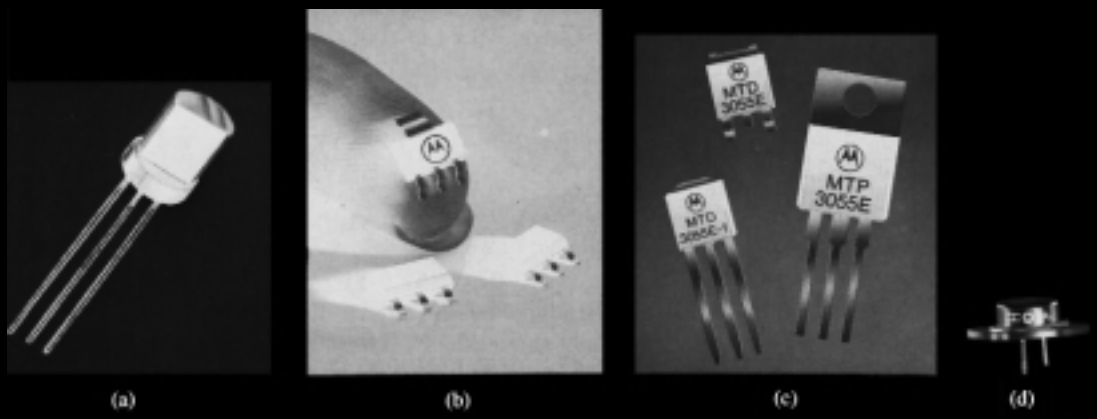


Figure 3.29 Various types of transistors: (a) Courtesy General Electric Company; (b) and (c) Courtesy of Motorola Inc.; (d) Courtesy International Rectifier Corporation.

Whenever possible, the transistor casing will have some marking to indicate which leads are connected to the emitter, collector, or base of a transistor. A few of the methods commonly used are indicated in Fig. 3.30.

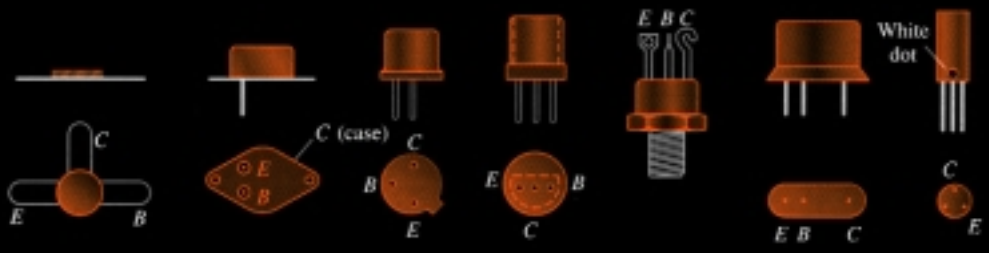


Figure 3.30 Transistor terminal identification.

The internal construction of a TO-92 package in the Fairchild line appears in Fig. 3.31. Note the very small size of the actual semiconductor device. There are gold bond wires, a copper frame, and an epoxy encapsulation.

Four (quad) individual *pnp* silicon transistors can be housed in the 14-pin plastic dual-in-line package appearing in Fig. 3.32a. The internal pin connections appear in Fig. 3.32b. As with the diode IC package, the indentation in the top surface reveals the number 1 and 14 pins.

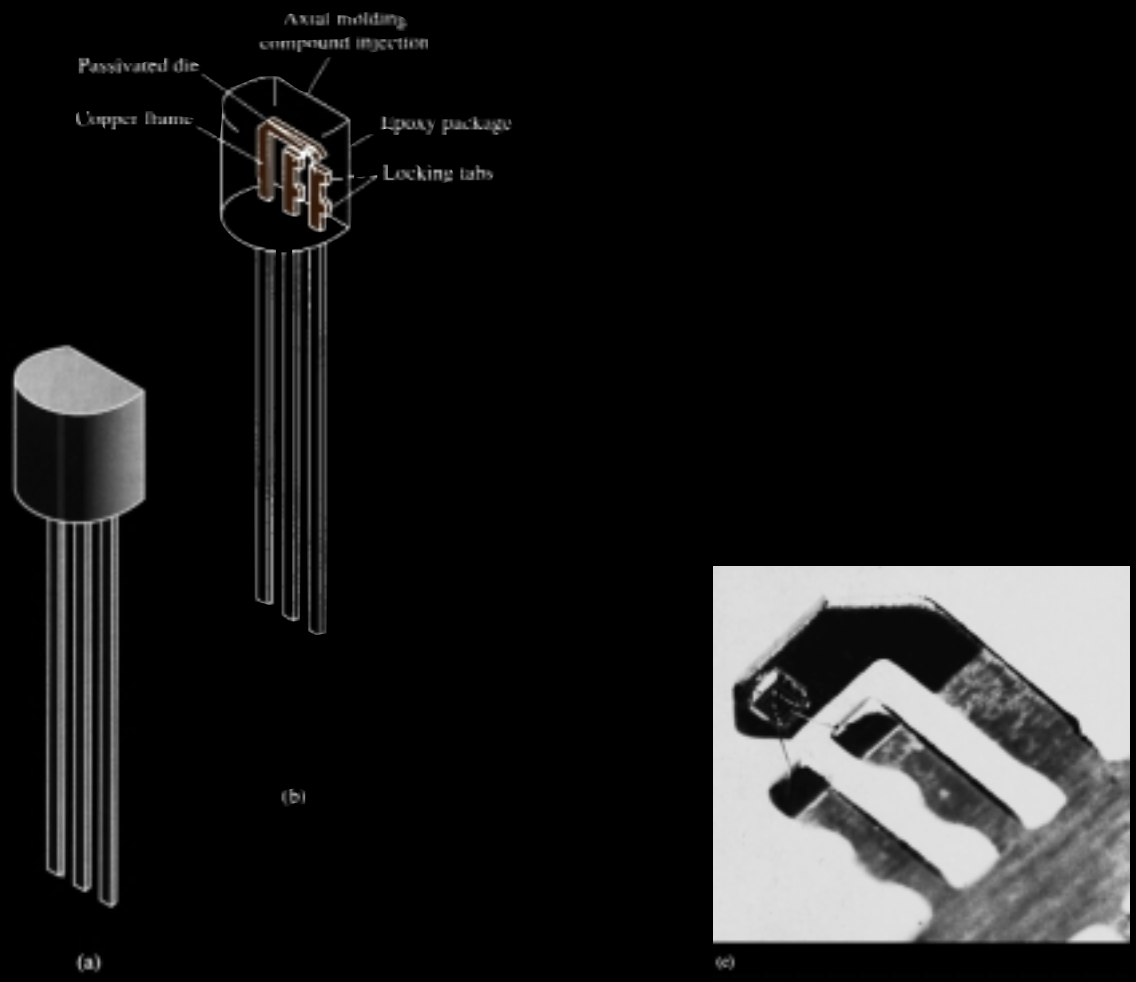


Figure 3.31 Internal construction of a Fairchild transistor in a TO-92 package. (Courtesy Fairchild Camera and Instrument Corporation.)

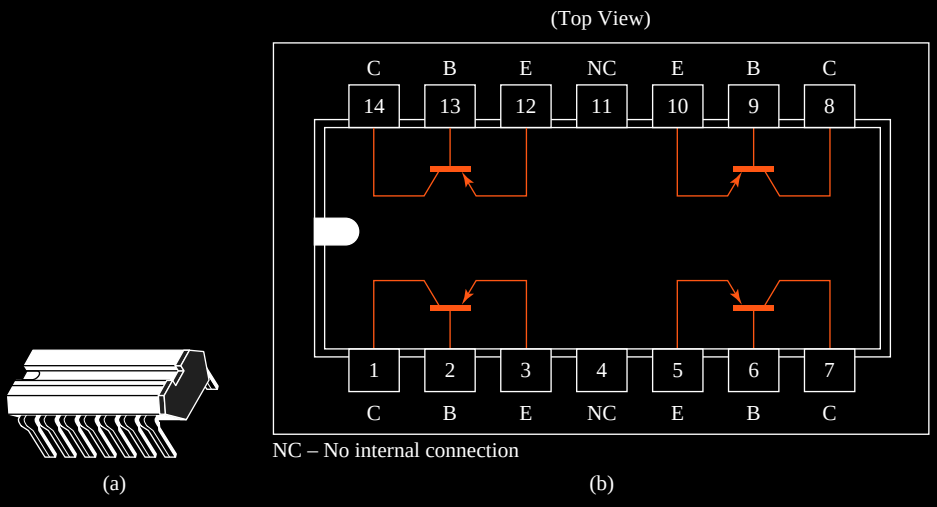


Figure 3.32 Type Q2T2905 Texas Instruments quad *pnp* silicon transistors: (a) appearance; (b) pin connections. (Courtesy Texas Instruments Incorporated.)

3.12 PSPICE WINDOWS

Since the transistor characteristics were introduced in this chapter it seems appropriate that a procedure for obtaining those characteristics using PSpice Windows should be examined. The transistors are listed in the **EVAL.slb** library and start with the letter **Q.** The library includes two *npn* transistors and two *pnp* transistors. The fact that there are a series of curves defined by the levels of I_B will require that a sweep of I_B values (a *nested sweep*) occur within a sweep of collector-to-emitter voltages. This is unnecessary for the diode, however, since only one curve would result.

First, the network in Fig. 3.33 is established using the same procedure defined in Chapter 2. The voltage V_{CC} will establish our main sweep while the voltage V_{BB} will determine the nested sweep. For future reference, note the panel at the top right of the menu bar with the scroll control when building networks. This option allows you to retrieve elements that have been used in the past. For instance, if you placed a resistor a few elements ago, simply return to the scroll bar and scroll until the resistor **R** appears. Click the location once, and the resistor will appear on the screen.

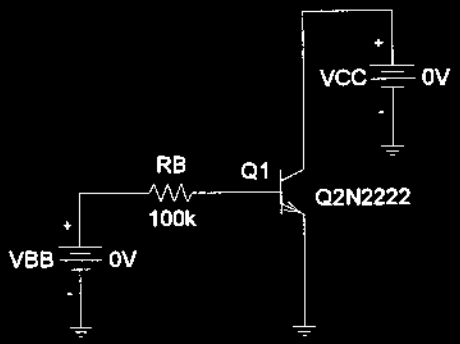


Figure 3.33 Network employed to obtain the collector characteristics of the Q2N2222 transistor.

Next, choose the **Analysis Setup** icon and enable the **DC Sweep.** Click on **DC Sweep,** and choose **Voltage Source** and **Linear.** Type in the **Name** V_{CC} with a **Start Value** of 0 V and an **End Value** of 10 V. Use an **Increment** of 0.01 V to ensure a continuous, detailed plot. Rather than click **OK,** this time we have to choose the **Nested Sweep** at the bottom left of the dialog box. When chosen, a **DC Nested Sweep** dialog box will appear and ask us to repeat the choices just made for the voltage V_{BB}. Again, Voltage Source and Linear are chosen, and the name is inserted as V_{BB}. The **Start Value** will now be 2.7 V to correspond with an initial current of 20 μA as determined by

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{2.7\text{ V} - 0.7\text{ V}}{100\text{ k}\Omega} = \mathbf{20\ \mu A}$$

The Increment will be 2V, corresponding with a change in base current of 20 μA between I_B levels. The final value will be 10.7 V, corresponding with a current of 100 μA. Before leaving the dialog box, be sure to enable the nested sweep. Then, choose **OK,** followed by a closing of the **Analysis Setup,** and we are ready for the analysis. This time we will automatically Run Probe after the analysis by choosing **Analysis-Probe Setup,** followed by selecting **Automatically run Probe after simulation.** After choosing **OK,** followed by a clicking of the **Simulation icon** (recall that it was the

icon with the yellow background and two waveforms), the **OrCAD MicroSim Probe** screen will automatically appear. This time, since V_{CC} is the collector-to-emitter voltage, there is no need to label the voltage at the collector. In fact, since it appears as the horizontal axis of the Probe response, there is no need to touch the **X-Axis Settings** at all if we recognize that V_{CC} is the collector-to-emitter voltage. For the vertical axis, we turn to **Trace-Add** and obtain the **Add Traces** dialog box. Choosing **IC(Q1)** and **OK,** we obtain the transistor characteristics. Unfortunately, however, they extend from −10 to +20 mA on the vertical axis. This can be corrected by choosing **Plot** and then **Y-Axis Settings** to obtain the **Y-Axis Settings** dialog box. By choosing **User Defined,** the range can be set from 0 to 20 mA with a Linear scale. Choose **OK** again, and the characteristics of Fig. 3.34 result.

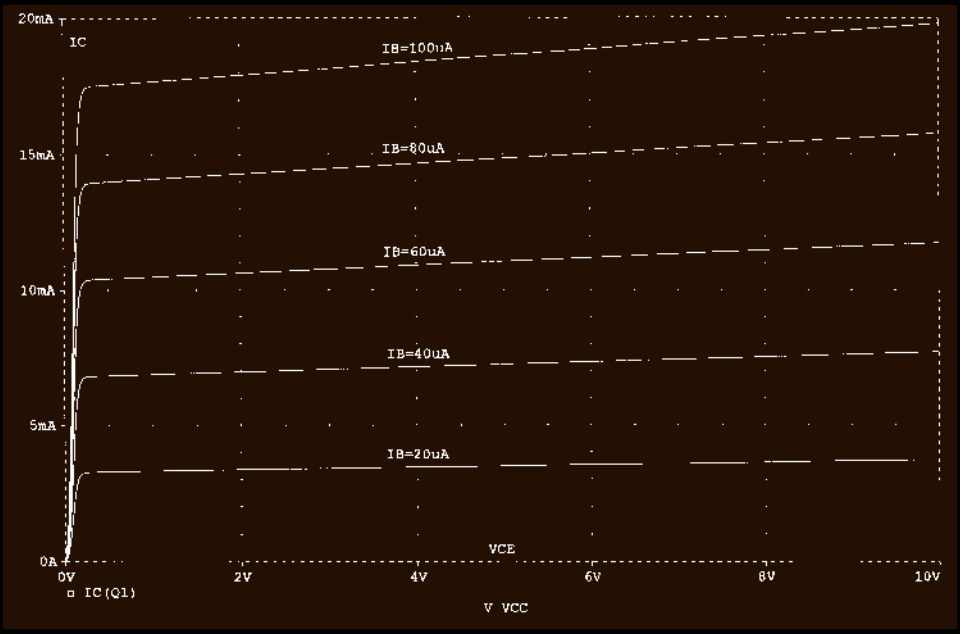


Figure 3.34 Collector characteristics for the transistor of Figure 3.33.

Using the **ABC** icon on the menu bar, the various levels of I_B can be inserted along with the axis labels V_{CE} and I_C. Simply click on the icon, and a dialog box appears asking for the text material. Enter the desired text, click **OK,** and it will appear on the screen. It can then be placed in the desired location.

If the ac beta is determined in the middle of the graph, you will find that its value is about 190—even though **Bf** in the list of specifications is 255.9. Again, like the diode, the other parameters of the element have a noticeable effect on the total operation. However, if we return to the diode specifications through **Edit-Model-Edit Instance Model (Text)** and remove all parameters of the device except Bf = 255.9 (don't forget the close parentheses at the end of the listing) and follow with an **OK** and a **Simulation,** a new set of curves will result. An adjustment of the range of the *y*-axis to 0–30 mA using the **Y-Axis Settings** will result in the characteristic curves of Fig. 3.35.

Note first that the curves are all horizontal, meaning that the element is void of any resistive elements. In addition, the equal spacing of the curves throughout reveals that beta is the same everywhere (as specified by our new device characteristics). Using a difference of 5 mA between any two curves and dividing by the difference in I_B of 20 μA will result in a β of 250, which is essentially the same as that specified for the device.

β

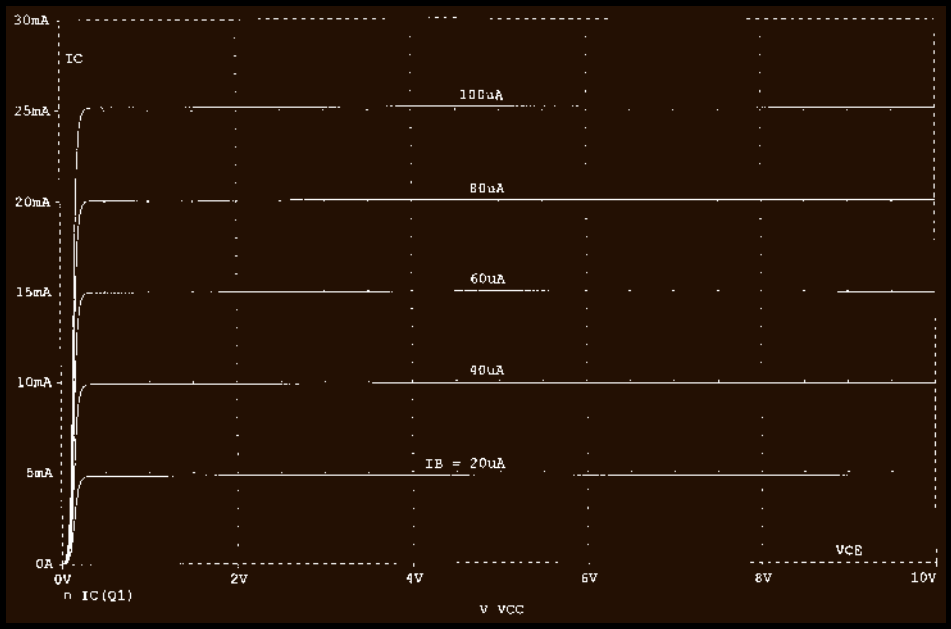


FIGURE 3.35 Ideal collector characteristics for the transistor of Figure 3.33.

PROBLEMS

§ 3.2 Transistor Construction

1. What names are applied to the two types of BJT transistors? Sketch the basic construction of each and label the various minority and majority carriers in each. Draw the graphic symbol next to each. Is any of this information altered by changing from a silicon to a germanium base?
2. What is the major difference between a bipolar and a unipolar device?

§ 3.3 Transistor Operation

3. How must the two transistor junctions be biased for proper transistor amplifier operation?
4. What is the source of the leakage current in a transistor?
5. Sketch a figure similar to Fig. 3.3 for the forward-biased junction of an *npn* transistor. Describe the resulting carrier motion.
6. Sketch a figure similar to Fig. 3.4 for the reverse-biased junction of an *npn* transistor. Describe the resulting carrier motion.
7. Sketch a figure similar to Fig. 3.5 for the majority- and minority-carrier flow of an *npn* transistor. Describe the resulting carrier motion.
8. Which of the transistor currents is always the largest? Which is always the smallest? Which two currents are relatively close in magnitude?
9. If the emitter current of a transistor is 8 mA and I_B is 1/100 of I_C, determine the levels of I_C and I_B.

§ 3.4 Common-Base Configuration

10. From memory, sketch the transistor symbol for a *pnp* and an *npn* transistor, and then insert the conventional flow direction for each current.
11. Using the characteristics of Fig. 3.7, determine V_{BE} at $I_E = 5$ mA for $V_{CB} = 1$, 10, and 20 V. Is it reasonable to assume on an approximate basis that V_{CB} has only a slight effect on the relationship between V_{BE} and I_E?
12. (a) Determine the average ac resistance for the characteristics of Fig. 3.10b.
    (b) For networks in which the magnitude of the resistive elements is typically in kilohms, is the approximation of Fig. 3.10c a valid one [based on the results of part (a)]?

13. (a) Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_E = 4.5$ mA and $V_{CB} = 4$ V.
(b) Repeat part (a) for $I_E = 4.5$ mA and $V_{CB} = 16$ V.
(c) How have the changes in V_{CB} affected the resulting level of I_C?
(d) On an approximate basis, how are I_E and I_C related based on the results above?

14. (a) Using the characteristics of Figs. 3.7 and 3.8, determine I_C if $V_{CB} = 10$ V and $V_{BE} = 800$ mV.
(b) Determine V_{BE} if $I_C = 5$ mA and $V_{CB} = 10$ V.
(c) Repeat part (b) using the characteristics of Fig. 3.10b.
(d) Repeat part (b) using the characteristics of Fig. 3.10c.
(e) Compare the solutions for V_{BE} for parts (b), (c), and (d). Can the difference be ignored if voltage levels greater than a few volts are typically encountered?

15. (a) Given an α_{dc} of 0.998, determine I_C if $I_E = 4$ mA.
(b) Determine α_{dc} if $I_E = 2.8$ mA and $I_B = 20\ \mu$A.
(c) Find I_E if $I_B = 40\ \mu$A and α_{dc} is 0.98.

16. From memory, and memory only, sketch the common-base BJT transistor configuration (for *npn* and *pnp*) and indicate the polarity of the applied bias and resulting current directions.

§ 3.5 Transistor Amplifying Action

17. Calculate the voltage gain ($A_v = V_L/V_i$) for the network of Fig. 3.12 if $V_i = 500$ mV and $R = 1$ kΩ. (The other circuit values remain the same.)

18. Calculate the voltage gain ($A_v = V_L/V_i$) for the network of Fig. 3.12 if the source has an internal resistance of 100 Ω in series with V_i.

§ 3.6 Common-Emitter Configuration

19. Define I_{CBO} and I_{CEO}. How are they different? How are they related? Are they typically close in magnitude?

20. Using the characteristics of Fig. 3.14:
(a) Find the value of I_C corresponding to $V_{BE} = +750$ mV and $V_{CE} = +5$ V.
(b) Find the value of V_{CE} and V_{BE} corresponding to $I_C = 3$ mA and $I_B = 30\ \mu$A.

* **21.** (a) For the common-emitter characteristics of Fig. 3.14, find the dc beta at an operating point of $V_{CE} = +8$ V and $I_C = 2$ mA.
(b) Find the value of α corresponding to this operating point.
(c) At $V_{CE} = +8$ V, find the corresponding value of I_{CEO}.
(d) Calculate the approximate value of I_{CBO} using the dc beta value obtained in part (a).

* **22.** (a) Using the characteristics of Fig. 3.14a, determine I_{CEO} at $V_{CE} = 10$ V.
(b) Determine β_{dc} at $I_B = 10\ \mu$A and $V_{CE} = 10$ V.
(c) Using the β_{dc} determined in part (b), calculate I_{CBO}.

23. (a) Using the characteristics of Fig. 3.14a, determine β_{dc} at $I_B = 80\ \mu$A and $V_{CE} = 5$ V.
(b) Repeat part (a) at $I_B = 5\ \mu$A and $V_{CE} = 15$ V.
(c) Repeat part (a) at $I_B = 30\ \mu$A and $V_{CE} = 10$ V.
(d) Reviewing the results of parts (a) through (c), does the value of β_{dc} change from point to point on the characteristics? Where were the higher values found? Can you develop any general conclusions about the value of β_{dc} on a set of characteristics such as those provided in Fig. 3.14a?

* **24.** (a) Using the characteristics of Fig. 3.14a, determine β_{ac} at $I_B = 80\ \mu$A and $V_{CE} = 5$ V.
(b) Repeat part (a) at $I_B = 5\ \mu$A and $V_{CE} = 15$ V.
(c) Repeat part (a) at $I_B = 30\ \mu$A and $V_{CE} = 10$ V.
(d) Reviewing the results of parts (a) through (c), does the value of β_{ac} change from point to point on the characteristics? Where are the high values located? Can you develop any general conclusions about the value of β_{ac} on a set of collector characteristics?
(e) The chosen points in this exercise are the same as those employed in Problem 23. If Problem 23 was performed, compare the levels of β_{dc} and β_{ac} for each point and comment on the trend in magnitude for each quantity.

25. Using the characteristics of Fig. 3.14a, determine β_{dc} at $I_B = 25\ \mu A$ and $V_{CE} = 10$ V. Then calculate α_{dc} and the resulting level of I_E. (Use the level of I_C determined by $I_C = \beta_{dc} I_B$.)

26. (a) Given that $\alpha_{dc} = 0.987$, determine the corresponding value of β_{dc}.
(b) Given $\beta_{dc} = 120$, determine the corresponding value of α.
(c) Given that $\beta_{dc} = 180$ and $I_C = 2.0$ mA, find I_E and I_B.

27. From memory, and memory only, sketch the common-emitter configuration (for *npn* and *pnp*) and insert the proper biasing arrangement with the resulting current directions for I_B, I_C, and I_E.

§ 3.7 Common-Collector Configuration

28. An input voltage of 2 V rms (measured from base to ground) is applied to the circuit of Fig. 3.21. Assuming that the emitter voltage follows the base voltage exactly and that V_{be} (rms) = 0.1 V, calculate the circuit voltage amplification ($A_v = V_o/V_i$) and emitter current for $R_E = 1\ k\Omega$.

29. For a transistor having the characteristics of Fig. 3.14, sketch the input and output characteristics of the common-collector configuration.

§ 3.8 Limits of Operation

30. Determine the region of operation for a transistor having the characteristics of Fig. 3.14 if $I_{C_{max}} = 7$ mA, $V_{CE_{max}} = 17$ V, and $P_{C_{max}} = 40$ mW.

31. Determine the region of operation for a transistor having the characteristics of Fig. 3.8 if $I_{C_{max}} = 6$ mA, $V_{CB_{max}} = 15$ V, and $P_{C_{max}} = 30$ mW.

§ 3.9 Transistor Specification Sheet

32. Referring to Fig. 3.23, determine the temperature range for the device in degrees Fahrenheit.

33. Using the information provided in Fig. 3.23 regarding $P_{D_{max}}$, $V_{CE_{max}}$, $I_{C_{max}}$ and $V_{CE_{sat}}$, sketch the boundaries of operation for the device.

34. Based on the data of Fig. 3.23, what is the expected value of I_{CEO} using the average value of β_{dc}?

35. How does the range of h_{FE} (Fig. 3.23(j), normalized from $h_{FE} = 100$) compare with the range of h_{fe} (Fig. 3.23(f)) for the range of I_C from 0.1 to 10 mA?

36. Using the characteristics of Fig. 3.23b, determine whether the input capacitance in the common-base configuration increases or decreases with increasing levels of reverse-bias potential. Can you explain why?

* **37.** Using the characteristics of Fig. 3.23f, determine how much the level of h_{fe} has changed from its value at 1 mA to its value at 10 mA. Note that the vertical scale is a log scale that may require reference to Section 11.2. Is the change one that should be considered in a design situation?

* **38.** Using the characteristics of Fig. 3.23j, determine the level of β_{dc} at $I_C = 10$ mA at the three levels of temperature appearing in the figure. Is the change significant for the specified temperature range? Is it an element to be concerned about in the design process?

§ 3.10 Transistor Testing

39. (a) Using the characteristics of Fig. 3.24, determine β_{ac} at $I_C = 14$ mA and $V_{CE} = 3$ V.
(b) Determine β_{dc} at $I_C = 1$ mA and $V_{CE} = 8$ V.
(c) Determine β_{ac} at $I_C = 14$ mA and $V_{CE} = 3$ V.
(d) Determine β_{dc} at $I_C = 1$ mA and $V_{CE} = 8$ V.
(e) How does the level of β_{ac} and β_{dc} compare in each region?
(f) Is the approximation $\beta_{dc} \cong \beta_{ac}$ a valid one for this set of characteristics?

*Please Note: Asterisks indicate more difficult problems.