CHAPTER

2 Diode Applications

2.1 INTRODUCTION

The construction, characteristics, and models of semiconductor diodes were introduced in Chapter 1. The primary goal of this chapter is to develop a working knowledge of the diode in a variety of configurations using models appropriate for the area of application. By chapter's end, the fundamental behavior pattern of diodes in dc and ac networks should be clearly understood. The concepts learned in this chapter will have significant carryover in the chapters to follow. For instance, diodes are frequently employed in the description of the basic construction of transistors and in the analysis of transistor networks in the dc and ac domains.

The content of this chapter will reveal an interesting and very positive side of the study of a field such as electronic devices and systems—once the basic behavior of a device is understood, its function and response in an infinite variety of configurations can be determined. The range of applications is endless, yet the characteristics and models remain the same. The analysis will proceed from one that employs the actual diode characteristic to one that utilizes the approximate models almost exclusively. It is important that the role and response of various elements of an electronic system be understood without continually having to resort to lengthy mathematical procedures. This is usually accomplished through the approximation process, which can develop into an art itself. Although the results obtained using the actual characteristics may be slightly different from those obtained using a series of approximations, keep in mind that the characteristics obtained from a specification sheet may in themselves be slightly different from the device in actual use. In other words, the characteristics of a 1N4001 semiconductor diode may vary from one element to the next in the same lot. The variation may be slight, but it will often be sufficient to validate the approximations employed in the analysis. Also consider the other elements of the network: Is the resistor labeled 100 Ω exactly 100 Ω? Is the applied voltage exactly 10 V or perhaps 10.08 V? All these tolerances contribute to the general belief that a response determined through an appropriate set of approximations can often be "as accurate" as one that employs the full characteristics. In this book the emphasis is toward developing a working knowledge of a device through the use of appropriate approximations, thereby avoiding an unnecessary level of mathematical complexity. Sufficient detail will normally be provided, however, to permit a detailed mathematical analysis if desired.

2.2 LOAD-LINE ANALYSIS

The applied load will normally have an important impact on the point or region of operation of a device. If the analysis is performed in a graphical manner, a line can be drawn on the characteristics of the device that represents the applied load. The intersection of the load line with the characteristics will determine the point of operation of the system. Such an analysis is, for obvious reasons, called *load-line analysis*. Although the majority of the diode networks analyzed in this chapter do not employ the load-line approach, the technique is one used quite frequently in subsequent chapters, and this introduction offers the simplest application of the method. It also permits a validation of the approximate technique described throughout the remainder of this chapter.

Consider the network of Fig. 2.1a employing a diode having the characteristics of Fig. 2.1b. Note in Fig. 2.1a that the "pressure" established by the battery is to establish a current through the series circuit in the clockwise direction. The fact that this current and the defined direction of conduction of the diode are a "match" reveals that the diode is in the "on" state and conduction has been established. The resulting polarity across the diode will be as shown and the first quadrant (V_D and I_D positive) of Fig. 2.1b will be the region of interest—the forward-bias region.

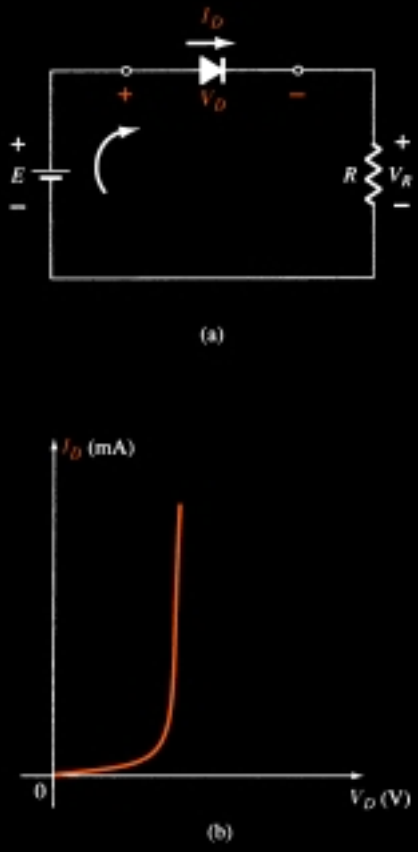


Figure 2.1 Series diode configuration: (a) circuit; (b) characteristics.

Applying Kirchhoff's voltage law to the series circuit of Fig. 2.1a will result in

$$E - V_D - V_R = 0$$

or

$$\boxed{E = V_D + I_D R} \tag{2.1}$$

The two variables of Eq. (2.1) (V_D and I_D) are the same as the diode axis variables of Fig. 2.1b. This similarity permits a plotting of Eq. (2.1) on the same characteristics of Fig. 2.1b.

The intersections of the load line on the characteristics can easily be determined if one simply employs the fact that anywhere on the horizontal axis $I_D = 0$ A and anywhere on the vertical axis $V_D = 0$ V.

If we *set* $V_D = 0$ V in Eq. (2.1) and solve for I_D, we have the magnitude of I_D *on* the vertical axis. Therefore, with $V_D = 0$ V, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= 0\ \text{V} + I_D R \end{aligned}$$

and

$$\boxed{I_D = \left.\frac{E}{R}\right|_{V_D = 0\ \text{V}}} \tag{2.2}$$

as shown in Fig. 2.2. If we *set* $I_D = 0$ A in Eq. (2.1) and solve for V_D, we have the magnitude of V_D *on* the horizontal axis. Therefore, with $I_D = 0$ A, Eq. (2.1) becomes

$$\begin{aligned} E &= V_D + I_D R \\ &= V_D + (0\ \text{A})R \end{aligned}$$

and

$$\boxed{V_D = \left. E \right|_{I_D = 0\ A}} \tag{2.3}$$

as shown in Fig. 2.2. A straight line drawn between the two points will define the load line as depicted in Fig. 2.2. Change the level of R (the load) and the intersection on the vertical axis will change. The result will be a change in the slope of the load line and a different point of intersection between the load line and the device characteristics.

We now have a load line defined by the network and a characteristic curve defined by the device. The point of intersection between the two is the point of opera-

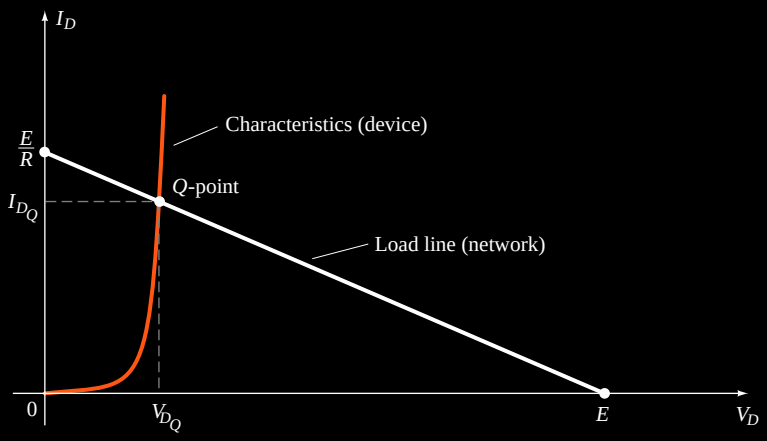


Figure 2.2 Drawing the load line and finding the point of operation.

tion for this circuit. By simply drawing a line down to the horizontal axis the diode voltage V_{D_Q} can be determined, whereas a horizontal line from the point of intersection to the vertical axis will provide the level of I_{D_Q}. The current I_D is actually the current through the entire series configuration of Fig. 2.1a. The point of operation is usually called the *quiescent point* (abbreviated "*Q*-pt.") to reflect its "still, unmoving" qualities as defined by a dc network.

The solution obtained at the intersection of the two curves is the same that would be obtained by a simultaneous mathematical solution of Eqs. (2.1) and (1.4) $[I_D = I_s(e^{kV_D/T_K} - 1)]$. Since the curve for a diode has nonlinear characteristics the mathematics involved would require the use of nonlinear techniques that are beyond the needs and scope of this book. The load-line analysis described above provides a solution with a minimum of effort and a "pictorial" description of why the levels of solution for V_{D_Q} and I_{D_Q} were obtained. The next two examples will demonstrate the techniques introduced above and reveal the relative ease with which the load line can be drawn using Eqs. (2.2) and (2.3).

EXAMPLE 2.1

For the series diode configuration of Fig. 2.3a employing the diode characteristics of Fig. 2.3b determine:
(a) V_{D_Q} and I_{D_Q}.
(b) V_R.

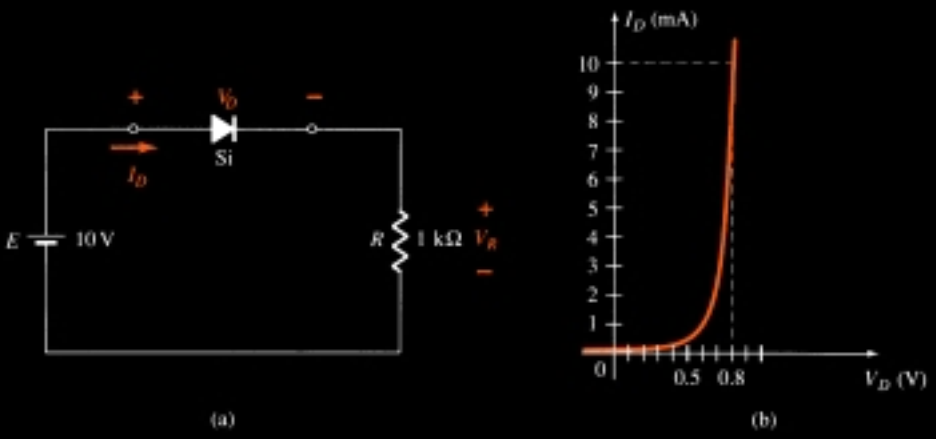


Figure 2.3 (a) Circuit; (b) characteristics.

Solution

(a) Eq. (2.2): $I_D = \left.\frac{E}{R}\right|_{V_D=0\text{ V}} = \frac{10\text{ V}}{2\text{ k}\Omega} = 10\text{ mA}$

Eq. (2.3): $V_D = E|_{I_D=0\text{ A}} = 10\text{ V}$

The resulting load line appears in Fig. 2.4. The intersection between the load line and the characteristic curve defines the *Q*-point as

$$V_{D_Q} \cong \mathbf{0.78\text{ V}}$$

$$I_{D_Q} \cong \mathbf{9.25\text{ mA}}$$

The level of V_D is certainly an estimate, and the accuracy of I_D is limited by the chosen scale. A higher degree of accuracy would require a plot that would be much larger and perhaps unwieldy.

(b) $V_R = I_R R = I_{D_Q} R = (9.25\text{ mA})(1\text{ k}\Omega) = \mathbf{9.25\text{ V}}$

or $V_R = E - V_D = 10\text{ V} - 0.78\text{ V} = \mathbf{9.22\text{ V}}$

The difference in results is due to the accuracy with which the graph can be read. Ideally, the results obtained either way should be the same.

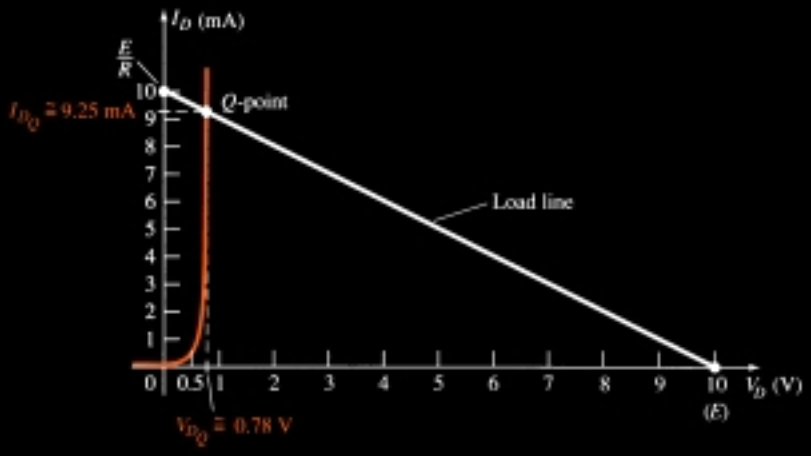


Figure 2.4 Solution to Example 2.1.

EXAMPLE 2.2 Repeat the analysis of Example 2.1 with $R = 2\text{ k}\Omega$.

Solution

(a) Eq. (2.2): $I_D = \left.\frac{E}{R}\right|_{V_D=0\text{ V}} = \frac{10\text{ V}}{2\text{ k}\Omega} = 5\text{ mA}$

Eq. (2.3): $V_D = E|_{I_D=0\text{ A}} = 10\text{ V}$

The resulting load line appears in Fig. 2.5. Note the reduced slope and levels of diode current for increasing loads. The resulting *Q*-point is defined by

$$V_{D_Q} \cong \mathbf{0.7\text{ V}}$$

$$I_{D_Q} \cong \mathbf{4.6\text{ mA}}$$

(b) $V_R = I_R R = I_{D_Q} R = (4.6\text{ mA})(2\text{ k}\Omega) = \mathbf{9.2\text{ V}}$

with $V_R = E - V_D = 10\text{ V} - 0.7\text{ V} = \mathbf{9.3\text{ V}}$

The difference in levels is again due to the accuracy with which the graph can be read. Certainly, however, the results provide an expected magnitude for the voltage V_R.

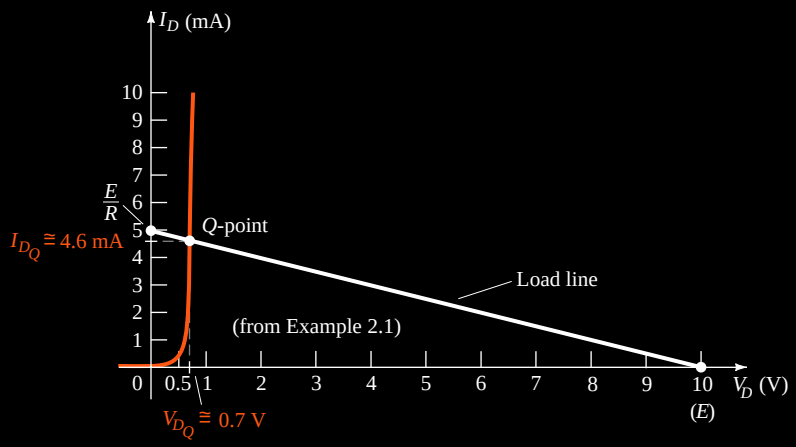


Figure 2.5 Solution to Example 2.2.

As noted in the examples above, the load line is determined solely by the applied network while the characteristics are defined by the chosen device. If we turn to our approximate model for the diode and do not disturb the network, the load line will be exactly the same as obtained in the examples above. In fact, the next two examples repeat the analysis of Examples 2.1 and 2.2 using the approximate model to permit a comparison of the results.

EXAMPLE 2.3

Repeat Example 2.1 using the approximate equivalent model for the silicon semiconductor diode.

Solution

The load line is redrawn as shown in Fig. 2.6 with the same intersections as defined in Example 2.1. The characteristics of the approximate equivalent circuit for the diode have also been sketched on the same graph. The resulting *Q*-point:

$$V_{D_Q} = \mathbf{0.7\ V}$$

$$I_{D_Q} = \mathbf{9.25\ mA}$$

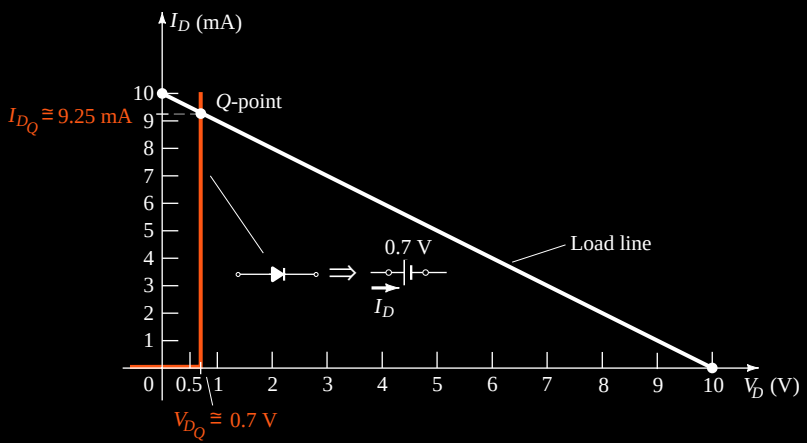


Figure 2.6 Solution to Example 2.1 using the diode approximate model.

The results obtained in Example 2.3 are quite interesting. The level of I_{D_Q} is exactly the same as obtained in Example 2.1 using a characteristic curve that is a great deal easier to draw than that appearing in Fig. 2.4. The level of $V_D = 0.7$ V versus 0.78 V from Example 2.1 is of a different magnitude to the hundredths place, but they are certainly in the same neighborhood if we compare their magnitudes to the magnitudes of the other voltages of the network.

EXAMPLE 2.4

Repeat Example 2.2 using the approximate equivalent model for the silicon semiconductor diode.

Solution

The load line is redrawn as shown in Fig. 2.7 with the same intersections defined in Example 2.2. The characteristics of the approximate equivalent circuit for the diode have also been sketched on the same graph. The resulting *Q*-point:

$$V_{D_Q} = \mathbf{0.7\ V}$$

$$I_{D_Q} = \mathbf{4.6\ mA}$$

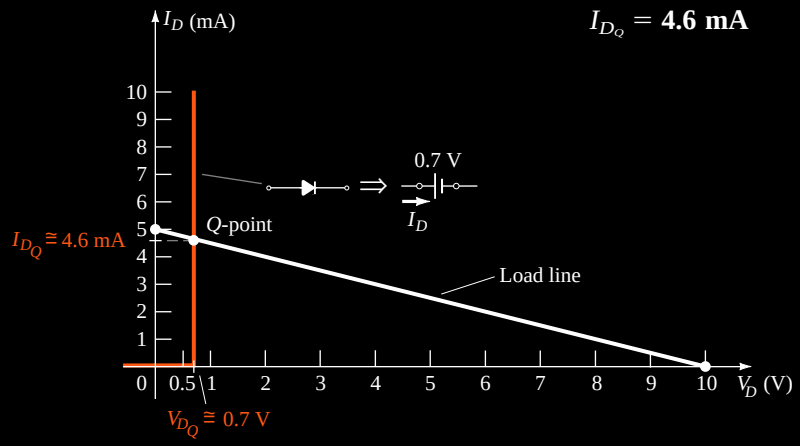


Figure 2.7 Solution to Example 2.2 using the diode approximate model.

In Example 2.4 the results obtained for both V_{D_Q} and I_{D_Q} are the same as those obtained using the full characteristics in Example 2.2. The examples above have demonstrated that the current and voltage levels obtained using the approximate model have been very close to those obtained using the full characteristics. It suggests, as will be applied in the sections to follow, that the use of appropriate approximations can result in solutions that are very close to the actual response with a reduced level of concern about properly reproducing the characteristics and choosing a large-enough scale. In the next example we go a step further and substitute the ideal model. The results will reveal the conditions that must be satisfied to apply the ideal equivalent properly.

EXAMPLE 2.4

Repeat Example 2.1 using the ideal diode model.

Solution

As shown in Fig. 2.8 the load line continues to be the same, but the ideal characteristics now intersect the load line on the vertical axis. The *Q*-point is therefore defined by

$$V_{D_Q} = \mathbf{0\ V}$$

$$I_{D_Q} = \mathbf{10\ mA}$$

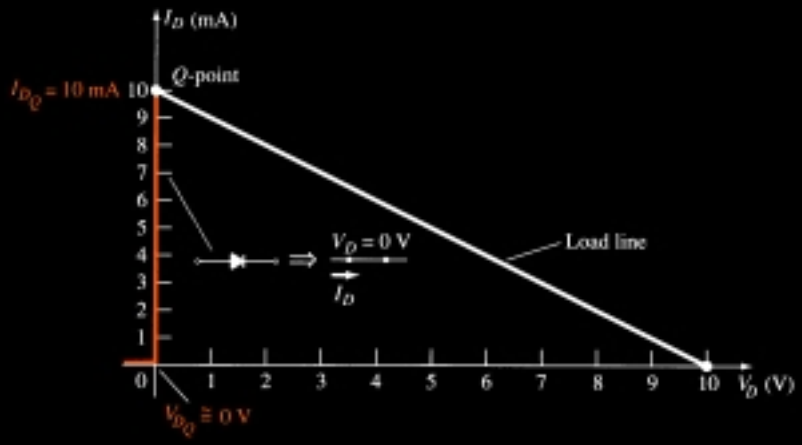


Figure 2.8 Solution to Example 2.1 using the ideal diode model.

The results are sufficiently different from the solutions of Example 2.1 to cause some concern about their accuracy. Certainly, they do provide some indication of the level of voltage and current to be expected relative to the other voltage levels of the network, but the additional effort of simply including the 0.7-V offset suggests that the approach of Example 2.3 is more appropriate.

Use of the ideal diode model therefore should be reserved for those occasions when the role of a diode is more important than voltage levels that differ by tenths of a volt and in those situations where the applied voltages are considerably larger than the threshold voltage V_T. In the next few sections the approximate model will be employed exclusively since the voltage levels obtained will be sensitive to variations that approach V_T. In later sections the ideal model will be employed more frequently since the applied voltages will frequently be quite a bit larger than V_T and the authors want to ensure that the role of the diode is correctly and clearly understood.

2.3 DIODE APPROXIMATIONS

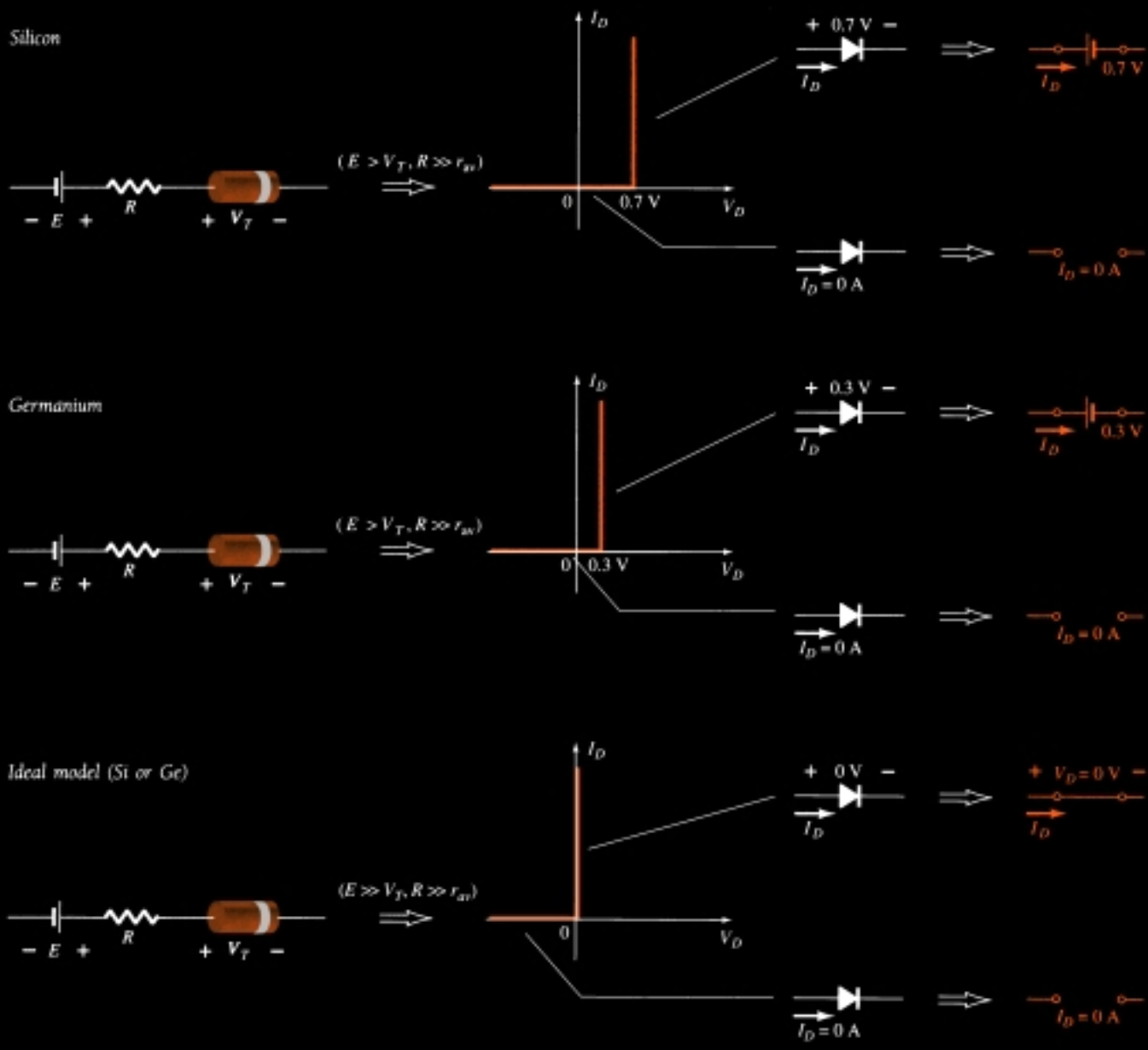
In Section 2.2 we revealed that the results obtained using the approximate piecewise-linear equivalent model were quite close, if not equal, to the response obtained using the full characteristics. In fact, if one considers all the variations possible due to tolerances, temperature, and so on, one could certainly consider one solution to be "as accurate" as the other. Since the use of the approximate model normally results in a reduced expenditure of time and effort to obtain the desired results, it is the approach that will be employed in this book unless otherwise specified. Recall the following:

The primary purpose of this book is to develop a general knowledge of the behavior, capabilities, and possible areas of application of a device in a manner that will minimize the need for extensive mathematical developments.

The complete piecewise-linear equivalent model introduced in Chapter 1 was not employed in the load-line analysis because r_{av} is typically much less than the other series elements of the network. If r_{av} should be close in magnitude to the other series elements of the network, the complete equivalent model can be applied in much the same manner as described in Section 2.2.

In preparation for the analysis to follow, Table 2.1 was developed to review the important characteristics, models, and conditions of application for the approximate and ideal diode models. Although the silicon diode is used almost exclusively due to

TABLE 2.1 Approximate and Ideal Semiconductor Diode Models



its temperature characteristics, the germanium diode is still employed and is therefore included in Table 2.1. As with the silicon diode, a germanium diode is approximated by an open-circuit equivalent for voltages less than V_T. It will enter the "on" state when $V_D \geq V_T = 0.3$ V.

Keep in mind that the 0.7 and 0.3 V in the equivalent circuits are not *independent* sources of energy but are there simply to remind us that there is a "price to pay" to turn on a diode. An isolated diode on a laboratory table will not indicate 0.7 or 0.3 V if a voltmeter is placed across its terminals. The supplies specify the voltage drop across each when the device is "on" and specify that the diode voltage must be at least the indicated level before conduction can be established.

In the next few sections we demonstrate the impact of the models of Table 2.1 on the analysis of diode configurations. For those situations where the approximate equivalent circuit will be employed, the diode symbol will appear as shown in Fig. 2.9a for the silicon and germanium diodes. If conditions are such that the ideal diode model can be employed, the diode symbol will appear as shown in Fig. 2.9b.

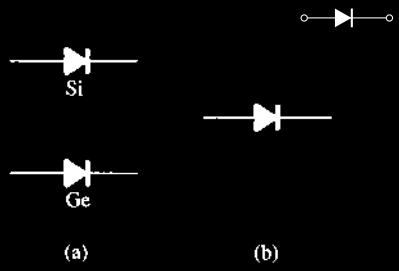


Figure 2.9 (a) Approximate model notation; (b) ideal diode notation.

2.4 SERIES DIODE CONFIGURATIONS WITH DC INPUTS

In this section the approximate model is utilized to investigate a number of series diode configurations with dc inputs. The content will establish a foundation in diode analysis that will carry over into the sections and chapters to follow. The procedure described can, in fact, be applied to networks with any number of diodes in a variety of configurations.

For each configuration the state of each diode must first be determined. Which diodes are "on" and which are "off"? Once determined, the appropriate equivalent as defined in Section 2.3 can be substituted and the remaining parameters of the network determined.

In general, a diode is in the "on" state if the current established by the applied sources is such that its direction matches that of the arrow in the diode symbol, and $V_D \geq 0.7$ V for silicon and $V_D \geq 0.3$ V for germanium.

For each configuration, *mentally* replace the diodes with resistive elements and note the resulting current direction as established by the applied voltages ("pressure"). If the resulting direction is a "match" with the arrow in the diode symbol, conduction through the diode will occur and the device is in the "on" state. The description above is, of course, contingent on the supply having a voltage greater than the "turn-on" voltage (V_T) of each diode.

If a diode is in the "on" state, one can either place a 0.7-V drop across the element, or the network can be redrawn with the V_T equivalent circuit as defined in Table 2.1. In time the preference will probably simply be to include the 0.7-V drop across each "on" diode and draw a line through each diode in the "off" or open state. Initially, however, the substitution method will be utilized to ensure that the proper voltage and current levels are determined.

The series circuit of Fig. 2.10 described in some detail in Section 2.2 will be used to demonstrate the approach described in the paragraphs above. The state of the diode is first determined by mentally replacing the diode with a resistive element as shown in Fig. 2.11. The resulting direction of I is a match with the arrow in the diode symbol, and since $E > V_T$ the diode is in the "on" state. The network is then redrawn as shown in Fig. 2.12 with the appropriate equivalent model for the forward-biased silicon diode. Note for future reference that the polarity of V_D is the same as would result if in fact the diode were a resistive element. The resulting voltage and current levels are the following:

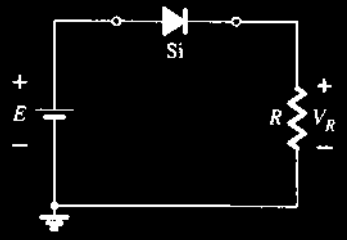


Figure 2.10 Series diode configuration.

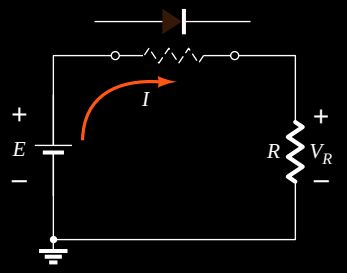


Figure 2.11 Determining the state of the diode of Fig. 2.10.

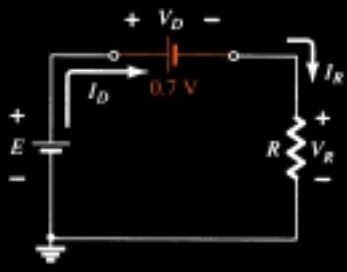


Figure 2.12 Substituting the equivalent model for the "on" diode of Fig. 2.10.

$$V_D = V_T \tag{2.4}$$

$$V_R = E - V_T \tag{2.5}$$

$$I_D = I_R = \frac{V_R}{R} \tag{2.6}$$

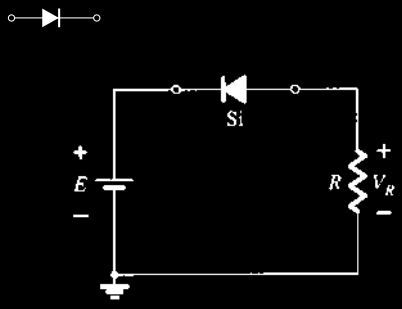


Figure 2.13 Reversing the diode of Fig. 2.10.

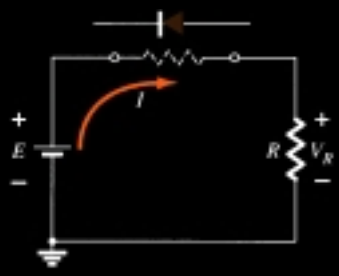


Figure 2.14 Determining the state of the diode of Fig. 2.13.

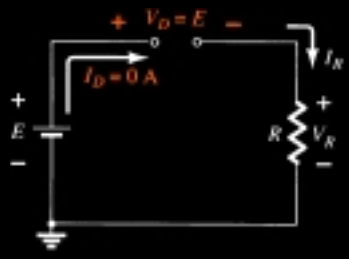


Figure 2.15 Substituting the equivalent model for the "off" diode of Figure 2.13.

In Fig. 2.13 the diode of Fig. 2.10 has been reversed. Mentally replacing the diode with a resistive element as shown in Fig. 2.14 will reveal that the resulting current direction does not match the arrow in the diode symbol. The diode is in the "off" state, resulting in the equivalent circuit of Fig. 2.15. Due to the open circuit, the diode current is 0 A and the voltage across the resistor R is the following:

$$V_R = I_R R = I_D R = (0\text{ A})R = \mathbf{0\text{ V}}$$

The fact that $V_R = 0$ V will establish E volts across the open circuit as defined by Kirchhoff's voltage law. Always keep in mind that under any circumstances—dc, ac instantaneous values, pulses, and so on—Kirchhoff's voltage law must be satisfied!

EXAMPLE 2.6

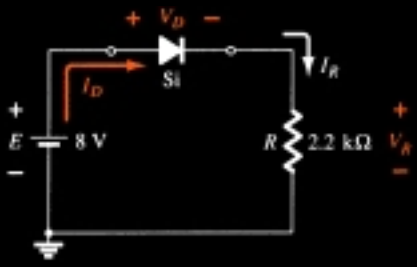


Figure 2.16 Circuit for Example 2.6.

For the series diode configuration of Fig. 2.16, determine V_D, V_R, and I_D.

Solution

Since the applied voltage establishes a current in the clockwise direction to match the arrow of the symbol and the diode is in the "on" state,

$$V_D = \mathbf{0.7\text{ V}}$$

$$V_R = E - V_D = 8\text{ V} - 0.7\text{ V} = \mathbf{7.3\text{ V}}$$

$$I_D = I_R = \frac{V_R}{R} = \frac{7.3\text{ V}}{2.2\text{ k}\Omega} \cong \mathbf{3.32\text{ mA}}$$

EXAMPLE 2.7

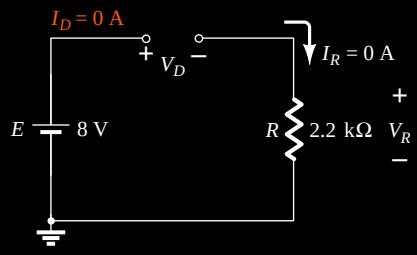


Figure 2.17 Determining the unknown quantities for Example 2.7.

Repeat Example 2.6 with the diode reversed.

Solution

Removing the diode, we find that the direction of I is opposite to the arrow in the diode symbol and the diode equivalent is the open circuit no matter which model is employed. The result is the network of Fig. 2.17, where $I_D = \mathbf{0\text{ A}}$ due to the open circuit. Since $V_R = I_R R$, $V_R = (0)R = 0$ V. Applying Kirchhoff's voltage law around the closed loop yields

$$E - V_D - V_R = 0$$

and

$$V_D = E - V_R = E - 0 = E = \mathbf{8\text{ V}}$$

In particular, note in Example 2.7 the high voltage across the diode even though it is an "off" state. The current is zero, but the voltage is significant. For review purposes, keep the following in mind for the analysis to follow:

1. An open circuit can have any voltage across its terminals, but the current is always 0 A.
2. A short circuit has a 0-V drop across its terminals, but the current is limited only by the surrounding network.

In the next example the notation of Fig. 2.18 will be employed for the applied voltage. It is a common industry notation and one with which the reader should become very familiar. Such notation and other defined voltage levels are treated further in Chapter 4.

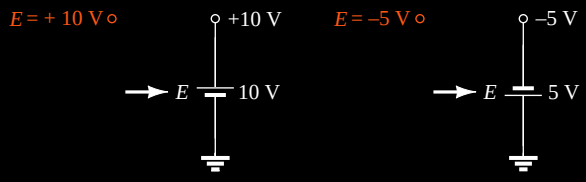


Figure 2.18 Source notation.

EXAMPLE 2.8

For the series diode configuration of Fig. 2.19, determine V_D, V_R, and I_D.

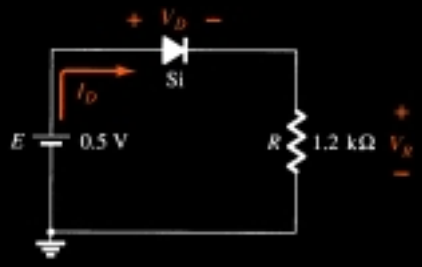


Figure 2.19 Series diode circuit for Example 2.8.

Solution

Although the "pressure" establishes a current with the same direction as the arrow symbol, the level of applied voltage is insufficient to turn the silicon diode "on." The point of operation on the characteristics is shown in Fig. 2.20, establishing the open-circuit equivalent as the appropriate approximation. The resulting voltage and current levels are therefore the following:

$$I_D = \mathbf{0\ A}$$

$$V_R = I_R R = I_D R = (0\ \text{A})1.2\ \text{k}\Omega = \mathbf{0\ V}$$

and

$$V_D = E = \mathbf{0.5\ V}$$

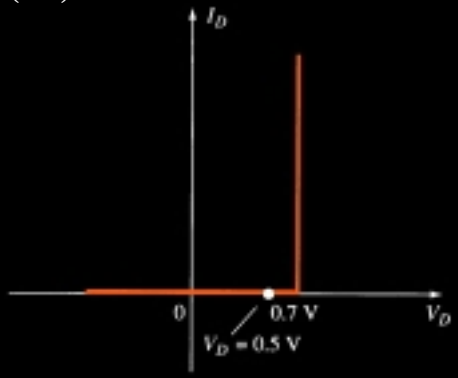


Figure 2.20 Operating point with $E = 0.5$ V.

EXAMPLE 2.9

Determine V_o and I_D for the series circuit of Fig. 2.21.

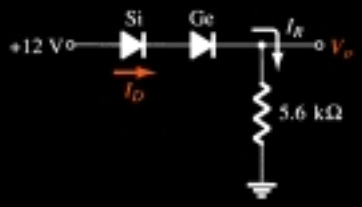


Figure 2.21 Circuit for Example 2.9.

Solution

An attack similar to that applied in Example 2.6 will reveal that the resulting current has the same direction as the arrowheads of the symbols of both diodes, and the network of Fig. 2.22 results because $E = 12\text{ V} > (0.7\text{ V} + 0.3\text{ V}) = 1\text{ V}$. Note the redrawn supply of 12 V and the polarity of V_o across the 5.6-kΩ resistor. The resulting voltage

$$V_o = E - V_{T_1} - V_{T_2} = 12\text{ V} - 0.7\text{ V} - 0.3\text{ V} = \mathbf{11\text{ V}}$$

and

$$I_D = I_R = \frac{V_R}{R} = \frac{V_o}{R} = \frac{11\text{ V}}{5.6\text{ k}\Omega} \cong \mathbf{1.96\text{ mA}}$$

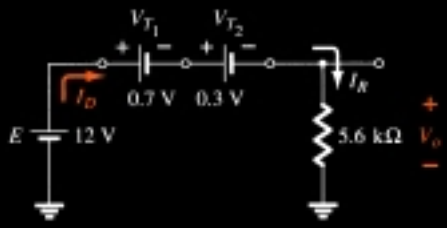


Figure 2.22 Determining the unknown quantities for Example 2.9.

EXAMPLE 2.10

Determine I_D, V_{D_2}, and V_o for the circuit of Fig. 2.23.

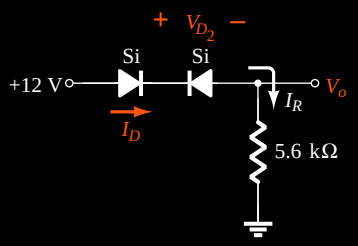


Figure 2.23 Circuit for Example 2.10.

Solution

Removing the diodes and determining the direction of the resulting current I will result in the circuit of Fig. 2.24. There is a match in current direction for the silicon diode but not for the germanium diode. The combination of a short circuit in series with an open circuit always results in an open circuit and $I_D = \mathbf{0\text{ A}}$, as shown in Fig. 2.25.

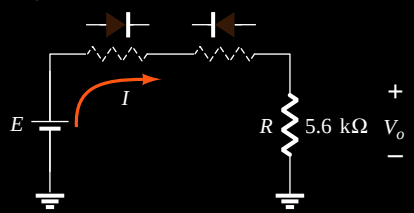


Figure 2.24 Determining the state of the diodes of Figure 2.23.

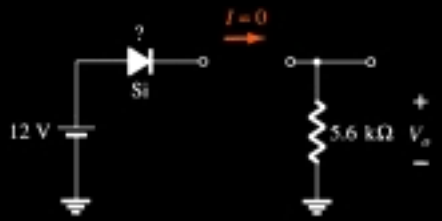


Figure 2.25 Substituting the equivalent state for the open diode.

The question remains as to what to substitute for the silicon diode. For the analysis to follow in this and succeeding chapters, simply recall for the actual practical diode that when $I_D = 0$ A, $V_D = 0$ V (and vice versa), as described for the no-bias situation in Chapter 1. The conditions described by $I_D = 0$ A and $V_{D_1} = 0$ V are indicated in Fig. 2.26.

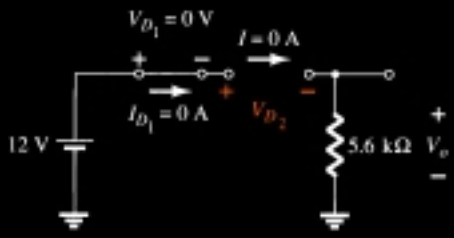


Figure 2.26 Determining the unknown quantities for the circuit of Example 2.10.

$$V_o = I_R R = I_D R = (0 \text{ A})R = 0 \text{ V}$$

and
$$V_{D_2} = V_{\text{open circuit}} = E = \mathbf{12\ V}$$

Applying Kirchhoff's voltage law in a clockwise direction gives us

$$E - V_{D_1} - V_{D_2} - V_o = 0$$

and
$$V_{D_2} = E - V_{D_1} - V_o = 12 \text{ V} - 0 - 0$$
$$= \mathbf{12\ V}$$

with
$$V_o = \mathbf{0\ V}$$

Determine I, V_1, V_2, and V_o for the series dc configuration of Fig. 2.27. *EXAMPLE 2.11*

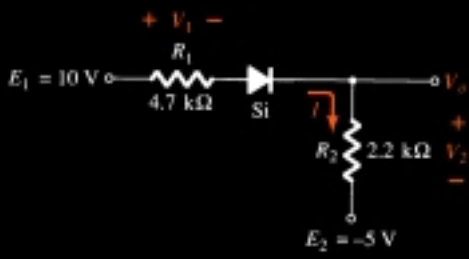


Figure 2.27 Circuit for Example 2.11.

Solution

The sources are drawn and the current direction indicated as shown in Fig. 2.28. The diode is in the "on" state and the notation appearing in Fig. 2.29 is included to indicate this state. Note that the "on" state is noted simply by the additional $V_D = 0.7$ V

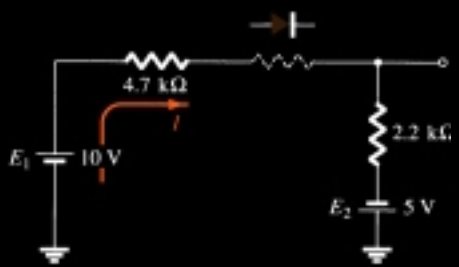


Figure 2.28 Determining the state of the diode for the network of Fig. 2.27.

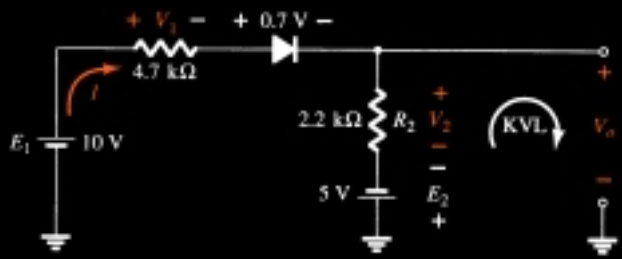


Figure 2.29 Determining the unknown quantities for the network of Fig. 2.27.

on the figure. This eliminates the need to redraw the network and avoids any confusion that may result from the appearance of another source. As indicated in the introduction to this section, this is probably the path and notation that one will take when a level of confidence has been established in the analysis of diode configurations. In time the entire analysis will be performed simply by referring to the original network. Recall that a reverse-biased diode can simply be indicated by a line through the device.

The resulting current through the circuit is,

$$I = \frac{E_1 + E_2 - V_D}{R_1 + R_2} = \frac{10\text{ V} + 5\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega + 2.2\text{ k}\Omega} = \frac{14.3\text{ V}}{6.9\text{ k}\Omega}$$

$$\cong \mathbf{2.072\text{ mA}}$$

and the voltages are

$$V_1 = IR_1 = (2.072\text{ mA})(4.7\text{ k}\Omega) = \mathbf{9.74\text{ V}}$$

$$V_2 = IR_2 = (2.072\text{ mA})(2.2\text{ k}\Omega) = \mathbf{4.56\text{ V}}$$

Applying Kirchhoff's voltage law to the output section in the clockwise direction will result in

$$-E_2 + V_2 - V_o = 0$$

and

$$V_o = V_2 - E_2 = 4.56\text{ V} - 5\text{ V} = \mathbf{-0.44\text{ V}}$$

The minus sign indicates that V_o has a polarity opposite to that appearing in Fig. 2.27.

2.5 PARALLEL AND SERIES–PARALLEL CONFIGURATIONS

The methods applied in Section 2.4 can be extended to the analysis of parallel and series–parallel configurations. For each area of application, simply match the sequential series of steps applied to series diode configurations.

EXAMPLE 2.12

Determine V_o, I_1, I_{D_1}, and I_{D_2} for the parallel diode configuration of Fig. 2.30.

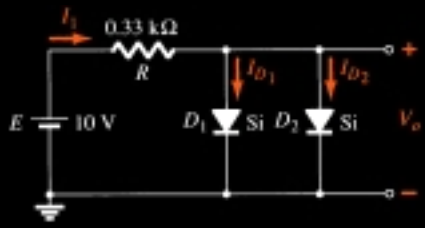


Figure 2.30 Network for Example 2.12.

Solution

For the applied voltage the "pressure" of the source is to establish a current through each diode in the same direction as shown in Fig. 2.31. Since the resulting current direction matches that of the arrow in each diode symbol and the applied voltage is greater than 0.7 V, both diodes are in the "on" state. The voltage across parallel elements is always the same and

$$V_o = \mathbf{0.7\text{ V}}$$

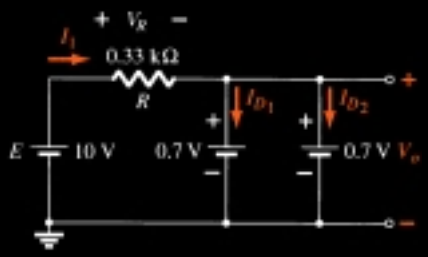


Figure 2.31 Determining the unknown quantities for the network of Example 2.12.

The current

$$I_1 = \frac{V_R}{R} = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{0.33\text{ k}\Omega} = \mathbf{28.18\text{ mA}}$$

Assuming diodes of similar characteristics, we have

$$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18\text{ mA}}{2} = \mathbf{14.09\text{ mA}}$$

Example 2.12 demonstrated one reason for placing diodes in parallel. If the current rating of the diodes of Fig. 2.30 is only 20 mA, a current of 28.18 mA would damage the device if it appeared alone in Fig. 2.30. By placing two in parallel, the current is limited to a safe value of 14.09 mA with the same terminal voltage.

EXAMPLE 2.13

Determine the current I for the network of Fig. 2.32.

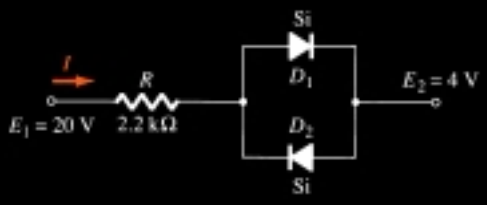


Figure 2.32 Network for Example 2.13.

Solution

Redrawing the network as shown in Fig. 2.33 reveals that the resulting current direction is such as to turn on diode D_1 and turn off diode D_2. The resulting current I is then

$$I = \frac{E_1 - E_2 - V_D}{R} = \frac{20\text{ V} - 4\text{ V} - 0.7\text{ V}}{2.2\text{ k}\Omega} \cong \mathbf{6.95\text{ mA}}$$

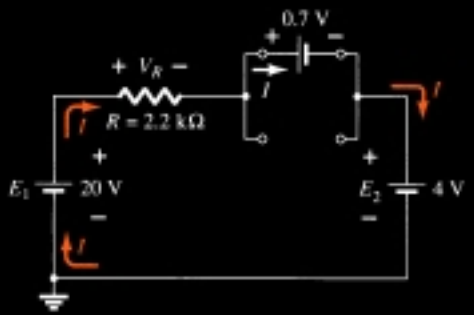


Figure 2.33 Determining the unknown quantities for the network of Example 2.13.

EXAMPLE 2.14

Determine the voltage V_o for the network of Fig. 2.34.

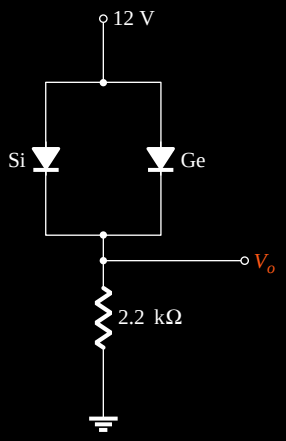


Figure 2.34 Network for Example 2.14.

Solution

Initially, it would appear that the applied voltage will turn both diodes "on." However, if both were "on," the 0.7-V drop across the silicon diode would not match the 0.3 V across the germanium diode as required by the fact that the voltage across parallel elements must be the same. The resulting action can be explained simply by realizing that when the supply is turned on it will increase from 0 to 12 V over a period of time—although probably measurable in milliseconds. At the instant during the rise that 0.3 V is established across the germanium diode it will turn "on" and maintain a level of 0.3 V. The silicon diode will never have the opportunity to capture its required 0.7 V and therefore remains in its open-circuit state as shown in Fig. 2.35. The result:

$$V_o = 12\text{ V} - 0.3\text{ V} = \mathbf{11.7\text{ V}}$$

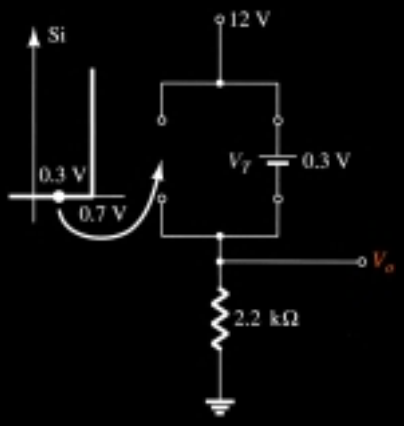


Figure 2.35 Determining V_o for the network of Fig. 2.34.

EXAMPLE 2.15

Determine the currents I_1, I_2, and I_{D_2} for the network of Fig. 2.36.

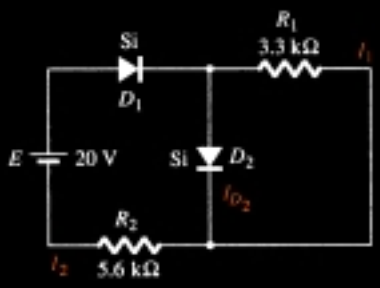


Figure 2.36 Network for Example 2.15.

Solution

The applied voltage (pressure) is such as to turn both diodes on, as noted by the resulting current directions in the network of Fig. 2.37. Note the use of the abbreviated notation for "on" diodes and that the solution is obtained through an application of techniques applied to dc series—parallel networks.

$$I_1 = \frac{V_{T_2}}{R_1} = \frac{0.7\text{ V}}{3.3\text{ k}\Omega} = \mathbf{0.212\text{ mA}}$$

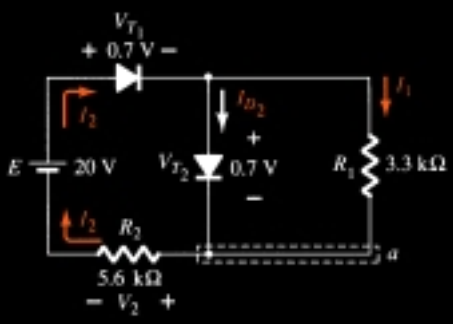


Figure 2.37 Determining the unknown quantities for Example 2.15.

Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction yields

$$-V_2 + E - V_{T_1} - V_{T_2} = 0$$

and $$V_2 = E - V_{T_1} - V_{T_2} = 20\text{ V} - 0.7\text{ V} - 0.7\text{ V} = 18.6\text{ V}$$

with $$I_2 = \frac{V_2}{R_2} = \frac{18.6\text{ V}}{5.6\text{ k}\Omega} = \mathbf{3.32\text{ mA}}$$

At the bottom node (a),

$$I_{D_2} + I_1 = I_2$$

and $$I_{D_2} = I_2 - I_1 = 3.32\text{ mA} - 0.212\text{ mA} = \mathbf{3.108\text{ mA}}$$

2.6 AND/OR GATES

The tools of analysis are now at our disposal, and the opportunity to investigate a computer configuration is one that will demonstrate the range of applications of this relatively simple device. Our analysis will be limited to determining the voltage levels and will not include a detailed discussion of Boolean algebra or positive and negative logic.

The network to be analyzed in Example 2.16 is an OR gate for positive logic. That is, the 10-V level of Fig. 2.38 is assigned a "1" for Boolean algebra while the 0-V input is assigned a "0." An OR gate is such that the output voltage level will be a 1 if either *or* both inputs is a 1. The output is a 0 if both inputs are at the 0 level.

The analysis of AND/OR gates is made measurably easier by using the approximate equivalent for a diode rather than the ideal because we can stipulate that the voltage across the diode must be 0.7 V positive for the silicon diode (0.3 V for Ge) to switch to the "on" state.

In general, the best approach is simply to establish a "gut" feeling for the state of the diodes by noting the direction and the "pressure" established by the applied potentials. The analysis will then verify or negate your initial assumptions.

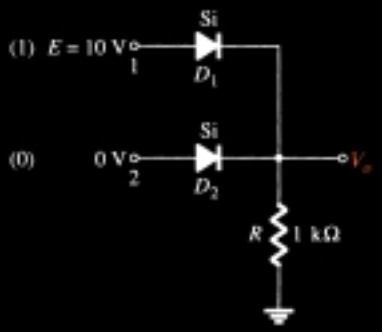


Figure 2.38 Positive logic OR gate.

EXAMPLE 2.16

Determine V_o for the network of Fig. 2.38.

Solution

First note that there is only one applied potential; 10 V at terminal 1. Terminal 2 with a 0-V input is essentially at ground potential, as shown in the redrawn network of Fig. 2.39. Figure 2.39 "suggests" that D_1 is probably in the "on" state due to the applied 10 V while D_2 with its "positive" side at 0 V is probably "off." Assuming these states will result in the configuration of Fig. 2.40.

The next step is simply to check that there is no contradiction to our assumptions. That is, note that the polarity across D_1 is such as to turn it on and the polarity across D_2 is such as to turn it off. For D_1 the "on" state establishes V_o at $V_o = E - V_D = 10\text{ V} - 0.7\text{ V} = \mathbf{9.3\text{ V}}$. With 9.3 V at the cathode (−) side of D_2 and 0 V at the anode (+) side, D_2 is definitely in the "off" state. The current direction and the resulting continuous path for conduction further confirm our assumption that D_1 is conducting. Our assumptions seem confirmed by the resulting voltages and current, and our initial analysis can be assumed to be correct. The output voltage level is not 10 V as defined for an input of 1, but the 9.3 V is sufficiently large to be considered a 1 level. The output is therefore at a 1 level with only one input, which suggests that

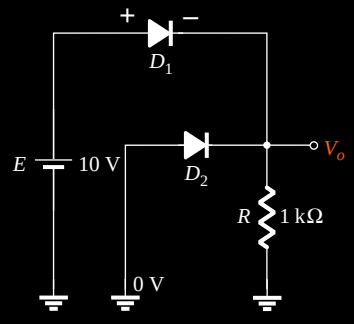


Figure 2.39 Redrawn network of Fig. 2.38.

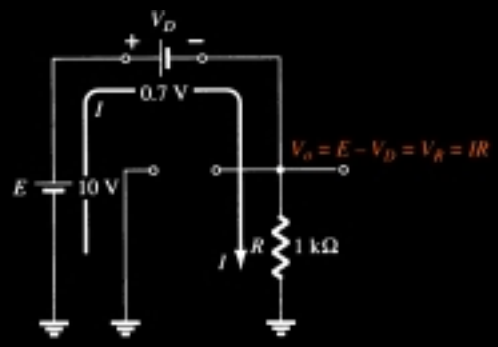


Figure 2.40 Assumed diode states for Fig. 2.38.

the gate is an OR gate. An analysis of the same network with two 10-V inputs will result in both diodes being in the "on" state and an output of 9.3 V. A 0-V input at both inputs will not provide the 0.7 V required to turn the diodes on, and the output will be a 0 due to the 0-V output level. For the network of Fig. 2.40 the current level is determined by

$$I = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

EXAMPLE 2.17

Determine the output level for the positive logic AND gate of Fig. 2.41.

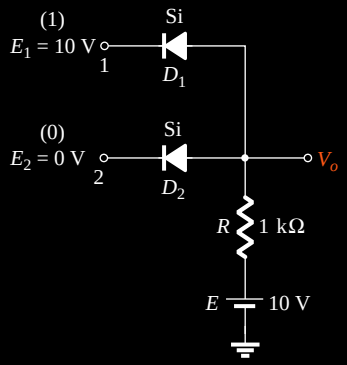


Figure 2.41 Positive logic AND gate.

Solution

Note in this case that an independent source appears in the grounded leg of the network. For reasons soon to become obvious it is chosen at the same level as the input logic level. The network is redrawn in Fig. 2.42 with our initial assumptions regarding the state of the diodes. With 10 V at the cathode side of D_1 it is assumed that D_1 is in the "off" state even though there is a 10-V source connected to the anode of D_1 through the resistor. However, recall that we mentioned in the introduction to this section that the use of the approximate model will be an aid to the analysis. For D_1, where will the 0.7 V come from if the input and source voltages are at the same level and creating opposing "pressures"? D_2 is assumed to be in the "on" state due to the low voltage at the cathode side and the availability of the 10-V source through the 1-kΩ resistor.

For the network of Fig. 2.42 the voltage at V_o is 0.7 V due to the forward-biased diode D_2. With 0.7 V at the anode of D_1 and 10 V at the cathode, D_1 is definitely in the "off" state. The current I will have the direction indicated in Fig. 2.42 and a magnitude equal to

$$I = \frac{E - V_D}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

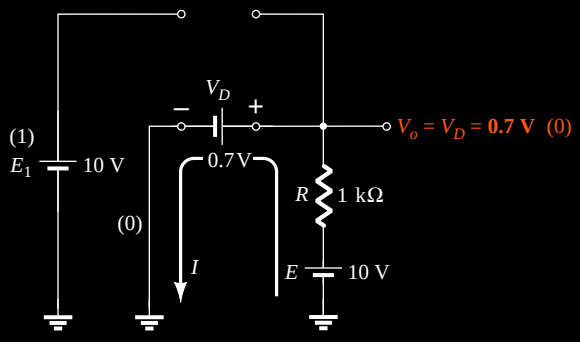


Figure 2.42 Substituting the assumed states for the diodes of Fig. 2.41.

The state of the diodes is therefore confirmed and our earlier analysis was correct. Although not 0 V as earlier defined for the 0 level, the output voltage is sufficiently small to be considered a 0 level. For the AND gate, therefore, a single input will result in a 0-level output. The remaining states of the diodes for the possibilities of two inputs and no inputs will be examined in the problems at the end of the chapter.

2.7 SINUSOIDAL INPUTS; HALF-WAVE RECTIFICATION

The diode analysis will now be expanded to include time-varying functions such as the sinusoidal waveform and the square wave. There is no question that the degree of difficulty will increase, but once a few fundamental maneuvers are understood, the analysis will be fairly direct and follow a common thread.

The simplest of networks to examine with a time-varying signal appears in Fig. 2.43. For the moment we will use the ideal model (note the absence of the Si or Ge label to denote ideal diode) to ensure that the approach is not clouded by additional mathematical complexity.

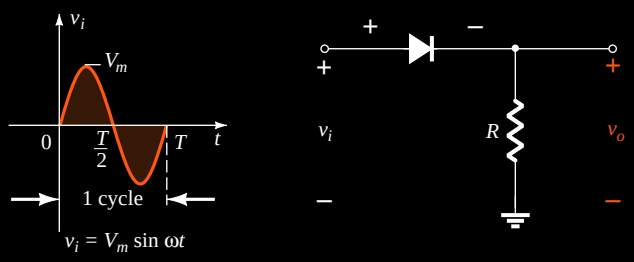


Figure 2.43 Half-wave rectifier.

Over one full cycle, defined by the period T of Fig. 2.43, the average value (the algebraic sum of the areas above and below the axis) is zero. The circuit of Fig. 2.43, called a *half-wave rectifier,* will generate a waveform v_o that will have an average value of particular, use in the ac-to-dc conversion process. When employed in the rectification process, a diode is typically referred to as a *rectifier.* Its power and current ratings are typically much higher than those of diodes employed in other applications, such as computers and communication systems.

During the interval $t = 0 \rightarrow T/2$ in Fig. 2.43 the polarity of the applied voltage v_i is such as to establish "pressure" in the direction indicated and turn on the diode with the polarity appearing above the diode. Substituting the short-circuit equivalence for the ideal diode will result in the equivalent circuit of Fig. 2.44, where it is fairly obvious that the output signal is an exact replica of the applied signal. The two terminals defining the output voltage are connected directly to the applied signal via the short-circuit equivalence of the diode.

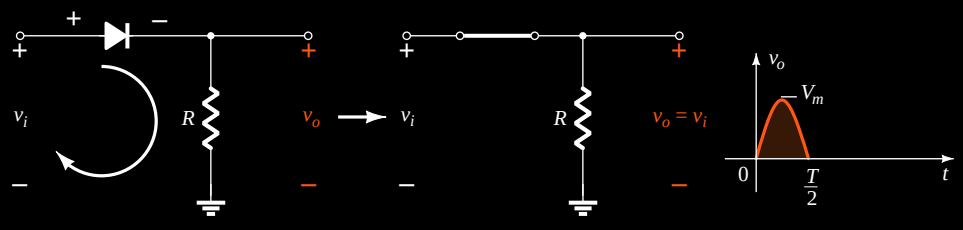


Figure 2.44 Conduction region $(0 \rightarrow T/2)$.

For the period $T/2 \rightarrow T$, the polarity of the input v_i is as shown in Fig. 2.45 and the resulting polarity across the ideal diode produces an "off" state with an open-circuit equivalent. The result is the absence of a path for charge to flow and $v_o = iR = (0)R = 0$ V for the period $T/2 \rightarrow T$. The input v_i and the output v_o were sketched together in Fig. 2.46 for comparison purposes. The output signal v_o now has a net positive area above the axis over a full period and an average value determined by

$$V_{dc} = 0.318V_m \quad \text{half-wave} \tag{2.7}$$

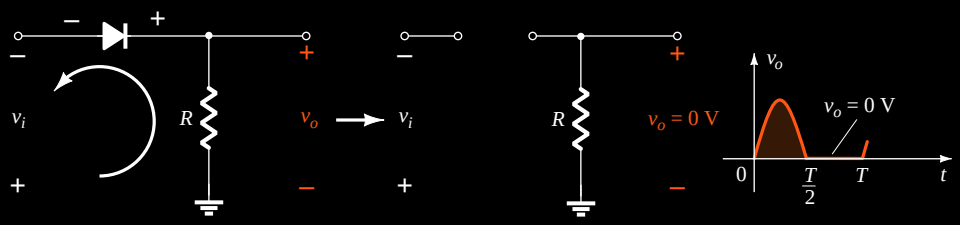


Figure 2.45 Nonconduction region ($T/2 \rightarrow T$).

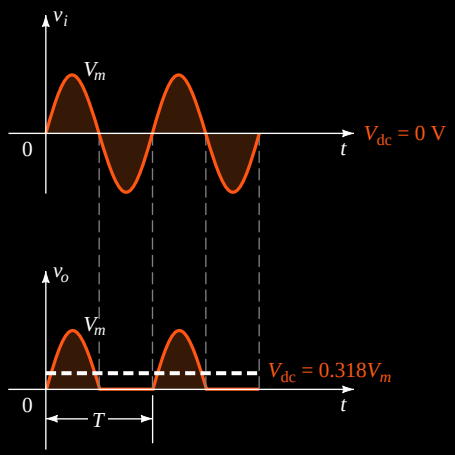


Figure 2.46 Half-wave rectified signal.

The process of removing one-half the input signal to establish a dc level is aptly called *half-wave rectification.*

The effect of using a silicon diode with $V_T = 0.7$ V is demonstrated in Fig. 2.47 for the forward-bias region. The applied signal must now be at least 0.7 V before the diode can turn "on." For levels of v_i less than 0.7 V, the diode is still in an open-circuit state and $v_o = 0$ V as shown in the same figure. When conducting, the difference between v_o and v_i is a fixed level of $V_T = 0.7$ V and $v_o = v_i - V_T$, as shown in the figure. The net effect is a reduction in area above the axis, which naturally reduces

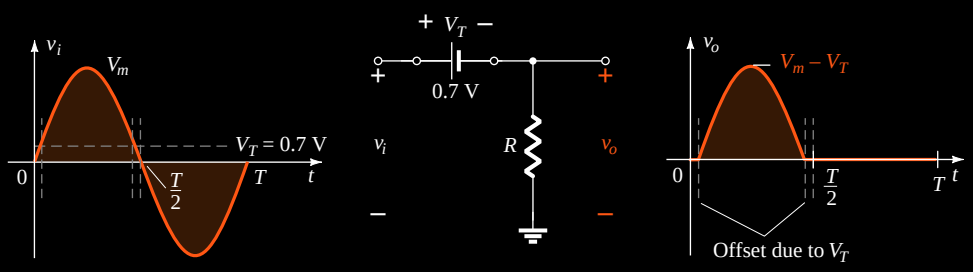


Figure 2.47 Effect of V_T on half-wave rectified signal.

the resulting dc voltage level. For situations where $V_m \gg V_T$, Eq. 2.8 can be applied to determine the average value with a relatively high level of accuracy.

$$V_{dc} \cong 0.318(V_m - V_T) \tag{2.8}$$

In fact, if V_m is sufficiently greater than V_T, Eq. 2.7 is often applied as a first approximation for V_{dc}.

EXAMPLE 2.18

(a) Sketch the output v_o and determine the dc level of the output for the network of Fig. 2.48.
(b) Repeat part (a) if the ideal diode is replaced by a silicon diode.
(c) Repeat parts (a) and (b) if V_m is increased to 200 V and compare solutions using Eqs. (2.7) and (2.8).

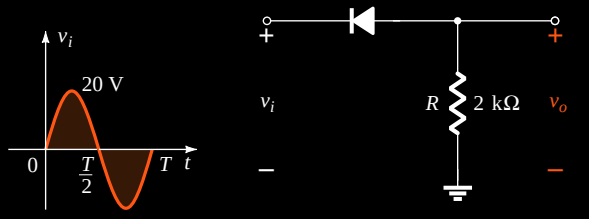


Figure 2.48 Network for Example 2.18.

Solution

(a) In this situation the diode will conduct during the negative part of the input as shown in Fig. 2.49, and v_o will appear as shown in the same figure. For the full period, the dc level is

$$V_{dc} = -0.318V_m = -0.318(20\text{ V}) = \mathbf{-6.36\text{ V}}$$

The negative sign indicates that the polarity of the output is opposite to the defined polarity of Fig. 2.48.

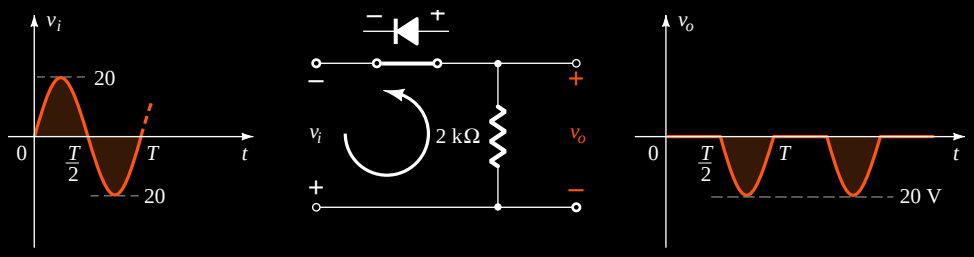


Figure 2.49 Resulting v_o for the circuit of Example 2.18.

(b) Using a silicon diode, the output has the appearance of Fig. 2.50 and

$$V_{dc} \cong -0.318(V_m - 0.7\text{ V}) = -0.318(19.3\text{ V}) \cong \mathbf{-6.14\text{ V}}$$

The resulting drop in dc level is 0.22 V or about 3.5%.

(c) Eq. (2.7): $V_{dc} = -0.318V_m = -0.318(200\text{ V}) = \mathbf{-63.6\text{ V}}$

Eq. (2.8): $V_{dc} = -0.318(V_m - V_T) = -0.318(200\text{ V} - 0.7\text{ V})$

$= -(0.318)(199.3\text{ V}) = \mathbf{-63.38\text{ V}}$

which is a difference that can certainly be ignored for most applications. For part c the offset and drop in amplitude due to V_T would not be discernible on a typical oscilloscope if the full pattern is displayed.

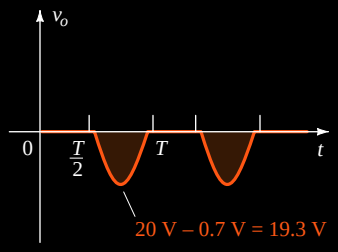


Figure 2.50 Effect of V_T on output of Fig. 2.49.

PIV (PRV)

The peak inverse voltage (PIV) [or PRV (peak reverse voltage)] rating of the diode is of primary importance in the design of rectification systems. Recall that it is the voltage rating that must not be exceeded in the reverse-bias region or the diode will enter the Zener avalanche region. The required PIV rating for the half-wave rectifier can be determined from Fig. 2.51, which displays the reverse-biased diode of Fig. 2.43 with maximum applied voltage. Applying Kirchhoff"s voltage law, it is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage. Therefore,

$$\text{PIV rating} \geqq V_m \quad \text{half-wave rectifier} \tag{2.9}$$

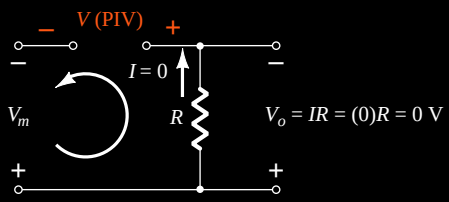


Figure 2.51 Determining the required PIV rating for the half-wave rectifier.

2.8 FULL-WAVE RECTIFICATION

Bridge Network

The dc level obtained from a sinusoidal input can be improved 100% using a process called *full-wave rectification*. The most familiar network for performing such a function appears in Fig. 2.52 with its four diodes in a *bridge* configuration. During the period $t = 0$ to $T/2$ the polarity of the input is as shown in Fig. 2.53. The resulting polarities across the ideal diodes are also shown in Fig. 2.53 to reveal that D_2 and D_3 are conducting while D_1 and D_4 are in the "off" state. The net result is the configuration of Fig. 2.54, with its indicated current and polarity across R. Since the diodes are ideal the load voltage is $v_o = v_i$, as shown in the same figure.

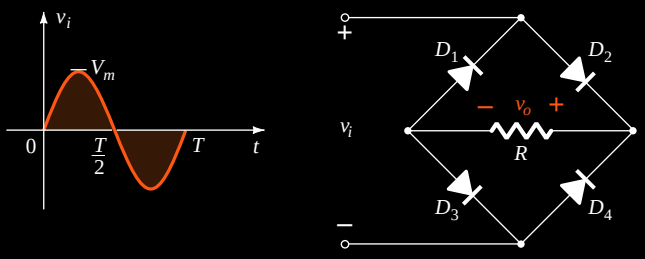


Figure 2.52 Full-wave bridge rectifier.

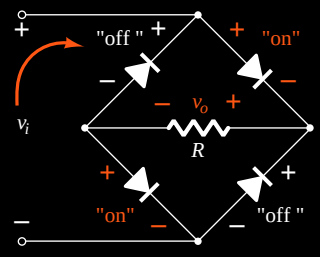


Figure 2.53 Network of Fig. 2.52 for the period $0 \rightarrow T/2$ of the input voltage v_i.

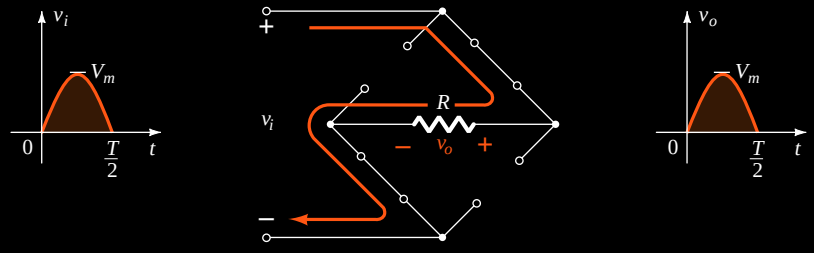


Figure 2.54 Conduction path for the positive region of v_i.

For the negative region of the input the conducting diodes are D_1 and D_4, resulting in the configuration of Fig. 2.55. The important result is that the polarity across the load resistor R is the same as in Fig. 2.53, establishing a second positive pulse, as shown in Fig. 2.55. Over one full cycle the input and output voltages will appear as shown in Fig. 2.56.

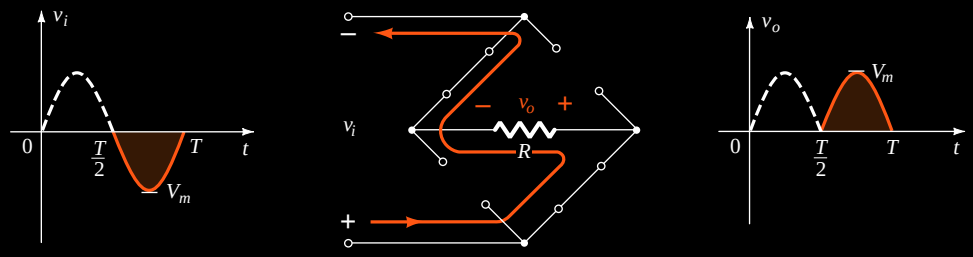


Figure 2.55 Conduction path for the negative region of v_i.

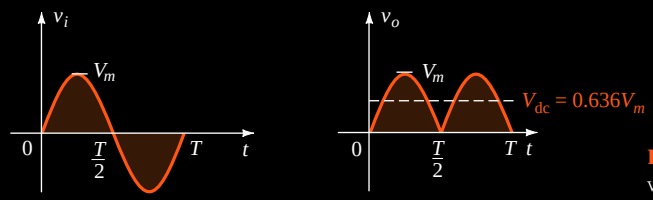


Figure 2.56 Input and output waveforms for a full-wave rectifier.

Since the area above the axis for one full cycle is now twice that obtained for a half-wave system, the dc level has also been doubled and

$$V_{dc} = 2(\text{Eq. } 2.7) = 2(0.318V_m)$$

or

$$\boxed{V_{dc} = 0.636V_m} \quad \text{full-wave} \tag{2.10}$$

If silicon rather than ideal diodes are employed as shown in Fig. 2.57, an application of Kirchhoff's voltage law around the conduction path would result in

$$v_i - V_T - v_o - V_T = 0$$

and

$$v_o = v_i - 2V_T$$

The peak value of the output voltage v_o is therefore

$$V_{o_{max}} = V_m - 2V_T$$

For situations where $V_m \gg 2V_T$, Eq. (2.11) can be applied for the average value with a relatively high level of accuracy.

$$\boxed{V_{dc} \cong 0.636(V_m - 2V_T)} \tag{2.11}$$

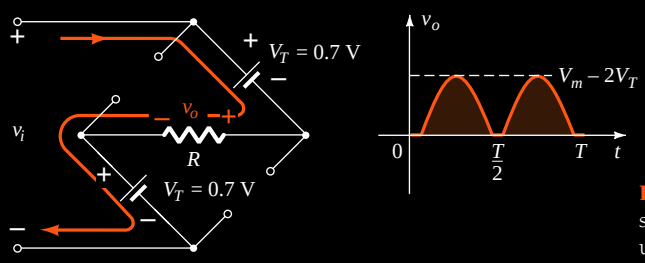


Figure 2.57 Determining $V_{o_{max}}$ for silicon diodes in the bridge configuration.

Then again, if V_m is sufficiently greater than $2V_T$, then Eq. (2.10) is often applied as a first approximation for V_{dc}.

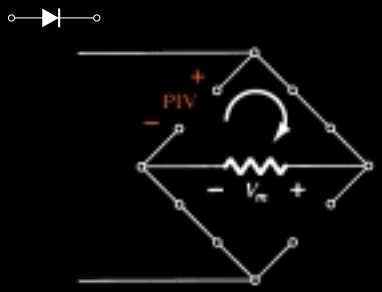


Figure 2.58 Determining the required PIV for the bridge configuration.

PIV

The required PIV of each diode (ideal) can be determined from Fig. 2.58 obtained at the peak of the positive region of the input signal. For the indicated loop the maximum voltage across R is V_m and the PIV rating is defined by

$$\text{PIV} \geqq V_m \quad \text{full-wave bridge rectifier} \tag{2.12}$$

Center-Tapped Transformer

A second popular full-wave rectifier appears in Fig. 2.59 with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer. During the positive portion of v_i applied to the primary of the transformer, the network will appear as shown in Fig. 2.60. D_1 assumes the short-circuit equivalent and D_2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions. The output voltage appears as shown in Fig. 2.60.

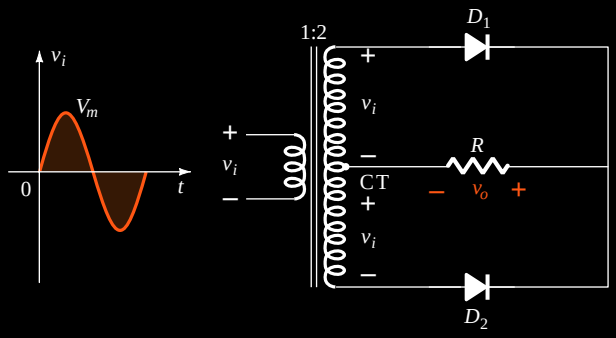


Figure 2.59 Center-tapped transformer full-wave rectifier.

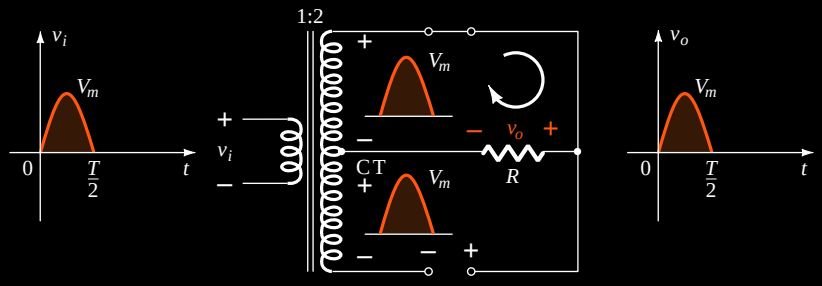


Figure 2.60 Network conditions for the positive region of v_i.

During the negative portion of the input the network appears as shown in Fig. 2.61, reversing the roles of the diodes but maintaining the same polarity for the volt-

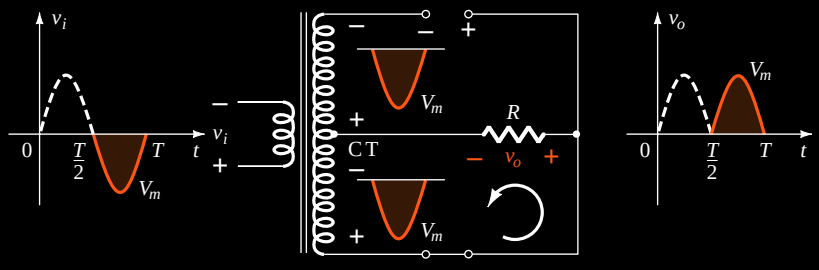


Figure 2.61 Network conditions for the negative region of v_i.

age across the load resistor R. The net effect is the same output as that appearing in Fig. 2.56 with the same dc levels.

PIV

The network of Fig. 2.62 will help us determine the net PIV for each diode for this full-wave rectifier. Inserting the maximum voltage for the secondary voltage and V_m as established by the adjoining loop will result in

$$\text{PIV} = V_{\text{secondary}} + V_R$$
$$= V_m + V_m$$

and

$$\boxed{\text{PIV} \geqq 2V_m} \quad \text{CT transformer, full-wave rectifier} \tag{2.13}$$

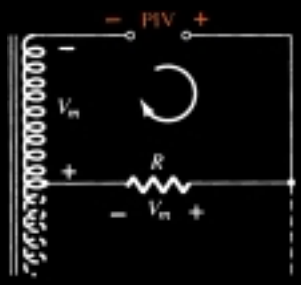


Figure 2.62 Determining the PIV level for the diodes of the CT transformer full-wave rectifier.

EXAMPLE 2.19

Determine the output waveform for the network of Fig. 2.63 and calculate the output dc level and the required PIV of each diode.

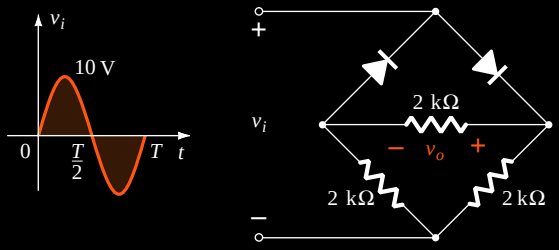


Figure 2.63 Bridge network for Example 2.19.

Solution

The network will appear as shown in Fig. 2.64 for the positive region of the input voltage. Redrawing the network will result in the configuration of Fig. 2.65, where $v_o = \frac{1}{2}v_i$ or $V_{o_{\max}} = \frac{1}{2}V_{i_{\max}} = \frac{1}{2}(10\text{ V}) = 5\text{ V}$, as shown in Fig. 2.65. For the negative part of the input the roles of the diodes will be interchanged and v_o will appear as shown in Fig. 2.66.

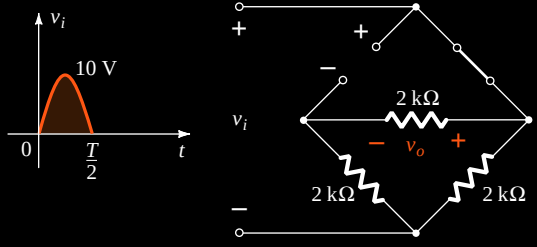


Figure 2.64 Network of Fig. 2.63 for the positive region of v_i.

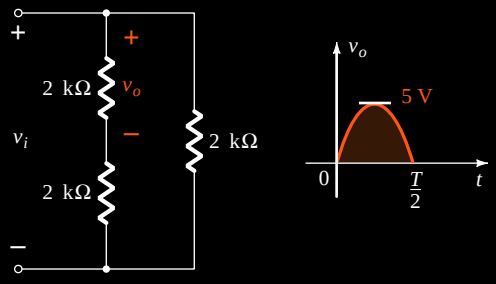


Figure 2.65 Redrawn network of Fig. 2.64.

The effect of removing two diodes from the bridge configuration was therefore to reduce the available dc level to the following:

$$V_{\text{dc}} = 0.636(5\text{ V}) = \mathbf{3.18\text{ V}}$$

or that available from a half-wave rectifier with the same input. However, the PIV as determined from Fig. 2.58 is equal to the maximum voltage across R, which is 5 V or half of that required for a half-wave rectifier with the same input.

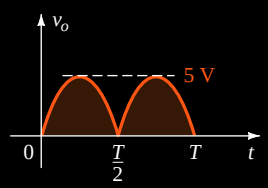


Figure 2.66 Resulting output for Example 2.19.

2.9 CLIPPERS

There are a variety of diode networks called *clippers* that have the ability to "clip" off a portion of the input signal without distorting the remaining part of the alternating waveform. The half-wave rectifier of Section 2.7 is an example of the simplest form of diode clipper—one resistor and diode. Depending on the orientation of the diode, the positive or negative region of the input signal is "clipped" off.

There are two general categories of clippers: *series* and *parallel*. The series configuration is defined as one where the diode is in series with the load, while the parallel variety has the diode in a branch parallel to the load.

Series

The response of the series configuration of Fig. 2.67a to a variety of alternating waveforms is provided in Fig. 2.67b. Although first introduced as a half-wave rectifier (for sinusoidal waveforms), there are no boundaries on the type of signals that can be applied to a clipper. The addition of a dc supply such as shown in Fig. 2.68 can have a pronounced effect on the output of a clipper. Our initial discussion will be limited to ideal diodes, with the effect of V_T reserved for a concluding example.

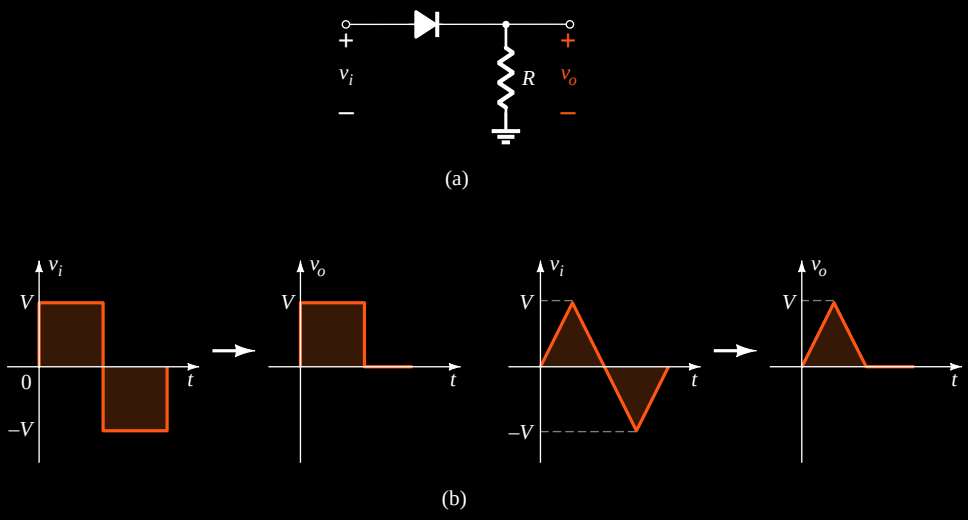


Figure 2.67 Series clipper.

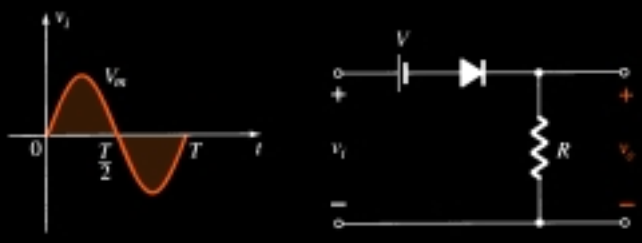


Figure 2.68 Series clipper with a dc supply.

There is no general procedure for analyzing networks such as the type in Fig. 2.68, but there are a few thoughts to keep in mind as you work toward a solution.

1. *Make a mental sketch of the response of the network based on the direction of the diode and the applied voltage levels.*

For the network of Fig. 2.68, the direction of the diode suggests that the signal v_i must be positive to turn it on. The dc supply further requires that the voltage v_i be greater than V volts to turn the diode on. The negative region of the input signal is

"pressuring" the diode into the "off" state, supported further by the dc supply. In general, therefore, we can be quite sure that the diode is an open circuit ("off" state) for the negative region of the input signal.

2. *Determine the applied voltage (transition voltage) that will cause a change in state for the diode.*

For the ideal diode the transition between states will occur at the point on the characteristics where $v_d = 0$ V and $i_d = 0$ A. Applying the condition $i_d = 0$ at $v_d = 0$ to the network of Fig. 2.68 will result in the configuration of Fig. 2.69, where it is recognized that the level of v_i that will cause a transition in state is

$$v_i = V \tag{2.14}$$

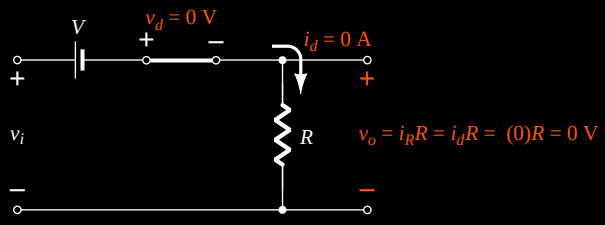


Figure 2.69 Determining the transition level for the circuit of Fig. 2.68.

For an input voltage greater than V volts the diode is in the short-circuit state, while for input voltages less than V volts it is in the open-circuit or "off" state.

3. *Be continually aware of the defined terminals and polarity of v_o.*

When the diode is in the short-circuit state, such as shown in Fig. 2.70, the output voltage v_o can be determined by applying Kirchhoff's voltage law in the clockwise direction:

$$v_i - V - v_o = 0 \text{ (CW direction)}$$

and

$$v_o = v_i - V \tag{2.15}$$

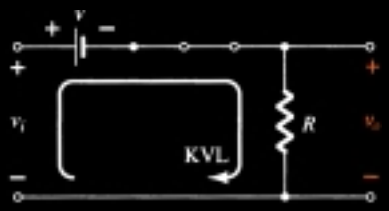


Figure 2.70 Determining v_o.

4. *It can be helpful to sketch the input signal above the output and determine the output at instantaneous values of the input.*

It is then possible that the output voltage can be sketched from the resulting data points of v_o as demonstrated in Fig. 2.71. Keep in mind that at an instantaneous value of v_i the input can be treated as a dc supply of that value and the corresponding dc value (the instantaneous value) of the output determined. For instance, at $v_i = V_m$ for the network of Fig. 2.68, the network to be analyzed appears in Fig. 2.72. For $V_m > V$ the diode is in the short-circuit state and $v_o = V_m - V$, as shown in Fig. 2.71.

At $v_i = V$ the diodes change state; at $v_i = -V_m$, $v_o = 0$ V; and the complete curve for v_o can be sketched as shown in Fig. 2.73.

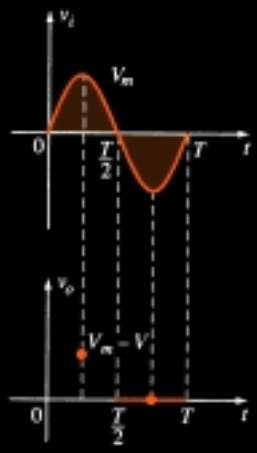


Figure 2.71 Determining levels of v_o.

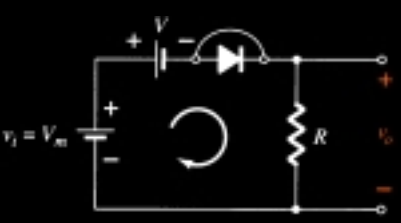


Figure 2.72 Determining v_o when $v_i = V_m$.

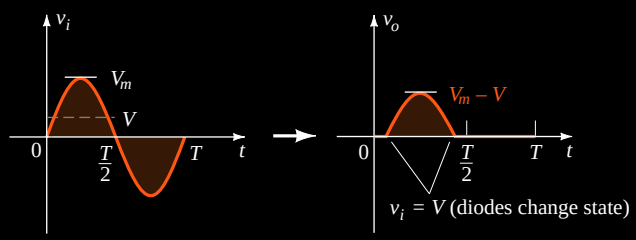


Figure 2.73 Sketching v_o.

EXAMPLE 2.20

Determine the output waveform for the network of Fig. 2.74.

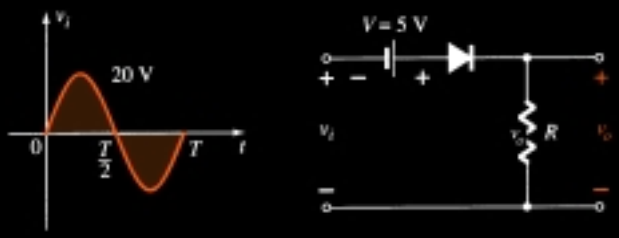


Figure 2.74 Series clipper for Example 2.20.

Solution

Past experience suggests that the diode will be in the "on" state for the positive region of v_i—especially when we note the aiding effect of $V = 5$ V. The network will then appear as shown in Fig. 2.75 and $v_o = v_i + 5$ V. Substituting $i_d = 0$ at $v_d = 0$ for the transition levels, we obtain the network of Fig. 2.76 and $v_i = -5$ V.

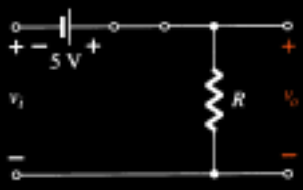


Figure 2.75 v_o with diode in the "on" state.

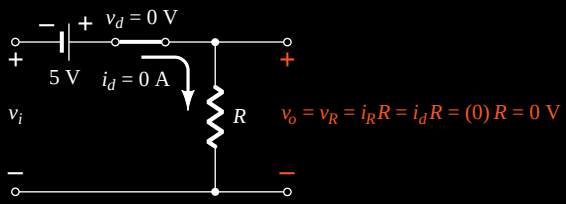


Figure 2.76 Determining the transition level for the clipper of Fig. 2.74.

For v_i more negative than -5 V the diode will enter its open-circuit state, while for voltages more positive than -5 V the diode is in the short-circuit state. The input and output voltages appear in Fig. 2.77.

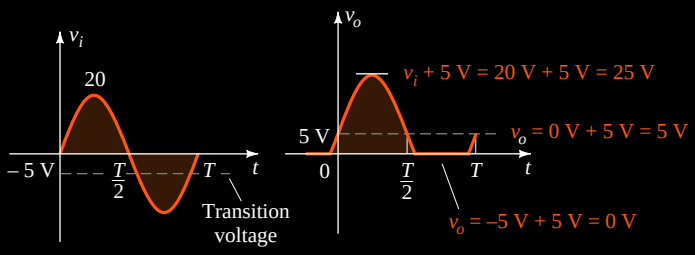


Figure 2.77 Sketching v_o for Example 2.20.

The analysis of clipper networks with square-wave inputs is actually easier to analyze than with sinusoidal inputs because only two levels have to be considered. In other words, the network can be analyzed as if it had two dc level inputs with the resulting output v_o plotted in the proper time frame.

Repeat Example 2.20 for the square-wave input of Fig. 2.78. *EXAMPLE 2.21*

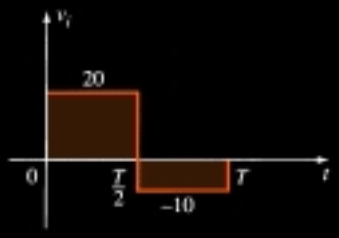


Figure 2.78 Applied signal for Example 2.21.

Solution

For $v_i = 20$ V $(0 \rightarrow T/2)$ the network of Fig. 2.79 will result. The diode is in the short-circuit state and $v_o = 20$ V + 5 V = 25 V. For $v_i = -10$ V the network of Fig. 2.80 will result, placing the diode in the "off" state and $v_o = i_R R = (0)R = 0$ V. The resulting output voltage appears in Fig. 2.81.

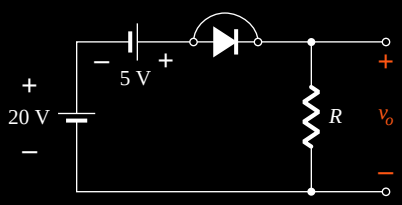


Figure 2.79 v_o at $v_i = +20$ V.

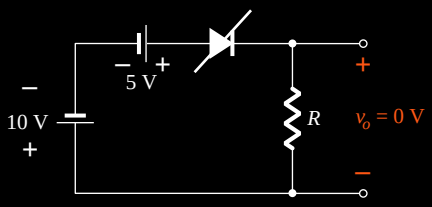


Figure 2.80 v_o at $v_i = -10$ V.

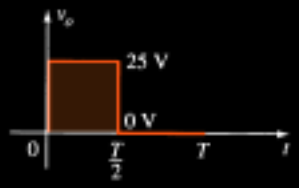


Figure 2.81 Sketching v_o for Example 2.21.

Note in Example 2.21 that the clipper not only clipped off 5 V from the total swing but raised the dc level of the signal by 5 V.

Parallel

The network of Fig. 2.82 is the simplest of parallel diode configurations with the output for the same inputs of Fig. 2.67. The analysis of parallel configurations is very similar to that applied to series configurations, as demonstrated in the next example.

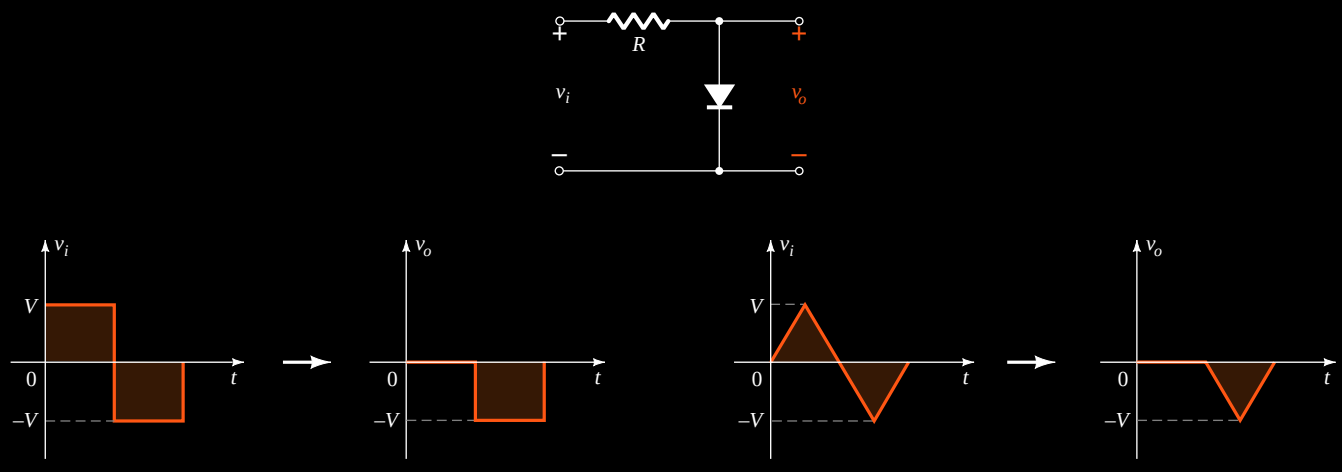


Figure 2.82 Response to a parallel clipper.

EXAMPLE 2.2

Determine v_o for the network of Fig. 2.83.

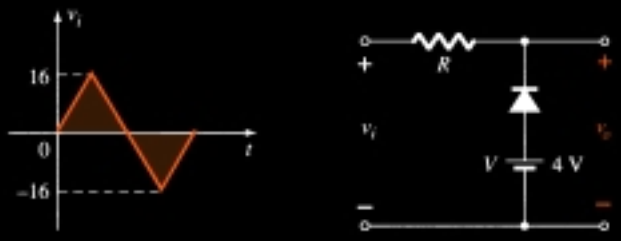


Figure 2.83 Example 2.22.

Solution

The polarity of the dc supply and the direction of the diode strongly suggest that the diode will be in the "on" state for the negative region of the input signal. For this region the network will appear as shown in Fig. 2.84, where the defined terminals for v_o require that $v_o = V = 4$ V.

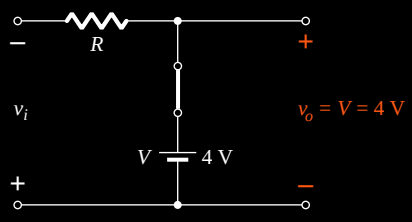


Figure 2.84 v_o for the negative region of v_i.

The transition state can be determined from Fig. 2.85, where the condition $i_d = 0$ A at $v_d = 0$ V has been imposed. The result is v_i (transition) $= V = 4$ V.

Since the dc supply is obviously "pressuring" the diode to stay in the short-circuit state, the input voltage must be greater than 4 V for the diode to be in the "off" state. Any input voltage less than 4 V will result in a short-circuited diode.

For the open-circuit state the network will appear as shown in Fig. 2.86, where $v_o = v_i$. Completing the sketch of v_o results in the waveform of Fig. 2.87.

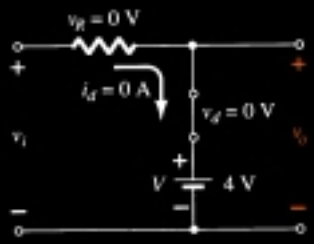


Figure 2.85 Determining the transition level for Example 2.22.

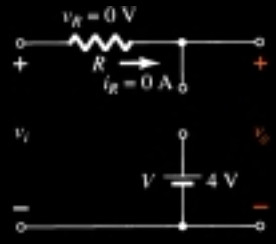


Figure 2.86 Determining v_o for the open state of the diode.

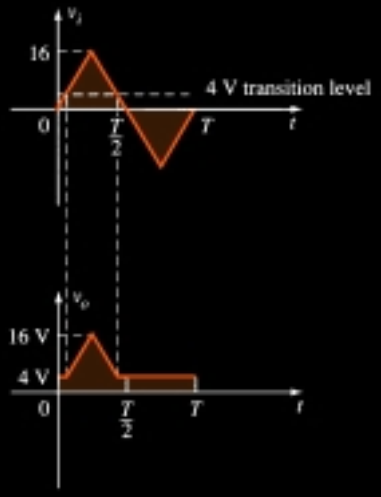


Figure 2.87 Sketching v_o for Example 2.22.

To examine the effects of V_T on the output voltage, the next example will specify a silicon diode rather than an ideal diode equivalent.

Repeat Example 2.22 using a silicon diode with $V_T = 0.7$ V. *EXAMPLE 2.23*

Solution

The transition voltage can first be determined by applying the condition $i_d = 0$ A at $v_d = V_D = 0.7$ V and obtaining the network of Fig. 2.88. Applying Kirchhoff's voltage law around the output loop in the clockwise direction, we find that

$$v_i + V_T - V = 0$$

and

$$v_i = V - V_T = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3 \text{ V}}$$

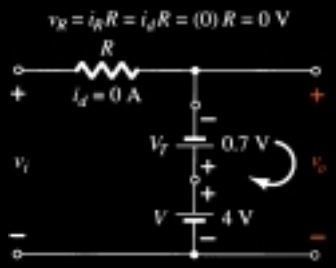


Figure 2.88 Determining the transition level for the network of Fig. 2.83.

For input voltages greater than 3.3 V, the diode will be an open circuit and $v_o = v_i$. For input voltages of less than 3.3 V, the diode will be in the "on" state and the network of Fig. 2.89 results, where

$$v_o = 4 \text{ V} - 0.7 \text{ V} = \mathbf{3.3 \text{ V}}$$

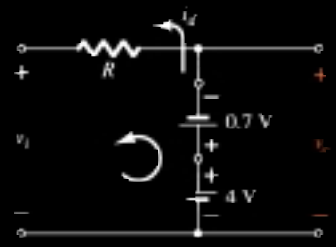


Figure 2.89 Determining v_o for the diode of Fig. 2.83 in the "on" state.

The resulting output waveform appears in Fig. 2.90. Note that the only effect of V_T was to drop the transition level to 3.3 from 4 V.

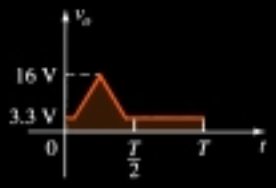


Figure 2.90 Sketching v_o for Example 2.23.

There is no question that including the effects of V_T will complicate the analysis somewhat, but once the analysis is understood with the ideal diode, the procedure, including the effects of V_T, will not be that difficult.

Summary

A variety of series and parallel clippers with the resulting output for the sinusoidal input are provided in Fig. 2.91. In particular, note the response of the last configuration, with its ability to clip off a positive and a negative section as determined by the magnitude of the dc supplies.

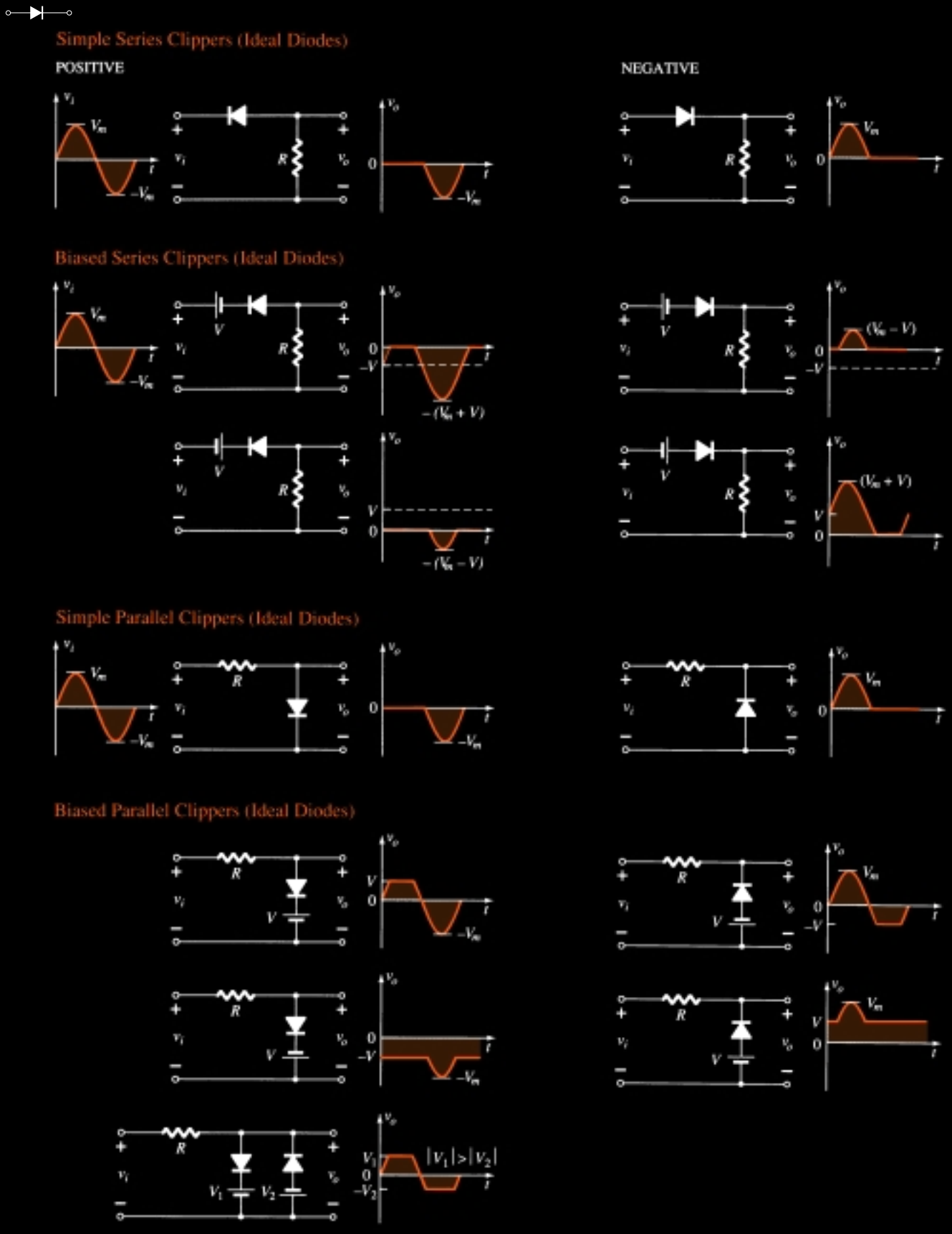


Figure 2.91 Clipping circuits.

2.10 CLAMPERS

The *clamping* network is one that will "clamp" a signal to a different dc level. The network must have a capacitor, a diode, and a resistive element, but it can also employ an independent dc supply to introduce an additional shift. The magnitude of R and C must be chosen such that the time constant $\tau = RC$ is large enough to ensure that the voltage across the capacitor does not discharge significantly during the interval the diode is nonconducting. Throughout the analysis we will assume that for all practical purposes the capacitor will fully charge or discharge in five time constants.

The network of Fig. 2.92 will clamp the input signal to the zero level (for ideal diodes). The resistor R can be the load resistor or a parallel combination of the load resistor and a resistor designed to provide the desired level of R.

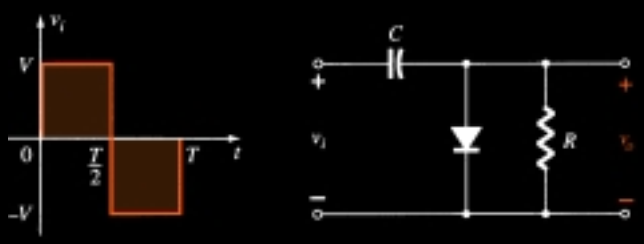


Figure 2.92 Clamper.

During the interval $0 \rightarrow T/2$ the network will appear as shown in Fig. 2.93, with the diode in the "on" state effectively "shorting out" the effect of the resistor R. The resulting RC time constant is so small (R determined by the inherent resistance of the network) that the capacitor will charge to V volts very quickly. During this interval the output voltage is directly across the short circuit and $v_o = 0$ V.

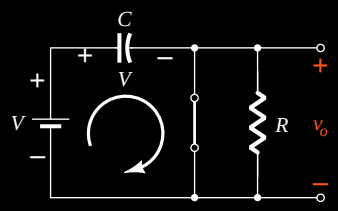


Figure 2.93 Diode "on" and the capacitor charging to V volts.

When the input switches to the $-V$ state, the network will appear as shown in Fig. 2.94, with the open-circuit equivalent for the diode determined by the applied signal and stored voltage across the capacitor—both "pressuring" current through the diode from cathode to anode. Now that R is back in the network the time constant determined by the RC product is sufficiently large to establish a discharge period 5τ much greater than the period $T/2 \rightarrow T$, and it can be assumed on an approximate basis that the capacitor holds onto all its charge and, therefore, voltage (since $V = Q/C$) during this period.

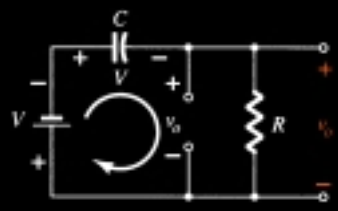


Figure 2.94 Determining v_o with the diode "off."

Since v_o is in parallel with the diode and resistor, it can also be drawn in the alternative position shown in Fig. 2.94. Applying Kirchhoff's voltage law around the input loop will result in

$$-V - V - v_o = 0$$

and

$$v_o = -2V$$

The negative sign resulting from the fact that the polarity of $2V$ is opposite to the polarity defined for v_o. The resulting output waveform appears in Fig. 2.95 with the input signal. The output signal is clamped to 0 V for the interval 0 to $T/2$ but maintains the same total swing ($2V$) as the input.

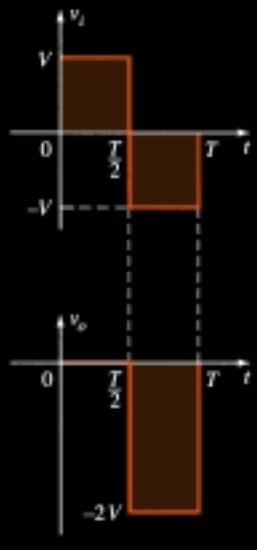


Figure 2.95 Sketching v_o for the network of Fig. 2.92.

For a clamping network:

The total swing of the output is equal to the total swing of the input signal.

This fact is an excellent checking tool for the result obtained.

In general, the following steps may be helpful when analyzing clamping networks:

1. *Start the analysis of clamping networks by considering that part of the input signal that will forward bias the diode.*

The statement above may require skipping an interval of the input signal (as demonstrated in an example to follow), but the analysis will not be extended by an unnecessary measure of investigation.

2. *During the period that the diode is in the "on" state, assume that the capacitor will charge up instantaneously to a voltage level determined by the network.*
3. *Assume that during the period when the diode is in the "off" state the capacitor will hold on to its established voltage level.*
4. *Throughout the analysis maintain a continual awareness of the location and reference polarity for v_o to ensure that the proper levels for v_o are obtained.*
5. *Keep in mind the general rule that the total swing of the total output must match the swing of the input signal.*

EXAMPLE 2.24

Determine v_o for the network of Fig. 2.96 for the input indicated.

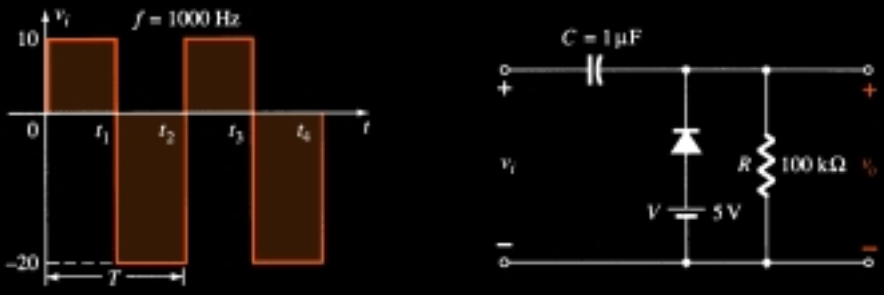


Figure 2.96 Applied signal and network for Example 2.24.

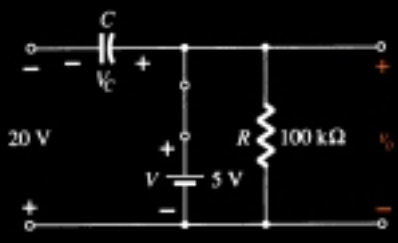


Figure 2.97 Determining v_o and V_C with the diode in the "on" state.

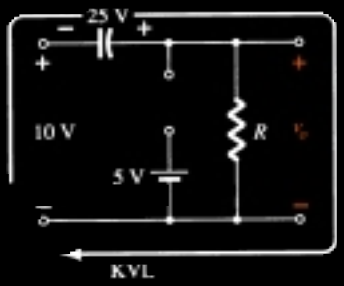


Figure 2.98 Determining v_o with the diode in the "off" state.

Solution

Note that the frequency is 1000 Hz, resulting in a period of 1 ms and an interval of 0.5 ms between levels. The analysis will begin with the period $t_1 \rightarrow t_2$ of the input signal since the diode is in its short-circuit state as recommended by comment 1. For this interval the network will appear as shown in Fig. 2.97. The output is across R, but it is also directly across the 5-V battery if you follow the direct connection between the defined terminals for v_o and the battery terminals. The result is $v_o = 5$ V for this interval. Applying Kirchhoff's voltage law around the input loop will result in

$$-20\text{ V} + V_C - 5\text{ V} = 0$$

and

$$V_C = 25\text{ V}$$

The capacitor will therefore charge up to 25 V, as stated in comment 2. In this case the resistor R is not shorted out by the diode but a Thévenin equivalent circuit of that portion of the network which includes the battery and the resistor will result in $R_{Th} = 0\ \Omega$ with $E_{Th} = V = 5$ V. For the period $t_2 \rightarrow t_3$ the network will appear as shown in Fig. 2.98.

The open-circuit equivalent for the diode will remove the 5-V battery from having any effect on v_o, and applying Kirchhoff's voltage law around the outside loop of the network will result in

$$+10\text{ V} + 25\text{ V} - v_o = 0$$

and

$$v_o = 35\text{ V}$$

The time constant of the discharging network of Fig. 2.98 is determined by the product RC and has the magnitude

$$\tau = RC = (100\ \text{k}\Omega)(0.1\ \mu\text{F}) = 0.01\ \text{s} = 10\ \text{ms}$$

The total discharge time is therefore $5\tau = 5(10\ \text{ms}) = 50\ \text{ms}$.

Since the interval $t_2 \rightarrow t_3$ will only last for 0.5 ms, it is certainly a good approximation that the capacitor will hold its voltage during the discharge period between pulses of the input signal. The resulting output appears in Fig. 2.99 with the input signal. Note that the output swing of 30 V matches the input swing as noted in step 5.

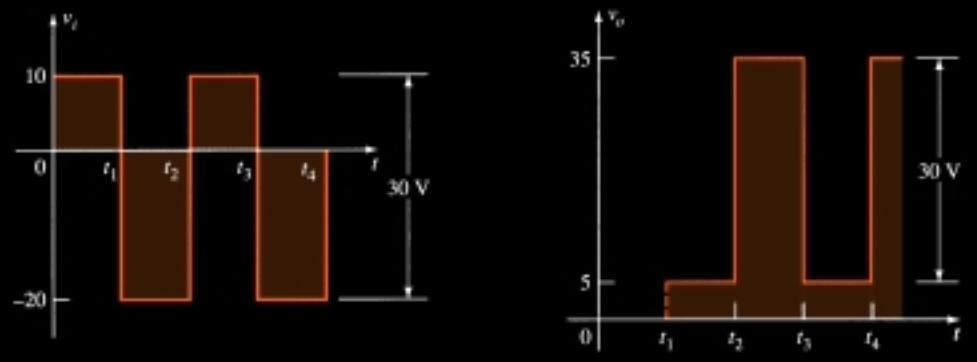


Figure 2.99 v_i and v_o for the clamper of Fig. 2.96.

EXAMPLE 2.25

Repeat Example 2.24 using a silicon diode with $V_T = 0.7$ V.

Solution

For the short-circuit state the network now takes on the appearance of Fig. 2.100 and v_o can be determined by Kirchhoff's voltage law in the output section.

$$+5\ \text{V} - 0.7\ \text{V} - v_o = 0$$

and

$$v_o = 5\ \text{V} - 0.7\ \text{V} = 4.3\ \text{V}$$

For the input section Kirchhoff's voltage law will result in

$$-20\ \text{V} + V_C + 0.7\ \text{V} - 5\ \text{V} = 0$$

and

$$V_C = 25\ \text{V} - 0.7\ \text{V} = 24.3\ \text{V}$$

For the period $t_2 \rightarrow t_3$ the network will now appear as in Fig. 2.101, with the only change being the voltage across the capacitor. Applying Kirchhoff's voltage law yields

$$+10\ \text{V} + 24.3\ \text{V} - v_o = 0$$

and

$$v_o = 34.3\ \text{V}$$

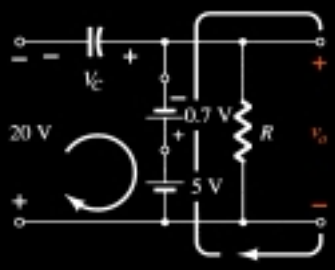


Figure 2.100 Determining v_o and V_C with the diode in the "on" state.

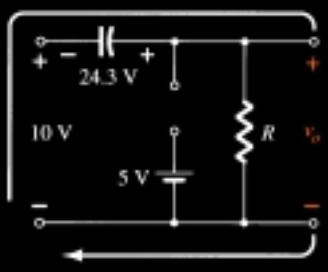


Figure 2.101 Determining v_o with the diode in the open state.

The resulting output appears in Fig. 2.102, verifying the statement that the input and output swings are the same.

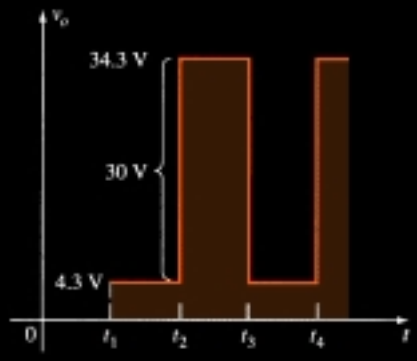


Figure 2.102 Sketching v_o for the clamper of Fig. 2.96 with a silicon diode.

A number of clamping circuits and their effect on the input signal are shown in Fig. 2.103. Although all the waveforms appearing in Fig. 2.103 are square waves, clamping networks work equally well for sinusoidal signals. In fact, one approach to the analysis of clamping networks with sinusoidal inputs is to replace the sinusoidal signal by a square wave of the same peak values. The resulting output will then form an envelope for the sinusoidal response as shown in Fig. 2.104 for a network appearing in the bottom right of Fig. 2.103.

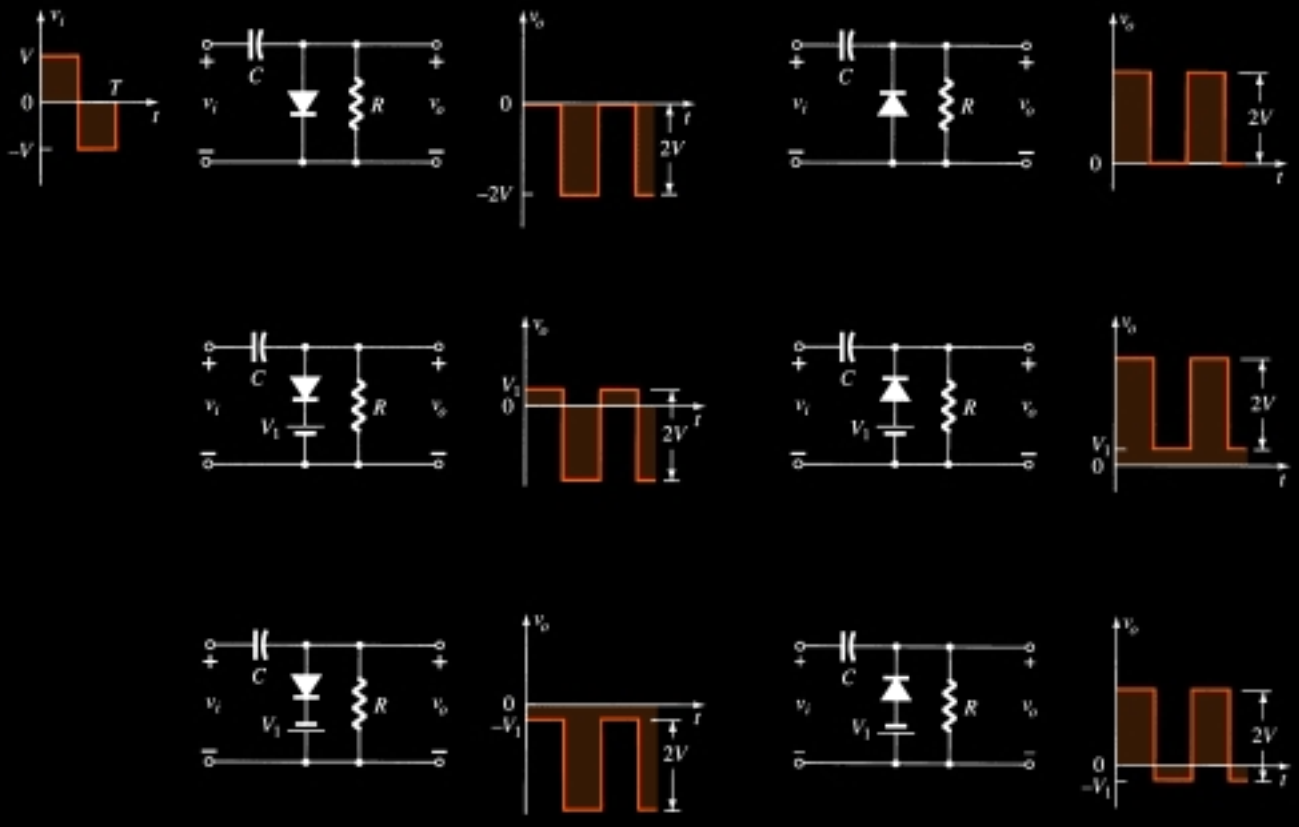


Figure 2.103 Clamping circuits with ideal diodes ($5\tau = 5RC \gg T/2$).

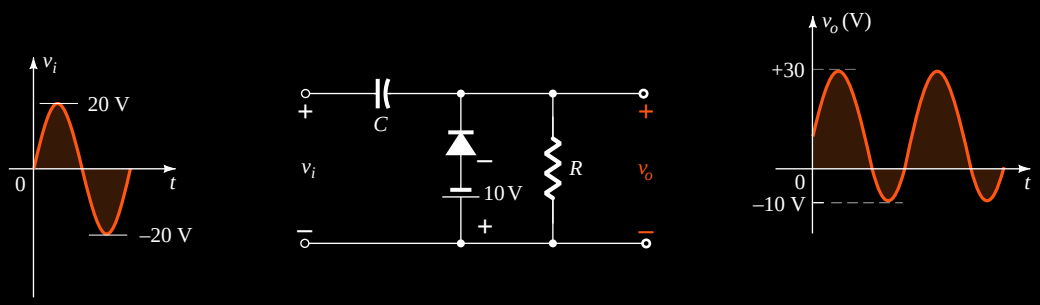


Figure 2.104 Clamping network with a sinusoidal input.

2.11 ZENER DIODES

The analysis of networks employing Zener diodes is quite similar to that applied to the analysis of semiconductor diodes in previous sections. First the state of the diode must be determined followed by a substitution of the appropriate model and a determination of the other unknown quantities of the network. Unless otherwise specified, the Zener model to be employed for the "on" state will be as shown in Fig. 2.105a. For the "off" state as defined by a voltage less than V_Z but greater than 0 V with the polarity indicated in Fig. 2.105b, the Zener equivalent is the open circuit that appears in the same figure.

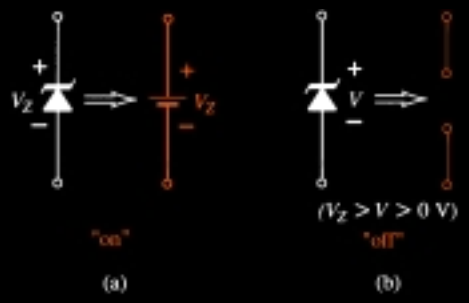


Figure 2.105 Zener diode equivalents for the (a) "on" and (b) "off" states.

V_i and R

The simplest of Zener diode networks appears in Fig. 2.106. The applied dc voltage is fixed, as is the load resistor. The analysis can fundamentally be broken down into two steps.

1. *Determine the state of the Zener diode by removing it from the network and calculating the voltage across the resulting open circuit.*

Applying step 1 to the network of Fig. 2.106 will result in the network of Fig. 2.107, where an application of the voltage divider rule will result in

$$V = V_L = \frac{R_L V_i}{R + R_L} \tag{2.16}$$

If $V \geq V_Z$, the Zener diode is "on" and the equivalent model of Fig. 2.105a can be substituted. If $V < V_Z$, the diode is "off" and the open-circuit equivalence of Fig. 2.105b is substituted.

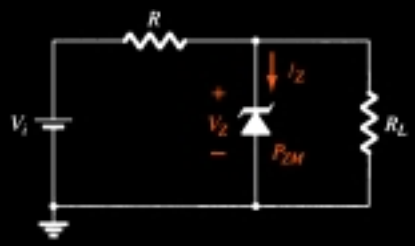


Figure 2.106 Basic Zener regulator.

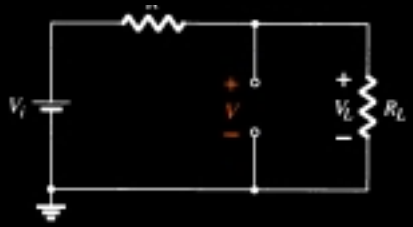


Figure 2.107 Determining the state of the Zener diode.

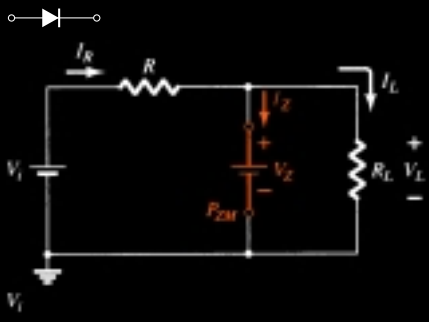


Figure 2.108 Substituting the Zener equivalent for the "on" situation.

2. Substitute the appropriate equivalent circuit and solve for the desired unknowns.

For the network of Fig. 2.106, the "on" state will result in the equivalent network of Fig. 2.108. Since voltages across parallel elements must be the same, we find that

$$V_L = V_Z \tag{2.17}$$

The Zener diode current must be determined by an application of Kirchhoff's current law. That is,

$$I_R = I_Z + I_L$$

and

$$I_Z = I_R - I_L \tag{2.18}$$

where

$$I_L = \frac{V_L}{R_L} \quad \text{and} \quad I_R = \frac{V_R}{R} = \frac{V_i - V_L}{R}$$

The power dissipated by the Zener diode is determined by

$$P_Z = V_Z I_Z \tag{2.19}$$

which must be less than the P_{ZM} specified for the device.

Before continuing, it is particularly important to realize that the first step was employed only to determine the *state of the Zener diode*. If the Zener diode is in the "on" state, the voltage across the diode is not V volts. When the system is turned on, the Zener diode will turn "on" as soon as the voltage across the Zener diode is V_Z volts. It will then "lock in" at this level and never reach the higher level of V volts.

Zener diodes are most frequently used in *regulator* networks or as a *reference* voltage. Figure 2.106 is a simple regulator designed to maintain a fixed voltage across the load R_L. For values of applied voltage greater than required to turn the Zener diode "on," the voltage across the load will be maintained at V_Z volts. If the Zener diode is employed as a reference voltage, it will provide a level for comparison against other voltages.

EXAMPLE 2.26

(a) For the Zener diode network of Fig. 2.109, determine V_L, V_R, I_Z, and P_Z.
(b) Repeat part (a) with $R_L = 3\ \text{k}\Omega$.

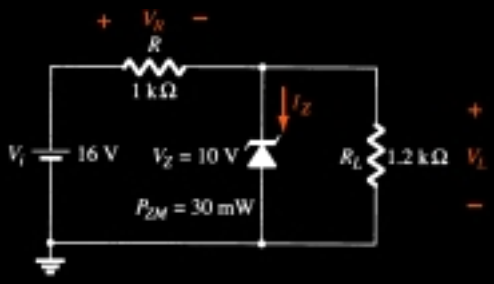


Figure 2.109 Zener diode regulator for Example 2.26.

Solution

(a) Following the suggested procedure the network is redrawn as shown in Fig. 2.110. Applying Eq. (2.16) gives

$$V = \frac{R_L V_i}{R + R_L} = \frac{1.2\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 1.2\ \text{k}\Omega} = 8.73\ \text{V}$$

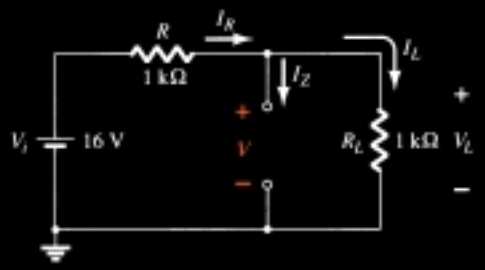


Figure 2.110 Determining V for the regulator of Fig. 2.109.

Since $V = 8.73$ V is less than $V_Z = 10$ V, the diode is in the "off" state as shown on the characteristics of Fig. 2.111. Substituting the open-circuit equivalent will result in the same network as in Fig. 2.110, where we find that

$$V_L = V = \mathbf{8.73\ V}$$

$$V_R = V_i - V_L = 16\ V - 8.73\ \text{V} = \mathbf{7.27\ V}$$

$$I_Z = \mathbf{0\ A}$$

and

$$P_Z = V_Z I_Z = V_Z(0\ \text{A}) = \mathbf{0\ W}$$

(b) Applying Eq. (2.16) will now result in

$$V = \frac{R_L V_i}{R + R_L} = \frac{3\ \text{k}\Omega(16\ \text{V})}{1\ \text{k}\Omega + 3\ \text{k}\Omega} = 12\ \text{V}$$

Since $V = 12$ V is greater than $V_Z = 10$ V, the diode is in the "on" state and the network of Fig. 2.112 will result. Applying Eq. (2.17) yields

$$V_L = V_Z = \mathbf{10\ V}$$

and

$$V_R = V_i - V_L = 16\ \text{V} - 10\ \text{V} = \mathbf{6\ V}$$

with

$$I_L = \frac{V_L}{R_L} = \frac{10\ \text{V}}{3\ \text{k}\Omega} = 3.33\ \text{mA}$$

and

$$I_R = \frac{V_R}{R} = \frac{6\ \text{V}}{1\ \text{k}\Omega} = 6\ \text{mA}$$

so that

$$I_Z = I_R - I_L\ [\text{Eq. (2.18)}]$$

$$= 6\ \text{mA} - 3.33\ \text{mA}$$

$$= \mathbf{2.67\ mA}$$

The power dissipated,

$$P_Z = V_Z I_Z = (10\ \text{V})(2.67\ \text{mA}) = \mathbf{26.7\ mW}$$

which is less than the specified $P_{ZM} = 30$ mW.

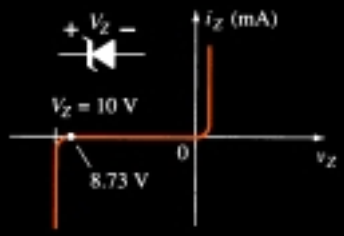


Figure 2.111 Resulting operating point for the network of Fig. 2.109.

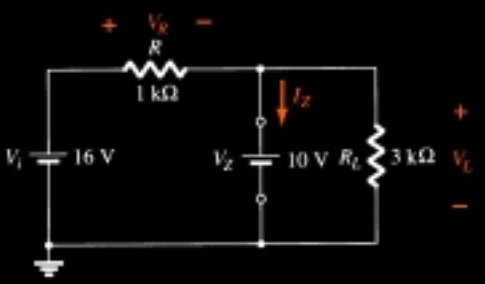


Figure 2.112 Network of Fig. 2.109 in the "on" state.

Fixed V_i, Variable R_L

Due to the offset voltage V_Z, there is a specific range of resistor values (and therefore load current) which will ensure that the Zener is in the "on" state. Too small a load resistance R_L will result in a voltage V_L across the load resistor less than V_Z, and the Zener device will be in the "off" state.

To determine the minimum load resistance of Fig. 2.106 that will turn the Zener diode on, simply calculate the value of R_L that will result in a load voltage $V_L = V_Z$. That is,

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

Solving for R_L, we have

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} \tag{2.20}$$

Any load resistance value greater than the R_L obtained from Eq. (2.20) will ensure that the Zener diode is in the "on" state and the diode can be replaced by its V_Z source equivalent.

The condition defined by Eq. (2.20) establishes the minimum R_L but in turn specifies the maximum I_L as

$$I_{L_{\max}} = \frac{V_L}{R_L} = \frac{V_Z}{R_{L_{\min}}} \tag{2.21}$$

Once the diode is in the "on" state, the voltage across R remains fixed at

$$V_R = V_i - V_Z \tag{2.22}$$

and I_R remains fixed at

$$I_R = \frac{V_R}{R} \tag{2.23}$$

The Zener current

$$I_Z = I_R - I_L \tag{2.24}$$

resulting in a minimum I_Z when I_L is a maximum and a maximum I_Z when I_L is a minimum value since I_R is constant.

Since I_Z is limited to I_{ZM} as provided on the data sheet, it does affect the range of R_L and therefore I_L. Substituting I_{ZM} for I_Z establishes the minimum I_L as

$$I_{L_{\min}} = I_R - I_{ZM} \tag{2.25}$$

and the maximum load resistance as

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} \tag{2.26}$$

EXAMPLE 2.27

(a) For the network of Fig. 2.113, determine the range of R_L and I_L that will result in V_{R_L} being maintained at 10 V.
(b) Determine the maximum wattage rating of the diode.

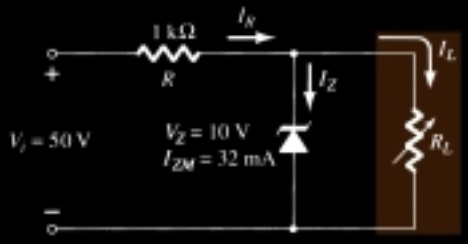


Figure 2.113 Voltage regulator for Example 2.27.

Solution

(a) To determine the value of R_L that will turn the Zener diode on, apply Eq. (2.20):

$$R_{L_{\min}} = \frac{RV_Z}{V_i - V_Z} = \frac{(1\text{ k}\Omega)(10\text{ V})}{50\text{ V} - 10\text{ V}} = \frac{10\text{ k}\Omega}{40} = \mathbf{250\ \Omega}$$

The voltage across the resistor R is then determined by Eq. (2.22):

$$V_R = V_i - V_Z = 50\text{ V} - 10\text{ V} = \mathbf{40\ V}$$

and Eq. (2.23) provides the magnitude of I_R:

$$I_R = \frac{V_R}{R} = \frac{40\text{ V}}{1\text{ k}\Omega} = \mathbf{40\ mA}$$

The minimum level of I_L is then determined by Eq. (2.25):

$$I_{L_{\min}} = I_R - I_{ZM} = 40\text{ mA} - 32\text{ mA} = \mathbf{8\ mA}$$

with Eq. (2.26) determining the maximum value of R_L:

$$R_{L_{\max}} = \frac{V_Z}{I_{L_{\min}}} = \frac{10\text{ V}}{8\text{ mA}} = \mathbf{1.25\ k\Omega}$$

A plot of V_L versus R_L appears in Fig. 2.114a and for V_L versus I_L in Fig. 2.114b.

(b) $P_{\max} = V_Z\, I_{ZM}$
$= (10\text{ V})(32\text{ mA}) = \mathbf{320\ mW}$

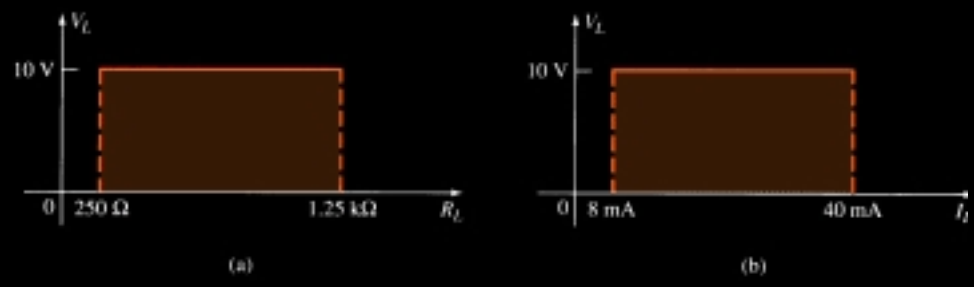


Figure 2.114 V_L versus R_L and I_L for the regulator of Fig. 2.113.

Fixed R_L, Variable V_i

For fixed values of R_L in Fig. 2.106, the voltage V_i must be sufficiently large to turn the Zener diode on. The minimum turn-on voltage $V_i = V_{i_{min}}$ is determined by

$$V_L = V_Z = \frac{R_L V_i}{R_L + R}$$

and

$$\boxed{V_{i_{min}} = \frac{(R_L + R)V_Z}{R_L}} \tag{2.27}$$

The maximum value of V_i is limited by the maximum Zener current I_{ZM}. Since $I_{ZM} = I_R - I_L$,

$$\boxed{I_{R_{max}} = I_{ZM} + I_L} \tag{2.28}$$

Since I_L is fixed at V_Z/R_L and I_{ZM} is the maximum value of I_Z, the maximum V_i is defined by

$$V_{i_{max}} = V_{R_{max}} + V_Z$$

$$\boxed{V_{i_{max}} = I_{R_{max}}R + V_Z} \tag{2.29}$$

EXAMPLE 2.28

Determine the range of values of V_i that will maintain the Zener diode of Fig. 2.115 in the "on" state.

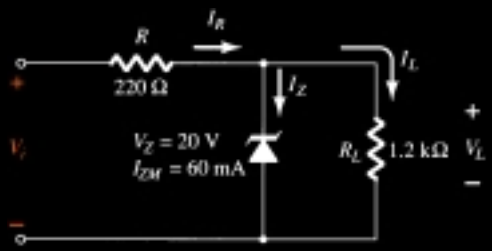


Figure 2.115 Regulator for Example 2.28.

Solution

Eq. (2.27): $V_{i_{min}} = \dfrac{(R_L + R)V_Z}{R_L} = \dfrac{(1200\ \Omega + 220\ \Omega)(20\ \text{V})}{1200\ \Omega} = \mathbf{23.67\ V}$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20\ \text{V}}{1.2\ \text{k}\Omega} = 16.67\ \text{mA}$$

Eq. (2.28): $I_{R_{max}} = I_{ZM} + I_L = 60\ \text{mA} + 16.67\ \text{mA}$

$$= 76.67\ \text{mA}$$

Eq. (2.29): $V_{i_{max}} = I_{R_{max}}R + V_Z$

$$= (76.67\ \text{mA})(0.22\ \text{k}\Omega) + 20\ \text{V}$$

$$= 16.87\ \text{V} + 20\ \text{V}$$

$$= \mathbf{36.87\ V}$$

A plot of V_L versus V_i is provided in Fig. 2.116.

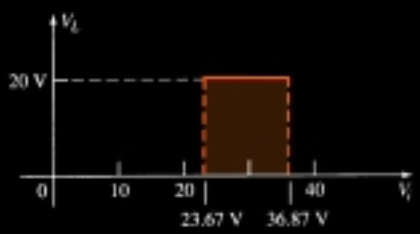


Figure 2.116 V_L versus V_i for the regulator of Fig. 2.115.

The results of Example 2.28 reveal that for the network of Fig. 2.115 with a fixed R_L, the output voltage will remain fixed at 20 V for a range of input voltage that extends from 23.67 to 36.87 V.

In fact, the input could appear as shown in Fig. 2.117 and the output would remain constant at 20 V, as shown in Fig. 2.116. The waveform appearing in Fig. 2.117 is obtained by *filtering* a half-wave- or full-wave-rectified output—a process described in detail in a later chapter. The net effect, however, is to establish a steady dc voltage (for a defined range of V_i) such as that shown in Fig. 2.116 from a sinusoidal source with 0 average value.

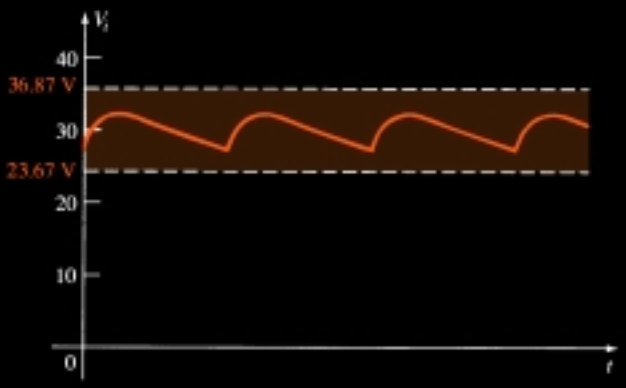


Figure 2.117 Waveform generated by a filtered rectified signal.

Two or more reference levels can be established by placing Zener diodes in series as shown in Fig. 2.118. As long as V_i is greater than the sum of V_{Z_1} and V_{Z_2}, both diodes will be in the "on" state and the three reference voltages will be available.

Two back-to-back Zeners can also be used as an ac regulator as shown in Fig. 2.119a. For the sinusoidal signal v_i the circuit will appear as shown in Fig. 2.119b at the instant $v_i = 10$ V. The region of operation for each diode is indicated in the adjoining figure. Note that Z_1 is in a low-impedance region, while the impedance of Z_2 is quite large, corresponding with the open-circuit representation. The result is that $v_o = v_i$ when $v_i = 10$ V. The input and output will continue to duplicate each other until v_i reaches 20 V. Z_2 will then "turn on" (as a Zener diode), while Z_1 will be in a

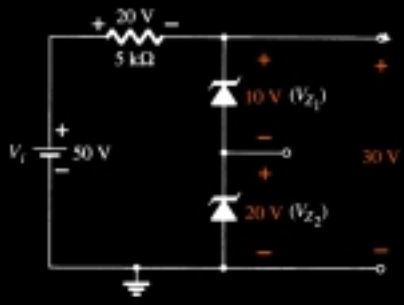


Figure 2.118 Establishing three reference voltage levels.

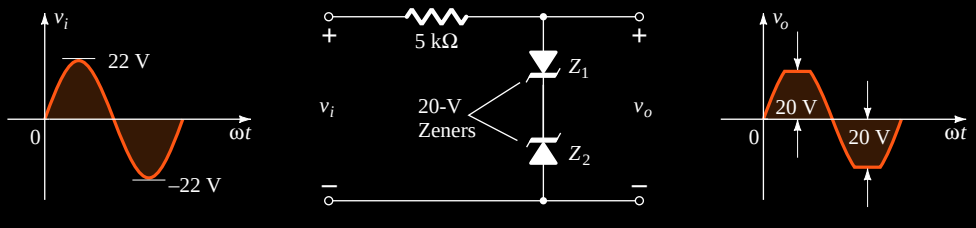


Figure 2.119 Sinusoidal ac regulation: (a) 40-V peak-to-peak sinusoidal ac regulator; (b) circuit operation at $v_i = 10$ V.

region of conduction with a resistance level sufficiently small compared to the series 5-kΩ resistor to be considered a short circuit. The resulting output for the full range of v_i is provided in Fig. 2.119(a). Note that the waveform is not purely sinusoidal, but its rms value is lower than that associated with a full 22-V peak signal. The network is effectively limiting the rms value of the available voltage. The network of Fig. 2.119a can be extended to that of a simple square-wave generator (due to the clipping action) if the signal v_i is increased to perhaps a 50-V peak with 10-V Zeners as shown in Fig. 2.120 with the resulting output waveform.

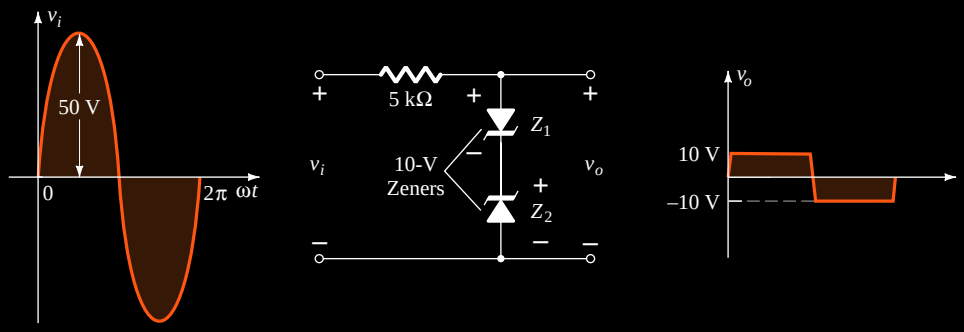


Figure 2.120 Simple square-wave generator.

2.12 VOLTAGE-MULTIPLIER CIRCUITS

Voltage-multiplier circuits are employed to maintain a relatively low transformer peak voltage while stepping up the peak output voltage to two, three, four, or more times the peak rectified voltage.

Voltage Doubler

The network of Figure 2.121 is a half-wave voltage doubler. During the positive voltage half-cycle across the transformer, secondary diode D_1 conducts (and diode D_2 is cut off), charging capacitor C_1 up to the peak rectified voltage (V_m). Diode D_1 is ideally a short during this half-cycle, and the input voltage charges capacitor C_1 to V_m with the polarity shown in Fig. 2.122a. During the negative half-cycle of the secondary voltage, diode D_1 is cut off and diode D_2 conducts charging capacitor C_2. Since diode D_2 acts as a short during the negative half-cycle (and diode D_1 is open), we can sum the voltages around the outside loop (see Fig. 2.122b):

$$-V_m - V_{C_1} + V_{C_2} = 0$$

$$-V_m - V_m + V_{C_2} = 0$$

from which

$$V_{C_2} = 2V_m$$

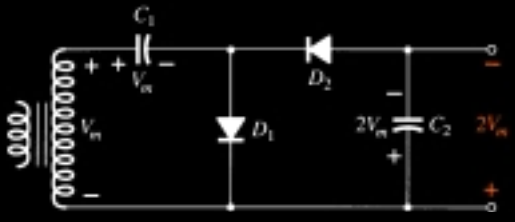


Figure 2.121 Half-wave voltage doubler.

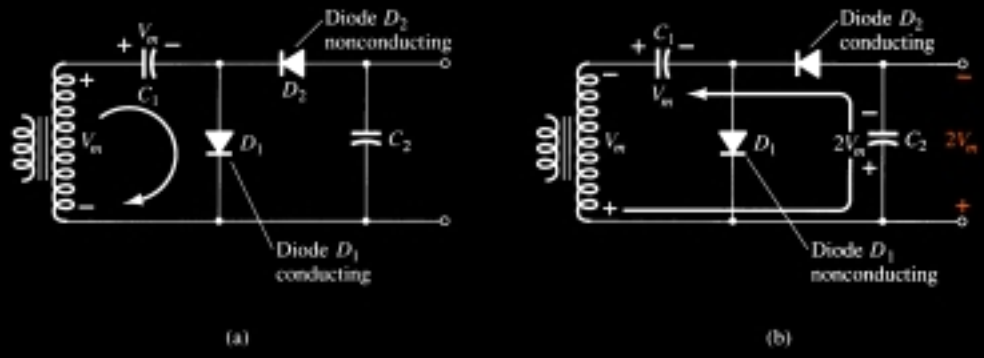


Figure 2.122 Double operation, showing each half-cycle of operation: (a) positive half-cycle; (b) negative half cycle.

On the next positive half-cycle, diode D_2 is nonconducting and capacitor C_2 will discharge through the load. If no load is connected across capacitor C_2, both capacitors stay charged—C_1 to V_m and C_2 to $2V_m$. If, as would be expected, there is a load connected to the output of the voltage doubler, the voltage across capacitor C_2 drops during the positive half-cycle (at the input) and the capacitor is recharged up to $2V_m$ during the negative half-cycle. The output waveform across capacitor C_2 is that of a half-wave signal filtered by a capacitor filter. The peak inverse voltage across each diode is $2V_m$.

Another doubler circuit is the full-wave doubler of Fig. 2.123. During the positive half-cycle of transformer secondary voltage (see Fig. 2.124a) diode D_1 conducts charging capacitor C_1 to a peak voltage V_m. Diode D_2 is nonconducting at this time.

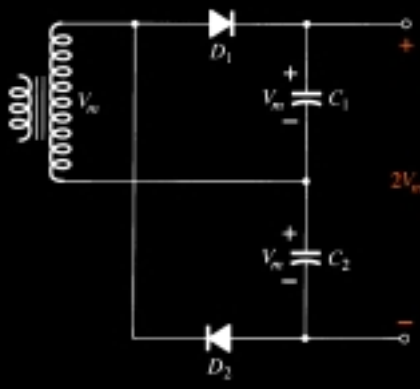


Figure 2.123 Full-wave voltage doubler.

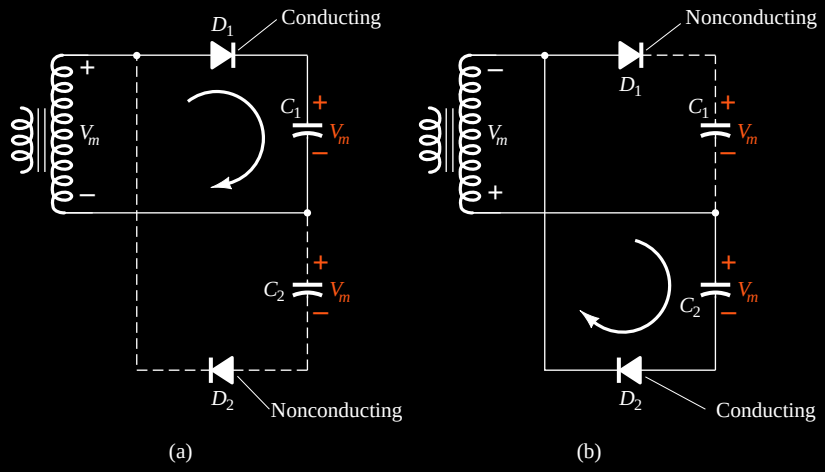


Figure 2.124 Alternate half-cycles of operation for full-wave voltage doubler.

During the negative half-cycle (see Fig. 2.124b) diode D_2 conducts charging capacitor C_2 while diode D_1 is nonconducting. If no load current is drawn from the circuit, the voltage across capacitors C_1 and C_2 is $2V_m$. If load current is drawn from the circuit, the voltage across capacitors C_1 and C_2 is the same as that across a capacitor fed by a full-wave rectifier circuit. One difference is that the effective capacitance is that of C_1 and C_2 in series, which is less than the capacitance of either C_1 or C_2 alone. The lower capacitor value will provide poorer filtering action than the single-capacitor filter circuit.

The peak inverse voltage across each diode is $2V_m$, as it is for the filter capacitor circuit. In summary, the half-wave or full-wave voltage-doubler circuits provide twice the peak voltage of the transformer secondary while requiring no center-tapped transformer and only $2V_m$ PIV rating for the diodes.

Voltage Tripler and Quadrupler

Figure 2.125 shows an extension of the half-wave voltage doubler, which develops three and four times the peak input voltage. It should be obvious from the pattern of the circuit connection how additional diodes and capacitors may be connected so that the output voltage may also be five, six, seven, and so on, times the basic peak voltage (V_m).

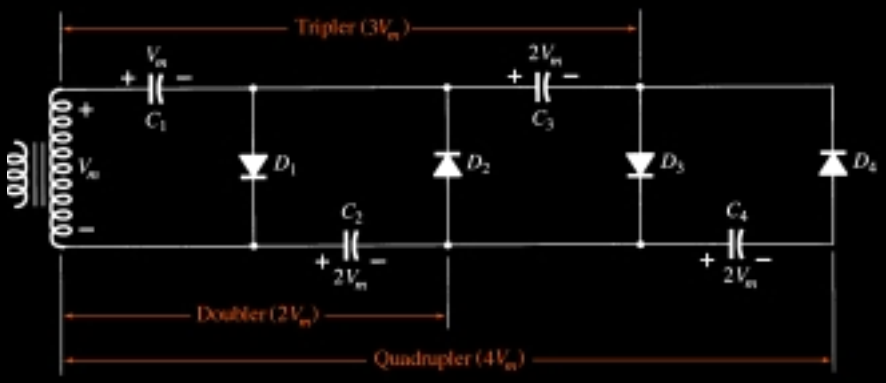


Figure 2.125 Voltage tripler and quadrupler.

In operation capacitor C_1 charges through diode D_1 to a peak voltage, V_m, during the positive half-cycle of the transformer secondary voltage. Capacitor C_2 charges to twice the peak voltage $2V_m$ developed by the sum of the voltages across capacitor C_1 and the transformer, during the negative half-cycle of the transformer secondary voltage.

During the positive half-cycle, diode D_3 conducts and the voltage across capacitor C_2 charges capacitor C_3 to the same $2V_m$ peak voltage. On the negative half-cycle, diodes D_2 and D_4 conduct with capacitor C_3, charging C_4 to $2V_m$.

The voltage across capacitor C_2 is $2V_m$, across C_1 and C_3 it is $3V_m$, and across C_2 and C_4 it is $4V_m$. If additional sections of diode and capacitor are used, each capacitor will be charged to $2V_m$. Measuring from the top of the transformer winding (Fig. 2.125) will provide odd multiples of V_m at the output, whereas measuring the output voltage from the bottom of the transformer will provide even multiples of the peak voltage, V_m.

The transformer rating is only V_m, maximum, and each diode in the circuit must be rated at $2V_m$ PIV. If the load is small and the capacitors have little leakage, extremely high dc voltages may be developed by this type of circuit, using many sections to step up the dc voltage.

2.13 PSPICE WINDOWS

Series Diode Configuration

PSpice Windows will now be applied to the network of Fig. 2.27 to permit a comparison with the hand-calculated solution. As briefly described in Chapter 1, the application of PSpice Windows requires that the network first be constructed on the schematics screen. The next few paragraphs will examine the basics of setting up the network on the screen, assuming no prior experience with the process. It might be helpful to reference the completed network of Fig. 2.126 as we progress through the discussion.

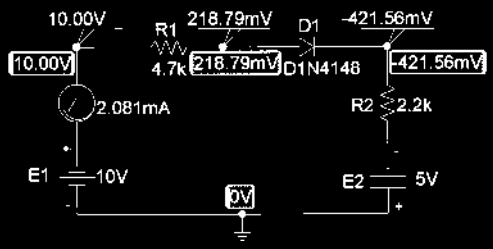


Figure 2.126 PSpice Windows analysis of a series diode configuration.

In general, it is easier to draw the network if the grid is on the screen and the stipulation is made that all elements be on the grid. This will ensure that all the connections are made between the elements. The screen can be set up by first choosing **Options** at the heading of the schematics screen, followed by **Display Options.** The **Display Options** dialog box will permit you to make all the choices necessary regarding the type of display desired. For our purposes, we will choose **Grid On, Stay on Grid,** and **Grid Spacing** of 0.1 in.

R

The resistor **R** will be the first to be positioned. By clicking on the **Get New Part** icon (the icon in the top right area with the binoculars) followed by **Libraries,** we can choose the **Analog.slb** library of basic elements. We can then scroll the **Part** list until we find **R.** Clicking on **R** followed by **OK** will result in the **Part Browser Basic** dialog box reflecting our choice of a resistive element. Choosing the **Place & Close** option will place the resistive element on the screen and close the dialog box. The resistor will appear horizontal, which is perfect for the R_1 of Fig. 2.27 (note Fig. 2.126). Move the resistor to a logical location, and click the left button of the mouse—the resistor R_1 is in place. Note that it snaps to the grid structure. The resistor R_2 must now be placed to the right of R_1. By simply moving the mouse to the right, the second resistor will appear, and R_2 can be placed in the proper location with a subsequent click of the mouse. Since the network only has two resistors, the depositing of resistors can be ended by a right click of the mouse. The resistor R_2 can be rotated by pressing the keys **Ctrl** and **R** simultaneously or by choosing **Edit** on the menu bar, followed by **Rotate.**

The result of the above is two resistors with the right labels but the wrong values. To change a value, double click on the value of the screen (first **R1**). A **Set Attribute Value** dialog box will appear. Type in the correct value, and send the value to the screen with **OK.** The 4.7kΩ will appear within a box that can be moved by simply clicking on the small box and, while holding the clicker down, moving the 4.7kΩ to the desired location. Release the clicker, and the 4.7kΩ label will remain where placed. Once located, an additional click anywhere on the screen will remove the boxes and end the process. If you want to move the 4.7kΩ in the future, simply click once on the value and the boxes will reappear. Repeat the above for the value of the resistor R_2.

To remove (clip) an element, simply click on it (to establish the red or active color), and then click the **scissors** icon or use the sequence **Edit-Delete.**

E

The voltage sources are set by going to the **source.slb** library of **Library Browser** and choosing **VDC.** Clicking **OK** results in the source symbol appearing on the schematic. This symbol can be placed as required. After clicking it in the appropriate place, a **V1** label will appear. To change the label to **E1** simply click the **V1** twice and an **Edit Reference Designator** dialog box will appear. Change the label to **E1** and click **OK,** and then **E1** will appear on the screen within a box. The box can be moved in the same manner as the labels for resistors. When you have the correct position, simply click the mouse once more and place $\mathbf{E_1}$ as desired.

To set the value of E_1, click the value twice and the **Set Attribute Value** will appear. Set the value to 10V and click **OK.** The new value will appear on the schematic. The value can also be set by clicking the battery symbol itself twice, after which a dialog box will appear labeled **E1 PartName:VDC.** By choosing **DC = 0V, DC** and **Value** will appear in the designated areas at the top of the dialog box. Using the mouse, bring the marker to the **Value** box and change it to 10V. Then click **Save Attr.** to be sure and save the new value, and an **OK** will result in E_1 being changed to 10V. E_1 can now be set, but be sure to turn it 180° with the appropriate operations.

DIODE

The diode is found in the **EVAL.slb** library of the **Library Browser** dialog box. Choosing the **D1N4148** diode followed by an **OK** and **Close & Place** will place the diode symbol on the screen. Move the diode to the correct position, click it in place with a left click, and end the operation with a right click of the mouse. The labels **D1** and **D1N4148** will appear near the diode. Clicking on either label will provide the boxes that permit movement of the labels.

Let us now take a look at the diode specs by clicking the diode symbol once, followed by the **Edit-Model-Edit Instance Model** sequence. For the moment, we will leave the parameters as listed. In particular, note that $I_s = 2.682\text{nA}$ and the terminal capacitance (important when the applied frequency becomes a factor) is 4pF.

IPROBE

One or more currents of a network can be displayed by inserting an **IPROBE** in the desired path. **IPROBE** is found in the **SPECIAL.slb** library and appears as a meter face on the screen. **IPROBE** will respond with a positive answer if the current (conventional) enters the symbol at the end with the arc representing the scale. Since we are looking for a positive answer in this investigation, **IPROBE** should be installed as shown in Fig. 2.126. When the symbol first appears, it is 180° out of phase with the desired current. Therefore, it is necessary to use the **Ctrl-R** sequence twice to rotate the symbol before finalizing its position. As with the elements described above, once it is in place a single click will place the meter and a right click will complete the insertion process.

LINE

The elements now need to be connected by choosing the icon with the thin line and pencil or by the sequence **Draw-Wire.** A pencil will appear that can draw the desired connections in the following manner: Move the pencil to the beginning of the line, and click the left side of the mouse. The pencil is now ready to draw. Draw the desired line (connection), and click the left side again when the connection is complete. The line will appear in red, waiting for another random click of the mouse or

the insertion of another line. It will then turn geen to indicate it is in memory. For additional lines, simply repeat the procedure. When done, simply click the right side of the mouse.

EGND

The system must have a ground to serve as a reference point for the nodal voltages. Earth ground **(EGND)** is part of the **PORT.slb** library and can be placed in the same manner as the elements described above.

VIEWPOINT

Nodal voltages can be displayed on the diagram after the simulation using **VIEWPOINTS,** which is found in the **SPECIAL.slb** library. Simply place the arrow of the **VIEWPOINT** symbol where you desire the voltage with respect to ground. A **VIEWPOINT** can be placed at every node of the network if necessary, although only three are placed in Fig. 2.126. The network is now complete, as shown in Fig 2.126.

ANALYSIS

The network is now ready to be analyzed. To expedite the process, click on **Analysis** and choose **Probe Setup.** By selecting **Do not auto-run Probe** you save intermediary steps that are inappropriate for this analysis; it is an option that will be discussed later in this chapter. After **OK,** go to **Analysis** and choose **Simulation**. If the network was installed properly, a **PSpiceAD** dialog box will appear and reveal that the bias (dc) points have been calculated. If we now exit the box by clicking on the small **x** in the top right corner, you will obtain the results appearing in Fig. 2.126. Note that the program has automatically provided four dc voltages of the network (in addition to the **VIEWPOINT** voltages). This occurred because an option under analysis was enabled. For future analysis we will want control over what is displayed so follow the path through **Analysis-Display Results on Schematic** and slide over to the adjoining **Enable** box. Clicking the **Enable** box will remove the check, and the dc voltages will not automatically appear. They will only appear where **VIEWPOINTS** have been inserted. A more direct path toward controlling the appearance of the dc voltages is to use the icon on the menu bar with the large capital **V.** By clicking it on and off, you can control whether the dc levels of the network will appear. The icon with the large capital **I** will permit all the dc currents of the network to be shown if desired. For practice, click it on and off and note the effect on the schematic. If you want to remove selected dc voltages on the schematic, simply click the nodal voltage of interest, then click the icon with the smaller capital **V** in the same grouping. Clicking it once will remove the selected dc voltage. The same can be done for selected currents with the remaining icon of the group. For the future, it should be noted that an analysis can also be initiated by simply clicking the **Simulation** icon having the yellow background and the two waveforms (square wave and sinusoidal).

Note also that the results are not an exact match with those obtained in Example 2.11. The **VIEWPOINT** voltage at the far right is -421.56 rather than the -454.2 mV obtained in Example 2.11. In addition, the current is 2.081 rather than the 2.066 mA obtained in the same example. Further, the voltage across the diode is 281.79 mV + 421.56 mV = 0.64 V rather than the 0.7 V assumed for all silicon diodes. This all results from our using a real diode with a long list of variables defining its operation. However, it is important to remember that the analysis of Example 2.11 was an approximate one and, therefore, it is expected that the results are only close to the actual response. On the other hand, the results obtained for the nodal voltage and current are quite close. If taken to the tenths place, the currents (2.1 mA) are an exact match.

The results obtained in Fig. 2.126 can be improved (in the sense that they will be a closer match to the hand-written solution) by clicking on the diode (to make it red)

Figure 2.127 The circuit of Figure 2.126 reexamined with I_s set to 3.5E-15A.

and using the sequence **Edit-Model-Edit Instance Model (Text)** to obtain the **Model Editor** dialog box. Choose **Is = 3.5E-15A** (a value determined by trial and error), and delete all the other parameters for the device. Then, follow with **OK-Simulate** icon to obtain the results of Fig. 2.127. Note that the voltage across the diode now is 260.17 mV + 440.93 mV = 0.701 V, or almost exactly 0.7 V. The **VIEWPOINT** voltage is −440.93 V or, again, an almost perfect match with the hand-written solution of −0.44 V. In either case, the results obtained are very close to the expected values. One is more accurate as far as the actual device is concerned, while the other provides an almost exact match with the hand-written solution. One cannot expect a perfect match for every diode network by simply setting I_s to 3.5E-15A. As the current through the diode changes, the level of I_s must also change if an exact match with the hand-written solution is to be obtained. However, rather than worry about the current in each system, it is suggested that I_s = 3.5E-15A be used as the standard value if the PSpice solution is desired to be a close match with the hand-written solution. The results will not always be perfect, but in most cases they will be closer than if the parameters of the diode are left at their default values. For transistors in the chapters to follow, it will be set to 2E-15A to obtain a suitable match with the hand-written solution. Note also that the **Bias Current Display** was enabled to show that the current is indeed the same everywhere in the circuit.

The results can also be viewed in tabulated form by returning to **Analysis** and choosing **Examine Output.** The result is the long listing of Fig. 2.128. The **Schematics Netlist** describes the network in terms of numbered nodes. The 0 refers to ground level, with the 10V source from node 0 to 5. The source **E2** is from 0 to node 3. The resistor **R2** is connected from node 3 to 4, and so on. Scrolling down the output file, we find the **Diode MODEL PARAMETERS** clearly showing that I_s is set at 3.5E-15A and is the only parameter listed. Next is the **SMALL SIGNAL BIAS SOLUTION** or dc solution with the voltages at the various nodes. In addition, the current through the sources of the network is shown. The negative sign reveals that it is reflecting the direction of electron flow (into the positive terminal). The total power dissipation of the elements is 31.1 mW. Finally, the **OPERATING POINT INFORMATION** reveals that the current through the diode is 2.07 mA and the voltage across the diode 0.701 V.

The analysis is now complete for the diode circuit of interest. We have not touched on all the alternative paths available through PSpice Windows, but sufficient coverage has been provided to examine any of the networks covered in this chapter with a dc source. For practice, the other examples should be examined using the Windows approach since the results are provided for comparison. The same can be said for the odd-numbered exercises at the end of this chapter.

Diode Characteristics

The characteristics of the D1N4148 diode used in the above analysis will now be obtained using a few maneuvers somewhat more sophisticated than those employed previously. First, the network in Fig. 2.129 is constructed using the procedures described

```
 ****     CIRCUIT DESCRIPTION

*******************************************************************************

* Schematics Netlist *

R_R1          $N_0002 $N_0001  4.7k
V_E2          0 $N_0003 5V
R_R2          $N_0003 $N_0004  2.2k
V_E1          $N_0005 0 10V
D_D1          $N_0001 $N_0004 D1N4148-X2
v_V3          $N_0005 $N_0002 0

****     Diode MODEL PARAMETERS

*******************************************************************************

               D1N4148-X2
          IS    3.500000E-15


 ****     SMALL SIGNAL BIAS SOLUTION       TEMPERATURE =   27.000 DEG C

*******************************************************************************

 NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE     NODE   VOLTAGE

($N_0001)     .2602                    ($N_0002)   10.0000

($N_0003)   -5.0000                    ($N_0004)    -.4409

($N_0005)   10.0000

    VOLTAGE SOURCE CURRENTS
    NAME         CURRENT

    V_E2         -2.072E-03
    V_E1         -2.072E-03
    v_V3          2.072E-03

    TOTAL POWER DISSIPATION   3.11E-02  WATTS

 ****     OPERATING POINT INFORMATION      TEMPERATURE =   27.000 DEG C

*******************************************************************************

 **** DIODES


NAME          D_D1
MODEL         D1N4148-X2
ID            2.07E-03
VD            7.01E-01
REQ           1.25E+01
CAP           0.00E+00
```

Figure 2.128 Output file for PSpice Windows analysis of the circuit of Figure 2.127.

above. Note, however, the **Vd** appearing above the diode **D1.** A point in the network (representing the voltage from anode to ground for the diode) has been identified as a particular voltage by double-clicking on the wire above the device and typing Vd in the **Set Attribute Value** as the **LABEL.** The resulting voltage V_d is, in this case, the voltage across the diode.

Next, **Analysis Setup** is chosen by either clicking on the Analysis Setup icon (at the top left edge of the schematic with the horizontal blue bar and the two small squares and rectangles) or by using the sequence **Analysis-Setup.** Within the **Analysis-Setup** dialog box the **DC Sweep** is enabled (the only one necessary for this exercise), followed by a single click of the **DC Sweep** rectangle. The **DC Sweep** dialog box will appear with various inquiries. In this case, we plan to sweep the source voltage from 0 to 10 V in 0.01-V increments, so the **Swept Var. Type** is Voltage Source, the **Sweep Type** will be linear, the **Name** E, and the **Start Value** 0V, the **End Value** 10V, and the **Increment** 0.01V. Then, with an **OK** followed by a **Close** of the

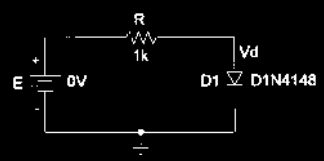


Figure 2.129 Network to obtain the characteristics of the D1N4148 diode.

Analysis Setup box, we are set to obtain the solution. The analysis to be performed will obtain a complete solution for the network for each value of E from 0 to 10 V in 0.01-V increments. In other words, the network will be analyzed 1000 times and the resulting data stored for the plot to be obtained. The analysis is performed by the sequence **Analysis-Run Probe,** followed by an immediate appearance of the **MicroSim Probe** graph showing only a horizontal axis of the source voltage E running from 0 to 10 V.

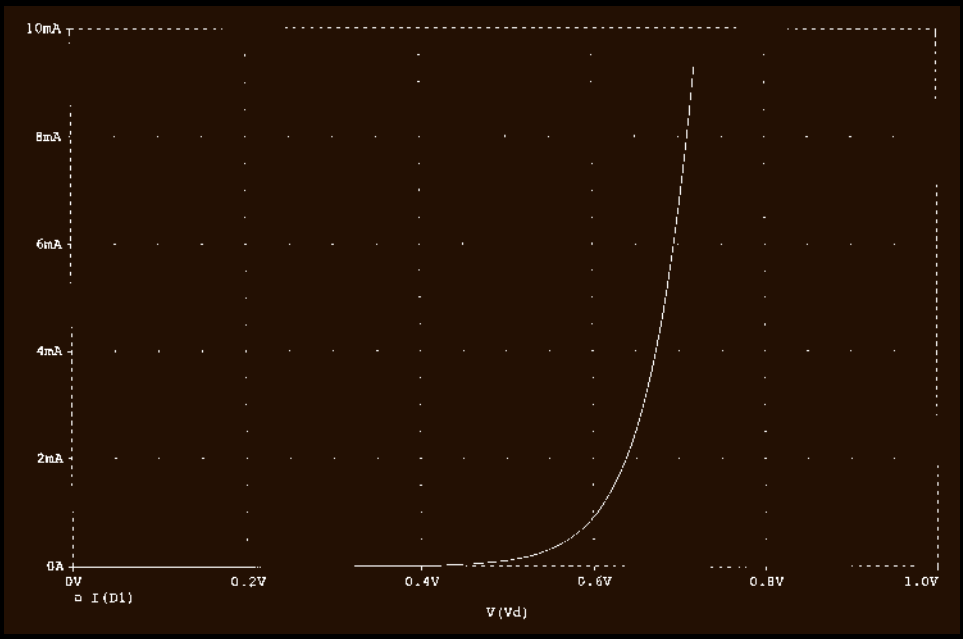


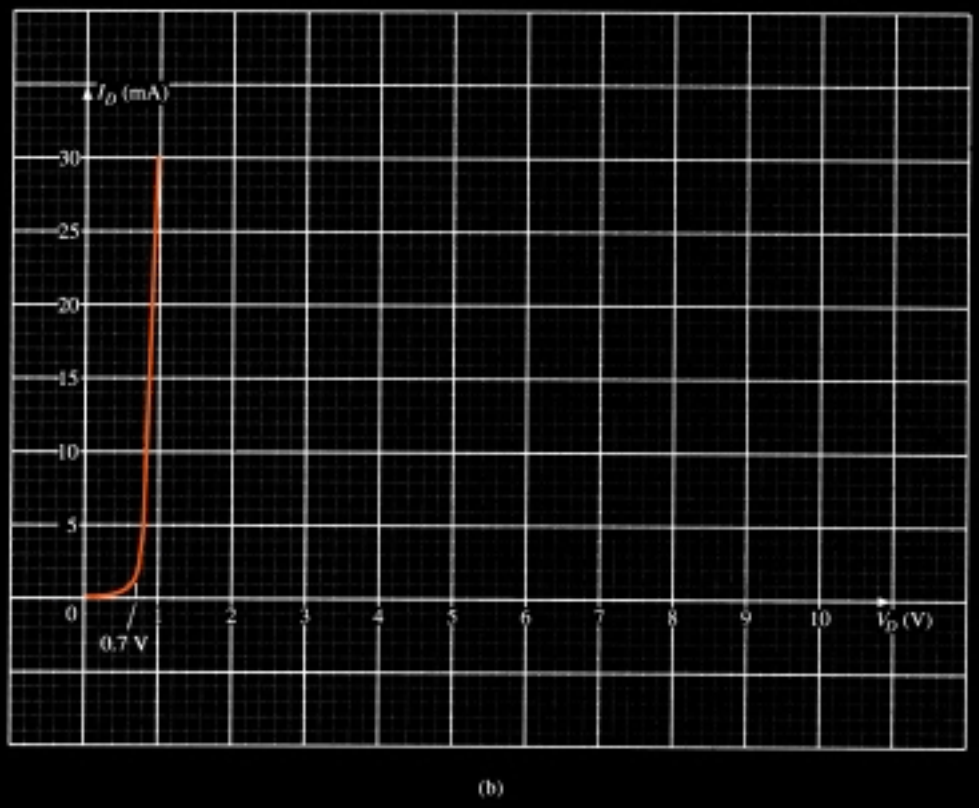
Figure 2.130 Characteristics of the D1N4148 diode.

Since the plot we want is of I_D versus V_D, we have to change the horizontal (x-axis) to V_D. This is accomplished by selecting **Plot** and then **X-Axis Settings** to obtain the **X Axis Settings** dialog box. Next, we click **Axis Variable** and select **V(Vd)** from the listing. After **OK**, we return to the dialog box to set the horizontal scale. Choose **User Defined,** then enter 0V to 1V since this is the range of interest for Vd with a **Linear** scale. Click **OK** and you will find that the horizontal axis is now V(Vd) with a range of 0 to 1.0 V. The vertical axis must now be set to I_D by first choosing **Trace** (or the **Trace** icon, which is the red waveform with two sharp peaks and a set of axis) and then **Add** to obtain **Add Traces.** Choosing **I(D1)** and clicking **OK** will result in the plot of Fig. 2.130. In this case, the resulting plot extended from 0 to 10 mA. The range can be reduced or expanded by simply going to **Plot-Y-Axis Setting** and defining the range of interest.

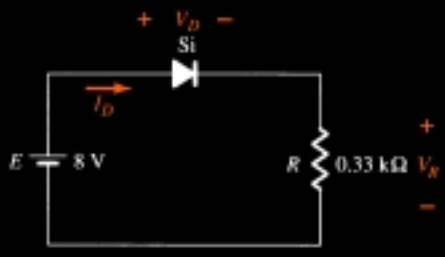
In the previous analysis, the voltage across the diode was 0.64 V, corresponding to a current of about 2 mA on the graph (recall the solution of 2.07 mA for the current). If the resulting current had been closer to 6.5 mA, the voltage across the diode would have been about 0.7 V and the PSpice solution closer to the hand-written approach. If I_s had been set to 3.5E-15A and all other parameters removed from the diode listing, the curve would have shifted to the right and an intersection of 0.7 V and 2.07 mA would have obtained.

§ 2.2 Load-Line Analysis

1. (a) Using the characteristics of Fig. 2.131b, determine I_D, V_D, and V_R for the circuit of Fig. 2.131a.
(b) Repeat part (a) using the approximate model for the diode and compare results.
(c) Repeat part (a) using the ideal model for the diode and compare results.



(b)



(a)

Figure 2.131 Problems 1, 2

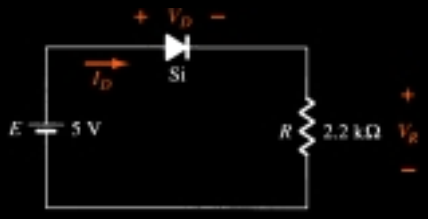


Figure 2.132 Problems 2, 3

2. (a) Using the characteristics of Fig. 2.131b, determine I_D and V_D for the circuit of Fig. 2.132.
(b) Repeat part (a) with $R = 0.47\ \text{k}\Omega$.
(c) Repeat part (a) with $R = 0.18\ \text{k}\Omega$.
(d) Is the level of V_D relatively close to 0.7 V in each case?

How do the resulting levels of I_D compare? Comment accordingly.

3. Determine the value of R for the circuit of Fig. 2.132 that will result in a diode current of 10 mA if $E = 7$ V. Use the characteristics of Fig. 2.131b for the diode.

4. (a) Using the approximate characteristics for the Si diode, determine the level of V_D, I_D, and V_R for the circuit of Fig. 2.133.
(b) Perform the same analysis as part (a) using the ideal model for the diode.
(c) Do the results obtained in parts (a) and (b) suggest that the ideal model can provide a good approximation for the actual response under some conditions?

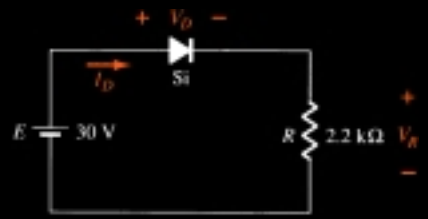


Figure 2.133 Problem 4

5. Determine the current I for each of the configurations of Fig. 2.134 using the approximate equivalent model for the diode.

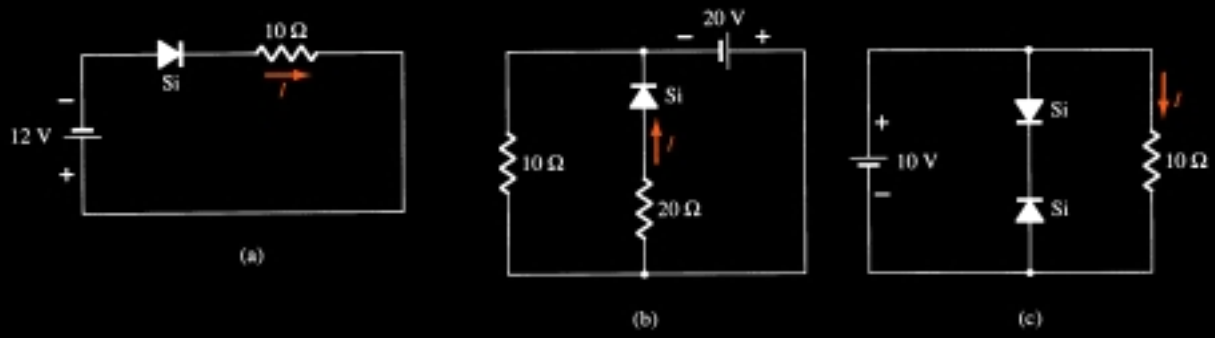


Figure 2.134 Problem 5

6. Determine V_o and I_D for the networks of Fig. 2.135.

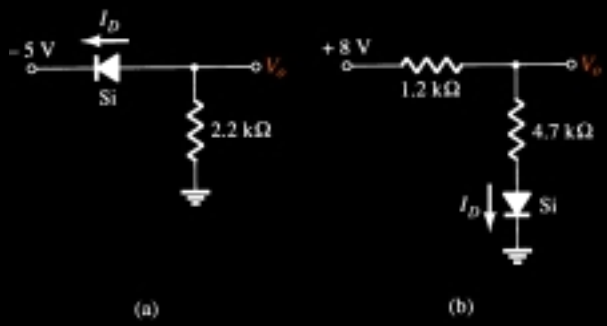


Figure 2.135 Problems 6, 49

* **7.** Determine the level of V_o for each network of Fig. 2.136.

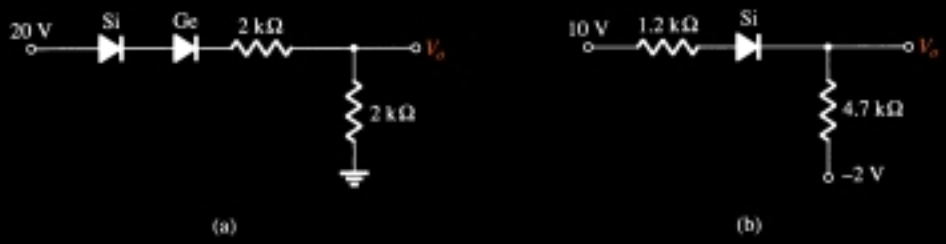


Figure 2.136 Problem 7

* **8.** Determine V_o and I_D for the networks of Fig. 2.137.

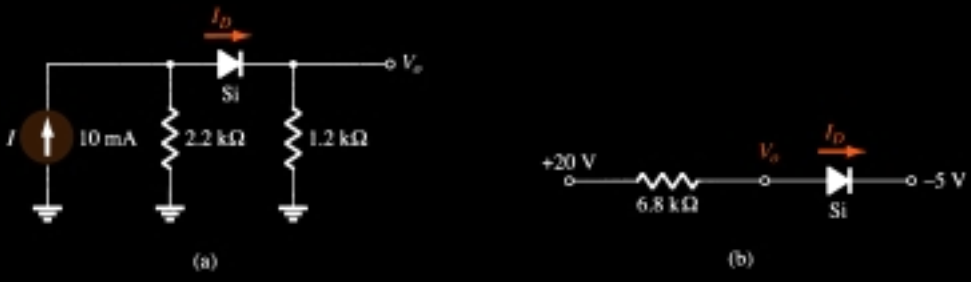


Figure 2.137 Problem 8

* **9.** Determine V_{o_1} and V_{o_2} for the networks of Fig. 2.138.

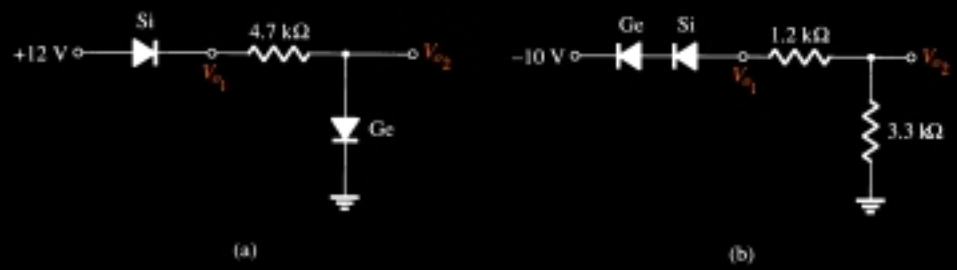


Figure 2.138 Problem 9

§ 2.5 Parallel and Series–Parallel Configurations

10. Determine V_o and I_D for the networks of Fig. 2.139.

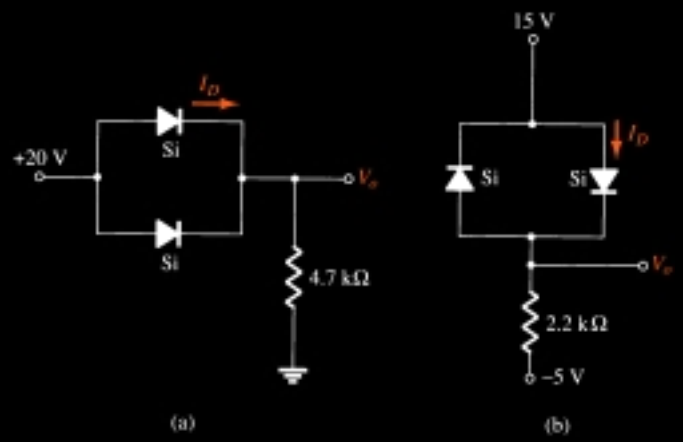


Figure 2.139 Problems 10, 50

* **11.** Determine V_o and I for the networks of Fig. 2.140.

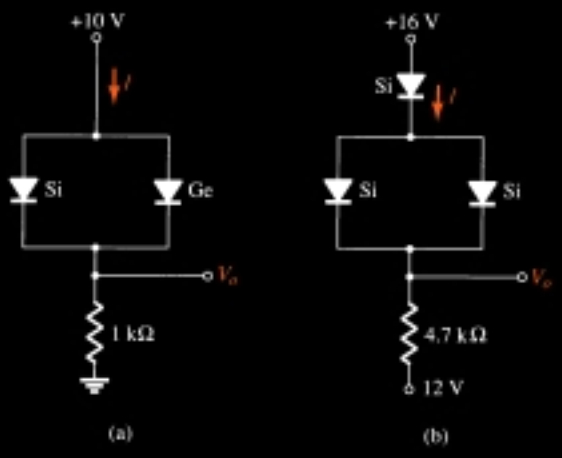


Figure 2.140 Problem 11

12. Determine V_{o_1}, V_{o_2}, and I for the network of Fig. 2.141.

* **13.** Determine V_o and I_D for the network of Fig. 2.142.

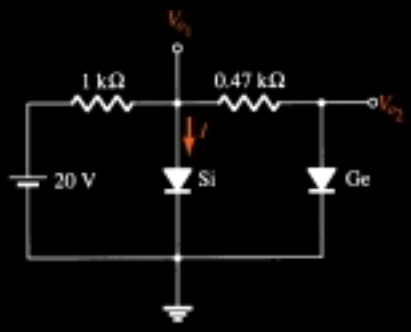


Figure 2.141 Problem 12

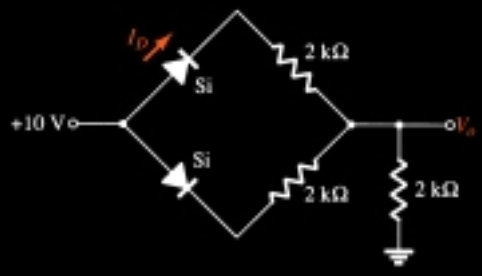


Figure 2.142 Problems 13, 51

§ 2.6 AND/OR Gates

14. Determine V_o for the network of Fig. 2.38 with 0 V on both inputs.

15. Determine V_o for the network of Fig. 2.38 with 10 V on both inputs.

16. Determine V_o for the network of Fig. 2.41 with 0 V on both inputs.

17. Determine V_o for the network of Fig. 2.41 with 10 V on both inputs.

18. Determine V_o for the negative logic OR gate of Fig. 2.143.

19. Determine V_o for the negative logic AND gate of Fig. 2.144.

20. Determine the level of V_o for the gate of Fig. 2.145.

21. Determine V_o for the configuration of Fig. 2.146.

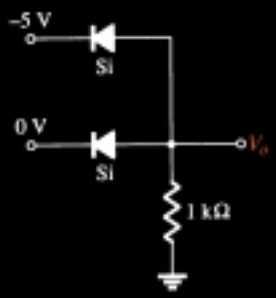


Figure 2.143 Problem 18

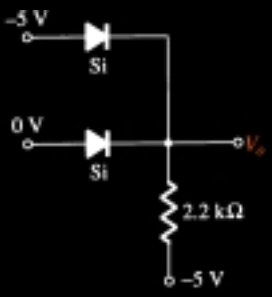


Figure 2.144 Problem 19

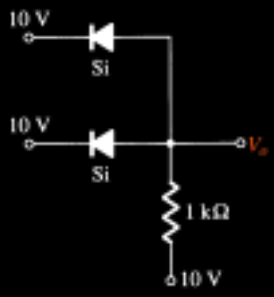


Figure 2.145 Problem 20

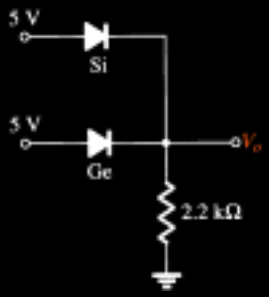


Figure 2.146 Problem 21

§ 2.7 Sinusoidal Inputs; Half-Wave Rectification

22. Assuming an ideal diode, sketch v_i, v_d, and i_d for the half-wave rectifier of Fig. 2.147. The input is a sinusoidal waveform with a frequency of 60 Hz

* **23.** Repeat Problem 22 with a silicon diode ($V_T = 0.7$ V).

* **24.** Repeat Problem 22 with a 6.8-kΩ load applied as shown in Fig. 2.148. Sketch v_L and i_L.

25. For the network of Fig. 2.149, sketch v_o and determine V_{dc}.

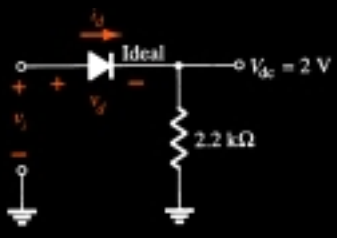


Figure 2.147 Problems 22, 23, 24

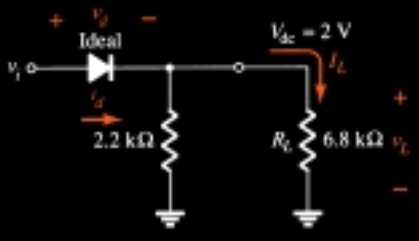


Figure 2.148 Problem 24

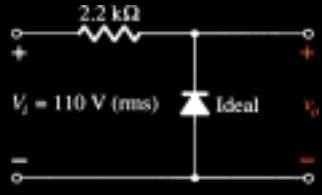


Figure 2.149 Problem 25

* **26.** For the network of Fig. 2.150, sketch v_o and i_R.

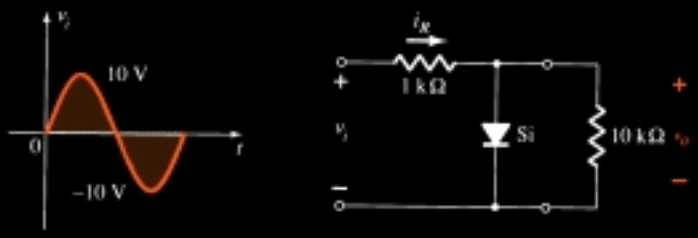


Figure 2.150 Problem 26

* **27.** (a) Given $P_{max} = 14$ mW for each diode of Fig. 2.151, determine the maximum current rating of each diode (using the approximate equivalent model).
(b) Determine I_{max} for $V_{i_{max}} = 160$ V.
(c) Determine the current through each diode at $V_{i_{max}}$ using the results of part (b).
(e) If only one diode were present, determine the diode current and compare it to the maximum rating.

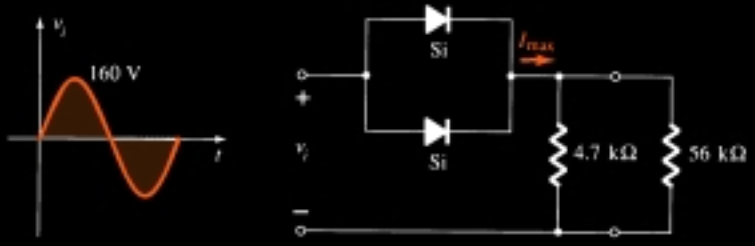


Figure 2.151 Problem 27

§ 2.8 Full-Wave Rectification

28. A full-wave bridge rectifier with a 120-V rms sinusoidal input has a load resistor of 1 kΩ.
(a) If silicon diodes are employed, what is the dc voltage available at the load?
(b) Determine the required PIV rating of each diode.
(c) Find the maximum current through each diode during conduction.
(d) What is the required power rating of each diode?

29. Determine v_o and the required PIV rating of each diode for the configuration of Fig. 2.152.

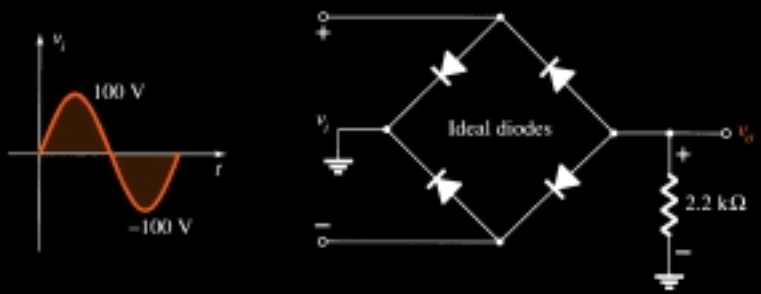


Figure 2.152 Problem 29

* **30.** Sketch v_o for the network of Fig. 2.153 and determine the dc voltage available.

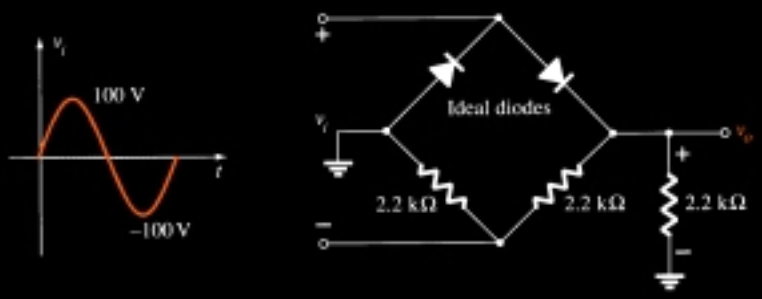


Figure 2.153 Problem 30

* **31.** Sketch v_o for the network of Fig. 2.154 and determine the dc voltage available.

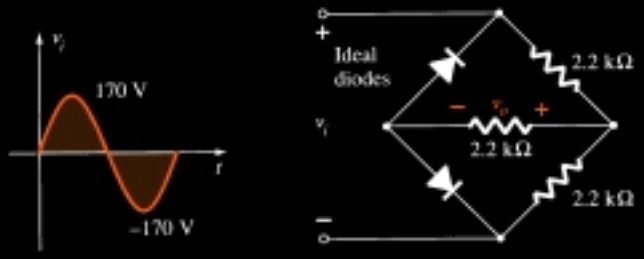


Figure 2.154 Problem 31

§ 2.9 Clippers

32. Determine v_o for each network of Fig. 2.155 for the input shown.

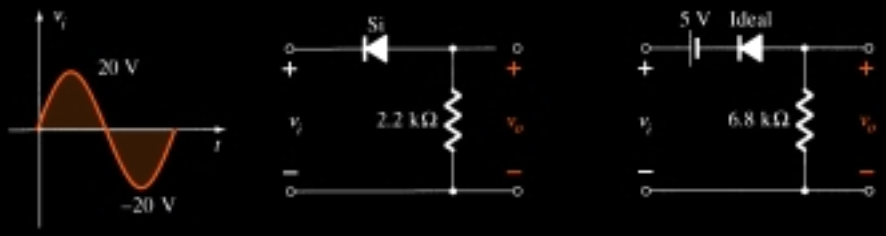


Figure 2.155 Problem 32

33. Determine v_o for each network of Fig. 2.156 for the input shown.

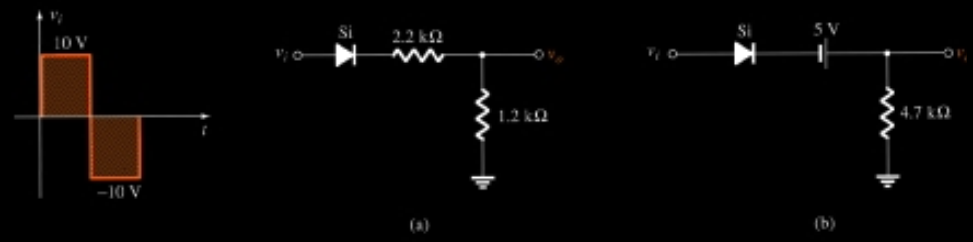


Figure 2.156 Problem 33

* **34.** Determine v_o for each network of Fig. 2.157 for the input shown.

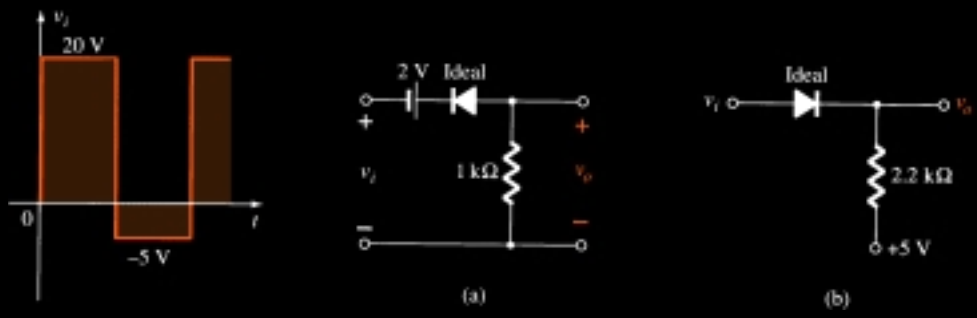


Figure 2.157 Problem 34

* **35.** Determine v_o for each network of Fig. 2.158 for the input shown.

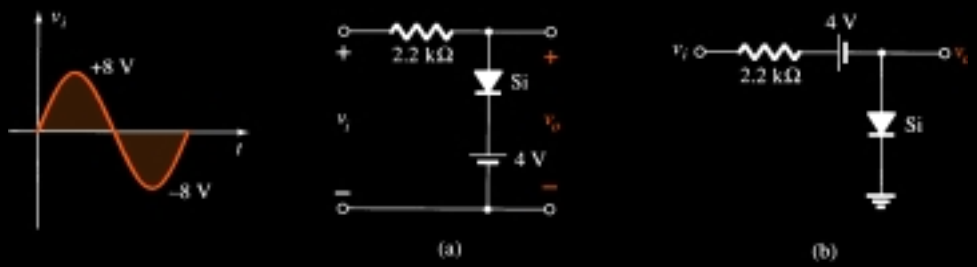


Figure 2.158 Problem 35

36. Sketch i_R and v_o for the network of Fig. 2.159 for the input shown.

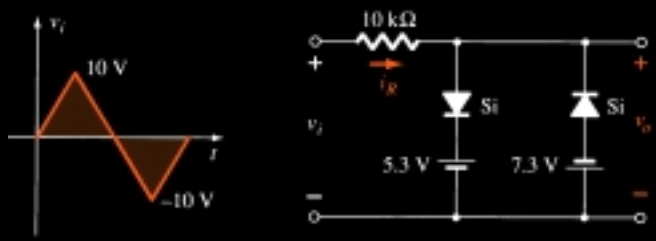


Figure 2.159 Problem 36

§ 2.10 Clampers

37. Sketch v_o for each network of Fig. 2.160 for the input shown.

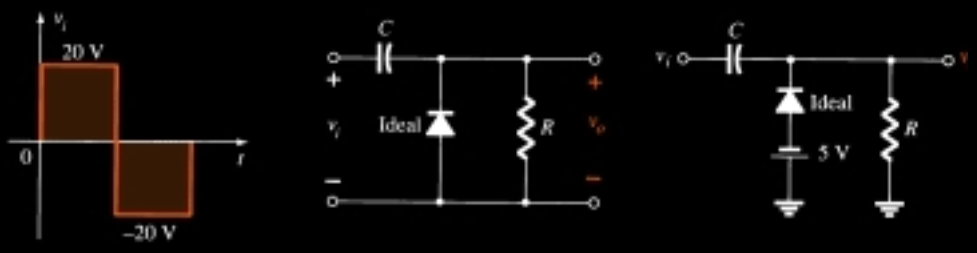


Figure 2.160 Problem 37

38. Sketch v_o for each network of Fig. 2.161 for the input shown. Would it be a good approximation to consider the diode to be ideal for both configurations? Why?

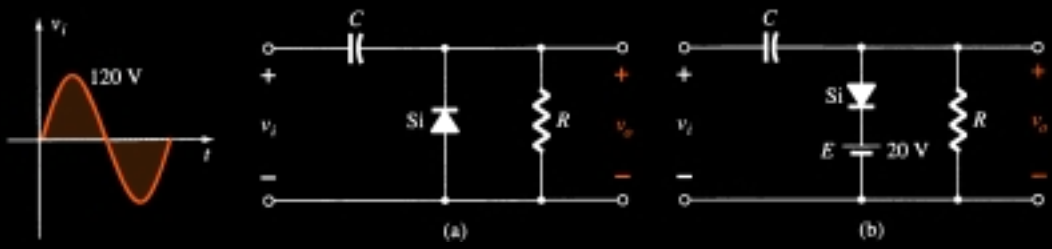


Figure 2.161 Problem 38

* **39.** For the network of Fig. 2.162:

(a) Calculate 5τ.

(b) Compare 5τ to half the period of the applied signal.

(c) Sketch v_o.

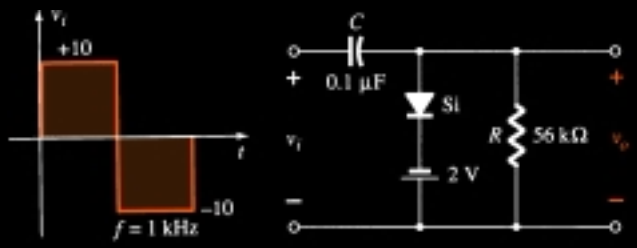


Figure 2.162 Problem 39

* **40.** Design a clamper to perform the function indicated in Fig. 2.163.

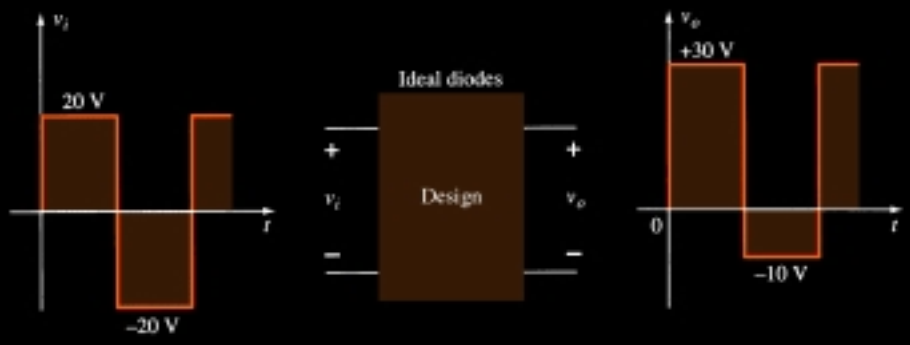


Figure 2.163 Problem 40

* **41.** Design a clamper to perform the function indicated in Fig. 2.164.

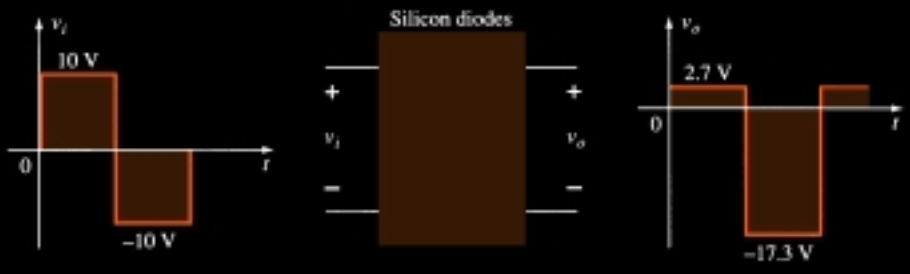


Figure 2.164 Problem 41

§ 2.11 Zener Diodes

* **42.** (a) Determine V_L, I_L, I_Z, and I_R for the network Fig. 2.165 if $R_L = 180\ \Omega$
(b) Repeat part (a) if $R_L = 470\ \Omega$.
(c) Determine the value of R_L that will establish maximum power conditions for the Zener diode.
(d) Determine the minimum value of R_L to ensure that the Zener diode is in the "on" state.

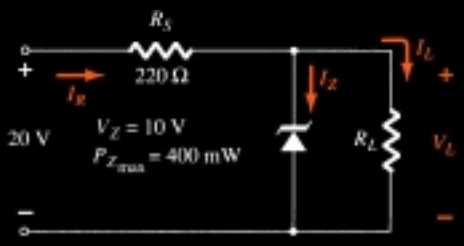


Figure 2.165 Problem 42

* **43.** (a) Design the network of Fig. 2.166 to maintain V_L at 12 V for a load variation (I_L) from 0 to 200 mA. That is, determine R_s and V_Z.
(b) Determine $P_{Z_{max}}$ for the Zener diode of part (a).

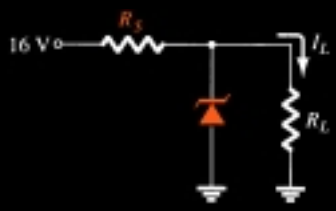


Figure 2.166 Problem 43

* **44.** For the network of Fig. 2.167, determine the range of V_i that will maintain V_L at 8 V and not exceed the maximum power rating of the Zener diode.

45. Design a voltage regulator that will maintain an output voltage of 20 V across a 1-kΩ load with an input that will vary between 30 and 50 V. That is, determine the proper value of R_s and the maximum current I_{ZM}.

46. Sketch the output of the network of Fig. 2.120 if the input is a 50-V square wave. Repeat for a 5-V square wave.

§ 2.12 Voltage-Multiplier Circuits

47. Determine the voltage available from the voltage doubler of Fig. 2.121 if the secondary voltage of the transformer is 120 V (rms).

48. Determine the required PIV ratings of the diodes of Fig. 2.121 in terms of the peak secondary voltage V_m.

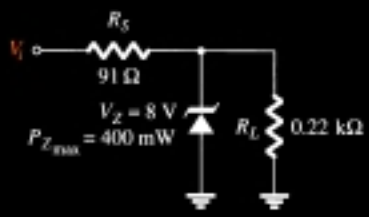


Figure 2.167 Problems 44, 52

§ 2.13 PSpice Windows

49. Perform an analysis of the network of Fig. 2.135 using PSpice Windows.

50. Perform an analysis of the network of Fig. 2.139 using PSpice Windows.

51. Perform an analysis of the network of Fig. 2.142 using PSpice Windows.

52. Perform a general analysis of the Zener network of Fig. 2.167 using PSpice Windows.

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* Please Note: Asterisks indicate more difficult problems.