



ZHONGJINGYUAN

郑州中景园电子技术有限公司

商城地址 : <https://zjy-display.taobao.com> TEL : 18601955397

Product Specification

Part Name: OEL Display Module

Customer Part ID:

Zhongjingyuan Part ID: ZJY128296-029EAAMFGN

Ver: A

Customer:

Approved by

From: Zhengzhou Zhongjingyuan Electronic Technology Co., LTD.

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Zhengzhou Zhongjingyuan Electronic Technology Co., LTD.

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Notes:

1. Please contact Zhengzhou Zhongjingyuan Electronic Technology Co., LTD. before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Zhengzhou Zhongjingyuan Electronic Technology Co., LTD. for any intellectual property claims or other problems that may result from application based on the module described herein.

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REVISION HISTORY

Rev	Date	Item	Page	Remark
1.0	MAR.15.2021	New Creation	ALL	
1.1	FEB.14.2022	Update Mechanical Drawing of EPD module Update Packaging	P5 P33	

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1. Over View

YMS128296-029EAAMFGN is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white, black full display capabilities. The 2.9 inch active area contains 296×128 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

- 296×128 pixels display
- High contrast High reflectance
- Ultra wide viewing angle Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform can stored in On-chip OTP or written by MCU
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I²C signal master interface to read external temperature sensor
- Built-in temperature sensor

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.9	Inch	
Display Resolution	128 (H)×296(V)	Pixel	Dpi:125
Active Area	29.056(H)×66.896(V)	mm	
Pixel Pitch	0.227×0.226	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.7(H)×79.0(V) ×1.2(D)	mm	
Weight	5.5±0.5	g	

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4. Mechanical Drawing of EPD module

CUSTOMER'S APPROVED:		DATE:	PAGE:1/1		
NO.	REVISION RECORD	NAME	DATE		
3		ZJY128296-029EAAMFGN Ver. 1	WJZ 2022/02/14		
2		Drv			
1		Chk			
Initial version.					
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PIN NO. Symbol					
1	NC	2	GDR		
2	GDR	3	RESE		
3	RESE	4	NC		
4	NC	5	VSH2		
5	VSH2	6	TSCL		
6	TSCL	7	TSDA		
7	TSDA	8	BS1		
8	BS1	9	BUSY		
9	BUSY	10	RST#		
10	RST#	11	D/C#		
11	D/C#	12	CS#		
12	CS#	13	SCL		
13	SCL	14	SDA		
14	SDA	15	VDDIO		
15	VDDIO	16	VCI		
16	VCI	17	VSS		
17	VSS	18	VDD		
18	VDD	19	VPP		
19	VPP	20	VSH1		
20	VSH1	21	VGH		
21	VGH	22	VSL		
22	VSL	23	VGL		
23	VGL	24	VCOM		
24	VCOM				
1 Display mode EPD,B/W					
2 Resolution ratio 2.9',128*296					
3 Operating Voltage: VGL=3.0V					
4 Operating Temp: 0°C~50°C					
5 Storage Temp: -25°C~70°C					
6 controller/driver: SSD1680					
7 Unspecified tolerance: ±0.2					
8 Customer No.: 9 Dimensions with mark "*" are important					
10 RoHS compliant					

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5. Input /Output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VSH2	C	Positive Source driving voltage(Red)	
6	TSCL	O	I ² C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I ² C Interface to digital temperature sensor Data pin	
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I/O	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	
20	VSH1	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH1	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

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I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent. The chip would put Busy pin High when –Outputting display waveform -Communicating with digital temperature sensor

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to +50	°C
Storage Temp range	TSTG	-25 to +70	°C
Optimal Storage Temp	TSTGo	23±2	°C
Optimal Storage Humidity	HSTGo	55±10	%RH

Note:

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

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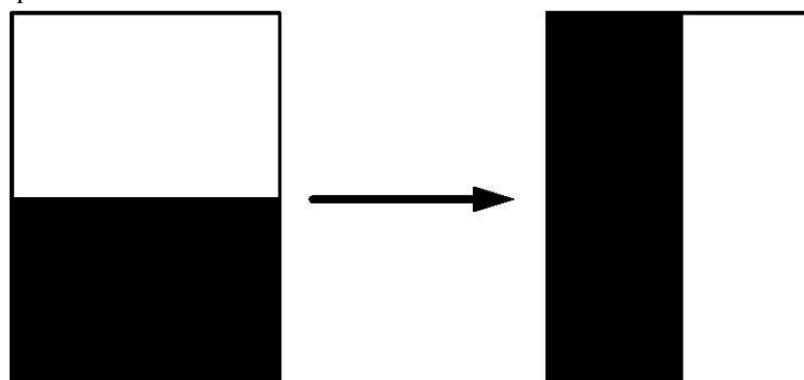
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6.2 Panel DC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25°C.

Parameter	Symbol	Conditions	Applicable pin	Min.	Typ.	Max	Units
Single ground	V _{SS}	-		-	0	-	V
Logic supply voltage	V _{CI}	-	VCI	2.2	3.0	3.7	V
Core logic voltage	V _{DD}		VDD	1.7	1.8	1.9	V
High level input voltage	V _{IH}	-	-	0.8 V _{CI}	-	-	V
Low level input voltage	V _{IL}	-	-	-	-	0.2 V _{CI}	V
High level output voltage	V _{OH}	IOH = -100uA	-	0.9 VCI	-	-	V
Low level output voltage	V _{OL}	IOL = 100uA	-	-	-	0.1 V _{CI}	V
Typical power	P _{TYP}	V _{CI} =3.0V	-	-	9	-	mW
Deep sleep mode	P _{STPY}	V _{CI} =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_V _{CI}	V _{CI} =3.0V	-	-	3.0	-	mA
Image update time	-	25 °C	-	-	3	-	sec
Sleep mode current	Islp_V _{CI}	DC/DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	Idslp_V _{CI}	DC/DC off No clock No input load Ram data not retain	-	-	1	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by ZHONGJINGYUAN.

6.3 Panel AC Characteristics

6.3.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDA	SCL	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDA	SCL	CS#	L	RES#

6.3.2 MCU Serial Interface (4-wire SPI)

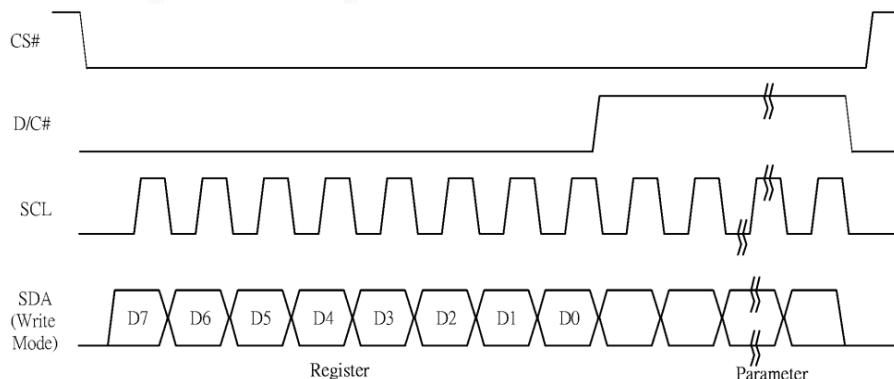
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

In the write mode SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte . The data byte in the shift register is written to the Graphic Display Data RAM /Data Byte register or command Byte register according to D/C# pin.

Figure 6-1: Write procedure in 4-wire SPI mode



In the Read mode:

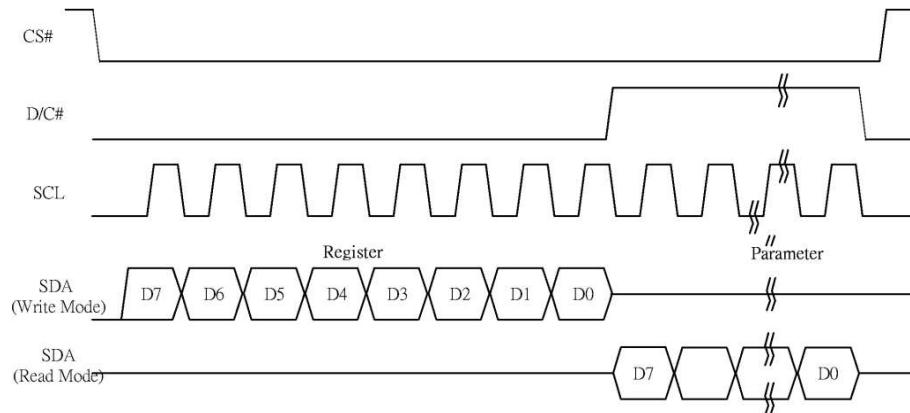
1. After driving CS# to low, MCU need to define the register to be read.
2. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0 with D/C# keep low.
3. After SCL change to low for the last bit of register, D/C# need to drive to high.
4. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
5. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

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商城地址 : <https://zjy-display.taobao.com> TEL : 18601955397**Figure 6-2: Read procedure in 4-wire SPI mode**

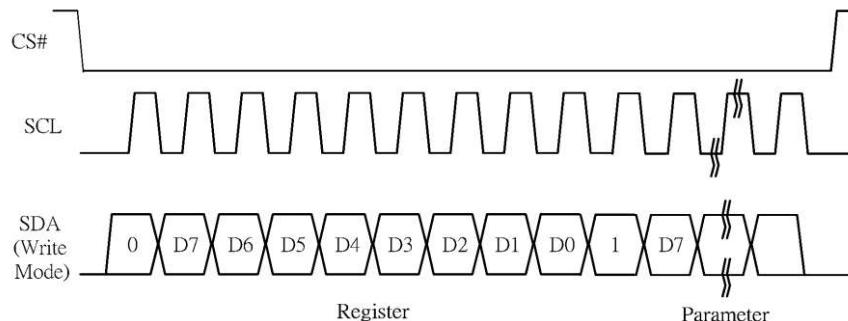
6.3.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

Note: ↑ stands for rising edge of signal

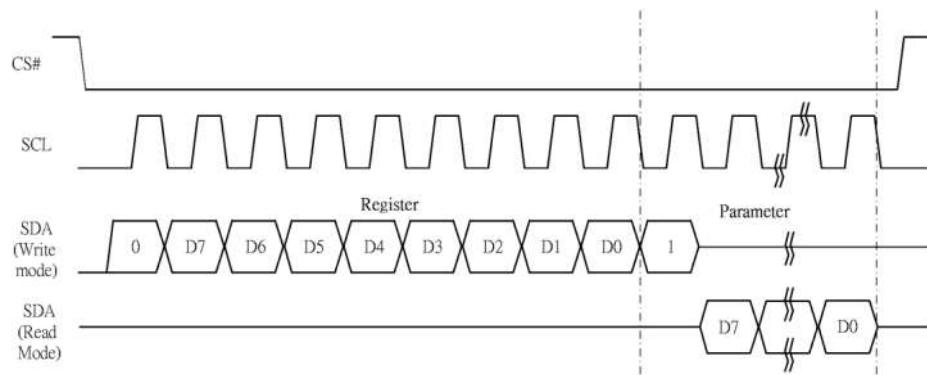
Figure 6-3: Write procedure in 3-wire SPI mode

In the Read mode:

1. After driving CS# to low, MCU need to define the register to be read.
2. D/C=0 is shifted thru SDA with one rising edge of SCL
3. SDA is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0.
4. D/C=1 is shifted thru SDA with one rising edge of SCL
5. SDA is shifted out an 8-bit data on every falling edge of SCL in the order of D7, D6, ... D0.
6. Depending on register type, more than 1 byte can be read out. After all byte are read, CS# need to drive to high to stop the read operation.

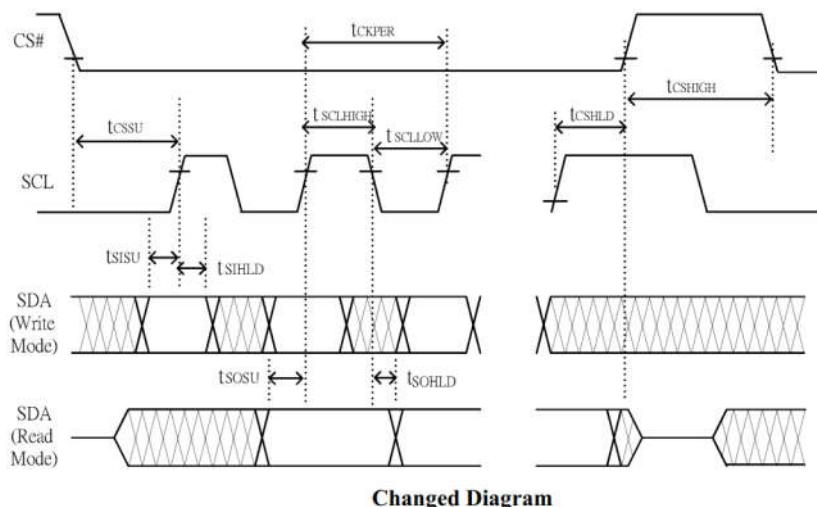
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Figure 6-4: Read procedure in 3-wire SPI mode



6.3.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =25°C.



Serial Interface Timing Characteristics

(VCI - VSS = 2.2V to 3.7V, TOPR = 25°C, CL=20pF)

Write mode

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL frequency (Write Mode)			20	MHz
t _{CSSU}	Time CS# has to be low before the first rising edge of SCLK	60			ns
t _{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	65			ns
t _{CSHIGH}	Time CS# has to remain high between two transfers	100			ns
t _{SCLHIGH}	Part of the clock period where SCL has to remain high	25			ns
t _{SCLLOW}	Part of the clock period where SCL has to remain low	25			ns
t _{SISU}	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
t _{SIHLD}	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
f _{SCL}	SCL frequency (Read Mode)			2.5	MHz
t _{CSSU}	Time CS# has to be low before the first rising edge of SCLK	100			ns
t _{CSHLD}	Time CS# has to remain low after the last falling edge of SCLK	50			ns
t _{CSHIGH}	Time CS# has to remain high between two transfers	250			ns
t _{SCLHIGH}	Part of the clock period where SCL has to remain high	180			ns
t _{SCLLOW}	Part of the clock period where SCL has to remain low	180			ns
t _{SOHU}	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL	50			ns
t _{SOHLD}	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL	0			ns



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7. Command Table

Command Table												
R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output control	Gate setting A[8:0]= 127h [POR], 296 MUX MUX Gate lines setting as (A[8:0] + 1). B[2:0] = 000 [POR]. Gate scanning sequence and direction
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		B[2]: GD Selects the 1st output Gate GD=0 [POR], G0 is the 1st gate output channel, gate output sequence is G0,G1, G2, G3, ... GD=1, G1 is the 1st gate output channel, gate output sequence is G1, G0, G3, G2, ...
0	1		0	0	0	0	0	0	B ₂	B ₁		B[1]: SM Change scanning order of gate driver. SM=0 [POR], G0, G1, G2, G3...295 (left and right gate interlaced) SM=1, G0, G2, G4 ...G294, G1, G3, ...G295
0	1		0	0	0	0	0	B ₀				B[0]: TB TB = 0 [POR], scan from G0 to G295 TB = 1, scan from G295 to G0.
0	0	03	0	0	0	0	0	0	1	1	Gate Driving voltage Control	Set Gate driving voltage A[4:0] = 00h [POR] VGH setting from 10V to 20V
0	1		0	0	0	A ₄	A ₃	A ₂	A ₁	A ₀		A[4:0] VGH A[4:0] VGH
												00h 20 0Dh 15
												03h 10 0Eh 15.5
												04h 10.5 0Fh 16
												05h 11 10h 16.5
												06h 11.5 11h 17
												07h 12 12h 17.5
												08h 12.5 13h 18
												07h 12 14h 18.5
												08h 12.5 15h 19
												09h 13 16h 19.5
												0Ah 13.5 17h 20
												0Bh 14 Other NA
												0Ch 14.5

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Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source driving voltage A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V. C[7:0] = 32h [POR], VSL at -15V
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		Remark: VSH1>=VSH2

A[7]/B[7] = 1,
VSH1/VSH2 voltage setting from 2.4V
to 8.8V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
8Eh	2.4	AFh	5.7
8Fh	2.5	B0h	5.8
90h	2.6	B1h	5.9
91h	2.7	B2h	6
92h	2.8	B3h	6.1
93h	2.9	B4h	6.2
94h	3	B5h	6.3
95h	3.1	B6h	6.4
96h	3.2	B7h	6.5
97h	3.3	B8h	6.6
98h	3.4	B9h	6.7
99h	3.5	BAh	6.8
9Ah	3.6	BBh	6.9
9Bh	3.7	BCh	7
9Ch	3.8	BDh	7.1
9Dh	3.9	BEh	7.2
9Eh	4	BFh	7.3
9Fh	4.1	C0h	7.4
A0h	4.2	C1h	7.5
A1h	4.3	C2h	7.6
A2h	4.4	C3h	7.7
A3h	4.5	C4h	7.8
A4h	4.6	C5h	7.9
A5h	4.7	C6h	8
A6h	4.8	C7h	8.1
A7h	4.9	C8h	8.2
A8h	5	C9h	8.3
A9h	5.1	CAh	8.4
AAh	5.2	CBh	8.5
ABh	5.3	CCh	8.6
ACh	5.4	CDh	8.7
ADh	5.5	CEh	8.8
AEh	5.6	Other	NA

A[7]/B[7] = 0,
VSH1/VSH2 voltage setting from 9V
to 17V

A/B[7:0]	VSH1/VSH2	A/B[7:0]	VSH1/VSH2
23h	9	3Ch	14
24h	9.2	3Dh	14.2
25h	9.4	3Eh	14.4
26h	9.6	3Fh	14.6
27h	9.8	40h	14.8
28h	10	41h	15
29h	10.2	42h	15.2
2Ah	10.4	43h	15.4
2Bh	10.6	44h	15.6
2Ch	10.8	45h	15.8
2Dh	11	46h	16
2Eh	11.2	47h	16.2
2Fh	11.4	48h	16.4
30h	11.6	49h	16.6
31h	11.8	4Ah	16.8
32h	12	4Bh	17
33h	12.2	Other	NA
34h	12.4		
35h	12.6		
36h	12.8		
37h	13		
38h	13.2		
39h	13.4		
3Ah	13.6		
3Bh	13.8		

C[7:0]	VSL
0Ah	-5
0Ch	-5.5
0Eh	-6
10h	-6.5
12h	-7
14h	-7.5
16h	-8
18h	-8.5
1Ah	-9
1Ch	-9.5
1Eh	-10
20h	-10.5
22h	-11
24h	-11.5
26h	-12
28h	-12.5
2Ah	-13
2Ch	-13.5
2Eh	-14
30h	-14.5
32h	-15
34h	-15.5
36h	-16
38h	-16.5
3Ah	-17
Other	NA

0	0	08	0	0	0	0	1	0	0	0	Initial Code Setting OTP Program	Program Initial Code Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
---	---	----	---	---	---	---	---	---	---	---	-------------------------------------	--

0	0	09	0	0	0	0	1	0	0	1	Write Register for Initial Code Setting	Write Register for Initial Code Setting Selection A[7:0] ~ D[7:0]: Reserved Details refer to Application Notes of Initial Code Setting
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
0	0	0A	0	0	0	0	1	0	1	0	Read Register for Initial Code Setting	Read Register for Initial Code Setting

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Command Table

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																												
0	0	0C	0	0	0	0	1	1	0	0	Booster Soft start Control	Booster Enable with Phase 1, Phase 2 and Phase 3 for soft start current and duration setting.																												
0	1			1	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁		A[7:0] -> Soft start setting for Phase1 = 8Bh [POR]																												
0	1			1	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁		B[7:0] -> Soft start setting for Phase2 = 9Ch [POR]																												
0	1			1	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁		C[7:0] -> Soft start setting for Phase3 = 96h [POR]																												
0	1		0	0	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D[7:0] -> Duration setting = 0Fh [POR]																												
Bit Description of each byte: A[6:0] / B[6:0] / C[6:0]:																																								
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Bit[6:4]</th><th style="text-align: center;">Driving Strength Selection</th></tr> </thead> <tbody> <tr><td style="text-align: center;">000</td><td style="text-align: center;">1(Weakest)</td></tr> <tr><td style="text-align: center;">001</td><td style="text-align: center;">2</td></tr> <tr><td style="text-align: center;">010</td><td style="text-align: center;">3</td></tr> <tr><td style="text-align: center;">011</td><td style="text-align: center;">4</td></tr> <tr><td style="text-align: center;">100</td><td style="text-align: center;">5</td></tr> <tr><td style="text-align: center;">101</td><td style="text-align: center;">6</td></tr> <tr><td style="text-align: center;">110</td><td style="text-align: center;">7</td></tr> <tr><td style="text-align: center;">111</td><td style="text-align: center;">8(Strongest)</td></tr> </tbody> </table>													Bit[6:4]	Driving Strength Selection	000	1(Weakest)	001	2	010	3	011	4	100	5	101	6	110	7	111	8(Strongest)										
Bit[6:4]	Driving Strength Selection																																							
000	1(Weakest)																																							
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111	8(Strongest)																																							
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Bit[3:0]</th><th style="text-align: center;">Min Off Time Setting of GDR [Time unit]</th></tr> </thead> <tbody> <tr><td style="text-align: center;">0000 ~ 0011</td><td style="text-align: center;">NA</td></tr> <tr><td style="text-align: center;">0100</td><td style="text-align: center;">2.6</td></tr> <tr><td style="text-align: center;">0101</td><td style="text-align: center;">3.2</td></tr> <tr><td style="text-align: center;">0110</td><td style="text-align: center;">3.9</td></tr> <tr><td style="text-align: center;">0111</td><td style="text-align: center;">4.6</td></tr> <tr><td style="text-align: center;">1000</td><td style="text-align: center;">5.4</td></tr> <tr><td style="text-align: center;">1001</td><td style="text-align: center;">6.3</td></tr> <tr><td style="text-align: center;">1010</td><td style="text-align: center;">7.3</td></tr> <tr><td style="text-align: center;">1011</td><td style="text-align: center;">8.4</td></tr> <tr><td style="text-align: center;">1100</td><td style="text-align: center;">9.8</td></tr> <tr><td style="text-align: center;">1101</td><td style="text-align: center;">11.5</td></tr> <tr><td style="text-align: center;">1110</td><td style="text-align: center;">13.8</td></tr> <tr><td style="text-align: center;">1111</td><td style="text-align: center;">16.5</td></tr> </tbody> </table>													Bit[3:0]	Min Off Time Setting of GDR [Time unit]	0000 ~ 0011	NA	0100	2.6	0101	3.2	0110	3.9	0111	4.6	1000	5.4	1001	6.3	1010	7.3	1011	8.4	1100	9.8	1101	11.5	1110	13.8	1111	16.5
Bit[3:0]	Min Off Time Setting of GDR [Time unit]																																							
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1111	16.5																																							
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Bit[1:0]</th><th style="text-align: center;">Duration of Phase [Approximation]</th></tr> </thead> <tbody> <tr><td style="text-align: center;">00</td><td style="text-align: center;">10ms</td></tr> <tr><td style="text-align: center;">01</td><td style="text-align: center;">20ms</td></tr> <tr><td style="text-align: center;">10</td><td style="text-align: center;">30ms</td></tr> <tr><td style="text-align: center;">11</td><td style="text-align: center;">40ms</td></tr> </tbody> </table>													Bit[1:0]	Duration of Phase [Approximation]	00	10ms	01	20ms	10	30ms	11	40ms																		
Bit[1:0]	Duration of Phase [Approximation]																																							
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11	40ms																																							
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep mode	Deep Sleep mode Control:																												
0	1		0	0	0	0	0	0	A ₁	A ₀		<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">A[1:0] :</th><th style="text-align: center;">Description</th></tr> </thead> <tbody> <tr><td style="text-align: center;">00</td><td style="text-align: center;">Normal Mode [POR]</td></tr> <tr><td style="text-align: center;">01</td><td style="text-align: center;">Enter Deep Sleep Mode 1</td></tr> <tr><td style="text-align: center;">11</td><td style="text-align: center;">Enter Deep Sleep Mode 2</td></tr> </tbody> </table> <p>After this command initiated, the chip will enter Deep Sleep Mode, BUSY pad will keep output high. Remark: To Exit Deep Sleep mode, User required to send HWRESET to the driver</p>	A[1:0] :	Description	00	Normal Mode [POR]	01	Enter Deep Sleep Mode 1	11	Enter Deep Sleep Mode 2																				
A[1:0] :	Description																																							
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0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence A[2:0] = 011 [POR]
0	1		0	0	0	0	0	A ₂	A ₁	A ₀	A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR]	
											A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated in the Y direction.	
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection A[7:0] = 00h [POR] The command required CLKEN=1 and ANALOGEN=1. Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀	A[6:4]=n for cool down duration: 10ms x (n+1) A[2:0]=m for number of Cool Down Loop to detect. The max HV ready duration is 10ms x (n+1) x (m) HV ready detection will be trigger after each cool down time. The detection will be completed when HV is ready. For 1 shot HV ready detection, A[7:0] can be set as 00h.	

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0	0	15	0	0	0	1	0	1	0	1	VCI Detection	VCI Detection A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect														
0	1		0	0	0	0	0	A ₂	A ₁	A ₀		<table border="1"> <tr><td>A[2:0]</td><td>VCI level</td></tr> <tr><td>011</td><td>2.2V</td></tr> <tr><td>100</td><td>2.3V</td></tr> <tr><td>101</td><td>2.4V</td></tr> <tr><td>110</td><td>2.5V</td></tr> <tr><td>111</td><td>2.6V</td></tr> <tr><td>Other</td><td>NA</td></tr> </table>	A[2:0]	VCI level	011	2.2V	100	2.3V	101	2.4V	110	2.5V	111	2.6V	Other	NA
A[2:0]	VCI level																									
011	2.2V																									
100	2.3V																									
101	2.4V																									
110	2.5V																									
111	2.6V																									
Other	NA																									
The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail.																										
After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).																										
0	0	18	0	0	0	1	1	0	0	0	Temperature Sensor Control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor														
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0] = 7FFh [POR]														
0	1		A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄																
0	1		A ₃	A ₂	A ₁	A ₀	0	0	0	0																
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.														
1	1		A ₁₁	A ₁₀	A ₉	A ₈	A ₇	A ₆	A ₅	A ₄																
1	1		A ₃	A ₂	A ₁	A ₀	0	0	0	0																
0	0	1C	0	0	0	1	1	1	0	0	Temperature Sensor Control (Write Command to External temperature sensor)	Write Command to External temperature sensor. A[7:0] = 00h [POR], B[7:0] = 00h [POR], C[7:0] = 00h [POR],														
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀																
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀																
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀																
<table border="1"> <tr><td>A[7:6]</td><td>Select no of byte to be sent</td></tr> <tr><td>00</td><td>Address + pointer</td></tr> <tr><td>01</td><td>Address + pointer + 1st parameter</td></tr> <tr><td>10</td><td>Address + pointer + 1st parameter + 2nd pointer</td></tr> <tr><td>11</td><td>Address</td></tr> </table> A[5:0] – Pointer Setting B[7:0] – 1 st parameter C[7:0] – 2 nd parameter The command required CLKEN=1. Refer to Register 0x22 for detail.												A[7:6]	Select no of byte to be sent	00	Address + pointer	01	Address + pointer + 1st parameter	10	Address + pointer + 1st parameter + 2nd pointer	11	Address					
A[7:6]	Select no of byte to be sent																									
00	Address + pointer																									
01	Address + pointer + 1st parameter																									
10	Address + pointer + 1st parameter + 2nd pointer																									
11	Address																									
After this command initiated, Write Command to external temperature sensor starts. BUSY pad will output high during operation.																										
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence The Display Update Sequence Option is located at R22h. BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.														

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0	0	21	0	0	1	0	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] B[7:0] = 00h [POR]
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀			A[7:4] Red RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content
0	1		B ₇	0	0	0	0	0	0	0	0		A[3:0] BW RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content
													B[7] Source Output Mode 0 Available Source from S0 to S175 1 Available Source from S8 to S167
0	0	22	0	0	1	0	0	0	1	0	A ₀	Display Update Control 2	Display Update Sequence Option: Enable the stage for Master Activation A[7:0]=FFh (POR)
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀			Operating sequence Parameter (in Hex) Enable clock signal 80 Disable clock signal 01 Enable clock signal → Enable Analog C0 Disable Analog → Disable clock signal 03 Enable clock signal → Load LUT with DISPLAY Mode 1 → Disable clock signal 91 Enable clock signal → Load LUT with DISPLAY Mode 2 → Disable clock signal 99 Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 1 → Disable clock signal B1 Enable clock signal → Load temperature value → Load LUT with DISPLAY Mode 2 → Disable clock signal B9 Enable clock signal → Enable Analog → Display with DISPLAY Mode 1 → Disable Analog → Disable OSC C7 Enable clock signal → Enable Analog → Display with DISPLAY Mode 2 → Disable Analog → Disable OSC CF Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 1 → Disable Analog → Disable OSC F7 Enable clock signal → Enable Analog → Load temperature value → DISPLAY with DISPLAY Mode 2 → Disable Analog → Disable OSC FF
0	0	24	0	0	1	0	0	1	0	0		Write RAM (Black White) / RAM 0x24	After this command, data entries will be written into the BW RAM until another command is written. Address pointers will advance accordingly For Write pixel: Content of Write RAM(BW) = 1 For Black pixel: Content of Write RAM(BW) = 0

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	26	0	0	1	0	0	1	1	0	Write RAM (RED) / RAM 0x26	After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly. For Red pixel: Content of Write RAM(RED) = 1 For non-Red pixel [Black or White]: Content of Write RAM(RED) = 0
0	0	27	0	0	1	0	0	1	1	1	Read RAM	After this command, data read on the MCU bus will fetch data from RAM. According to parameter of Register 41h to select reading RAM0x24/ RAM0x26, until another command is written. Address pointers will advance accordingly. The 1 st byte of data read is dummy data.
0	0	28	0	0	1	0	1	0	0	0	VCOM Sense	Enter VCOM sensing conditions and hold for duration defined in 29h before reading VCOM value. The sensed VCOM voltage is stored in register The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	29	0	0	1	0	1	0	0	1	VCOM Sense Duration	Stabiling time between entering VCOM sensing mode and reading acquired. A[3:0] = 9h, duration = 10s. VCOM sense duration = (A[3:0]+1) sec
0	0	2A	0	0	1	0	1	0	1	0	Program VCOM OTP	Program VCOM register into OTP The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	2B	0	0	1	0	1	0	1	1	Write Register for VCOM Control	This command is used to reduce glitch when ACVCOM toggle. Two data bytes D04h and D63h should be set for this command.

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R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description																																																																
0	0	2C	0	0	1	0	1	1	0	0	Write VCOM register	Write VCOM register from MCU interface A[7:0] = 00h [POR]																																																																
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		<table border="1"> <tr><td>A[7:0]</td><td>VCOM</td><td>A[7:0]</td><td>VCOM</td></tr> <tr><td>08h</td><td>-0.2</td><td>44h</td><td>-1.7</td></tr> <tr><td>0Ch</td><td>-0.3</td><td>48h</td><td>-1.8</td></tr> <tr><td>10h</td><td>-0.4</td><td>4Ch</td><td>-1.9</td></tr> <tr><td>14h</td><td>-0.5</td><td>50h</td><td>-2</td></tr> <tr><td>18h</td><td>-0.6</td><td>54h</td><td>-2.1</td></tr> <tr><td>1Ch</td><td>-0.7</td><td>58h</td><td>-2.2</td></tr> <tr><td>20h</td><td>-0.8</td><td>5Ch</td><td>-2.3</td></tr> <tr><td>24h</td><td>-0.9</td><td>60h</td><td>-2.4</td></tr> <tr><td>28h</td><td>-1</td><td>64h</td><td>-2.5</td></tr> <tr><td>2Ch</td><td>-1.1</td><td>68h</td><td>-2.6</td></tr> <tr><td>30h</td><td>-1.2</td><td>6Ch</td><td>-2.7</td></tr> <tr><td>34h</td><td>-1.3</td><td>70h</td><td>-2.8</td></tr> <tr><td>38h</td><td>-1.4</td><td>74h</td><td>-2.9</td></tr> <tr><td>3Ch</td><td>-1.5</td><td>78h</td><td>-3</td></tr> <tr><td>40h</td><td>-1.6</td><td>Other</td><td>NA</td></tr> </table>	A[7:0]	VCOM	A[7:0]	VCOM	08h	-0.2	44h	-1.7	0Ch	-0.3	48h	-1.8	10h	-0.4	4Ch	-1.9	14h	-0.5	50h	-2	18h	-0.6	54h	-2.1	1Ch	-0.7	58h	-2.2	20h	-0.8	5Ch	-2.3	24h	-0.9	60h	-2.4	28h	-1	64h	-2.5	2Ch	-1.1	68h	-2.6	30h	-1.2	6Ch	-2.7	34h	-1.3	70h	-2.8	38h	-1.4	74h	-2.9	3Ch	-1.5	78h	-3	40h	-1.6	Other	NA
A[7:0]	VCOM	A[7:0]	VCOM																																																																									
08h	-0.2	44h	-1.7																																																																									
0Ch	-0.3	48h	-1.8																																																																									
10h	-0.4	4Ch	-1.9																																																																									
14h	-0.5	50h	-2																																																																									
18h	-0.6	54h	-2.1																																																																									
1Ch	-0.7	58h	-2.2																																																																									
20h	-0.8	5Ch	-2.3																																																																									
24h	-0.9	60h	-2.4																																																																									
28h	-1	64h	-2.5																																																																									
2Ch	-1.1	68h	-2.6																																																																									
30h	-1.2	6Ch	-2.7																																																																									
34h	-1.3	70h	-2.8																																																																									
38h	-1.4	74h	-2.9																																																																									
3Ch	-1.5	78h	-3																																																																									
40h	-1.6	Other	NA																																																																									
0	0	2D	0	0	1	0	1	1	0	1	OTP Register Read for Display Option	Read Register for Display Option: A[7:0]: VCOM OTP Selection (Command 0x37, Byte A) B[7:0]: VCOM Register (Command 0x2C) C[7:0]~G[7:0]: Display Mode (Command 0x37, Byte B to Byte F) [5 bytes] H[7:0]~K[7:0]: Waveform Version (Command 0x37, Byte G to Byte J) [4 bytes]																																																																
0	0	2E	0	0	1	0	1	1	1	0	User ID Read	Read 10 Byte User ID stored in OTP: A[7:0]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]																																																																
0	0	2F	0	0	1	0	1	1	1	1	Status Bit Read	Read IC status Bit [POR 0x01] A[5]: HV Ready Detection flag [POR=0] 0: Ready 1: Not Ready A[4]: VCI Detection flag [POR=0] 0: Normal 1: VCI lower than the Detect level A[3]: [POR=0] A[2]: Busy flag [POR=0] 0: Normal 1: BUSY A[1:0]: Chip ID [POR=01] Remark: A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.																																																																

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0	0	30	0	0	1	1	0	0	0	0	Program WS OTP	Program OTP of Waveform Setting The contents should be written into RAM before sending this command. The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	31	0	0	1	1	0	0	0	1	Load WS OTP	Load OTP of Waveform Setting The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [153 bytes], which contains the content of VS[nX-LUTm], TP[nX], RP[n], SR[nXY], FR[n] and XON[nXY] Refer to Session 6.7 WAVEFORM SETTING
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		:	:	:	:	:	:	:	:		
0	1			
0	0	34	0	0	1	1	0	1	0	0	CRC calculation	CRC calculation command For details, please refer to SSD1680 application note. BUSY pad will output high during operation.
0	0	35	0	0	1	1	0	1	0	1	CRC Status Read	CRC Status Read A[15:0] is the CRC read out value
1	1		A ₁₅	A ₁₄	A ₁₃	A ₁₂	A ₁₁	A ₁₀	A ₉	A ₈		
1	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	36	0	0	1	1	0	1	1	0	Program OTP selection	Program OTP Selection according to the OTP Selection Control [R37h and R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation.
0	0	37	0	0	1	1	0	1	1	1	Write Register for Display Option	Write Register for Display Option A[7] Spare VCOM OTP selection 0: Default [POR] 1: Spare B[7:0] Display Mode for WS[7:0] C[7:0] Display Mode for WS[15:8] D[7:0] Display Mode for WS[23:16] E[7:0] Display Mode for WS[31:24] F[3:0] Display Mode for WS[35:32] 0: Display Mode 1 1: Display Mode 2 F[6]: PingPong for Display Mode 2 0: RAM Ping-Pong disable [POR] 1: RAM Ping-Pong enable G[7:0]~J[7:0] module ID /waveform version. Remarks: 1) A[7:0]-J[7:0] can be stored in OTP 2) RAM Ping-Pong function is not support for Display Mode 1
0	1		J ₇	J ₆	J ₅	J ₄	J ₃	J ₂	J ₁	J ₀		

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0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]~J[7:0]: UserID [10 bytes]
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀	Remarks: A[7:0]~J[7:0] can be stored in OTP	
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		
0	1		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
0	1		E ₇	E ₆	E ₅	E ₄	E ₃	E ₂	E ₁	E ₀		
0	1		F ₇	F ₆	F ₅	F ₄	F ₃	F ₂	F ₁	F ₀		
0	1		G ₇	G ₆	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀		
0	1		H ₇	H ₆	H ₅	H ₄	H ₃	H ₂	H ₁	H ₀		
0	1		I ₇	I ₆	I ₅	I ₄	I ₃	I ₂	I ₁	I ₀		
0	1		J ₇	J ₆	J ₅	J ₄	J ₃	J ₂	J ₁	J ₀		
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 00: Normal Mode [POR] A[1:0] = 11: Internal generated OTP programming voltage
0	1		0	0	0	0	0	0	A ₁	A ₀		Remark: User is required to EXACTLY follow the reference code sequences
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A[7:0] = C0h [POR], set VBD as HiZ. A[7:6] :Select VBD option
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		A[7:6] Select VBD as 00 GS Transition, Defined in A[2] and A[1:0] 01 Fix Level, Defined in A[5:4] 10 VCOM 11[POR] HiZ
												A[5:4] Fix Level Setting for VBD A[5:4] VBD level 00 VSS 01 VSH1 10 VSL 11 VSH2
												A[2] GS Transition control A[2] GS Transition control 0 Follow LUT (Output VCOM @ RED) 1 Follow LUT
												A[1:0] GS Transition setting for VBD A[1:0] VBD Transition 00 LUT0 01 LUT1 10 LUT2 11 LUT3
0	0	3F	0	0	1	1	1	1	1	1	End Option (EOPT)	Option for LUT end A[7:0]= 02h [POR]
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		22h Normal. 07h Source output level keep previous output before power off
0	0	41	0	1	0	0	0	0	0	1	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to RAM0x24 1 : Read RAM corresponding to RAM0x26
0	1		0	0	0	0	0	0	0	A ₀		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit for RAM
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[5:0]: XSA[5:0], XStart, POR = 00h B[5:0]: XEA[5:0], XEnd, POR = 15h
0	1		0	0	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		

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0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit for RAM A[8:0]: YSA[8:0], YStart, POR = 000h B[8:0]: YEA[8:0], YEnd, POR = 127h
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		0	0	0	0	0	0	0	A ₈		
0	1		B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		
0	1		0	0	0	0	0	0	0	B ₈		
0	0	46	0	1	0	0	0	1	1	0	Auto Write RED RAM for Regular Pattern	Auto Write RED RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source BUSY pad will output high during operation.
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		
0	0	47	0	1	0	0	0	1	1	1	Auto Write B/W RAM for Regular Pattern	Auto Write B/W RAM for Regular Pattern A[7:0] = 00h [POR] A[7]: The 1st step value, POR = 0 A[6:4]: Step Height, POR= 000 Step of alter RAM in Y-direction according to Gate A[2:0]: Step Width, POR= 000 Step of alter RAM in X-direction according to Source During operation, BUSY pad will output high.
0	1		A ₇	A ₆	A ₅	A ₄	0	A ₂	A ₁	A ₀		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X address counter	Make initial settings for the RAM X address in the address counter (AC) A[5:0]: 00h [POR].
0	1		0	0	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0]: 000h [POR].
0	1		A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	1		0	0	0	0	0	0	0	A ₈		
0	0	7F	0	1	1	1	1	1	1	1	NOP	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read Commands.

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8. Optical Specifications

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	Indoor	8:1		-		8-2
GN	2Grey Level	-		DS+(WS-DS)*n(m-1)			8-3
T update	Image update time	at 25 °C		3	-	sec	
Life		Topr		1000000times or 5years			

Notes: 8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3 WS: White state, DS: Dark state

9. Handling, Safety and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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10.Reliability test

NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=70° C, RH=40%, 240h Test in white pattern
3	High-Temperature Operation	T=50° C, RH=35%, 240h
4	Low-Temperature Operation	0° C, 240h
5	High-Temperature, High-Humidity Operation	T=40° C, RH=80%, 240h
6	High Temperature, High Humidity Storage	T=50° C, RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25° C 30min]→[+70 ° C 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m ² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell, not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display, no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display, including IC and FPC area)

Note: Put in normal temperature for 1hour after test finished, display performance is ok.

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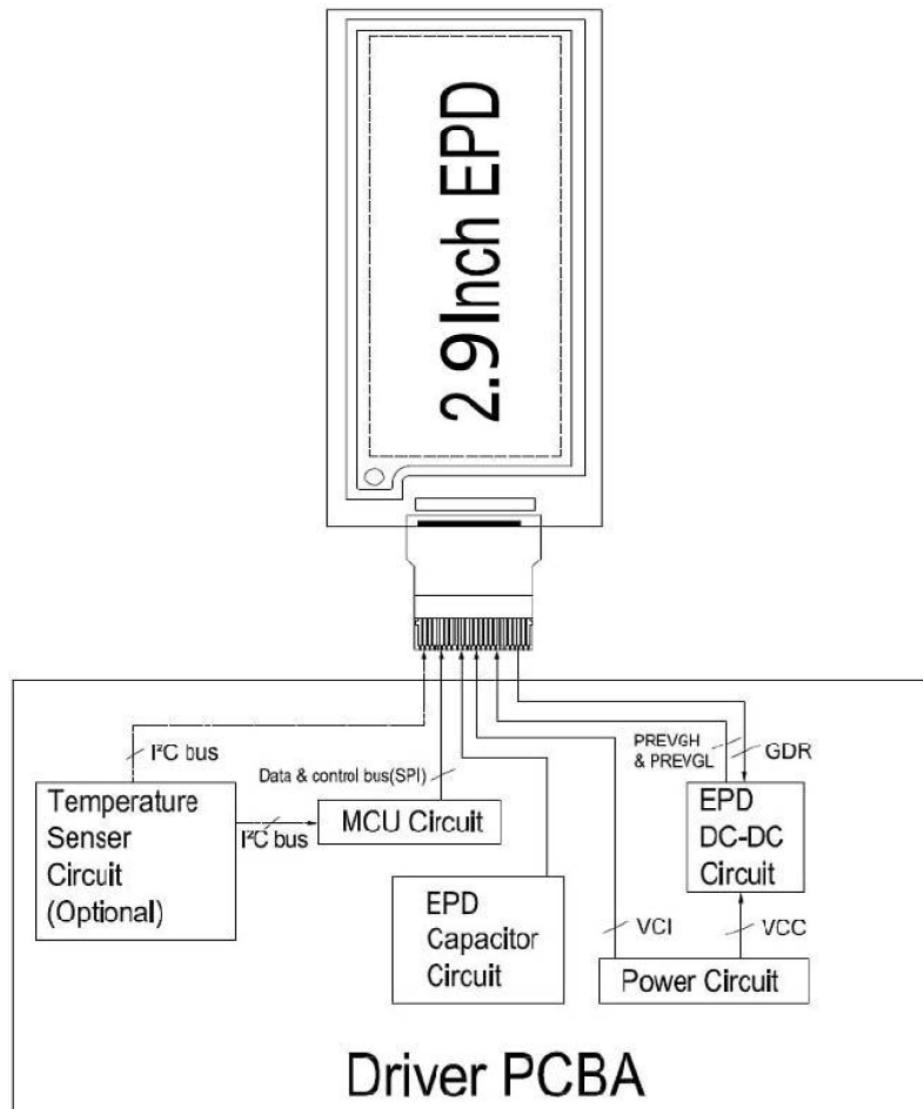


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11. Block Diagram



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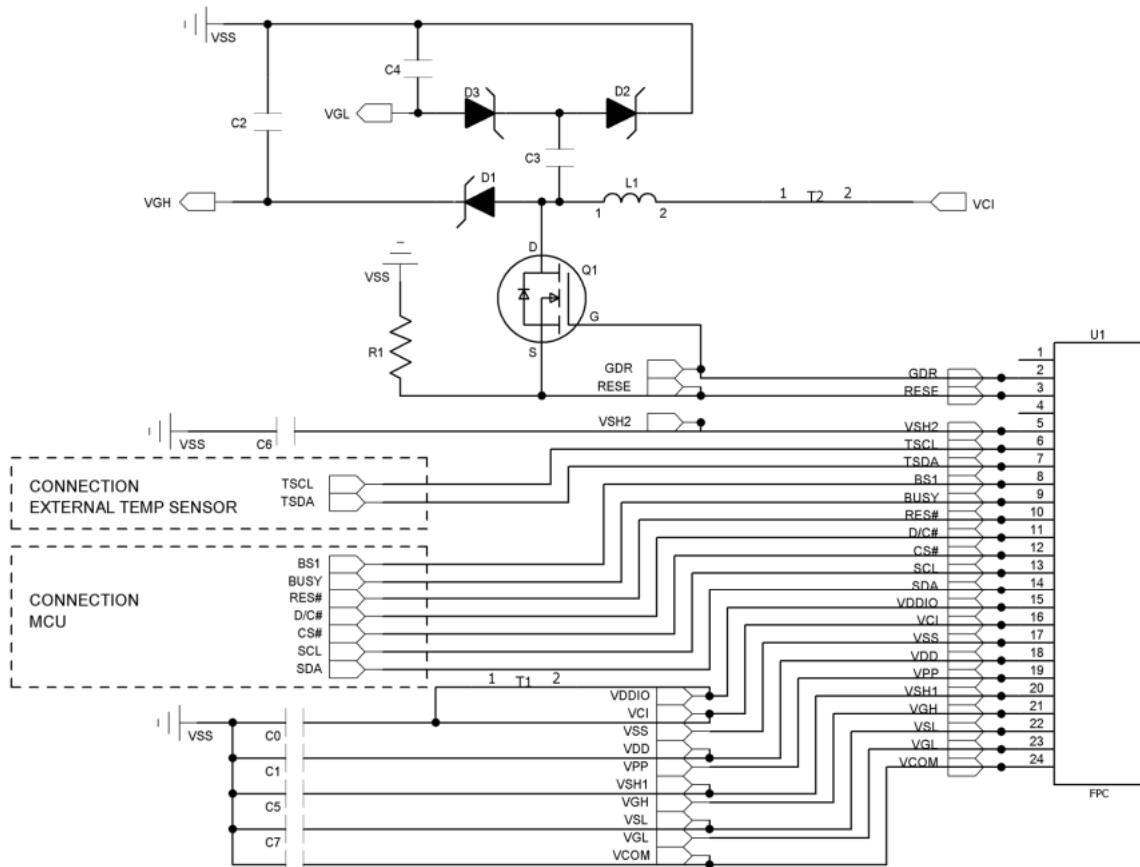


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12. Typical Application Circuit with SPI Interface



Part Name	Value	Requirements/Reference Part
C0-C1	1uF	X5R/X7R; Voltage Rating : 6V or 25V
C2-C7	1uF	0402/0603/0805; X5R/X7R; Voltage Rating : 25V
C8	0.47uF, 1uF	0603/0805; X7R; Voltage Rating : 25V Note: Effective capacitance > 0.25uF @ 18V DC bias
R1	2.2 ohm	0402, 0603, 0805; 1% variation, $\geq 0.05W$
D1-D3	Diode	MBR0530 1) Reverse DC voltage $\geq 30V$ 2) $I_{o} \geq 500mA$ 3) Forward voltage $\leq 430mV$
Q1	NMOS	Si1304BDL/NX3008NBK 1) Drain-Source breakdown voltage $\geq 30V$ 2) $V_{gs(th)} = 0.9V$ (Typ), $1.3V$ (Max) 3) $R_{ds(on)} \leq 2.1\Omega$ @ $V_{gs} = 2.5V$
L1	47uH	CDRH2D18 / LDNP-470NC $I_{o} = 500mA$ (Max)
U1	0.5mm ZIF socket	24pins, 0.5mm pitch

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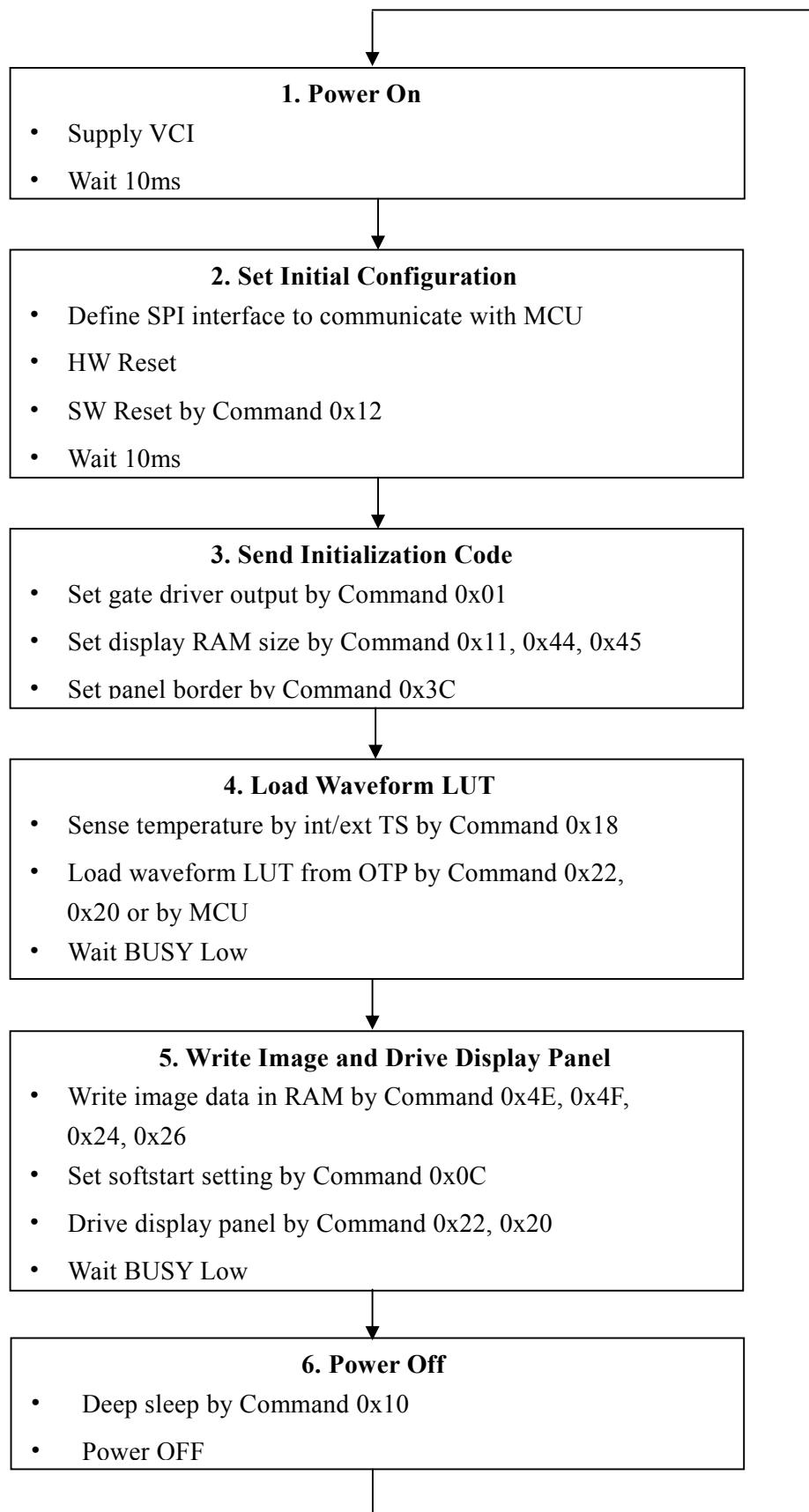
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13. Typical Operating Sequence

13.1 Normal Operation Flow



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13.2 Normal Operation Reference Program Code

TBD

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14. Part Number Definition

TBD

15. Inspection condition

15. 1 Environment

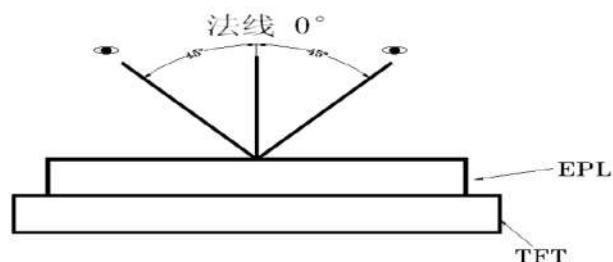
Temperature : $25\pm3^{\circ}\text{C}$

Humidity : $55\pm10\%\text{RH}$

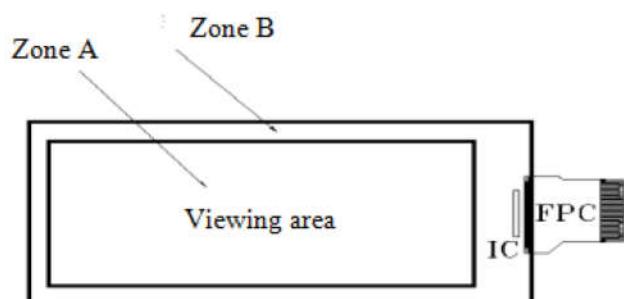
15. 2 Illuminance

Brightness:1200 ~ 1500LUX;distance:20-30CM;Angle:Relate 30°surround.

15.3 Inspection method



15. 4 Display area



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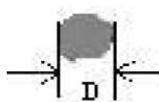
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15.5 Inspection standard

15.5.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Display complete Display uniform	MA		
2	Black/White spots	 D≤0.25mm, Allowed 0.25mm<D≤0.4mm。N≤3, and Distance≥5mm 0.4mm<D Not Allow	MI	Visual inspection	
3	Black/White spots (No switch)	 L≤0.6mm, W≤0.2mm, N≤1 L≤2.0mm,W>0.2mm, Not Allow L>0.6mm, Not Allow		Visual/ Inspection card	Zone A
4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash spots/ Larger FPL size	Flash spots in switching, Allowed FPL size larger than viewing area, Allowed	MI	Visual/ Inspection card	Zone A Zone B
6	Display wrong/Missing	All appointed displays are showed correct	MA	Visual inspection	Zone A
7	Short circuit/ Circuit break/ Display abnormal	Not Allow			

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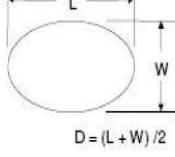
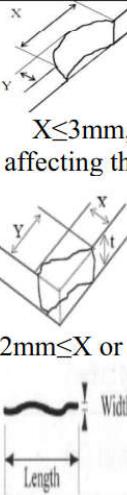


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15.5.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 <p>D≤0.25mm, Allowed 0.25mm<D≤0.4mm, N≤3 D>0.4mm, Not Allow</p>	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A
3	Dirty	Allowed if can be removed			Zone B
4	Chips/Scratch/ Edge crown	 <p>X≤3mm, Y≤0.5mm And without affecting the electrode is permissible 2mm≤X or 2mm≤Y Not Allow W≤0.1mm, L≤5mm, No harm to the electrodes and N≤2 allow</p>	MI	Visual / Microscope	Zone A Zone B
5	TFT Cracks	 <p>Not Allow</p>	MA	Visual / Microscope	Zone A Zone B
6	Dirty/ foreign body	Allowed if can be removed/ allow	MI	Visual / Microscope	Zone A / Zone B
7	FPC broken/ Goldfingers oxidation/ scratch	 <p>Not Allow</p>	MA	Visual / Microscope	Zone B

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8	TFT edge bulge /TFT chromatic aberration	TFT edge bulge: X≤3mm, Y≤0.3mm Allowed TFT chromatic aberration :Allowed	MI	Visual / Microscope	Zone A Zone B
9	PCB damaged/ Poor welding/ Curl	PCB (Circuit area) damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%			
10	Edge glue height/ Edge glue bubble	Edge Adhesives H≤PS surface (Including protect film) Edge adhesives seep in≤1/2 Margin width Length excluding Edge adhesives bubble: bubble Width ≤1/2 Margin width; Length ≤0.5mm。n≤5	MI	Visual / Ruler	Zone B
11	Protect film	Surface scratch but not effect protect function, Allowed			
12	Silicon glue	Thickness≤PS surface(With protect film): Full cover the IC; Shape: The width on the FPC ≤ 0.5mm (Front) The width on the FPC≤1.0mm (Back) smooth surface,No obvious raised.	MI	Visual Inspection	
13	Warp degree (TFT substrate)	t≤2.0mm	MI	Ruler	
14	Color difference in COM area (Silver point area)	Allowed		Visual Inspection	

DATE FEB.14.2022

Version

1.1

TECHNICAL SPECIFICATION

EPD

ZHONGJINGYUAN

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ZHONGJINGYUAN

郑州中景园电子技术有限公司

商城地址 : <https://zjy-display.taobao.com> TEL : 18601955397

16.Packaging

CUSTOMER'S APPROVED:

DATE: 2020.01.02

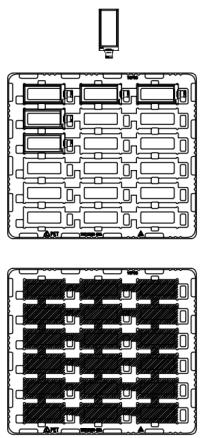
PAGE: 1/1

PRODUCT PART NO.: YMS128296-029

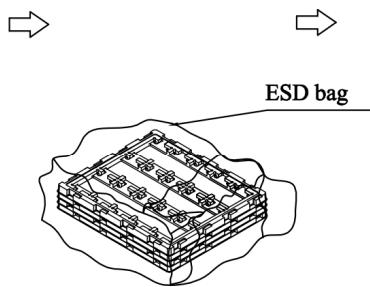
PACKING TYPE: BY PET TRAY(TPET128296-029A)

PACKLING ORDER:

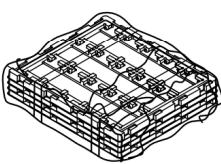
- 1) Putting 18 pcs Modules on each PET tray. And cover a dedicated EPE film.



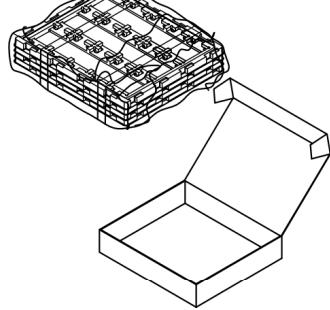
- 2) Putting 9 pcs PET trays together with 1 empty tray on the top of PET tray. Insert in the ESD bag, add desiccant in the ESD bag.



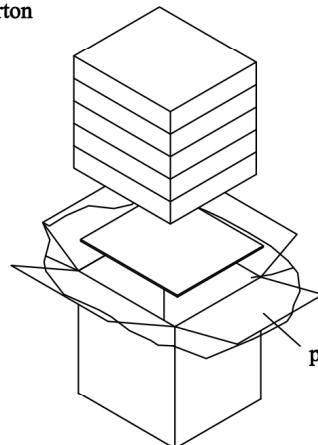
- 3) the tray together with rubber band



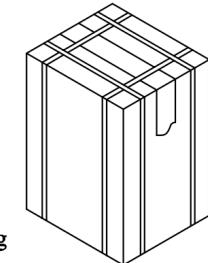
- 4) Putting in the inner small carton



- 5) Putting 5 small cartons into one outcarton



- 6) Packing finished



Note: 18 pcs in a tray, 9 trays in a inner carton, 5 inner cartons in a out carton, so $18 \times 9 \times 5 = 810$ pcs/Outcarton

Dimension (Small carton): 385*325*87mm

Dimension (Out carton): 394*344*470mm

NO. YMS128296-029

Ver. 1 Drw:

Chk:

Apv:

NEWFACE Optoelectronics Co.,Ltd

DATE FEB.14.2022

Version

1.1

TECHNICAL SPECIFICATION

EPD

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