MSP430F552x、MSP430F551x 混合信号微控制器

1 器件概述

1.1 特性

- 低电源电压范围：
  从 3.6V 低至 1.8V
- 超低功耗
  - 激活模式 (AM)：
    - 所有系统时钟激活：
      - 8MHz 时为 290µA/MHz、3.0V、闪存程序执行（典型值）
      - 8MHz 时为 150µA/MHz、3.0V、RAM 程序执行（典型值）
  - 待机模式 (LPM3)：
    - 含晶体的实时时钟 (RTC)、看门狗、电源监控器可用、完全 RAM 保持、快速唤醒：
      - 2.2V 时为 1.9µA，3.0V 时为 2.1µA（典型值）
    - 低功耗振荡器 (VLO)、通用计数器、看门狗、电源监控器可用、完全 RAM 保持、快速唤醒：
      - 3.0V 时为 1.4µA（典型值）
  - 关闭模式 (LPM4)：
    - 完全 RAM 保持、电源监视器可用、快速唤醒：
      - 3.0V 时为 1.1µA（典型值）
  - 关断模式 (LPM4.5)：
    - 3.0V 时为 0.18µA（典型值）
- 在 3.5µs（典型值）内从待机模式唤醒
- 16 位精简指令集计算机 (RISC) 架构，扩展内存，高达 25MHz 的系统时钟
- 灵活的电源管理系统
  - 内置可编程的低压降稳压器 (LDO)
  - 电源电压监控、监视和临时限电
- 统一时钟系统
  - 针对频率稳定的锁相环 (FLL) 控制环路
  - 低功耗低频内部时钟源 (VLO)
  - 低频修整内部基准源 (REFO)
  - 32kHz 手表晶振 (XT1)
  - 高达 32MHz 的高频晶振 (XT2)
- 具有 5 个捕捉/比较寄存器的 16 位定时器 TA0，Timer_A
- 具有 3 个捕捉/比较寄存器的 16 位定时器 TA1，Timer_A
- 具有 3 个捕捉/比较寄存器的 16 位定时器 TA2，Timer_A
- 具有 7 个捕捉/比较影子寄存器的 16 位定时器 TB0，Timer_B
- 2 个通用串行通信接口
  - USCI_A0 和 USCI_A1 均支持：
    - 增强型通用异步收发器 (UART) 支持自动波特率检测
    - IrDA 编码和解码
    - 同步串行外设接口 (SPI)
  - USCI_B0 和 USCI_B1 每个都支持：
    - I^{2}C
    - 同步串行外设接口 (SPI)
- 全速通用串行总线 (USB)
  - 集成的 USB - 物理层 (PHY)
  - 集成 3.3V 和 1.8V USB 电源系统
  - 集成 USB- 锁相环 (PLL)
  - 8 输入和 8 输出端点
- 具有内部基准、采样保持和自动扫描功能的 12 位模数转换器 (ADC)（仅限 MSP430F552x）
- 比较器
- 硬件乘法器支持 32 位运算
- 串行板上编程，无需外部编程电压
- 3 通道内部 DMA
- 具有 RTC 特性的基本计时器
- 器件比较 总结了可用的系列产品成员

1.2 应用范围

- 模拟和数字传感器系统
- 数据记录器
- 连接到 USB 主机

1.3 说明

TI 的 MSP430™系列的超低功耗微控制器包含数个采用外设集的器件，可广泛应用于各种 应用。此架构与多种低功耗模式配合使用，是延长便携式测量应用电池寿命的最优 选择。该微控制器 具有 一个强大的 16 位精简指令集 (RISC) CPU，使用 16 位寄存器以及常数发生器，以便获得最高编码效率。此数控振荡器 (DCO) 可使器件在 3.5µs（典型值）内从低功耗模式唤醒至激活模式。

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

English Data Sheet: SLAS590

MSP430F5529、MSP430F5527、MSP430F5525 和 MSP430F5521 微控制器具有支持 USB 2.0 的集成 USB 和 PHY、4 个 16 位计时器、1 个高性能 12 位模数转换器 (ADC)、2 个 USCI、1 个硬件乘法器、DMA、1 个带有警报功能的 RTC 模块和 63 个 I/O 引脚。MSP430F5528、MSP430F5526、MSP430F5524 和 MSP430F5522 微控制器包含同样的外设，但具有 47 个 I/O 引脚。

MSP430F5519、MSP430F5517 和 MSP430F5515 微控制器具有支持 USB 2.0 的集成 USB 和 PHY、4 个 16 位计时器、2 个 USCI、1 个硬件乘法器、DMA、1 个带有警报功能的 RTC 模块和 63 个 I/O 引脚。MSP430F5514 和 MSP430FF5513 微控制器包含同样的外设，但具有 47 个 I/O 引脚。

典型 应用 包括需要与多种 USB 主机连接的模拟和数字传感器系统、数据记录器和其它应用。

要获得完整的模块说明，请参阅*《MSP430F5xx 和 MSP430F6xx 系列用户指南》*

器件信息 (1)

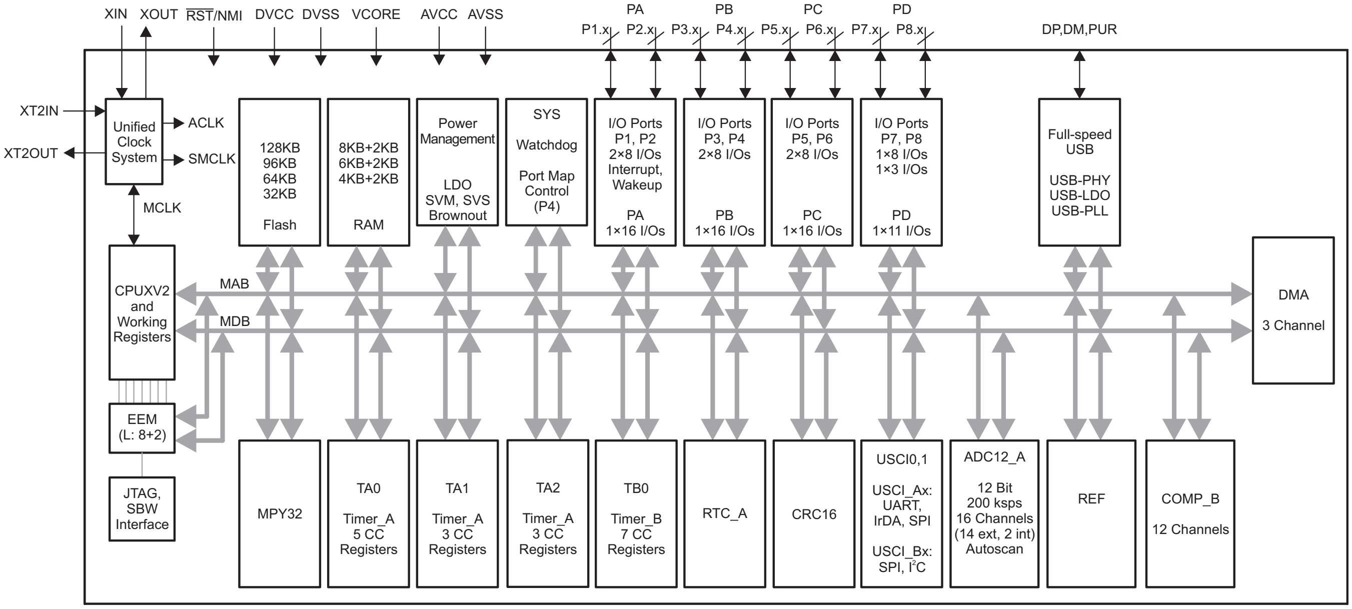
器件型号	封装	封装尺寸 (2)
MSP430F5529IPN	LQFP (80)	12mm x 12mm
MSP430F5528IRGC	VQFN (64)	9mm x 9mm
MSP430F5528IYFF	DSBGA (64)	请参见 节 8
MSP430F5528IZQE	MicroStar Junior™BGA (80)	5mm x 5mm

(1) 要获得所有可用器件的最新部件、封装和订购信息，请参见*封装选项附录*（节 8）或浏览 TI 网站 www.ti.com.cn。

(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见*机械数据*（节 8）。

1.4 功能方框图

图 1-1 展示了采用 PN 封装的 MSP430F5529、MSP430F5527、MSP430F5525 和 MSP430F5521 器件的功能方框图。


XIN
XOUT
RST/NMI
DVCC
DVSS
VCORE
AVCC
AVSS
PA
PB
PC
PD
P1.x
P2.x
P3.x
P4.x
P5.x
P6.x
P7.x
P8.x
DP,DM,PUR
XT2IN
XT2OUT
Unified Clock System
ACLK
SMCLK
MCLK
128KB 96KB 64KB 32KB
Flash
8KB+2KB 6KB+2KB 4KB+2KB
RAM
Power Management
LDO SVM, SVS Brownout
SYS
Watchdog
Port Map Control (P4)
I/O Ports P1, P2 2×8 I/Os Interrupt, Wakeup
PA 1×16 I/Os
I/O Ports P3, P4 2×8 I/Os
PB 1×16 I/Os
I/O Ports P5, P6 2×8 I/Os
PC 1×16 I/Os
I/O Ports P7, P8 1×8 I/Os 1×3 I/Os
PD 1×11 I/Os
Full-speed USB
USB-PHY USB-LDO USB-PLL
CPUXV2 and Working Registers
MAB
MDB
DMA
3 Channel
EEM (L: 8+2)
JTAG, SBW Interface
MPY32
TA0
Timer_A 5 CC Registers
TA1
Timer_A 3 CC Registers
TA2
Timer_A 3 CC Registers
TB0
Timer_B 7 CC Registers
RTC_A
CRC16
USCI0,1
USCI_Ax: UART, IrDA, SPI
USCI_Bx: SPI, I²C
ADC12_A
12 Bit 200 ksps 16 Channels (14 ext, 2 int) Autoscan
REF
COMP_B
12 Channels

Copyright © 2017, Texas Instruments Incorporated

图 **1-1.** 功能方框图 **– MSP430F5529IPN**、**MSP430F5527IPN**、**MSP430F5525IPN**、**MSP430F5521IPN**

图 1-2 展示了采用 RGC 和 ZQE 封装的 MSP430F5528、MSP430F5526、MSP430F5524 和 MSP430F5522 器件的功能方框图，以及采用 YFF 封装的 MSP430F5528、MSP430F5526 和 MSP430F5524 器件的功能方框图。

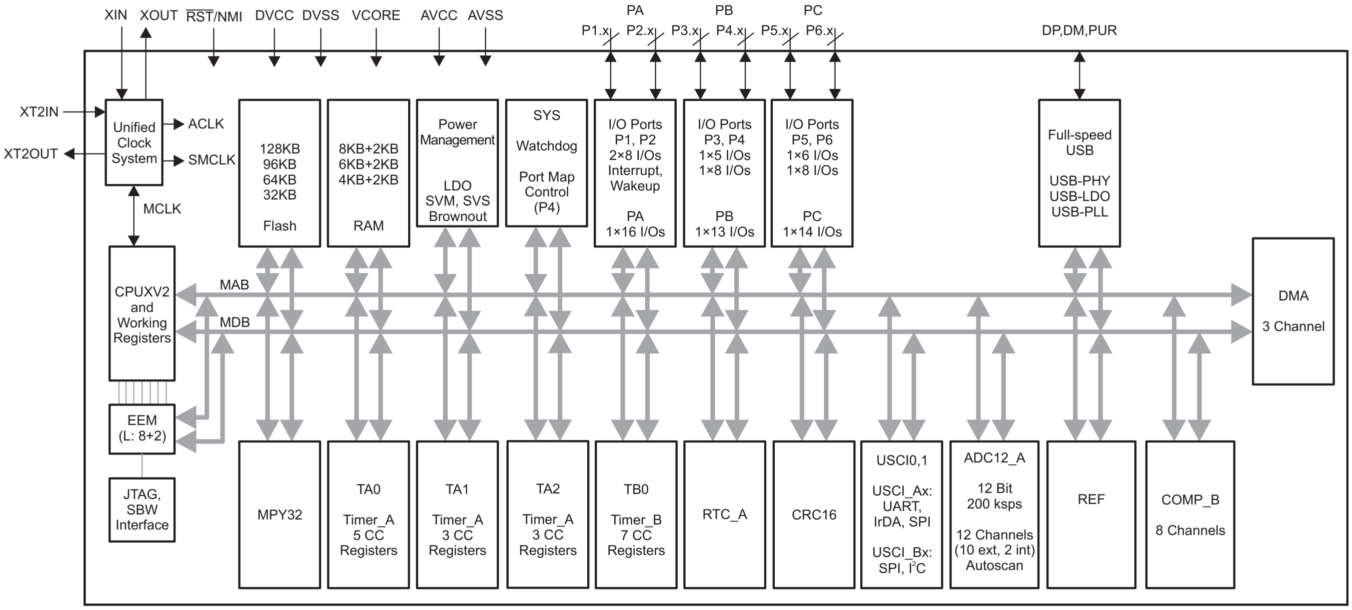

XIN
XOUT
RST/NMI
DVCC
DVSS
VCORE
AVCC
AVSS
PA
PB
PC
P1.x
P2.x
P3.x
P4.x
P5.x
P6.x
DP,DM,PUR
XT2IN
XT2OUT
Unified Clock System
ACLK
SMCLK
MCLK
128KB 96KB 64KB 32KB Flash
8KB+2KB 6KB+2KB 4KB+2KB RAM
Power Management LDO SVM, SVS Brownout
SYS Watchdog Port Map Control (P4)
I/O Ports P1, P2 2×8 I/Os Interrupt, Wakeup PA 1×16 I/Os
I/O Ports P3, P4 1×5 I/Os 1×8 I/Os PB 1×13 I/Os
I/O Ports P5, P6 1×6 I/Os 1×8 I/Os PC 1×14 I/Os
Full-speed USB USB-PHY USB-LDO USB-PLL
CPUXV2 and Working Registers
MAB
MDB
DMA 3 Channel
EEM (L: 8+2)
JTAG, SBW Interface
MPY32
TA0 Timer_A 5 CC Registers
TA1 Timer_A 3 CC Registers
TA2 Timer_A 3 CC Registers
TB0 Timer_B 7 CC Registers
RTC_A
CRC16
USCI0,1 USCI_Ax: UART, IrDA, SPI USCI_Bx: SPI, I2C
ADC12_A 12 Bit 200 ksps 12 Channels (10 ext, 2 int) Autoscan
REF
COMP_B 8 Channels

图 **1-2.** 功能方框图 **–**
MSP430F5528IRGC、MSP430F5526IRGC、MSP430F5524IRGC、MSP430F5522IRGC
MSP430F5528IZQE、MSP430F5526IZQE、MSP430F5524IZQE、MSP430F5522IZQE
MSP430F5528IYFF、MSP430F5526IYFF、MSP430F5524IYFF

图 1-3 展示了采用 PN 封装的 MSP430F5519、MSP430F5517 和 MSP430F5515 器件的功能方框图。

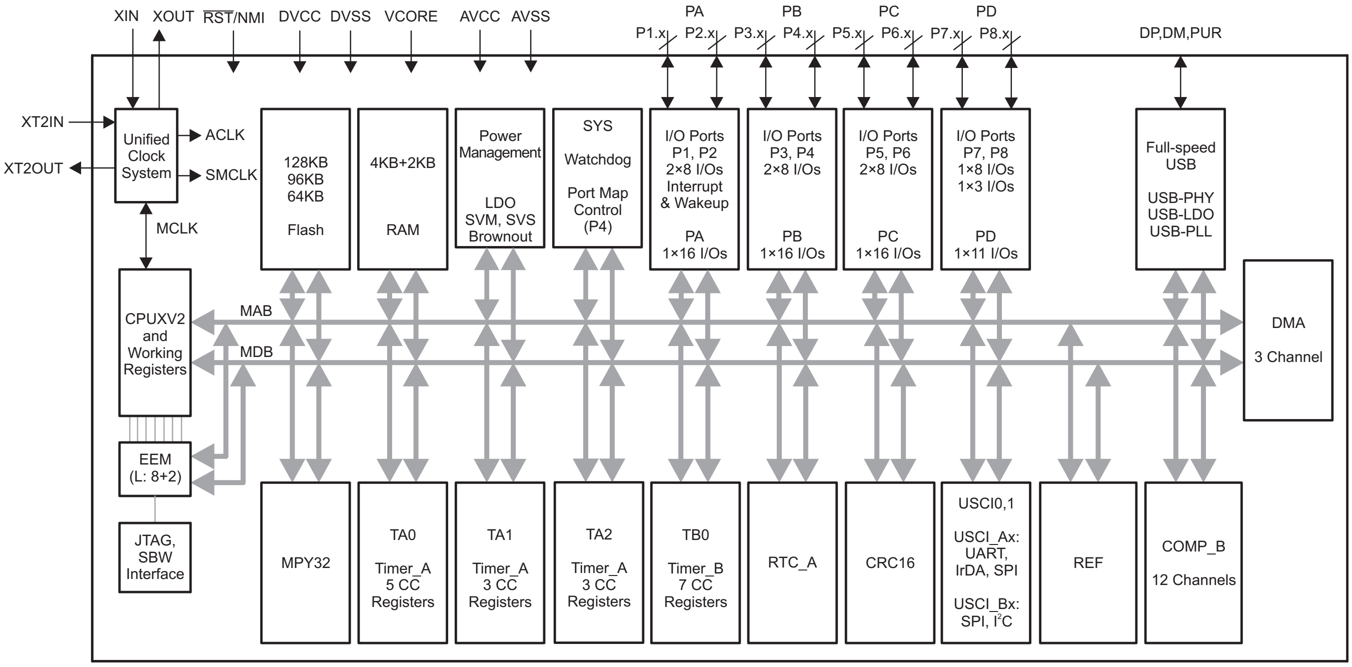

XIN
XOUT
RST/NMI
DVCC
DVSS
VCORE
AVCC
AVSS
PA
PB
PC
PD
P1.x
P2.x
P3.x
P4.x
P5.x
P6.x
P7.x
P8.x
DP,DM,PUR
XT2IN
XT2OUT
Unified Clock System
ACLK
SMCLK
MCLK
128KB 96KB 64KB Flash
4KB+2KB RAM
Power Management LDO SVM, SVS Brownout
SYS Watchdog Port Map Control (P4)
I/O Ports P1, P2 2×8 I/Os Interrupt & Wakeup PA 1×16 I/Os
I/O Ports P3, P4 2×8 I/Os PB 1×16 I/Os
I/O Ports P5, P6 2×8 I/Os PC 1×16 I/Os
I/O Ports P7, P8 1×8 I/Os 1×3 I/Os PD 1×11 I/Os
Full-speed USB USB-PHY USB-LDO USB-PLL
CPUXV2 and Working Registers
MAB
MDB
DMA 3 Channel
EEM (L: 8+2)
JTAG, SBW Interface
MPY32
TA0 Timer_A 5 CC Registers
TA1 Timer_A 3 CC Registers
TA2 Timer_A 3 CC Registers
TB0 Timer_B 7 CC Registers
RTC_A
CRC16
USCI0,1 USCI_Ax: UART, IrDA, SPI USCI_Bx: SPI, I²C
REF
COMP_B 12 Channels

图 **1-3.** 功能方框图 **– MSP430F5519IPN**、**MSP430F5517IPN**、**MSP430F5515IPN**

图 1-4 展示了采用 RGC 和 ZQE 封装的 MSP430F5514 和 MSP430F5513 器件的功能方框图。

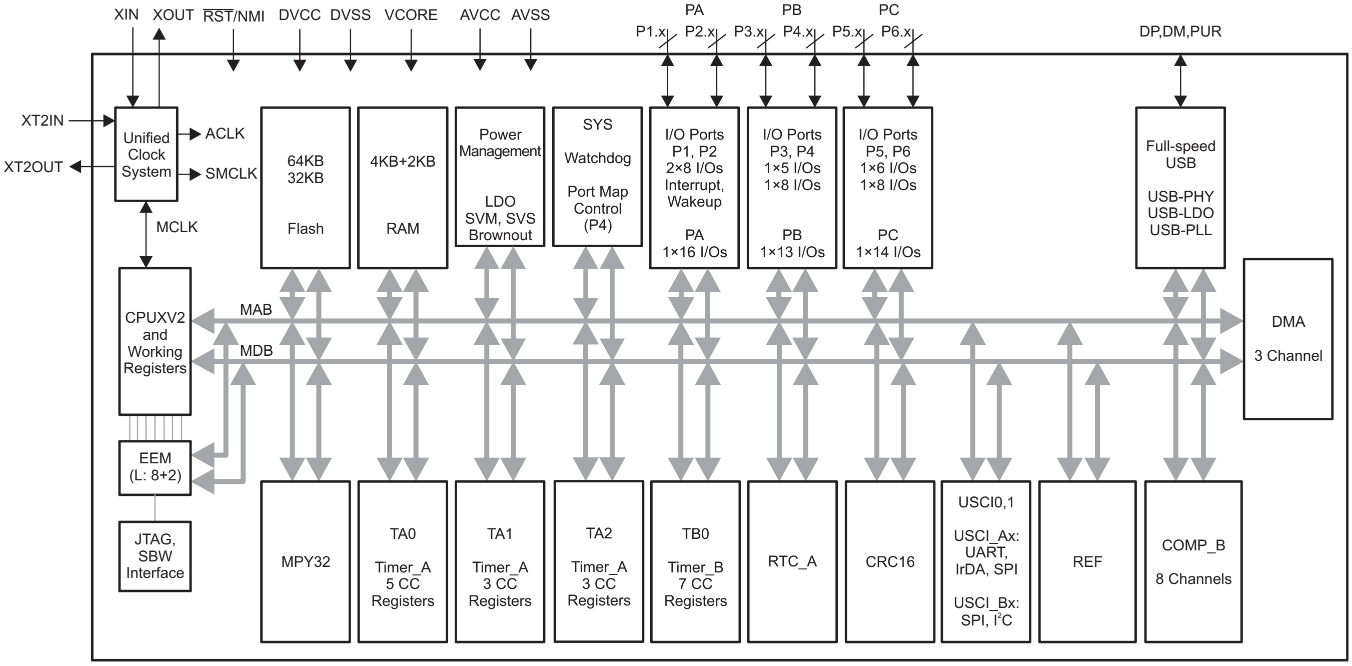

XIN
XOUT
RST/NMI
DVCC
DVSS
VCORE
AVCC
AVSS
PA
PB
PC
P1.x
P2.x
P3.x
P4.x
P5.x
P6.x
DP,DM,PUR
XT2IN
XT2OUT
Unified Clock System
ACLK
SMCLK
MCLK
64KB 32KB Flash
4KB+2KB RAM
Power Management LDO SVM, SVS Brownout
SYS Watchdog Port Map Control (P4)
I/O Ports P1, P2 2×8 I/Os Interrupt, Wakeup PA 1×16 I/Os
I/O Ports P3, P4 1×5 I/Os 1×8 I/Os PB 1×13 I/Os
I/O Ports P5, P6 1×6 I/Os 1×8 I/Os PC 1×14 I/Os
Full-speed USB USB-PHY USB-LDO USB-PLL
CPUXV2 and Working Registers
MAB
MDB
DMA 3 Channel
EEM (L: 8+2)
JTAG, SBW Interface
MPY32
TA0 Timer_A 5 CC Registers
TA1 Timer_A 3 CC Registers
TA2 Timer_A 3 CC Registers
TB0 Timer_B 7 CC Registers
RTC_A
CRC16
USCI0,1 USCI_Ax: UART, IrDA, SPI USCI_Bx: SPI, I²C
REF
COMP_B 8 Channels

图 **1-4.** 功能方框图 **– MSP430F5514IRGC**、**MSP430F5513IRGC**、**MSP430F5514IZQE**、**MSP430F5513IZQE**

内容

1 器件概述 1
1.1 特性 1
1.2 应用范围 1
1.3 说明 1
1.4 功能方框图 2
2 修订历史记录 6
3 Device Comparison 7
3.1 Related Products 8
4 Terminal Configuration and Functions 9
4.1 Pin Diagrams 9
4.2 Signal Descriptions 15
5 Specifications 21
5.1 Absolute Maximum Ratings 21
5.2 ESD Ratings 21
5.3 Recommended Operating Conditions 21
5.4 Active Mode Supply Current Into V_{CC} Excluding External Current 23
5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current 24
5.6 Thermal Resistance Characteristics 25
5.7 Schmitt-Trigger Inputs – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.7, P5.0 to P5.7, P6.0 to P6.7, P7.0 to P7.7, P8.0 to P8.2, PJ.0 to PJ.3, $\overline{\text{RST}}$/NMI) 26
5.8 Inputs – Ports P1 and P2 (P1.0 to P1.7, P2.0 to P2.7) 26
5.9 Leakage Current – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.7) (P5.0 to P5.7, P6.0 to P6.7, P7.0 to P7.7, P8.0 to P8.2, PJ.0 to PJ.3, $\overline{\text{RST}}$/NMI) 26
5.10 Outputs – General-Purpose I/O (Full Drive Strength) (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.7, P5.0 to P5.7, P6.0 to P6.7, P7.0 to P7.7, P8.0 to P8.2, PJ.0 to PJ.3) 26
5.11 Outputs – General-Purpose I/O (Reduced Drive Strength) (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.7, P5.0 to P5.7, P6.0 to P6.7, P7.0 to P7.7, P8.0 to P8.2, PJ.0 to PJ.3) 27
5.12 Output Frequency – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.7, P5.0 to P5.7, P6.0 to P6.7, P7.0 to P7.7, P8.0 to P8.2, PJ.0 to PJ.3) 27
5.13 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0) 28
5.14 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1) 29
5.15 Crystal Oscillator, XT1, Low-Frequency Mode 30
5.16 Crystal Oscillator, XT2 31
5.17 Internal Very-Low-Power Low-Frequency Oscillator (VLO) 32
5.18 Internal Reference, Low-Frequency Oscillator (REFO) 32
5.19 DCO Frequency 33
5.20 PMM, Brownout Reset (BOR) 34
5.21 PMM, Core Voltage 34
5.22 PMM, SVS High Side 34
5.23 PMM, SVM High Side 35
5.24 PMM, SVS Low Side 35
5.25 PMM, SVM Low Side 35
5.26 Wake-up Times From Low-Power Modes and Reset 36
5.27 Timer_A 36
5.28 Timer_B 36
5.29 USCI (UART Mode) Clock Frequency 37
5.30 USCI (UART Mode) 37
5.31 USCI (SPI Master Mode) Clock Frequency 37
5.32 USCI (SPI Master Mode) 37
5.33 USCI (SPI Slave Mode) 39
5.34 USCI (I^{2}C Mode) 41
5.35 12-Bit ADC, Power Supply and Input Range Conditions 42
5.36 12-Bit ADC, Timing Parameters 42
5.37 12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage 43
5.38 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage 43
5.39 12-Bit ADC, Temperature Sensor and Built-In V_{MID} 44
5.40 REF, External Reference 45
5.41 REF, Built-In Reference 45
5.42 Comparator_B 47
5.43 Ports PU.0 and PU.1 47
5.44 USB Output Ports DP and DM 49
5.45 USB Input Ports DP and DM 49
5.46 USB-PWR (USB Power System) 49
5.47 USB-PLL (USB Phase-Locked Loop) 50
5.48 Flash Memory 50
5.49 JTAG and Spy-Bi-Wire Interface 50
6 Detailed Description 51
6.1 CPU (Link to User's Guide) 51
6.2 Operating Modes 52
6.3 Interrupt Vector Addresses 53
6.4 Memory Organization 54
6.5 Bootloader (BSL) 55
6.6 JTAG Operation 56
6.7 Flash Memory (Link to User's Guide) 57
6.8 RAM (Link to User's Guide) 57
6.9 Peripherals 57
6.10 Input/Output Diagrams 82
6.11 Device Descriptors (TLV) 106
7 器件和文档支持 112
7.1 入门和后续步骤 112
7.2 Device Nomenclature 112
7.3 工具与软件 114
7.4 文档支持 116
7.5 相关链接 118
7.6 社区资源 118

7.7 商标 118
7.8 静电放电警告 119
7.9 Export Control Notice 119
7.10 Glossary 119
8 机械、封装和可订购信息 119

2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from November 3, 2015 to September 20, 2018 **Page**

- 更改了*器件信息* 表中 DSBGA 封装的封装尺寸条目 2
- Added Section 3.1, *Related Products* 8
- Removed D and E dimension lines from the YFF pinout (for package dimensions, see the *Mechanical Data* in 节 8) 14
- Added typical conditions statements at the beginning of Section 5, *Specifications* 21
- Changed the MIN value of the $V_{(DVCC\_BOR\_hys)}$ parameter from 60 mV to 50 mV in Section 5.20, *PMM, Brownout Reset (BOR)* 34
- Updated notes (1) and (2) and added note (3) in Section 5.26, *Wake-up Times From Low-Power Modes and Reset* 36
- Removed ADC12DIV from the formula for the TYP value in the second row of the $t_{CONVERT}$ parameter in Section 5.36, *12-Bit ADC, Timing Parameters*, because ADC12CLK is after division 42
- Added second row for t_{EN_CMP} with Test Conditions of "CBPWRMD = 10" and MAX value of 100 µs in Section 5.42, *Comparator_B* 47
- Renamed FCTL4.MGR0 and MGR1 bits in the $f_{MCLK,MGR}$ parameter in Section 5.48, *Flash Memory*, to be consistent with header files 50
- Throughout document, changed all instances of "bootstrap loader" to "bootloader" 55
- Added YFF pin numbers to Table 6-11, *TA0 Signal Connections* 63
- Added YFF pin numbers to Table 6-12, *TA1 Signal Connections* 64
- Added YFF pin numbers to Table 6-13, *TA2 Signal Connections* 65
- 已将先前的"*开发工具支持*"部分替换为"节 7.3、*工具与软件*" 114
- 更改了格式并添加内容至节 7.4*文档支持* 116

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison(1)(2)

DEVICE	FLASH (KB)	SRAM (KB)(3)	Timer_A(4)	Timer_B(5)	USCI CHANNEL A: UART, IrDA, SPI	USCI CHANNEL B: SPI, I²C	ADC12_A (Ch)	COMP_B (Ch)	I/Os	PACKAGE
MSP430F5529	128	8 + 2	5, 3, 3	7	2	2	14 ext, 2 int	12	63	80 PN
MSP430F5528	128	8 + 2	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 64 YFF, 80 ZQE
MSP430F5527	96	6 + 2	5, 3, 3	7	2	2	14 ext, 2 int	12	63	80 PN
MSP430F5526	96	6 + 2	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 64 YFF, 80 ZQE
MSP430F5525	64	4 + 2	5, 3, 3	7	2	2	14 ext, 2 int	12	63	80 PN
MSP430F5524	64	4 + 2	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 64 YFF, 80 ZQE
MSP430F5522	32	8 + 2	5, 3, 3	7	2	2	10 ext, 2 int	8	47	64 RGC, 80 ZQE
MSP430F5521	32	6 + 2	5, 3, 3	7	2	2	14 ext, 2 int	12	63	80 PN
MSP430F5519	128	8 + 2	5, 3, 3	7	2	2	–	12	63	80 PN
MSP430F5517	96	6 + 2	5, 3, 3	7	2	2	–	12	63	80 PN
MSP430F5515	64	4 + 2	5, 3, 3	7	2	2	–	12	63	80 PN
MSP430F5514	64	4 + 2	5, 3, 3	7	2	2	–	8	47	64 RGC, 80 ZQE
MSP430F5513	32	4 + 2	5, 3, 3	7	2	2	–	8	47	64 RGC, 80 ZQE

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in 节 8, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) The additional 2KB of USB SRAM that is listed can be used as general-purpose SRAM when USB is not in use.
(4) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(5) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for TI Microcontrollers TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

Products for MSP430 Ultra-Low-Power Microcontrollers One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

Companion Products for MSP430F5529 Review products that are frequently purchased or used with this product.

Reference Designs for MSP430F5529 The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout for the MSP430F5529, MSP430F5527, MSP430F5525, and MSP430F5521 devices in the 80-pin PN package.

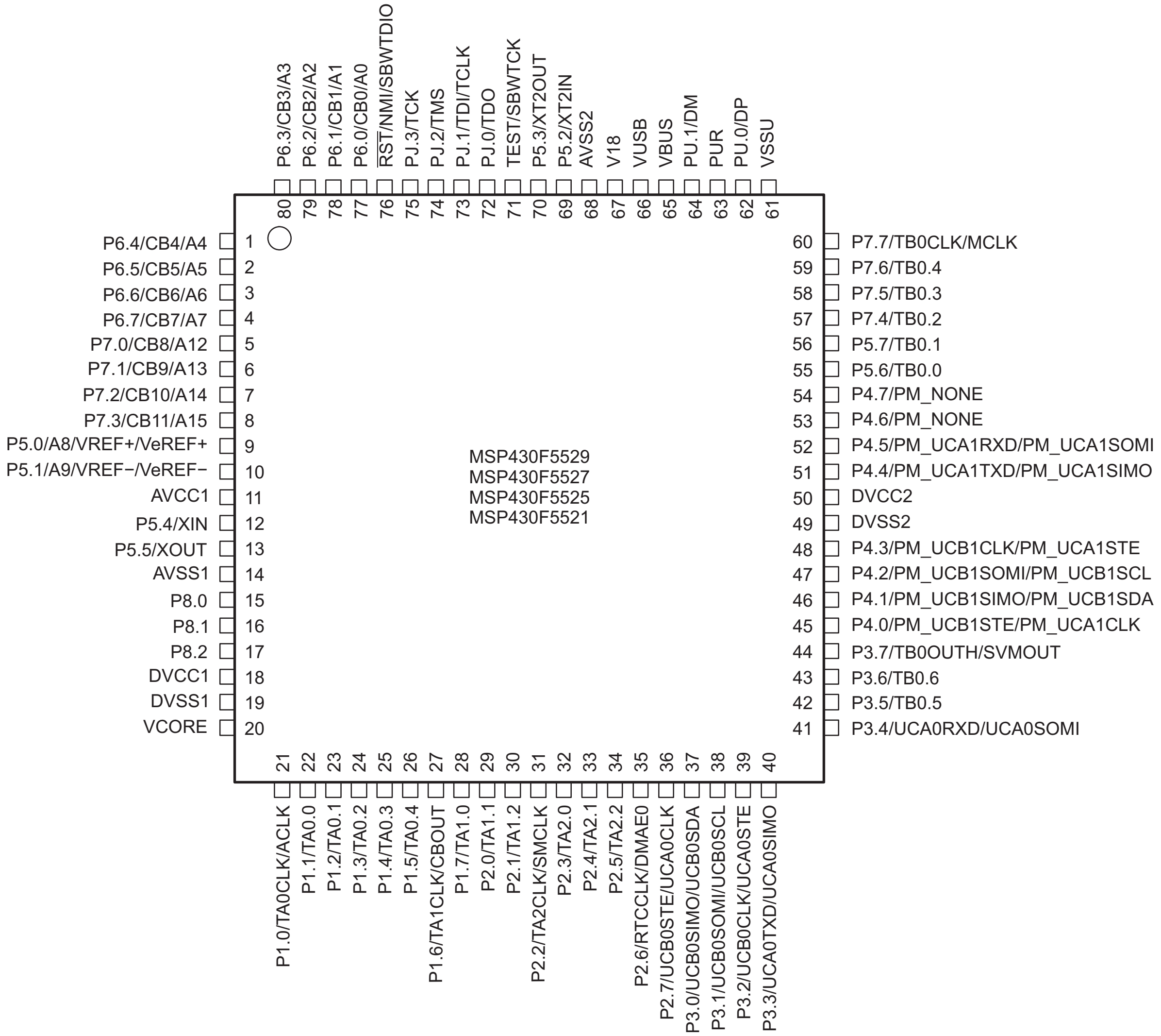
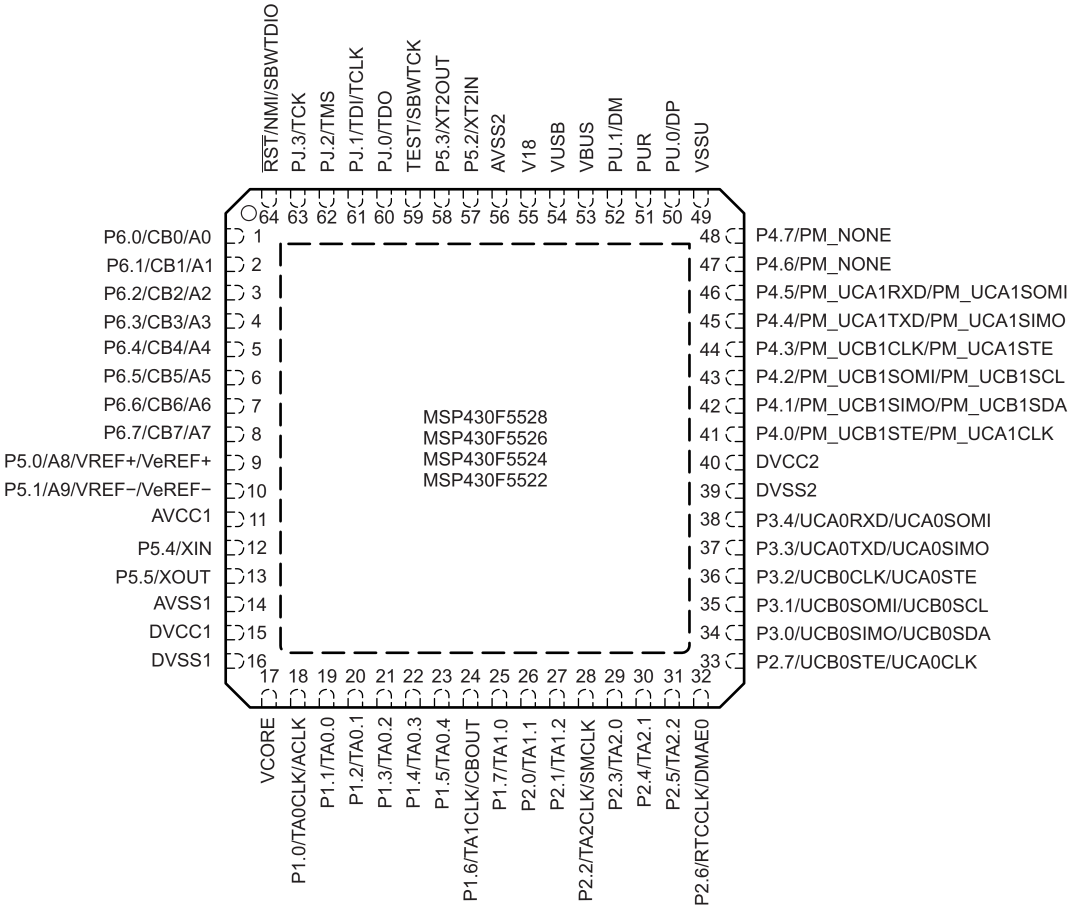

P6.3/CB3/A3 80
P6.2/CB2/A2 79
P6.1/CB1/A1 78
P6.0/CB0/A0 77
RST/NMI/SBWTDIO 76
PJ.3/TCK 75
PJ.2/TMS 74
PJ.1/TDI/TCLK 73
PJ.0/TDO 72
TEST/SBWTCK 71
P5.3/XT2OUT 70
P5.2/XT2IN 69
AVSS2 68
V18 67
VUSB 66
VBUS 65
PU.1/DM 64
PUR 63
PU.0/DP 62
VSSU 61
P6.4/CB4/A4 1
P6.5/CB5/A5 2
P6.6/CB6/A6 3
P6.7/CB7/A7 4
P7.0/CB8/A12 5
P7.1/CB9/A13 6
P7.2/CB10/A14 7
P7.3/CB11/A15 8
P5.0/A8/VREF+/VeREF+ 9
P5.1/A9/VREF−/VeREF− 10
AVCC1 11
P5.4/XIN 12
P5.5/XOUT 13
AVSS1 14
P8.0 15
P8.1 16
P8.2 17
DVCC1 18
DVSS1 19
VCORE 20
60 P7.7/TB0CLK/MCLK
59 P7.6/TB0.4
58 P7.5/TB0.3
57 P7.4/TB0.2
56 P5.7/TB0.1
55 P5.6/TB0.0
54 P4.7/PM_NONE
53 P4.6/PM_NONE
52 P4.5/PM_UCA1RXD/PM_UCA1SOMI
51 P4.4/PM_UCA1TXD/PM_UCA1SIMO
50 DVCC2
49 DVSS2
48 P4.3/PM_UCB1CLK/PM_UCA1STE
47 P4.2/PM_UCB1SOMI/PM_UCB1SCL
46 P4.1/PM_UCB1SIMO/PM_UCB1SDA
45 P4.0/PM_UCB1STE/PM_UCA1CLK
44 P3.7/TB0OUTH/SVMOUT
43 P3.6/TB0.6
42 P3.5/TB0.5
41 P3.4/UCA0RXD/UCA0SOMI
MSP430F5529
MSP430F5527
MSP430F5525
MSP430F5521
21 P1.0/TA0CLK/ACLK
22 P1.1/TA0.0
23 P1.2/TA0.1
24 P1.3/TA0.2
25 P1.4/TA0.3
26 P1.5/TA0.4
27 P1.6/TA1CLK/CBOUT
28 P1.7/TA1.0
29 P2.0/TA1.1
30 P2.1/TA1.2
31 P2.2/TA2CLK/SMCLK
32 P2.3/TA2.0
33 P2.4/TA2.1
34 P2.5/TA2.2
35 P2.6/RTCCLK/DMAE0
36 P2.7/UCB0STE/UCA0CLK
37 P3.0/UCB0SIMO/UCB0SDA
38 P3.1/UCB0SOMI/UCB0SCL
39 P3.2/UCB0CLK/UCA0STE
40 P3.3/UCA0TXD/UCA0SIMO

Figure 4-1. 80-Pin PN Package – MSP430F5529IPN, MSP430F5527IPN, MSP430F5525IPN, MSP430F5521IPN (Top View)

Figure 4-2 shows the pinout for the MSP430F5528, MSP430F5526, MSP430F5524, and MSP430F5522 devices in the 64-pin RGC package.


RST/NMI/SBWTDIO
PJ.3/TCK
PJ.2/TMS
PJ.1/TDI/TCLK
PJ.0/TDO
TEST/SBWTCK
P5.3/XT2OUT
P5.2/XT2IN
AVSS2
V18
VUSB
VBUS
PU.1/DM
PUR
PU.0/DP
VSSU
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
P6.0/CB0/A0 1
P6.1/CB1/A1 2
P6.2/CB2/A2 3
P6.3/CB3/A3 4
P6.4/CB4/A4 5
P6.5/CB5/A5 6
P6.6/CB6/A6 7
P6.7/CB7/A7 8
P5.0/A8/VREF+/VeREF+ 9
P5.1/A9/VREF−/VeREF− 10
AVCC1 11
P5.4/XIN 12
P5.5/XOUT 13
AVSS1 14
DVCC1 15
DVSS1 16
48 P4.7/PM_NONE
47 P4.6/PM_NONE
46 P4.5/PM_UCA1RXD/PM_UCA1SOMI
45 P4.4/PM_UCA1TXD/PM_UCA1SIMO
44 P4.3/PM_UCB1CLK/PM_UCA1STE
43 P4.2/PM_UCB1SOMI/PM_UCB1SCL
42 P4.1/PM_UCB1SIMO/PM_UCB1SDA
41 P4.0/PM_UCB1STE/PM_UCA1CLK
40 DVCC2
39 DVSS2
38 P3.4/UCA0RXD/UCA0SOMI
37 P3.3/UCA0TXD/UCA0SIMO
36 P3.2/UCB0CLK/UCA0STE
35 P3.1/UCB0SOMI/UCB0SCL
34 P3.0/UCB0SIMO/UCB0SDA
33 P2.7/UCB0STE/UCA0CLK
MSP430F5528
MSP430F5526
MSP430F5524
MSP430F5522
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
VCORE
P1.0/TA0CLK/ACLK
P1.1/TA0.0
P1.2/TA0.1
P1.3/TA0.2
P1.4/TA0.3
P1.5/TA0.4
P1.6/TA1CLK/CBOUT
P1.7/TA1.0
P2.0/TA1.1
P2.1/TA1.2
P2.2/TA2CLK/SMCLK
P2.3/TA2.0
P2.4/TA2.1
P2.5/TA2.2
P2.6/RTCCLK/DMAE0

NOTE: TI recommends connecting the exposed thermal pad to V_{SS}.

Figure 4-2. 64-Pin RGC Package – MSP430F5528IRGC, MSP430F5526IRGC, MSP430F5524IRGC, MSP430F5522IRGC (Top View)

Figure 4-3 shows the pinout for the MSP430F5519, MSP430F5517, and MSP430F5515 devices in the 80-pin PN package.

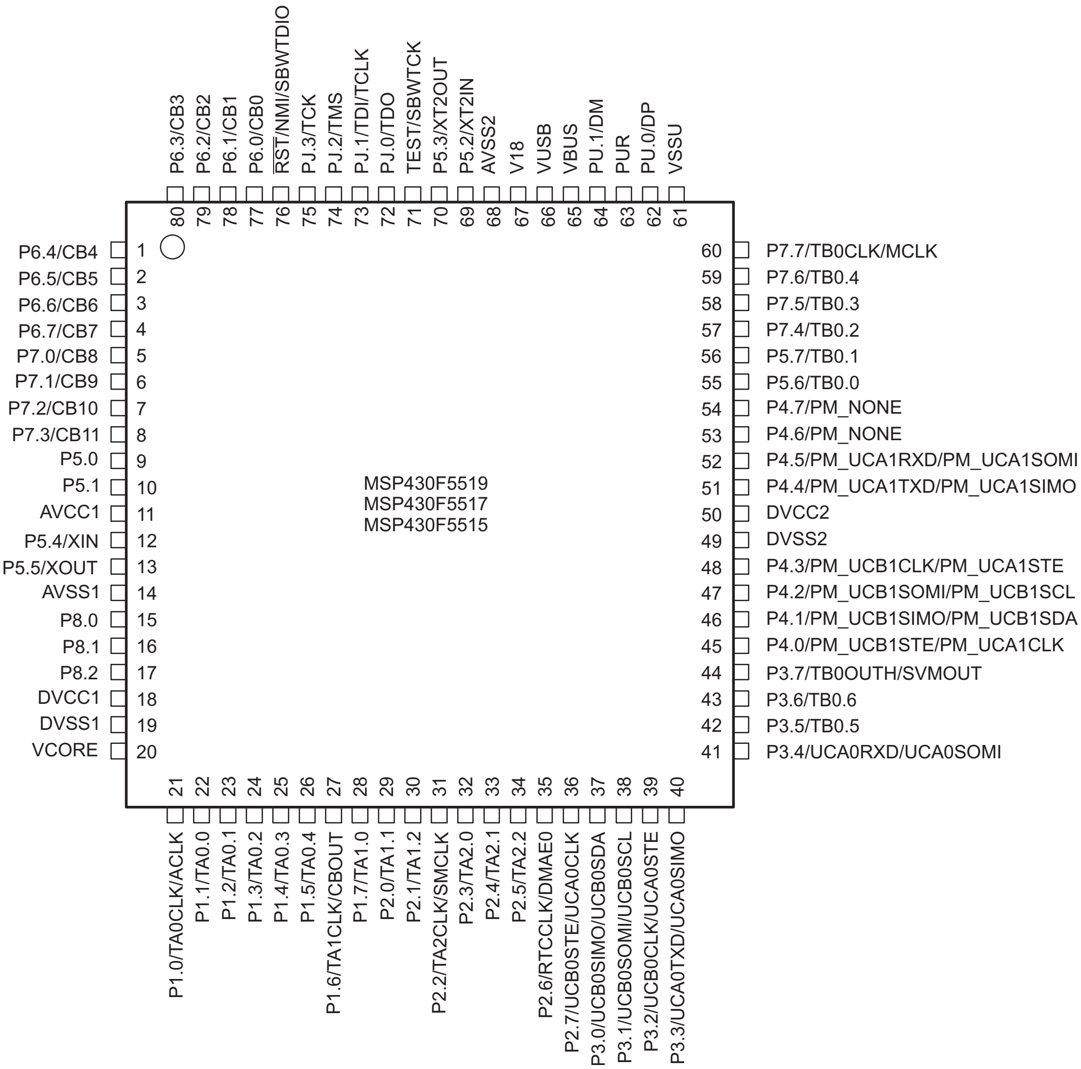
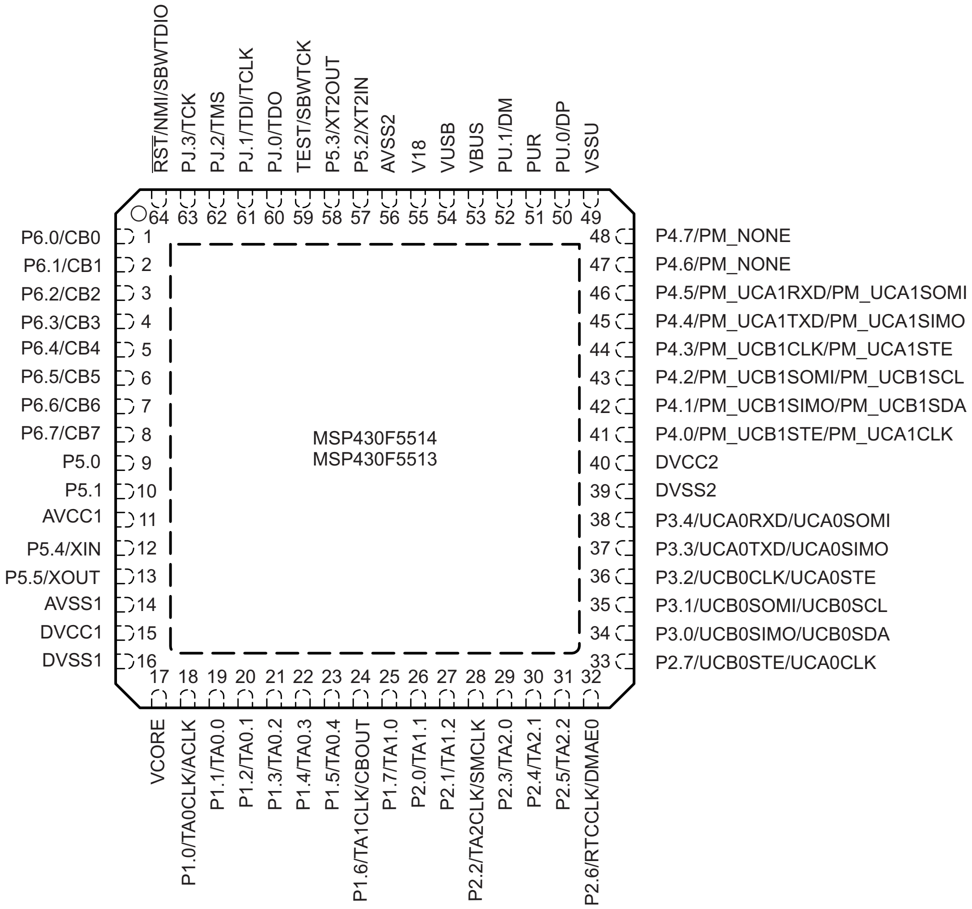

P6.3/CB3 80
P6.2/CB2 79
P6.1/CB1 78
P6.0/CB0 77
RST/NMI/SBWTDIO 76
PJ.3/TCK 75
PJ.2/TMS 74
PJ.1/TDI/TCLK 73
PJ.0/TDO 72
TEST/SBWTCK 71
P5.3/XT2OUT 70
P5.2/XT2IN 69
AVSS2 68
V18 67
VUSB 66
VBUS 65
PU.1/DM 64
PUR 63
PU.0/DP 62
VSSU 61
P6.4/CB4 1
P6.5/CB5 2
P6.6/CB6 3
P6.7/CB7 4
P7.0/CB8 5
P7.1/CB9 6
P7.2/CB10 7
P7.3/CB11 8
P5.0 9
P5.1 10
AVCC1 11
P5.4/XIN 12
P5.5/XOUT 13
AVSS1 14
P8.0 15
P8.1 16
P8.2 17
DVCC1 18
DVSS1 19
VCORE 20
60 P7.7/TB0CLK/MCLK
59 P7.6/TB0.4
58 P7.5/TB0.3
57 P7.4/TB0.2
56 P5.7/TB0.1
55 P5.6/TB0.0
54 P4.7/PM_NONE
53 P4.6/PM_NONE
52 P4.5/PM_UCA1RXD/PM_UCA1SOMI
51 P4.4/PM_UCA1TXD/PM_UCA1SIMO
50 DVCC2
49 DVSS2
48 P4.3/PM_UCB1CLK/PM_UCA1STE
47 P4.2/PM_UCB1SOMI/PM_UCB1SCL
46 P4.1/PM_UCB1SIMO/PM_UCB1SDA
45 P4.0/PM_UCB1STE/PM_UCA1CLK
44 P3.7/TB0OUTH/SVMOUT
43 P3.6/TB0.6
42 P3.5/TB0.5
41 P3.4/UCA0RXD/UCA0SOMI
MSP430F5519
MSP430F5517
MSP430F5515
21 P1.0/TA0CLK/ACLK
22 P1.1/TA0.0
23 P1.2/TA0.1
24 P1.3/TA0.2
25 P1.4/TA0.3
26 P1.5/TA0.4
27 P1.6/TA1CLK/CBOUT
28 P1.7/TA1.0
29 P2.0/TA1.1
30 P2.1/TA1.2
31 P2.2/TA2CLK/SMCLK
32 P2.3/TA2.0
33 P2.4/TA2.1
34 P2.5/TA2.2
35 P2.6/RTCCLK/DMAE0
36 P2.7/UCB0STE/UCA0CLK
37 P3.0/UCB0SIMO/UCB0SDA
38 P3.1/UCB0SOMI/UCB0SCL
39 P3.2/UCB0CLK/UCA0STE
40 P3.3/UCA0TXD/UCA0SIMO

Figure 4-3. 80-Pin PN Package – MSP430F5519IPN, MSP430F5517IPN, MSP430F5515IPN (Top View)

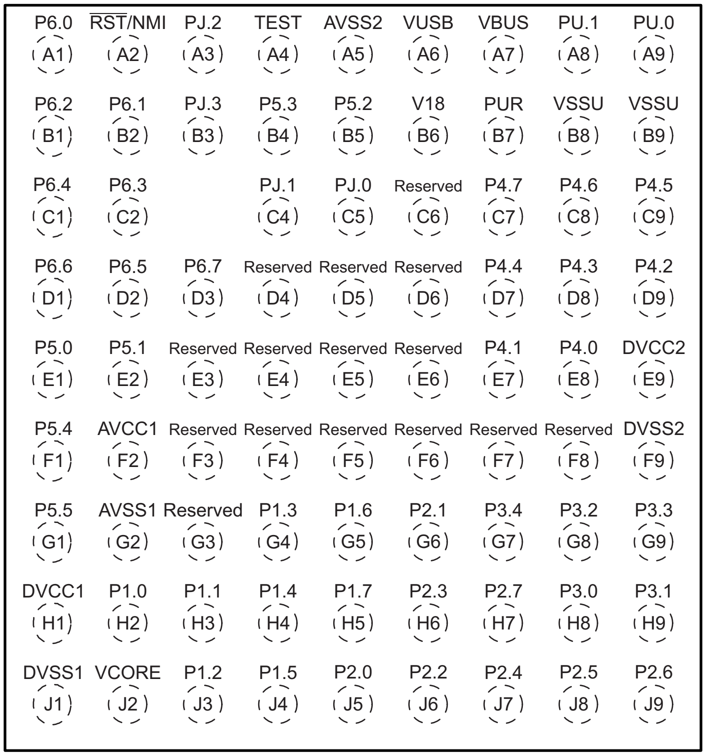
Figure 4-4 shows the pinout for the MSP430F5514 and MSP430F5513 devices in the 64-pin RGC package.


RST/NMI/SBWTDIO
PJ.3/TCK
PJ.2/TMS
PJ.1/TDI/TCLK
PJ.0/TDO
TEST/SBWTCK
P5.3/XT2OUT
P5.2/XT2IN
AVSS2
V18
VUSB
VBUS
PU.1/DM
PUR
PU.0/DP
VSSU
64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49
P6.0/CB0 1
P6.1/CB1 2
P6.2/CB2 3
P6.3/CB3 4
P6.4/CB4 5
P6.5/CB5 6
P6.6/CB6 7
P6.7/CB7 8
P5.0 9
P5.1 10
AVCC1 11
P5.4/XIN 12
P5.5/XOUT 13
AVSS1 14
DVCC1 15
DVSS1 16
48 P4.7/PM_NONE
47 P4.6/PM_NONE
46 P4.5/PM_UCA1RXD/PM_UCA1SOMI
45 P4.4/PM_UCA1TXD/PM_UCA1SIMO
44 P4.3/PM_UCB1CLK/PM_UCA1STE
43 P4.2/PM_UCB1SOMI/PM_UCB1SCL
42 P4.1/PM_UCB1SIMO/PM_UCB1SDA
41 P4.0/PM_UCB1STE/PM_UCA1CLK
40 DVCC2
39 DVSS2
38 P3.4/UCA0RXD/UCA0SOMI
37 P3.3/UCA0TXD/UCA0SIMO
36 P3.2/UCB0CLK/UCA0STE
35 P3.1/UCB0SOMI/UCB0SCL
34 P3.0/UCB0SIMO/UCB0SDA
33 P2.7/UCB0STE/UCA0CLK
MSP430F5514
MSP430F5513
17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32
VCORE
P1.0/TA0CLK/ACLK
P1.1/TA0.0
P1.2/TA0.1
P1.3/TA0.2
P1.4/TA0.3
P1.5/TA0.4
P1.6/TA1CLK/CBOUT
P1.7/TA1.0
P2.0/TA1.1
P2.1/TA1.2
P2.2/TA2CLK/SMCLK
P2.3/TA2.0
P2.4/TA2.1
P2.5/TA2.2
P2.6/RTCCLK/DMAE0

NOTE: TI recommends connecting the exposed thermal pad to V_{SS}.

Figure 4-4. 64-Pin RGC Package – MSP430F5514IRGC, MSP430F5513IRGC (Top View)

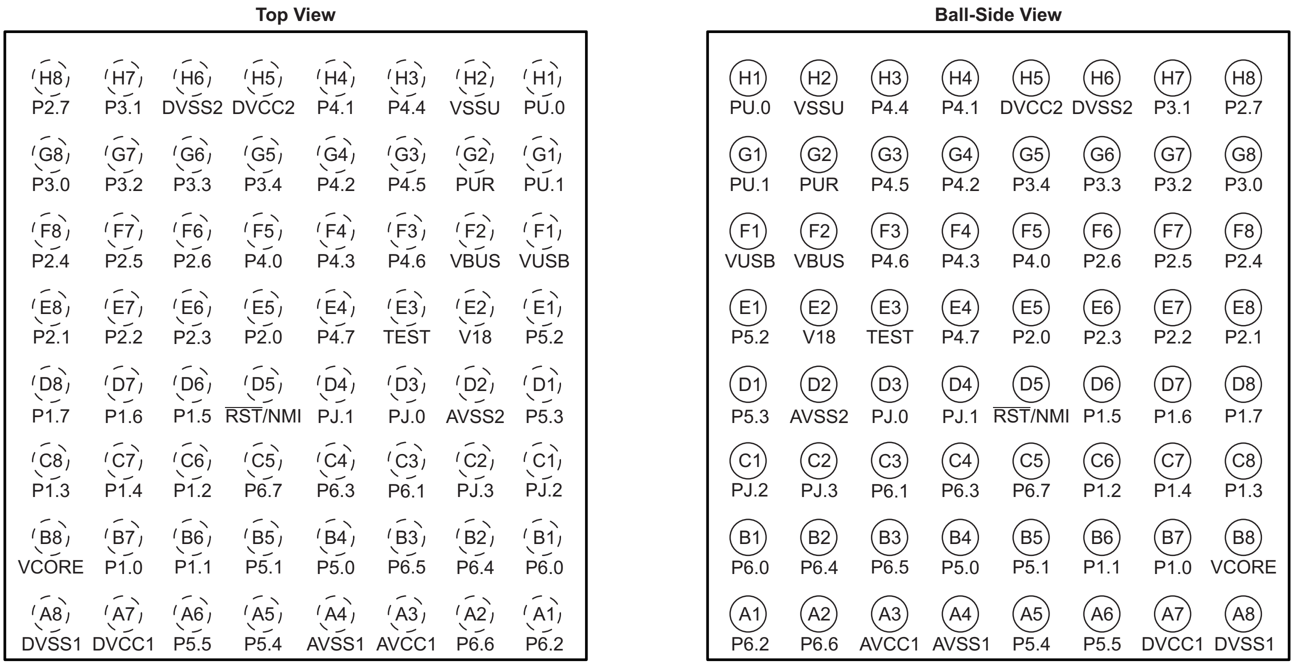
Figure 4-5 shows the pinout for the MSP430F5528, MSP430F5526, MSP430F5524, MSP430F5522, MSP430F5514, and MSP430F5513 devices in the 80-pin ZQE package.



P6.0 A1	$\overline{\text{RST}}$/NMI A2	PJ.2 A3	TEST A4	AVSS2 A5	VUSB A6	VBUS A7	PU.1 A8	PU.0 A9
P6.2 B1	P6.1 B2	PJ.3 B3	P5.3 B4	P5.2 B5	V18 B6	PUR B7	VSSU B8	VSSU B9
P6.4 C1	P6.3 C2		PJ.1 C4	PJ.0 C5	Reserved C6	P4.7 C7	P4.6 C8	P4.5 C9
P6.6 D1	P6.5 D2	P6.7 D3	Reserved D4	Reserved D5	Reserved D6	P4.4 D7	P4.3 D8	P4.2 D9
P5.0 E1	P5.1 E2	Reserved E3	Reserved E4	Reserved E5	Reserved E6	P4.1 E7	P4.0 E8	DVCC2 E9
P5.4 F1	AVCC1 F2	Reserved F3	Reserved F4	Reserved F5	Reserved F6	Reserved F7	Reserved F8	DVSS2 F9
P5.5 G1	AVSS1 G2	Reserved G3	P1.3 G4	P1.6 G5	P2.1 G6	P3.4 G7	P3.2 G8	P3.3 G9
DVCC1 H1	P1.0 H2	P1.1 H3	P1.4 H4	P1.7 H5	P2.3 H6	P2.7 H7	P3.0 H8	P3.1 H9
DVSS1 J1	VCORE J2	P1.2 J3	P1.5 J4	P2.0 J5	P2.2 J6	P2.4 J7	P2.5 J8	P2.6 J9

Figure 4-5. 80-Pin ZQE Package – MSP430F5528IZQE, MSP430F5526IZQE, MSP430F5524IZQE, MSP430F5522IZQE, MSP430F5514IZQE, MSP430F5513IZQE (Top View)

Figure 4-6 shows the pinout for the MSP430F5528, MSP430F5526, and MSP430F5524 devices in the 64-pin YFF package. For package dimensions, see the *Mechanical Data* in 节 8.



Top View

H8 P2.7	H7 P3.1	H6 DVSS2	H5 DVCC2	H4 P4.1	H3 P4.4	H2 VSSU	H1 PU.0
G8 P3.0	G7 P3.2	G6 P3.3	G5 P3.4	G4 P4.2	G3 P4.5	G2 PUR	G1 PU.1
F8 P2.4	F7 P2.5	F6 P2.6	F5 P4.0	F4 P4.3	F3 P4.6	F2 VBUS	F1 VUSB
E8 P2.1	E7 P2.2	E6 P2.3	E5 P2.0	E4 P4.7	E3 TEST	E2 V18	E1 P5.2
D8 P1.7	D7 P1.6	D6 P1.5	D5 $\overline{\text{RST}}$/NMI	D4 PJ.1	D3 PJ.0	D2 AVSS2	D1 P5.3
C8 P1.3	C7 P1.4	C6 P1.2	C5 P6.7	C4 P6.3	C3 P6.1	C2 PJ.3	C1 PJ.2
B8 VCORE	B7 P1.0	B6 P1.1	B5 P5.1	B4 P5.0	B3 P6.5	B2 P6.4	B1 P6.0
A8 DVSS1	A7 DVCC1	A6 P5.5	A5 P5.4	A4 AVSS1	A3 AVCC1	A2 P6.6	A1 P6.2

Ball-Side View

H1 PU.0	H2 VSSU	H3 P4.4	H4 P4.1	H5 DVCC2	H6 DVSS2	H7 P3.1	H8 P2.7
G1 PU.1	G2 PUR	G3 P4.5	G4 P4.2	G5 P3.4	G6 P3.3	G7 P3.2	G8 P3.0
F1 VUSB	F2 VBUS	F3 P4.6	F4 P4.3	F5 P4.0	F6 P2.6	F7 P2.5	F8 P2.4
E1 P5.2	E2 V18	E3 TEST	E4 P4.7	E5 P2.0	E6 P2.3	E7 P2.2	E8 P2.1
D1 P5.3	D2 AVSS2	D3 PJ.0	D4 PJ.1	D5 $\overline{\text{RST}}$/NMI	D6 P1.5	D7 P1.6	D8 P1.7
C1 PJ.2	C2 PJ.3	C3 P6.1	C4 P6.3	C5 P6.7	C6 P1.2	C7 P1.4	C8 P1.3
B1 P6.0	B2 P6.4	B3 P6.5	B4 P5.0	B5 P5.1	B6 P1.1	B7 P1.0	B8 VCORE
A1 P6.2	A2 P6.6	A3 AVCC1	A4 AVSS1	A5 P5.4	A6 P5.5	A7 DVCC1	A8 DVSS1

Figure 4-6. 64-Pin YFF Package – MSP430F5528IYFF, MSP430F5526IYFF, MSP430F5524IYFF

4.2 Signal Descriptions

Table 4-1 describes the signals for all device and package options.

Table 4-1. Terminal Functions

TERMINAL					I/O[(1)]	DESCRIPTION
NAME	NO.					
	PN	RGC	YFF	ZQE		
P6.4/CB4/A4	1	5	B2	C1	I/O	General-purpose digital I/O Comparator_B input CB4 Analog input A4 for ADC (not available on F551x devices)
P6.5/CB5/A5	2	6	B3	D2	I/O	General-purpose digital I/O Comparator_B input CB5 Analog input A5 for ADC (not available on F551x devices)
P6.6/CB6/A6	3	7	A2	D1	I/O	General-purpose digital I/O Comparator_B input CB6 Analog input A6 for ADC (not available on F551x devices)
P6.7/CB7/A7	4	8	C5	D3	I/O	General-purpose digital I/O Comparator_B input CB7 Analog input A7 for ADC (not available on F551x devices)
P7.0/CB8/A12	5	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Comparator_B input CB8 (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Analog input A12 for ADC (not available on F551x devices)
P7.1/CB9/A13	6	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Comparator_B input CB9 (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Analog input A13 for ADC (not available on F551x devices)
P7.2/CB10/A14	7	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Comparator_B input CB10 (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Analog input A14 for ADC (not available on F551x devices)
P7.3/CB11/A15	8	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Comparator_B input CB11 (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Analog input A15 for ADC (not available on F551x devices)
P5.0/A8/VREF+/VeREF+	9	9	B4	E1	I/O	General-purpose digital I/O Output of reference voltage to the ADC (not available on F551x devices) Input for an external reference voltage to the ADC (not available on F551x devices) Analog input A8 for ADC (not available on F551x devices)
P5.1/A9/VREF-/VeREF-	10	10	B5	E2	I/O	General-purpose digital I/O Negative terminal for the ADC reference voltage for both sources, the internal reference voltage, or an external applied reference voltage (not available on F551x devices) Analog input A9 for ADC (not available on F551x devices)
AVCC1	11	11	A3	F2		Analog power supply

---

(1) I = input, O = output, N/A = not available

Table 4-1. Terminal Functions (continued)

TERMINAL					I/O[1]	DESCRIPTION
NAME	NO.					
	PN	RGC	YFF	ZQE		
P5.4/XIN	12	12	A5	F1	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1
P5.5/XOUT	13	13	A6	G1	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT1
AVSS1	14	14	A4	G2		Analog ground supply
P8.0	15	N/A	N/A	N/A	I/O	General-purpose digital I/O
P8.1	16	N/A	N/A	N/A	I/O	General-purpose digital I/O
P8.2	17	N/A	N/A	N/A	I/O	General-purpose digital I/O
DVCC1	18	15	A7	H1		Digital power supply
DVSS1	19	16	A8	J1		Digital ground supply
VCORE[2]	20	17	B8	J2		Regulated core power supply output (internal use only, no external current loading)
P1.0/TA0CLK/ACLK	21	18	B7	H2	I/O	General-purpose digital I/O with port interrupt TA0 clock signal TA0CLK input ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P1.1/TA0.0	22	19	B6	H3	I/O	General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output
P1.2/TA0.1	23	20	C6	J3	I/O	General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input
P1.3/TA0.2	24	21	C8	G4	I/O	General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output
P1.4/TA0.3	25	22	C7	H4	I/O	General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output
P1.5/TA0.4	26	23	D6	J4	I/O	General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output
P1.6/TA1CLK/CBOUT	27	24	D7	G5	I/O	General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input Comparator_B output
P1.7/TA1.0	28	25	D8	H5	I/O	General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output
P2.0/TA1.1	29	26	E5	J5	I/O	General-purpose digital I/O with port interrupt TA1 CCR1 capture: CCI1A input, compare: Out1 output
P2.1/TA1.2	30	27	E8	G6	I/O	General-purpose digital I/O with port interrupt TA1 CCR2 capture: CCI2A input, compare: Out2 output
P2.2/TA2CLK/SMCLK	31	28	E7	J6	I/O	General-purpose digital I/O with port interrupt TA2 clock signal TA2CLK input SMCLK output
P2.3/TA2.0	32	29	E6	H6	I/O	General-purpose digital I/O with port interrupt TA2 CCR0 capture: CCI0A input, compare: Out0 output
P2.4/TA2.1	33	30	F8	J7	I/O	General-purpose digital I/O with port interrupt TA2 CCR1 capture: CCI1A input, compare: Out1 output

---

(2) VCORE is for internal use only. No external current loading is possible. Connect VCORE to the recommended capacitor value, C_{VCORE} (see Section 5.3).

Table 4-1. Terminal Functions (continued)

TERMINAL					I/O (1)	DESCRIPTION
NAME	NO.					
	PN	RGC	YFF	ZQE		
P2.5/TA2.2	34	31	F7	J8	I/O	General-purpose digital I/O with port interrupt TA2 CCR2 capture: CCI2A input, compare: Out2 output
P2.6/RTCCLK/DMAE0	35	32	F6	J9	I/O	General-purpose digital I/O with port interrupt RTC clock output for calibration DMA external trigger input
P2.7/UCB0STE/UCA0CLK	36	33	H8	H7	I/O	General-purpose digital I/O with port interrupt Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode
P3.0/UCB0SIMO/ UCB0SDA	37	34	G8	H8	I/O	General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I^2C data – USCI_B0 I^2C mode
P3.1/UCB0SOMI/UCB0SCL	38	35	H7	H9	I/O	General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I^2C clock – USCI_B0 I^2C mode
P3.2/UCB0CLK/UCA0STE	39	36	G7	G8	I/O	General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode
P3.3/UCA0TXD/ UCA0SIMO	40	37	G6	G9	I/O	General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode
P3.4/UCA0RXD/ UCA0SOMI	41	38	G5	G7	I/O	General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode
P3.5/TB0.5	42	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR5 capture: CCI5A input, compare: Out5 output
P3.6/TB0.6	43	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR6 capture: CCI6A input, compare: Out6 output
P3.7/TB0OUTH/SVMOUT	44	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) Switch all PWM outputs high impedance input – TB0 (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) SVM output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
P4.0/PM_UCB1STE/ PM_UCA1CLK	45	41	F5	E8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave transmit enable – USCI_B1 SPI mode Default mapping: Clock signal input – USCI_A1 SPI slave mode Default mapping: Clock signal output – USCI_A1 SPI master mode
P4.1/PM_UCB1SIMO/ PM_UCB1SDA	46	42	H4	E7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave in, master out – USCI_B1 SPI mode Default mapping: I^2C data – USCI_B1 I^2C mode

Table 4-1. Terminal Functions (continued)

TERMINAL					I/O[1]	DESCRIPTION
NAME	NO.					
	PN	RGC	YFF	ZQE		
P4.2/PM_UCB1SOMI/ PM_UCB1SCL	47	43	G4	D9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave out, master in – USCI_B1 SPI mode Default mapping: I^2C clock – USCI_B1 I^2C mode
P4.3/PM_UCB1CLK/ PM_UCA1STE	48	44	F4	D8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Clock signal input – USCI_B1 SPI slave mode Default mapping: Clock signal output – USCI_B1 SPI master mode Default mapping: Slave transmit enable – USCI_A1 SPI mode
DVSS2	49	39	H6	F9		Digital ground supply
DVCC2	50	40	H5	E9		Digital power supply
P4.4/PM_UCA1TXD/ PM_UCA1SIMO	51	45	H3	D7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Transmit data – USCI_A1 UART mode Default mapping: Slave in, master out – USCI_A1 SPI mode
P4.5/PM_UCA1RXD/ PM_UCA1SOMI	52	46	G3	C9	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data – USCI_A1 UART mode Default mapping: Slave out, master in – USCI_A1 SPI mode
P4.6/PM_NONE	53	47	F3	C8	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.
P4.7/PM_NONE	54	48	E4	C7	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.
P5.6/TB0.0	55	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR0 capture: CCI0A input, compare: Out0 output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
P5.7/TB0.1	56	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR1 capture: CCI1A input, compare: Out1 output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
P7.4/TB0.2	57	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR2 capture: CCI2A input, compare: Out2 output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
P7.5/TB0.3	58	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR3 capture: CCI3A input, compare: Out3 output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
P7.6/TB0.4	59	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 CCR4 capture: CCI4A input, compare: Out4 output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)
P7.7/TB0CLK/MCLK	60	N/A	N/A	N/A	I/O	General-purpose digital I/O (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) TB0 clock signal TBCLK input (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices) MCLK output (not available on F5528, F5526, F5524, F5522, F5514, F5513 devices)

Table 4-1. Terminal Functions (continued)

TERMINAL					I/O[1]	DESCRIPTION
NAME	NO.					
	PN	RGC	YFF	ZQE		
VSSU	61	49	H2	B8, B9		USB PHY ground supply
PU.0/DP	62	50	H1	A9	I/O	General-purpose digital I/O. Controlled by USB control register USB data terminal DP
PUR	63	51	G2	B7	I/O	USB pullup resistor pin (open drain). The voltage level at the PUR pin is used to invoke the default USB BSL. Recommended 1-MΩ resistor to ground. See Section 6.5.1 for more information.
PU.1/DM	64	52	G1	A8	I/O	General-purpose digital I/O. Controlled by USB control register USB data terminal DM
VBUS	65	53	F2	A7		USB LDO input (connect to USB power source)
VUSB	66	54	F1	A6		USB LDO output
V18	67	55	E2	B6		USB regulated power (internal use only, no external current loading)
AVSS2	68	56	D2	A5		Analog ground supply
P5.2/XT2IN	69	57	E1	B5	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT2
P5.3/XT2OUT	70	58	D1	B4	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT2
TEST/SBWTCK (3)	71	59	E3	A4	I	Test mode pin – selects 4-wire JTAG operation Spy-Bi-Wire input clock when Spy-Bi-Wire operation activated
PJ.0/TDO (4)	72	60	D3	C5	I/O	General-purpose digital I/O JTAG test data output port
PJ.1/TDI/TCLK (4)	73	61	D4	C4	I/O	General-purpose digital I/O JTAG test data input Test clock input
PJ.2/TMS (4)	74	62	C1	A3	I/O	General-purpose digital I/O JTAG test mode select
PJ.3/TCK (4)	75	63	C2	B3	I/O	General-purpose digital I/O JTAG test clock
$\overline{\text{RST}}$/NMI/SBWTDIO (3)	76	64	D5	A2	I/O	Reset input, active low (5) Nonmaskable interrupt input Spy-Bi-Wire data input/output when Spy-Bi-Wire operation activated
P6.0/CB0/A0	77	1	B1	A1	I/O	General-purpose digital I/O Comparator_B input CB0 Analog input A0 for ADC (not available on F551x devices)
P6.1/CB1/A1	78	2	C3	B2	I/O	General-purpose digital I/O Comparator_B input CB1 Analog input A1 for ADC (not available on F551x devices)
P6.2/CB2/A2	79	3	A1	B1	I/O	General-purpose digital I/O Comparator_B input CB2 Analog input A2 for ADC (not available on F551x devices)
P6.3/CB3/A3	80	4	C4	C2	I/O	General-purpose digital I/O Comparator_B input CB3 Analog input A3 for ADC (not available on F551x devices)

---

(3) See Section 6.5 and Section 6.6 for use with BSL and JTAG functions.
(4) See Section 6.6 for use with JTAG function.
(5) When this pin is configured as reset, the internal pullup resistor is enabled by default.

Table 4-1. Terminal Functions (continued)

TERMINAL					I/O[1]	DESCRIPTION
NAME	NO.					
	PN	RGC	YFF	ZQE		
Reserved	N/A	N/A	N/A	[6]		Reserved. Connect to ground.
QFN Pad	N/A	Pad	N/A	N/A		QFN package pad. TI recommends connecting to V_{SS}.

(6) C6, D4, D5, D6, E3, E4, E5, E6, F3, F4, F5, F6, F7, F8, G3 are reserved and should be connected to ground.

5 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at V_{CC} = 3.3 V and T_A = 25°C, unless otherwise noted.

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}	–0.3	4.1	V
Voltage applied to any pin (excluding VCORE, VBUS, V18)(2)	–0.3	V_{CC} + 0.3	V
Diode current at any device pin		±2	mA
Maximum operating junction temperature, T_J		95	°C
Storage temperature, T_{stg}(3)	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. VCORE is for internal device use only. No external DC loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

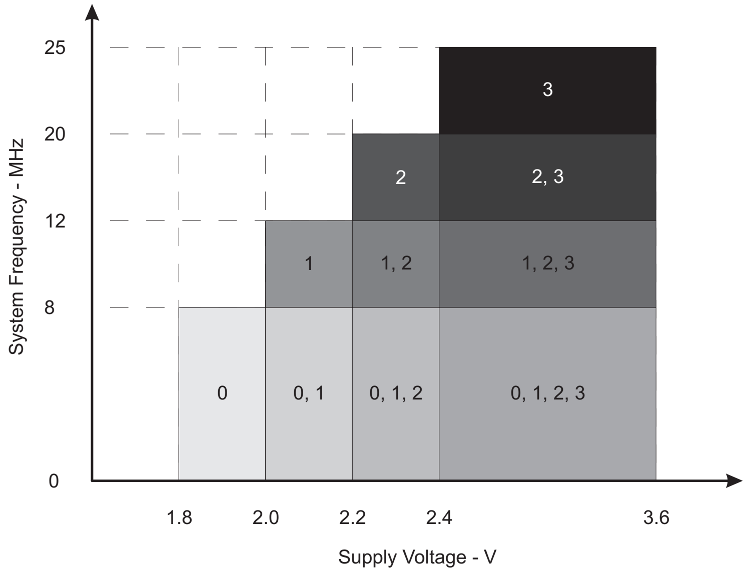
			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming (AV_{CC} = DV_{CC1} = DV_{CC2} = DV_{CC})(1)(2)	PMMCOREVx = 0	1.8		3.6	V
		PMMCOREVx = 0, 1	2.0		3.6	
		PMMCOREVx = 0, 1, 2	2.2		3.6	
		PMMCOREVx = 0, 1, 2, 3	2.4		3.6	
$V_{CC, USB}$	Supply voltage during USB operation, USB PLL disabled, USB_EN = 1, UPLLEN = 0	PMMCOREVx = 0	1.8		3.6	V
		PMMCOREVx = 0, 1	2.0		3.6	
		PMMCOREVx = 0, 1, 2	2.2		3.6	
		PMMCOREVx = 0, 1, 2, 3	2.4		3.6	
	Supply voltage during USB operation, USB PLL enabled(3), USB_EN = 1, UPLLEN = 1	PMMCOREVx = 2	2.2		3.6	
		PMMCOREVx = 2, 3	2.4		3.6	
V_{SS}	Supply voltage (AV_{SS} = DV_{SS1} = DV_{SS2} = DV_{SS})			0		V
T_A	Operating free-air temperature	I version	–40		85	°C
T_J	Operating junction temperature	I version	–40		85	°C
C_{VCORE}	Recommended capacitor at VCORE(4)			470		nF
C_{DVCC}/ C_{VCORE}	Capacitor ratio of DVCC to VCORE		10			ratio

(1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.
(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the Section 5.22 threshold parameters for the exact values and further details.
(3) USB operation with USB PLL enabled requires PMMCOREVx ≥ 2 for proper operation.
(4) A capacitor tolerance of ±20% or better is required.

Recommended Operating Conditions *(continued)*

			MIN	NOM	MAX	UNIT
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)[5] (see Figure 5-1)	PMMCOREVx = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V (default condition)	0		8.0	MHz
		PMMCOREVx = 1, 2.0 V ≤ V_{CC} ≤ 3.6 V	0		12.0	
		PMMCOREVx = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V	0		20.0	
		PMMCOREVx = 3, 2.4 V ≤ V_{CC} ≤ 3.6 V	0		25.0	
f_{SYSTEM_USB}	Minimum processor frequency for USB operation		1.5			MHz
USB_wait	Wait state cycles during USB operation			16		cycles

(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: The numbers within the fields denote the supported PMMCOREVx settings.

Figure 5-1. Maximum System Frequency

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3)

PARAMETER	EXECUTION MEMORY	V_{CC}	PMMCOREVx	FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$)										UNIT
				1 MHz		8 MHz		12 MHz		20 MHz		25 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM,\ Flash}$	Flash	3.0 V	0	0.36	0.47	2.32	2.60							mA
			1	0.40		2.65		4.0	4.4					
			2	0.44		2.90		4.3		7.1	7.7			
			3	0.46		3.10		4.6		7.6		10.1	11.0	
$I_{AM,\ RAM}$	RAM	3.0 V	0	0.20	0.24	1.20	1.30							mA
			1	0.22		1.35		2.0	2.2					
			2	0.24		1.50		2.2		3.7	4.2			
			3	0.26		1.60		2.4		3.9		5.3	6.2	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing. USB disabled (VUSBEN = 0, SLDOEN = 0).
f_{ACLK} = 32786 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF= SMCLKOFF = 0.

5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		V_{CC}	PMMCOREVx	–40°C		25°C		60°C		85°C		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$	Low-power mode 0(3)(4)	2.2 V	0	73		77	85	80		85	97	µA
		3.0 V	3	79		83	92	88		95	105	
I_{LPM2}	Low-power mode 2(5)(4)	2.2 V	0	6.5		6.5	12	10		11	17	µA
		3.0 V	3	7.0		7.0	13	11		12	18	
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode(6)(4)	2.2 V	0	1.60		1.90		2.6		5.6		µA
			1	1.65		2.00		2.7		5.9		
			2	1.75		2.15		2.9		6.1		
		3.0 V	0	1.8		2.1	2.9	2.8		5.8	8.3	
			1	1.9		2.3		2.9		6.1		
			2	2.0		2.4		3.0		6.3		
			3	2.0		2.5	3.9	3.1		6.4	9.3	
$I_{LPM3,VLO}$	Low-power mode 3, VLO mode(7)(4)	3.0 V	0	1.1		1.4	2.7	1.9		4.9	7.4	µA
			1	1.1		1.4		2.0		5.2		
			2	1.2		1.5		2.1		5.3		
			3	1.3		1.6	3.0	2.2		5.4	8.5	
I_{LPM4}	Low-power mode 4(8)(4)	3.0 V	0	0.9		1.1	1.5	1.8		4.8	7.3	µA
			1	1.1		1.2		2.0		5.1		
			2	1.2		1.2		2.1		5.2		
			3	1.3		1.3	1.6	2.2		5.3	8.1	
$I_{LPM4.5}$	Low-power mode 4.5(9)	3.0 V		0.15		0.18	0.35	0.26		0.5	1.0	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

(3) Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz
USB disabled (VUSBEN = 0, SLDOEN = 0).

(4) Current for brownout, high-side supervisor (SVS_H) normal mode included. Low-side supervisor and monitor disabled (SVS_L, SVM_L). High-side monitor disabled (SVM_H). RAM retention enabled.

(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.
USB disabled (VUSBEN = 0, SLDOEN = 0)

(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
USB disabled (VUSBEN = 0, SLDOEN = 0)

(7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = f_{VLO}, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
USB disabled (VUSBEN = 0, SLDOEN = 0)

(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
USB disabled (VUSBEN = 0, SLDOEN = 0)

(9) Internal regulator disabled. No data retention.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz

5.6 Thermal Resistance Characteristics

THERMAL METRIC				VALUE	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	Low-K board (JESD51-3)	LQFP (PN)	70	°C/W
			VQFN (RGC)	55	
			BGA (ZQE)	84	
		High-K board (JESD51-7)	LQFP (PN)	45	
			VQFN (RGC)	25	
			BGA (ZQE)	46	
$R\theta_{JC}$	Junction-to-case thermal resistance		LQFP (PN)	12	°C/W
			VQFN (RGC)	12	
			BGA (ZQE)	30	
$R\theta_{JB}$	Junction-to-board thermal resistance		LQFP (PN)	22	°C/W
			VQFN (RGC)	6	
			BGA (ZQE)	20	

5.7 Schmitt-Trigger Inputs – General-Purpose I/O(1) (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.7, P5.0 to P5.7, P6.0 to P6.7, P7.0 to P7.7, P8.0 to P8.2, PJ.0 to PJ.3, $\overline{\text{RST}}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
$V_{IT–}$	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT–}$)		1.8 V	0.3		0.85	V
			3 V	0.4		1.0	
R_{Pull}	Pullup and pulldown resistor(2)	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).
(2) Also applies to $\overline{\text{RST}}$ pin when pullup or pulldown resistor is enabled.

5.8 Inputs – Ports P1 and P2(1) (P1.0 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing(2)	External trigger pulse duration to set interrupt flag	2.2 V, 3 V	20		ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

5.9 Leakage Current – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.7) (P5.0 to P5.7, P6.0 to P6.7, P7.0 to P7.7, P8.0 to P8.2, PJ.0 to PJ.3, $\overline{\text{RST}}$/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	See (1) (2)	1.8 V, 3 V	–50	50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

5.10 Outputs – General-Purpose I/O (Full Drive Strength) (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.7, P5.0 to P5.7, P6.0 to P6.7, P7.0 to P7.7, P8.0 to P8.2, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage (see Figure 5-8 and Figure 5-9)	$I_{(OHmax)} = –3$ mA(1)	1.8 V	$V_{CC} – 0.25$	V_{CC}	V
		$I_{(OHmax)} = –10$ mA(2)		$V_{CC} – 0.60$	V_{CC}	
		$I_{(OHmax)} = –5$ mA(1)	3 V	$V_{CC} – 0.25$	V_{CC}	
		$I_{(OHmax)} = –15$ mA(2)		$V_{CC} – 0.60$	V_{CC}	
V_{OL}	Low-level output voltage (see Figure 5-6 and Figure 5-7)	$I_{(OLmax)} = 3$ mA(1)	1.8 V	V_{SS}	$V_{SS} + 0.25$	V
		$I_{(OLmax)} = 10$ mA(2)		V_{SS}	$V_{SS} + 0.60$	
		$I_{(OLmax)} = 5$ mA(1)	3 V	V_{SS}	$V_{SS} + 0.25$	
		$I_{(OLmax)} = 15$ mA(2)		V_{SS}	$V_{SS} + 0.60$	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

5.11 Outputs – General-Purpose I/O (Reduced Drive Strength) (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.7, P5.0 to P5.7, P6.0 to P6.7, P7.0 to P7.7, P8.0 to P8.2, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage (see Figure 5-4 and Figure 5-5)	$I_{(OHmax)}$ = –1 mA[2]	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA[3]		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA[2]	3.0 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA[3]		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage (see Figure 5-2 and Figure 5-3)	$I_{(OLmax)}$ = 1 mA[2]	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA[3]		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA[2]	3.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA[3]		V_{SS}	V_{SS} + 0.60	

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

5.12 Output Frequency – General-Purpose I/O (P1.0 to P1.7, P2.0 to P2.7, P3.0 to P3.7, P4.0 to P4.7, P5.0 to P5.7, P6.0 to P6.7, P7.0 to P7.7, P8.0 to P8.2, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	See [1][2]	V_{CC} = 1.8 V, PMMCOREVx = 0		16	MHz
			V_{CC} = 3 V, PMMCOREVx = 3		25	
f_{Port_CLK}	Clock output frequency	ACLK, SMCLK, MCLK, C_L = 20 pF[2]	V_{CC} = 1.8 V, PMMCOREVx = 0		16	MHz
			V_{CC} = 3 V, PMMCOREVx = 3		25	

(1) A resistive divider with 2 × R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.13 Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

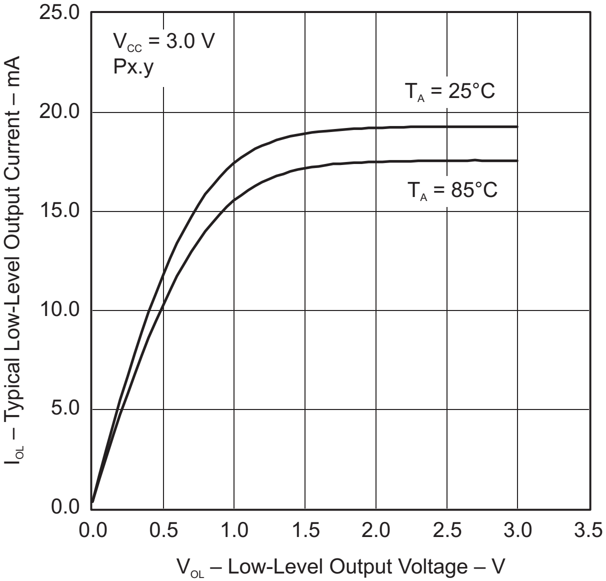


Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage

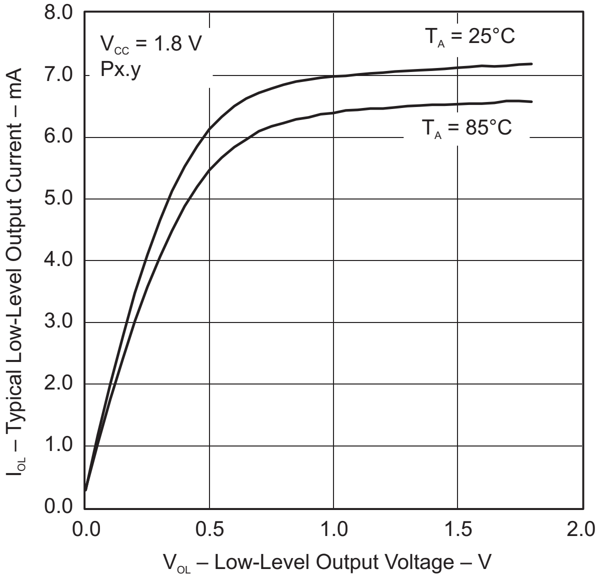


Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage

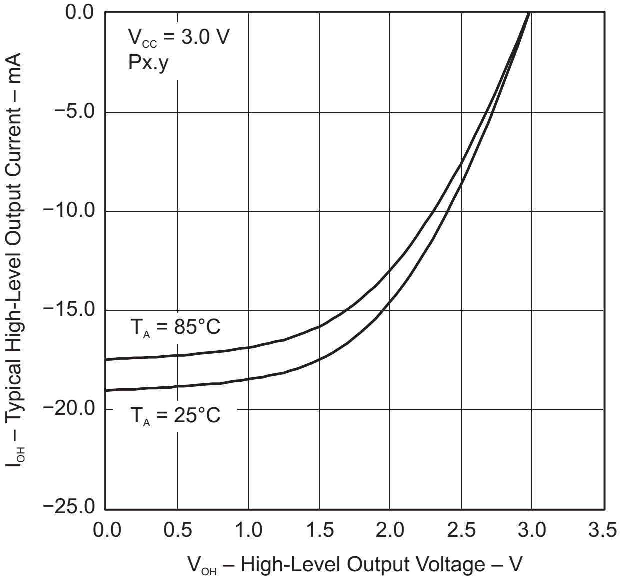


Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage

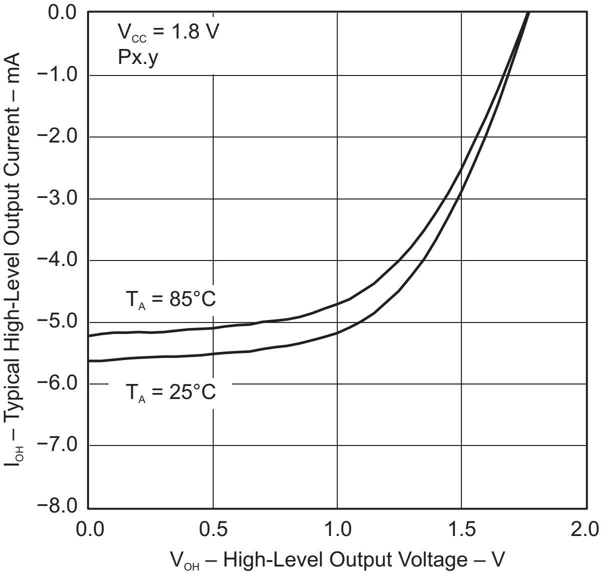


Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage

5.14 Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

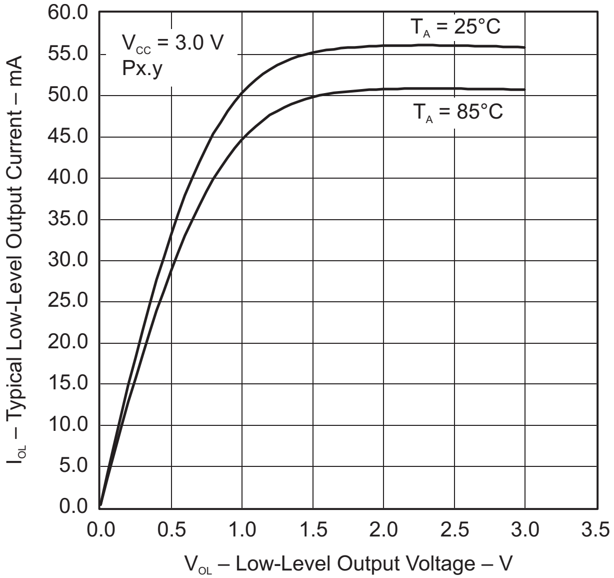


Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage

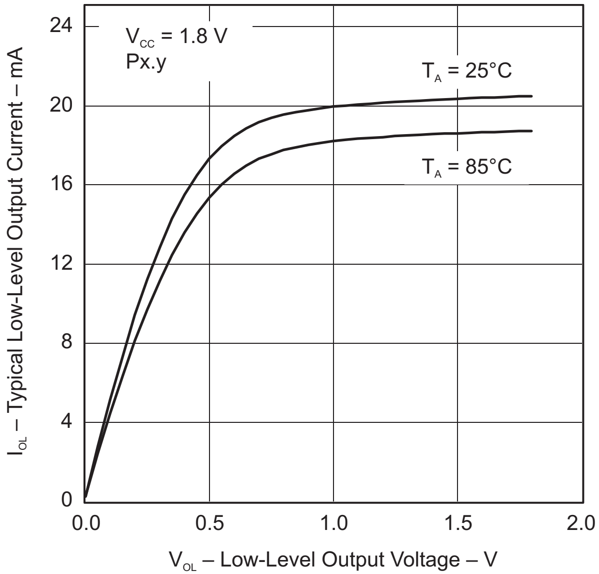


Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage

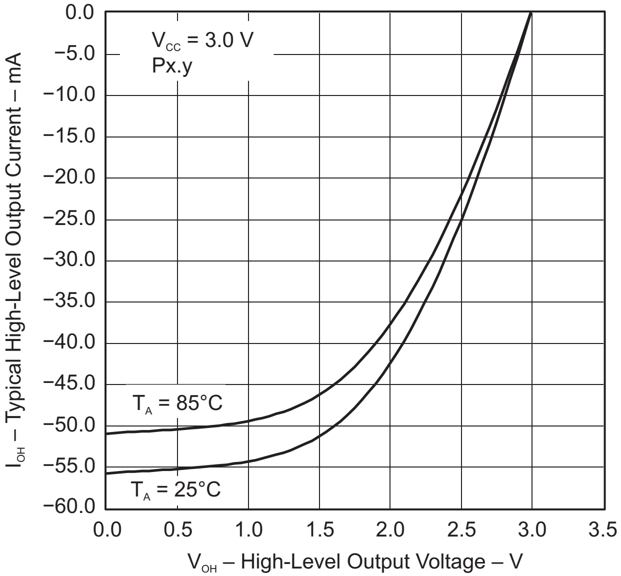


Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage

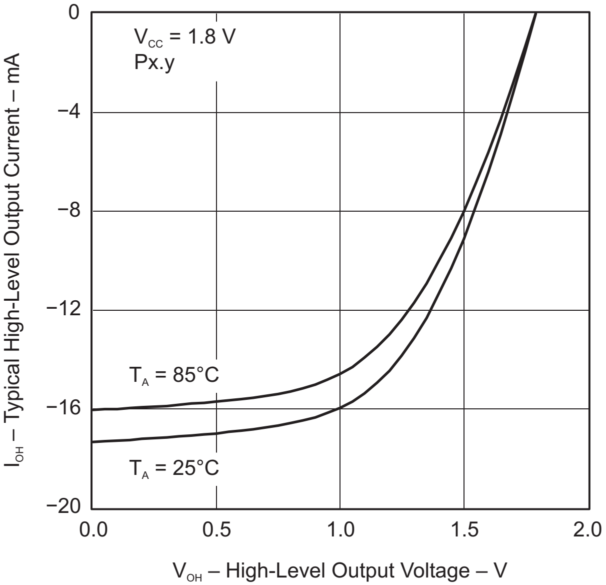


Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage

5.15 Crystal Oscillator, XT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{DVCC.LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C	3.0 V		0.075		µA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			0.170		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			0.290		
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1(2) (3)		10	32.768	50	kHz
OA_{LF}	Oscillation allowance for LF crystals(4)	XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(5)	XTS = 0, XCAPx = 0(6)			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			12.0		
	Duty cycle, LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30%		70%	
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(7)	XTS = 0(8)		10		10000	Hz
$t_{START,LF}$	Start-up time, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 6 pF	3.0 V		1000		ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 12 pF			500		

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For XT1DRIVEx = 0, $C_{L,eff} \leq 6$ pF.
- For XT1DRIVEx = 1, 6 pF $\leq C_{L,eff} \leq 9$ pF.
- For XT1DRIVEx = 2, 6 pF $\leq C_{L,eff} \leq 10$ pF.
- For XT1DRIVEx = 3, $C_{L,eff} \geq 6$ pF.

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

5.16 Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC.XT2}$	XT2 oscillator crystal current consumption	f_{OSC} = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C	3.0 V		200		µA
		f_{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 1, T_A = 25°C			260		
		f_{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C			325		
		f_{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 3, T_A = 25°C			450		
$f_{XT2,HF0}$	XT2 oscillator crystal frequency, mode 0	XT2DRIVEx = 0, XT2BYPASS = 0(3)		4		8	MHz
$f_{XT2,HF1}$	XT2 oscillator crystal frequency, mode 1	XT2DRIVEx = 1, XT2BYPASS = 0(3)		8		16	MHz
$f_{XT2,HF2}$	XT2 oscillator crystal frequency, mode 2	XT2DRIVEx = 2, XT2BYPASS = 0(3)		16		24	MHz
$f_{XT2,HF3}$	XT2 oscillator crystal frequency, mode 3	XT2DRIVEx = 3, XT2BYPASS = 0(3)		24		32	MHz
$f_{XT2,HF,SW}$	XT2 oscillator logic-level square-wave input frequency, bypass mode	XT2BYPASS = 1(4) (3)		0.7		32	MHz
OA_{HF}	Oscillation allowance for HF crystals(5)	XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XT2DRIVEx = 1, XT2BYPASS = 0, $f_{XT2,HF1}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XT2DRIVEx = 2, XT2BYPASS = 0, $f_{XT2,HF2}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XT2DRIVEx = 3, XT2BYPASS = 0, $f_{XT2,HF3}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		
$t_{START,HF}$	Start-up time	f_{OSC} = 6 MHz, XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF	3.0 V		0.5		ms
		f_{OSC} = 20 MHz, XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C, $C_{L,eff}$ = 15 pF			0.3		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(6) (1)				1		pF
	Duty cycle	Measured at ACLK, $f_{XT2,HF2}$ = 20 MHz		40%	50%	60%	
$f_{Fault,HF}$	Oscillator fault frequency(7)	XT2BYPASS = 1(8)		30		300	kHz

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. In general, an effective load capacitance of up to 18 pF can be supported.

(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.
- Keep the traces between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
- Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
- If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.

(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this data sheet.

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

5.17 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.18 Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	1.8 V to 3.6 V		3		µA
f_{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V	–3.5%		3.5%	
		T_A = 25°C	3 V	–1.5%		1.5%	
df_{REFO}/d_T	REFO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.01		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40%	50%	60%	
t_{START}	REFO start-up time	40%/60% duty cycle	1.8 V to 3.6 V		25		µs

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

5.19 DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$	DCO frequency (0, 0)(1)	DCORSELx = 0, DCOx = 0, MODx = 0	0.07		0.20	MHz
$f_{DCO(0,31)}$	DCO frequency (0, 31)(1)	DCORSELx = 0, DCOx = 31, MODx = 0	0.70		1.70	MHz
$f_{DCO(1,0)}$	DCO frequency (1, 0)(1)	DCORSELx = 1, DCOx = 0, MODx = 0	0.15		0.36	MHz
$f_{DCO(1,31)}$	DCO frequency (1, 31)(1)	DCORSELx = 1, DCOx = 31, MODx = 0	1.47		3.45	MHz
$f_{DCO(2,0)}$	DCO frequency (2, 0)(1)	DCORSELx = 2, DCOx = 0, MODx = 0	0.32		0.75	MHz
$f_{DCO(2,31)}$	DCO frequency (2, 31)(1)	DCORSELx = 2, DCOx = 31, MODx = 0	3.17		7.38	MHz
$f_{DCO(3,0)}$	DCO frequency (3, 0)(1)	DCORSELx = 3, DCOx = 0, MODx = 0	0.64		1.51	MHz
$f_{DCO(3,31)}$	DCO frequency (3, 31)(1)	DCORSELx = 3, DCOx = 31, MODx = 0	6.07		14.0	MHz
$f_{DCO(4,0)}$	DCO frequency (4, 0)(1)	DCORSELx = 4, DCOx = 0, MODx = 0	1.3		3.2	MHz
$f_{DCO(4,31)}$	DCO frequency (4, 31)(1)	DCORSELx = 4, DCOx = 31, MODx = 0	12.3		28.2	MHz
$f_{DCO(5,0)}$	DCO frequency (5, 0)(1)	DCORSELx = 5, DCOx = 0, MODx = 0	2.5		6.0	MHz
$f_{DCO(5,31)}$	DCO frequency (5, 31)(1)	DCORSELx = 5, DCOx = 31, MODx = 0	23.7		54.1	MHz
$f_{DCO(6,0)}$	DCO frequency (6, 0)(1)	DCORSELx = 6, DCOx = 0, MODx = 0	4.6		10.7	MHz
$f_{DCO(6,31)}$	DCO frequency (6, 31)(1)	DCORSELx = 6, DCOx = 31, MODx = 0	39.0		88.0	MHz
$f_{DCO(7,0)}$	DCO frequency (7, 0)(1)	DCORSELx = 7, DCOx = 0, MODx = 0	8.5		19.6	MHz
$f_{DCO(7,31)}$	DCO frequency (7, 31)(1)	DCORSELx = 7, DCOx = 31, MODx = 0	60		135	MHz
$S_{DCORSEL}$	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
S_{DCO}	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$	1.02		1.12	ratio
	Duty cycle	Measured at SMCLK	40%	50%	60%	
df_{DCO}/dT	DCO frequency temperature drift(2)	f_{DCO} = 1 MHz		0.1		%/°C
df_{DCO}/dV_{CC}	DCO frequency voltage drift(3)	f_{DCO} = 1 MHz		1.9		%/V

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO}, should be set to reside within the range of $f_{DCO(n, 0),MAX} \le f_{DCO} \le f_{DCO(n, 31),MIN}$, where $f_{DCO(n, 0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.

(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))

(3) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

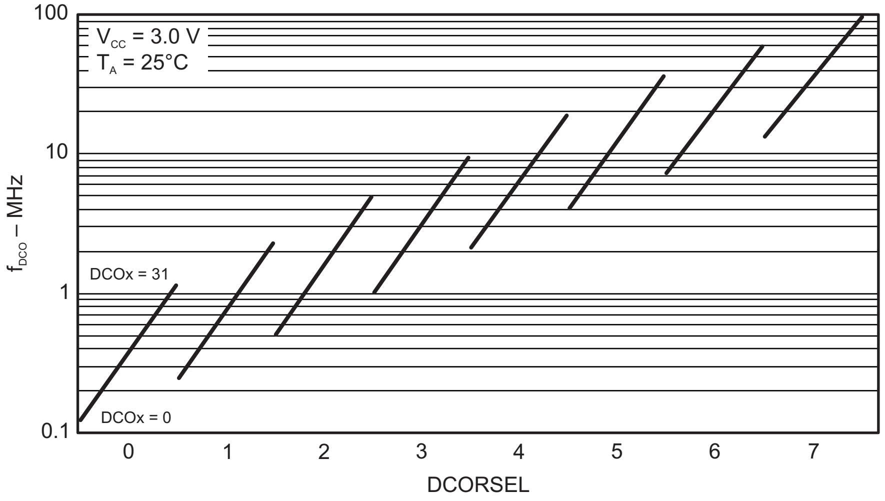


Figure 5-10. Typical DCO Frequency

5.20 PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(DVCC\_BOR\_IT-)}$	BOR_H on voltage, DV_{CC} falling level	$\| dDV_{CC}/d_t \| < 3$ V/s			1.45	V
$V_{(DVCC\_BOR\_IT+)}$	BOR_H off voltage, DV_{CC} rising level	$\| dDV_{CC}/d_t \| < 3$ V/s	0.80	1.30	1.50	V
$V_{(DVCC\_BOR\_hys)}$	BOR_H hysteresis		50		250	mV
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset		2			µs

5.21 PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CORE3}(AM)	Core voltage, active mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.90		V
V_{CORE2}(AM)	Core voltage, active mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.80		V
V_{CORE1}(AM)	Core voltage, active mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.60		V
V_{CORE0}(AM)	Core voltage, active mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.40		V
V_{CORE3}(LPM)	Core voltage, low-current mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.94		V
V_{CORE2}(LPM)	Core voltage, low-current mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.84		V
V_{CORE1}(LPM)	Core voltage, low-current mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.64		V
V_{CORE0}(LPM)	Core voltage, low-current mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.44		V

5.22 PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV_{CC} = 3.6 V		0		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		1.5		µA
$V_{(SVSH\_IT-)}$	SVS_H on voltage level(1)	SVSHE = 1, SVSHRVL = 0	1.57	1.68	1.78	V
		SVSHE = 1, SVSHRVL = 1	1.79	1.88	1.98	
		SVSHE = 1, SVSHRVL = 2	1.98	2.08	2.21	
		SVSHE = 1, SVSHRVL = 3	2.10	2.18	2.31	
$V_{(SVSH\_IT+)}$	SVS_H off voltage level(1)	SVSHE = 1, SVSMHRRL = 0	1.62	1.74	1.85	V
		SVSHE = 1, SVSMHRRL = 1	1.88	1.94	2.07	
		SVSHE = 1, SVSMHRRL = 2	2.07	2.14	2.28	
		SVSHE = 1, SVSMHRRL = 3	2.20	2.30	2.42	
		SVSHE = 1, SVSMHRRL = 4	2.32	2.40	2.55	
		SVSHE = 1, SVSMHRRL = 5	2.52	2.70	2.88	
		SVSHE = 1, SVSMHRRL = 6	2.90	3.10	3.23	
		SVSHE = 1, SVSMHRRL = 7	2.90	3.10	3.23	
$t_{pd(SVSH)}$	SVS_H propagation delay	SVSHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		2.5		µs
		SVSHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		20		
$t_{(SVSH)}$	SVS_H on or off delay time	SVSHE = 0 → 1, SVSHFP = 1		12.5		µs
		SVSHE = 0 → 1, SVSHFP = 0		100		
dV_{DVCC}/dt	DVCC rise time		0		1000	V/s

(1) The SVS_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430F5xx and MSP430F6xx Family User's Guide* on recommended settings and use.

5.23 PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$	SVM_H current consumption	SVMHE = 0, DV_{CC} = 3.6 V		0		nA
		SVMHE= 1, DV_{CC} = 3.6 V, SVMHFP = 0		200		
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 1		1.5		µA
$V_{(SVMH)}$	SVM_H on or off voltage level[1]	SVMHE = 1, SVSMHRRL = 0	1.62	1.74	1.85	V
		SVMHE = 1, SVSMHRRL = 1	1.88	1.94	2.07	
		SVMHE = 1, SVSMHRRL = 2	2.07	2.14	2.28	
		SVMHE = 1, SVSMHRRL = 3	2.20	2.30	2.42	
		SVMHE = 1, SVSMHRRL = 4	2.32	2.40	2.55	
		SVMHE = 1, SVSMHRRL = 5	2.52	2.70	2.88	
		SVMHE = 1, SVSMHRRL = 6	2.90	3.10	3.23	
		SVMHE = 1, SVSMHRRL = 7	2.90	3.10	3.23	
		SVMHE = 1, SVMHOVPE = 1		3.75		
$t_{pd(SVMH)}$	SVM_H propagation delay	SVMHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		2.5		µs
		SVMHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		20		
$t_{(SVMH)}$	SVM_H on or off delay time	SVMHE = 0 → 1, SVMHFP = 1		12.5		µs
		SVMHE = 0 → 1, SVMHFP = 0		100		

[1] The SVM_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430F5xx and MSP430F6xx Family User's Guide* on recommended settings and use.

5.24 PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$	SVS_L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		1.5		µA
$t_{pd(SVSL)}$	SVS_L propagation delay	SVSLE = 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		2.5		µs
		SVSLE = 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		20		
$t_{(SVSL)}$	SVS_L on or off delay time	SVSLE = 0 → 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		12.5		µs
		SVSLE = 0 → 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		100		

5.25 PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$	SVM_L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
		SVMLE= 1, PMMCOREV = 2, SVMLFP = 0		200		
		SVMLE= 1, PMMCOREV = 2, SVMLFP = 1		1.5		µA
$t_{pd(SVML)}$	SVM_L propagation delay	SVMLE = 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		2.5		µs
		SVMLE = 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		20		
$t_{(SVML)}$	SVM_L on or off delay time	SVMLE = 0 → 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		12.5		µs
		SVMLE = 0 → 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		100		

5.26 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{WAKE-UP-FAST}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode[1]	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1	$f_{MCLK} \geq 4.0$ MHz		3.5	7.5	µs
			1.0 MHz < f_{MCLK} < 4.0 MHz		4.5	9	
$t_{WAKE-UP-SLOW}$	Wake-up time from LPM2, LPM3 or LPM4 to active mode[2][3]	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0			150	165	µs
$t_{WAKE-UP-LPM5}$	Wake-up time from LPM4.5 to active mode[4]				2	3	ms
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode[4]				2	3	ms

(1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{WAKE-UP-FAST}$ is possible with SVS_L and SVM_L in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430F5xx and MSP430F6xx Family User's Guide*.

(2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVS_L) and low-side monitor (SVM_L). $t_{WAKE-UP-SLOW}$ is set with SVS_L and SVM_L in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the *MSP430F5xx and MSP430F6xx Family User's Guide*.

(3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.

(4) This value represents the time from the wake-up event to the reset vector execution.

5.27 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK or ACLK, External: TACLK, Duty cycle = 50% ±10%	1.8 V, 3 V		25	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, minimum pulse duration required for capture	1.8 V, 3 V	20		ns

5.28 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, Duty cycle = 50% ±10%	1.8 V, 3 V		25	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	1.8 V, 3 V	20		ns

5.29 USCI (UART Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%		f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)			1	MHz

5.30 USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	MAX	UNIT
t_t	UART receive deglitch time (1)	2.2 V	50	600	ns
		3 V	50	600	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

5.31 USCI (SPI Master Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, Duty cycle = 50% ±10%		f_{SYSTEM}	MHz

5.32 USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)
(see Figure 5-11 and Figure 5-12)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK or ACLK, Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time	PMMCOREV = 0	1.8 V	55		ns
			3.0 V	38		
		PMMCOREV = 3	2.4 V	30		
			3.0 V	25		
$t_{HD,MI}$	SOMI input data hold time	PMMCOREV = 0	1.8 V	0		ns
			3.0 V	0		
		PMMCOREV = 3	2.4 V	0		
			3.0 V	0		
$t_{VALID,MO}$	SIMO output data valid time (2)	UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 0	1.8 V		20	ns
			3.0 V		18	
		UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 3	2.4 V		16	
			3.0 V		15	
$t_{HD,MO}$	SIMO output data hold time (3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	–10		ns
			3.0 V	–8		
		C_L = 20 pF, PMMCOREV = 3	2.4 V	–10		
			3.0 V	–8		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-11 and Figure 5-12.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-11 and Figure 5-12.

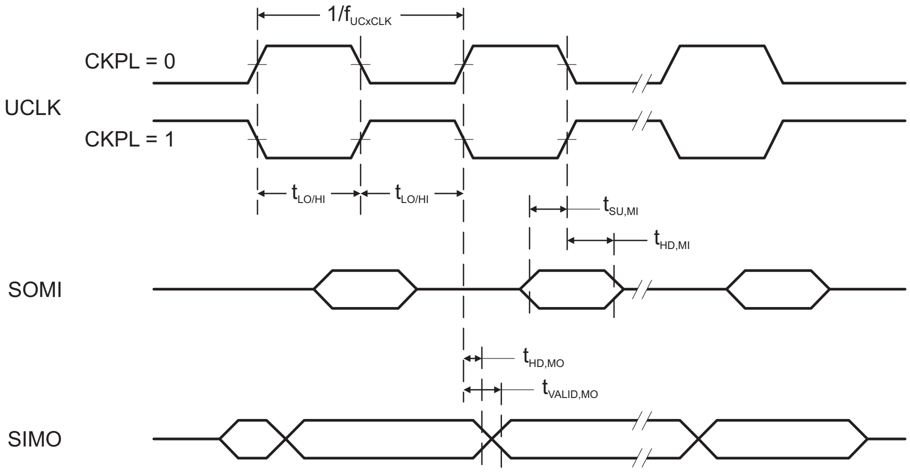

1/f_UCxCLK
CKPL = 0
UCLK
CKPL = 1
t_LO/HI
t_LO/HI
t_SU,MI
t_HD,MI
SOMI
t_HD,MO
t_VALID,MO
SIMO

Figure 5-11. SPI Master Mode, CKPH = 0

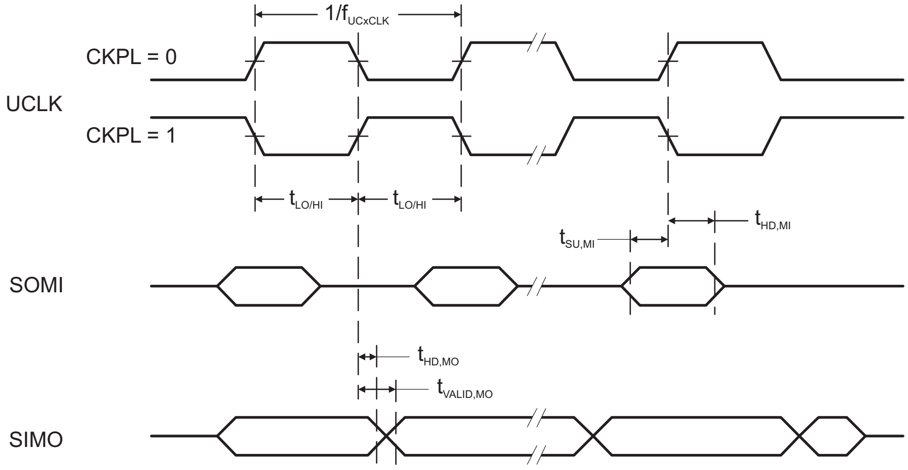

1/f_UCxCLK
CKPL = 0
UCLK
CKPL = 1
t_LO/HI
t_LO/HI
t_HD,MI
t_SU,MI
SOMI
t_HD,MO
t_VALID,MO
SIMO

Figure 5-12. SPI Master Mode, CKPH = 1

5.33 USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)
(see Figure 5-13 and Figure 5-14)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock	PMMCOREV = 0	1.8 V	11		ns
			3.0 V	8		
		PMMCOREV = 3	2.4 V	7		
			3.0 V	6		
$t_{STE,LAG}$	STE lag time, Last clock to STE high	PMMCOREV = 0	1.8 V	3		ns
			3.0 V	3		
		PMMCOREV = 3	2.4 V	3		
			3.0 V	3		
$t_{STE,ACC}$	STE access time, STE low to SOMI data out	PMMCOREV = 0	1.8 V		66	ns
			3.0 V		50	
		PMMCOREV = 3	2.4 V		36	
			3.0 V		30	
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance	PMMCOREV = 0	1.8 V		30	ns
			3.0 V		23	
		PMMCOREV = 3	2.4 V		16	
			3.0 V		13	
$t_{SU,SI}$	SIMO input data setup time	PMMCOREV = 0	1.8 V	5		ns
			3.0 V	5		
		PMMCOREV = 3	2.4 V	2		
			3.0 V	2		
$t_{HD,SI}$	SIMO input data hold time	PMMCOREV = 0	1.8 V	5		ns
			3.0 V	5		
		PMMCOREV = 3	2.4 V	5		
			3.0 V	5		
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 0	1.8 V		76	ns
			3.0 V		60	
		UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 3	2.4 V		44	
			3.0 V		40	
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	18		ns
			3.0 V	12		
		C_L = 20 pF, PMMCOREV = 3	2.4 V	10		
			3.0 V	8		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.

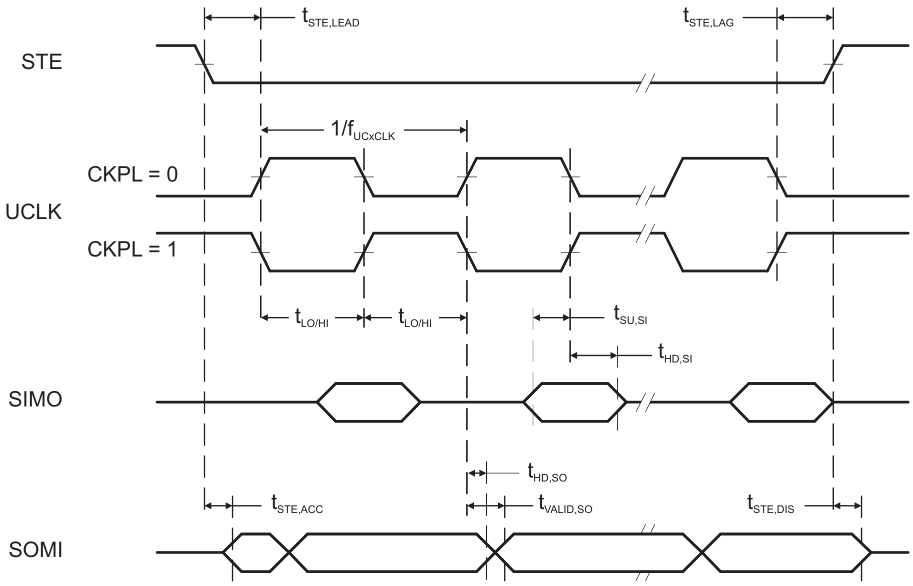

$t_{STE,LEAD}$
$t_{STE,LAG}$
STE
$1/f_{UCxCLK}$
CKPL = 0
UCLK
CKPL = 1
$t_{LO/HI}$
$t_{LO/HI}$
$t_{SU,SI}$
$t_{HD,SI}$
SIMO
$t_{HD,SO}$
$t_{STE,ACC}$
$t_{VALID,SO}$
$t_{STE,DIS}$
SOMI

Figure 5-13. SPI Slave Mode, CKPH = 0

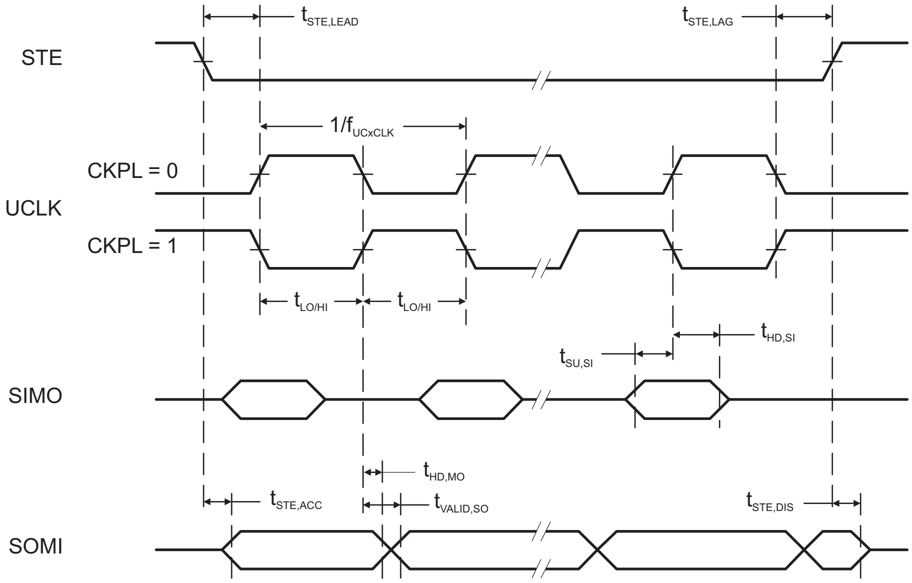

$t_{STE,LEAD}$
$t_{STE,LAG}$
STE
$1/f_{UCxCLK}$
CKPL = 0
UCLK
CKPL = 1
$t_{LO/HI}$
$t_{LO/HI}$
$t_{HD,SI}$
$t_{SU,SI}$
SIMO
$t_{HD,MO}$
$t_{STE,ACC}$
$t_{VALID,SO}$
$t_{STE,DIS}$
SOMI

Figure 5-14. SPI Slave Mode, CKPH = 1

5.34 USCI (I^{2}C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-15)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ±10%			f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0	400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0		µs
		f_{SCL} > 100 kHz		0.6		
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.7		µs
		f_{SCL} > 100 kHz		0.6		
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0		ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	250		ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} ≤ 100 kHz	2.2 V, 3 V	4.0		µs
		f_{SCL} > 100 kHz		0.6		
t_{SP}	Pulse duration of spikes suppressed by input filter		2.2 V	50	600	ns
			3 V	50	600	

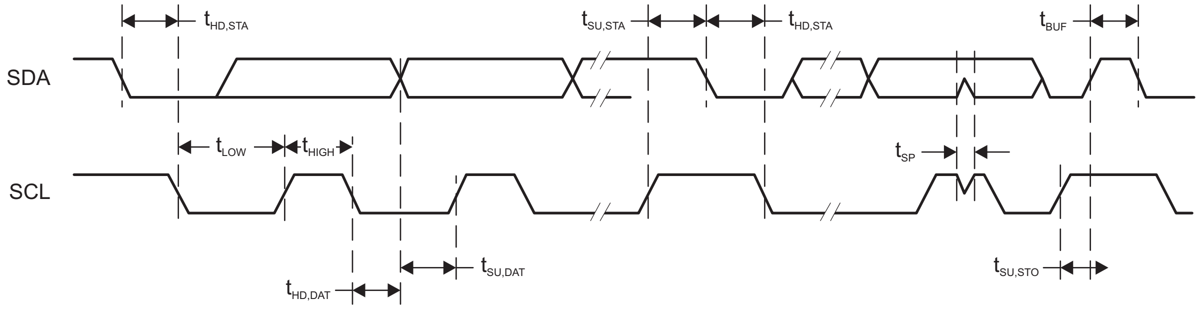


Figure 5-15. I^{2}C Mode Timing

5.35 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(Ax)}$	Analog input voltage range(2)	All ADC12 analog input pins Ax		0		AV_{CC}	V
I_{ADC12_A}	Operating supply current into AVCC terminal(3)	$f_{ADC12CLK} = 5.0$ MHz(4)	2.2 V		125	155	µA
			3 V		150	220	
C_I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		20	25	pF
R_I	Input MUX ON resistance	$0\text{ V} \leq V_{Ax} \leq$ AVCC		10	200	1900	Ω

(1) The leakage current is specified by the digital I/O input leakage.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. If the reference voltage is supplied by an external source or if the internal reference voltage is used and REFOUT = 1, then decoupling capacitors are required. See Section 5.40 and Section 5.41.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12_A}.
(4) ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0

5.36 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	ADC conversion clock	For specified performance of ADC12 linearity parameters using an external reference voltage or AVCC as reference(1)	2.2 V, 3 V	0.45	4.8	5.0	MHz
		For specified performance of ADC12 linearity parameters using the internal reference(2)		0.45	2.4	4.0	
		For specified performance of ADC12 linearity parameters using the internal reference(3)		0.45	2.4	2.7	
$f_{ADC12OSC}$	Internal ADC12 oscillator(4)	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	4.2	4.8	5.4	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, internal oscillator, ADC12OSC used for ADC conversion clock	2.2 V, 3 V	2.4		3.1	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL ≠ 0			$13 \times 1 / f_{ADC12CLK}$		
t_{Sample}	Sampling time	$R_S = 400\ \Omega$, $R_I = 1000\ \Omega$, $C_I = 20$ pF, $t = (R_S + R_I) \times C_I$ (5)	2.2 V, 3 V	1000			ns

(1) REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. AVCC as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC. For other clock sources, the specified performance of the ADC12 linearity is ensured with $f_{ADC12CLK}$ maximum of 5.0 MHz.
(2) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1
(3) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.
(4) The ADC12OSC is sourced directly from MODOSC inside the UCS.
(5) Approximately 10 Tau (t) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

5.37 12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (1)	1.4 V ≤ dVREF ≤ 1.6 V (2)	2.2 V, 3 V			±2.0	LSB
		1.6 V < dVREF (2)				±1.7	
E_D	Differential linearity error (1)	See (2)	2.2 V, 3 V			±1.0	LSB
E_O	Offset error (3)	dVREF ≤ 2.2 V (2)	2.2 V, 3 V		±1.0	±2.0	LSB
		dVREF > 2.2 V (2)			±1.0	±2.0	
E_G	Gain error (3)	See (2)	2.2 V, 3 V		±1.0	±2.0	LSB
E_T	Total unadjusted error	dVREF ≤ 2.2 V (2)	2.2 V, 3 V		±1.4	±3.5	LSB
		dVREF > 2.2 V (2)			±1.4	±3.5	

(1) Parameters are derived using the histogram method.
(2) The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. dVREF = $V_{R+} – V_{R–}$, V_{R+} < AVCC, $V_{R–}$ > AVSS. Unless otherwise mentioned, dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω, and two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF+ and VREF- to decouple the dynamic current. Also see the *MSP430F5xx and MSP430F6xx Family User's Guide*.
(3) Parameters are derived using a best fit curve.

5.38 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1)		V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (2)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ = 4.0 MHz	2.2 V, 3 V			±1.7	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ = 2.7 MHz				±2.5	
E_D	Differential linearity error (2)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ = 4.0 MHz	2.2 V, 3 V	–1.0		+2.0	LSB
		ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ = 2.7 MHz		–1.0		+1.5	
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ = 2.7 MHz		–1.0		+2.5	
E_O	Offset error (3)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ = 4.0 MHz	2.2 V, 3 V		±1.0	±2.0	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ = 2.7 MHz			±1.0	±2.0	
E_G	Gain error (3)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ = 4.0 MHz	2.2 V, 3 V		±1.0	±2.0	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ = 2.7 MHz				±1.5% (4)	VREF
E_T	Total unadjusted error	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ = 4.0 MHz	2.2 V, 3 V		±1.4	±3.5	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ = 2.7 MHz				±1.5% (4)	VREF

(1) The internal reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 1. dVREF = $V_{R+} – V_{R–}$.
(2) Parameters are derived using the histogram method.
(3) Parameters are derived using a best fit curve.
(4) The gain error and total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode the reference voltage used by the ADC12_A is not available on a pin.

5.39 12-Bit ADC, Temperature Sensor and Built-In V_{MID} (1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-16)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{SENSOR}	See (2)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		680		mV
			3 V		680		
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V		2.25		mV/°C
			3 V		2.25		
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected (3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	100			µs
			3 V	100			
V_{MID}	AV_{CC} divider at channel 11, V_{AVCC} factor	ADC12ON = 1, INCH = 0Bh		0.48	0.5	0.52	V_{AVCC}
	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh	2.2 V	1.06	1.1	1.14	V
			3 V	1.44	1.5	1.56	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (4)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V, 3 V	1000			ns

(1) The temperature sensor is provided by the REF module. See the REF module parametric, I_{REF+}, regarding the current consumption of the temperature sensor.

(2) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor. The TLV structure contains calibration values for 30°C ±3°C and 85°C ±3°C for each of the available reference voltage levels. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature,°C}) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy. See also the *MSP430F5xx and MSP430F6xx Family User's Guide*.

(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.

(4) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

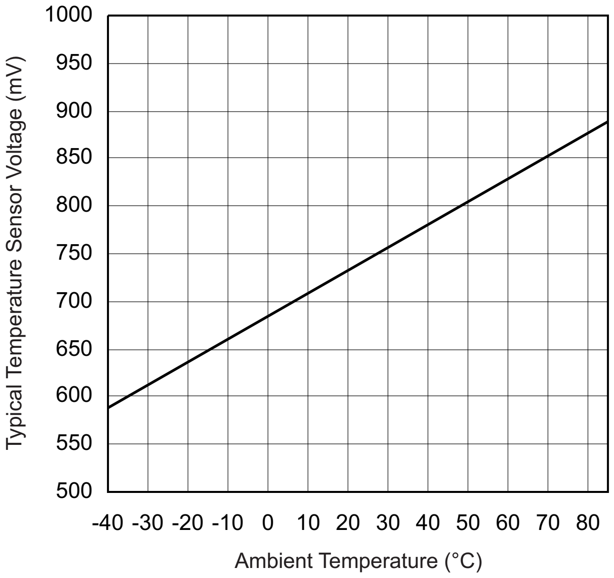


Figure 5-16. Typical Temperature Sensor Voltage

5.40 REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}$ and V_{eREF-} (2)		1.4		AV_{CC}	V
V_{REF-}, V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}$ and V_{eREF-} (3)		0		1.2	V
(V_{eREF+} – V_{REF-} or V_{eREF-})	Differential external reference voltage input	$V_{eREF+} > V_{REF-}$ and V_{eREF-} (4)		1.4		AV_{CC}	V
I_{VeREF+}, $I_{VREF-,VeREF-}$	Static input current	1.4 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, Conversion rate 200 ksps	2.2 V, 3 V	–26		26	µA
		1.4 V ≤ V_{eREF+} ≤ V_{AVCC}, V_{eREF-} = 0 V, $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 8h, Conversion rate 20 ksps		–1		1	µA
C_{VREF+}, C_{VREF-}	Capacitance at V_{VREF+}, V_{VREF-} terminal			(5)10			µF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance (C_i) is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. See also the *MSP430F5xx and MSP430F6xx Family User's Guide*.

5.41 REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = {2} for 2.5 V, REFON = REFOUT = 1, I_{VREF+} = 0 A	3 V	2.4625	2.50	2.5375	V
		REFVSEL = {1} for 2.0 V, REFON = REFOUT = 1, I_{VREF+} = 0 A		1.9503	1.98	2.0097	
		REFVSEL = {0} for 1.5 V, REFON = REFOUT = 1, I_{VREF+} = 0 A	2.2 V, 3 V	1.4677	1.49	1.5124	
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.5 V		2.2			V
		REFVSEL = {1} for 2.0 V		2.3			
		REFVSEL = {2} for 2.5 V		2.8			
I_{REF+}	Operating supply current into AVCC terminal (2) (3)	ADC12SR = 1 (4), REFON = 1, REFOUT = 0, REFBURST = 0	3 V		70	100	µA
		ADC12SR = 1 (4), REFON = 1, REFOUT = 1, REFBURST = 0			0.45	0.75	mA
		ADC12SR = 0 (4), REFON = 1, REFOUT = 0, REFBURST = 0			210	310	µA
		ADC12SR = 0 (4), REFON = 1, REFOUT = 1, REFBURST = 0			0.95	1.7	mA

(1) The reference is supplied to the ADC by the REF module and is buffered locally inside the ADC. The ADC uses two internal buffers, one smaller and one larger for driving the VREF+ terminal. When REFOUT = 1, the reference is available at the VREF+ terminal, as well as, used as the reference for the conversion and uses the larger buffer. When REFOUT = 0, the reference is only used as the reference for the conversion and uses the smaller buffer.
(2) The internal reference current is supplied by the AVCC terminal. Consumption is independent of the ADC12ON control bit, unless a conversion is active. REFOUT = 0 represents the current contribution of the smaller buffer. REFOUT = 1 represents the current contribution of the larger buffer without external load.
(3) The temperature sensor is provided by the REF module. Its current is supplied via terminal AVCC and is equivalent to I_{REF+} with REFON =1 and REFOUT = 0.
(4) For devices without the ADC12, the parametrics with ADC12SR = 0 are applicable.

REF, Built-In Reference *(continued)*

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{L(VREF+)}$	Load-current regulation, VREF+ terminal(5)	REFVSEL = (0, 1, 2), I_{VREF+} = +10 µA, –1000 µA, AV_{CC} = AV_{CC}(min) for each reference level, REFVSEL = (0, 1, 2), REFON = REFOUT = 1				2500	µV/mA
C_{VREF+}	Capacitance at VREF+ terminal	REFON = REFOUT = 1		20		100	pF
TC_{REF+}	Temperature coefficient of built-in reference(6)	I_{VREF+} = 0 A, REFVSEL = (0, 1, 2), REFON = 1, REFOUT = 0 or 1			30	50	ppm/°C
PSRR_DC	Power supply rejection ratio (DC)	AV_{CC} = AV_{CC}(min) to AV_{CC}(max), T_A = 25°C, REFVSEL = (0, 1, 2), REFON = 1, REFOUT = 0 or 1			120	300	µV/V
PSRR_AC	Power supply rejection ratio (AC)	AV_{CC} = AV_{CC}(min) to AV_{CC}(max), T_A = 25°C, f = 1 kHz, ΔVpp = 100 mV, REFVSEL = (0, 1, 2), REFON = 1, REFOUT = 0 or 1			6.4		mV/V
t_{SETTLE}	Settling time of reference voltage(7)	AV_{CC} = AV_{CC}(min) to AV_{CC}(max), REFVSEL = (0, 1, 2), REFOUT = 0, REFON = 0 → 1			75		µs
		AV_{CC} = AV_{CC}(min) to AV_{CC}(max), C_{VREF} = C_{VREF}(max), REFVSEL = (0, 1, 2), REFOUT = 1, REFON = 0 → 1			75		

(5) Contribution only due to the reference and buffer including package. This does not include resistance due to PCB trace.
(6) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C)/(85°C – (–40°C)).
(7) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load when REFOUT = 1.

5.42 Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			1.8		3.6	V
I_{AVCC_COMP}	Comparator operating supply current into AVCC, excludes reference resistor ladder	CBPWRMD = 00	1.8 V			40	µA
			2.2 V		30	50	
			3.0 V		40	65	
		CBPWRMD = 01	2.2 V, 3 V		10	30	
		CBPWRMD = 10	2.2 V, 3 V		0.1	0.5	
I_{AVCC_REF}	Quiescent current of local reference voltage amplifier into AVCC	CBREFACC = 1, CBREFLx = 01				22	µA
V_{IC}	Common mode input range			0		V_{CC} – 1	V
V_{OFFSET}	Input offset voltage	CBPWRMD = 00		–20		20	mV
		CBPWRMD = 01, 10		–10		10	
C_{IN}	Input capacitance				5		pF
R_{SIN}	Series input resistance	On (switch closed)			3	4	kΩ
		Off (switch open)		30			MΩ
t_{PD}	Propagation delay, response time	CBPWRMD = 00, CBF = 0				450	ns
		CBPWRMD = 01, CBF = 0				600	
		CBPWRMD = 10, CBF = 0				50	µs
$t_{PD,filter}$	Propagation delay with filter active	CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 00		0.35	0.6	1.0	µs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01		0.6	1.0	1.8	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10		1.0	1.8	3.4	
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11		1.8	3.4	6.5	
t_{EN_CMP}	Comparator enable time, settling time	CBON = 0 to CBON = 1, CBPWRMD = 00, 01			1	2	µs
		CBON = 0 to CBON = 1, CBPWRMD = 10				100	
t_{EN_REF}	Resistor reference enable time	CBON = 0 to CBON = 1			1	1.5	µs
V_{CB_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder (n = 0 to 31)		VIN × (n + 0.5) / 32	VIN × (n + 1) / 32	VIN × (n + 1.5) / 32	V

5.43 Ports PU.0 and PU.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	V_{USB} = 3.3 V ±10%, I_{OH} = –25 mA, See Figure 5-18 for typical characteristics	2.4		V
V_{OL}	Low-level output voltage	V_{USB} = 3.3 V ±10%, I_{OL} = 25 mA, See Figure 5-17 for typical characteristics		0.4	V
V_{IH}	High-level input voltage	V_{USB} = 3.3 V ±10%, See Figure 5-19 for typical characteristics	2.0		V
V_{IL}	Low-level input voltage	V_{USB} = 3.3 V ±10%, See Figure 5-19 for typical characteristics		0.8	V

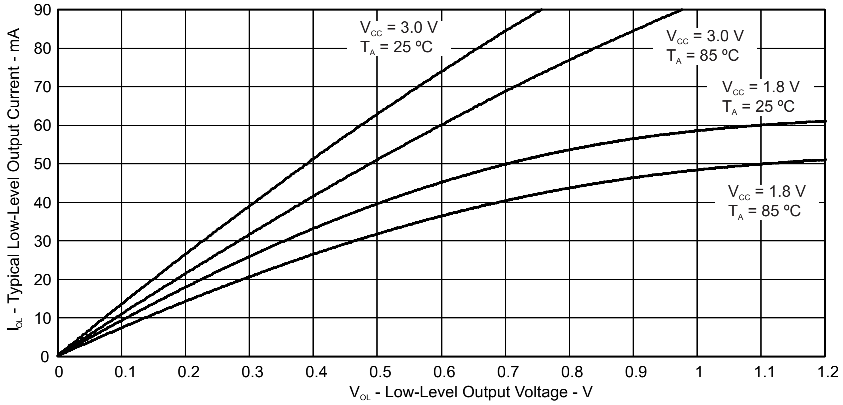


Figure 5-17. Ports PU.0, PU.1 Typical Low-Level Output Characteristics

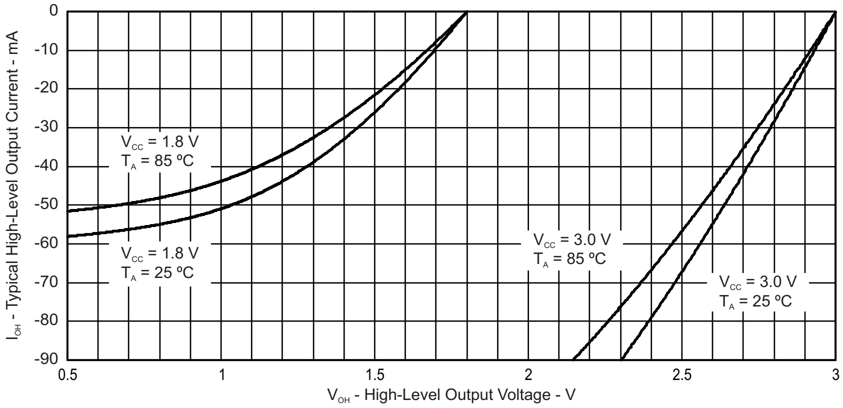


Figure 5-18. Ports PU.0, PU.1 Typical High-Level Output Characteristics

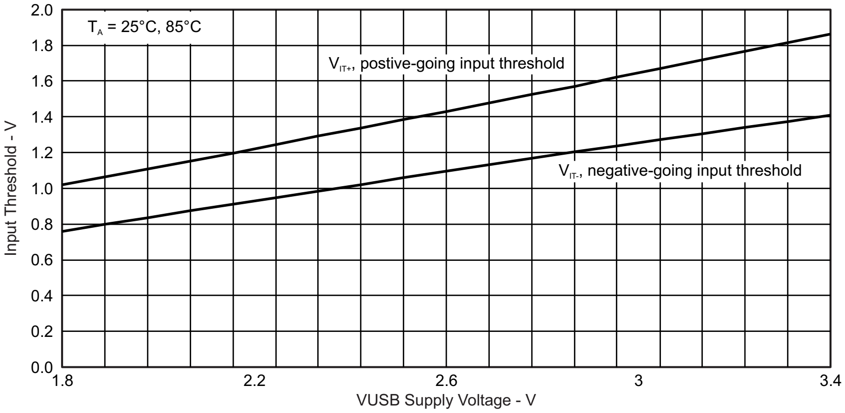


Figure 5-19. Ports PU.0, PU.1 Typical Input Threshold Characteristics

5.44 USB Output Ports DP and DM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	D+, D– single ended	USB 2.0 load conditions	2.8	3.6	V
V_{OL}	D+, D– single ended	USB 2.0 load conditions	0	0.3	V
$Z_{(DRV)}$	D+, D– impedance	Including external series resistor of 27 Ω	28	44	Ω
t_{RISE}	Rise time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns
t_{FALL}	Fall time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4	20	ns

5.45 USB Input Ports DP and DM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$V_{(CM)}$	Differential input common mode range	0.8	2.5	V
$Z_{(IN)}$	Input impedance	300		kΩ
V_{CRS}	Crossover voltage	1.3	2.0	V
V_{IL}	Static SE input logic low level		0.8	V
V_{IH}	Static SE input logic high level	2.0		V
V_{DI}	Differential input voltage		0.2	V

5.46 USB-PWR (USB Power System)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{LAUNCH}	V_{BUS} detection threshold					3.75	V
V_{BUS}	USB bus voltage	Normal operation		3.76		5.5	V
V_{USB}	USB LDO output voltage			3.003	3.3	3.597	V
V_{18}	Internal USB voltage (1)				1.8		V
I_{USB_EXT}	Maximum external current from VUSB terminal (2)	USB LDO is on				12	mA
I_{DET}	USB LDO current overload detection (3)			60		100	mA
$I_{SUSPEND}$	Operating supply current into VBUS terminal (4)	USB LDO is on, USB PLL disabled				250	µA
I_{USB_LDO}	Operating supply current into VBUS terminal, represents the current of the 3.3-V LDO only	USB LDO is on, USB 1.8-V LDO is disabled, V_{BUS} = 5.0 V, USBDETEN = 0 or 1	1.8 V, 3 V		60		µA
I_{VBUS_DETECT}	Operating supply current into VBUS terminal, represents the current of the VBUS detection logic	USB LDO is disabled, USB 1.8-V LDO is disabled, VBUS > V_{LAUNCH}, USBDETEN = 1	1.8 V, 3 V		30		µA
C_{BUS}	VBUS terminal recommended capacitance				4.7		µF
C_{USB}	VUSB terminal recommended capacitance				220		nF
C_{18}	V18 terminal recommended capacitance				220		nF
t_{ENABLE}	Settling time V_{USB} and V_{18}	Within 2%, recommended capacitances				2	ms
R_{PUR}	Pullup resistance of PUR terminal (5)			70	110	150	Ω

(1) This voltage is for internal uses only. No external DC loading should be applied.
(2) This represents additional current that can be supplied to the application from the VUSB terminal beyond the needs of the USB operation.
(3) A current overload is detected when the total current supplied from the USB LDO, including I_{USB_EXT}, exceeds this value.
(4) Does not include current contribution of Rpu and Rpd as outlined in the USB specification.
(5) This value, in series with an external resistor between PUR and D+, produces the Rpu as outlined in the USB specification.

5.47 USB-PLL (USB Phase-Locked Loop)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PLL}	Operating supply current				7	mA
f_{PLL}	PLL frequency			48		MHz
f_{UPD}	PLL reference frequency		1.5		3	MHz
t_{LOCK}	PLL lock time				2	ms
t_{Jitter}	PLL jitter			1000		ps

5.48 Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_J	MIN	TYP	MAX	UNIT
$DV_{CC(PGM,ERASE)}$	Program and erase supply voltage		1.8		3.6	V
I_{PGM}	Average supply current from DVCC during program(1)			3	5	mA
I_{ERASE}	Average supply current from DVCC during erase(1)			6	11	mA
I_{MERASE}, I_{BANK}	Average supply current from DVCC during mass erase or bank erase(1)			6	11	mA
t_{CPT}	Cumulative program time(2)				16	ms
	Program and erase endurance		10^4	10^5		cycles
$t_{Retention}$	Data retention duration	25°C	100			years
t_{Word}	Word or byte program time(3)		64		85	µs
$t_{Block,\ 0}$	Block program time for first byte or word(3)		49		65	µs
$t_{Block,\ 1–(N–1)}$	Block program time for each additional byte or word, except for last byte or word(3)		37		49	µs
$t_{Block,\ N}$	Block program time for last byte or word(3)		55		73	µs
t_{Erase}	Erase time for segment, mass erase, and bank erase when available(3)		23		32	ms
$f_{MCLK,MGR}$	MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1)		0		1	MHz

(1) Default clock system frequency of MCLK = 1 MHz, ACLK = 32768 Hz, SMCLK = 1 MHz. No peripherals are enabled or active.
(2) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word- or byte-write and block-write modes.
(3) These values are hardwired into the state machine of the flash controller.

5.49 JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	0.025		15	µs
$t_{SBW,\ En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge)(1)	2.2 V, 3 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency, 4-wire JTAG(2)	2.2 V	0		5	MHz
		3 V	0		10	
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3 V	45	60	80	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 CPU (Link to User's Guide)

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see Figure 6-1).

Peripherals are connected to the CPU using data, address, and control buses. The peripherals can be managed with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

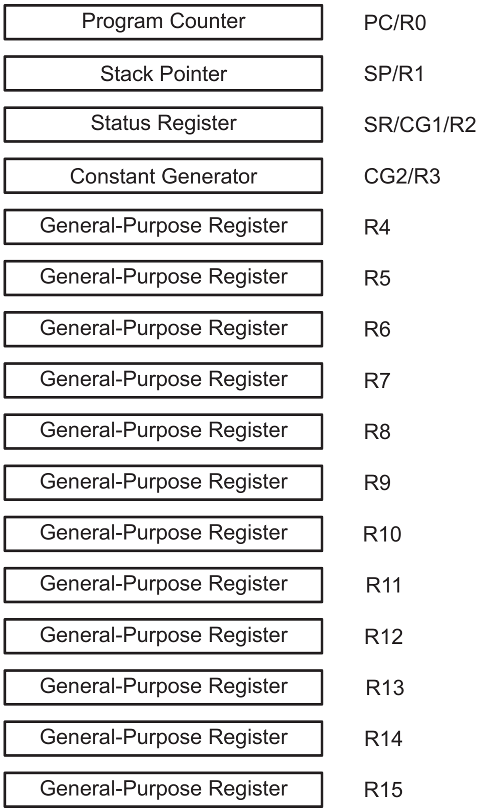

Program Counter
PC/R0
Stack Pointer
SP/R1
Status Register
SR/CG1/R2
Constant Generator
CG2/R3
General-Purpose Register
R4
General-Purpose Register
R5
General-Purpose Register
R6
General-Purpose Register
R7
General-Purpose Register
R8
General-Purpose Register
R9
General-Purpose Register
R10
General-Purpose Register
R11
General-Purpose Register
R12
General-Purpose Register
R13
General-Purpose Register
R14
General-Purpose Register
R15

Figure 6-1. Integrated CPU Registers

6.2 Operating Modes

These microcontrollers have one active mode and six software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - Wake-up signal from $\overline{\text{RST}}$/NMI, P1, and P2

6.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see Table 6-1). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-1. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up External reset Watchdog time-out, password violation Flash memory password violation	WDTIFG, KEYV (SYSRSTIV)(1)(2)	Reset	0FFFEh	63, highest
System NMI PMM Vacant memory access JTAG mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV)(1)	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator fault Flash memory access violation	NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV)(1)(2)	(Non)maskable	0FFFAh	61
Comp_B	Comparator B interrupt flags (CBIV)(1)(3)	Maskable	0FFF8h	60
TB0	TB0CCR0 CCIFG0(3)	Maskable	0FFF6h	59
TB0	TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TB0IV)(1)(3)	Maskable	0FFF4h	58
Watchdog Timer_A interval timer mode	WDTIFG	Maskable	0FFF2h	57
USCI_A0 receive or transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV)(1)(3)	Maskable	0FFF0h	56
USCI_B0 receive or transmit	UCB0RXIFG, UCB0TXIFG (UCB0IV)(1)(3)	Maskable	0FFEEh	55
ADC12_A	ADC12IFG0 to ADC12IFG15 (ADC12IV)(1)(3)(4)	Maskable	0FFECh	54
TA0	TA0CCR0 CCIFG0(3)	Maskable	0FFEAh	53
TA0	TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV)(1)(3)	Maskable	0FFE8h	52
USB_UBM	USB interrupts (USBIV)(1)(3)	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV)(1)(3)	Maskable	0FFE4h	50
TA1	TA1CCR0 CCIFG0(3)	Maskable	0FFE2h	49
TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV)(1)(3)	Maskable	0FFE0h	48
I/O port P1	P1IFG.0 to P1IFG.7 (P1IV)(1)(3)	Maskable	0FFDEh	47
USCI_A1 receive or transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV)(1)(3)	Maskable	0FFDCh	46
USCI_B1 receive or transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV)(1)(3)	Maskable	0FFDAh	45
TA2	TA2CCR0 CCIFG0(3)	Maskable	0FFD8h	44
TA2	TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV)(1)(3)	Maskable	0FFD6h	43
I/O port P2	P2IFG.0 to P2IFG.7 (P2IV)(1)(3)	Maskable	0FFD4h	42
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV)(1)(3)	Maskable	0FFD2h	41
Reserved	Reserved(5)		0FFD0h	40
			⋮	⋮
			0FF80h	0, lowest

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space. (Non)maskable: the individual interrupt enable bit can disable an interrupt event, but the general interrupt enable bit cannot disable it.
(3) Interrupt flags are in the module.
(4) Only on devices with ADC, otherwise reserved.
(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

6.4 Memory Organization

Table 6-2 summarizes the memory map of the devices.

Table 6-2. Memory Organization(1)

		MSP430F5522 MSP430F5521 MSP430F5513	MSP430F5525 MSP430F5524 MSP430F5515 MSP430F5514	MSP430F5527 MSP430F5526 MSP430F5517	MSP430F5529 MSP430F5528 MSP430F5519
Memory (flash) Main: interrupt vector	Total Size	32KB 00FFFFh to 00FF80h	64KB 00FFFFh to 00FF80h	96KB 00FFFFh to 00FF80h	128KB 00FFFFh to 00FF80h
Main: code memory	Bank D	N/A	N/A	N/A	32KB 0243FFh to 01C400h
	Bank C	N/A	N/A	32KB 01C3FFh to 014400h	32KB 01C3FFh to 014400h
	Bank B	15KB 00FFFFh to 00C400h	32KB 0143FFh to 00C400h	32KB 0143FFh to 00C400h	32KB 0143FFh to 00C400h
	Bank A	17KB 00C3FFh to 008000h	32KB 00C3FFh to 004400h	32KB 00C3FFh to 004400h	32KB 00C3FFh to 004400h
RAM	Sector 3	2KB(2) 0043FFh to 003C00h	N/A	N/A	2KB 0043FFh to 003C00h
	Sector 2	2KB(3) 003BFFh to 003400h	N/A	2KB 003BFFh to 003400h	2KB 003BFFh to 003400h
	Sector 1	2KB 0033FFh to 002C00h	2KB 0033FFh to 002C00h	2KB 0033FFh to 002C00h	2KB 0033FFh to 002C00h
	Sector 0	2KB 002BFFh to 002400h	2KB 002BFFh to 002400h	2KB 002BFFh to 002400h	2KB 002BFFh to 002400h
USB RAM(4)	Sector 7	2KB 0023FFh to 001C00h	2KB 0023FFh to 001C00h	2KB 0023FFh to 001C00h	2KB 0023FFh to 001C00h
Information memory (flash)	Info A	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h
	Info B	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h
	Info C	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h
	Info D	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h
Bootloader (BSL) memory (flash)	BSL 3	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h
	BSL 2	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h
	BSL 1	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h
	BSL 0	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h
Peripherals	Size	4KB 000FFFh to 0h	4KB 000FFFh to 0h	4KB 000FFFh to 0h	4KB 000FFFh to 0h

(1) N/A = Not available
(2) MSP430F5522 only
(3) MSP430F5522 and MSP430F5521 only
(4) USB RAM can be used as general purpose RAM when not used for USB operation.

6.5 Bootloader (BSL)

The BSL enables users to program the flash memory or RAM using various serial interfaces. Access to the device memory by the BSL is protected by an user-defined password. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For complete description of the features of the BSL and its implementation, see *MSP430 Programming With the Bootloader (BSL)*.

6.5.1 USB BSL

All devices come preprogrammed with the USB BSL. Table 6-3 lists the required pins for the USB BSL. In addition to these pins, the application must support external components necessary for normal USB operation; for example, the proper crystal on XT2IN and XT2OUT, proper decoupling, and so on.

Table 6-3. USB BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
PU.0/DP	USB data terminal DP
PU.1/DM	USB data terminal DM
PUR	USB pullup resistor terminal
VBUS	USB bus power supply
VSSU	USB ground supply

NOTE

The default USB BSL evaluates the logic level of the PUR pin after a BOR reset. If the PUR pin is pulled high externally, then the BSL is invoked. Therefore, unless the application is invoking the BSL, it is important to keep PUR pulled low after a BOR reset, even if BSL or USB is never used. TI recommends applying a 1-MΩ resistor to ground.

6.5.2 UART BSL

A UART BSL is also available that can be programmed by the user into the BSL memory by replacing the preprogrammed, factory supplied, USB BSL. Table 6-4 lists the required pins for the UART BSL.

Table 6-4. UART BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.1	Data transmit
P1.2	Data receive
VCC	Power supply
VSS	Ground supply

6.6 JTAG Operation

6.6.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. Table 6-5 lists the required pins for the JTAG interface. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming With the JTAG Interface*.

Table 6-5. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

6.6.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. Table 6-6 lists the required pins for the Spy-Bi-Wire interface. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*. For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming With the JTAG Interface*.

Table 6-6. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

6.7 Flash Memory (Link to User's Guide)

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

6.8 RAM (Link to User's Guide)

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however; all data is lost. Features of the RAM include:

- RAM has n sectors. The size of a sector can be found in Section 6.4.
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.
- For devices that contain USB memory, the USB memory can be used as normal RAM if USB is not required.

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. Peripherals can be controlled using all instructions. For complete module descriptions, see the *MSP430F5xx and MSP430F6xx Family User's Guide*.

6.9.1 Digital I/O (Link to User's Guide)

Up to eight 8-bit I/O ports are implemented: For 80-pin packages, P1, P2, P3, P4, P5, P6, and P7 are complete, and P8 is reduced to 3-bit I/O. For 64-pin packages, P3 and P5 are reduced to 5-bit I/O and 6-bit I/O, respectively, and P7 and P8 are completely removed. Port PJ contains four individual I/O ports, common to all devices.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- All bits of ports P1 and P2 support edge-selectable interrupt and LPM4.5 wake-up input.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P8) or word-wise in pairs (PA through PD).

6.9.2 Port Mapping Controller (Link to User's Guide)

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P4 (see Table 6-7). Table 6-8 shows the default mappings.

Table 6-7. Port Mapping Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_CBOUT0	-	Comparator_B output
	PM_TB0CLK	TB0 clock input	
2	PM_ADC12CLK	-	ADC12CLK
	PM_DMAE0	DMAE0 input	
3	PM_SVMOUT	-	SVM output
	PM_TB0OUTH	TB0 high impedance input TB0OUTH	
4	PM_TB0CCR0A	TB0 CCR0 capture input CCI0A	TB0 CCR0 compare output Out0
5	PM_TB0CCR1A	TB0 CCR1 capture input CCI1A	TB0 CCR1 compare output Out1
6	PM_TB0CCR2A	TB0 CCR2 capture input CCI2A	TB0 CCR2 compare output Out2
7	PM_TB0CCR3A	TB0 CCR3 capture input CCI3A	TB0 CCR3 compare output Out3
8	PM_TB0CCR4A	TB0 CCR4 capture input CCI4A	TB0 CCR4 compare output Out4
9	PM_TB0CCR5A	TB0 CCR5 capture input CCI5A	TB0 CCR5 compare output Out5
10	PM_TB0CCR6A	TB0 CCR6 capture input CCI6A	TB0 CCR6 compare output Out6
11	PM_UCA1RXD	USCI_A1 UART RXD (Direction controlled by USCI – input)	
	PM_UCA1SOMI	USCI_A1 SPI slave out master in (direction controlled by USCI)	
12	PM_UCA1TXD	USCI_A1 UART TXD (Direction controlled by USCI – output)	
	PM_UCA1SIMO	USCI_A1 SPI slave in master out (direction controlled by USCI)	
13	PM_UCA1CLK	USCI_A1 clock input/output (direction controlled by USCI)	
	PM_UCB1STE	USCI_B1 SPI slave transmit enable (direction controlled by USCI)	
14	PM_UCB1SOMI	USCI_B1 SPI slave out master in (direction controlled by USCI)	
	PM_UCB1SCL	USCI_B1 I^2C clock (open drain and direction controlled by USCI)	
15	PM_UCB1SIMO	USCI_B1 SPI slave in master out (direction controlled by USCI)	
	PM_UCB1SDA	USCI_B1 I^2C data (open drain and direction controlled by USCI)	
16	PM_UCB1CLK	USCI_B1 clock input/output (direction controlled by USCI)	
	PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI)	
17	PM_CBOUT1	None	Comparator_B output
18	PM_MCLK	None	MCLK
19–30	Reserved	None	DVSS
31 (0FFh)(1)	PM_ANALOG	Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide, and the upper bits are ignored, resulting in a read out value of 31.

Table 6-8. Default Mapping

PIN	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P4.0/P4MAP0	PM_UCB1STE/PM_UCA1CLK	USCI_B1 SPI slave transmit enable (direction controlled by USCI) USCI_A1 clock input/output (direction controlled by USCI)	
P4.1/P4MAP1	PM_UCB1SIMO/PM_UCB1SDA	USCI_B1 SPI slave in master out (direction controlled by USCI) USCI_B1 I^{2}C data (open drain and direction controlled by USCI)	
P4.2/P4MAP2	PM_UCB1SOMI/PM_UCB1SCL	USCI_B1 SPI slave out master in (direction controlled by USCI) USCI_B1 I^{2}C clock (open drain and direction controlled by USCI)	
P4.3/P4MAP3	PM_UCB1CLK/PM_UCA1STE	USCI_A1 SPI slave transmit enable (direction controlled by USCI) USCI_B1 clock input/output (direction controlled by USCI)	
P4.4/P4MAP4	PM_UCA1TXD/PM_UCA1SIMO	USCI_A1 UART TXD (Direction controlled by USCI – output) USCI_A1 SPI slave in master out (direction controlled by USCI)	
P4.5/P4MAP5	PM_UCA1RXD/PM_UCA1SOMI	USCI_A1 UART RXD (Direction controlled by USCI – input) USCI_A1 SPI slave out master in (direction controlled by USCI)	
P4.6/P4MAP6	PM_NONE	None	DVSS
P4.7/P4MAP7	PM_NONE	None	DVSS

6.9.3 Oscillator and System Clock *(Link to User's Guide)*

The clock system in the MSP430F552x and MSP430F551x family of devices is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (XT1 in LF mode) (XT1 in HF mode is not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator (XT2). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency-locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turnon clock source and stabilizes in 3.5 µs (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally controlled oscillator (DCO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

6.9.4 Power-Management Module (PMM) *(Link to User's Guide)*

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (SVS) (the device is automatically reset) and supply voltage monitoring (SVM) (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

6.9.5 Hardware Multiplier *(Link to User's Guide)*

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

6.9.6 Real-Time Clock (RTC_A) (Link to User's Guide)

The RTC_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated real-time clock (RTC) (calendar mode). In counter mode, the RTC_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_A also supports flexible alarm functions and offset-calibration hardware.

6.9.7 Watchdog Timer (WDT_A) (Link to User's Guide)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.9.8 System Module (SYS) (Link to User's Guide)

The SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, bootstrap loader entry mechanisms, and configuration management (device descriptors). It also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application. Table 6-9 lists the SYS module interrupt vector registers.

Table 6-9. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		$\overline{\text{RST}}$/NMI (POR)	04h	
		PMMSWBOR (BOR)	06h	
		Wakeup from LPMx.5	08h	
		Security violation (BOR)	0Ah	
		SVSL (POR)	0Ch	
		SVSH (POR)	0Eh	
		SVML_OVP (POR)	10h	
		SVMH_OVP (POR)	12h	
		PMMSWPOR (POR)	14h	
		WDT time-out (PUC)	16h	
		WDT password violation (PUC)	18h	
		KEYV flash password violation (PUC)	1Ah	
		Reserved	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMM password violation (PUC)	20h	
		Reserved	22h to 3Eh	Lowest

Table 6-9. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		SVMLIFG	02h	Highest
		SVMHIFG	04h	
		SVSMLDLYIFG	06h	
		SVSMHDLYIFG	08h	
		VMAIFG	0Ah	
		JMBINIFG	0Ch	
		JMBOUTIFG	0Eh	
		SVMLVLRIFG	10h	
		SVMHVLRIFG	12h	
		Reserved	14h to 1Eh	Lowest
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIIFG	02h	Highest
		OFIFG	04h	
		ACCVIFG	06h	
		BUSIFG	08h	
		Reserved	0Ah to 1Eh	Lowest

6.9.9 DMA Controller (Link to User's Guide)

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

The USB timestamp generator also uses the DMA trigger assignments described in Table 6-10.

Table 6-10. DMA Trigger Assignments[1]

TRIGGER	CHANNEL		
	0	1	2
0	DMAREQ	DMAREQ	DMAREQ
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG
5	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG
6	TA2CCR2 CCIFG	TA2CCR2 CCIFG	TA2CCR2 CCIFG
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG
9	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved
11	Reserved	Reserved	Reserved
12	Reserved	Reserved	Reserved
13	Reserved	Reserved	Reserved
14	Reserved	Reserved	Reserved
15	Reserved	Reserved	Reserved

(1) If a reserved trigger source is selected, no Trigger1 is generated.

Table 6-10. DMA Trigger Assignments[1] (continued)

TRIGGER	CHANNEL		
	0	1	2
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG
18	UCB0RXIFG	UCB0RXIFG	UCB0RXIFG
19	UCB0TXIFG	UCB0TXIFG	UCB0TXIFG
20	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG
21	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG
22	UCB1RXIFG	UCB1RXIFG	UCB1RXIFG
23	UCB1TXIFG	UCB1TXIFG	UCB1TXIFG
24	ADC12IFGx(2)	ADC12IFGx(2)	ADC12IFGx(2)
25	Reserved	Reserved	Reserved
26	Reserved	Reserved	Reserved
27	USB FNRXD	USB FNRXD	USB FNRXD
28	USB ready	USB ready	USB ready
29	MPY ready	MPY ready	MPY ready
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

(2) Only on devices with ADC. Reserved on devices without ADC.

6.9.10 Universal Serial Communication Interface (USCI) (Links to User's Guide: UART Mode, SPI Mode, I^2C Mode)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3- or 4-pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3- or 4-pin) or I^2C.

The MSP430F55xx series includes two complete USCI modules (n = 0, 1).

6.9.11 TA0 (Link to User's Guide)

TA0 is a 16-bit timer and counter (Timer_A type) with five capture/compare registers. TA0 can support multiple capture/compare registers, PWM outputs, and interval timing (see Table 6-11). TA0 also has extensive interrupt capabilities. Interrupts can be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-11. TA0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, YFF, ZQE	**PN**						**RGC, YFF, ZQE**	**PN**
18, B7, H2 - P1.0	21 - P1.0	TA0CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
18, B7, H2 - P1.0	21 - P1.0	TA0CLK	$\overline{\text{TACLK}}$					
19, B6, H3 - P1.1	22 - P1.1	TA0.0	CCI0A	CCR0	TA0	TA0.0	19, B6, H3 - P1.1	22 - P1.1
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
20, C6, J3 - P1.2	23 - P1.2	TA0.1	CCI1A	CCR1	TA1	TA0.1	20, C6, J3 - P1.2	23 - P1.2
		CBOUT (internal)	CCI1B				ADC12 (internal) (1) ADC12SHSx = {1}	ADC12 (internal) (1) ADC12SHSx = {1}
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
21, C8, G4 - P1.3	24 - P1.3	TA0.2	CCI2A	CCR2	TA2	TA0.2	21, C8, G4 - P1.3	24 - P1.3
		ACLK (internal)	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
22, C7, H4 - P1.4	25 - P1.4	TA0.3	CCI3A	CCR3	TA3	TA0.3	22, C7, H4 - P1.4	25 - P1.4
		DV_{SS}	CCI3B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
23, D6, J4 - P1.5	26 - P1.5	TA0.4	CCI4A	CCR4	TA4	TA0.4	23, D6, J4 - P1.5	26 - P1.5
		DV_{SS}	CCI4B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

(1) Only on devices with ADC.

6.9.12 TA1 (Link to User's Guide)

TA1 is a 16-bit timer and counter (Timer_A type) with three capture/compare registers. TA1 can support multiple capture/compare registers, PWM outputs, and interval timing (see Table 6-12). TA1 also has extensive interrupt capabilities. Interrupts can be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-12. TA1 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, YFF, ZQE	PN						RGC, YFF, ZQE	PN
24, D7, G5 - P1.6	27 - P1.6	TA1CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
24, D7, G5 - P1.6	27 - P1.6	TA1CLK	$\overline{\text{TACLK}}$					
25, D8, H5 - P1.7	28 - P1.7	TA1.0	CCI0A	CCR0	TA0	TA1.0	25, D8, H5 - P1.7	28 - P1.7
		DV$_{SS}$	CCI0B					
		DV$_{SS}$	GND					
		DV$_{CC}$	V$_{CC}$					
26, E5, J5 - P2.0	29 - P2.0	TA1.1	CCI1A	CCR1	TA1	TA1.1	26, E5, J5 - P2.0	29 - P2.0
		CBOUT (internal)	CCI1B					
		DV$_{SS}$	GND					
		DV$_{CC}$	V$_{CC}$					
27, E8, G6 - P2.1	30 - P2.1	TA1.2	CCI2A	CCR2	TA2	TA1.2	27, E8, G6 - P2.1	30 - P2.1
		ACLK (internal)	CCI2B					
		DV$_{SS}$	GND					
		DV$_{CC}$	V$_{CC}$					

6.9.13 TA2 (Link to User's Guide)

TA2 is a 16-bit timer and counter (Timer_A type) with three capture/compare registers. TA2 can support multiple capture/compare registers, PWM outputs, and interval timing (see Table 6-13). TA2 also has extensive interrupt capabilities. Interrupts can be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-13. TA2 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, YFF, ZQE	PN						RGC, YFF, ZQE	PN
28, E7, J6 - P2.2	31 - P2.2	TA2CLK	TACLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
28, E7, J6 - P2.2	31 - P2.2	TA2CLK	$\overline{\text{TACLK}}$					
29, E6, H6 - P2.3	32 - P2.3	TA2.0	CCI0A	CCR0	TA0	TA2.0	29, E6, H6 - P2.3	32 - P2.3
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
30, F8, J7 - P2.4	33 - P2.4	TA2.1	CCI1A	CCR1	TA1	TA2.1	30, F8, J7 - P2.4	33 - P2.4
		CBOUT (internal)	CCI1B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
31, F7, J8 - P2.5	34 - P2.5	TA2.2	CCI2A	CCR2	TA2	TA2.2	31, F7, J8 - P2.5	34 - P2.5
		ACLK (internal)	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

6.9.14 TB0 (Link to User's Guide)

TB0 is a 16-bit timer and counter (Timer_B type) with seven capture/compare registers. TB0 can support multiple capture/compare registers, PWM outputs, and interval timing (see Table 6-14). TB0 also has extensive interrupt capabilities. Interrupts can be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-14. TB0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
RGC, YFF, ZQE (1)	PN						RGC, YFF, ZQE (1)	PN
	60 - P7.7	TB0CLK	TBCLK	Timer	NA	NA		
		ACLK (internal)	ACLK					
		SMCLK (internal)	SMCLK					
	60 - P7.7	TB0CLK	$\overline{\text{TBCLK}}$					
	55 - P5.6	TB0.0	CCI0A	CCR0	TB0	TB0.0		55 - P5.6
	55 - P5.6	TB0.0	CCI0B				ADC12 (internal) (2) ADC12SHSx = {2}	ADC12 (internal) (2) ADC12SHSx = {2}
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
	56 - P5.7	TB0.1	CCI1A	CCR1	TB1	TB0.1		56 - P5.7
		CBOUT (internal)	CCI1B				ADC12 (internal) ADC12SHSx = {3}	ADC12 (internal) ADC12SHSx = {3}
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
	57 - P7.4	TB0.2	CCI2A	CCR2	TB2	TB0.2		57 - P7.4
	57 - P7.4	TB0.2	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
	58 - P7.5	TB0.3	CCI3A	CCR3	TB3	TB0.3		58 - P7.5
	58 - P7.5	TB0.3	CCI3B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
	59 - P7.6	TB0.4	CCI4A	CCR4	TB4	TB0.4		59 - P7.6
	59 - P7.6	TB0.4	CCI4B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
	42 - P3.5	TB0.5	CCI5A	CCR5	TB5	TB0.5		42 - P3.5
	42 - P3.5	TB0.5	CCI5B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
	43 - P3.6	TB0.6	CCI6A	CCR6	TB6	TB0.6		43 - P3.6
		ACLK (internal)	CCI6B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

(1) Timer functions are selectable through the port mapping controller.
(2) Only on devices with ADC

6.9.15 Comparator_B (Link to User's Guide)

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

6.9.16 ADC12_A (Link to User's Guide)

The ADC12_A module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

6.9.17 CRC16 (Link to User's Guide)

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.9.18 Voltage Reference (REF) Module (Link to User's Guide)

The REF module generates all critical reference voltages that can be used by the various analog peripherals in the device.

6.9.19 Universal Serial Bus (USB) (Link to User's Guide)

The USB module is a fully integrated USB interface that is compliant with the USB 2.0 specification. The module supports full-speed operation of control, interrupt, and bulk transfers. The module includes an integrated LDO, PHY, and PLL. The PLL is highly flexible and supports a wide range of input clock frequencies. USB RAM, when not used for USB communication, can be used by the system.

6.9.20 Embedded Emulation Module (EEM) (Link to User's Guide)

The EEM supports real-time in-system debugging. The L version of the EEM has the following features:

- Eight hardware triggers or breakpoints on memory access
- Two hardware triggers or breakpoints on CPU register write access
- Up to 10 hardware triggers can be combined to form complex triggers or breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

6.9.21 Peripheral File Map

Table 6-15 lists the base address for the registers of each module. Table 6-16 through Table 6-45 list the available registers in each module.

Table 6-15. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see Table 6-16)	0100h	000h to 01Fh
PMM (see Table 6-17)	0120h	000h to 010h
Flash Control (see Table 6-18)	0140h	000h to 00Fh
CRC16 (see Table 6-19)	0150h	000h to 007h
RAM Control (see Table 6-20)	0158h	000h to 001h
Watchdog (see Table 6-21)	015Ch	000h to 001h
UCS (see Table 6-22)	0160h	000h to 01Fh
SYS (see Table 6-23)	0180h	000h to 01Fh
Shared Reference (see Table 6-24)	01B0h	000h to 001h
Port Mapping Control (see Table 6-25)	01C0h	000h to 002h
Port Mapping Port P4 (see Table 6-25)	01E0h	000h to 007h
Port P1 and P2 (see Table 6-26)	0200h	000h to 01Fh
Port P3 and P4 (see Table 6-27)	0220h	000h to 00Bh
Port P5 and P6 (see Table 6-28)	0240h	000h to 00Bh
Port P7 and P8 (see Table 6-29)	0260h	000h to 00Bh
Port PJ (see Table 6-30)	0320h	000h to 01Fh
TA0 (see Table 6-31)	0340h	000h to 02Eh
TA1 (see Table 6-32)	0380h	000h to 02Eh
TB0 (see Table 6-33)	03C0h	000h to 02Eh
TA2 (see Table 6-34)	0400h	000h to 02Eh
Real-Time Clock (RTC_A) (see Table 6-35)	04A0h	000h to 01Bh
32-Bit Hardware Multiplier (see Table 6-36)	04C0h	000h to 02Fh
DMA General Control (see Table 6-37)	0500h	000h to 00Fh
DMA Channel 0 (see Table 6-37)	0510h	000h to 00Ah
DMA Channel 1 (see Table 6-37)	0520h	000h to 00Ah
DMA Channel 2 (see Table 6-37)	0530h	000h to 00Ah
USCI_A0 (see Table 6-38)	05C0h	000h to 01Fh
USCI_B0 (see Table 6-39)	05E0h	000h to 01Fh
USCI_A1 (see Table 6-40)	0600h	000h to 01Fh
USCI_B1 (see Table 6-41)	0620h	000h to 01Fh
ADC12_A (see Table 6-42)	0700h	000h to 03Eh
Comparator_B (see Table 6-43)	08C0h	000h to 00Fh
USB Configuration (see Table 6-44)	0900h	000h to 014h
USB Control (see Table 6-45)	0920h	000h to 01Fh

Table 6-16. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 6-17. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high-side control	SVSMHCTL	04h
SVS low-side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM power mode 5 control	PM5CTL0	10h

Table 6-18. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 6-19. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 6-20. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 6-21. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 6-22. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

Table 6-23. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 6-24. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

Table 6-25. Port Mapping Registers (Base Address of Port Mapping Control: 01C0h, Port P4: 01E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping key and ID	PMAPKEYID	00h
Port mapping control	PMAPCTL	02h
Port P4.0 mapping	P4MAP0	00h
Port P4.1 mapping	P4MAP1	01h
Port P4.2 mapping	P4MAP2	02h
Port P4.3 mapping	P4MAP3	03h
Port P4.4 mapping	P4MAP4	04h
Port P4.5 mapping	P4MAP5	05h
Port P4.6 mapping	P4MAP6	06h
Port P4.7 mapping	P4MAP7	07h

Table 6-26. Port P1 and P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 resistor enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 resistor enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 6-27. Port P3 and P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 resistor enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 resistor enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh

Table 6-28. Port P5 and P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 resistor enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 resistor enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh

Table 6-29. Port P7 and P8 Registers (Base Address: 0260h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 input	P7IN	00h
Port P7 output	P7OUT	02h
Port P7 direction	P7DIR	04h
Port P7 resistor enable	P7REN	06h
Port P7 drive strength	P7DS	08h
Port P7 selection	P7SEL	0Ah
Port P8 input	P8IN	01h
Port P8 output	P8OUT	03h
Port P8 direction	P8DIR	05h
Port P8 resistor enable	P8REN	07h
Port P8 drive strength	P8DS	09h
Port P8 selection	P8SEL	0Bh

Table 6-30. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ resistor enable	PJREN	06h
Port PJ drive strength	PJDS	08h

Table 6-31. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter	TA0R	10h
Capture/compare 0	TA0CCR0	12h
Capture/compare 1	TA0CCR1	14h
Capture/compare 2	TA0CCR2	16h
Capture/compare 3	TA0CCR3	18h
Capture/compare 4	TA0CCR4	1Ah
TA0 expansion 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 6-32. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter	TA1R	10h
Capture/compare 0	TA1CCR0	12h
Capture/compare 1	TA1CCR1	14h
Capture/compare 2	TA1CCR2	16h
TA1 expansion 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 6-33. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
Capture/compare 3	TB0CCR3	18h
Capture/compare 4	TB0CCR4	1Ah
Capture/compare 5	TB0CCR5	1Ch
Capture/compare 6	TB0CCR6	1Eh
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 6-34. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
Capture/compare control 2	TA2CCTL2	06h
TA2 counter	TA2R	10h
Capture/compare 0	TA2CCR0	12h
Capture/compare 1	TA2CCR1	14h
Capture/compare 2	TA2CCR2	16h
TA2 expansion 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

Table 6-35. Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds, RTC counter 1	RTCSEC, RTCNT1	10h
RTC minutes, RTC counter 2	RTCMIN, RTCNT2	11h
RTC hours, RTC counter 3	RTCHOUR, RTCNT3	12h
RTC day of week, RTC counter 4	RTCDOW, RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh

Table 6-36. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control 0	MPY32CTL0	2Ch

Table 6-37. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Eh

Table 6-38. USCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA0CTL1	00h
USCI control 0	UCA0CTL0	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

Table 6-39. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB0CTL1	00h
USCI synchronous control 0	UCB0CTL0	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

Table 6-40. USCI_A1 Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA1CTL1	00h
USCI control 0	UCA1CTL0	01h
USCI baud rate 0	UCA1BR0	06h
USCI baud rate 1	UCA1BR1	07h
USCI modulation control	UCA1MCTL	08h
USCI status	UCA1STAT	0Ah
USCI receive buffer	UCA1RXBUF	0Ch
USCI transmit buffer	UCA1TXBUF	0Eh
USCI LIN control	UCA1ABCTL	10h
USCI IrDA transmit control	UCA1IRTCTL	12h
USCI IrDA receive control	UCA1IRRCTL	13h
USCI interrupt enable	UCA1IE	1Ch
USCI interrupt flags	UCA1IFG	1Dh
USCI interrupt vector word	UCA1IV	1Eh

Table 6-41. USCI_B1 Registers (Base Address: 0620h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB1CTL1	00h
USCI synchronous control 0	UCB1CTL0	01h
USCI synchronous bit rate 0	UCB1BR0	06h
USCI synchronous bit rate 1	UCB1BR1	07h
USCI synchronous status	UCB1STAT	0Ah
USCI synchronous receive buffer	UCB1RXBUF	0Ch
USCI synchronous transmit buffer	UCB1TXBUF	0Eh
USCI I2C own address	UCB1I2COA	10h
USCI I2C slave address	UCB1I2CSA	12h
USCI interrupt enable	UCB1IE	1Ch
USCI interrupt flags	UCB1IFG	1Dh
USCI interrupt vector word	UCB1IV	1Eh

Table 6-42. ADC12_A Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Control 0	ADC12CTL0	00h
Control 1	ADC12CTL1	02h
Control 2	ADC12CTL2	04h
Interrupt flag	ADC12IFG	0Ah
Interrupt enable	ADC12IE	0Ch
Interrupt vector word	ADC12IV	0Eh
ADC memory control 0	ADC12MCTL0	10h
ADC memory control 1	ADC12MCTL1	11h
ADC memory control 2	ADC12MCTL2	12h
ADC memory control 3	ADC12MCTL3	13h
ADC memory control 4	ADC12MCTL4	14h
ADC memory control 5	ADC12MCTL5	15h
ADC memory control 6	ADC12MCTL6	16h
ADC memory control 7	ADC12MCTL7	17h
ADC memory control 8	ADC12MCTL8	18h
ADC memory control 9	ADC12MCTL9	19h
ADC memory control 10	ADC12MCTL10	1Ah
ADC memory control 11	ADC12MCTL11	1Bh
ADC memory control 12	ADC12MCTL12	1Ch
ADC memory control 13	ADC12MCTL13	1Dh
ADC memory control 14	ADC12MCTL14	1Eh
ADC memory control 15	ADC12MCTL15	1Fh
Conversion memory 0	ADC12MEM0	20h
Conversion memory 1	ADC12MEM1	22h
Conversion memory 2	ADC12MEM2	24h
Conversion memory 3	ADC12MEM3	26h
Conversion memory 4	ADC12MEM4	28h
Conversion memory 5	ADC12MEM5	2Ah
Conversion memory 6	ADC12MEM6	2Ch
Conversion memory 7	ADC12MEM7	2Eh
Conversion memory 8	ADC12MEM8	30h
Conversion memory 9	ADC12MEM9	32h
Conversion memory 10	ADC12MEM10	34h
Conversion memory 11	ADC12MEM11	36h
Conversion memory 12	ADC12MEM12	38h
Conversion memory 13	ADC12MEM13	3Ah
Conversion memory 14	ADC12MEM14	3Ch
Conversion memory 15	ADC12MEM15	3Eh

Table 6-43. Comparator_B Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comp_B control 0	CBCTL0	00h
Comp_B control 1	CBCTL1	02h
Comp_B control 2	CBCTL2	04h
Comp_B control 3	CBCTL3	06h
Comp_B interrupt	CBINT	0Ch
Comp_B interrupt vector word	CBIV	0Eh

Table 6-44. USB Configuration Registers (Base Address: 0900h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USB key and ID	USBKEYID	00h
USB module configuration	USBCNF	02h
USB PHY control	USBPHYCTL	04h
USB power control	USBPWRCTL	08h
USB PLL control	USBPLLCTL	10h
USB PLL divider	USBPLLDIV	12h
USB PLL interrupts	USBPLLIR	14h

Table 6-45. USB Control Registers (Base Address: 0920h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Input endpoint_0 configuration	USBIEPCNF_0	00h
Input endpoint_0 byte count	USBIEPCNT_0	01h
Output endpoint_0 configuration	USBOEPCNF_0	02h
Output endpoint_0 byte count	USBOEPCNT_0	03h
Input endpoint interrupt enables	USBIEPIE	0Eh
Output endpoint interrupt enables	USBOEPIE	0Fh
Input endpoint interrupt flags	USBIEPIFG	10h
Output endpoint interrupt flags	USBOEPIFG	11h
USB interrupt vector	USBIV	12h
USB maintenance	USBMAINT	16h
Timestamp	USBTSREG	18h
USB frame number	USBFN	1Ah
USB control	USBCTL	1Ch
USB interrupt enables	USBIE	1Dh
USB interrupt flags	USBIFG	1Eh
Function address	USBFUNADR	1Fh

6.10 Input/Output Diagrams

6.10.1 Port P1 (P1.0 to P1.7) Input/Output With Schmitt Trigger

Figure 6-2 shows the port diagram. Table 6-46 summarizes the selection of the pin function.

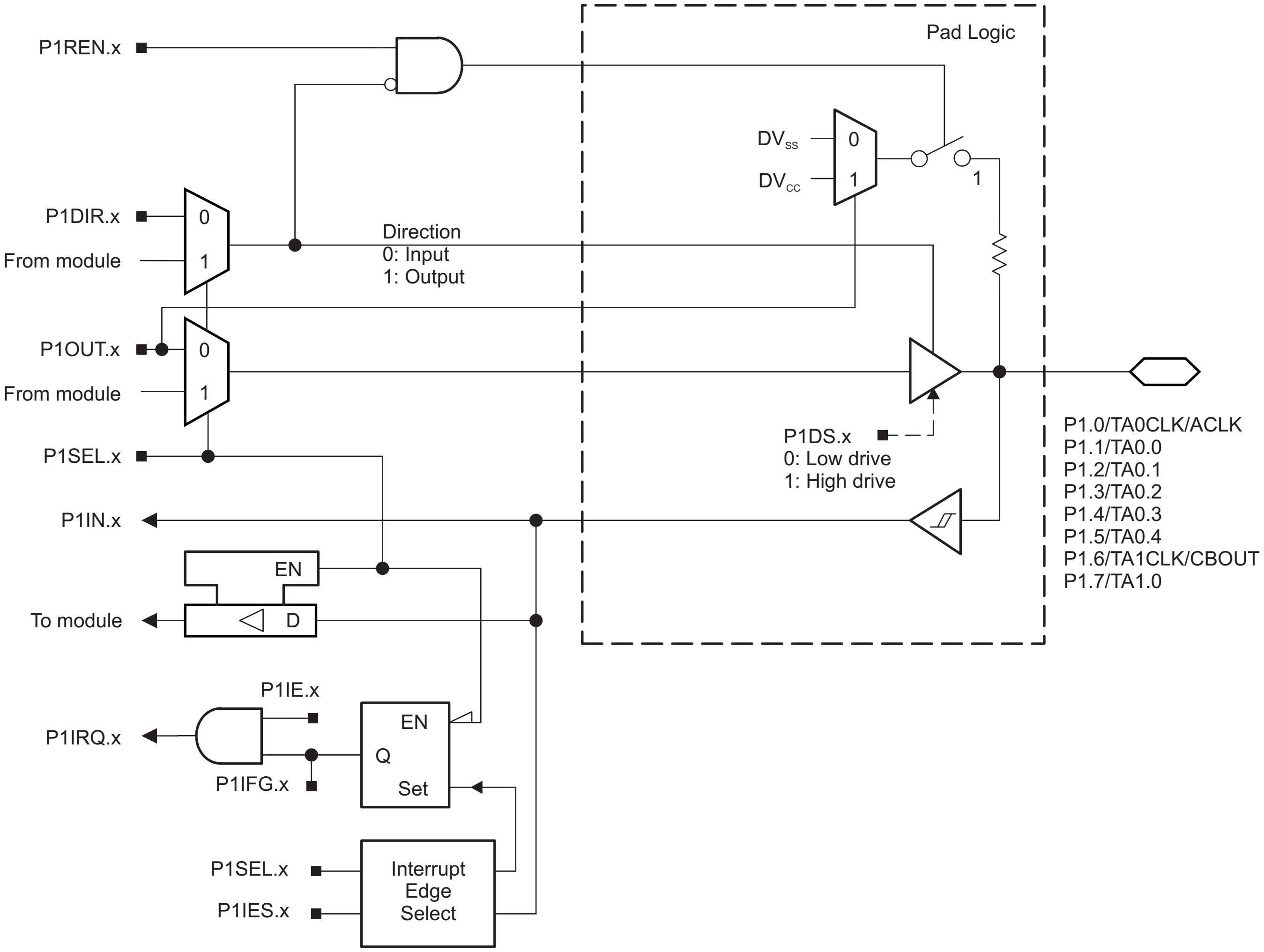

Pad Logic
P1REN.x
DV_SS
DV_CC
0
1
1
P1DIR.x
From module
0
1
Direction
0: Input
1: Output
P1OUT.x
From module
0
1
P1DS.x
0: Low drive
1: High drive
P1SEL.x
P1IN.x
P1.0/TA0CLK/ACLK
P1.1/TA0.0
P1.2/TA0.1
P1.3/TA0.2
P1.4/TA0.3
P1.5/TA0.4
P1.6/TA1CLK/CBOUT
P1.7/TA1.0
EN
To module
D
P1IE.x
P1IRQ.x
EN
Q
Set
P1IFG.x
P1SEL.x
P1IES.x
Interrupt
Edge
Select

Figure 6-2. Port P1 (P1.0 to P1.7) Diagram

Table 6-46. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0CLK/ACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		TA0CLK	0	1
		ACLK	1	1
P1.1/TA0.0	1	P1.1 (I/O)	I: 0; O: 1	0
		TA0.CCI0A	0	1
		TA0.0	1	1
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0
		TA0.CCI1A	0	1
		TA0.1	1	1
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0
		TA0.CCI2A	0	1
		TA0.2	1	1
P1.4/TA0.3	4	P1.4 (I/O)	I: 0; O: 1	0
		TA0.CCI3A	0	1
		TA0.3	1	1
P1.5/TA0.4	5	P1.5 (I/O)	I: 0; O: 1	0
		TA0.CCI4A	0	1
		TA0.4	1	1
P1.6/TA1CLK/CBOUT	6	P1.6 (I/O)	I: 0; O: 1	0
		TA1CLK	0	1
		CBOUT comparator B	1	1
P1.7/TA1.0	7	P1.7 (I/O)	I: 0; O: 1	0
		TA1.CCI0A	0	1
		TA1.0	1	1

6.10.2 Port P2 (P2.0 to P2.7) Input/Output With Schmitt Trigger

Figure 6-3 shows the port diagram. Table 6-47 summarizes the selection of the pin function.

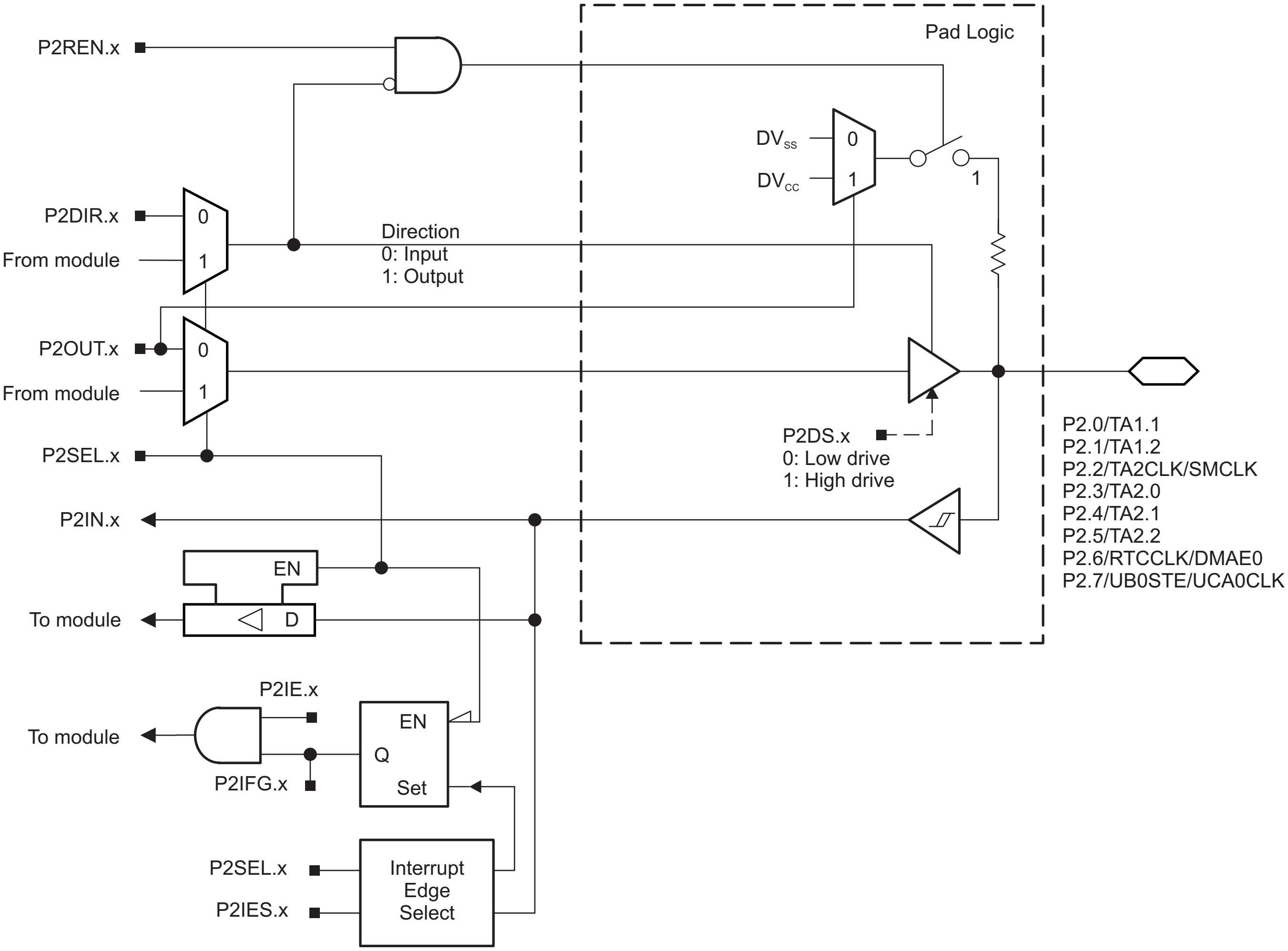

P2REN.x
Pad Logic
DV$_{SS}$
DV$_{CC}$
0
1
1
P2DIR.x
From module
0
1
Direction
0: Input
1: Output
P2OUT.x
From module
0
1
P2DS.x
0: Low drive
1: High drive
P2SEL.x
P2IN.x
P2.0/TA1.1
P2.1/TA1.2
P2.2/TA2CLK/SMCLK
P2.3/TA2.0
P2.4/TA2.1
P2.5/TA2.2
P2.6/RTCCLK/DMAE0
P2.7/UB0STE/UCA0CLK
EN
To module
D
P2IE.x
EN
To module
Q
P2IFG.x
Set
P2SEL.x
P2IES.x
Interrupt
Edge
Select

Figure 6-3. Port P2 (P2.0 to P2.7) Diagram

Table 6-47. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]	
			P2DIR.x	P2SEL.x
P2.0/TA1.1	0	P2.0 (I/O)	I: 0; O: 1	0
		TA1.CCI1A	0	1
		TA1.1	1	1
P2.1/TA1.2	1	P2.1 (I/O)	I: 0; O: 1	0
		TA1.CCI2A	0	1
		TA1.2	1	1
P2.2/TA2CLK/SMCLK	2	P2.2 (I/O)	I: 0; O: 1	0
		TA2CLK	0	1
		SMCLK	1	1
P2.3/TA2.0	3	P2.3 (I/O)	I: 0; O: 1	0
		TA2.CCI0A	0	1
		TA2.0	1	1
P2.4/TA2.1	4	P2.4 (I/O)	I: 0; O: 1	0
		TA2.CCI1A	0	1
		TA2.1	1	1
P2.5/TA2.2	5	P2.5 (I/O)	I: 0; O: 1	0
		TA2.CCI2A	0	1
		TA2.2	1	1
P2.6/RTCCLK/DMAE0	6	P2.6 (I/O)	I: 0; O: 1	0
		DMAE0	0	1
		RTCCLK	1	1
P2.7/UCB0STE/UCA0CLK	7	P2.7 (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK[2] [3]	X	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.

6.10.3 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger

Figure 6-4 shows the port diagram. Table 6-48 summarizes the selection of the pin function.

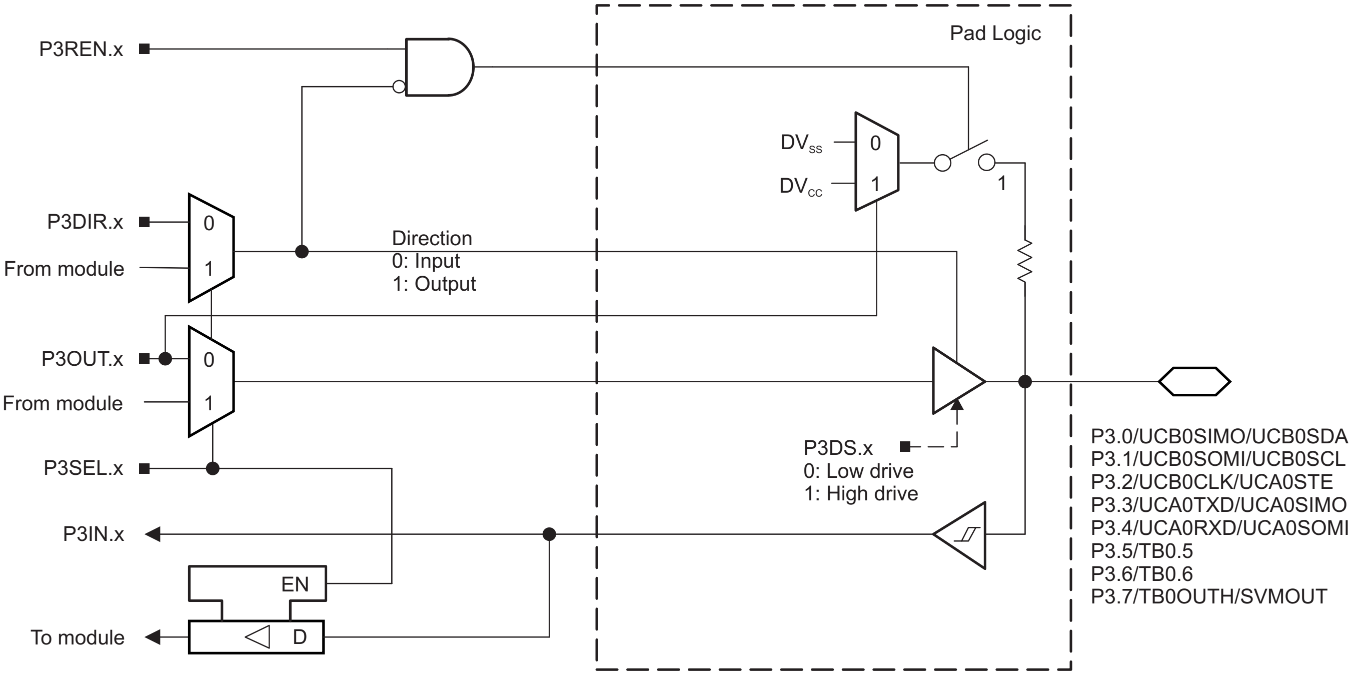

Pad Logic
P3REN.x
DV$_{SS}$
DV$_{CC}$
0
1
1
P3DIR.x
From module
0
1
Direction
0: Input
1: Output
P3OUT.x
From module
0
1
P3DS.x
0: Low drive
1: High drive
P3SEL.x
P3IN.x
EN
D
To module
P3.0/UCB0SIMO/UCB0SDA
P3.1/UCB0SOMI/UCB0SCL
P3.2/UCB0CLK/UCA0STE
P3.3/UCA0TXD/UCA0SIMO
P3.4/UCA0RXD/UCA0SOMI
P3.5/TB0.5
P3.6/TB0.6
P3.7/TB0OUTH/SVMOUT

Figure 6-4. Port P3 (P3.0 to P3.7) Diagram

Table 6-48. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)	
			P3DIR.x	P3SEL.x
P3.0/UCB0SIMO/UCB0SDA	0	P3.0 (I/O)	I: 0; O: 1	0
		UCB0SIMO/UCB0SDA(2) (3)	X	1
P3.1/UCB0SOMI/UCB0SCL	1	P3.1 (I/O)	I: 0; O: 1	0
		UCB0SOMI/UCB0SCL(2) (3)	X	1
P3.2/UCB0CLK/UCA0STE	2	P3.2 (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE(2) (4)	X	1
P3.3/UCA0TXD/UCA0SIMO	3	P3.3 (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO(2)	X	1
P3.4/UCA0RXD/UCA0SOMI	4	P3.4 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI(2)	X	1
P3.5/TB0.5(5)	5	P3.5 (I/O)	I: 0; O: 1	0
		TB0.CCI5A	0	1
		TB0.5	1	1
P3.6/TB0.6(5)	6	P3.6 (I/O)	I: 0; O: 1	0
		TB0.CCI6A	0	1
		TB0.6	1	1
P3.7/TB0OUTH/SVMOUT(5)	7	P3.7 (I/O)	I: 0; O: 1	0
		TB0OUTH	0	1
		SVMOUT	1	1

(1) X = Don't care
(2) The pin direction is controlled by the USCI module.
(3) If the I^2C functionality is selected, the output drives only the logical 0 to V_{SS} level.
(4) UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.
(5) F5529, F5527, F5525, F5521, F5519, F5517, F5515 devices only.

6.10.4 Port P4 (P4.0 to P4.7) Input/Output With Schmitt Trigger

Figure 6-5 shows the port diagram. Table 6-49 summarizes the selection of the pin function.

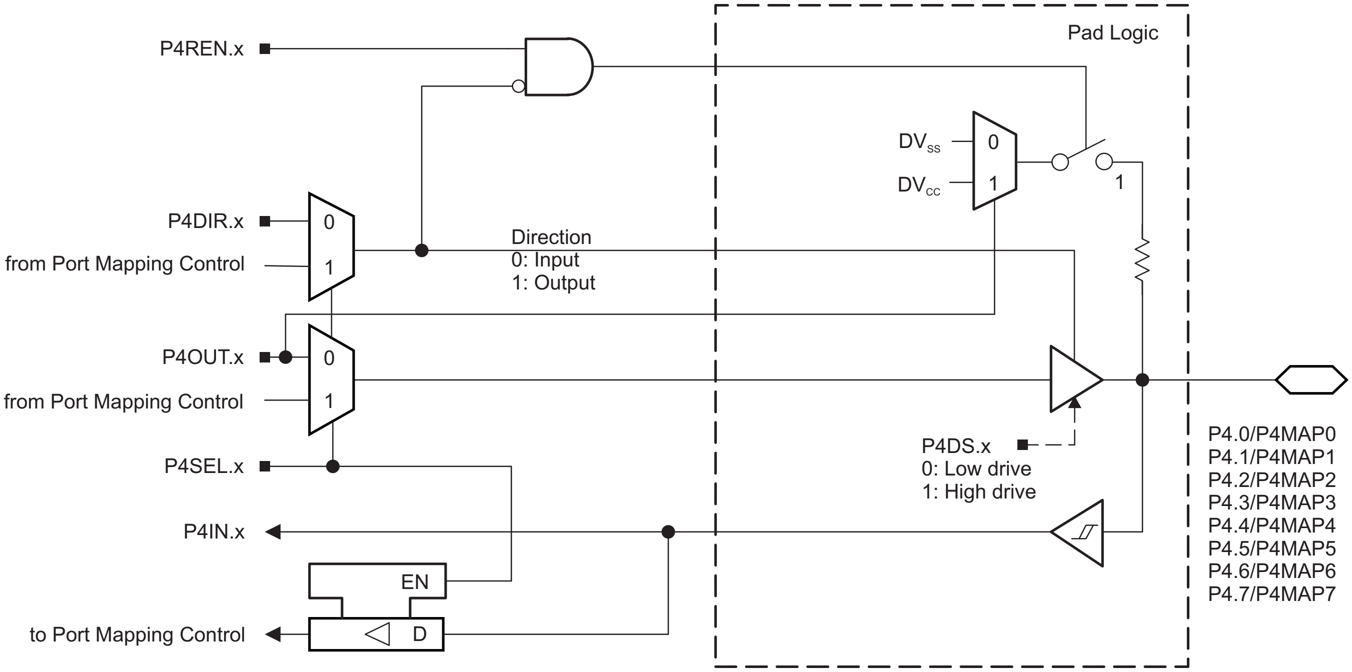

P4REN.x
Pad Logic
DV$_{SS}$
DV$_{CC}$
0
1
1
P4DIR.x
from Port Mapping Control
0
1
Direction
0: Input
1: Output
P4OUT.x
from Port Mapping Control
0
1
P4SEL.x
P4DS.x
0: Low drive
1: High drive
P4IN.x
EN
D
to Port Mapping Control
P4.0/P4MAP0
P4.1/P4MAP1
P4.2/P4MAP2
P4.3/P4MAP3
P4.4/P4MAP4
P4.5/P4MAP5
P4.6/P4MAP6
P4.7/P4MAP7

Figure 6-5. Port P4 (P4.0 to P4.7) Diagram

Table 6-49. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P4DIR.x[1]	P4SEL.x	P4MAPx
P4.0/P4MAP0	0	P4.0 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.1/P4MAP1	1	P4.1 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.2/P4MAP2	2	P4.2 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.3/P4MAP3	3	P4.3 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.4/P4MAP4	4	P4.4 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.5/P4MAP5	5	P4.5 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.6/P4MAP6	6	P4.6 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30
P4.7/P4MAP7	7	P4.7 (I/O)	I: 0; O: 1	0	X
		Mapped secondary digital function	X	1	≤ 30

(1) The direction of some mapped secondary functions are controlled directly by the module. See Table 6-7 for specific direction control information of mapped secondary functions.

6.10.5 Port P5 (P5.0 and P5.1) Input/Output With Schmitt Trigger

Figure 6-6 shows the port diagram. Table 6-50 summarizes the selection of the pin function.

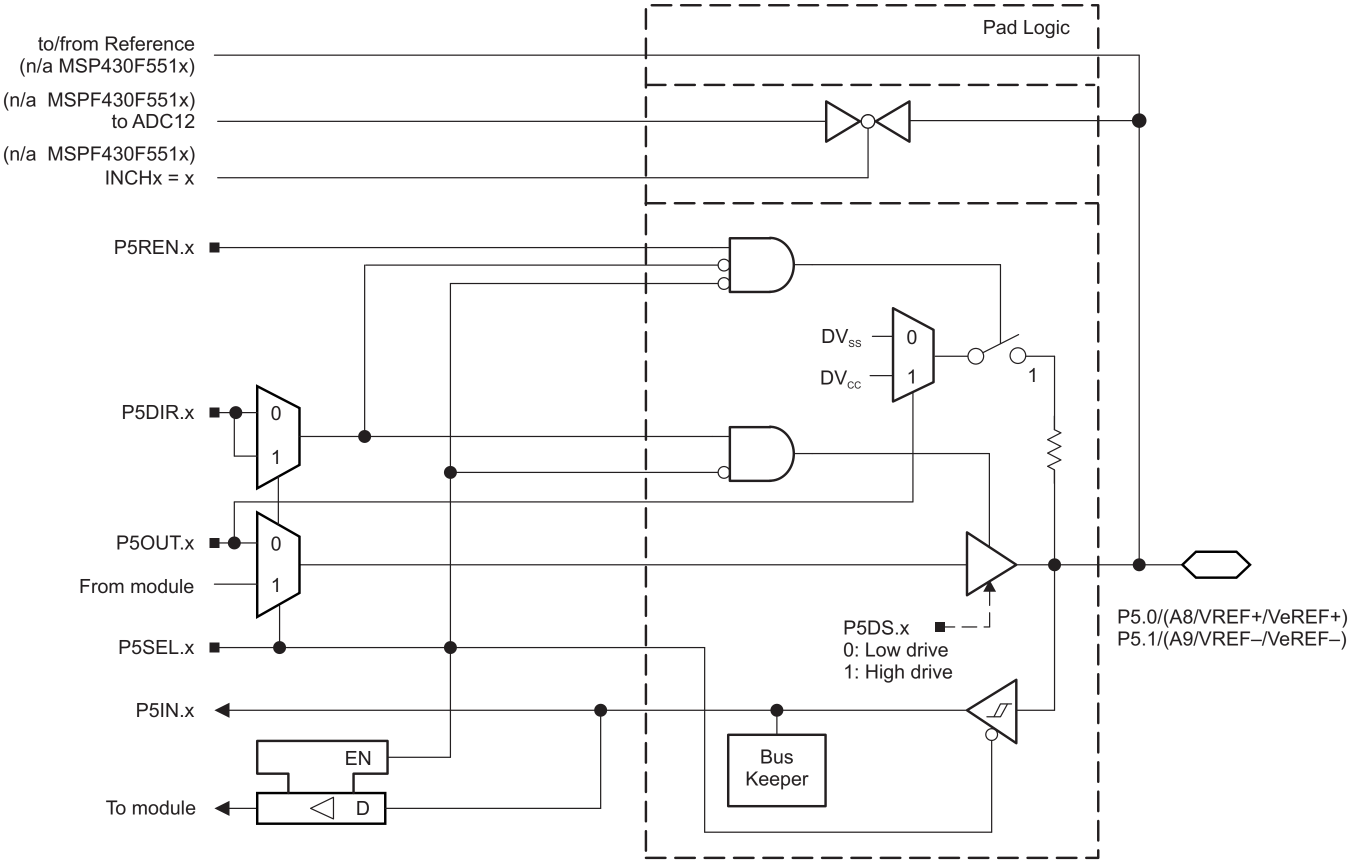

Pad Logic
to/from Reference
(n/a MSP430F551x)
(n/a MSPF430F551x)
to ADC12
(n/a MSPF430F551x)
INCHx = x
P5REN.x
DVSS
DVCC
0
1
1
P5DIR.x
0
1
P5OUT.x
0
From module
1
P5SEL.x
P5DS.x
0: Low drive
1: High drive
P5.0/(A8/VREF+/VeREF+)
P5.1/(A9/VREF–/VeREF–)
P5IN.x
EN
Bus
Keeper
To module
D

Figure 6-6. Port P5 (P5.0 and P5.1) Diagram

Table 6-50. Port P5 (P5.0 and P5.1) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)		
			P5DIR.x	P5SEL.x	REFOUT
P5.0/A8/VREF+/VeREF+(2)	0	P5.0 (I/O)(3)	I: 0; O: 1	0	X
		A8/VeREF+(4)	X	1	0
		A8/VREF+(5)	X	1	1
P5.1/A9/VREF-/VeREF-(6)	1	P5.1 (I/O)(3)	I: 0; O: 1	0	X
		A9/VeREF–(7)	X	1	0
		A9/VREF–(8)	X	1	1

(1) X = Don't care
(2) VREF+/VeREF+ available on MSP430F552x devices only.
(3) Default condition
(4) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC12_A when available. Channel A8, when selected with the INCHx bits, is connected to the VREF+/VeREF+ pin.
(5) Setting the P5SEL.0 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The VREF+ reference is available at the pin. Channel A8, when selected with the INCHx bits, is connected to the VREF+/VeREF+ pin.
(6) VREF-/VeREF- available on MSP430F552x devices only.
(7) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC12_A when available. Channel A9, when selected with the INCHx bits, is connected to the VREF-/VeREF- pin.
(8) Setting the P5SEL.1 bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The VREF– reference is available at the pin. Channel A9, when selected with the INCHx bits, is connected to the VREF-/VeREF- pin.

6.10.6 Port P5 (P5.2 and P5.3) Input/Output With Schmitt Trigger

Figure 6-7 and Figure 6-8 show the port diagrams. Table 6-51 summarizes the selection of the pin function.

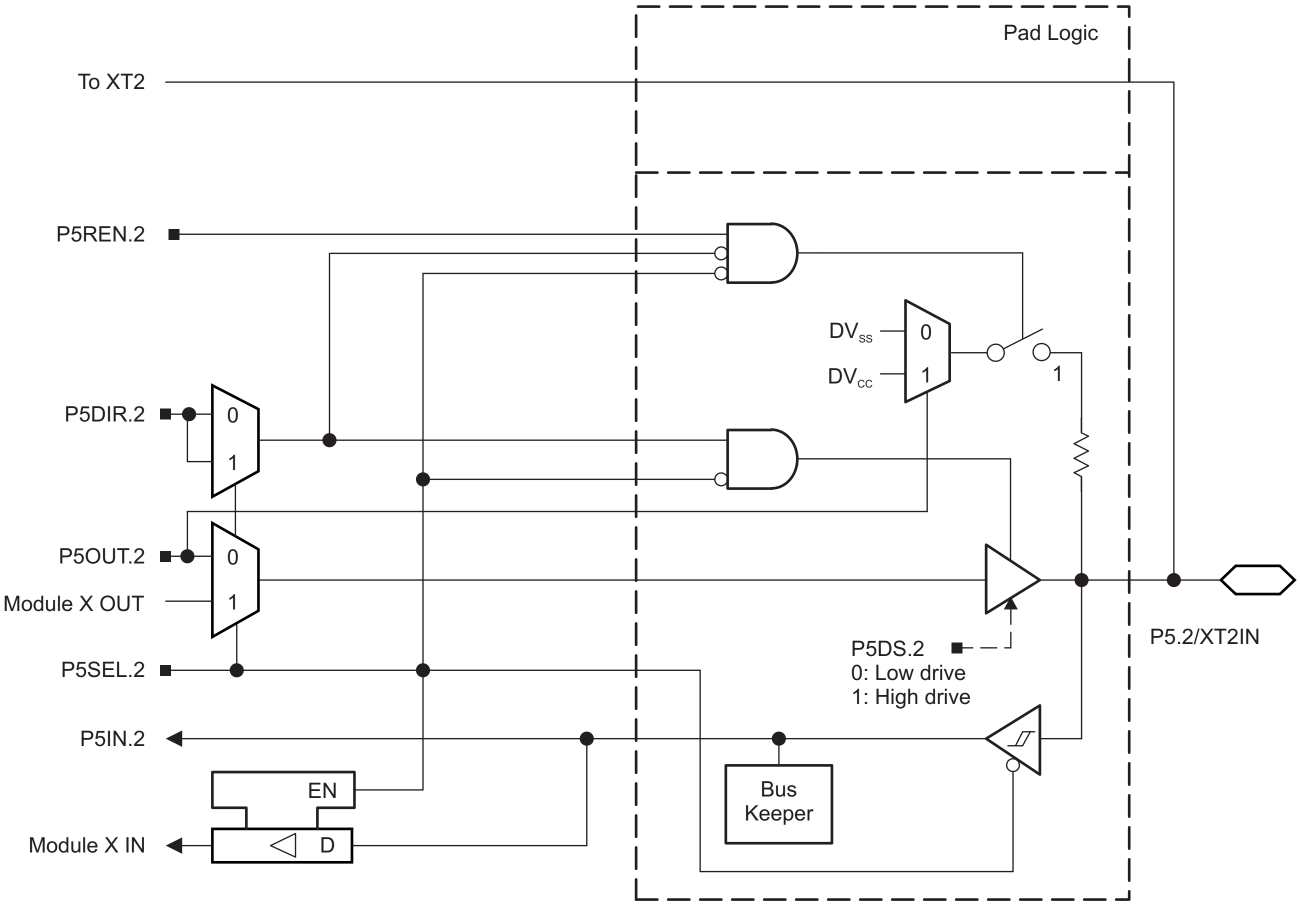

Pad Logic
To XT2
P5REN.2
DVSS
DVCC
0
1
1
P5DIR.2
0
1
P5OUT.2
0
Module X OUT
1
P5SEL.2
P5IN.2
EN
Module X IN
D
P5DS.2
0: Low drive
1: High drive
Bus Keeper
P5.2/XT2IN

Figure 6-7. Port P5 (P5.2) Diagram

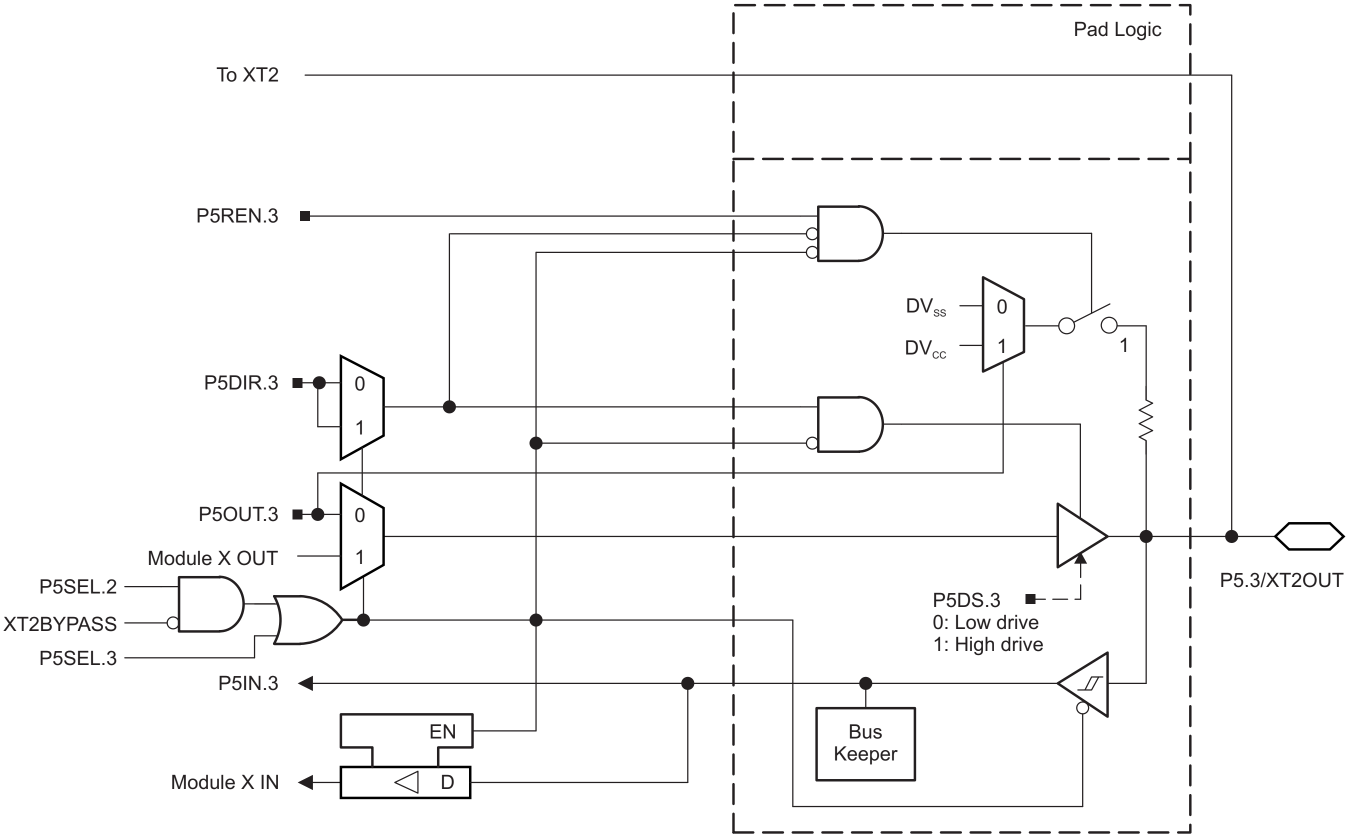

Pad Logic
To XT2
P5REN.3
DVSS
DVCC
0
1
1
P5DIR.3
0
1
P5OUT.3
0
1
Module X OUT
P5SEL.2
XT2BYPASS
P5SEL.3
P5.3/XT2OUT
P5DS.3
0: Low drive
1: High drive
P5IN.3
EN
D
Module X IN
Bus Keeper

Figure 6-8. Port P5 (P5.3) Diagram

Table 6-51. Port P5 (P5.2 and P5.3) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]			
			P5DIR.x	P5SEL.2	P5SEL.3	XT2BYPASS
P5.2/XT2IN	2	P5.2 (I/O)	I: 0; O: 1	0	X	X
		XT2IN crystal mode[2]	X	1	X	0
		XT2IN bypass mode[2]	X	1	X	1
P5.3/XT2OUT	3	P5.3 (I/O)	I: 0; O: 1	0	0	X
		XT2OUT crystal mode[3]	X	1	X	0
		P5.3 (I/O)[3]	X	1	0	1

(1) X = Don't care
(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.

6.10.7 Port P5 (P5.4 and P5.5) Input/Output With Schmitt Trigger

Figure 6-9 and Figure 6-10 show the port diagrams. Table 6-52 summarizes the selection of the pin function.

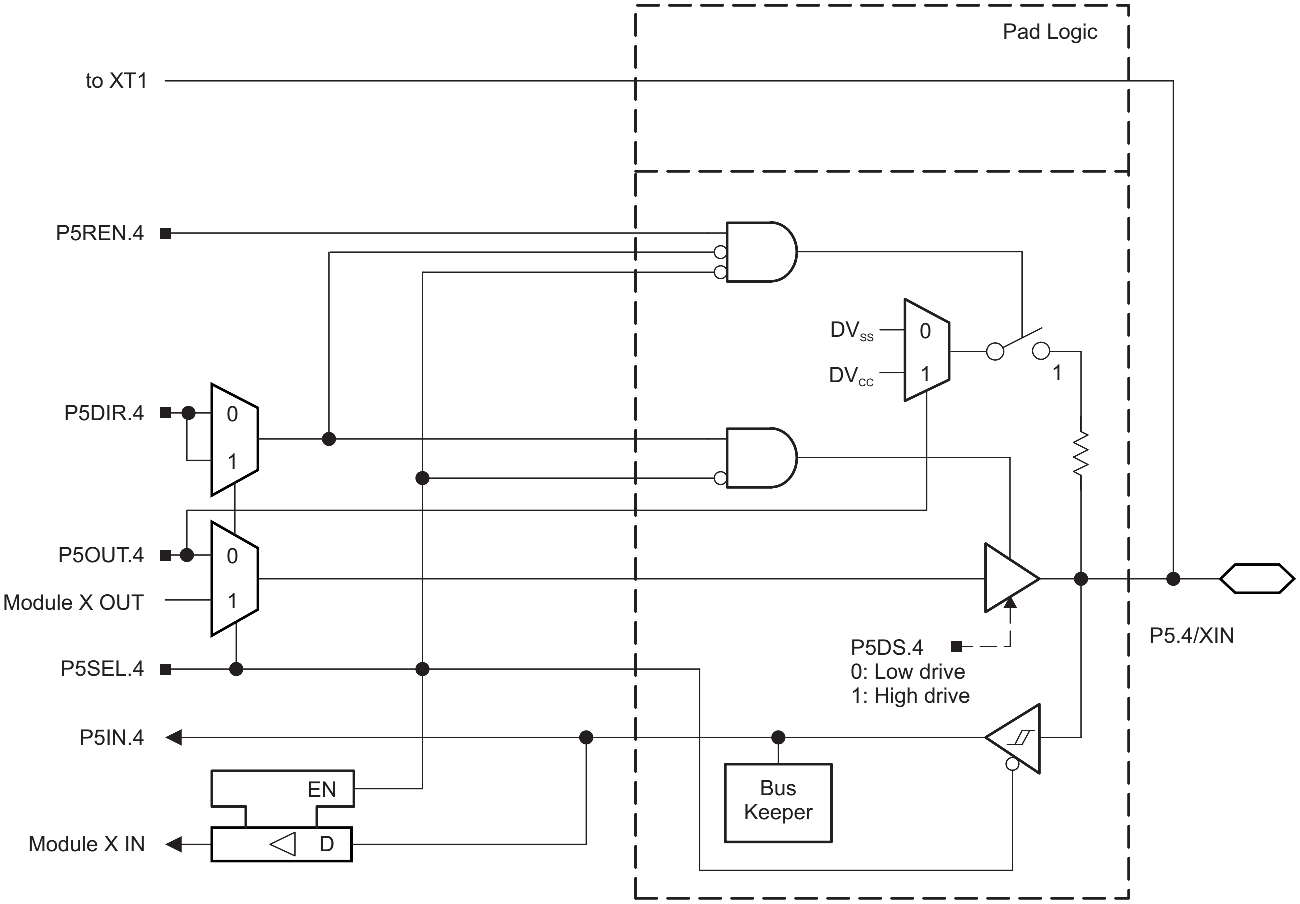

Pad Logic
to XT1
P5REN.4
DVSS
DVCC
0
1
P5DIR.4
0
1
P5OUT.4
0
1
Module X OUT
P5SEL.4
P5IN.4
EN
D
Module X IN
Bus Keeper
P5DS.4
0: Low drive
1: High drive
P5.4/XIN

Figure 6-9. Port P5 (P5.4) Diagram

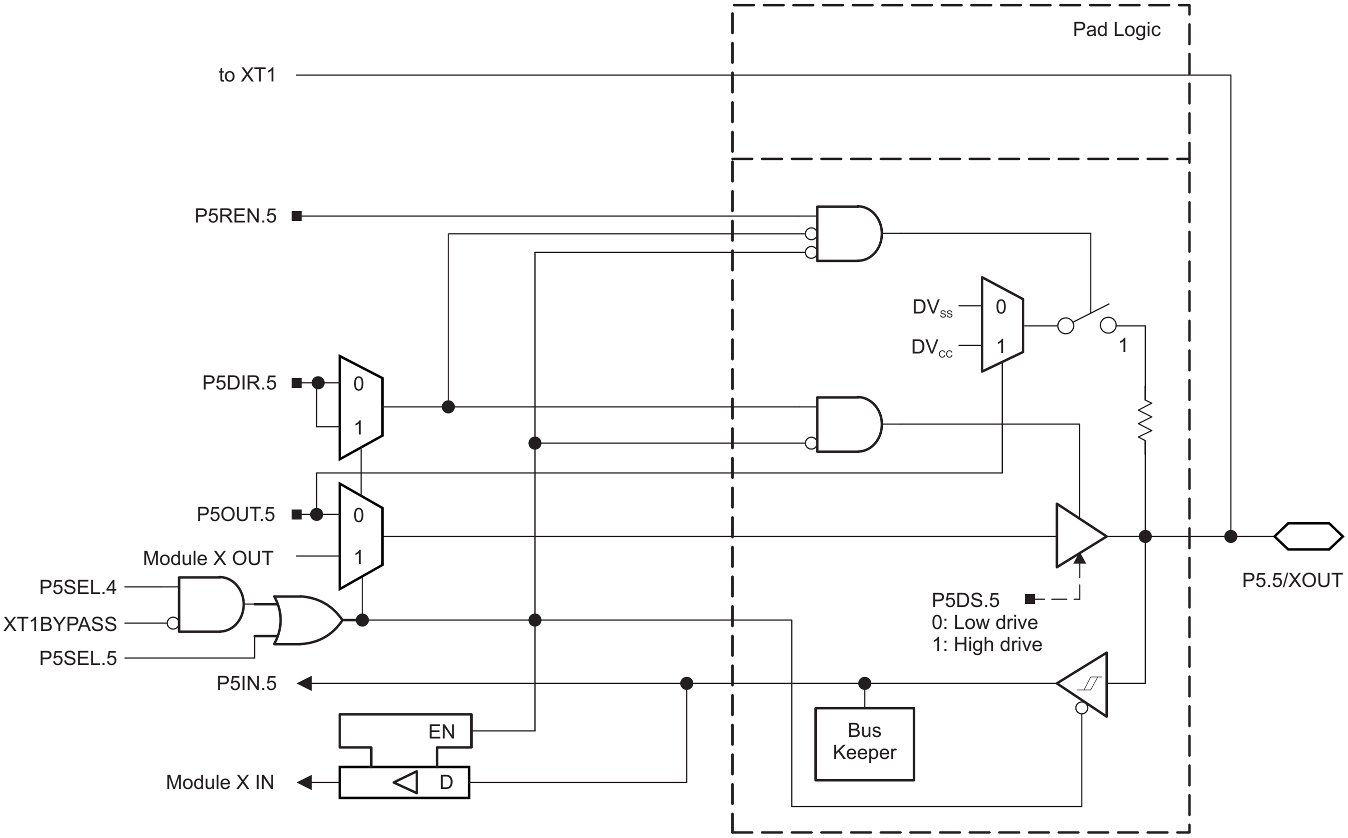

Pad Logic
to XT1
P5REN.5
DV_{SS}
DV_{CC}
0
1
1
P5DIR.5
0
1
P5OUT.5
0
1
Module X OUT
P5SEL.4
XT1BYPASS
P5SEL.5
P5.5/XOUT
P5DS.5
0: Low drive
1: High drive
P5IN.5
EN
D
Module X IN
Bus Keeper

Figure 6-10. Port P5 (P5.5) Diagram

Table 6-52. Port P5 (P5.4 and P5.5) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS(1)			
			P5DIR.x	P5SEL.4	P5SEL.5	XT1BYPASS
P5.4/XIN	4	P5.4 (I/O)	I: 0; O: 1	0	X	X
		XIN crystal mode(2)	X	1	X	0
		XIN bypass mode(2)	X	1	X	1
P5.5/XOUT	5	P5.5 (I/O)	I: 0; O: 1	0	0	X
		XOUT crystal mode(3)	X	1	X	0
		P5.5 (I/O)(3)	X	1	0	1

(1) X = Don't care
(2) Setting P5SEL.4 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P5.4 is configured for crystal mode or bypass mode.
(3) Setting P5SEL.4 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.5 can be used as general-purpose I/O.

6.10.8 Port P5 (P5.6 and P5.7) Input/Output With Schmitt Trigger

Figure 6-11 shows the port diagram. Table 6-53 summarizes the selection of the pin function.

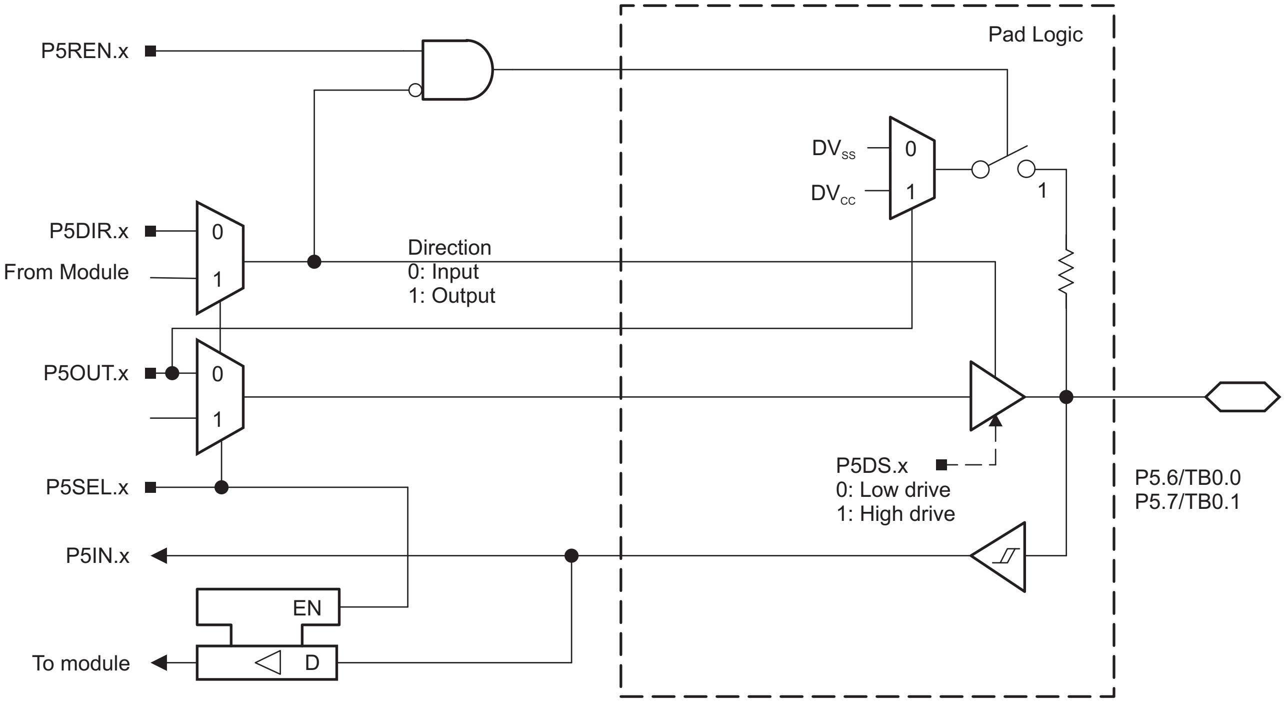

P5REN.x
Pad Logic
DV$_{SS}$
DV$_{CC}$
0
1
1
P5DIR.x
From Module
0
1
Direction
0: Input
1: Output
P5OUT.x
0
1
P5DS.x
0: Low drive
1: High drive
P5SEL.x
P5.6/TB0.0
P5.7/TB0.1
P5IN.x
EN
To module
D

Figure 6-11. Port P5 (P5.6 and P5.7) Diagram

Table 6-53. Port P5 (P5.6 and P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P5DIR.x	P5SEL.x
P5.6/TB0.0[1]	6	P5.6 (I/O)	I: 0; O: 1	0
		TB0.CCI0A	0	1
		TB0.0	1	1
P5.7/TB0.1[1]	7	TB0.CCI1A	0	1
		TB0.1	1	1

[1] F5529, F5527, F5525, F5521, F5519, F5517, F5515 devices only.

6.10.9 Port P6 (P6.0 to P6.7) Input/Output With Schmitt Trigger

Figure 6-12 shows the port diagram. Table 6-54 summarizes the selection of the pin function.

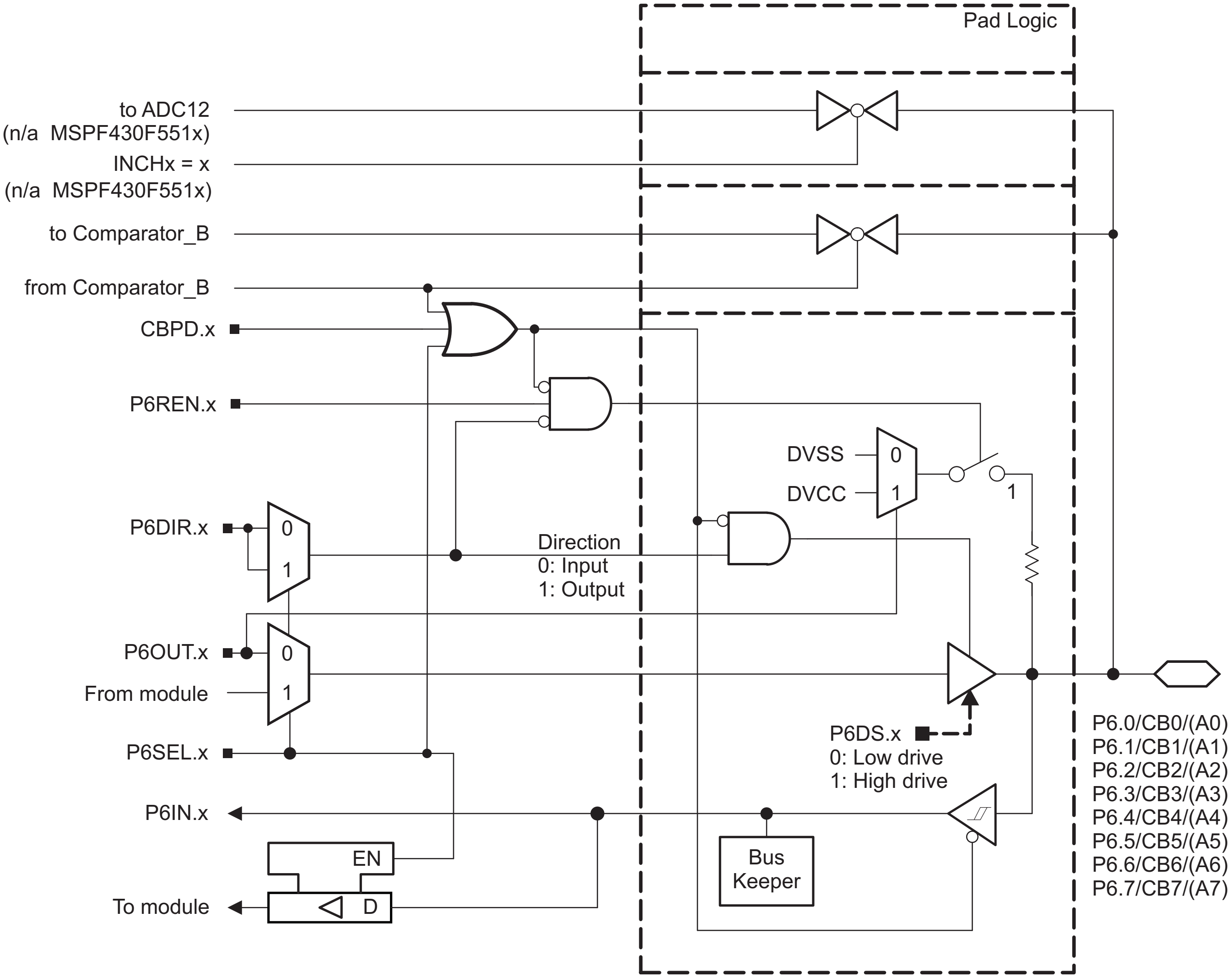

Pad Logic
to ADC12
(n/a MSPF430F551x)
INCHx = x
(n/a MSPF430F551x)
to Comparator_B
from Comparator_B
CBPD.x
P6REN.x
DVSS
DVCC
0
1
1
P6DIR.x
0
1
Direction
0: Input
1: Output
P6OUT.x
0
From module
1
P6SEL.x
P6DS.x
0: Low drive
1: High drive
P6IN.x
EN
To module
D
Bus
Keeper
P6.0/CB0/(A0)
P6.1/CB1/(A1)
P6.2/CB2/(A2)
P6.3/CB3/(A3)
P6.4/CB4/(A4)
P6.5/CB5/(A5)
P6.6/CB6/(A6)
P6.7/CB7/(A7)

Figure 6-12. Port P6 (P6.0 to P6.7) Diagram

Table 6-54. Port P6 (P6.0 to P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P6DIR.x	P6SEL.x	CBPD
P6.0/CB0/(A0)	0	P6.0 (I/O)	I: 0; O: 1	0	0
		A0 (only MSP430F552x)	X	1	X
		CB0[1]	X	X	1
P6.1/CB1/(A1)	1	P6.1 (I/O)	I: 0; O: 1	0	0
		A1 (only MSP430F552x)	X	1	X
		CB1[1]	X	X	1
P6.2/CB2/(A2)	2	P6.2 (I/O)	I: 0; O: 1	0	0
		A2 (only MSP430F552x)	X	1	X
		CB2[1]	X	X	1
P6.3/CB3/(A3)	3	P6.3 (I/O)	I: 0; O: 1	0	0
		A3 (only MSP430F552x)	X	1	X
		CB3[1]	X	X	1
P6.4/CB4/(A4)	4	P6.4 (I/O)	I: 0; O: 1	0	0
		A4 (only MSP430F552x)	X	1	X
		CB4[1]	X	X	1
P6.5/CB5/(A5)	5	P6.5 (I/O)	I: 0; O: 1	0	0
		A5 (only MSP430F552x)	X	1	X
		CB5[1]	X	X	1
P6.6/CB6/(A6)	6	P6.6 (I/O)	I: 0; O: 1	0	0
		A6 (only MSP430F552x)	X	1	X
		CB6[1]	X	X	1
P6.7/CB7/(A7)	7	P6.7 (I/O)	I: 0; O: 1	0	0
		A7 (only MSP430F552x)	X	1	X
		CB7[1]	X	X	1

(1) Setting the CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

6.10.10 Port P7 (P7.0 to P7.3) Input/Output With Schmitt Trigger

Figure 6-13 shows the port diagram. Table 6-55 summarizes the selection of the pin function.

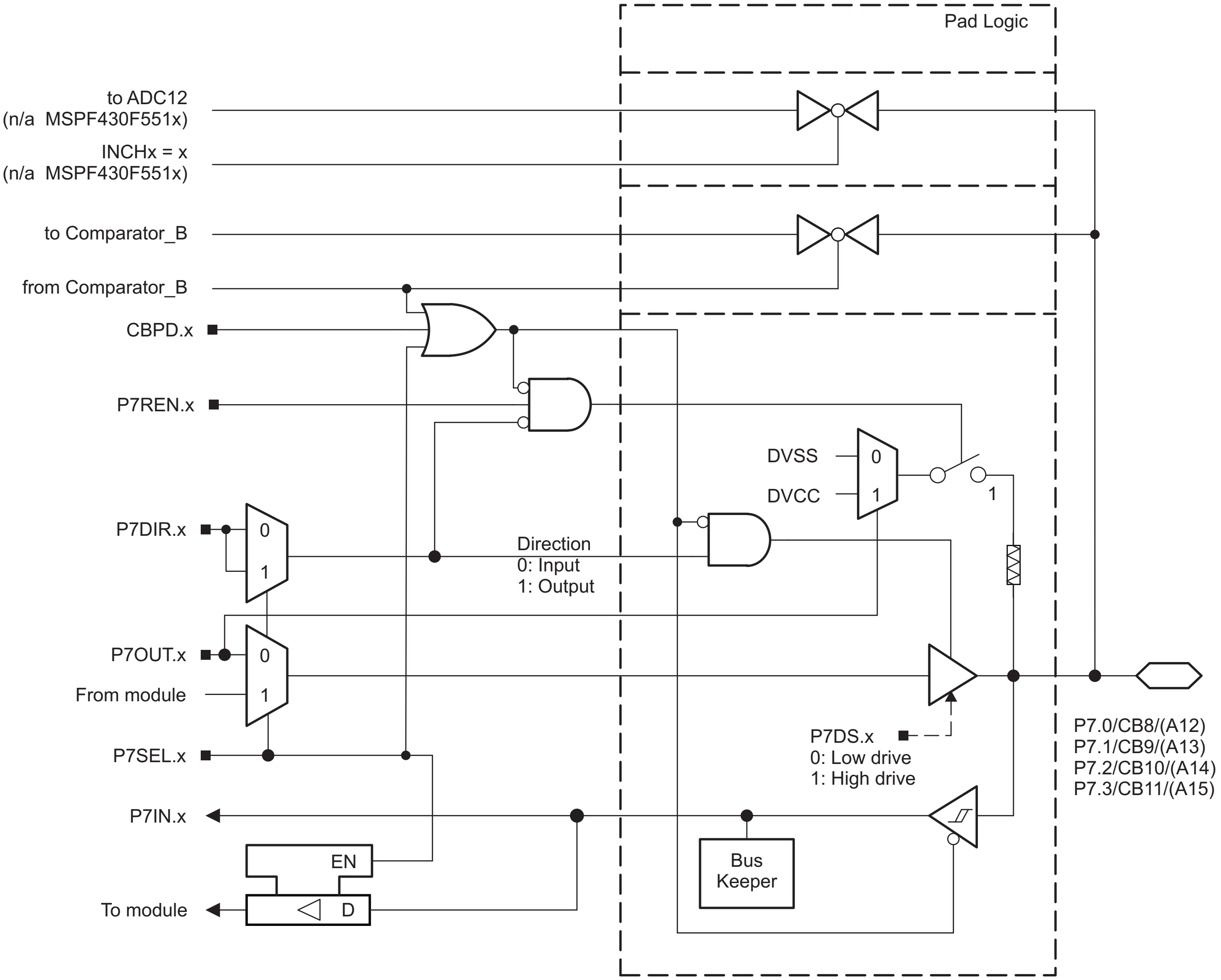

Pad Logic
to ADC12
(n/a MSPF430F551x)
INCHx = x
(n/a MSPF430F551x)
to Comparator_B
from Comparator_B
CBPD.x
P7REN.x
DVSS
DVCC
0
1
1
P7DIR.x
0
1
Direction
0: Input
1: Output
P7OUT.x
0
1
From module
P7DS.x
0: Low drive
1: High drive
P7.0/CB8/(A12)
P7.1/CB9/(A13)
P7.2/CB10/(A14)
P7.3/CB11/(A15)
P7SEL.x
P7IN.x
EN
D
To module
Bus
Keeper

Figure 6-13. Port P7 (P7.0 to P7.3) Diagram

Table 6-55. Port P7 (P7.0 to P7.3) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS		
			P7DIR.x	P7SEL.x	CBPD
P7.0/CB8/(A12)	0	P7.0 (I/O) (1)	I: 0; O: 1	0	0
		A12 (2)	X	1	X
		CB8 (3) (1)	X	X	1
P7.1/CB9/(A13)	1	P7.1 (I/O) (1)	I: 0; O: 1	0	0
		A13 (2)	X	1	X
		CB9 (3) (1)	X	X	1
P7.2/CB10/(A14)	2	P7.2 (I/O) (1)	I: 0; O: 1	0	0
		A14 (2)	X	1	X
		CB10 (3) (1)	X	X	1
P7.3/CB11/(A15)	3	P7.3 (I/O) (1)	I: 0; O: 1	0	0
		A15 (2)	X	1	X
		CB11 (3) (1)	X	X	1

(1) F5529, F5527, F5525, F5521, F5519, F5517, F5515 devices only
(2) F5529, F5527, F5525, F5521 devices only
(3) Setting the CBPD.x bit disables the output driver and the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

6.10.11 Port P7 (P7.4 to P7.7) Input/Output With Schmitt Trigger

Figure 6-14 shows the port diagram. Table 6-56 summarizes the selection of the pin function.

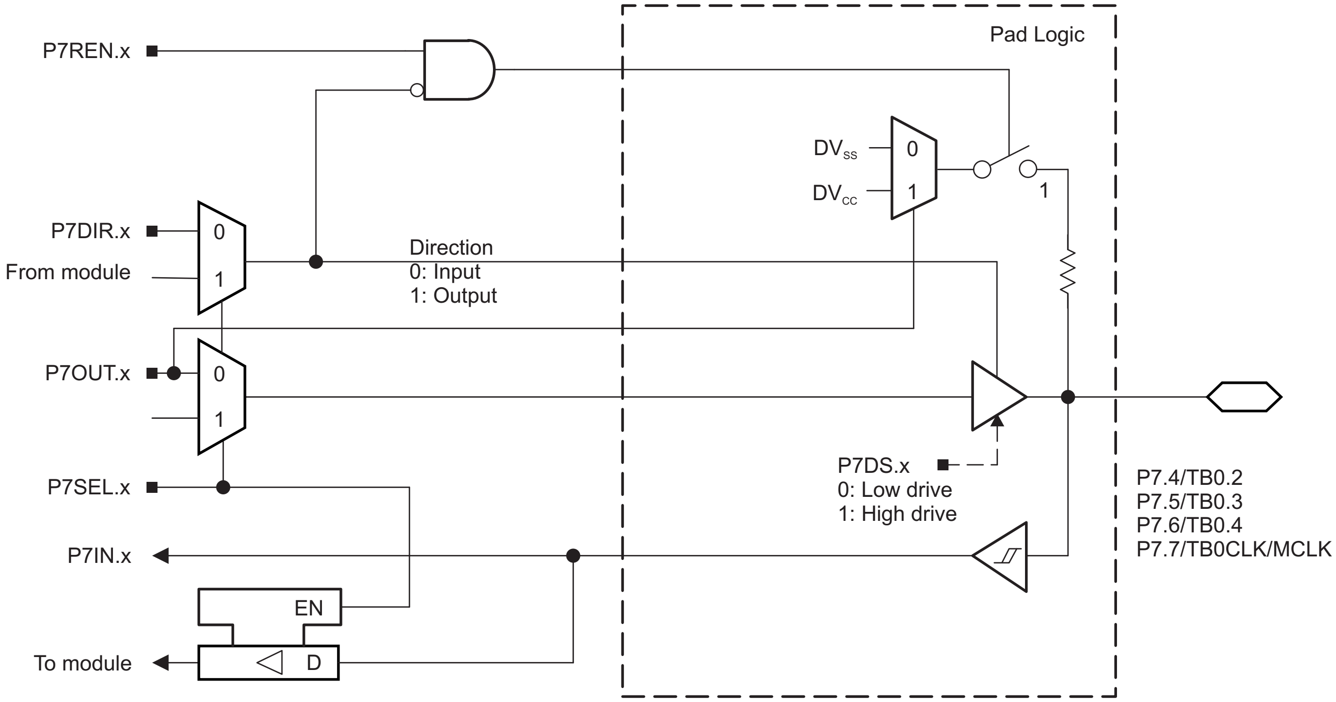

Pad Logic
P7REN.x
DVSS
DVCC
0
1
1
P7DIR.x
From module
0
1
Direction
0: Input
1: Output
P7OUT.x
0
1
P7DS.x
0: Low drive
1: High drive
P7SEL.x
P7IN.x
P7.4/TB0.2
P7.5/TB0.3
P7.6/TB0.4
P7.7/TB0CLK/MCLK
EN
D
To module

Figure 6-14. Port P7 (P7.4 to P7.7) Diagram

Table 6-56. Port P7 (P7.4 to P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P7DIR.x	P7SEL.x
P7.4/TB0.2[1]	4	P7.4 (I/O)	I: 0; O: 1	0
		TB0.CCI2A	0	1
		TB0.2	1	1
P7.5/TB0.3[1]	5	P7.5 (I/O)	I: 0; O: 1	0
		TB0.CCI3A	0	1
		TB0.3	1	1
P7.6/TB0.4[1]	6	P7.6 (I/O)	I: 0; O: 1	0
		TB0.CCI4A	0	1
		TB0.4	1	1
P7.7/TB0CLK/MCLK[1]	7	P7.7 (I/O)	I: 0; O: 1	0
		TB0CLK	0	1
		MCLK	1	1

(1) F5529, F5527, F5525, F5521, F5519, F5517, F5515 devices only

6.10.12 Port P8 (P8.0 to P8.2) Input/Output With Schmitt Trigger

Figure 6-15 shows the port diagram. Table 6-57 summarizes the selection of the pin function.

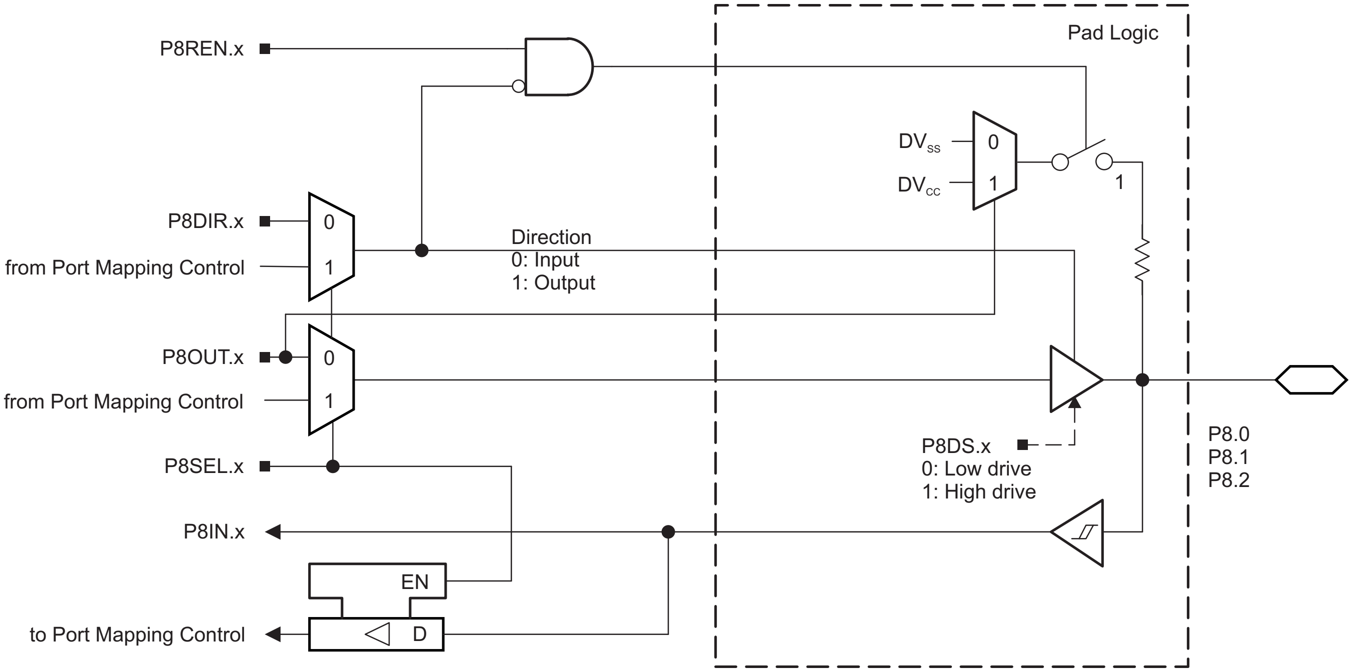

Pad Logic
P8REN.x
DVSS
DVCC
0
1
1
P8DIR.x
0
1
from Port Mapping Control
Direction
0: Input
1: Output
P8OUT.x
0
1
from Port Mapping Control
P8SEL.x
P8DS.x
0: Low drive
1: High drive
P8.0
P8.1
P8.2
P8IN.x
EN
to Port Mapping Control
D

Figure 6-15. Port P8 (P8.0 to P8.2) Diagram

Table 6-57. Port P8 (P8.0 to P8.2) Pin Functions

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS OR SIGNALS	
			P8DIR.x	P8SEL.x
P8.0[1]	0	P8.0(I/O)	I: 0; O: 1	0
P8.1[1]	1	P8.1(I/O)	I: 0; O: 1	0
P8.2[1]	2	P8.2(I/O)	I: 0; O: 1	0

[1] F5529, F5527, F5525, F5521, F5519, F5517, F5515 devices only

6.10.13 Port PU (PU.0/DP, PU.1/DM, PUR) USB Ports

Figure 6-16 shows the port diagram. Table 6-58 through Table 6-60 summarize the pin function selection.

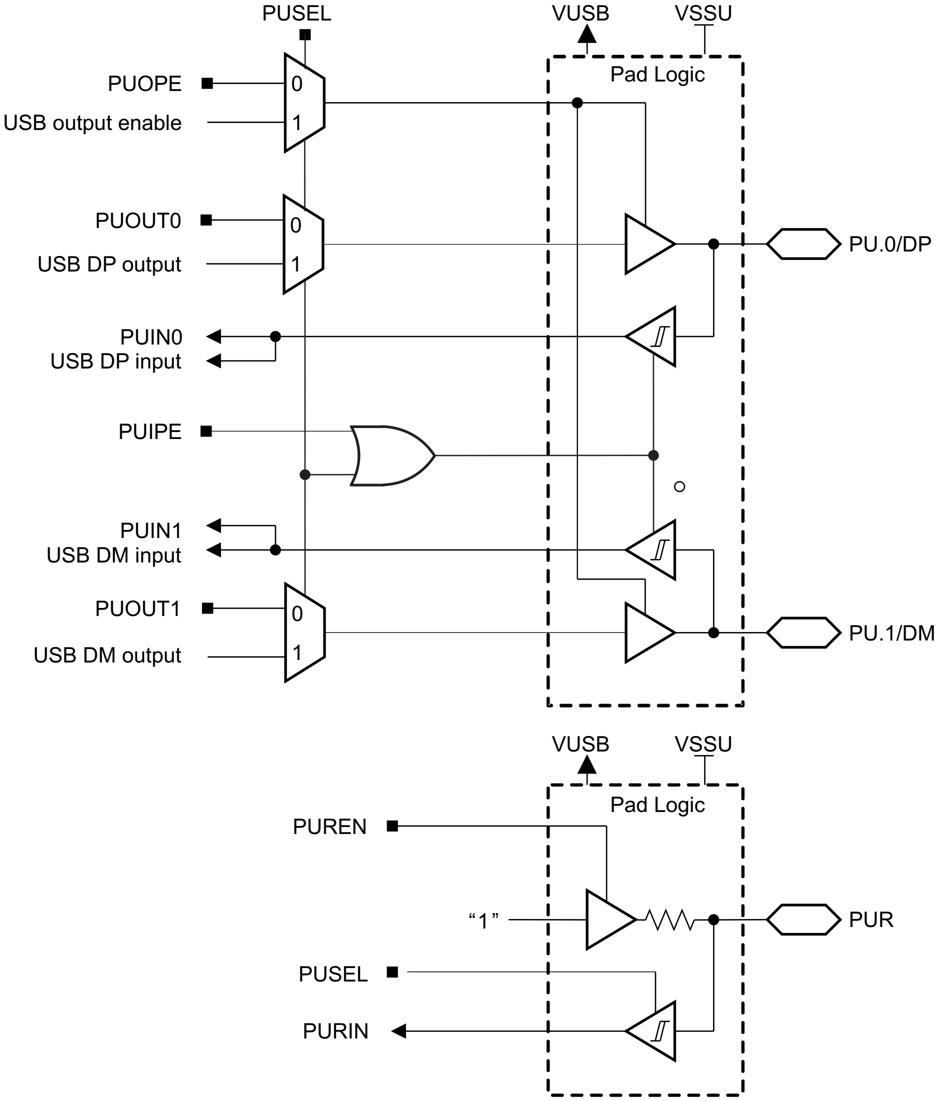

PUSEL
VUSB
VSSU
Pad Logic
PUOPE
USB output enable
0
1
PUOUT0
USB DP output
0
1
PU.0/DP
PUIN0
USB DP input
PUIPE
PUIN1
USB DM input
PUOUT1
USB DM output
0
1
PU.1/DM
VUSB
VSSU
Pad Logic
PUREN
"1"
PUR
PUSEL
PURIN

Figure 6-16. Port PU (PU.0/DP, PU.1/DM) Diagram

Table 6-58. Port PU (PU.0/DP, PU.1/DM) Output Functions(1)

CONTROL BITS				PIN NAME	
PUSEL	PUOPE	PUOUT1	PUOUT0	PU.1/DM	PU.0/DP
0	0	X	X	Output disabled	Output disabled
0	1	0	0	Output low	Output low
0	1	0	1	Output low	Output high
0	1	1	0	Output high	Output low
0	1	1	1	Output high	Output high
1	X	X	X	DM(2)	DP(2)

(1) PU.1/DM and PU.0/DP inputs and outputs are supplied from VUSB. VUSB can be generated by the device using the integrated 3.3-V LDO when enabled. VUSB can also be supplied externally when the 3.3-V LDO is not being used and is disabled.
(2) Output state set by the USB module.

Table 6-59. Port PU (PU.0/DP, PU.1/DM) Input Functions(1)

CONTROL BITS		PIN NAME	
PUSEL	PUIPE	PU.1/DM	PU.0/DP
0	0	Input disabled	Input disabled
0	1	Input enabled	Input enabled
1	X	DM input	DP input

(1) PU.1/DM and PU.0/DP inputs and outputs are supplied from VUSB. VUSB can be generated by the device using the integrated 3.3-V LDO when enabled. VUSB can also be supplied externally when the 3.3-V LDO is not being used and is disabled.

Table 6-60. Port PUR Input Functions

CONTROL BITS		FUNCTION
PUSEL	PUREN	
0	0	Input disabled Pullup disabled
0	1	Input disabled Pullup enabled
1	0	Input enabled Pullup disabled
1	1	Input enabled Pullup enabled

6.10.14 Port PJ (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

Figure 6-17 shows the port diagram. Table 6-61 summarizes the selection of the pin function.

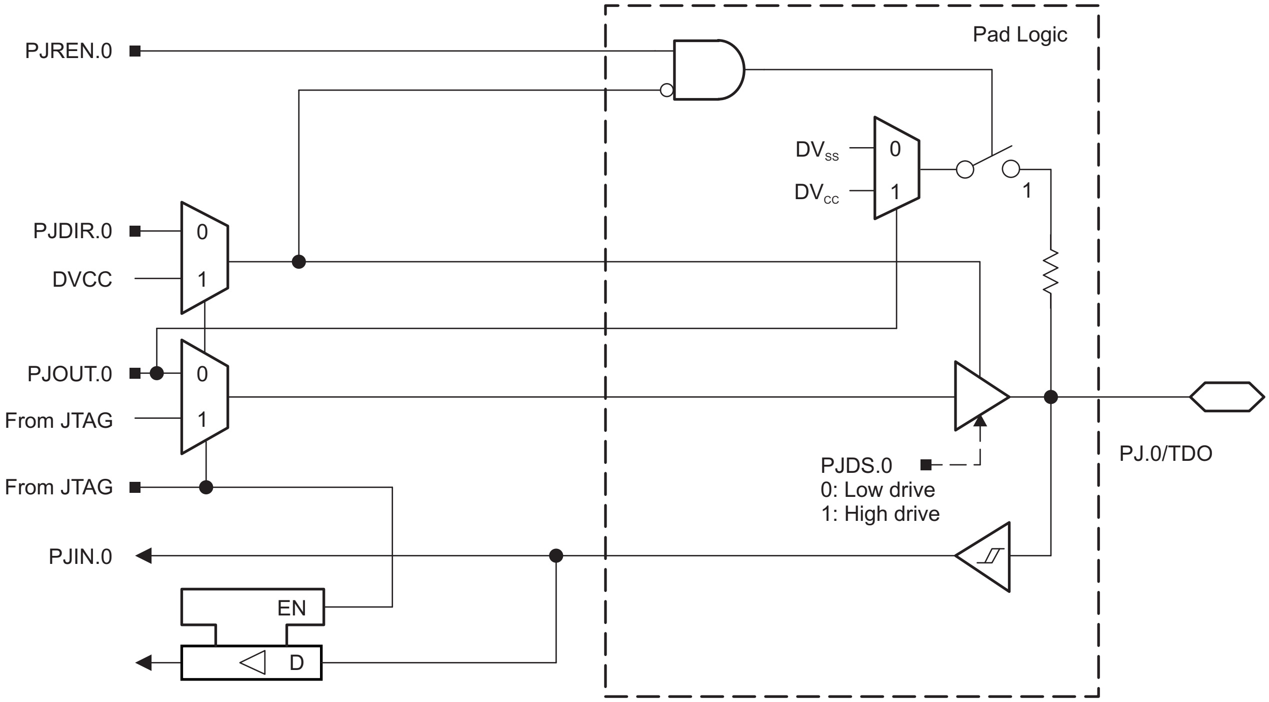

Pad Logic
PJREN.0
DV$_{SS}$
DV$_{CC}$
0
1
1
PJDIR.0
DVCC
0
1
PJOUT.0
From JTAG
0
1
From JTAG
PJIN.0
EN
D
PJDS.0
0: Low drive
1: High drive
PJ.0/TDO

Figure 6-17. Port J (PJ.0) Diagram

6.10.15 Port PJ (PJ.1 to PJ.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

Figure 6-18 shows the port diagram. Table 6-61 summarizes the selection of the pin function.

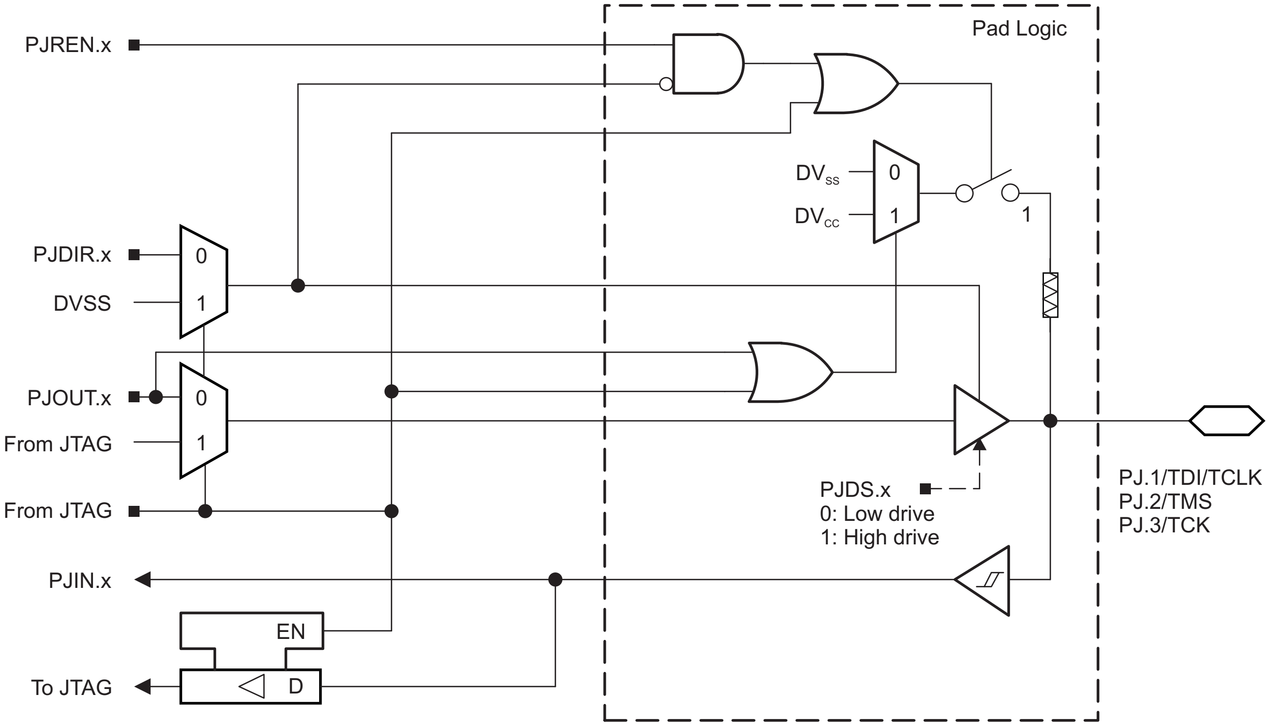

PJREN.x
Pad Logic
DVSS
DVCC
0
1
1
PJDIR.x
DVSS
0
1
PJOUT.x
From JTAG
0
1
From JTAG
PJDS.x
0: Low drive
1: High drive
PJ.1/TDI/TCLK
PJ.2/TMS
PJ.3/TCK
PJIN.x
EN
To JTAG
D

Figure 6-18. Port J (PJ.1 to PJ.3) Diagram

Table 6-61. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS OR SIGNALS[1]
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O)[2]	I: 0; O: 1
		TDO[3]	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O)[2]	I: 0; O: 1
		TDI/TCLK[3] [4]	X
PJ.2/TMS	2	PJ.2 (I/O)[2]	I: 0; O: 1
		TMS[3] [4]	X
PJ.3/TCK	3	PJ.3 (I/O)[2]	I: 0; O: 1
		TCK[3] [4]	X

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.

6.11 Device Descriptors (TLV)

Table 6-62 and Table 6-63 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 6-62. MSP430F552x Device Descriptor Table[1]

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE							
				F5529	F5528	F5527	F5526	F5525	F5524	F5522	F5521
Info Block	Info length	01A00h	1	06h	06h	06h	06h	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h	06h	06h	06h	06h
	CRC value	01A02h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Device ID	01A04h	1	55h	55h	55h	55h	55h	55h	55h	55h
	Device ID	01A05h	1	29h	28h	27h	26h	25h	24h	22h	21h
	Hardware revision	01A06h	1	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Firmware revision	01A07h	1	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
Die Record	Die record tag	01A08h	1	08h	08h	08h	08h	08h	08h	08h	08h
	Die record length	01A09h	1	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/wafer ID	01A0Ah	4	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Die X position	01A0Eh	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Die Y position	01A10h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	Test results	01A12h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
ADC12 Calibration	ADC12 calibration tag	01A14h	1	11h	11h	11h	11h	11h	11h	11h	11h
	ADC12 calibration length	01A15h	1	10h	10h	10h	10h	10h	10h	10h	10h
	ADC gain factor	01A16h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC offset	01A18h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 1.5-V reference Temperature sensor 30°C	01A1Ah	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 1.5-V reference Temperature sensor 85°C	01A1Ch	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V reference Temperature sensor 30°C	01A1Eh	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.0-V reference Temperature sensor 85°C	01A20h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V reference Temperature sensor 30°C	01A22h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	ADC 2.5-V reference Temperature sensor 85°C	01A24h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
REF Calibration	REF calibration tag	01A26h	1	12h	12h	12h	12h	12h	12h	12h	12h
	REF calibration length	01A27h	1	06h	06h	06h	06h	06h	06h	06h	06h
	REF 1.5-V reference factor	01A28h	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	REF 2.0-V reference factor	01A2Ah	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit
	REF 2.5-V reference factor	01A2Ch	2	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit	Per unit

---

(1) N/A = Not applicable, blank = unused and reads FFh.

Table 6-62. MSP430F552x Device Descriptor Table[1] (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE							
				F5529	F5528	F5527	F5526	F5525	F5524	F5522	F5521
Peripheral Descriptor	Peripheral descriptor tag	01A2Eh	1	02h	02h	02h	02h	02h	02h	02h	02h
	Peripheral descriptor length	01A2Fh	1	63h	61h	65h	63h	63h	61h	61h	64h
	Memory 1		2	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah
	Memory 2		2	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h
	Memory 3		2	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah
	Memory 4		2	12h 2Eh	12h 2Eh	12h 2Dh	12h 2Dh	12h 2Ch	12h 2Ch	12h 2Eh	12h 2Dh
	Memory 5		2	22h 96h	22h 96h	2Ah 22h	2Ah 22h	22h 94h	22h 94h	40h 92h	2Ah 40h
	Memory 6		1/2	N/A	N/A	95h 92h	95h 92h	N/A	N/A	N/A	92h
	Delimiter		1	00h	00h	00h	00h	00h	00h	00h	00h
	Peripheral count		1	21h	20h	21h	20h	21h	20h	20h	21h
	MSP430CPUXV2		2	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h
	JTAG		2	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h
	SBW		2	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh
	EEM-L		2	00h 05h	00h 05h	00h 05h	00h 05h	00h 05h	00h 05h	00h 05h	00h 05h
	TI BSL		2	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh
	SFR		2	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h
	PMM		2	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h
	FCTL		2	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h
	CRC16		2	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch
	CRC16_RB		2	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh
	RAMCTL		2	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h
	WDT_A		2	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h
	UCS		2	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h
	SYS		2	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h
	REF		2	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h
	Port mapping		2	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h
	Port 1 and 2		2	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h
	Port 3 and 4		2	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h
	Port 5 and 6		2	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h
	Port 7 and 8		2	02h 54h	N/A	02h 54h	N/A	02h 54h	N/A	N/A	02h 54h

Table 6-62. MSP430F552x Device Descriptor Table[(1)] (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE							
				F5529	F5528	F5527	F5526	F5525	F5524	F5522	F5521
Peripheral Descriptor (continued)	JTAG		2	0Ch 5Fh	0Eh 5Fh	0Ch 5Fh	0Eh 5Fh	0Ch 5Fh	0Eh 5Fh	0Eh 5Fh	0Ch 5Fh
	TA0		2	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h
	TA1		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	TB0		2	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h
	TA2		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	RTC		2	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h
	MPY32		2	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h
	DMA-3		2	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h
	USCI_A and USCI_B		2	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h
	USCI_A and USCI_B		2	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h
	ADC12_A		2	10h D1h	10h D1h	10h D1h	10h D1h	10h D1h	10h D1h	10h D1h	10h D1h
	COMP_B		2	1Ch A8h	1Ch A8h	1Ch A8h	1Ch A8h	1Ch A8h	1Ch A8h	1Ch A8h	1Ch A8h
	USB		2	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h
Interrupts	COMP_B		1	A8h	A8h	A8h	A8h	A8h	A8h	A8h	A8h
	TB0.CCIFG0		1	64h	64h	64h	64h	64h	64h	64h	64h
	TB0.CCIFG1..6		1	65h	65h	65h	65h	65h	65h	65h	65h
	WDTIFG		1	40h	40h	40h	40h	40h	40h	40h	40h
	USCI_A0		1	90h	90h	90h	90h	90h	90h	90h	90h
	USCI_B0		1	91h	91h	91h	91h	91h	91h	91h	91h
	ADC12_A		1	D0h	D0h	D0h	D0h	D0h	D0h	D0h	D0h
	TA0.CCIFG0		1	60h	60h	60h	60h	60h	60h	60h	60h
	TA0.CCIFG1..4		1	61h	61h	61h	61h	61h	61h	61h	61h
	USB		1	98h	98h	98h	98h	98h	98h	98h	98h
	DMA		1	46h	46h	46h	46h	46h	46h	46h	46h
	TA1.CCIFG0		1	62h	62h	62h	62h	62h	62h	62h	62h
	TA1.CCIFG1..2		1	63h	63h	63h	63h	63h	63h	63h	63h
	P1		1	50h	50h	50h	50h	50h	50h	50h	50h
	USCI_A1		1	92h	92h	92h	92h	92h	92h	92h	92h
	USCI_B1		1	93h	93h	93h	93h	93h	93h	93h	93h
	TA1.CCIFG0		1	66h	66h	66h	66h	66h	66h	66h	66h
	TA1.CCIFG1..2		1	67h	67h	67h	67h	67h	67h	67h	67h
	P2		1	51h	51h	51h	51h	51h	51h	51h	51h
	RTC_A		1	68h	68h	68h	68h	68h	68h	68h	68h
	Delimiter		1	00h	00h	00h	00h	00h	00h	00h	00h

Table 6-63. MSP430F551x Device Descriptor Table[1]

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE				
				F5519	F5517	F5515	F5514	F5513
Info Block	Info length	01A00h	1	55h	55h	55h	55h	55h
	CRC length	01A01h	1	19h	17h	15h	14h	13h
	CRC value	01A02h	2	Per unit	Per unit	Per unit	Per unit	Per unit
	Device ID	01A04h	1	22h	21h	55h	55h	20h
	Device ID	01A05h	1	80h	80h	15h	14h	80h
	Hardware revision	01A06h	1	Per unit	Per unit	Per unit	Per unit	Per unit
	Firmware revision	01A07h	1	Per unit	Per unit	Per unit	Per unit	Per unit
Die Record	Die record tag	01A08h	1	08h	08h	08h	08h	08h
	Die record length	01A09h	1	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/wafer ID	01A0Ah	4	Per unit	Per unit	Per unit	Per unit	Per unit
	Die X position	01A0Eh	2	Per unit	Per unit	Per unit	Per unit	Per unit
	Die Y position	01A10h	2	Per unit	Per unit	Per unit	Per unit	Per unit
	Test results	01A12h	2	Per unit	Per unit	Per unit	Per unit	Per unit
ADC12 Calibration	ADC12 calibration tag	01A14h	1	05h	05h	11h	11h	05h
	ADC12 calibration length	01A15h	1	10h	10h	10h	10h	10h
	ADC gain factor	01A16h	2	blank	blank	blank	blank	blank
	ADC offset	01A18h	2	blank	blank	blank	blank	blank
	ADC 1.5-V reference Temperature sensor 30°C	01A1Ah	2	blank	blank	blank	blank	blank
	ADC 1.5-V reference Temperature sensor 85°C	01A1Ch	2	blank	blank	blank	blank	blank
	ADC 2.0-V reference Temperature sensor 30°C	01A1Eh	2	blank	blank	blank	blank	blank
	ADC 2.0-V reference Temperature sensor 85°C	01A20h	2	blank	blank	blank	blank	blank
	ADC 2.5-V reference Temperature sensor 30°C	01A22h	2	blank	blank	blank	blank	blank
	ADC 2.5-V reference Temperature sensor 85°C	01A24h	2	blank	blank	blank	blank	blank
REF Calibration	REF calibration tag	01A26h	1	12h	12h	12h	12h	12h
	REF calibration length	01A27h	1	06h	06h	06h	06h	06h
	REF 1.5-V reference factor	01A28h	2	Per unit	Per unit	Per unit	Per unit	Per unit
	REF 2.0-V reference factor	01A2Ah	2	Per unit	Per unit	Per unit	Per unit	Per unit
	REF 2.5-V reference factor	01A2Ch	2	Per unit	Per unit	Per unit	Per unit	Per unit

---

(1) N/A = not applicable, blank = unused and reads FFh.

Table 6-63. MSP430F551x Device Descriptor Table[1] (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE				
				F5519	F5517	F5515	F5514	F5513
Peripheral Descriptor	Peripheral descriptor tag	01A2Eh	1	02h	02h	02h	02h	02h
	Peripheral descriptor length	01A2Fh	1	61h	63h	61h	5Fh	5Fh
	Memory 1		2	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah	08h 8Ah
	Memory 2		2	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h	0Ch 86h
	Memory 3		2	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah	0Eh 2Ah
	Memory 4		2	12h 2Eh	12h 2Dh	12h 2Ch	12h 2Ch	12h 2Ch
	Memory 5		2	22h 96h	2Ah 22h	22h 94h	22h 94h	40h 92h
	Memory 6		1/2	N/A	95h 92h	N/A	N/A	N/A
	Delimiter		1	00h	00h	00h	00h	00h
	Peripheral count		1	20h	20h	20h	1Fh	1Fh
	MSP430CPUXV2		2	00h 23h	00h 23h	00h 23h	00h 23h	00h 23h
	JTAG		2	00h 09h	00h 09h	00h 09h	00h 09h	00h 09h
	SBW		2	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh	00h 0Fh
	EEM-L		2	00h 05h	00h 05h	00h 05h	00h 05h	00h 05h
	TI BSL		2	00h FCh	00h FCh	00h FCh	00h FCh	00h FCh
	SFR		2	10h 41h	10h 41h	10h 41h	10h 41h	10h 41h
	PMM		2	02h 30h	02h 30h	02h 30h	02h 30h	02h 30h
	FCTL		2	02h 38h	02h 38h	02h 38h	02h 38h	02h 38h
	CRC16		2	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch	01h 3Ch
	CRC16_RB		2	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh	00h 3Dh
	RAMCTL		2	00h 44h	00h 44h	00h 44h	00h 44h	00h 44h
	WDT_A		2	00h 40h	00h 40h	00h 40h	00h 40h	00h 40h
	UCS		2	01h 48h	01h 48h	01h 48h	01h 48h	01h 48h
	SYS		2	02h 42h	02h 42h	02h 42h	02h 42h	02h 42h
	REF		2	03h A0h	03h A0h	03h A0h	03h A0h	03h A0h
	Port mapping		2	01h 10h	01h 10h	01h 10h	01h 10h	01h 10h
	Port 1 and 2		2	04h 51h	04h 51h	04h 51h	04h 51h	04h 51h
	Port 3 and 4		2	02h 52h	02h 52h	02h 52h	02h 52h	02h 52h
	Port 5 and 6		2	02h 53h	02h 53h	02h 53h	02h 53h	02h 53h
	Port 7 and 8		2	02h 54h	02h 54h	02h 54h	N/A	N/A

Table 6-63. MSP430F551x Device Descriptor Table[(1)] (continued)

DESCRIPTION		ADDRESS	SIZE (bytes)	VALUE				
				F5519	F5517	F5515	F5514	F5513
Peripheral Descriptor (continued)	JTAG		2	0Ch 5Fh	0Ch 5Fh	0Ch 5Fh	0Eh 5Fh	0Eh 5Fh
	TA0		2	02h 62h	02h 62h	02h 62h	02h 62h	02h 62h
	TA1		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	TB0		2	04h 67h	04h 67h	04h 67h	04h 67h	04h 67h
	TA2		2	04h 61h	04h 61h	04h 61h	04h 61h	04h 61h
	RTC		2	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h	0Ah 68h
	MPY32		2	02h 85h	02h 85h	02h 85h	02h 85h	02h 85h
	DMA-3		2	04h 47h	04h 47h	04h 47h	04h 47h	04h 47h
	USCI_A and USCI_B		2	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h	0Ch 90h
	USCI_A and USCI_B		2	04h 90h	04h 90h	04h 90h	04h 90h	04h 90h
	ADC12_A		2	N/A	N/A	N/A	N/A	N/A
	COMP_B		2	2Ch A8h	2Ch A8h	2Ch A8h	2Ch A8h	2Ch A8h
	USB		2	04h 98h	04h 98h	04h 98h	04h 98h	04h 98h
Interrupts	COMP_B		1	A8h	A8h	A8h	A8h	A8h
	TB0.CCIFG0		1	64h	64h	64h	64h	64h
	TB0.CCIFG1..6		1	65h	65h	65h	65h	65h
	WDTIFG		1	40h	40h	40h	40h	40h
	USCI_A0		1	90h	90h	90h	90h	90h
	USCI_B0		1	91h	91h	91h	91h	91h
	ADC12_A		1	01h	01h	01h	01h	01h
	TA0.CCIFG0		1	60h	60h	60h	60h	60h
	TA0.CCIFG1..4		1	61h	61h	61h	61h	61h
	USB		1	98h	98h	98h	98h	98h
	DMA		1	46h	46h	46h	46h	46h
	TA1.CCIFG0		1	62h	62h	62h	62h	62h
	TA1.CCIFG1..2		1	63h	63h	63h	63h	63h
	P1		1	50h	50h	50h	50h	50h
	USCI_A1		1	92h	92h	92h	92h	92h
	USCI_B1		1	93h	93h	93h	93h	93h
	TA1.CCIFG0		1	66h	66h	66h	66h	66h
	TA1.CCIFG1..2		1	67h	67h	67h	67h	67h
	P2		1	51h	51h	51h	51h	51h
	RTC_A		1	68h	68h	68h	68h	68h
	Delimiter		1	00h	00h	00h	00h	00h

7 器件和文档支持

7.1 入门和后续步骤

关于 MSP 系列器件以及开发协助工具和库的简介，请访问入门页面。

7.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

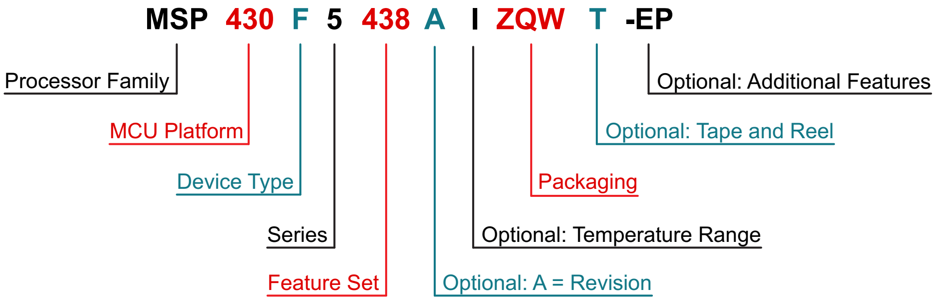
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. 图 7-1 provides a legend for reading the complete device name.


MSP 430 F 5 438 A I ZQW T -EP
Processor Family
MCU Platform
Device Type
Series
Feature Set
Optional: A = Revision
Optional: Temperature Range
Packaging
Optional: Tape and Reel
Optional: Additional Features

Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory	**Specialized Application** AFE = Analog Front End BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD 0 = Low-Voltage Series
Feature Set	Various levels of integration within a series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced Product (–40°C to 105°C) -HT = Extreme Temperature Parts (–55°C to 150°C) -Q1 = Automotive Q100 Qualified	

图 7-1. Device Nomenclature

7.3 工具与软件

所有 MSP 微控制器均受多种软件和硬件开发工具的支持。相关工具由 TI 以及多家第三方供应商提供。请参阅 MSP430 超低功耗 MCU – 工具与软件，了解所有工具。

表 7-1 列出了 MSP430FR203x 微控制器所 了 的调试功能。关于可用特性的详细信息，请参见*《适用于 MSP430 的 Code Composer Studio 用户指南》*。

表 **7-1.** 硬件调试 特性

MSP430 架构	四线制 JTAG	2 线 JTAG	断点 (N)	范围断点	时钟控制	状态序列发生器	跟踪缓冲器	LPMx.5 调试支持
MSP430Xv2	有	是	8	是	是	是	是	否

设计套件与评估模块

MSP430F5529 USB LaunchPad 评估套件 利用集成的 全速 USB 2.0 (HID/MSC/CDC) 开发 连接 PC 的低功耗应用。MSP-EXP430F5529LP LaunchPad 是适用于 MSP430F5529 USB 微控制器的廉价、简单的微控制器开发套件。这是在 MSP430 MCU 上开始开发的一种简单方法，具有用于编程和调试的板载仿真功能，以及用于简化用户界面的按钮和 LED。

MSP430F5529 USB 实验板 MSP430F5529 实验板 (MSP-EXP430F5529) 是一个用于 MSP430F5529 器件（来自最新一代具有集成 USB 的 MSP430 器件）的开发平台。该实验板兼容多种 TI 低功耗射频无线评估模块（例如，CC2520EMK）。实验板可帮助设计人员利用新型 F55xx MCU 快速学习和开发，F55xx MCU 为能量收集、无线传感以及自动抄表基础设施 (AMI) 等 应用 提供低功耗、更多内存和领先的集成技术。

适用于 MSP430F5x MCU 的 64 引脚目标开发板和 MSP-FET 编程器捆绑包 MSP-FET430U64USB 是一款强大的闪存仿真工具，可在 MSP430 MCU 上快速开始应用开发。它包含 USB 调试接口，用于通过 JTAG 接口或节省引脚的 Spy Bi-Wire（2 线 JTAG）协议在系统内对 MSP430 进行编程和调试。只需使用几个按键即可在数秒钟内擦除闪存并对其进行编程。由于 MSP430 闪存的功耗极低，因此无需外部电源。

适用于 MSP430F5x MCU 的 80 引脚目标开发板和 MSP-FET 编程器捆绑包 MSP-FET 是一款强大的闪存仿真工具，可在 MSP430 MCU 上快速开始应用开发。它包含 USB 调试接口，用于通过 JTAG 接口或节省引脚的 Spy-Bi-Wire（2 线 JTAG）协议在系统内对 MSP430 进行编程和调试。只需使用几个按键即可在数秒钟内擦除闪存并对其进行编程。由于 MSP430 闪存的功耗极低，因此无需外部电源。调试工具可将 MSP430 连接到附带的集成软件环境，提供的代码可帮助您立即开始设计工作。

软件

MSP430Ware™ 软件 MSP430Ware 软件集合了所有 MSP430 器件的代码示例、产品说明书以及其他设计资源，打包提供给用户。除了提供已有 MSP430 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件可作为 Code Composer Studio™IDE 的一部分提供，也可以以独立软件包的形式提供。

MSP430F552x 代码示例 根据不同应用需求配置各集成外设的每个 MSP 器件均具备相应的 C 代码示例。

MSP 驱动程序库 驱动程序库的抽象化 API 通过提供易于使用的函数调用使您不再拘泥于 MSP430 硬件的细节。完整的文档通过具有帮助意义的 API 指南交付，其中包括有关每个函数调用和经过验证的参数的详细信息。开发人员可以使用驱动程序库功能，以最低开销编写完整项目。

MSP EnergyTrace™ 技术 MSP430 微控制器的 EnergyTrace 技术是基于能量的代码分析工具，用于测量和显示应用的能量配置，同时协助优化应用以实现超低功耗。

ULP（超低功耗）Advisor ULP Advisor™软件是一款辅助工具，旨在指导开发人员编写更为高效的代码，从而充分利用 MSP 和 MSP432 微控制器独特的 超低功耗 功能。ULP Advisor 的目标人群是微控制器的资深开发者和开发新手，可以根据详尽的 ULP 检验表检查代码，以便最大限度地利用应用程序。在编译时，ULP Advisor 会提供通知和备注以突出显示代码中可以进一步优化的区域，进而实现更低功耗。

IEC60730 软件包 IEC60730 MSP430 软件包经过专门开发，用于协助客户达到 IEC 60730-1:2010（家用及类似用途的自动化电气控制 - 第 1 部分：一般要求）B 类产品的要求。其中涵盖家用电器、电弧检测器、电源转换器、电动工具、电动自行车及其他诸多产品。IEC60730 MSP430 软件包可以嵌入在 MSP430 中 运行的客户应用， 从而帮助客户简化其消费类器件在功能安全方面遵循 IEC 60730-1:2010 B 类规范的认证工作。

适用于 MSP 的定点数学运算库 MSP IQmath 和 Qmath 库是为 C 语言开发者提供的一套经过高度优化的高

精度数学运算函数集合，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集型实时 应用， 而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

适用于 MSP430 的浮点数学运算库 TI 在低功耗和低成本微控制器领域锐意创新，为您提供 MSPMATHLIB。这是标量函数的浮点数学运算库，能够充分利用器件的智能外设，使性能提升高达 26 倍。Mathlib 能够轻松集成到您的设计中。该运算库免费使用并集成在 Code Composer Studio 和 IAR IDE 中。如需深入了解该数学运算库及相关基准，请阅读用户指南。

开发工具

适用于 MSP 微控制器的 Code Composer Studio™ 集成开发环境 Code Composer Studio 是一种集成开发环境 (IDE)，支持所有 MSP 微控制器。Code Composer Studio 包含一整套开发和调试嵌入式应用 的嵌入式软件实用程序的工具。它包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他多种 功能。直观的 IDE 提供了单个用户界面，有助于完成应用程序开发流程的每个步骤。熟悉的实用程序和界面可提升用户的入门速度。Code Composer Studio 将 Eclipse 软件框架的优点和 TI 先进的嵌入式调试功能相结合，为嵌入式开发人员提供了一种功能丰富的优异开发环境。当 CCS 与 MSP MCU 搭配使用时，可以使用独特而强大的插件和嵌入式软件实用程序，从而充分利用 MSP 微控制器的功能。

命令行编程器 MSP Flasher 是一款基于 shell 的开源接口，可使用 JTAG 或 Spy-Bi-Wire (SBW) 通信通过 FET 编程器或 eZ430 对 MSP 微控制器进行编程。MSP Flasher 可用于将二进制文件（.txt 或 .hex 文件）直接下载到 MSP 微控制器，而无需使用 IDE。

MSP MCU 编程器和调试器 MSP-FET 是一款强大的仿真开发工具（通常称为调试探针），可帮助用户在 MSP 低功耗微控制器 (MCU) 中快速开发应用。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件，以进行验证和调试。MSP-FET 在主机和目标 MSP 间提供调试通信通道。此外，MSP-FET 还可在计算机的 USB 接口和 MSP UART 间提供反向通道 UART 连接。这为 MSP 编程器提供了一种在 MSP 和计算机上运行的终端之间进行串行通信的便捷方法。它还支持使用 BSL（引导加载程序）通过 UART 和 I^{2}C 通信协议将程序（通常称为固件）加载到 MSP 目标中。

MSP-GANG 生产编程器	MSP Gang 编程器是一款 MSP430 或 MSP432™器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。MSP Gang 编程器配有扩展板，即“Gang 分离器”，可在 MSP Gang 编程器和多个目标器件间实施互连。提供了八条电缆，用于将扩展板与八个目标器件相连（通过 JTAG 或 SPY-Bi-Wire 连接器）。编程工作可在 PC 或独立设备上完成。PC 端具备基于 DLL 的图形化用户界面。

7.4 文档支持

以下文档介绍了 MSP430F552x 和 MSP430F551x 器件。www.ti.com.cn 网站上提供了这些文档的副本。

接收文档更新通知

如需接收文档更新通知（包括芯片勘误表），请访问 ti.com.cn 网站上的器件产品文件夹（例如 MSP430F5529）。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

勘误

《**MSP430F5529** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。
《**MSP430F5528** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。
《**MSP430F5527** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。
《**MSP430F5526** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。
《**MSP430F5525** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。
《**MSP430F5524** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。
《**MSP430F5522** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。
《**MSP430F5521** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。
《**MSP430F5519** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。
《**MSP430F5517** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。
《**MSP430F5515** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。
《**MSP430F5514** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。
《**MSP430F5513** 器件勘误表》	描述了此器件所有芯片修订版本的功能技术规格的已知例外情况。

用户指南

《**MSP430x5xx** 和 **MSP430x6xx** 系列用户指南》 详细介绍了该器件系列提供的模块和外设。

《适用于 **MSP430 MCU** 的 **Code Composer Studio IDE** 用户指南》 此用户指南介绍如何将 TI Code Composer Studio IDE 与 MSP430 超低功耗微控制器结合使用。

《**MSP430** 闪存器件引导加载程序 **(BSL)** 用户指南》 MSP430 引导加载程序 (BSL) 允许用户在原型设计、投产和维护等各阶段与 MSP430 微控制器中的嵌入式存储器进行通信。可编程存储器（闪存）和数据存储器 (RAM) 可根据相关要求进行变更。不要将此处的引导加载程序与某些数字信号处理器 (DSP) 中将外部存储器中的程序代码（和数据）自动加载到 DSP 内部存储器的引导装载程序混为一谈。

《通过 **JTAG** 接口对 **MSP430** 进行编程》 此文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。此外，该文档还介绍了如何编程所有 MSP430 器件上均具备的 JTAG 访问安全保险丝。此文档介绍了使用标准四线制 JTAG 接口和两线制 JTAG 接口（也称为 Spy-Bi-Wire (SBW)）的器件访问。

《**MSP430** 硬件工具用户指南》 此手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。文中对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

应用报告

《**MSP430 32kHz** 晶体振荡器》 选择合适的晶体、正确的负载电路和适当的电路板布局是实现稳定的晶体振荡器的关键。该应用报告总结了晶体振荡器的功能，介绍了用于选择合适的晶体以实现 MSP430 超低功耗运行的参数。此外，还给出了正确电路板布局的提示和示例。此外，为了确保振荡器在大规模生产后能够稳定运行，还可能需要进行一些振荡器测试，该文档中提供了有关这些测试的详细信息。

《**MSP430** 系统级 **ESD** 注意事项》 系统级 ESD 对于低电压下的硅晶技术以及经济高效型和超低功耗组件的需求日益增加。此应用报告重点讨论了三个不同的 ESD 主题，以帮助板卡设计师和原始设备制造商 (OEM) 理解和设计稳健的系统级设计产品：(1) 组件级 ESD 测试和系统级 ESD 测试，二者的差异以及为何组件级 ESD 无法确保达到系统级的稳健性。(2) 系统级 ESD 保护在不同电平下的通用设计指南（包括外壳、电缆、PCB 布局和板载 ESD 防护器件）。(3) 介绍了系统高效 ESD 设计 (SEED)。这是一种板上和片上 ESD 保护协同设计的方法论，用于实现系统级 ESD 的稳健性，配备仿真示例和测试结果。另外，还讨论了一些真实的系统级 ESD 保护设计示例及其成果。

7.5 相关链接

表 7-2 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具与软件，以及申请样片或购买产品的快速链接。

表 **7-2.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具与软件	支持和社区
MSP430F5529	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5528	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5527	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5526	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5525	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5524	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5522	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5521	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5519	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5517	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5515	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5514	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
MSP430F5513	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

7.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的 《使用条款》 。

TI E2E™ 社区
TI 的工程师交流 (E2E) 社区. 此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

TI 嵌入式处理器维基网页
德州仪器 (TI) 嵌入式处理器维基网页。此网站的建立是为了帮助开发人员熟悉德州仪器 (TI) 的嵌入式处理器，并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

7.7 商标

MSP430, MicroStar Junior, MSP430Ware, Code Composer Studio, EnergyTrace, ULP Advisor, 适用于 MSP 微控制器的 Code Composer Studio, MSP432, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

7.8 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

8 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2018 德州仪器半导体技术（上海）有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ASP00886IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5522	Samples
ASP00886IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5522	Samples
MSP430F5513IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	M430F5513	Samples
MSP430F5513IZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430F5513	Samples
MSP430F5514IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	M430F5514	Samples
MSP430F5514IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	M430F5514	Samples
MSP430F5514IZQE	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	490	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430F5514	Samples
MSP430F5514IZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430F5514	Samples
MSP430F5515IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5515	Samples
MSP430F5515IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5515	Samples
MSP430F5517IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5517	Samples
MSP430F5517IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5517	Samples
MSP430F5519IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5519	Samples
MSP430F5519IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5519	Samples
MSP430F5521IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5521	Samples
MSP430F5521IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5521	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F5522IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	M430F5522	Samples
MSP430F5522IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	M430F5522	Samples
MSP430F5522IZQE	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	490	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430F5522	Samples
MSP430F5522IZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430F5522	Samples
MSP430F5524IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	M430F5524	Samples
MSP430F5524IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	M430F5524	Samples
MSP430F5524IZQE	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	490	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430F5524	Samples
MSP430F5524IZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430F5524	Samples
MSP430F5525IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5525	Samples
MSP430F5525IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5525	Samples
MSP430F5526IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	M430F5526	Samples
MSP430F5526IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	M430F5526	Samples
MSP430F5526IZQE	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	490	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430F5526	Samples
MSP430F5526IZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430F5526	Samples
MSP430F5527IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5527	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F5527IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5527	Samples
MSP430F5528IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	M430F5528	Samples
MSP430F5528IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-3-260C-168 HR	-40 to 85	M430F5528	Samples
MSP430F5528IYFFR	ACTIVE	DSBGA	YFF	64	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	M430F5528	Samples
MSP430F5528IZQE	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	490	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430F5528	Samples
MSP430F5528IZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	M430F5528	Samples
MSP430F5529IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5529	Samples
MSP430F5529IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F5529	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

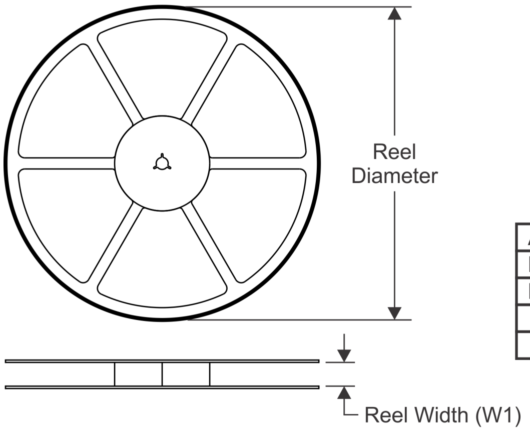
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

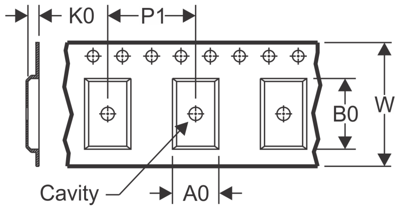
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

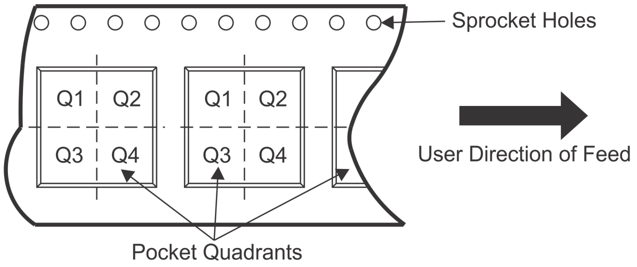


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

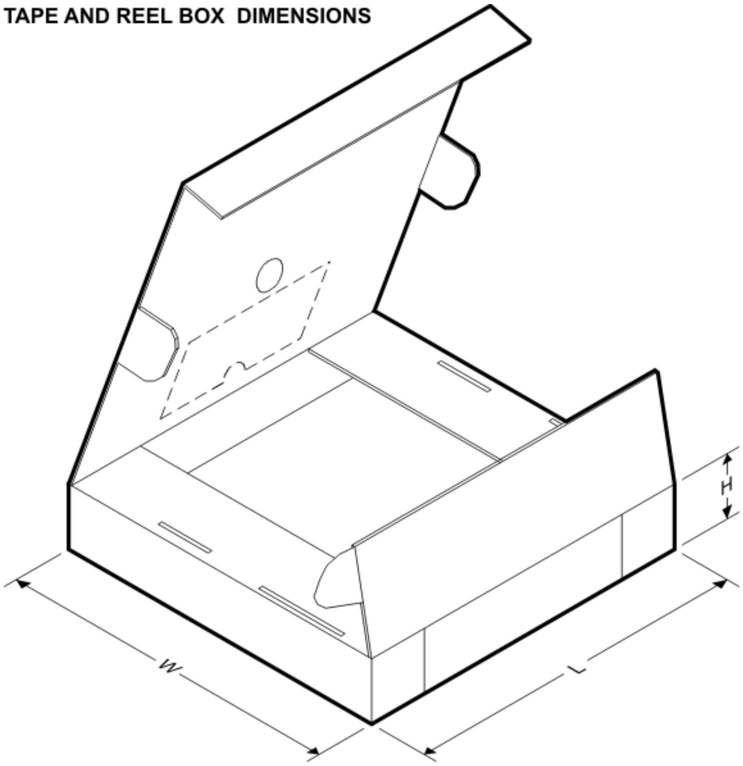


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F5513IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5513IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
MSP430F5514IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5514IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
MSP430F5515IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F5517IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F5519IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F5521IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F5522IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5522IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
MSP430F5524IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5524IZQER	BGA MI	ZQE	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	CROSTAR JUNIOR											
MSP430F5525IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F5526IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5526IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5526IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
MSP430F5527IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2
MSP430F5528IRGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F5528IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
MSP430F5529IPNR	LQFP	PN	80	1000	330.0	24.4	15.0	15.0	2.1	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

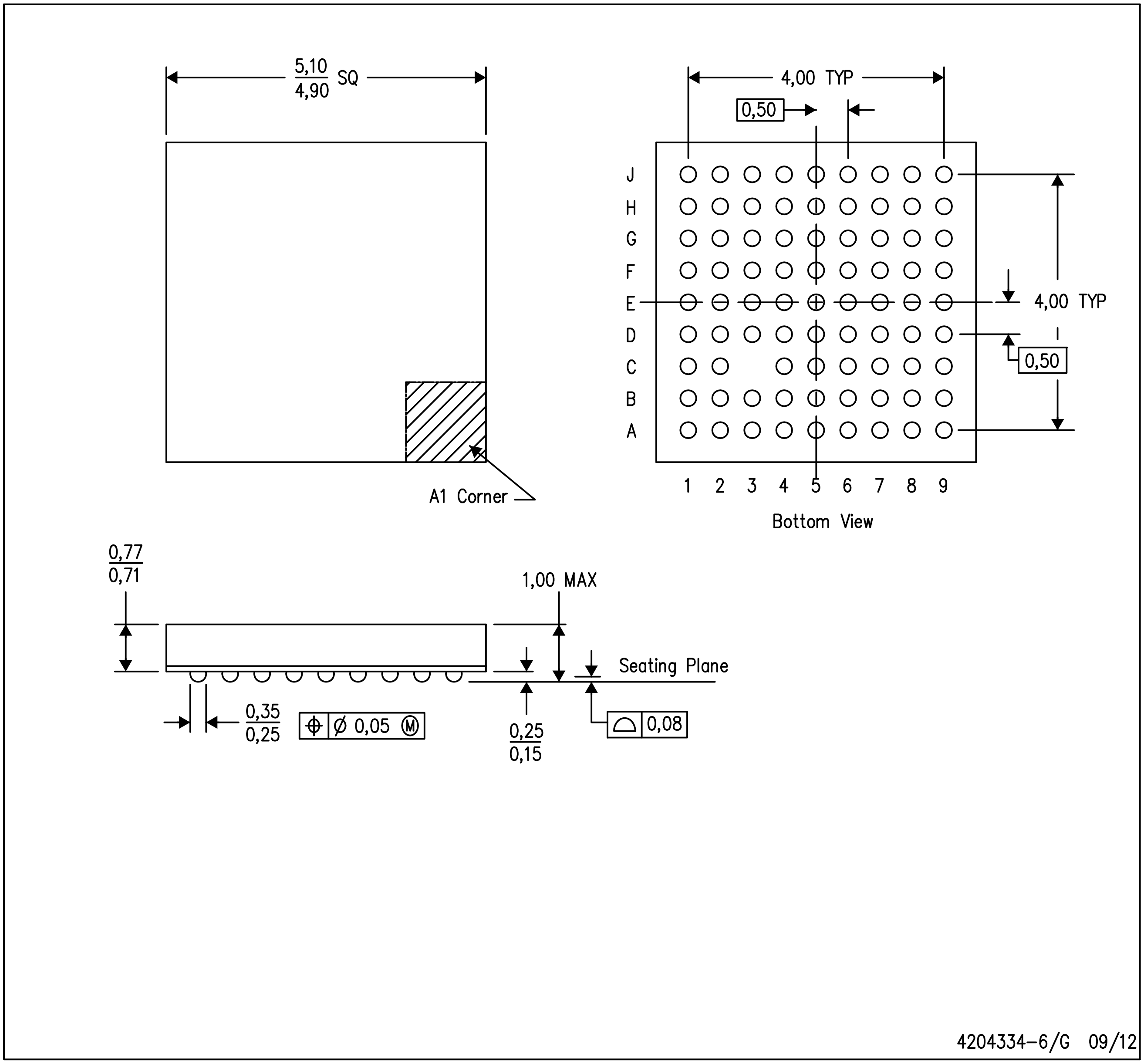


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F5513IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430F5513IZQER	BGA MICROSTAR	ZQE	80	2500	350.0	350.0	43.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	JUNIOR						
MSP430F5514IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5514IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	350.0	350.0	43.0
MSP430F5515IPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F5517IPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F5519IPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F5521IPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F5522IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5522IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	350.0	350.0	43.0
MSP430F5524IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5524IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	350.0	350.0	43.0
MSP430F5525IPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F5526IRGCR	VQFN	RGC	64	2000	367.0	367.0	38.0
MSP430F5526IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5526IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	350.0	350.0	43.0
MSP430F5527IPNR	LQFP	PN	80	1000	350.0	350.0	43.0
MSP430F5528IRGCT	VQFN	RGC	64	250	210.0	185.0	35.0
MSP430F5528IZQER	BGA MICROSTAR JUNIOR	ZQE	80	2500	350.0	350.0	43.0
MSP430F5529IPNR	LQFP	PN	80	1000	350.0	350.0	43.0

ZQE (S-PBGA-N80) PLASTIC BALL GRID ARRAY


5,10
4,90
SQ
A1 Corner
4,00 TYP
0,50
J
H
G
F
E
D
C
B
A
1
2
3
4
5
6
7
8
9
Bottom View
4,00 TYP
0,50
0,77
0,71
1,00 MAX
Seating Plane
0,35
0,25
⌖ Ø 0,05 Ⓜ
0,25
0,15
⌓ 0,08
4204334-6/G 09/12

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-225
- D. This is a Pb-free solder ball design.

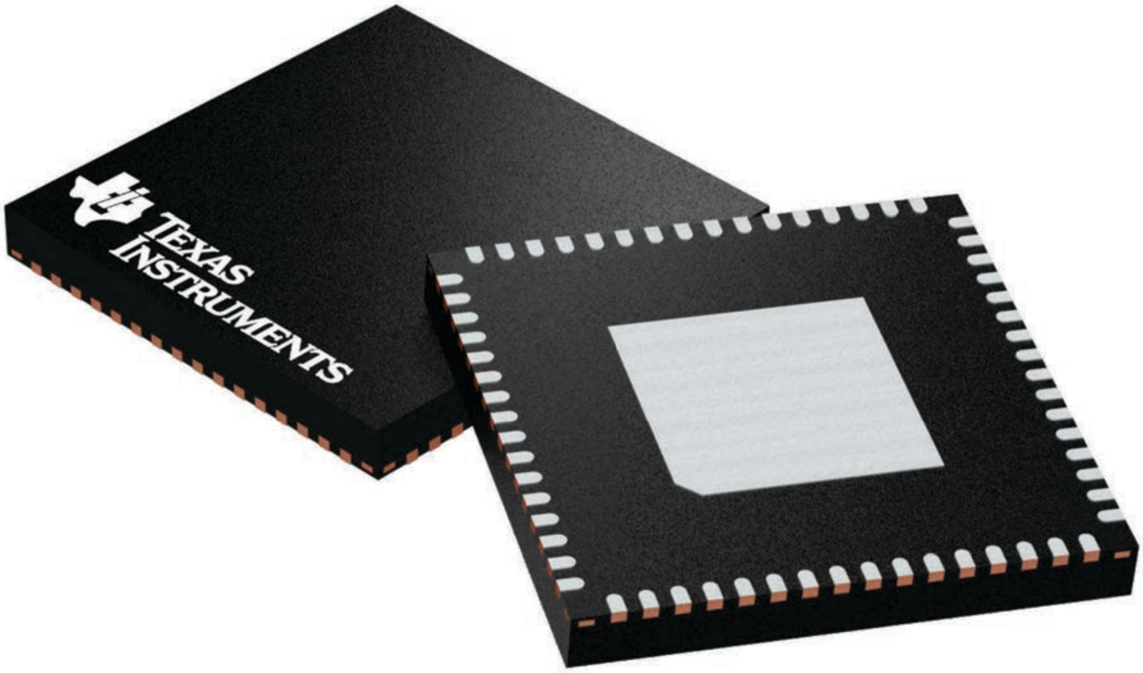
MicroStar Junior is a trademark of Texas Instruments.

RGC 64

VQFN - 1 mm max height

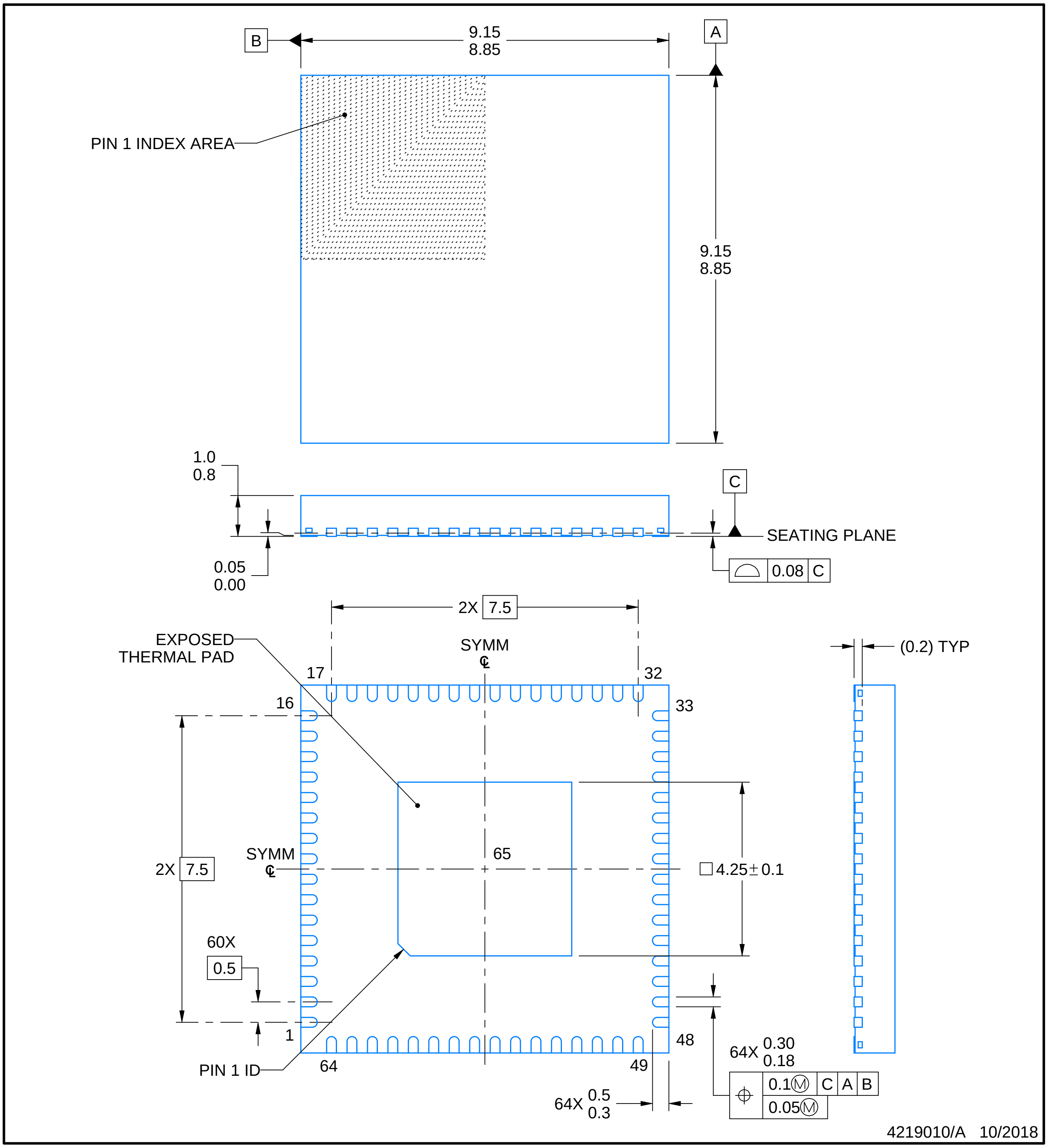
9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



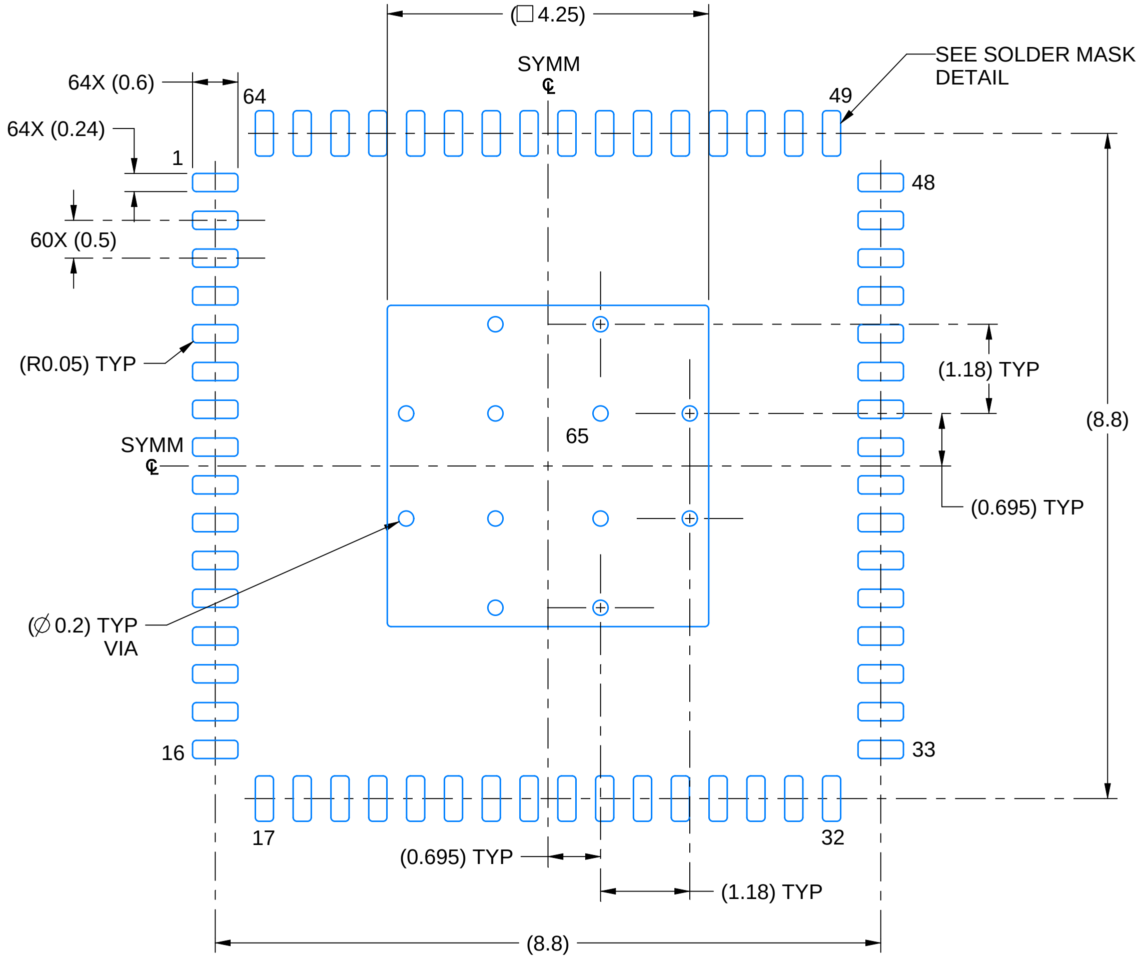
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224597/A

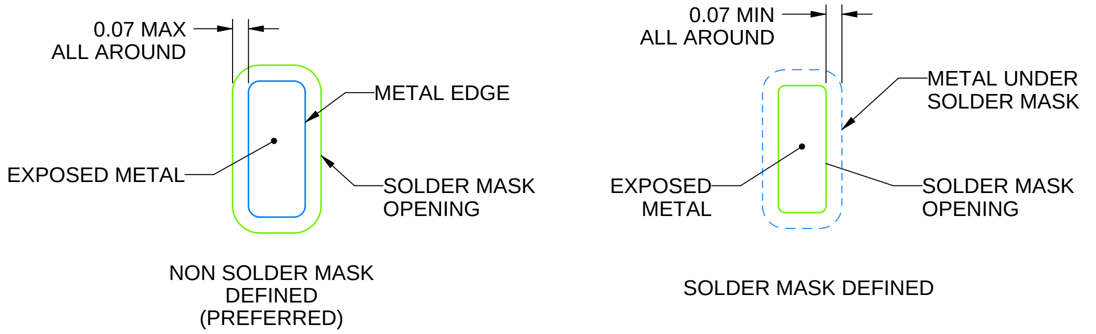

B
9.15
8.85
A
PIN 1 INDEX AREA
9.15
8.85
1.0
0.8
C
SEATING PLANE
0.05
0.00
0.08 C
2X 7.5
EXPOSED THERMAL PAD
SYMM
17
32
(0.2) TYP
16
33
65
2X 7.5
SYMM
4.25±0.1
60X 0.5
1
48
PIN 1 ID
64
49
64X 0.30 0.18
0.1Ⓜ C A B
0.05Ⓜ
64X 0.5 0.3
4219010/A 10/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.


(□4.25)
64X (0.6)
64X (0.24)
SYMM
℄
64
49
SEE SOLDER MASK DETAIL
1
48
60X (0.5)
(R0.05) TYP
(1.18) TYP
(8.8)
65
SYMM
℄
(0.695) TYP
(∅0.2) TYP
VIA
16
33
17
32
(0.695) TYP
(1.18) TYP
(8.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

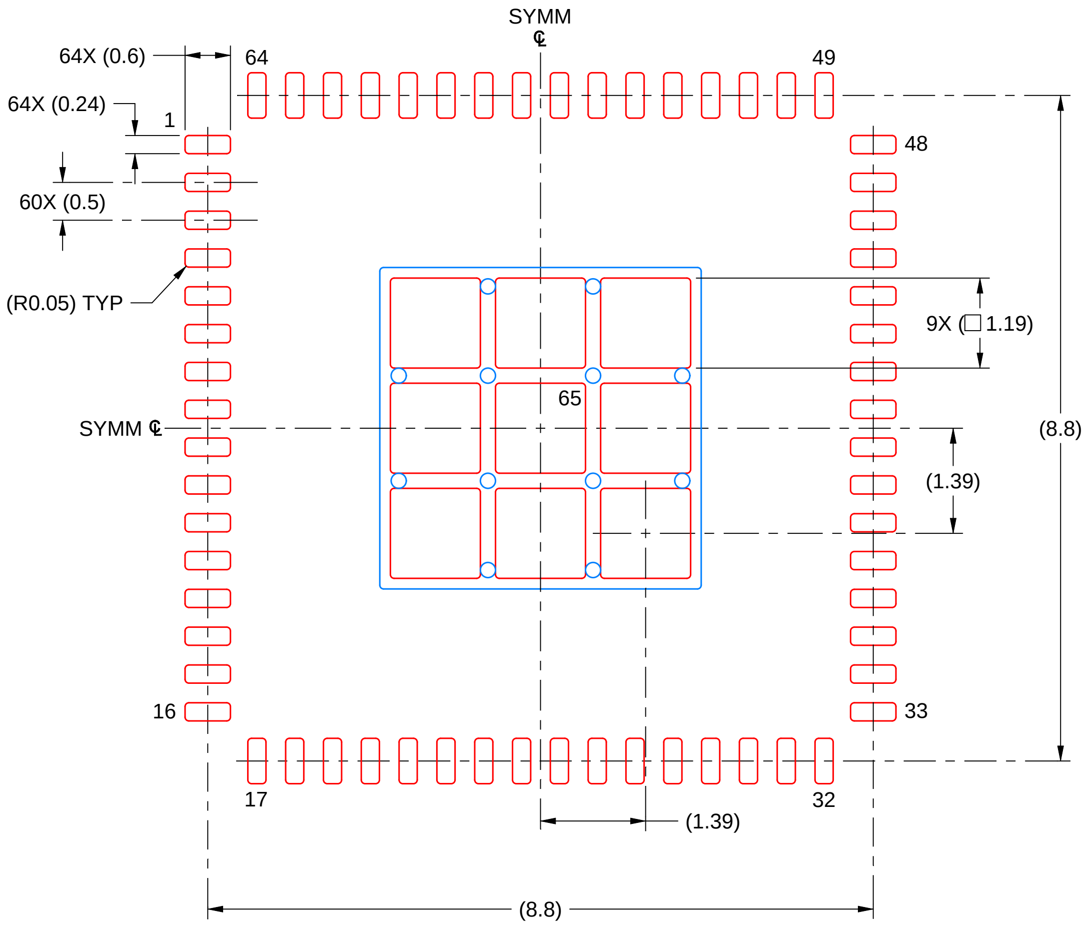

0.07 MAX
ALL AROUND
METAL EDGE
EXPOSED METAL
SOLDER MASK OPENING
NON SOLDER MASK DEFINED
(PREFERRED)
0.07 MIN
ALL AROUND
METAL UNDER SOLDER MASK
EXPOSED METAL
SOLDER MASK OPENING
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4219010/A 10/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.


SYMM
℄
64X (0.6)
64
49
64X (0.24)
1
48
60X (0.5)
(R0.05) TYP
9X (☐1.19)
65
SYMM ℄
(8.8)
(1.39)
16
33
17
32
(1.39)
(8.8)

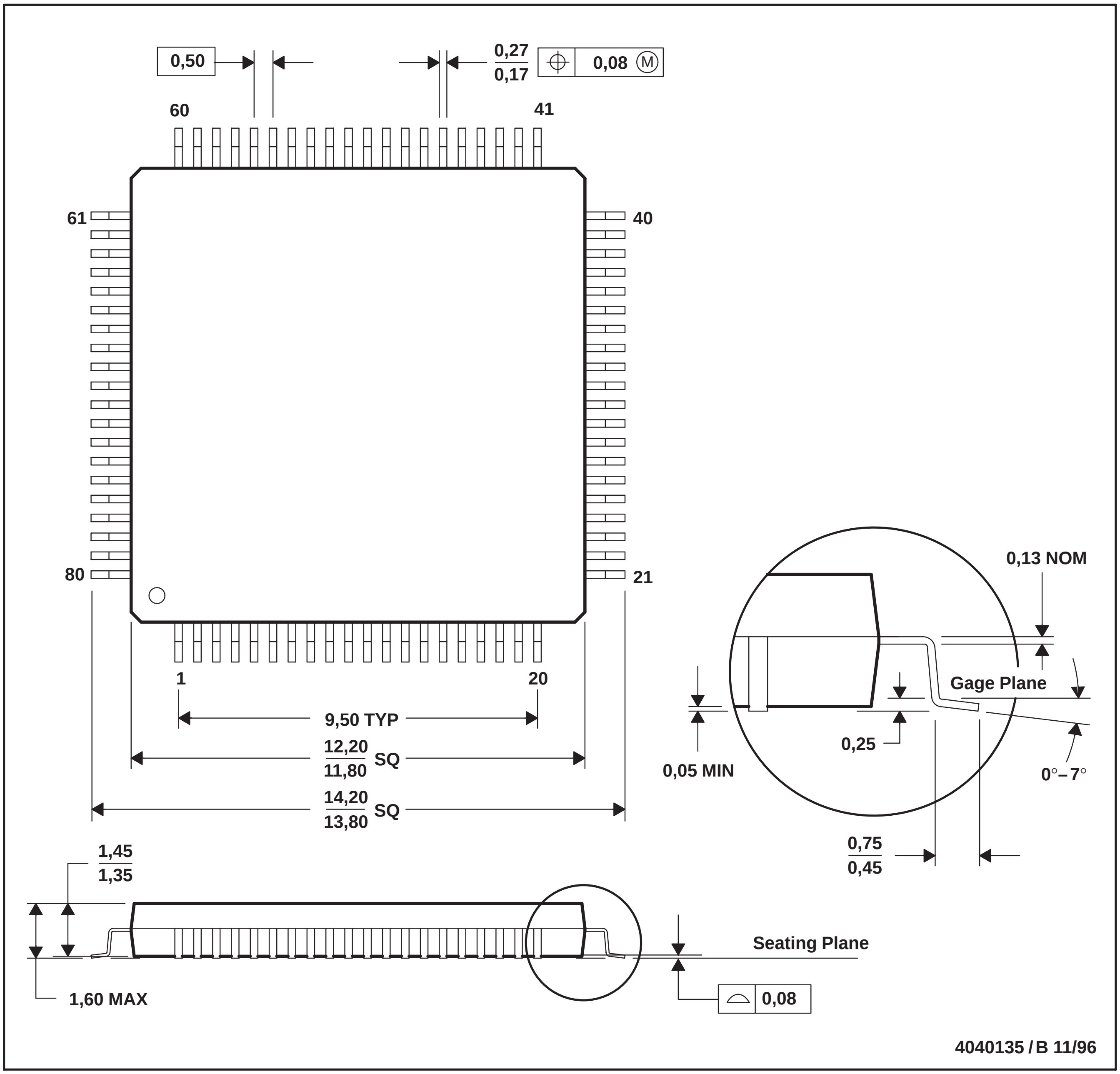
SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

NOTES: (continued)

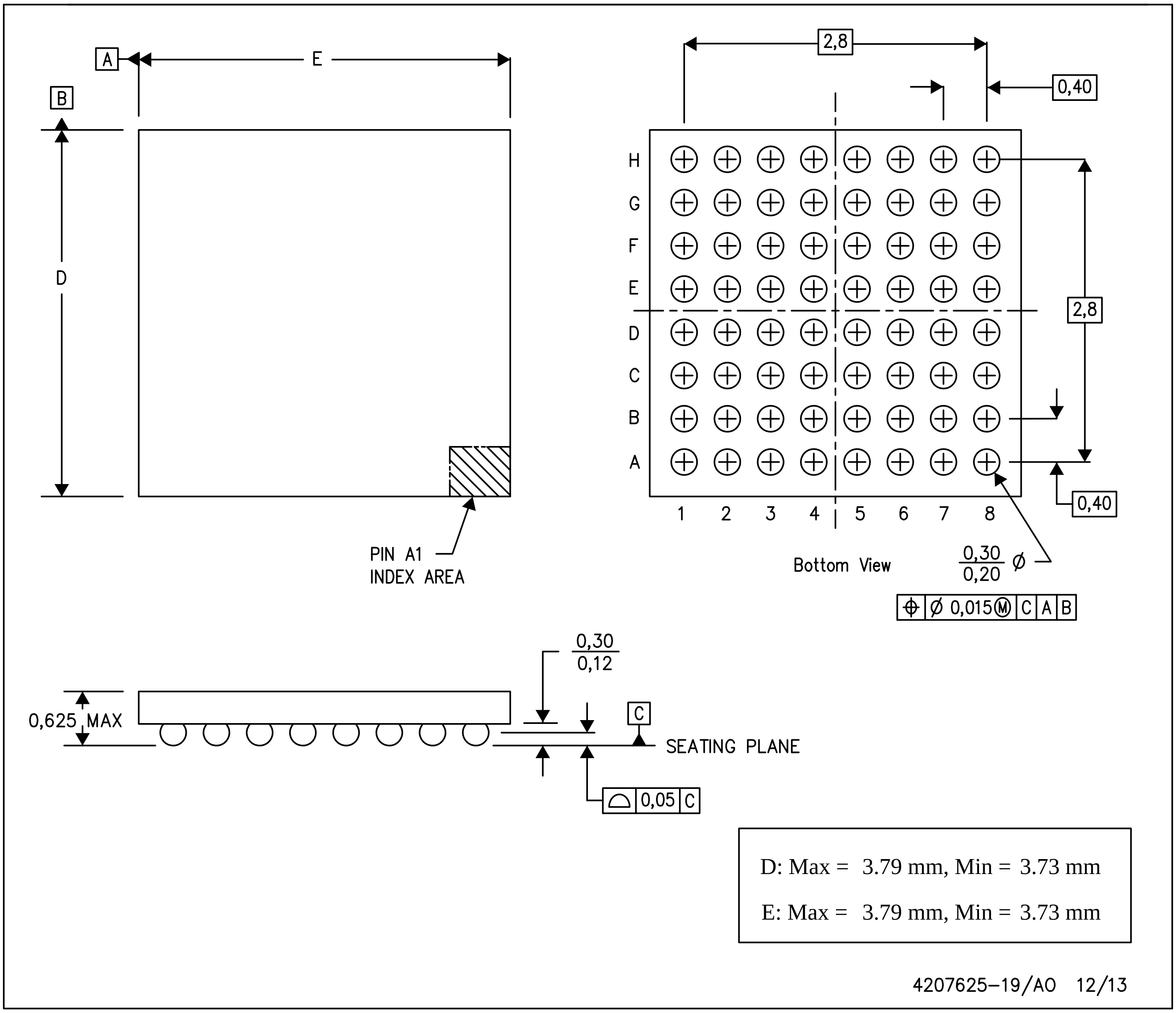
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**


0,50
0,27
0,17
0,08 M
60
41
61
40
80
21
1
20
9,50 TYP
12,20
11,80
SQ
14,20
13,80
SQ
0,13 NOM
Gage Plane
0,25
0,05 MIN
0°–7°
0,75
0,45
1,45
1,35
Seating Plane
1,60 MAX
0,08
4040135 / B 11/96

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

YFF (R-XBGA-N64) DIE-SIZE BALL GRID ARRAY


A
B
E
D
PIN A1
INDEX AREA
2,8
0,40
H
G
F
E
D
C
B
A
1 2 3 4 5 6 7 8
2,8
0,40
Bottom View
0,30
0,20 Ø
⌖ Ø 0,015Ⓜ C A B
0,30
0,12
0,625 MAX
C
SEATING PLANE
⌓ 0,05 C
4207625-19/A0 12/13

D: Max = 3.79 mm, Min = 3.73 mm

E: Max = 3.79 mm, Min = 3.73 mm

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司