IoT Security Project

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SENIOR DESIGN

FALL 2018

Abstract

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1 Introduction

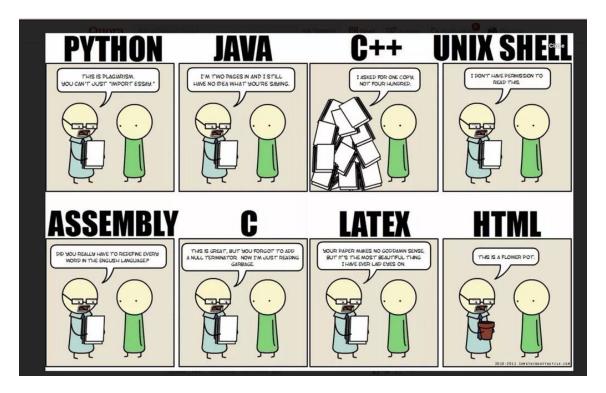


Figure 1: Insert caption here. © Google, 2017.

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1.1 Subsection

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Example Table:

1.1.1 Subsubsection

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2 Appendix

2.1 Design Synthesis and Analysis

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2.2 Source Code

2.2.1 top module

```
module top module (input logic N64 data,
                    input logic remote data,
                    input logic [7:0] buttons,
                    \begin{array}{ll} \textbf{input} & \texttt{logic} & \texttt{nes\_clk} \;, \; \texttt{snes\_clk} \;, \; \texttt{n64\_clk} \;, \\ \textbf{input} & \texttt{logic} & \texttt{NES\_latch} \;, \; \texttt{SNES\_latch} \;, \end{array}
                    input logic nes_reset, snes_reset,
                      input logic remote_reset,
                    input logic reset_n, //reset for clock_counter_1MHz
input logic [1:0] controller_select,
                    input logic console_select
                    output logic nes_output [7:0] //nes controller output data line
                    output logic snes output [11:0]
       );
       logic nes_data_bus;
       logic clk_bus;
logic clk_4M;
       logic clk 1M;
       logic remote selection; //12-bit data line from controller MUX to console
    DEMUX
       logic [7:0] N64_state_bus;
       logic [11:0] to_NES_12;
       logic [7:0] to \overline{NES} 8;
       logic [11:0] to SNES;
       logic [11:0] to_active_controller;
       assign to NES 8 = \text{to NES } 12[7:0];
        //TODO:
       //4 modules
        //Instance of built in module to select 4.29MHz clock
       OSCH #("4.29") osc int (
          .STDBY(1'b0), //\overline{S} pecifies active state
          .OSC(clk\_4M)\,, //Output 4.29MHz to clk_4M net
          .SEDSTDBY()); //Leaves SEDSTDBY pin unconnected
       //Instantiation of 1MHz clock divider (4MHz input, 1MHz output)
       clock_counter_1MHz clk_divider(
          .clk 4MHz(clk 4M),
          . reset_n(reset_n),
.clk_1MHz(clk_1M));
       //Active Controller selector (MUX)
       active controller (
          .remote_data(to_active_controller), //8-bit raw remote data input
```

```
.\,N64\_data(N64\_state\_bus)\,,\ //8-bit\ raw\ N64\ data\ input
             .button_data(buttons), //8-bit raw button input
.select_bits(controller_select), //2-bit data input
.selection(remote_selection) //Output 12-bit selection
        );
        //Active Console selector (DEMUX)
        active_console console_select(
          . controller_selection(remote_selection),
                   .select_bit(console_select), //Bit to select console .NES_console(to_NES_12), //12-bit data output
                           . SNES console (to SNES) //12-bit data output
        );
        shift_register_PISO_8bit NES(
          . clk (nes_clk),
          . reset ( nes _ reset ) ,
. load (NES _ latch) ,
          data (to NES 8),
          . sout (nes_output)
        {\tt shift\_register\_PISO\_12bit~SNES(}
           .clk(snes_clk),
          . reset (snes_reset),
.load (SNES_latch),
          data (to SNES),
           .sout(snes_output)
        );
        //N64 Controller Reader
        n64_button_reader N64_C(
                .clk_4M(clk_4M),
.clk_1M(clk_1M),
                .n64 data (\overline{N}64 data),
                .n64_button_state(N64_state_bus),
                .n64_controller_clk(n64_clk)
          );
        //Remote Reader
        remote_translator IR_translator(
          . serial_from_IR(remote_data),
. OneMHz_clock(clk_1M),
          . reset (remote_reset) ,
          .to_NES_shift_register(to_active_controler)
        );
endmodule
                                          ./source/top module.sv
```

2.3 Subsection

Source code listing

References

- [1] J. Doe and J. Doe, "Title." http://www.google.com, 2013.
- [2] Author, "Title2." http://www.yahoo.com, 2012.