Noise Limits of CMOS Current Interfaces for Biosensors: A Review

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***Abstract*—Current sensing readout is one of the most frequent techniques used in biosensing due to the charge-transfer phenomena occurring at solid-liquid interfaces. The development of novel nanodevices for biosensing determines new challenges for electronic interface design based on current sensing, especially when compact and efficient arrays need to be organized, such as in recent trends of rapid label-free electronic detection of DNA synthesis. This paper will review the basic noise limitations of current sensing interfaces with particular emphasis on integrated CMOS technology. Starting from the basic theory, the paper presents, investigates and compares charge-sensitive amplifier architectures used in both continuous-time and discrete-time approaches, along with their design trade-offs involving noise floor, sensitivity to stray capacitance and bandwidth. The ultimate goal of this review is providing analog designers with helpful design rules and analytical tools. Also, in order to present a comprehensive overview of the state-of-the-art, the most relevant papers recently appeared in the literature about this topic are discussed and compared.**

***Index Terms*—Biosensors, current amplifiers, noise, sensor interfaces.**

I. Introduction

CURRENT readout is a well-known technique widely used in electronic sensors such as radiation detectors, impedance spectroscopy interfaces and mechanical sensors. In the upcoming era of biosensors, new opportunities are emerging in that field and new challenges are focusing electronic design attention on miniaturization and array arrangement issues especially. More specifically, current sensing is becoming one of the most useful readout techniques for detecting signals from bio-nanosensors, which include: 1) ion channels [1]; 2) solid-state nanopores [2]; 3) silicon nanowires [3] and 4) carbon nanotubes [4]. Additionally, current sensing plays a fundamental role in electrochemical impedance spectroscopy (EIS) which is a technique currently used for studying a large variety of electrochemical phenomena over a wide frequency range, as well as being recently used for biosensor applications [5]–[7].

The most critical current signals in biosensing applications are in the order of pA and in the kHz bandwidth. This means that very low-noise electronic interfaces are required, with an input-referred root mean square (r.m.s.) noise as low as hundreds of fA in the kHz bandwidth. The benchmark instrument for current sensing in electrophysiology is the Axon Axopatch 200B [8], which achieves a noise floor as low as 25 fA r.m.s. at 1 kHz (0.7 $\mathrm{fA}/\sqrt{\mathrm{Hz}}$ until 1 kHz). However, it is a bulky and expensive instrument intended for electrophysiology laboratories and experienced users.

Integrated circuit (IC) miniaturization offers a unique opportunity to shrink complex current-sensing architectures into silicon chips, whose main benefits are: 1) lowering the noise due to reduction of stray and interconnection capacitances so as to achieve performances comparable with laboratory instruments; and 2) the possibility of arranging readout structures into compact arrays with applications in high throughput biosensing and chemical sensing as well as in point-of-care applications. Thus, CMOS integration of current sensing arrays is becoming a strategic technology when it comes to realizing low-noise, high-parallel and cost-effective current-sensing interfaces for bio-nanosensor applications such as those proposed for rapid label-free electronic detection of DNA synthesis [9], [10].

This paper analyzes and derives noise limits and design trade-offs which characterize the best-performing architectures and reviews the state of the art in the field of low-noise, integrated current-sensing interfaces based on CMOS technology. Although the focus is on the noise performance of the front-end amplifier, it must be mentioned that in order to increase the sensitivity and reliability of bio-nanosensors, alternative approaches can be concurrently adopted such as error-correcting bio-circuits [11], [12].

In Section II the most relevant bio-nanosensors recently appeared in the literature will be reviewed, highlighting their noise properties and detection requirements. For a deeper analysis about effects of sensor impedance on the electronic noise, please refer to [13]. Section III will introduce the basic theory of current amplifiers, which will be used to analyze the noise performance of circuits based on continuous time (CT) architectures (illustrated in Section IV), and for discrete time (DT) approaches (Section V). Finally, Section VI reviews and compares state-of-the-art performance of both solutions.

Manuscript received November 24, 2012; revised March 02, 2013; accepted April 20, 2013. Date of publication June 21, 2013; date of current version May 23, 2014. The research leading to these results received funding from the EC Seventh Framework Programme (FP7/2007-2013) under grant agreements NANOFUNCTION (257375) and ENIAC END (120214). This paper was recommended by Associate Editor S. Chakrabartty.

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Digital Object Identifier 10.1109/TBCAS.2013.2262998

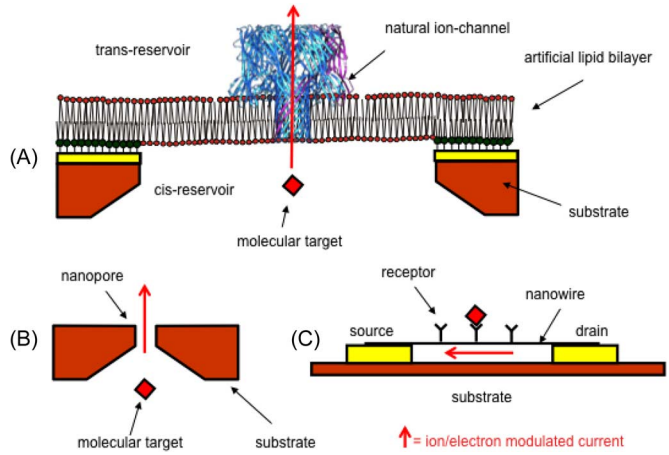

Fig. 1. Current-based biosensors. (a) Biological nanopores embedded in BLMs allow ionic current to pass between two reservoirs and be modulated by molecular interactions. (b) Artificial nanopores acting similarly to previous ones. (c) Nanowires and nanotubes where the current flowing through them is modulated by the binding interactions between target molecules and a functionalized surface.

II. Bio-Nanosensors

Pioneering work on current recording started decades ago with the advent of electrophysiology science demonstrating current recordings on single-ion channels through cell membranes using the patch-clamp technique [14]. In these experiments, a voltage clamp is applied across a membrane hosting one or more ion channels so as to monitor the ionic current flowing through the pore. An alternative technique for single ion channel recordings is based on embedding transmembrane proteins in artificial lipid bilayer membranes (BLM) [Fig. 1(a)] [15]. Recent advances on hybrid technologies have made available BLM arrays using microfabricated devices coupled with CMOS technology [16]. The envisioned application of BLMs is to high throughput screening (HTS) [17], [18], which is gaining a crucial role in screening drugs and medical compounds, and ultimately in ensuring consumer safety [19]. Lately, nanopore sensors have attracted considerable scientific and commercial interest as a direct means of sensing individual nucleic acids for DNA sequencing [20]–[22].

Even if biological pores have proven to be very useful for a wide range of interesting translocation experiments, they do exhibit a number of disadvantages such as fixed size and limited stability [21], [23]. Recent advances in fabricating membranes containing a single nanopore [Fig. 1(b)] have envisioned novel applications thanks to their ability to replace natural ion-channels [24].

An alternative way to selectively sense molecules is by means of nanowire devices [Fig. 1(c)], which are characterized by an exceptionally large surface to volume ratio and present new challenging opportunities for biomolecular sensing. The current flowing through the nanowire is strongly modulated by the surface charge given by its functionalization [25]. It has been shown that detection of protein biomarkers is possible over a wide dynamic range and down to physiological concentrations with as much selectivity and sensitivity as the state-of-the-art approaches used in clinical laboratories [26]–[28]. Very similar to nanowires, nanotubes could be used for biosensing [29]. Recently, new CMOS interfaces have been proposed for nanotube biosensing based on resistive sensing [30].

TABLE I
Summary of Bio-Nanosensor Parameters and Requirements

SENSOR TYPE	SENSOR NOISE FLOOR	SENSOR BANDWIDTH	SENSOR IMPEDANCE
Ion Channels [33]	≤6fA/√Hz	1 –100kHz	10 – 100GΩ
Solid-state Nanopores [34]	6fA/√Hz	10 – 20MHz	100MΩ – 5GΩ
Si Nanowires [27]	≥150fA/√Hz	10 – 20kHz	100k – 100MΩ
C Nanotubes [28]	10-20pA/√Hz	10 – 100kHz	100k – 20MΩ

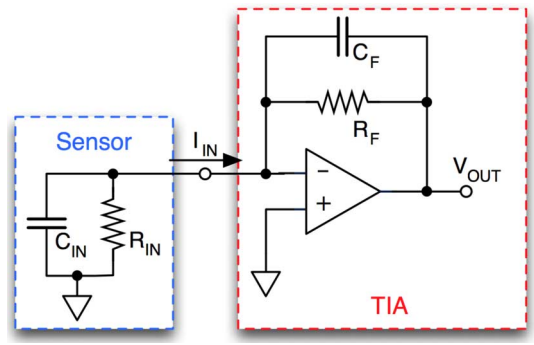

Fig. 2. Transimpedance amplifier coupled with the simplest equivalent model for a biosensor. More accurate biosensor models are described in [13].

Depending on both the application and the biosensor type, current interfaces should cope with various different requirements. Ion channels are characterized by low-noise, moderate bandwidth and high output impedance [13], [31], [32]. For instance, sodium ion channels have a typical conductance of approximately 100 pS, resulting in current in the order of 10 pA when driven with 100 mV [14], and r.m.s. noise level smaller than 0.1 pA at 1 kHz [33]. Solid-state nanopores show high intrinsic impedance and are among the most demanding devices for their signal bandwidth [34]. Silicon nanowires, as well as carbon nanotubes, are subject to great variance as regards their typical impedance because they are closely dependent on technology and realization processes [35]–[37]. Finally, carbon nanotubes are among the noisiest sensors, suffering from high flicker noise [29], [38]. Table I summarizes typical values for noise, bandwidth and output impedance among the bio-nanosensors referred to in this paper. Following, for the sake of simplicity we will model the biosensor with a capacitor and a resistor connected in parallel (Fig. 2). For a more accurate and general model of the sensor please refer to [13], where sensor effects on measurements and noise level are thoroughly addressed.

III. CMOS Current Amplifiers Basic Architectures

A. The Transimpedance Amplifier

The foremost classic current readout scheme is based on the transimpedance amplifier (TIA) shown in Fig. 2. It is a cur-

rent-to-voltage converter based on a resistive feedback operational amplifier (opamp) whose output voltage is given by

$$v_{OUT} = R_F \cdot i_{IN} \tag{1}$$

where R_F is the feedback resistance and i_{IN} is the input current [39]. To cope with extremely low currents the feedback resistance should be very high. For instance, assuming a full-scale output of 1 V, 1 GΩ resistance is needed to read 1 nA full-scale input current. Although high resistors are on the market, integrating them into a CMOS silicon chip is very challenging. Moreover, discrete resistors have unavoidable stray shunt capacitance (C_F) limiting the bandwidth according to the transfer function

$$v_{OUT} = -\frac{R_F}{1 + j2\pi f R_F C_F} i_{IN}. \tag{2}$$

As will be shown in the next section, feedback resistance contributes significantly in terms of noise; hence, basic TIA scheme suffers from a pronounced trade-off between noise and bandwidth.

B. Noise in Current-Sensing Interfaces

Since bio-nanosensor and electronic readout are uncorrelated noise sources, a current-sensing system shows an input-referred noise power $\overline{i_{IN}^2}$ given by

$$\overline{i_{IN}^2} = \overline{i_D^2} + \overline{i_N^2} \tag{3}$$

where $\overline{i_D^2}$ is the noise power spectrum density relating to the nanodevice, usually composed of both thermal and flicker components, and $\overline{i_N^2}$ is the noise PSD relating to the electronic interface.

As shown in Fig. 3 the feedback resistor noise $\overline{i_R^2}$ and the input current noise generator $\overline{i_{n-op}^2}$ of the opamp can be directly referred to the input as $\overline{i_{N1}^2}$, the expression for which is

$$\overline{i_{N1}^2} = \overline{i_R^2} + \overline{i_{n-op}^2} = \frac{4kT}{R_F} + 2qI_{IN} \tag{4}$$

where k is the Boltzmann constant, T is the temperature in Kelvin degrees and $2qI_{IN}$ is the shot noise of the input devices, where applicable. The output noise PSD due to $\overline{e_{n-op}^2}$ can be expressed as

$$\begin{aligned}\overline{v_{on}^2} &= \overline{e_{n-op}^2}\left|1+\frac{Z_F}{Z_{IN}}\right|^2 \\ &= \overline{e_{n-op}^2}\frac{(R_{IN}+R_F)^2+4\pi^2 f^2 R_F^2 R_{IN}^2 (C_F+C_{IN})^2}{R_{IN}^2\,(1+4\pi^2 f^2 R_F^2 C_F^2)}\end{aligned} \tag{5}$$

where Z_F is the feedback impedance and Z_{IN} is the sensor impedance. Equation (5) shows the relationship of the input impedance to the noise, leading to the following considerations: a) at a low frequency regime, the output noise is related to resistances ratio, minimized for high R_{IN}; and b) at a high frequency regime, the noise is related to capacitances ratio, minimized for low C_{IN}. As illustrated in Table I, the majority of bio-nanosensors offers a high output resistance, so we can approximate (5) by:

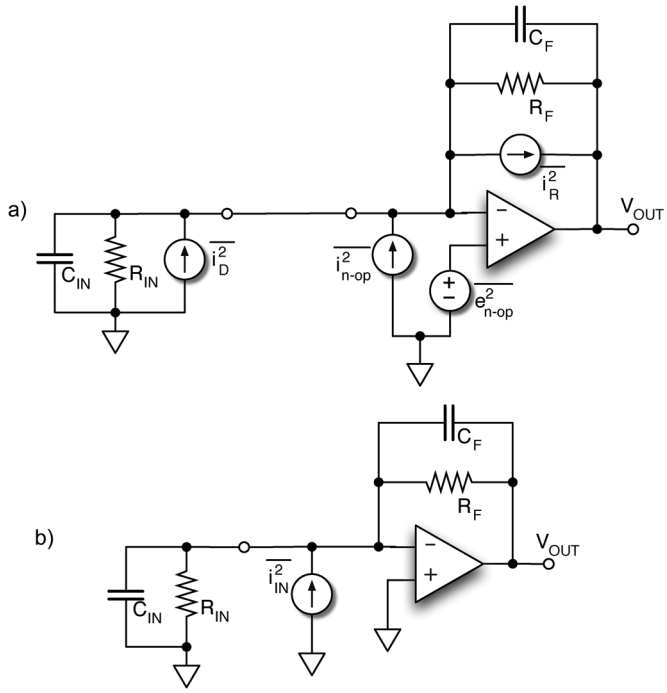

Fig. 3. (a) Noise sources of the TIA. $\overline{i_D^2}$ is the equivalent noise current generator of the DUT, $\overline{i_{n-op}^2}$ and $\overline{e_{n-op}^2}$ represent the noise generators of the opamp and $\overline{i_R^2}$ is the equivalent noise current generator of the feedback resistor. (b) Equivalent input-referred noise current generator $\overline{i_{IN}^2}$ taking into account all the noise sources.

$$\overline{v_{on}^2} = \overline{e_{n-op}^2}\frac{1 + 4\pi^2 f^2 R_F^2 (C_F + C_{IN})^2}{(1 + 4\pi^2 f^2 R_F^2 C_F^2)}. \tag{6}$$

In the following sections we will always ignore R_{IN}, since it has no effect on our analysis or argument. In cases where the sensor resistance cannot be ignored, (5) is used instead of (6). Now, dividing (6) by the square of the TIA transfer function (2), we get the input-referred noise relating to $\overline{e_{n-op}^2}$

$$\overline{i_{N2}^2} = \overline{e_{n-op}^2}\left[\frac{1}{R_F^2} + (2\pi f)^2 (C_F + C_{IN})^2\right]. \tag{7}$$

Thus, the total input-referred noise power spectral density(PSD) of the TIA is given by the sum of (4) and (7)

$$\overline{i_N^2} = 2qI_{IN} + \frac{4kT}{R_F} + \overline{e_{n-op}^2}\left[\frac{1}{R_F^2} + (2\pi f)2(C_F + C_{IN})^2\right] \tag{8}$$

where C_{IN} takes care of both sensor output capacitance and stray capacitance placed on the input node of the electronic interface. Thus, the input-referred noise PSD of the interface is given by the sum of three terms. The first one takes into account, where applicable, the shot noise of the input devices such as BJT or JFET transistors. The second one relates to current noise of

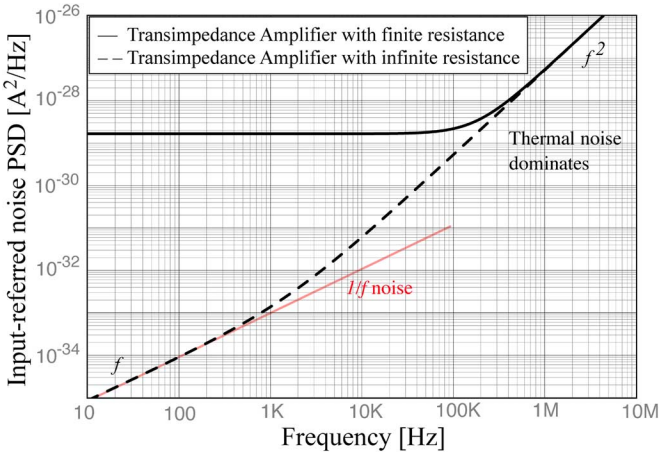

Fig. 4. Input-referred noise power spectrum for standard TIA with finite feedback resistance $R_F = 1\ \mathrm{G\Omega}$ (solid line) and infinite feedback resistance, which is also known as CSA(dashed line). The graph refers to a low-noise custom opamp described by a thermal noise voltage of approximately $3\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ and $C_F + C_{IN} = 1.2\ \mathrm{pF}$.

the feedback resistor, which hinges on the fact that a high resistance value is required for low-noise performance. Finally, the third term relates to the opamp voltage noise source and expresses the dependency on sensor impedance.

CMOS technology offers the advantage of a negligible shot noise term at the expense of greater contributions of low-frequency noise than BJT and JFET. More specifically, the expression for input-referred noise voltage power in a CMOS opamp is

$$\overline{e_{n-op}^2} = \frac{16kT}{g_m} + \frac{2K_F}{C_{OX}WL} \cdot \frac{1}{f} \tag{9}$$

where g_m is the transconductance of the MOS input pair, W and L are width and length of a single input device, K_F is the flicker noise coefficient and C_{OX} is the oxide capacitance per unit area [40], [41].

As is well known, BJT and JFET devices offer better noise performance than MOS ones due to their higher transconductance and lower flicker coefficient on expenses of power dissipation. However, CMOS technology shows unique advantages when it comes to implementing low-cost low-power autonomous systems and mixed-signal dense arrays.

C. Integrator-Differentiator Scheme

Assuming a CMOS realization for the TIA, the input-referred noise PSD becomes

$$\overline{i_N^2} = \frac{4kT}{R_F} + \overline{e_{n-op}^2}\left[\frac{1}{R_F^2} + (2\pi f)^2(C_F + C_{IN})^2\right]. \tag{10}$$

This equation shows a low frequency noise floor set by R_F (in this white plateau $4kT/R_F$ dominates with respect to $\overline{e_{n-op}^2}/R_F^2$) and then an asymptotic noise increase, weighted by the total capacitance connected to the input node $C_F + C_{IN}$, for frequencies greater than the corner point given by (10) (Fig. 4). Clearly, the total noise power will decrease for higher R_F, reaching a minimum with an infinite feedback resistance. Thus,

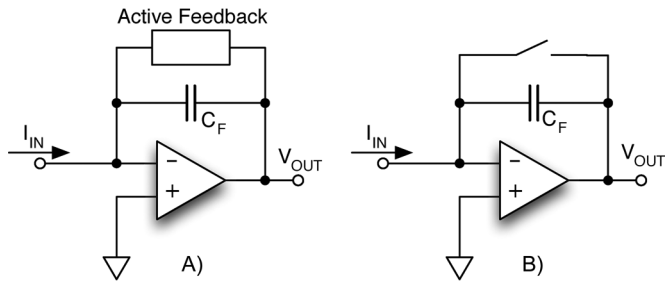

Fig. 5. Implementations of a transimpedance amplifier based on a charge-sensitive amplifier. (a) CT approach using active feedback. (b) DT approach using periodic reset.

it is apparent that replacing R_F with a noise-free capacitor C_F represents the optimum choice from the noise standpoint.

With this kind of substitution, the TIA behaves as a charge-sensitive amplifier (CSA) in which the output voltage is equal to the integral of the input current. As represented in Fig. 4, in this case the input-referred current noise PSD shows two rising slopes corresponding to the two terms of $\overline{e_{n-op}^2}$ reported in (9) and multiplied by f^2. Thus, at low frequency, the 1/f noise results in a power spectrum rising with f, while for higher frequencies, the white term is dominant and rises with a double slope f^2.

Equation (10) shows how to improve the signal-to-noise ratio:

1) Avoid feedback resistance in favor of charge-sensing approaches.
2) Reduce input capacitance as much as possible.

In any case, (10) demonstrates that miniaturization of the electronic interface and related routing has a dramatic impact on the noise reduction, due to C_{IN} decreasing. Miniaturization of the system also has a great effect on the nanosensor noise [42]. For instance, noise generated by nanopore devices can be modeled as current noise generated by resistor, in first approximation. Hence, smaller pore translates in higher resistance and lower noise [42].

The above-cited features indicate CSA as the best solution for low-noise current sensing, regardless of the technology employed. However CSA suffers from saturation because it integrates the current over time. To cope with that issue two techniques have been developed:

1) A continuous-time approach using low-noise active devices in place of resistors to set the bias point [Fig. 5(a)].
2) A discrete-time approach implemented by resetting the charge stored in the feedback capacitance [Fig. 5(b)].

These approaches have a lower input-referred noise PSD than the TIA scheme, but they still introduce deviations from ideal CSA behavior, such as insufficient reduction of noise floor in the former case, or charge injection and kTC noise in the latter. In both cases the output voltage is proportional to the integral of the input current and thus a subsequent derivation step is needed so as to recover the signal. That architecture, usually known as an integrator-differentiator scheme, also allows us to ignore the flicker noise of the first opamp thanks to differentiation of the noise spectrum performed by the second stage that reduces its impact at low frequency. This effect is shown in Fig. 6, in

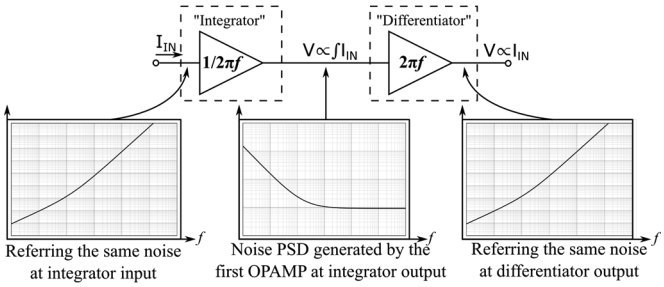

Fig. 6. Noise generated by the first opamp shows different PSD shapes with respect to the node which is referred to.

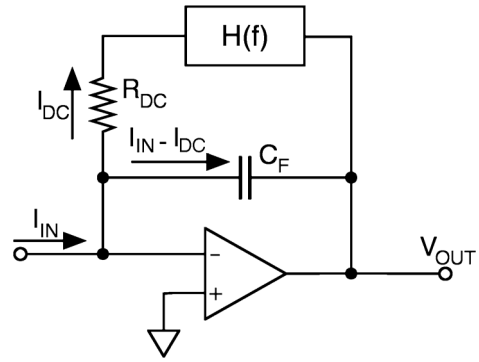

Fig. 7. Circuit diagram of the CT current-sensing scheme presented in [46].

which the propagation of the noise spectrum through the system is illustrated.

As the global transfer function between the differentiator output voltage and the input current is flat (as long as the differentiator loop gain is >1) the output noise spectrum is characterized by the same shape of the input with two rising slopes. Moreover, the integration-differentiation approach eliminates the noise-bandwidth trade-off typical of TIA. More specifically, the first pole of differentiator stage fixes the maximum acquisition bandwidth [43].

IV. Continuous-Time Approach

A. Resistive Feedback

The continuous-time approach is based on an integrator-differentiator scheme with a continuous-time feedback technique setting the bias point and coping with the amplifier saturation issue. A first approach could be to use a large feedback resistance, referring back to the TIA scheme. A recent paper [43] shows how input-referred noise as low as 1.9 $\mathrm{fA}/\sqrt{\mathrm{Hz}}$ up to several hundred hertz could be achieved with bipolar technologies even using discrete components. However, the large value resistor required is not well suited to VLSI implementation as needed by a nanosensor array.

A more interesting architecture using the classic TIA approach is presented in [44], where an integrated patch-clamp system is proposed. The resistor integration problem was solved by using a silicon-on-insulator (SOI) technology, which enables high feedback resistances to be implemented with reduced parasitic capacitances, lowering the input-referred noise floor down to 5 pA r.m.s. in the 10 kHz bandwidth ($50\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$). However, SOI technology is not frequently used in analog design and could be expensive.

B. Active Feedback

An interesting solution for current interfaces employing CSA in CT approach is presented in [45] and [46], where a low-noise active feedback taps out the input DC current to prevent opamp saturation. A simplified scheme of this approach is shown in Fig. 7. The amplifier $H(f)$ in the active feedback is characterized by very high gain at very-low frequencies and high attenuation at higher frequencies. In this way, the feedback is strong enough to redirect the input DC current into R_{DC} while not affecting the upper limit of the bandwidth, as the feedback is deactivated at higher frequencies.

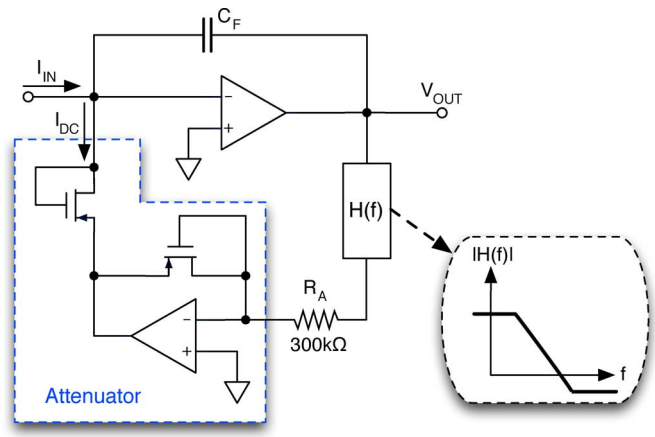

Fig. 8. Resistance R_{DC} of Fig. 7 is implemented using a physical resistor $R_A = 300$ kΩ combined with an active bidirectional attenuator that reduces the current by a factor $A = 150$ [45], [47].

The main concern in the design of this current interface is the stability of this additional $R_{DC} - H(f)$ feedback loop. In fact, since there are two low-frequency poles, one due to the integrator and one added by $H(f)$, a zero should be placed after the pole but before the frequency f_m for which the loop gain is unitary. Frequency f_m is set by the position of the singularities of $H(f)$ and represents the maximum frequency for which this DC-canceling loop is active, i.e., the lower limit of the amplification bandwidth. Since the order of the slope between the pole and the zero has no particular impact on the dynamic performance, a first order has been usually implemented. However, higher-order slopes, though increasing the complexity, would allow placing the poles closer to the zeros. Thus, given a fixed target f_m at low frequency (1–100 Hz), this would allow placing the poles of $H(f)$ at higher frequencies, relaxing the difficulty to synthesize such a large time constant.

From the noise standpoint, the impact of the additional noise introduced by $H(f)$ is made negligible thanks to the high value of R_{DC}. Furthermore, as in this scheme the dominant noise contribution of $H(f)$ is the thermal noise due to R_{DC}, the value of this resistor should be maximized. Thus, R_{DC} is actually implemented by a physical resistor R_A with value suitable for integration (for instance 300 kΩ) in series with an active bidirectional attenuator based on a matched-MOS scheme, where the MOS devices work in the sub-threshold region [47] (Fig. 8). Since the attenuation factor A is 150, the equivalent R_{DC} is 45 MΩ

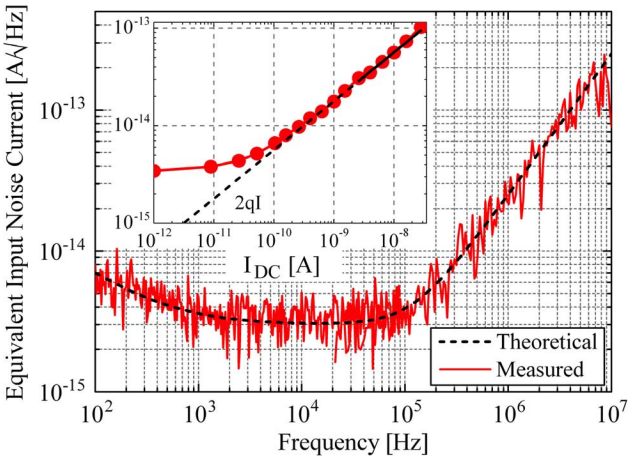

Fig. 9. Measured input-referred current noise for the CT integrator-differentiator amplifier described in ref. [45] matches with the theoretical expectation, calculated by means of eq. (11) for the case of $\mathrm{en} = 3\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, low DC input current (below 10 pA) and small external capacitance (below 2 pF). Flicker noise generated by the active feedback has been taken into account. The increase of the value of the current noise PSD (flat middle-frequency region) with increasing levels of DC input current I_{DC} is also reported in the inset, in excellent agreement with the theoretical estimate of noise increase due to the shot noise of the active attenuator transistors (dashed line).

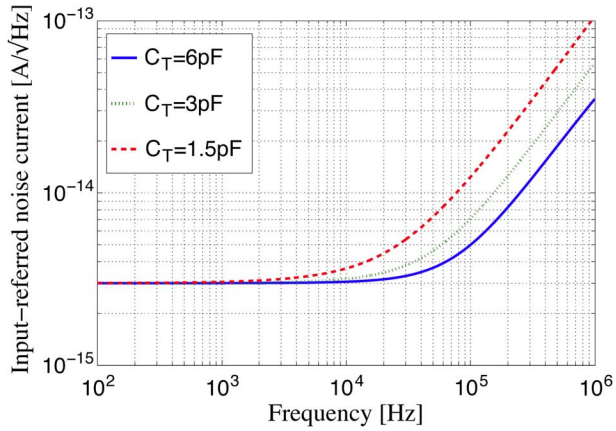

Fig. 10. Simulation of input-referred noise current of the system presented in [46] for various input capacitances. The simulation has been done using the same circuit parameters described in [46], where $C_F = 100$ fF and $R_A = 300$ kΩ. The active feedback has been realized using ideal opamps, thus the flicker noise generated by the active feedback is not shown in the picture.

providing a maximum range for the DC current of ±25 nA. The resulting input-referred noise can be estimated as

$$\overline{i_N^2} = \frac{4kT}{A^2 \cdot R_A} + \overline{i_{MOS}^2} + (2\pi f)^2 (C_F + C_{IN})^2 \cdot \overline{e_{n-op}^2}. \quad (11)$$

The first term in (11) describes the thermal noise physically generated by R_A that is divided by the attenuator scheme. The second term, $\overline{i_{MOS}^2}$ is the shot noise generated by diode-connected MOSes working in sub-threshold regime in the attenuator scheme. This shot noise is negligible for low input currents, while it comes into play for rather high input current depending on the value of the equivalent resistance R_{DC}, limiting the signal-to-noise ratio (SNR) at the full-scale (see inset of Fig. 9). In this case the shot noise term is negligible with respect to the thermal noise of R_A for input current lower than 10 pA. The third term is different from the second one in (10), although they both describe the noise created by the opamp. The effectiveness of the noise model of (11) is experimentally verified as reported in the measurement results shown in Fig. 9. Note that the flicker noise generated by the active feedback—responsible for the slight noise raise observed at low frequency—has been ignored in (11). However, it should be taken into care inside the second term. Indeed, this noise component is outside the integration path, thus it is directly referred to the input as $1/f$ noise, significantly increasing the noise floor signal at low frequencies.

Substituting (9) in (11)the input-referred noise PSD becomes

$$\begin{aligned}\overline{i_N^2} &= \overline{i_{MOS}^2} + 4kT\left(\frac{1}{R_{DC}} + \frac{4}{3}\frac{(2\pi f)^2 (C_F + C_{IN})^2}{g_m}\right) \\ &\quad + \frac{8\pi^2 K_F}{C}(C_F + C_{IN})^2 \cdot f = \\ &\approx \overline{i_{MOS}^2} + \frac{4kT}{R_{DC}} + \frac{16kT}{3}\frac{(C_F + C_{IN})^2}{g_m}(2\pi f)^2 \end{aligned} \quad (12)$$

where the last term in the first line relates to flicker noise of the opamp, which is directly proportional to the frequency. Hence, the flicker term is negligible with respect to thermal noise. The input-referred noise PSD given by (12) shows a flat behavior at low frequency and a quadratic asymptotical increase at high frequency beyond a corner point. This PSD behavior is very similar to TIA behavior: both have a noise floor strictly related to the value of the equivalent feedback resistance R_{DC}, resulting in one of the main limitations of the CT approach (Fig. 10).

The last term in the second line of (12) is dependent on the transconductance g_m and on the total capacitance $C_T = C_F + C_{IN}$ facing the input node, where C_F is the feedback capacitance and C_{IN} is the sum of the sensor output and input stray capacitance. The above terms set the corner frequency between flat and asymptotic f^2 behavior. Increasing C_T decreases the corner frequency, as shown in Fig. 10, resulting in a reduction of the low-noise bandwidth (i.e., the bandwidth in which the system reaches the noise floor).Note that the input stray capacitance includes the stray capacitances of wires, pads and bonding-wires together with the opamp input capacitance, which is mainly given by C_{GS}. This last capacitance produces a trade-off in noise optimization since it acts twice in (12), both on C_T and on g_m. For instance, a low C_{GS} will reduce C_{IN} and thus the noise; however, it requires smaller input devices for the opamp and thus a smaller transconductance g_m, which increases the noise power. That means there is an optimum value for C_{GS}, which minimizes the input-referred noise power [48]. By substituting the expression of $g_m = 2\sqrt{kI}$ in (12) and evaluating the differentiated function considering a constant bias current (i.e., constant power dissipation), we get as the optimum value

$$C_{GS-OPT} = \frac{C_{IN} + C_F}{3}. \quad (13)$$

The above analysis on CT approaches employing active feedback proves the advantage of miniaturization process on noise performance. A low input capacitance C_{IN} reduces the input-referred noise of the electronic interface, as stated by (12), and allows the use of smaller input transistors, reducing

the power consumption. Indeed, the possibility to deactivate the resistive feedback at high frequencies, combined with the integrator-differentiator scheme, unleashes the noise-bandwidth trade-off typical of classic TIA scheme. However, if very large signal bandwidth is targeted, shunt stray capacitance, though small, becomes critical also in CMOS implementations. In fact, the synthesis of large resistance by means of active solutions, though beneficial from both area and noise standpoints, is anyhow affected by the presence of dominant time constant. If 1 MHz bandwidth is desired and 1 GΩ resistor is implemented, then the maximum shunt stray capacitance is 0.16 fF. The main limitations of this approach are the need for a separate output for the acquisition of low frequency signals (<100 Hz) and the complex design required to ensure stability of the additional active feedback network. As an example, a CT integrator-differentiator CMOS current detector based on this scheme has been shown to reach a noise floor as low as $3\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$ with a corner frequency of 100 kHz and with a 100 Hz–2 MHz bandwidth [46].

An alternative approach, based on a different active feedback scheme leveraging bidirectional matched-MOS current amplification[49], provides a single output with a wide bandwidth (DC–1 MHz). Unparalleled noise performance has been achieved with 1 pF input capacitance, reaching 15 fA r.m.s. with 1 kHz bandwidth and 1 pA r.m.s with 100 kHz [50]. However, the input-referred noise becomes dominated by the shot noise of the feedback transistors when the DC current signals are larger than 50 pA (noise floor larger than $4\,\mathrm{fA}/\sqrt{\mathrm{Hz}}$). This is one of the main drawbacks of the approach: the noise depends on the signal level and for high signal values it could be higher than competitive approaches.

V. Discrete-Time Approach

A. Synchronous Reset

The discrete-time approach [51]–[59] offers several implementation advantages, since it is more suitable for interfacing with digital structures and offers less distortion than continuous-time architectures [60]. DT schemes rely on a common structure and functionality based on current integration performed over a fixed amount of time. In a standard DT current readout circuit a switch periodically resets the charge stored in the feedback capacitance C_F, thus avoiding opamp saturation. The presence of a reset period may cause the loss of input data, though this might be considered negligible if one were to minimize the reset time.

Moreover, CSA may suffer from a limited dynamic range due to the limited value of the feedback capacitance, since the final output voltage is given by the integral of the input current. To increase sensitivity without reducing bandwidth, it is mandatory to use a low capacitance in the feedback loop, implying kTC noise due to the reset switch and charge injection phenomena as major issues. To cope with these errors, correlated double sampling (CDS) has proved to be an excellent solution [51]–[53], [61]. CDS is the most frequently used technique for reset noise reduction, although other schemes can be used [62]. This manuscript includes preliminary noise analysis of CDS in discrete-time current sensing we presented in [63].

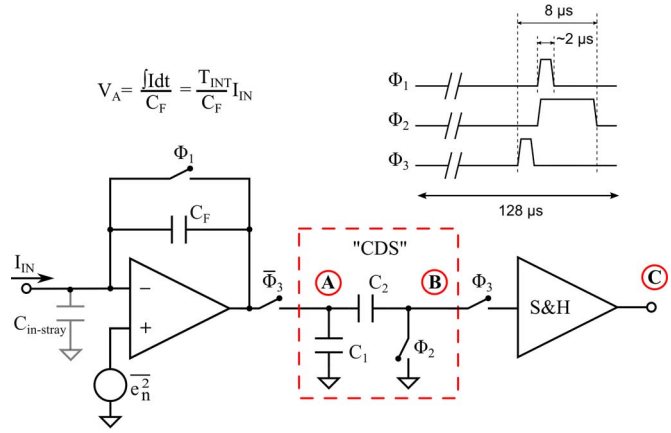

Fig. 11. DT current readout system followed by a CDS block to reduce low frequency noise and offset [52]. When Φ1 is closed the CSA is reset. Then, Φ1 and Φ3 are opened and Φ2 is closed. While Φ2 opens the CDS takes the noise sample and then starts to integrate the input current. At the end, switch Φ3 opens and the difference between the last sample and the initial noise sample is stored in the S&H. Capacitors have the values: $C_F = 100$ fF; $C_1 = C_2 = 4$ pF.

CDS is a noise and offset reduction technique based on differentiating successive samples [64]–[68]; it can thus even work as a differentiator stage. The principle is that when noise is acting in a finite bandwidth, low frequency components become correlated and can be used to cancel each other. In summary, the CDS technique is based on sampling the 'signal' twice: the first time when only noise and offset $n(T1)$ are present, and the second time when both signal and noise are present

$$\begin{aligned} v_A(T_1) &= n(T_1), \\ v_A(T_2), &= s(T_2) + n(T_2) \end{aligned} \tag{14}$$

where $s(t)$ is the informative component of the signal. Finally, CDS computes the difference between the two samples

$$v_B(T_2) = v_A(T_2) - n(T_1) \approx s(T_2). \tag{15}$$

The more the two noise samples correlate with each other, the better the output difference corresponds to the signal itself. For this reason, the CDS technique turns out to be useful in reducing low-frequency noise [64], [66]. Although CDS reduces $1/f$ noise, it results in an increase of white noise due to a folding process, and this causes a more complex expression for input-referred noise. For this reason, accurate noise modeling is necessary to understand the trade-off in the DT approach [63]. Fig. 11 shows the DT current-sensing circuit presented in [52] composed of a CSA, a CDS and a sample and hold (S&H). This scheme follows the integration-differentiator principle, since CDS acts as a differentiation stage. This circuit will be used as the reference scheme from here on. It is implemented using AMSC35 technology, where $C_{OX} = 4.5\,\mathrm{fF}/\mu\mathrm{m}^2$, $K_n = 170\ \mu\mathrm{A/V}^2$, $V_{TN} = 0.5$ V, $K_p = 58\ \mu\mathrm{A/V}^2$ *and* $V_{TP} = -0.65$ V. The operational amplifier used in the CSA of Fig. 11 is a standard folded cascode scheme, showing 86 dB of DC gain, 27 MHz of GBW and consumes 200 μA. For a complete description of the circuit, please refer to [52].

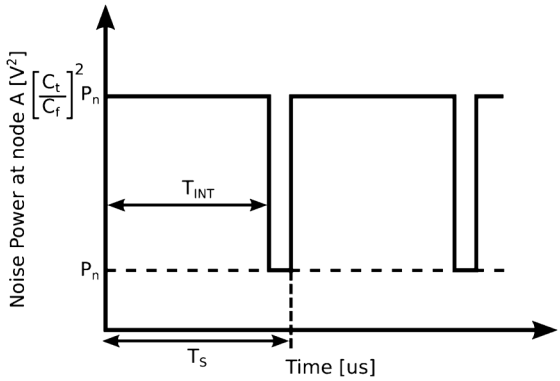

Fig. 12. Time-variant cyclostationary noise power at CSA output. It is modulated by a square wave of period T_S and alternates between $\overline{e^2_{n-op}}$ and $\overline{e^2_{n-op}} \cdot (C_T/C_F)^2$.

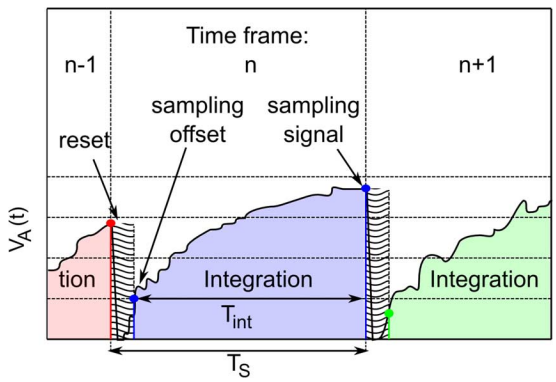

Fig. 13. CDS timing. The first noise sample is taken immediately after the end of the reset period and the second sample is performed just before the reset period.

Another interesting effect that should be taken into account is the noise modulation due to the periodic reset. When the reset switch is open, the opamp works as a non-inverting amplifier from the noise standpoint. Hence, the input noise power is approximately multiplied by the ratio C_T^2/C_F^2, where $C_T = C_F + C_{IN}$. On the other hand, when the reset switch is closed, the noise power is amplified by one. Thus, the noise voltage is multiplied by a square wave of period T_S and duty cycled d given by

$$d = \frac{T_{INT}}{T_S} \tag{16}$$

where T_{INT} is the integration period and T_S is the sampling period. In other words, the stochastic process becomes cyclostationary with time-varying statistical functions [71]. Fig. 12 illustrates the effect of noise modulation, showing the time variant noise power at the CSA output.

To mitigate this problem, a "ping-pong" scheme switching between two feedback capacitances of the same value could be used [72]. However, in our reference circuit, CDS always takes samples outside the reset frame, as shown in Fig. 13 hence it is possible to ignore the modulation effect. As a result, the noise signal could be treated as stationary.

B. Noise Modeling in DT Current-Sensing Interfaces

To calculate the minimum detectable input signal of DT schemes it is necessary to compute the input-referred current noise. However, the input-referred noise can be rigorously defined only for linear time-invariant circuits; moreover, since the sampling behavior aliases the high frequency noise components, it is not possible, either, to define a classic noise transfer function [66]. Thus, we will compute the input-referred noise dividing the output noise PSD by the square of the equivalent analog transfer function, which is the amplifier transimpedance [63]. Note that the validity of the input-referred noise computed in this way is confined to that of the amplifier transimpedance. Taking into account the circuit diagram in Fig. 11, we will assume that the circuit is working over time frames of period T_S composed of an integration period lasting T_{INT} and a reset period (Fig. 13).

The kTC noise and the charge injection, generated by the feedback capacitance C_F and the reset switch, are eliminated by CDS. Additionally, the capacitances used in CDS are made large enough for their own noise sources to be ignored (these are mainly kTC noise and charge injection). Thus, the main source of noise in the overall sensing scheme is the opamp, represented by the noise voltage generator $\overline{e^2_{n-op}}$. This is amplified and filtered by the CSA, which can be modeled as a first-order amplifier giving a noise PSD at node (A) as

$$S_A(f) = \frac{C_T^2}{(C_F + C_T/A_0)^2} \cdot \frac{1}{1 + \left(\frac{f}{f_c}\right)^2} \cdot \overline{e^2_{n-op}} \tag{17}$$

where A_0 is the open-loop gain, and f_C is the opamp closed-loop cut-off frequency.

Equation (15) clearly states that voltage $v_B(t)$ at CDS output (outside the reset) is equal to the input voltage $v_A(t)$ minus the pre-stored input sample. At time $t = 0$ the relation can be written as

$$v_B(0) = v_A(0) - v_A(-T_{INT}). \tag{18}$$

For a nonspecific time t, (18) can be generalized to

$$v_B(t) = v_A(t) - \sum_n v_A(nT_S - T_{INT}) \cdot p(t - nT_S) \tag{19}$$

where $p(t)$ is a rectangular function equal to one for $-T_{INT} < t < 0$ and zero elsewhere. Passing from the time domain to the frequency domain, and writing the noise PSD at node (B), we get [64]–[70]

$$S_B(f) \approx S_A(f)\left[1 + d^2\mathrm{sinc}^2(f \cdot T_{INT}) - 2d\mathrm{sinc}(2f \cdot T_{INT})\right] + d^2\mathrm{sinc}^2(f \cdot T_{INT}) \sum_{k \neq 0} S_A\left(f + \frac{k}{T_s}\right) \tag{20}$$

where the sinc function is defined as $\mathrm{sinc}(x) = \sin(\pi x)/\pi x$. The full math derivation of (20) is given in [73] pp. 151–159. Equation (20) recognizes two major components, both shown

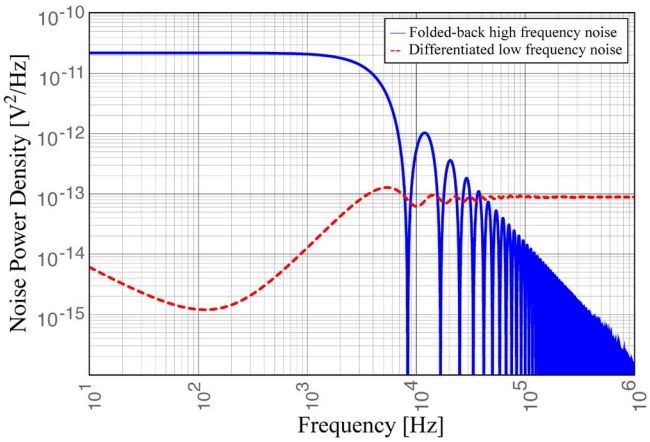

Fig. 14. Noise PSD at node (B) highlighting the components of eq. (20). The dashed red line is the differentiated noise given by the first term in (20). The solid blue line is the folded-back white noise due to undersampling by the CDS and given by the second term in (20).

in Fig. 14. The first one, shown in the upper line of (20), is differentiation of the input noise PSD. This term describes the CDS as a standard DT differentiator. For frequencies below the sampling frequency, where the correlation between samples is not negligible, the CDS differentiates the input noise, while for higher frequencies it follows the input noise [74]. As a result, the $1/f$ noise and the offset are markedly reduced [64]. Due to the non-zero reset time, the CDS is not able to completely eliminate the low frequency noise and the offset, but it mitigates them. Indeed, the first term in (20) increases at low frequencies, as shown in Fig. 14.

The last term, shown in the lower line of (20), is related to the high-frequency white noise folded back in the baseband due to the undersampling activity of the CDS. Assuming $S_A(f)$ as band-limited white noise with f_C as the -3 dB frequency, undersampling at $f_S \ll f_C$, where $f_S = 1/T_S$ is the sampling frequency, implies a process of folding the noise components (Fig. 15). Thus, the baseband noise is increased by the undersampling ratio (USR) defined as [64]

$$USR = \pi f_C T_S. \tag{21}$$

At the end of the integration period, an S&H circuit follows the CDS and stores the final result of (19). From a noise standpoint, the S&H operation performs additional noise folding and further $sinc$ shaping, so that the noise PSD at node (C) becomes

$$\begin{aligned} S_C(f) \approx & \operatorname{sinc}^2(fT_S) \\ & \cdot \{S_A(f)\left[1+d^2\operatorname{sinc}^2(fT_{INT})-2d\cdot\operatorname{sinc}(2fT_{INT})\right] \\ & +2d^2\operatorname{sinc}^2(fT_{INT})\sum_{k\neq 0} S_A\left(f+\frac{k}{T_S}\right). \end{aligned} \tag{22}$$

The folding of the flicker noise can be ignored with respect to white noise, because it is a low frequency noise [64]. Moreover,

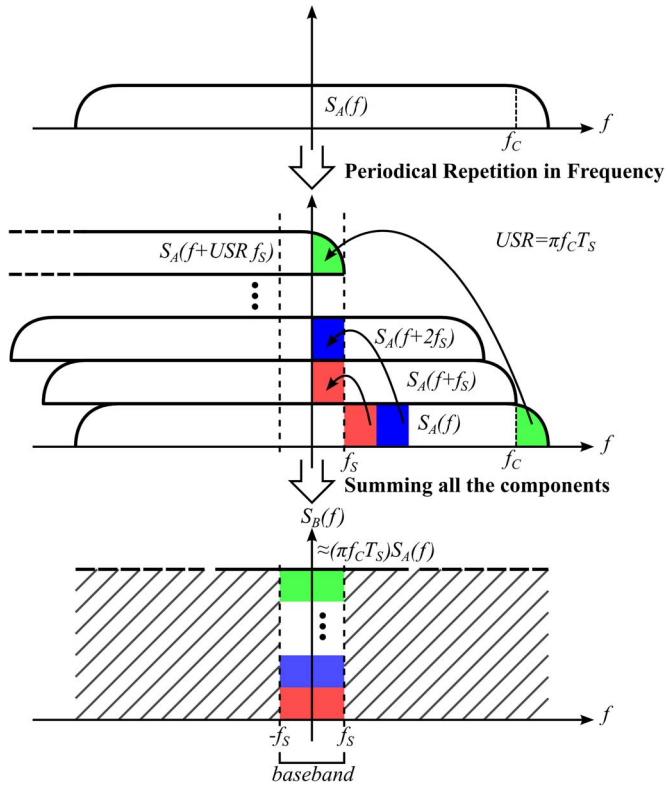

Fig. 15. Noise folding process due to undersampling. Summing all the shifted spectra results in a white noise density in the useful bandwidth USR times higher than the original one.

the undersampling factor given by (21) can be used to simplify the last term in (22) as follows:

$$d^2\sum_{k\approx 0} S_A\left(f+\frac{k}{T_S}\right) \approx d^2(\pi f_C T_S - 1)\cdot S_{A,Th}(f) \tag{23}$$

where $S_{A,Th}(f)$ is the thermal component of $S_A(f)$ [64]. Note the above approximation is valid only for frequencies below f_S. Combining (23) with (22)

$$\begin{aligned} S_c(f) \approx & \operatorname{sinc}^2(fT_S) \\ & \times\{S_A(f)\left[1+d^2\operatorname{sinc}^2(fT_{INT})-2d\operatorname{sinc}(2fT_{INT})\right] \\ & +2d^2(\pi f_c T_S-1)S_{A,Th}(f)\cdot\operatorname{sinc}^2(fT_{INT})\}. \end{aligned} \tag{24}$$

The folding process greatly increases the noise PSD, but it cannot be eliminated since the sampling frequency fS must be intrinsically lower than the opamp closed-loop cut-off frequency in order to sample the signal with the proper degree of accuracy. As shown in Fig. 14, the folding component dominates the output noise in the baseband; thus it is possible to further reduce (24) by ignoring the first term

$$S_C(f) \approx 2d^2(\pi f_C T_S - 1)S_{A,Th}(f)\cdot\operatorname{sinc}^2(fT_S). \tag{25}$$

Considering a short reset time, which implies $d \approx 1$, and applying (17) in (25) with $A_0 \gg 1$ and $f_C \gg f_S$, the output noise PSD becomes

$$S_C(f) \approx 2(\pi f_C T_S - 1) \cdot \left(\frac{C_T}{C_F}\right)^2 \cdot \overline{e^2_{n-op,Th}} \cdot \mathrm{sinc}^2(fT_S) \quad (26)$$

where $\overline{e^2_{n-op,Th}}$ is the thermal component of (9). For frequencies below f_S, CSA and CDS act on the input signal as an integrator and a differentiator, respectively, and together work as a total equivalent resistance of value

$$R_{EQ} = \frac{T_{INT}}{C_F} \approx \frac{T_S}{C_F} \quad (27)$$

where a negligible reset time has been assumed. For input signals at higher frequencies the CDS does not work as a differentiator anymore, so the signal is band-limited. Since R_{EQ} is fixed by the input full scale and C_F should be greater than a minimum value given by the technology, (27) sets the maximum acquisition bandwidth of the DT approach. For instance, using a minimum feedback capacitance of 100 fF for a full scale of about 1 nA, maximum bandwidth of few kHz could be achieved [46]. This is one of the main limitations in DT approaches as far as bandwidth is concerned. Dividing (26) by the square of (27) and assuming a USR much greater than one, we can write the input-referred noise PSD as

$$\overline{i^2_N} \approx \frac{S_C(f)}{R^2_{EQ}} \approx 2C_T^2 \cdot \frac{\pi f_C}{T_S} \cdot \overline{e^2_{n-op,Th}} \cdot \mathrm{sinc}^2(fT_S) \quad (28)$$

and for frequencies below $f_S/2$ it can be approximated to

$$\overline{i^2_N} \approx 2C_T^2 \cdot \frac{\pi f_C}{T_S} \cdot \overline{e^2_{n-op,Th}}. \quad (29)$$

From (28) and (29) it is clear that the noise floor of this circuit is set by the bandwidth of the opamp. In principle, input-referred noise benefits from reduction of f_C; however, it cannot be too small. The minimum allowed value for f_C depends on the sampling time T_S and the precision required by the application in terms of equivalent number of bits (ENOB) following the equation [75]

$$e^{-\frac{\pi f_C}{f_S}} < 2^{-(ENOB+1)}. \quad (30)$$

In order to identify design constraints, (29) could be revised introducing

$$f_C \approx GBW \cdot \frac{C_F}{C_T} \quad (31)$$

where GBW is the gain-bandwidth product, which for CMOS transconductance amplifier is given by

$$GBW = \frac{g_m}{2\pi C_O}. \quad (32)$$

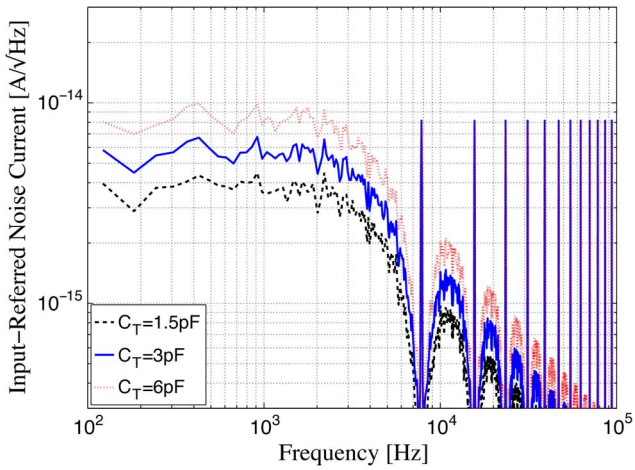

Fig. 16. Noise simulation of the input-referred noise current for various input capacitances. Increasing the input capacitance raises the noise floor by means of a square law. Note that both input and output ranges are constant, thus the noise reduction causes an increase in DR. The simulations were performed on the system proposed in [52] where $C_F = 100$ fF, $T_S = 128\,\mu$s, $T_{INT} = 120\,\mu$s, $T = 300°$K and $C_O = 4$ pF.

The capacitance C_O is the total capacitance connected to the opamp output (i.e., $C_1 + C_2$) in a one-stage opamp, and the compensation capacitance in a multi-stage realization. Equation (29) together with (9), (31), and (32) yields

$$\overline{i^2_N} \approx \frac{16}{3}\frac{C_T C_F}{T_S}\frac{kT}{C_O} = \frac{16}{3}\frac{C_T}{R_{EQ}}\frac{kT}{C_O} \quad (33)$$

where the input-referred noise power of DT current sensing is regarded as the noise generated by an equivalent resistor of value R_{EQ}, or, more precisely, as kTC noise relating to the output capacitance. Equation (33) shows how the input stray and the sensor capacitances act directly on the noise PSD by means of C_T, and how a large C_O reduces noise power at the expense of settling time. It is interesting to note that (27) associates the sensitivity of DT systems with the sampling frequency, affecting the dynamic range (DR), which is given by the ratio between the maximum input signal power and the in-bandwidth noise power

$$DR = \frac{V^2_{OM}}{R^2_{EQ} \cdot \overline{i^2_N} \cdot \frac{f_S}{2}} = \frac{V^2_{OM} \cdot C_F^2}{\frac{\overline{i^2_N}}{f_S}} = \frac{V^2_{OM}}{\frac{8}{3}\frac{C_T}{C_F}\frac{kT}{C_O}} \quad (34)$$

where V_{OM} is the maximum output voltage of the amplifier.

Since the CDS is a time-variant discrete-time circuit, it is not possible to use the classical AC noise analysis to correctly describe its noise behavior. To confirm the above analysis on real circuits, time-varying noise simulations using the Spectre simulation tool [76] were performed on the circuit of Fig. 11 and are illustrated in Figs. 16–18.

Note that noise simulations have been done using several different random seeds in the statistical noise models, showing negligible variations from the shown results. Fig. 16 shows a

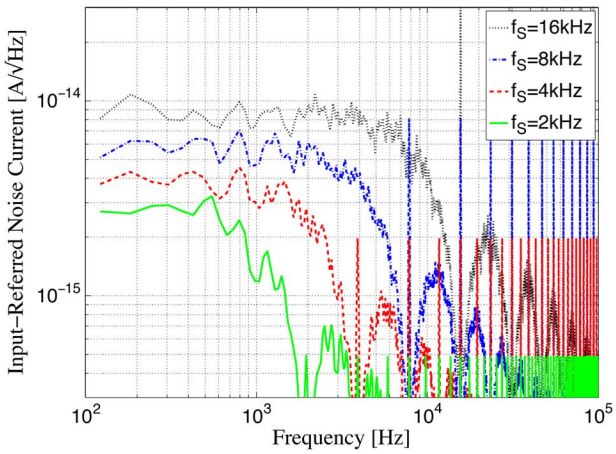

Fig. 17. Noise simulations of the input-referred noise current for different sampling frequencies f_S. The simulations were done on the system proposed in [52], where C_F was fixed at 100 fF and a 3pF input stray capacitance was used. Other circuit parameters are the same used for Fig. 16. Noise reduction is mainly related to the increase in the equivalent resistance R_{EQ} following (27).

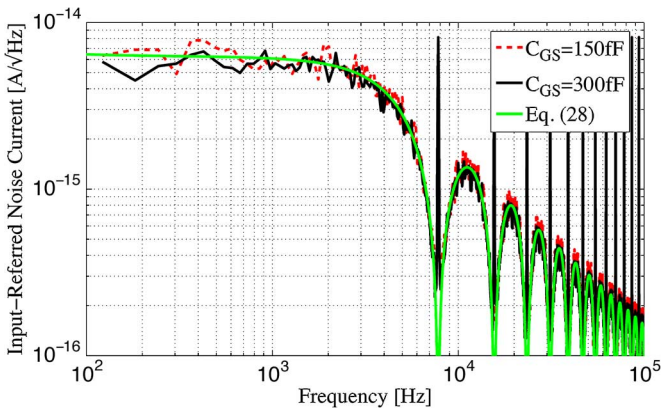

Fig. 18. Noise simulation of the input-referred noise current on the system proposed in [52] with an input stray capacitance of 3 pF and the same circuit parameters used for Fig. 16. Doubling the form factor of the input differential pair in the employed opamp, we increase the gate-source capacitance C_{GS} (from 150 fF to 300 fF) as well as the transconductance g_m. However, these changes do not affect the input-referred noise that is independent of opamp parameters. The figure also compares the theoretical model with simulation results, showing a good matching with 3pF as input stray capacitance, which is a reasonable value.

linear reduction of input-referred noise with C_T as in (33). Conversely, as illustrated in Fig. 17, a linear reduction of the sampling frequency causes a root square reduction of the input-referred noise current, while the DR being unchanging (34).

Finally, note that there are no parameters relating to the opamp in (35). This is due to the fact that, as in kTC noise, a decrease in the input noise voltage power $\overline{e^2_{n-op}}$ by means of g_m involves an equivalent increase in the bandwidth according to (31) and (32). Thus, opamp noise performance does not affect the overall DR, as indicated in (34), and the input-referred noise is not subject to the C_{GS} trade-off, as shown in Fig. 18, where the form factor of the input pair of the opamp has been changed.

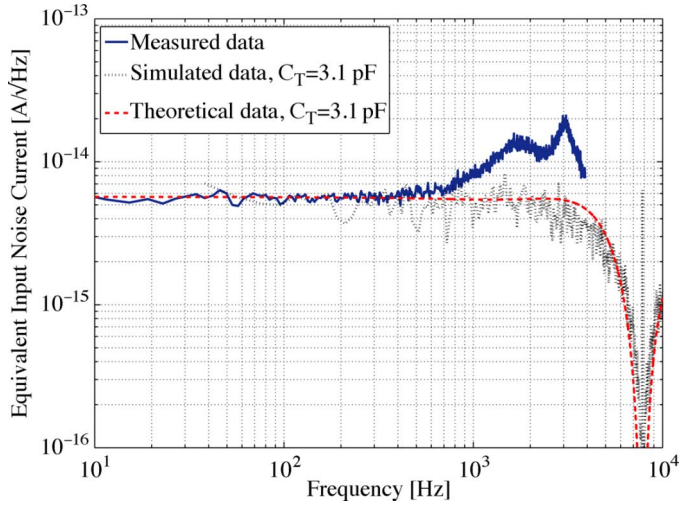

Fig. 19. Verification of the noise model with measurements and simulations. Measured current noise on the prototype presented in [52] (solid blue line), theoretical input-referred noise current given by (28) using parameters $T_S = 128\ \mu$s, $T_{INT} = 120\ \mu$s, $C_F = 100$ fF, $C_T = 3.1$ pF, $C_O = 4$ pF (dashed red line) and simulated input noise using the same parameters (pointed black line). The picture shows a good match for an input stray capacitance of 3 pF, which is in good agreement with the estimated values for the device under test. Peaks at 2 kHz and 3 kHz in measurements are related to clock coupling effects.

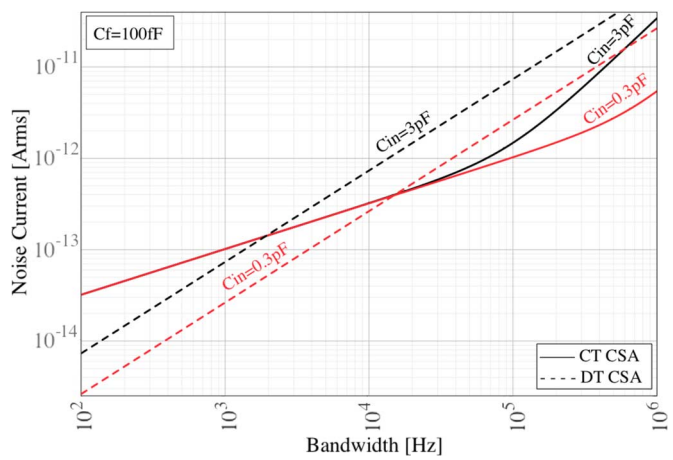

Fig. 20. Root mean square noise versus system bandwidth for a given feedback capacitance. The r.m.s. noise is computed on (12) and (33) using the same parameters employed for simulations used in Fig. 10 and Fig. 17 for CT and DT, respectively. DT approach achieves better noise performance for reduced acquisition bandwidth while CT approach is the better solution for high bandwidth applications. Moreover, DT schemes are intrinsically limited at high bandwidth, since integration time is related to the minimum feedback capacitance according to (27).

The plot clearly shows that the input-referred noise current is not affected by opamp parameters, like transconductance g_m or input capacitance C_{GS}, validating the proposed noise model. In Fig. 19 the input-referred noise current given by the square root of (28) is compared with a measurement taken from the system developed in [52], and proves a good match. Peaks at 2 kHz and 3 kHz are related to clock coupling effects.

DT current sensing schemes are also affected by jitter noise, since the equivalent transresistance R_{EQ} is directly related to

TABLE II
PUBLISHED INTEGRATED IMPLEMENTATIONS OF CURRENT INTERFACES AIMING AT SUB-pA RESOLUTIONS COMPARED IN TERMS OF NOISE PERFORMANCE, BANDWIDTH AND POWER CONSUMPTION. NOTE THAT POWER CONSUMPTION DATA ARE NORMALIZED OVER NUMBER OF ACQUISITION CHANNELS AND DO NOT TAKE INTO CARE ADC POWER. THE ONLY EXCEPTION IS [54], WHERE IT IS NOT POSSIBLE SPLITTING POWER CONSUMPTIONS. THE TABLE SHOWS THAT CT IMPLEMENTATIONS CAN ACHIEVE HIGH ACQUISITION BANDWIDTH WHILE DT IMPLEMENTATIONS ARE LESS POWER HUNGRY

Paper	*Approach*	*Noise floor @ room temperature*	*Noise Floor Bandwidth [kHz]*	*Analog Power Consumption*	*Input capacitance for characterization of noise floor*	*Operating bandwidth [kHz]*	*Technology Node*	*Notes*
[46]	CT	3 fA/√Hz	100	60 mW	800 fF	0.1 – 4,000	CMOS 0.35µm	
[49]	CT	0.5 fA/√Hz	4	55 mW	1 pF	0 – 1,000	CMOS 0.35µm	Shot noise limited
[44]	CT	50 fA/√Hz	10	300 µW	10 pF	0 – 10	SOI 0.5µm	1/f noise not compensated
[78]	CT	158 fA/√Hz	1 – 500	132 µW	No	1,000	CMOS 0.18µm	
[80]	CT	280 fA/√Hz	–	4 mW	No	1000	CMOS 0.35µm	
[81]	CT	42 fA/√Hz	0.1 – 10	437 µW	No	10	CMOS 0.35µm	
[82]	CT	12 fA/√Hz	100	5 mW	No	10000	CMOS 0.13µm	
[56]	DT	80 fA/√Hz	0.1	1.1 mW	No	0 – 1	CMOS 0.5µm	Noise effect of CDS not modeled
[54]	DT	130 fA/√Hz*	0.5	11 µW	No	0 – 1	CMOS 0.5µm	*Noise current inferred assuming feedback cap=500 fF and other paper data
[51]	DT	3 fA/√Hz	2	1 µW	No	0 – 2	CMOS 0.5µm	Noise characterized using internal current generators
[55]	DT	100 fA/√Hz*	1E-4	3.4 µW	No	0 – 3E-2	CMOS 0.5µm	*Noise power inferred from paper data
[53]	DT	33 fA/√Hz	0.1	–	50 pF	0.1	SOI 0.5µm	
[52]	DT	5 fA/√Hz	0.7	15 mW	3 pF	0 – 4	CMOS 0.35µm	DT and CDS noise modeled on input capacitance
[79]	DT	7 fA/√Hz	5	–	6.5 pF	5	CMOS 0.35µm	Noise current inferred assuming white noise limited
[83]	DT	150 fA/√Hz	0.8	–	No	0.8	CMOS 0.18µm	Noise current inferred assuming white noise limited
[84]	DT	6 fA/√Hz	1	1.5 mW	7pF	100	CMOS 0.5µm	
[85]	DT	24 fA/√Hz	–	–	–	1.1	CMOS 0.35µm	

the sampling frequency, as shown in (27). Thus, the random timing error generates an output error given by

$$\Delta V_{OUT} = i_{IN} \cdot \frac{\Delta T}{C_F} \tag{35}$$

where ΔT is the jitter error. Assuming the maximum allowed output error is $V_{OM}/2^{ENOB}$, we can compute the maximum allowed jitter error as

$$\max \Delta T = \frac{C_F}{i_{IN-MAX}} \cdot \frac{V_{OM}}{2^{ENOB}} = \frac{C_F}{2^{ENOB}} \cdot R_{EQ} \approx \frac{T_S}{2^{ENOB}} \tag{36}$$

where i_{IN-MAX} is the full-scale input. Since typical DT current sensing interfaces work with a sampling frequency in the order of tens of kHz, the requirements in terms of jitter error are in the order of some picoseconds, even for acquisition to a 16 bit accuracy requirement. Finally, it should be pointed out that the requirement given by (36) should be considered as a worst case [77].

To summarize, DT current-sensing interfaces are described by input-referred PSD noise which is substantially different from what characterizes TIA or CT interfaces, and is unaffected by the C_{GS} trade-off. The use of CDS stage releases DT approach from kTC and flicker noise, however white noise increases due to the folding process, becoming the dominant component and setting the noise floor. Input capacitance results to be a strong limiting factor for DT schemes because it directly affects the noise floor (33); hence miniaturization of sensor and system comes to be a key point. However, noise reduction in DT current amplifiers could be accomplished by acting on several parameters. For some of them, such as output, stray and feedback capacitances, reduction of noise also implies an increase in DR. Conversely, other parameters, such as the sampling time, do not affect the DR because the output swing is reduced by the same amount.

Finally, an interesting feature of DT approach is the weak dependence of the overall noise performance with respect to opamp parameters. This allows circuit designer to release the opamp design from noise constraints, focusing on other issues

such as lowering the power consumption. As an example, a DT current sensing scheme based on CSA and CDS has been shown to reach a noise floor as low as 3 $\mathrm{fA}/\sqrt{\mathrm{Hz}}$ with 2 kHz bandwidth and a power consumption of only 1 μW [51].

VI. Comparative Summary Between CT and DT Approaches

Both CT and DT solutions are based on charge-sensitive amplifiers and are sensitive to the input capacitance. Hence, for a fair comparison between them the feedback capacitance C_F and the input capacitance C_{IN}, should be equal. Fig. 20 shows the r.m.s. noise current versus the acquisition bandwidth for both approaches with C_F fixed to 100 fF. The r.m.s. noise currents are computed on (12) and (33) for CT and DT, respectively. As shown by the picture, DT approach has lower r.m.s. noise for small acquisition bandwidth, while CT approach shows to be the best solution for high bandwidth applications. Moreover, DT schemes are intrinsically limited at high bandwidth, since integration cannot be lower than few microseconds. Thus, the choice of the best approach is tightly dependent on the bandwidth required by the application.

A. State-of-the-Art Review

To organize a fair comparison between them, based on different schemes as presented in the literature, it is important to characterize the noise floor by taking into account the total input capacitance C_T, which strongly affects both approaches. It reduces the noise floor bandwidth in CT schemes whereas it directly increases the noise floor value in DT schemes.

Table II compares recent CMOS integrated implementations of current interfaces as presented in the literature. From this comparison, it is apparent that many CT approaches reach the MHz bandwidth, while DT approaches are more limited in bandwidth, confirming our analyses. For this reason the CT approach appears to be the best solution for applications where fast current tracking is mandatory, like DNA sequencing. While, DT approach offers the possibility of better integration into complex system, low power capability, as well as noise performance comparable to CT schemes.

VII. Conclusion

This paper presents an overview of the basic noise limits of CMOS implementations of current-sensing interfaces for bio-nanosensors. Both continuous-time and discrete-time approaches have been described in detail with particular reference to the overall noise performance and the design parameter trade-off. Analytical models for input-referred noise in CT and DT architectures have been derived. The former is valid for the entire frequency spectrum, while the latter is limited to frequencies lower than f_S. The paper illustrates how to evaluate the fundamental noise limits of the most conventional architectures.

The main results of the analysis are: 1) CT approaches are limited in resolution by the noise of feedback devices that are required in order to set the bias point. Thus, design should focus on this issue rather than opamp noise optimization. On the other side, the resolution of DT approaches is limited by the aliasing of the high frequency noise inside the baseband; 2) CT solutions offer better performance in terms of bandwidth, which is fixed by the first pole of the differentiator, whilst in DT approaches the bandwidth is limited by the feedback capacitance value and full-scale trade-off; 3) DT approaches offer better noise performance at reduced bandwidth but they are surpassed by CT ones for larger bandwidths; 4) Input capacitance strongly affects noise performance in both CT and DT solutions, but most remarkably on the last one; and 5) 1/f noise of CSA plays a marginal role in input-referred noise in both approaches due to the derivative effect of the input transimpedance amplifier. Finally, by way of summary, a comparative table of recent papers appearing in the literature has been presented.

Acknowledgment

The authors would like to thank F. Thei, M. Rossi, G. Ferrari, and M. Sampietro for their helpful suggestions and comments.

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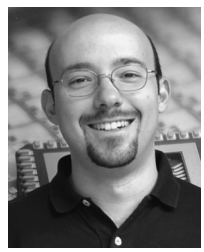

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