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A Review on Serial Communication by UART

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Abstract: In parallel communication the cost as well as complexity of the system increases due to simultaneous transmission of data bits on multiple wires. Serial communication alleviates this drawback and emerges as effective candidate in many applications for long distance communication as it reduces the signal distortion because of its simple structure. Universal Asynchronous Receiver Transmitter (UART) is a kind of serial communication protocol. This paper presents implementation of UART with different methods. Different techniques which were using with UART are discussed for reliable data transmission. The proposed work suggests application Design using UART.

Keywords— UART; Asynchronous serial communication; VHDL; Quartus II; simulation.

I. INTRODUCTION

A universal asynchronous receive/transmit (UART) is an integrated circuit which plays the most important role in serial communication. It handles the conversion between serial and parallel data. Serial communication reduces the distortion of a signal, therefore makes data transfer between two systems separated in great distance possible. It contains a parallel-to serial converter for data transmitted from the computer and a serial to parallel converter for data coming in via the serial line. The UART also has a buffer for temporarily storing data from high speed transmissions. In addition to the basic job of converting data from parallel to serial for transmission and from serial to parallel on reception, a UART will usually provide additional circuits for signals that can be used to indicate the state of the transmission media and to regulate the flow of data in the event that the remote device is not prepared to accept more data. UART must have a larger internal buffer to store data coming from the modem until the CPU has time to process it.

The UART serial communication module is divided into three sub-modules: the baud rate generator, receiver module and transmitter module Therefore, the implementation of the UART communication module is actually the realization of the three sub-modules. The baud rate generator is used to produce a local clock signal which is much higher than the baud rate to control the UART receive and transmit; The UART receiver module is used to receive the serial signals at RXD, and convert them into parallel data; The UART transmit module converts the bytes into serial bits according to the basic frame format and transmits those bits through TXD.

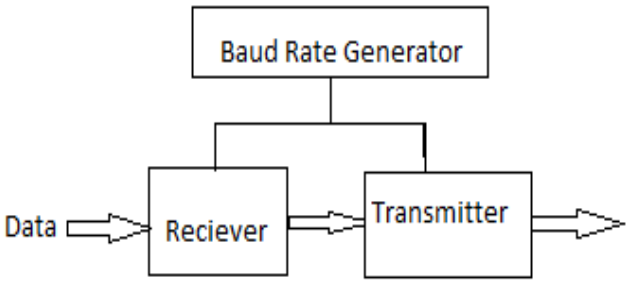

Fig 1. UART MODULE

UART Transmission Protocol:

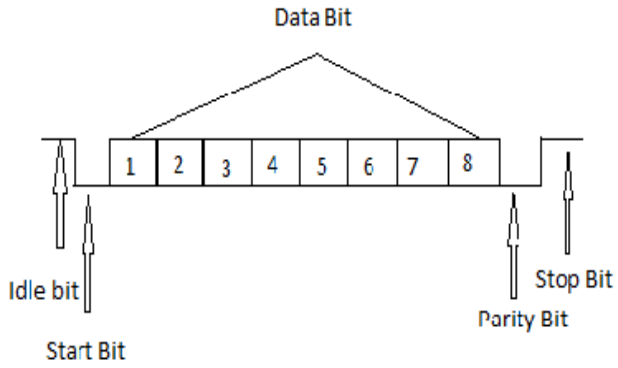

Fig 2. UART FRAME FORMAT

It usually includes start bit, data bit, parity bit, stop bit and idle state as shown in fig 2.When a word is given to the UART for Asynchronous transmissions, a bit called the "Start Bit" is added to the beginning of each word that is to be transmitted. The Start Bit is used to alert the receiver that a word of data is about to be sent, and to force the clock in the receiver After the Start Bit, the individual bits of the word of data are sent, with the Least Significant Bit (LSB) being sent first into synchronization with the clock in the transmitter. When the entire data word has been sent, the transmitter may add a Parity Bit that the transmitter generates. The Parity Bit may be used by the receiver to perform simple error checking. Then at least one Stop Bit is sent by the transmitter. If incorrectly formatted data is received, the UART may signal a framing error. If another byte is received before the previous one is read, the UART will signal an overrun error.

II CASE STUDY ON UART

From review of related work and published literature, it is observed that many researchers have designed UART by applying different techniques like algorithms, logical relations. Researchers have undertaken different phenomena with regards to design UART and attempted to find better result. Today in real world the actual applications, usually needed only a few key features of UART. Specific interface chip will cause waste of resources and increased cost. Particularly in the field of electronic design, SOC technology is recently becoming increasingly mature. This situation results in the requirement of realizing the whole system function in a single or a very few chips. From the careful study of reported work it is observed that very few researchers have taken a work for integrating the required feature of UART.

Mohd Yamani Idna Idris, Mashkuri Yaacob and Zaidi Razak have design UART with BIST capability [1]. In this designed, To increase reliability, manufacturers must be able to discover a high percentage of defective chips during their testing procedures. They highlight the attention given by most customers who are expecting the designer to include testability features that will increase their product reliability. They suggested the design of a UART chip with embedded built-in-self-test (BIST) architecture using FPGA technology. In this technique the behaviour of UART circuit is describe by using VHISC hardware description language (VHDL). In the implementation phase, the BIST technique will be incorporated into the UART design before the overall design is synthesized by means of reconfiguring the existing design to match testability requirements.

One of the most important applications of UART is Multi-channel UART Controller designed by Shouqian Yu, Lili Yi, Weihai Chen and Zhaojin Wen.[2]. The proposed method paper presents a multi-channel UART controller based on FIFO technique and FPGA. This controller is designed with FIFO circuit block and UART circuit block to implement communication in modern complex control systems quickly and effectively. In this, the flow charts of data processing as well as the implementation state machine are also presented in detail. This controller can be used to implement communication when master equipment and slaver equipment are set at different Baud Rate. It also can be used to reduce synchronization error between sub-systems in a system with several sub-systems. The controller is reconfigurable and scalable.

From the survey it is observe that the implementation of UART basically uses the on-chip UART IP hard core because it has high performance but it has poor flexibility and poor transportability, hence it is usually unable to meet the high requirements of the customer. With the rapid development of FPGA soft core plays an increasingly important role in embedded system depending on the high performance, high flexibility, transportability and configuration. Huimei Yuan, Junyou Yang and Peipei Pan presented new methodology that provide Optimized Design of UART IP Soft Core based on DMA Mode [3]. They provide UART IP soft core based on DMA mode. The IP core is AVALON bus-compatible with the control and arithmetic logic of entire IP core completed by a single FPGA chip so that it is very suited to NIOSII embedded system. Since the two kinds of transmission will often interrupt the operation of CPU during the data transmission process, especially when transmitting large data, it will occupy a lot of time of CPU, thus greatly reducing the performance of the overall NIOSII system.The whole IP core is tested and verified in a simple NIOSII embedded hardware system. It turns out that UART IP soft core based on DMA mode can reduce elapsed time of CPU

greatly in data transmission process so that the performance of NIOSII system can be improved and design requirement can be better met with less resources occupied, high speed, high flexibility and high transportability.

Researchers have undertaken different design processes or phenomena with regards to use serial communication as it reduces signal distortion. Naresh patel, Vatsalkumar Patel and Vikaskumar Patel proposed design of UART with Status register [4] which includes three modules which are the baud rate generator, receiver and transmitter that satisfies the system requirements of high integration, stabilization, low bit error rate, and low cost. The work also supports configurable baud rate generator and variable data length from 5-8 bits per frame. This work detect the different types of errors occurred during communication and hence correct them.

In recent year, a need of high speed UART might be the first demand in serial communication. Hazim Kamal Ansari and Asad Suhail Farooqi introduces concept of high speed UART for programming FPGA [5]. They suggested that to maintain time triggered communication within FPGA a separate controller must be designed within it and this controller is called UART. FPGAs are suited to I/O intensive operations and it is very fast. Design Partitioning across the two devices can increase overall system speeds, reduce costs, and potentially absorb all of the other discrete logic functions in a design – thus presenting a truly reconfigurable system. They describe UART controller which is designed within FPGA based on SRAM with high speed and high reliability. The controller can be used to implement communications in complex system And it also can be used to reduce time delays between sub-controllers of a complex control system to improve the synchronization of each sub-controller. According to them, FPGAs are replacing convention programmable logic devices and within next few years they would be required at each and every application.

III. APPLICATION DESIGN USING UART

From Careful study of reported work, it is observed that researchers have proposed various techniques to design the UART chip and to improve its characteristics. Considering all the advantages suggested by different researchers we are defining an application of UART where there is serial communication of key board characters from PC hyper terminal through RS232 serial port using UART controller will be display on the HD44780 based 16x2 LCD display using LCD controller. The hardware implementation of UART Controller and LCD driver would be based on VHDL language. The proposed block diagram is shown below:

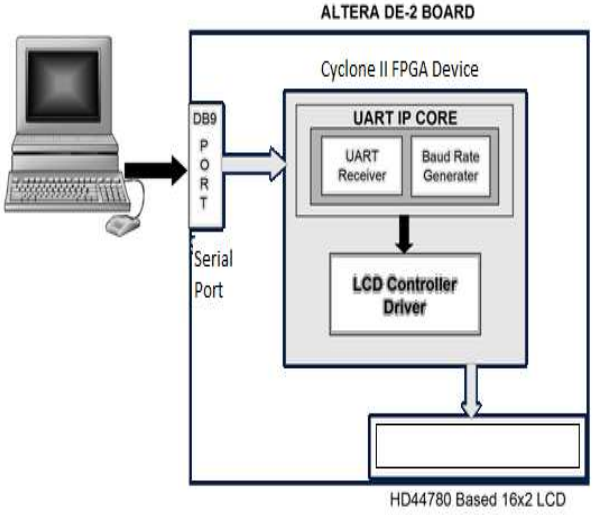

Fig. 3 Application design of UART

IV. CONCLUSION

A survey of various method for implementation of serial communication through UART is done in this paper. From the reported work we are designing an application that explore usage of UART to achieve benifits like great flexibility, low cost, high performance logic solutions and also meet communication demands quickly and efficiently.This design shows great significance especially in the field of electronic design, where SOC technology has recently become increasingly mature.

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