Review and Analysis of CMOS Current Readout Circuits for Biosensing Applications

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***Abstract*—CMOS current readout is a critical circuit block for various applications like bio-sensing. This paper presents an overview of CMOS current readout techniques and analyze their merits and demerits, including noise floor, sensitivity, and achievable system bandwidth. Mainly, the practical applicability of individual technique/design for integrated low-noise bio-sensing applications is discussed. To present a thorough insight of the state-of-the-art, most recent and relevant articles published in the literature related to the current sensing interface are summarized and compared. The paper identified the primary DC current rejection schemes, where each approach and its limitations are discussed and shown that each system comes with its limits.**

***Index Terms*—Current sensing, sensor readout interface, noise, biosensors, biomedical applications.**

I. Introduction

An emerging interest has been witnessed over the last decade in the confluence of nanotechnology with biotechnology and integrated circuits. This trend promises huge potential for the development of real-time, sensitive, and robust biosensor systems composed of CMOS technologies to extract analytical details. CMOS-enabled biosensors will certainly play critical roles in applications such as healthcare, food safety, and many more. Till now, CMOS current readout is the most creditable technique used in bio-sensing systems, such as photoplethysmography monitoring, molecular-concentration detection, and bioluminescent protein sensing, etc. [1]. As an example, some of the most used biosensors are shown in Fig. 1, including the solid-state nanopore [2], electrochemical sensors [3], ion sensor [4], and carbon nano-tube [5], etc.

In bio-sensing applications, accurate current measurement is crucial while challenging, such as in the case of nanopore or fluorescence sensing in which a sub-pA signal current is always overlaid by a fA∼nA dark current and up to μA baseline current [2]. Therefore, the current readout circuitry must often exhibit as low as a few fA input-referred noise, wide dynamic range (e.g., above 120 dB), and high linearity albeit often with low bandwidth (a few Hz to a few kHz) [2]. Over the years, CMOS current readout system benefits from the constant improvements at the circuit and architectural level. Almost every design presents a novel perspective to address certain limitations and/or resolves some of the system-related technological constraints [6]. The main challenge a circuit designer faces is to select a suitable topology based on the design specifications such as bandwidth, input-referred noise, power consumption, dynamic range, and sensitivity [7]. Some

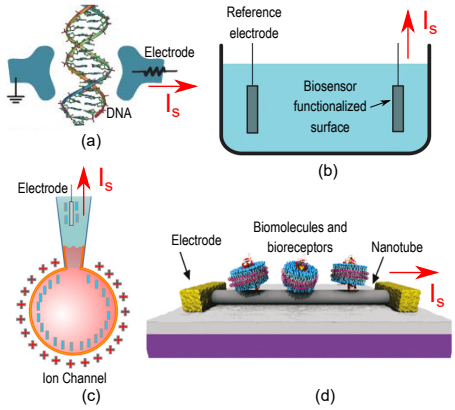

Fig. 1. Some example biosensors with current output: (a) solid-state nanopore [2], (b) electrochemical sensing [3], (c) patch clamp [4], (d) nano-tube [5].

of these aspects have a direct tradeoff with each other, which makes the choice even more challenging.

This paper presents an overview analyzing the evolution of existing CMOS current readout systems that target for low noise, wide dynamic range, and with good trade-offs between bandwidth and power consumption. This paper summarizes the limitations of resistive feedback systems and emphasizes why capacitive feedback systems are more favorable in bio-sensing applications. Moreover, different topologies of capacitive feedback system to achieve input baseline current cancellation are briefed and analyzed.

II. Basic CMOS Current Readout Topologies

Transimpedance amplifier (TIA) is a major building block used in current sensing systems. It converts a weak signal current to a voltage output with substantial magnitude [6]. A TIA employs negative feedback to minimize its input impedance, which makes it suitable for current sensing [8]. In this section, two basic TIA structures will be analyzed, including the conventional resistive shunt feedback topology and the increasingly popular capacitive feedback topology.

A. Resistive Feedback TIA

The term "TIA" usually refers to the classical resistive shunt feedback operational amplifier shown in Fig. 2. Its output voltage can be expressed as: $V_{\text{out}} = I_{\text{in}} \cdot R_{\text{f}}$, where R_{f} is the feedback resistor and I_{in} is the input current (the sensor output). For an ultra-small input signal current, a large R_{f} is

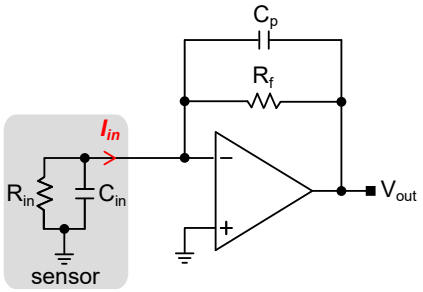

Fig. 2. Schematic of a simplified resistive feedback TIA (including the shunt parasitic cap $C_{\rm p}$).

required to produce a reasonable output voltage amplitude. For example, a 1 V full-scale voltage output mandates a 1 GΩ resistor for a 1 nA input current (a typical sensor output value). Integrating such a large resistor on chip is challenging, not only because of its large area, but the TIA's bandwidth will be degraded by the large stray shunt capacitance $C_{\rm p}$ of this resistor as in (2).

$$V_{\rm out} = I_{\rm in} \cdot R_{\rm f} \cdot \frac{1}{1 + sR_{\rm f}C_{\rm p}} \tag{1}$$

If we look from the noise prospective, the input-referred current noise density of this TIA is

$$\overline{I^2_{\rm n,in}} = \frac{4kT}{R_{\rm f}} + 2q \cdot I_{\rm in} + \overline{V}^2_{\rm n,in\text{-}amp} \cdot [\frac{1}{R^2_{\rm f}} + s^2(C_{\rm in} + C_{\rm p})^2] \tag{2}$$

where $I_{\rm in}$ is the input current, $\overline{V}^2_{\rm n,in\text{-}amp}$ is the input-referred noise of the error amplifier, k is the Boltzmann constant, T is the absolute temperature and $2q \cdot I_{\rm in}$ represents shot noise of the input devices. The influence of $R_{\rm in}$ is ignored in this calculation as $R_{\rm in} \ll R_{\rm f}$ often holds. (1)(2) indicates that the resistive feedback TIA to achieve high gain and low noise (e.g., a large $R_{\rm f}$) will suffer from poor bandwidth performance or vice versa, thus making it less attractive.

B. Capacitive Feedback TIA

An effective solution to maintain the high gain (or minimal noise) of the resistive feedback TIA without sacrificing its bandwidth is to replace the resistor with a noise-free component such as a capacitor. With this arrangement, the TIA output voltage is an integral of the input current,

$$V_{\rm out} = \frac{1}{C_{\rm f}} \int_0^{T_{\rm int}} I_{\rm in} \cdot dt \tag{3}$$

where $C_{\rm f}$ is the feedback capacitance and $T_{\rm int}$ is the current integration time. The main drawback of capacitive feedback TIA is that its output saturates over time either because of the large baseline current of the sensor and/or a large signal current. To overcome this limitation, two techniques are usually adopted. The first technique is discrete-time (DT) by adding a reset switch to periodically clear the charge stored in $C_{\rm f}$, as in Fig. 3(a). The second technique is continuous-time (CT) by adding an active feedback network to cancel the input baseline current to prevent the output from saturation, as in Fig. 3(b).

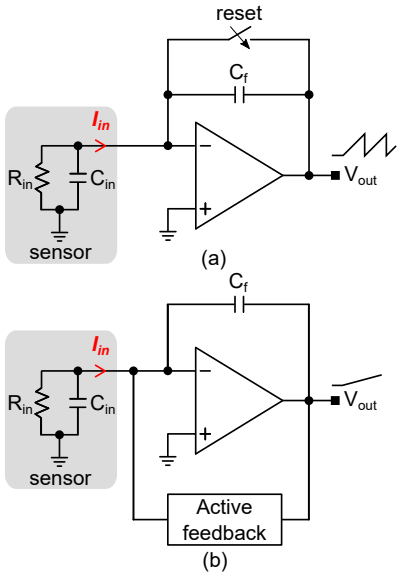

Fig. 3. Capacitive feedback TIA using (a) a reset switch, and (b) an active feedback network to avoid output saturation.

Because capacitive feedback TIA offers lower input-referred noise as compared to that of the resistive feedback TIA, it is preferred in most of the high-resolution current sensor interfaces [9]. However, both the DT and CT implementation scheme mentioned-above still have many drawbacks to be addressed, such as the charge injection and KTC noise issues in the DT scheme, or the noise associated with the feedback path in the CT scheme. The evolution of technical improvements made over time to overcome these limitations is discussed in the next section.

III. Key Technique Evolution of Capacitive Feedback TIA Design

A. Discrete Time Approach with Reset Switch

As in Fig. 3(a), in a typical DT implementation, the Opamp is prevented from saturation by periodically resetting $C_{\rm f}$. This reset may cause the loss of input data thus the reset duration must be minimized. The dynamic range of the DT approach is limited by the size of $C_{\rm f}$ as its output is obtained by integrating the input current. Dynamic range can be improved by a self-resetting scheme that can be employed to detect higher photocurrent [10]. Whereas to improve sensitivity, a small $C_{\rm f}$ is often preferred. This unfortunately implies a large KTC noise contributed by the reset switch, let alone the influence of charge injection.

Most current interface designs used the correlated double sampling (CDS) technique shown in Fig. 4 to reduce the time-correlated flicker noise and to improve the readout sensitivity [11]–[13]. The CDS technique is principled on the fact that in the presence of noise in a band-limited system, low-frequency components are correlated and can be used to cancel

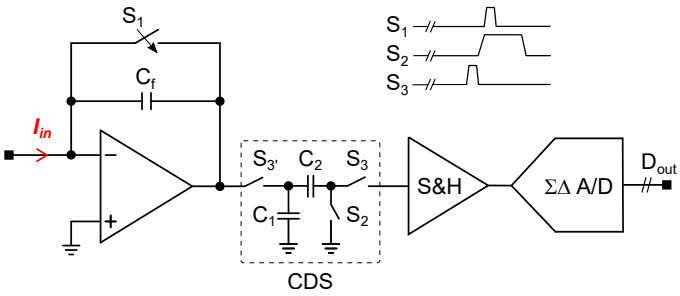

Fig. 4. Schematic of discrete time current readout system followed by a CDS block to reduce low frequency noise and offset [11].

each other. This technique benefits from sampling the input signal twice, firstly in the presence of only the low-frequency noise, then in the presence of signal and low-frequency noise. Though CDS reduces time-correlated flicker noise, due to the sampling operation, it increases the overall white noise because of noise-folding. Therefore, an explicit input anti-aliasing filter is required when using this DT approach. For biomedical applications, the signal bandwidth is relativity low, designing such a filter again mandates large chip area and power. As a result, the advantage of using capacitive feedback is somehow dissolved.

Moreover, in biomedical applications such as fluorescence sensing, the readout must be sensitive to femto-ampere inputs. In this case, besides low-frequency noise, the dark current generated by the sensing diode must be minimized as well. The design in [13] utilizes the leakage current of the reset switch to compensate for the leakage current of the reverse-biased sensing diode. Though no perfect cancellation can be achieved, it indeed improves the readout sensitivity. However, for most designs, leakage from this reset switch is unwanted and difficult to avoid.

B. Continuous Time Approach with Active Feedback

The main limitation of the discrete-time capacitive feedback system is noise-folding and the leakage current of the reset switch, making it band-limited. The continuous-time approach introduces an active feedback loop to resolve the saturation issue by canceling the baseline current present at the input thus making it suitable for higher bandwidth applications. A CT architecture typically includes an integrator followed by a differentiator. The integral of the input current is present at the integrator output; thus, a differentiator is required to restore the actual input signal information and have a constant gain within the desired signal bandwidth. The transimpedance gain and the output voltage of integrator-differentiator architecture can be expressed as [9]:

$$\frac{V_{\text{out}}}{I_{\text{in}}} = R_{\text{fd}} \cdot \frac{C_{\text{d}}}{C_{\text{f}}} \tag{4}$$

$$V_{\text{out}} = I_{\text{in}} \cdot R_{\text{fd}} \cdot \frac{C_{\text{d}}}{C_{\text{f}}} \tag{5}$$

where C_{f} is the feedback capacitance of an integrator, R_{fd} and C_{d} is the feedback resistance and input capacitance of

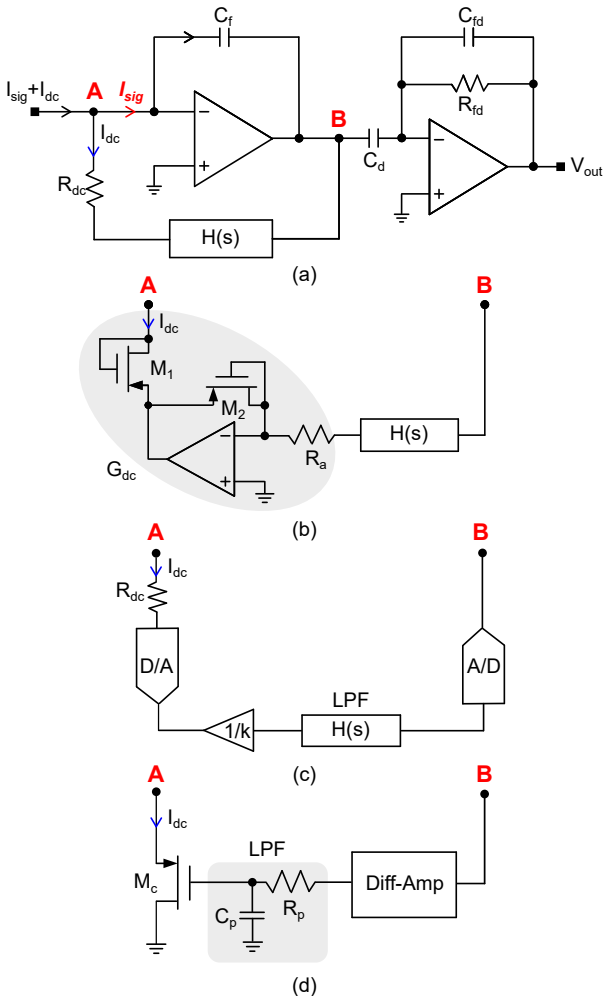

Fig. 5. Schematic of CT system with active feedback network for baseline input DC current removal. (a) CT feedback [16], (b) low noise active feedback [17], (c) semi-digital feedback [18], (d) passive LPF network [9].

the differentiator respectively. The combination of integrator-differentiator architecture offers a robust current to voltage conversion without noise or bandwidth penalties. One of the critical building blocks of a CT capacitive TIA is the active feedback network. It provides a low impedance path to sink the input baseline current I_{dc} and removes charge accumulated on the integration capacitor. As a result, only the signal will be processed. The most popular feedback networks used in the literature are summarized in Fig. 5 and are explained below.

1) Different Feedback Networks: A fully integrated feedback network presented by [16] is shown in Fig. 5(a). It utilizes a feedback path, consisting of a low-pass block $H(s)$ and a resistor R_{dc} to sink the baseline current from the integration path. The main limitations of this design are the feedback loop stability and the noise contribution of R_{dc}. A latter improvement based on this scheme is presented in [17], where it replaces R_{dc} with R_{a} connected in series to an active low-noise linear transconductor G_{dc} as shown in Fig. 5(b). The key advantage of this network is the trasconductor's self-adaption to the amount of DC current from the input.

TABLE I
COMPARISON OF INTEGRATED CAPACITIVE FEEDBACK CURRENT READOUT INTERFACE AIMING AT SUB-PA RESOLUTION.

Design	Approach	Application	Technology (nm)	Noise (fA/$\sqrt{\text{Hz}}$)	Bandwidth (kHz)	Power (mW)	Input Cap (pF)	Input range (pA)
[11]	DT	Carbon nano-tubes	350	5	2	15	3	200 $\sim$ 5000
[12]	DT	Nanoparticles nanopores	500	6	10	1.5	7	10 $\sim$ 1200
[14]	DT	Impedance spectroscopy	**90**	**0.235**	2	**0.147**	n/a	0.075 $\sim$ 200
[15]	DT	Fluorescence sensing	180	150	1	2.24	n/a	**4 $\sim$ 21000**
[17]	CT	Single molecule sensing	350	3	**4000**	60	1	10
[18]	CT	DNA sequencing	Discrete IC	8.5	950	65	**10**	n/a
[9]	CT	DNA sequencing	130	52	1000	30	6	100 $\sim$ 10000
[20]	CT	Ion conduction microscopy	180	150	2700	18	2	n/a

Furthermore, this network can achieve a very high resistance up to 300 GΩ with high linearity, high sensitivity, thus extending the integrator bandwidth to a few megahertz. Another interesting integrator-differentiator design employing a hybrid semi-digital (HSD) feedback network is introduced by [18], as shown in Fig. 5(c). Its feedback path composed of an ADC, a digital low pass filter, a DAC, and a resistor R_{dc} connected in series. It not only cancels the input baseline current but also minimizes the flicker noise content of the integrator.

However, the approaches described above involve complex feedback circuitry to ensure the stability of the feedback network and require a giga-ohm resistor R_{dc} to reduce the overall noise floor. Later, a low-complexity, robust, and stable feedback loop with baseline current rejection block is manifested in [9]. Its feedback network is shown in Fig. 5(d). It includes a differential pair with a diode-connected load, a low pass RC filter, and a source follower PMOS device to sink the baseline current. Meanwhile, it reduces the complexity of the low-frequency feedback loop by reducing the number of poles with improved stability.

2) Design Trade Offs and Discussion: For the noise performance of the CT topology presented in state of the art [16] and [18] shown in Fig. 5(a) and (c) respectively. As $C_{\text{f}} \ll C_{\text{d}}$ often holds, the main noise contributors are the input-referred noise of the integrator opamp $\overline{V}^2_{\text{n,in-amp}}$, which is shaped by C_{f}, and parasitic input capacitance C_{in} [20]. The equivalent input-referred current noise density of this integrator-differentiator based TIA is [20]:

$$\overline{I^2_{\text{n,in}}} = \frac{4kT}{R_{\text{dc}}} + \overline{V}^2_{\text{n,in-amp}} \cdot [(2\pi f)^2 (C_{\text{in}} + C_{\text{f}})^2] \qquad (6)$$

(6) shows that R_{dc} can be increased autonomously to decrease the equivalent input noise, whereas R_{dc} has no impact on the overall gain. However, the value of R_{dc} limits the maximum input DC current, expressed as [19],

$$I_{\text{MAX,DC}} = \frac{V_{\text{DD}}}{R_{\text{dc}}} \qquad (7)$$

Thus requires compensation. Since R_{dc} is not in the signal path, it can be realized by a pseudo-resistor, whose nonlinearity will not affect the end-to-end SNDR of the system. A DC servo feedback loop proposed by [20] replaces R_{dc} by a multi-element pseudo resistor (MEPR), which greatly improves the TIA's robustness against shot noise at large DC current levels. Additionally, MEPR is very robust against process variations and offers high linearity. In [9], the noise generated by the feedback network is filtered out by the low-pass filter. The PMOS transistor operates in its deep sub-threshold region for a limited baseline current I_{dc} (e.g., 4 nA, 10 nA with off-chip calibrations), the only noise that will be injected to the integrator inputs is the shot noise associated with I_{dc}. The affirmative analysis concludes that noise and DC rejection have a trade-off. Particularly, the DC rejection schemes must be optimized to minimize their noise contributions. Such designs and architectures will be useful and required for bio-sensing applications where the DC current usually ranges from tens of nano amperes to μA range [21] [22].

IV. CONCLUSION

While considering current readouts for biosensing applications, Noise consideration is paramount and should be the essential factor followed by the bandwidth in selecting the current sensing technique. Different CMOS current readout techniques using resistive and capacitive feedback approaches (both DT and CT) are compared and analyzed in this paper regarding their noise and bandwidth performance. Due to the tradeoff between noise and bandwidth, the resistive feedback TIA is not favored in high-precision bio-sensing applications compared to the capacitive feedback TIA. Table I presents a brief comparison of recent capacitive feedback current readout designs, to address output saturation. It can provide the reader with an insight to choose between a discrete-time or continuous-time current sensing approach. It can be observed from the table that most of the architectures discussed are designed in a 180 nm CMOS process or above. One of the main issues at lower technology nodes is device leakage current. It can degrade the overall dynamic range when this leakage current is more than the minimum detectable current. If design with low-power, low-noise, and a few kHz-range bandwidths is desired, the discrete-time approach is recommended. If a large bandwidth is desired (e.g., to detect fast protein activity and rapid moving molecules), the continuous-time system is more favorable to allow time-resolved detection in the sub-μs range.

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