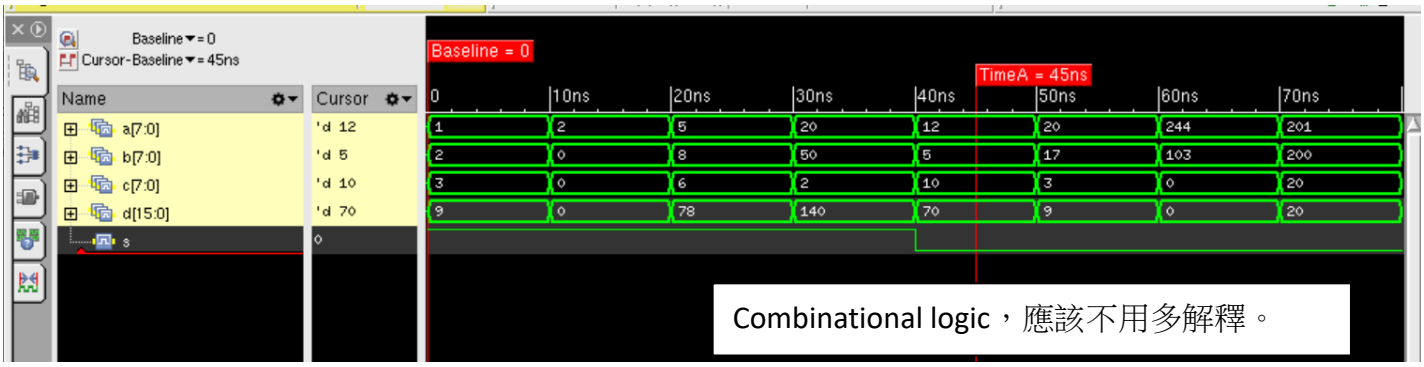
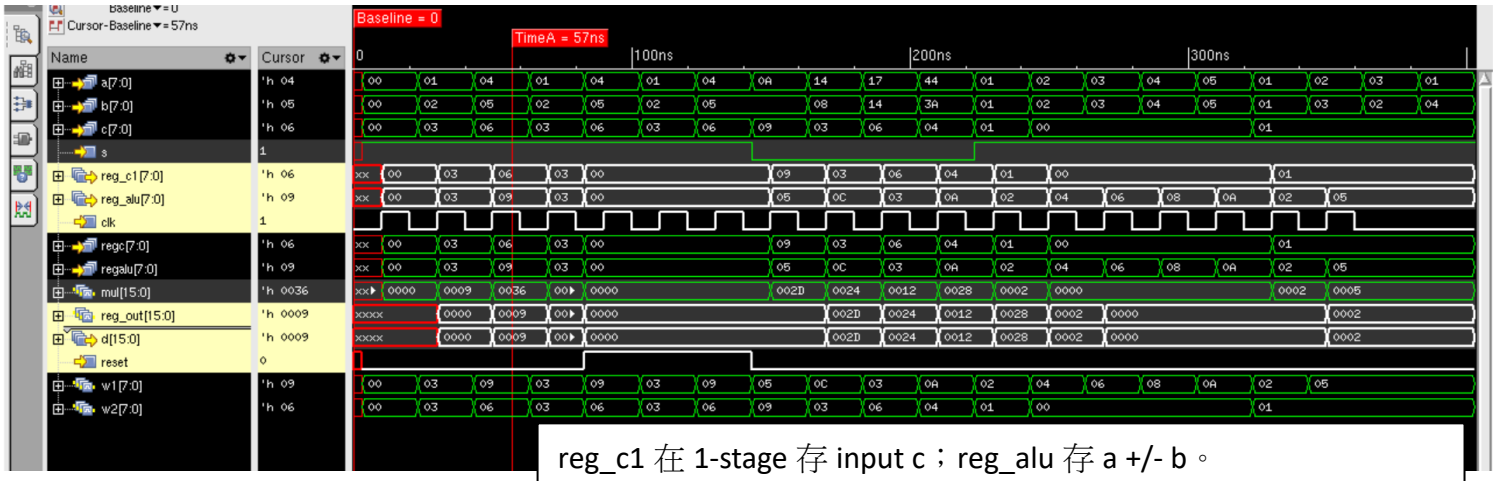
一、 Design Compiler

1. RTL 波型與解釋

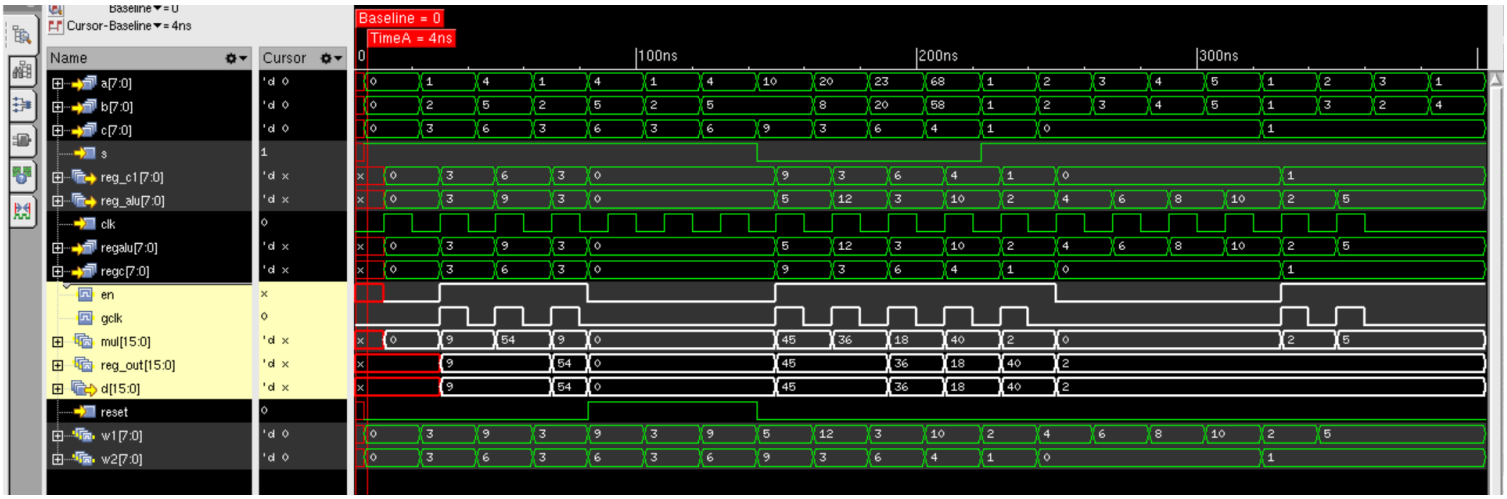
i. Nonpipe



ii. Pipe



iii. Pipe using clock gating

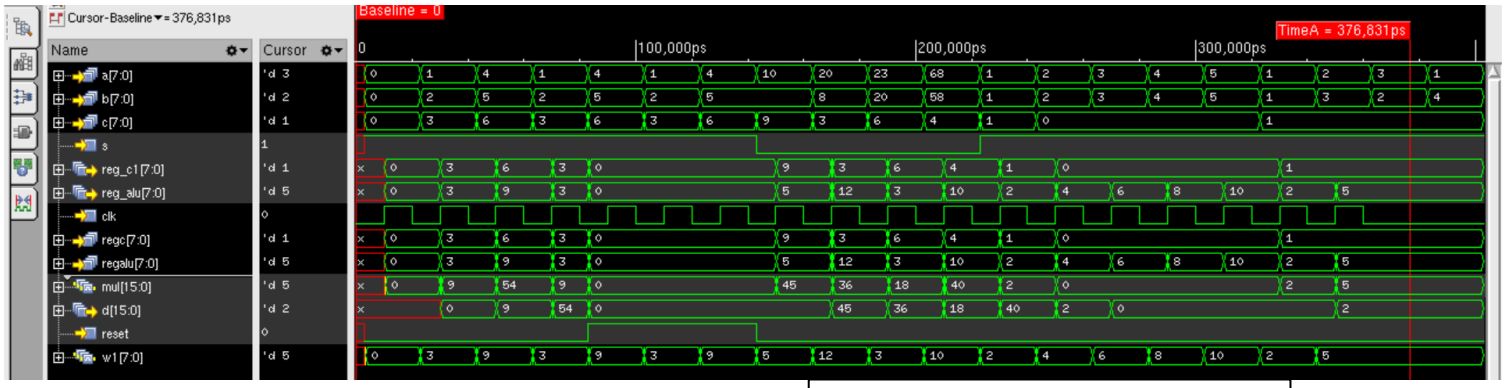


可以看到當 en (即 c)為 0 時，gclk 即關掉 2-stage pipeline register，使 mul[15:0](作 wire 用)，及上述提到的 reg_out 維持不變。

2. Gate-level 波型與解釋

i. Nonpipe

ii. Pipe



與 Gate-level 類似，不多解釋。

iii. Pipe using clock gating

看到 gclk 有個問題，導致 d[15:0]沒有值能接，不知道是不是 glitch？

3. 比較數據表格

	Area (um^2)			Delay	Latency	Power (W)		
	Cl	Sl	Total	(ns)	(ns)	dynamic	leakage	total
Non-pipelined (DC)	635.94	0	635.94	2.03		5.062(uW)	7.545(uW)	1.2606e-02 (mW)
Non-pipelined (PrimeTime)						Int: 3.29e-06 Swi: 1.91e-06	7.54e-06	1.27e-05
Pipelined (DC)	326.13	145.15	471.29	1.43		3.698(uW)	5.422(uW)	9.1195e-03 (mW)
Pipelined (PtimeTime)						Int: 2.96e-06 Swi: 4.04e-07	5.44e-06	8.80e-06
Clock-gated (DC)	330.9	145.15	476.05	1.43		3.262(uW)	5.476(uW)	8.7375e-03 (mW)
Clock-gated (PrimeTime)						Int: 2.69e-06 Swi: 4.85e-07	5.49e-06	8.67e-06

4. 二階不同 **pipeline** 內的 **timing** 資訊

```
Point                                                   Incr       Path
------------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
p1/reg_c1_reg_2_/CK (DFFRPQ_X2M_A9TR)                   0.00       0.00 r
p1/reg_c1_reg_2_/Q (DFFRPQ_X2M_A9TR)                    0.11       0.11 r
p1/reg_c1[2] (pipe1)                                    0.00       0.11 r
```

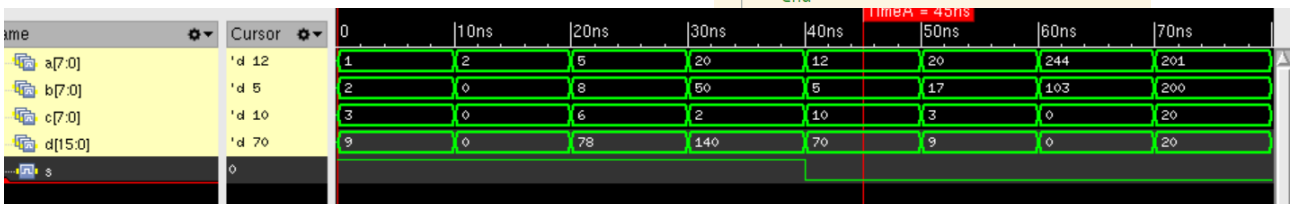
```
p2/regc[2] (pipe2)                                      0.00       0.11 r
p2/mult_36/a[2] (pipe2_DW_mult_uns_0)                   0.00       0.11 r
p2/mult_36/U152/Y (INV_X1M_A9TR)                        0.03       0.14 f
p2/mult_36/U175/Y (NOR2_X0P5A_A9TR)                     0.10       0.24 r
p2/mult_36/U53/S (ADDF_X1M_A9TR)                        0.15       0.39 f
p2/mult_36/U52/S (ADDF_X1M_A9TR)                        0.11       0.50 r
p2/mult_36/U12/CO (ADDF_X1M_A9TR)                       0.09       0.59 r
p2/mult_36/U11/CO (ADDF_X1M_A9TR)                       0.08       0.68 r
p2/mult_36/U10/CO (ADDF_X1M_A9TR)                       0.08       0.76 r
p2/mult_36/U9/CO (ADDF_X1M_A9TR)                        0.08       0.84 r
p2/mult_36/U8/CO (ADDF_X1M_A9TR)                        0.08       0.92 r
p2/mult_36/U7/CO (ADDF_X1M_A9TR)                        0.08       1.01 r
p2/mult_36/U6/CO (ADDF_X1M_A9TR)                        0.08       1.09 r
p2/mult_36/U5/CO (ADDF_X1M_A9TR)                        0.08       1.17 r
p2/mult_36/U4/CO (ADDF_X1M_A9TR)                        0.08       1.25 r
p2/mult_36/U3/CO (ADDF_X1M_A9TR)                        0.08       1.34 r
p2/mult_36/U2/S (ADDF_X1M_A9TR)                         0.09       1.43 r
p2/mult_36/product[14] (pipe2_DW_mult_uns_0)            0.00       1.43 r
p2/reg_out_reg_14_/D (DFFRPQ_X2M_A9TR)                  0.00       1.43 r
```

第一階 delay：0.11
第二階 delay：1.32

5. 自動驗證運算結果

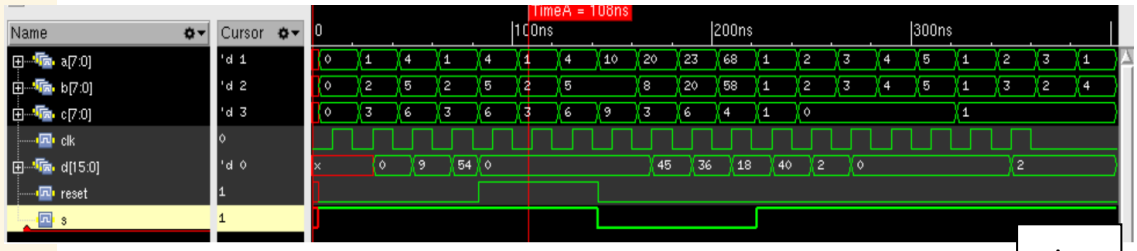
i. nonpipe

```
initial
    begin
        // (a+b)*c
        s = 1;
        a = 1; b = 2; c = 3; #10;
        a = 2; b = 0; c = 0; #10;
        a = 5; b = 8; c = 6; #10;
        a = 20; b = 50; c = 2; #10;

        // (a-b)*c
        s = 0;
        a = 12; b = 5; c = 10; #10;
        a = 20; b = 17; c = 3; #10;
        a = 500; b = 103; c = 0; #10;
        a = 201; b = 200; c = 20; #10;
    end
```

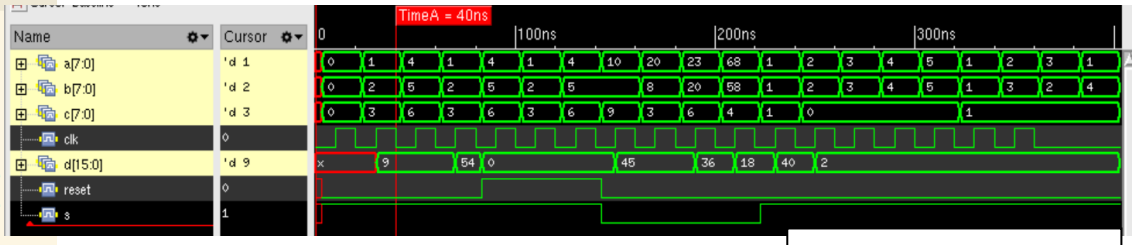


ii. pipe & pipe using clock gating

```
initial begin
    #3;
    s = 1;
    reset = 1'b0;
    a = 0; b = 0; c = 0; #20;
    a = 1; b = 2; c = 3; #20;
    a = 4; b = 5; c = 6; #20;
    a = 1; b = 2; c = 3; #20;

    reset = 1'b1;
    a = 4; b = 5; c = 6; #20;
    a = 1; b = 2; c = 3; #20;
    a = 4; b = 5; c = 6; #20;

    s = 0;
    reset = 1'b0;
    a = 10; b = 5; c = 9; #20;
    a = 20; b = 8; c = 3; #20;
    a = 23; b = 20; c = 6; #20;
    a = 68; b = 58; c = 4; #20;

    s = 1;
    reset = 1'b0;
    a = 1; b = 1; c = 1; #20;
    a = 2; b = 2; c = 0; #20;
    a = 3; b = 3; #20;
    a = 4; b = 4; #20;
    a = 5; b = 5; #20;
    a = 1; b = 1; c = 1; #20;
    a = 2; b = 3; #20;
    a = 3; b = 2; #20;
    a = 1; b = 4; #20;
```



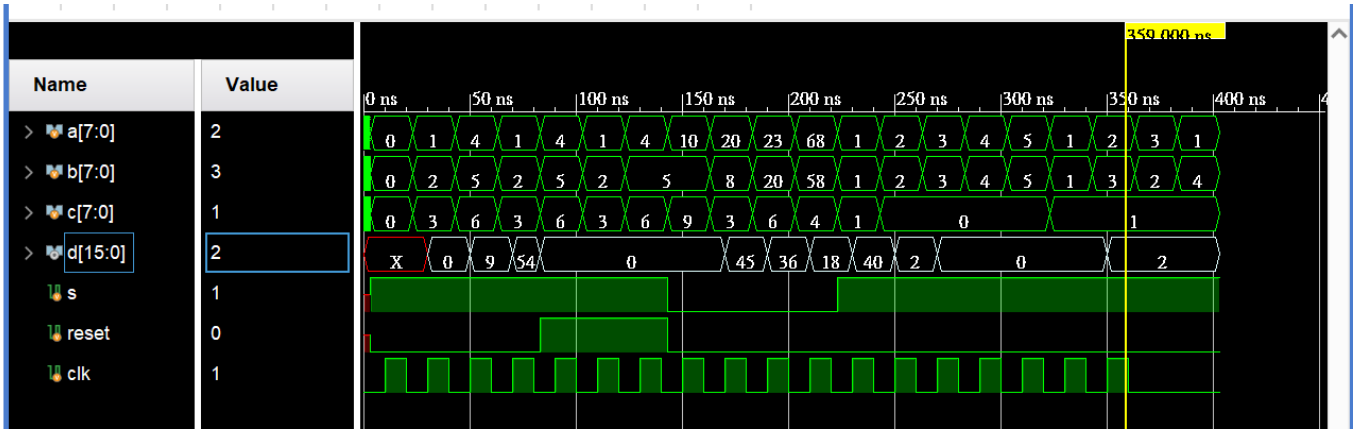
pipe



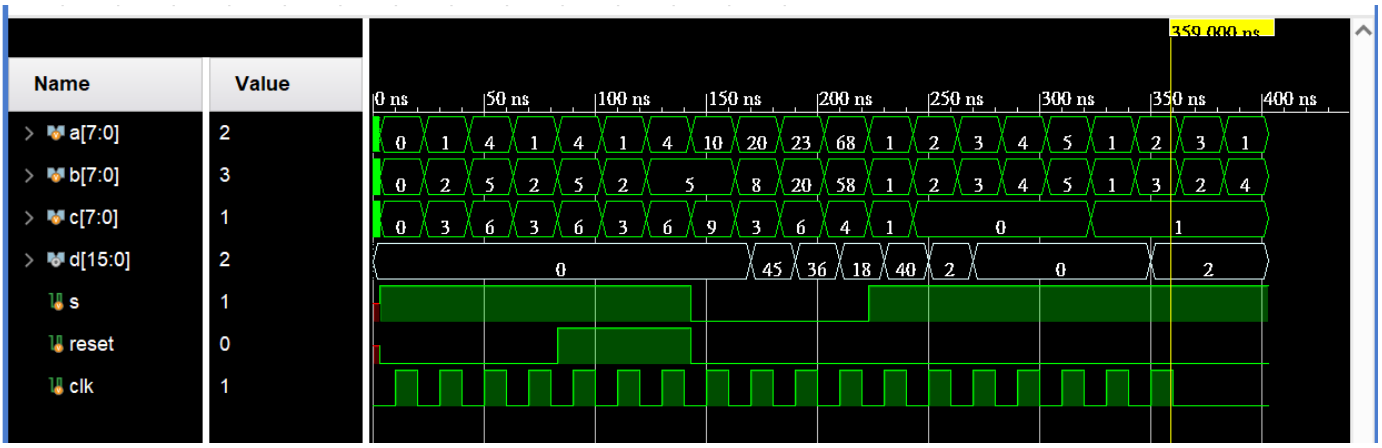
pipe using clock gating

二、 Xilinx Vivado

1. Behavior 波型與解釋



2. Post-implement 波型與解釋



3. Summary-Overview

(next page)

Project Summary

Overview | Dashboard

Synthesis

Status:	✓ Complete
Messages:	! 1 warning
Part:	xc7z020clg484-1
Strategy:	Vivado Synthesis Defaults
Report Strategy:	Vivado Synthesis Default Reports

Implementation

Summary | Route Status

Status:	✓ Complete
Messages:	No errors or warnings
Part:	xc7z020clg484-1
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

DRC Violations

Summary: ! 2 critical warnings

! 1 warning

Implemented DRC Report

Timing

Setup | Hold | Pulse Width

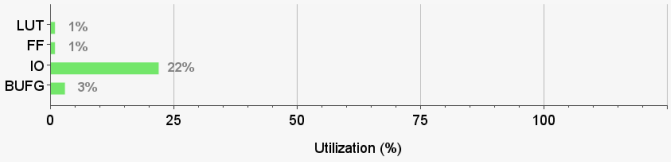
Worst Negative Slack (WNS):	3.154 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	16

Implemented Timing Report

Utilization

Post-Synthesis | **Post-Implementation**

Graph | Table



Power

Summary | On-Chip

Total On-Chip Power:	**0.121 W**
Junction Temperature:	**26.4 °C**
Thermal Margin:	58.6 °C (4.9 W)
Effective ϑJA:	11.5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report