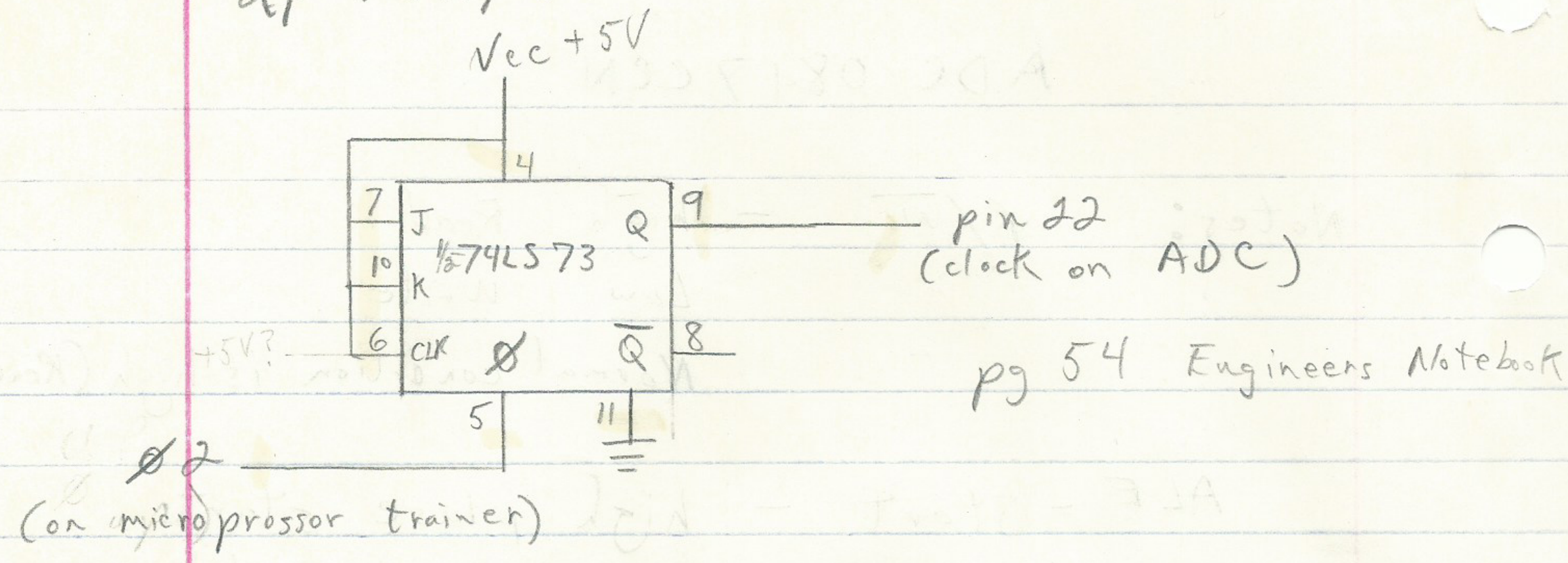
This circuit is a divide-by-two. Input 1 MHz from clp & outputs 500 kHz



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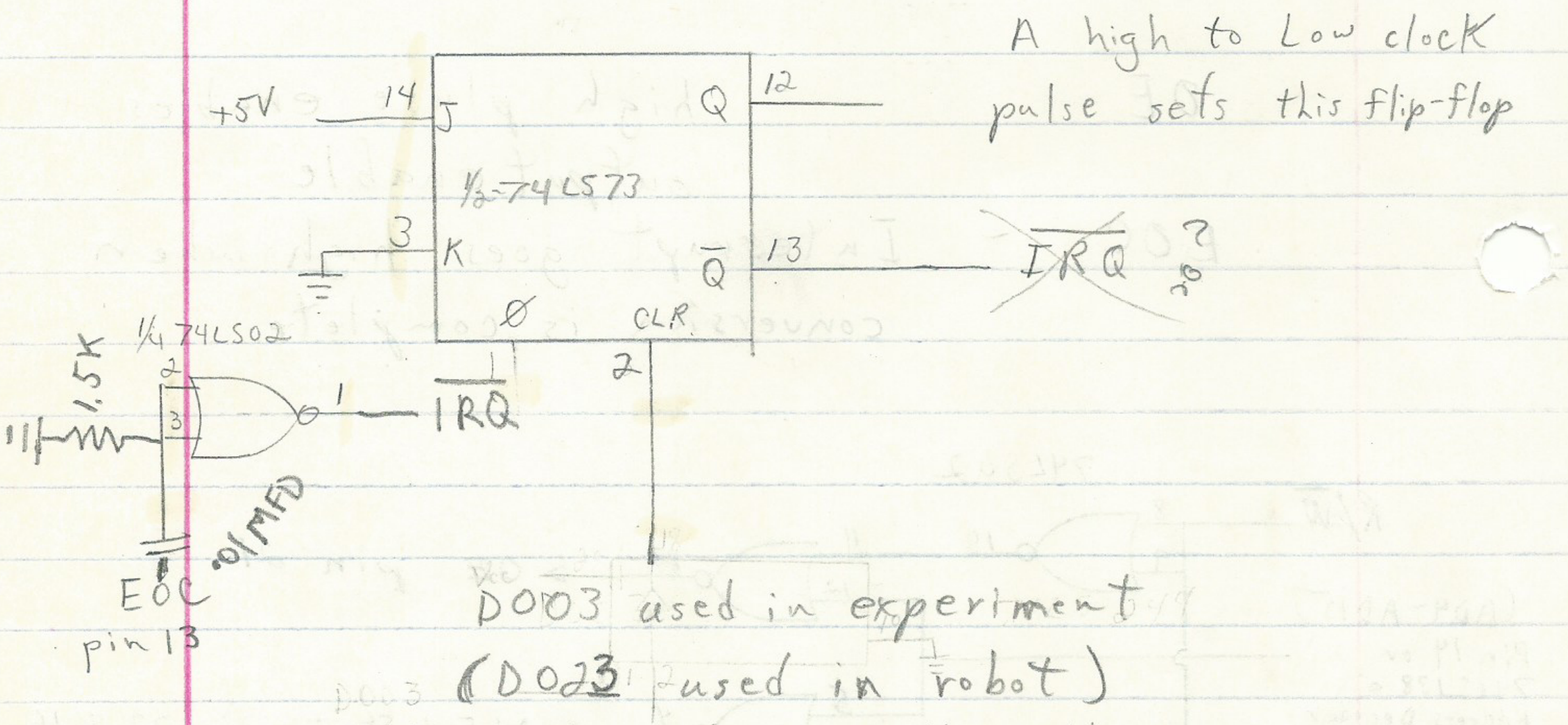

Note: A low pulse from the address decoder clears the flip-flop so it does not call for a interupt.

Note: Disconnected 74LS73 from $\overline{IRQ}$ & reconnected through capacitor as shown.