# FISA 1.0 - Instruction Set Architecture

**Overview:**
FISA (Fast Instruction Set Architecture) 1.0 is a custom ISA built to demonstrate low-level programming concepts. It features registers, memory, arithmetic, bitwise operations, jumps, and string support. This version provides a solid foundation for execution of assembly-like instructions without graphics.

**Registers:**
- 16 Integer Registers (R0 - R15)
- 16 String Registers (S0 - S15)

**Memory:**
- 512 RAM elements (addressable memory slots)

## Instruction Set (Core):

| Instruction | Description |
|---|---|
| MOV | Move value between registers or memory |
| ADD | Add values |
| SUB | Subtract values |
| MUL | Multiply values |
| DIV | Divide values |
| AND | Bitwise AND |
| OR | Bitwise OR |
| XOR | Bitwise XOR |
| NOT | Bitwise NOT |
| SHL | Shift left |
| SHR | Shift right |
| LOAD | Load from memory to register |
| STORE | Store register value to memory |
| CALL | Call a subroutine |
| RET | Return from subroutine |
| HLT | Halt execution |
| SHOW | Display output (e.g., ASCII values for text) |

**Notes:**
- CALL/RET allow basic subroutine handling.
- No direct JMP in 1.0 (will come in 2.0).
- Graphics instructions are not part of 1.0.

**Made By Me, and got some help from CHATGPT!!!**

*FISA Graphics Extension will be published soon, as it is still being worked on.*