8-bit ALU Design using eSim and Verilog

Objective:
The aim of this project is to design, simulate, and verify an 8-bit Arithmetic Logic Unit (ALU) using eSim, Verilog, and related open-source EDA tools. The ALU supports multiple arithmetic and logical operations including Addition, Subtraction, AND, OR, XOR, Inversion, XNOR, NOR, NAND, Left Shift, Right Shift, Left Rotation, and Right Rotation.

Circuit Schematic:
The ALU design consists of an 8-bit data path with control signals for selecting operations. Each operation is implemented using combinational logic blocks such as adders, multiplexers, and logic gates. The circuit was first designed using eSim and Verilog HDL. The Verilog files were simulated using Icarus Verilog and GTKWave for waveform visualization.

Simulation Results:
Due to certain limitations with eSim's mixed-signal simulator (ngspice-verilog interface), the functional verification was performed using Icarus Verilog (iverilog) and GTKWave. The results successfully demonstrated correct behavior for all ALU operations based on control input selection. Synthesis was performed using Yosys to verify gate-level implementation, and a corresponding ngspice model was generated. Additionally, the design was implemented and verified using Xilinx Vivado for hardware synthesis validation.

GitHub Repository:
https://github.com/subh2027/eSim_Marathon_2025

README Description:
This repository contains the complete project files for the 8-bit ALU designed using eSim and Verilog.
All project materials are organized within the ZIP file provided.

ZIP File Contents:
- Verilog Source Codes
- Testbench Files
- Simulation Scripts for Icarus Verilog and GTKWave
- Yosys Synthesis Scripts
- Generated Ngspice Models
- Vivado Implementation Files
- Documentation (PDF Report and README)

Features Implemented:
1. Addition
2. Subtraction
3. AND
4. OR
5. XOR
6. Inversion
7. XNOR
8. NOR
9. NAND
10. Left Shift
11. Right Shift
12. Left Rotation
13. Right Rotation

Tools Used:

- eSim
- Ngspice
- Icarus Verilog
- GTKWave
- Yosys
- Vivado

Conclusion:
The 8-bit ALU was successfully designed, simulated, and synthesized using both open-source and proprietary tools. Functional verification confirmed correct operation across all implemented arithmetic and logic functions. This project demonstrates the design flow from RTL coding to gate-level synthesis and mixed-signal model generation using eSim and supporting EDA tools.