Nisha Brahmankar | **16D070019**
Electrical Engineering | **Dual Degree (B.Tech. + M.Tech.)**
Indian Institute of Technology, Bombay | **Gender: Female**
Specialization: Communication & Signal Processing | **DOB: 04-08-1998**

Examination	University	Institute	Year	CPI / %
Graduation	IIT Bombay	IIT Bombay	2021	[redacted]
Intermediate	Maharashtra HSC	LVH Jr College, Nashik	2016	88.92%
Matriculation	Maharashtra SSC	RJEM School, Nashik	2014	94.80%

Academic Achievements

- Selected for a **fully funded** internship at VLSI Design and Education Center, The University of Tokyo, Japan *('19)*
- Invited as a speaker to **FOSSASIA** *Open Source Conference* in Singapore to present recent progress in *OpenStack* *('20)*
- JEE Main - All India **99.68** Percentile among 1.2M | JEE Advanced - All India **98.85** Percentile among 0.2M *('16)*
- Achieved state-level **2nd rank** in the Tilak Maharashtra Vidyapeeth Mathematics Examination *('12)*
- Received Maharashtra Talent Search Examination (MTSE) scholarship for **3 consecutive years** *('12 -'14)*

Internship Experience

- **Hardware Implementation of Optimised CNN Algorithm** | **Hardware Internship at The University of Tokyo**
  Guide: Prof. Masahiro Fujita, Director, VLSI Design and Education Center, UTokyo, Japan *(May'19 - Jul'19)*
  ⋆ *Awarded* **Letter of Recommendation** *by the Director for excellent research, impeccable soft skills & quick adaption*
  - Optimised parallel computations in **CNN** using **mesh architecture**, **hamiltonian path** & synthesised using **Verilog**
  - Achieved **40%** reduction in computation time by overlapping **MAC** operation and data transfer in the mesh cells
  - Solved the data feeding problem and proved that performance of **AI** system can be close to theoretical upper bounds
  - Formulated relation between external memory **bandwidth** and **clock frequency** for speedup and simplification

- **Upgrade Image Building Tool in OpenStack Cloud** | **Software Internship at OpenStack**
  Mentors: Dmitry Tantsur & Illya Etingof, Principal Software Engineer, Red Hat, Germany *(May'19 - Aug'19)*
  ⋆ *Awarded* **Letter of Recommendation** *by mentor for valuable contributions and strong passion for technology*
  - Selected among **800+** global applicants in **Outreachy**, an internship program to promote diversity in Tech & FOSS
  - Added **3.1k+** lines of code to upgrade *ironic-python-agent* - a python service which runs in a **temporary ramdisk** and provides **remote access**, **in-band hardware control** & **hardware introspection** to other OpenStack submodules
  - Consolidated existing image building tools in **ironic**, a program that provisions **Bare Metal** Machine in the cloud

Research and Development Experience

- **Energy Efficient Core Design** | **Master's Thesis** *(Jun'20 - Ongoing)*
  Guide: Prof. Virendra Singh, Electrical Engineering, IIT Bombay
  - Conducted extensive literature survey in exploiting ways to achieve energy efficient **Out-of-Order** & **In-Order** cores
  - Implementing **In-Order** core design that alters **scheduling policy** to improve performance and energy efficiency
  - Modifying the pipeline structure to implement **separate pipelines** for **critical**, **ready** and **non-ready** instructions

- **Superscalar Processor Design** | **Project in Computer Architecture** *(Jan'19 - May'19)*
  Guide: Prof. Virendra Singh, Electrical Engineering, IIT Bombay
  - Designed a **16-bit** superscalar RISC processor with **15** diverse instructions in **VHDL** and tested it on **FPGA** board
  - Exploited **ILP** with **Out-of-Order** pipeline and used 2-bit dynamic **branch predictor** & **64-bit** set associative **cache**
  - Implemented **Multi-Cycle Processor** and **Pipelined Processor** with **6-stage** pipeline design of the same ISA
  - Achieved **CPI** close to **1** with **Hazard Mitigation** techniques like data forwarding and static branch prediction

Key Projects

- **Real Time Vowel Classification** | Digital Signal Processing Lab | Course Project *(Spring 2019)*
  - Achieved **real-time** vowel classification robust to both male and female voice using **Digital Signal Processor**
  - Performed **512-point FFT** on a moving window and analysed the **frequency spectrum** to classify the vowel
  - Attained **90%** accuracy with vowel utterances from diverse speakers after deploying on **stereo codec** and DSP

- **Video Cartoonification** | Digital Image Processing | Course Project *(Autumn 2019)*
  - Applied **Edge Tangent Flow** (ETF) and **Flow-based Bilateral Filter** (FBL) techniques to cartoonify video clips
  - Achieved **77%** faster average time and **robustness to noise** compared to per-image cartoonification approach

- **Aberration Free Audio Systems** | Digital Signal Processing | Course Project *(Spring 2019)*
  - Contributed to the **Make in India** initiative and proposed application of speech comprehensibility in hearing aids
  - Applied **Formant Equalisation** and **Wide Dynamic Range Compression** (WDRC) at playback to improve speech
  - Conducted randomised user survey and **85%** of the users reported an improved audio perception and comfort
- **Honk Analyser to Curb Noise Pollution** | Electronic Design Lab | Course Project *(Spring 2019)*
  - Fabricated a **vehicle-powered** & **tamper-proof** prototype hardware device for tracking honk count of a car in traffic
  - Rectified noise using **Butterworth** & **Bandpass** filters and developed frequency & amplitude comparison techniques
  - Processed sensor data on **TIVA** microcontroller to detect horn & used **ESP8266** to transmit horn count to web server
- **Walkie Talkie** | Analog Circuits Lab | Course Project *(Spring 2018)*
  - Designed a walkie talkie system consisting of **audio amplifier**, **frequency modulator**, transmitter; using analog ICs
  - Achieved audio amplification using feedback & snubber circuits and frequency modulation using **LC oscillatory** circuit
- **Digital Reaction Time Calculator** | Digital Systems | Course Project *(Spring 2018)*
  - Developed a game that displays react time of user on an LCD screen and implemented it on **Altera CPLD** board
  - Constructed switch **debouncer**, random number generator and LCD controller in **VHDL** using **RTL** abstraction
- **Automated Waste Segregator** | Institute Technical Summer Project *(May'17 - Jun'17)*
  - Architected and assembled a low-cost, **automated three-tier bin** within a budget of **₹3k** for waste segregation
  - Implemented **Magnetic Induction** and **Capacitive Touch Sensing** to differentiate among metallic, wet & dry waste
- **Modelling Non-idealities in FinFET** | Research Project | *Guide: Prof. Udayan Ganguly* *(May'18)*
  - Analysed Line Edge Roughness and Metal Grain Granularity with their effects on **threshold voltage** of FinFETs
  - Examined the mathematical model and simulated 2-D structures of LER affected FinFET using **TCAD Sentaurus**

Roles and Responsibilities

- **Teaching Assistant** | Digital Systems | *Prof. Virendra Singh, Electrical Engineering, IIT Bombay* *(Aug'20 - Present)*
  - Responsible for managing **course logistics** and assisting the professor in ensuring smooth functioning of the course
  - Assisting in designing and evaluating projects, tutorials and exams for a batch of **200+** undergraduate students
- **Institute Student Mentor** | *Student Mentor Programme, IIT Bombay* *(Aug'20 - Present)*
  - Selected (**1** of **108** in batch of **1000**) after rigorous screening based on overall performance, interview & peer reviews
  - Responsible to mentor a **group** of incoming freshers to adapt to life at IIT; guide them for their holistic development
- **Business Analyst** | **Internship at Dhanvikas** *(Nov'17 - Jan'18)*
  Received positive feedback from CEO extolling leadership, teamwork, business understanding and intuition
  - Part of the **founding team** for B2B enterprise providing end-to-end corporate finance solutions for SME businesses
  - Worked alongside consultant from **Bain, NY** office to define operating model and identify differentiated products
  - Developed **business model** & strategy by identifying white spaces and underserved market segments in SME-lending
- **Events Coordinator** | *Entrepreneurship Cell, IIT Bombay* *(Apr'17 - Jan'18)*
  - Organised **The Ten Minute Million**, India's first **Shark Tank** style pitching event in ESummit with **23k+** attendees
  - Scrutinised startup entries with the leading investors for the event which led to on-spot funding of **₹3.2 million**

Technical Skills

- **Programming Languages** C++, C, Python, VHDL, Verilog, Assembly, MATLAB, Embedded C, LaTeX
- **Software Tools** Intel Quartus, Xilinx Vivado, ModelSim, Git, MS Office, NGspice, TI CCS, SolidWorks
- **Hardware Platforms** DE0 Nano Board, Zynq ZedBoard, Tiva-C, Arduino, 8051, Altera CPLD

Relevant Courses

- **Architecture** Advanced Topics in Computer Architecture, Processor Design, Microprocessors
- **Electronics** Digital Systems, Analog Circuits, Electronic Design Lab, Electronic Devices and Circuits
- **Signal Processing** Image Processing, Digital Signal Processing, Speech Processing, Communication Systems
- **Others** Data Analysis & Interpretation, Probability & Random Processes, Fibre Optic Communications, Communication Networks, Power Systems, Applied Linear Algebra, Machine Learning

Miscellaneous

Sports
- Awarded **Bronze Medal** in **Squash** tournament at **Udghosh**, the sports festival of IIT Kanpur *('18)*
- Bagged 4th position in the inter-hostel Girls **Squash General Championship** in the institute *('17)*

Social
- Conceptualised **SHE** & **Nirbhaya**, the social initiatives of TechFest for women empowerment *('17)*

Events
- Organised tech-competitions like **NCrypt**, **Technofrenzy** in the Electrical Department festival, Aavriti *('17)*

Adventures
- Trekking in Sahyadris; Escapades at FujiQ Highlands in Japan; Travelled **8+** cities to explore culture of Japan

Scholastic achievements and extracurricular activities are not verified by the Placement Cell