Devesh Kumar | **16D070044**
Electrical Engineering | **Dual Degree (B.Tech. + M.Tech.)**
Indian Institute of Technology, Bombay | **Gender: Male**
Specialization: Microelectronics and VLSI | **DOB: 11-02-1997**

Examination	University	Institute	Year	CPI / %
Graduation	IIT Bombay	IIT Bombay	2021	[redacted]
Intermediate	CBSE	St Joseph Public School, Kota	2015	84.00%
Matriculation	CBSE	Delhi Public School, Patna	2013	9.6

ACADEMIC ACHIEVEMENTS

- Completed a minor in **Computer Sciences and Engineering** at IIT Bombay.
- Secured 99.1 percentile in JEE Mains 2016 among 1.2 million candidates.
- Ranked in top 1 percent among 2 lakh aspirants in JEE Advanced examination, 2016.
- Qualified for National Talent Search Exam (NTSE).
- Received certificate of high distinction in Australian National Chemistry Quiz.
- Qualified for first stage of National Mathematics Talent Contest, 2014.

INTERNSHIPS

- **Chicago Mercantile Exchange (CME) Group, Bangalore** [*May 19 - Jul 19*]
  Quant Research Team
  - **Movements in interest rate curve**: Identified the largest percentile movement of interest rate curve for given strategies using principal component analysis of the interest rate curves. This helps in testing the existing risk models so that they could perform better on extreme market events in the future.
  - **Margin offset analysis**: Developed R tool to calculate the margin offset at the currency level across currencies for all accounts. This tool provides benefit of margin reduction achieved by netting trades across currencies.
  - Developed a tool to calculate the **notional of synthetic trades** generated at curve level to mimic the delta profile of the account. This tool is used to reduce the no of actual trades and hence speed up the backtesting process.

- **Speed Labs, Mumbai**: [*Dec 17*]
  Software development and content team
  - Analyzed the software architecture from a user perspective and recommended new features.
  - Many of the recommended features were added to the platform; Improved the utility of the existing content by adding more patterns; Significantly improved the overall presentation and quality.

PROJECTS

- **Multitask Convolution Neural Network** [*Spring 20*]
  Guide: Virendra Singh | Electrical Engineering Department
  - Did a comprehensive literature review of MTCNN architecture which is used for facial recognition.
  - Suggested improvements to lower the computation so that it could be implemented on multiple FPGA.

- **Face Recognition** [*Autumn 18*]
  Fundamentals of Image Processing | Guide: Ajit Rajwade | Computer Science Department *Course project*
  - Developed a facial recognition program on Matlab based on fisher discriminant analysis and principal component analysis, did a comparison between them (using cropped Yale dataset). Achieved 88 percent accuracy
  - The program is capable of handling lighting and facial variation between the dataset and the input.

- **Syntactic sentence parsing using Recursive Neural Networks** [*Autumn 18*]
  Introduction to Machine Learning | Guide: Sunita Sarawagi | Computer Science Department *Course project*
  - Applied an RNN to build a parsed tree-structure based on the phrasal category prediction of the words.
  - Converted the Penn Treebank dataset to a binary form by chomsky normal form and unary collapsing.
  - Reduced the syntactic phrasal tags to 6 subcategories and used pre-trained word embeddings.

- **SAT Solver Program** [*Autumn 19*]
  Foundation of VLSI CAD | Guide: Virendra Singh | Electrical Engineering Department *Course project*
  - Implemented DPLL algorithm to solve NP-Complete boolean satisfiability problem in python.
  - Applied unit clause propagation & pure literal elimination to speed up program.

- **Backpropagation in Spiking Neural Network** [*Spring 20*]
  Neuromorphic Engineering | Guide: Udayan Ganguli | Electrical Engineering Department *Course project*
  - Applied back-propagation algorithm on a spiking neural network. Used MNIST data set for training.

- **Brent Kung Adder and Dadda Multiplier** [*Autumn 19*]
  VLSI Design | *Guide: Dinesh Sharma* | *Electrical Engineering Department* *Course project*
  - Coded 32 bit Brent Kung adder and 16 bit Dadda multiplier on VHDL and verified it using test-bench.
  - Created schematic of Brent Kung adder and performed layout of its components in Cadence Virtuoso.
- **Wireless Encrypted Messenger** [*Summer 18*]
  Guide: Madhav P. Desai | *Electrical Engineering Department*
  - Developed a messaging system to wirelessly exchange encrypted messages between two Krypton board.
  - Configured the keypad to take 32 key input including A-Z, backspace, space, enter and delete.
- **OTA Design and Layout** [*Autumn 19*]
  CMOS Analog VLSI Design | *Guide: Rajesh Zele* | *Electrical Engineering Department* *Course project*
  - Designed a 2-stage fully differential input & single ended output Operational Transconductance Amplifier (OTA) with telescopic cascode design in Cadence Virtuoso with 180 nm SCL technology node.
  - Performed its layout, and achieved 87dB DC gain and 70 degree phase margin post parasitic extraction.
- **Impedance Measurement Sensor** [*Spring 19*]
  Electronic Design Lab | *Guide: Pramod Murali* | *Electrical Engineering Department* *Course project*
  - Designed and fabricated a circuit to do frequency sweep analysis of a blackbox and to find its bode plot .
  - Configured a krypton board to automatically generate sinusoidal signal (20Hz - 20KHz).
- **RISC Architecture Implementation** [*Autumn 18*]
  Microprocessors | *Guide: Virendra Singh* | *Electrical Engineering Department* *Course project*
  - Designed a RISC based multicycle 16 bit processor using point to point communication infrastructure.
  - Coded a total of 14 instructions with three machine code instruction formats on VHDL and then demonstrated on an FPGA board. Did pipelining to reduce the CPI of the program.
- **Power Amplifier Design and Layout** [*Spring 19*]
  Solid State Microwave Devices | *Guide: Jayanta Mukherjee* | *Electrical Engineering Department* *Course project*
  - Designed a power amplifier using AFIC901N on Keysight ADS to get a gain of 20 dB at 520 MHz.
  - Developed a PCB layout, fabricated it on an FR4 substrate and tested it using a Network Analyser.
- **Reaction Time Calculator** [*Spring 18*]
  Digital Circuit Lab | *Guide: Madhav P. Desai* | *Electrical Engineering Department* *Course project*
  - Programmed a CPLD to calculate the reaction time of a user between a LED glowing and pressing of a react button and displaying the total score after five rounds on an LCD in real time.
  - Made it foolproof by disqualifying the user if he/she presses the button before the LED glows

POSITION OF RESPONSIBILITY

- **Manager | Events | Aavriti, 2018** [*Jan 18 - Mar 18*]
  Member of core team of Aavriti, 2018, Electrical Engineering Department Annual Fest at IIT Bombay
  - Headed a team of 8 members responsible for proper planning and execution of various technical events, with a footfall of over 500 students from different colleges all over Mumbai.
- **Teaching Assistant | Microprocessors** [*Ongoing*]
  - Assisting professor to evaluate 30+ 3rd year UG students, conduct tutorials, and manage logistics.

TECHNICAL SKILLS

- **Programming Languages**: C/C++, Python, Assembly, Matlab, R, Latex.
- **Circuit Simulation**: VHDL, Verilog, NGspice, LTspice, Eagle, Keil, Arduino, Cadence Virtuoso.

RELEVANT COURSES

- **Electrical**: VLSI Design, Processor Design, CMOS Analog VLSI Design, Testing & Verification of VLSI Circuits.
- **Computer Science**: Data Structures & Algorithms, Operating systems, Intro. to Machine Learning.

EXTRACURRICULAR ACTIVITIES

- Active participation in algorithmic coding contests on online judges like Codeforces (max rating Expert).
- Worked in the electrical division of team Shunya. Made a database of the products used in the house and characterized them according to energy needs. Participated in planning the lighting of the house.
- Actively contributed to the Green campus (NSS group). Made placard for proper identification of trees on the campus. Made motivational videos for people in their local language to encourage them to start gardening.
- Participated in VIII IIT Bombay national debate competition.