G O K A R A J U R A N G A R A J U

Institute of Engineering and Technology

(Autonomous Institute under JNTU Hyderabad)

II B Tech I Semester – 2021-22 – GR20 Regulation

DIGITAL LOGIC DESIGN

Answers to Problem Sheet 4

Unit IV (Synchronous Logic, Register and Counters)

Syllabus: **Synchronous Sequential Logic**: Sequential Circuits, latches, Flip-Flops, Analysis of clocked sequential circuits, State Reduction and Assignment, Design Procedure.

Registers and Counters: Registers, shift registers, Ripple Counters, Synchronous Counters, other counters.

---

1. Explain SR, D, JK, and T Flip flops with their characteristic tables.

Answer: The storage elements used in clocked sequential circuits are called flip flops. A flip flop is a binary cell capable of storing one bit of information. It has two outputs, one for the normal value and one for the complement values of the bit stored in it. A flip flop maintains a binary state until directed by a clock pulse to switch states. The difference among various types of flip flops are is in the number of inputs they possess and in the manner in which the inputs affect the binary state.

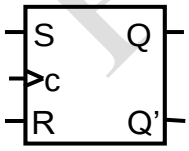
The most common types of flip flops are:

a. SR Flip Flop

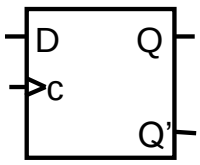
b. D Flip Flop

c. JK Flip Flop

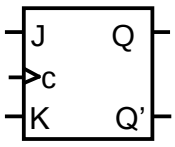
d. T Flip Flop



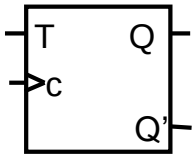
S	R	Q(t+1)	
0	0	Q(t)	No change
0	1	0	Clear to 0
1	0	1	Set to 1
1	1	?	Indeterminate



D	Q(t+1)	
0	0	Clear to 0
1	1	Set to 1



J	K	Q(t+1)	
0	0	Q(t)	No change
0	1	0	Clear to 0
1	0	1	Set to 1
1	1	$Q^1(t)$	Complement



T	Q(t+1)	
0	Q(t)	NO CHANGE
1	$Q^1(t)$	COMPLEMENT

The logical properties of a flip flop as described in the characteristic table can be expressed also algebraically with a characteristic equation.

For D flip flop ---- Q(t+1)=D

For JK flip flop --- $Q(t+1)=JQ^1+K^1Q$

For T flip flop ---- $Q(t+1)= TQ^1+T^1Q$

Where Q is the value of the flip flop output prior to the application of a clock edge.

2. Illustrate the analysis procedure for sequential circuit with a suitable example.

Answer: The behavior of a clocked sequential circuit is determined from the inputs, the outputs, and the state of its flip flops. The outputs and next state are both a function of the inputs and the present state.

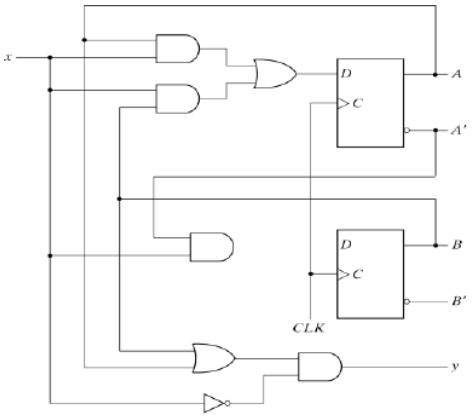
The analysis of a sequential circuit consists of obtaining a table or a diagram for the time sequence of inputs, outputs and internal states. It is also possible to write Boolean Expressions that describe the behavior of the sequential circuits.

The behavior of a clocked sequential circuit can be described algebraically by means of state equations.

A state equation specifies the next state as a function of the present state and inputs.

A state equation is an algebraic expression that specifies the condition for a flip flop state transition.

For Example: consider the following logic diagram,



The state equations for the above logic diagram will be:

$$A(t+1)=A(t)\,x(t) + B(t)\,x(t)$$

$$B(t+1)=A^1(t)x(t)$$

$$y(t)=[A(t)+B(t)]x^1(t)$$

The left side of the equation with (t+1) denotes the next state of the flip flop one clock edge later. The right side of the equation is a Boolean expression that specifies the present state and input conditions that make the next equal to 1.

They can be formally written as:

$$A(t+1)=Ax + Bx$$

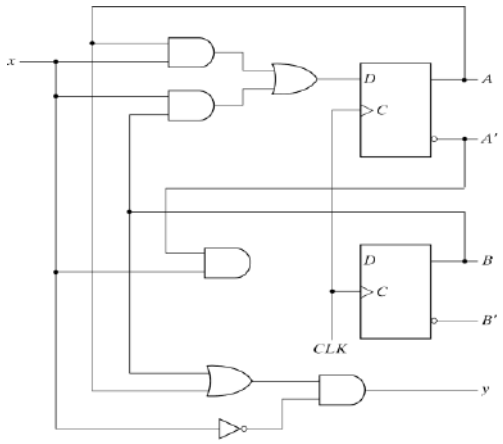
$$B(t+1)=A^1x$$

$$y(t)=[A+B]x^1$$

After, finding the flip flop next state equations, it is necessary to derive the state table of the logic diagram to present its behavior.

Present state		Input	Next state		Output
A	B	X	A	B	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

3. Analyze the following sequential circuit and draw state table and state diagram.



The state equations for the above logic diagram will be:

$A(t+1)=A(t)\,x(t) + B(t)\,x(t)$

$B(t+1)=A^1(t)x(t)$

$y(t)=[A(t)+B(t)]x^1(t)$

The left side of the equation with (t+1) denotes the next state of the flip flop one clock edge later. The right side of the equation is a Boolean expression that specifies the present state and input conditions that make the next equal to 1.

They can be formally written as:

$A(t+1)=Ax + Bx$

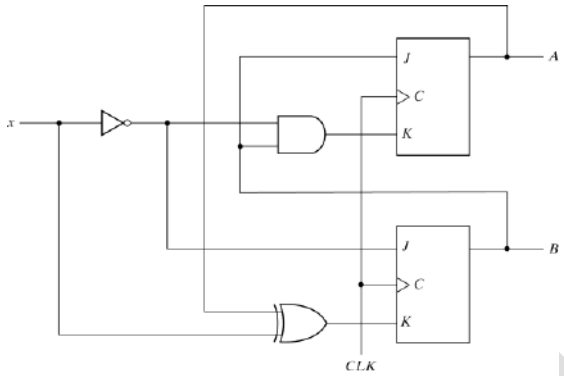
$B(t+1)=A^1x$

$y(t)=[A+B]x^1$

After, finding the flip flop next state equations, it is necessary to derive the state table of the logic diagram to present its behavior.

Present state		Input	Next state		Output
A	B	X	A	B	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

4. Analyze the following sequential circuit and draw state table and state diagram



The sequential circuit contains two JK flip flops A and B and one input x, and has no outputs and therefore the state table does not contain an output column.

The circuit can be specified by the flip flop input equations:

$J_A=B$ $K_A=Bx^1$

$J_B=x^1$ $K_B=A^1X+AX^1$

The characteristic equation of JK Flip Flop is $Q(t+1)=JQ^1+K^1Q$.

The characteristic equations for the flip flops in the circuit are obtained by substituting the names of the flip flops instead of Q in the characteristic equation.

So, we obtain: $A(t+1)= JA^1+K^1A$

$B(t+1)= JB^1+K^1B$

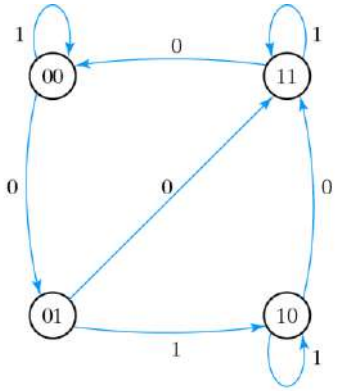
Substituting the values of JA and KA from the input equations, we obtain the state equation for A:

$A(t+1)= JA^1+K^1A=BA^1+(Bx^1)^1A=A^1B+AB^1+Ax$

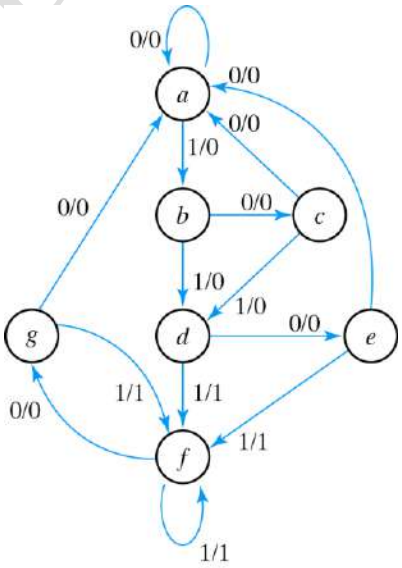
$B(t+1)= JB^1+K^1B=x^1B^1+(A^1X+AX^1)^1B=B^1x^1+ABx+A^1Bx^1$

Present state		Input	Next state	
A	B	X	A(t+1)	B(t+1)
0	0	0	0	1
0	0	1	0	0
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

The state table representation of above state table would be:



5. What is state reduction and assignment. Draw a reduced state diagram for the following state diagram.



The problem of state reduction is to find ways of reducing the number of states in a sequential circuit without altering the input-output relationship

The state table representation of the above state diagram will be of the following form:

Present state	Next state		Output	
	X=0	x=1	X=0	X=1
A	A	B	0	0
B	C	D	0	0
C	A	D	0	0
D	E	F	0	1
E	A	F	0	1
F	G	F	0	1
G	A	F	0	1

By observing the rows with similar entries, the similar states are reduced and the other entries with the removed state symbols are replaced with the similar states that are existing.

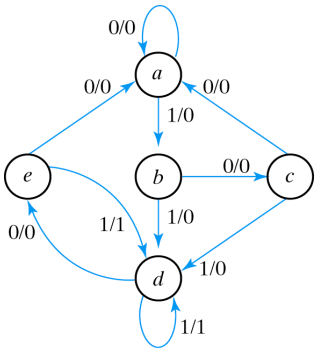
By following the above procedure till there are no more rows with similar entries.

The following reduced tables are obtained by following the above procedure:

Present state	Next stsate		Output	
	X=0	x=1	X=0	X=1
A	A	B	0	0
B	C	D	0	0
C	A	D	0	0
D	E	F	0	1
E	A	F	0	1
F	E	F	0	1

Present state	Next stsate		Output	
	X=0	x=1	X=0	X=1
A	A	B	0	0
B	C	D	0	0
C	A	D	0	0
D	E	D	0	1
E	A	D	0	1

After obtaining the reduced state table, it will be transformed into reduced state diagram



6. Illustrate the Design Procedure for Sequential circuits.

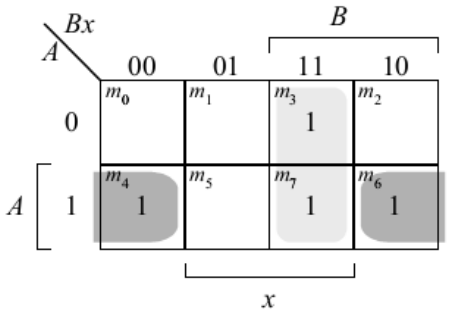
The design of a clocked sequential circuit starts from a set of specifications and culminates in a logic diagram or a list of Boolean functions.

The procedure for designing synchronous sequential circuits can be as follows:

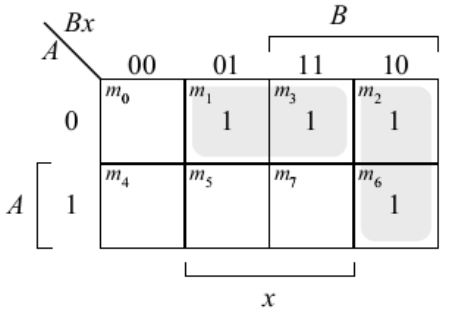
a. From the word description of the desired operation, derive a state diagram for the circuit.
b. Reduce the number of states if necessary.
c. Assign binary values to the states.
d. Obtain the binary coded state table.
e. Choose the type of flip flops to be used.
f. Derive the simplified flip flop input equations and output equations.
g. Draw the logic diagram.

7. Design a sequential circuit with two D Flip Flops, A and B, and one input, x. When x=0, the state of the circuit remains the same. When x=1, the circuit goes through the state transitions from 00 to 01 to 11 to 10 back to 00, and repeats.

Present state		Input	Next state	
A	B	x	A	B
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	1
1	1	1	1	0

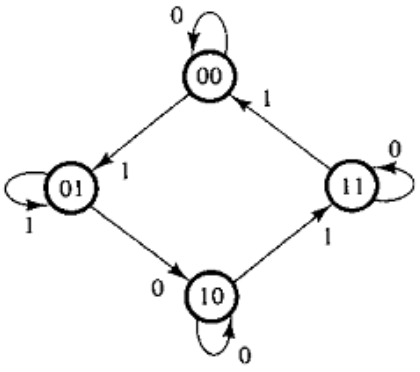


$$D_A = Ax' + Bx$$

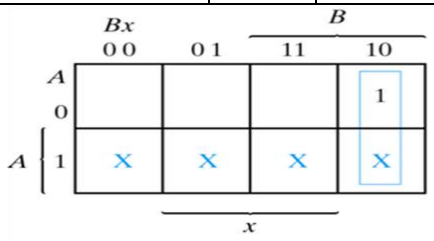


$$D_B = A'x + Bx'$$

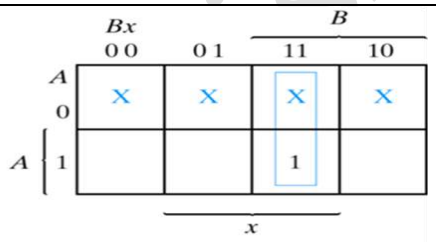
8. Design a sequential circuit for the following state diagram with JK Flip Flops.



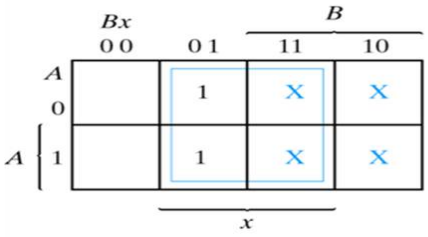
Present state		Input	Next state		Flip Flop Input Equations			
A	B	X	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1



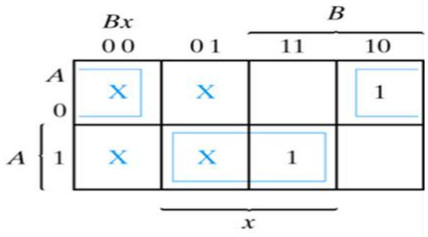
$J_A = Bx'$



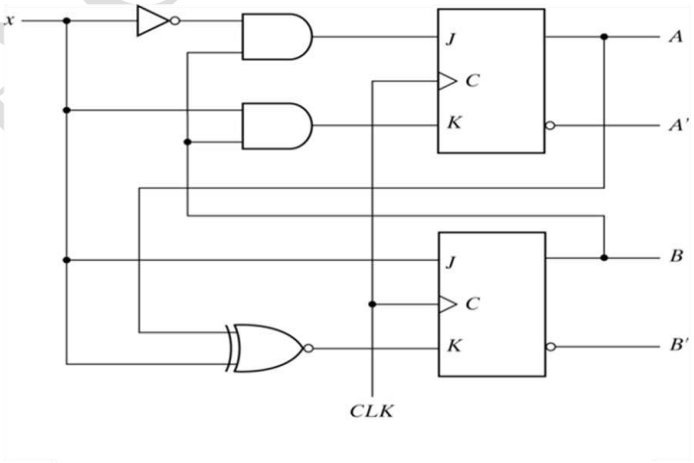
$K_A = Bx$



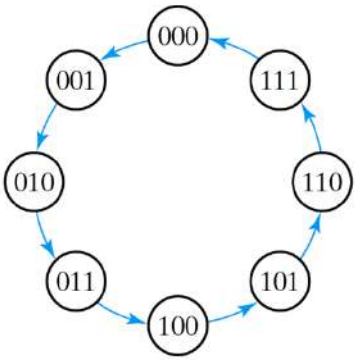
$J_B = x$



$K_B = (A \oplus x)'$



9. Design a sequential circuit for the following state diagram with T Flip Flops.



Present state			Next state			Flip Flop Inputs		
A2	A1	A0	A2	A1	A0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

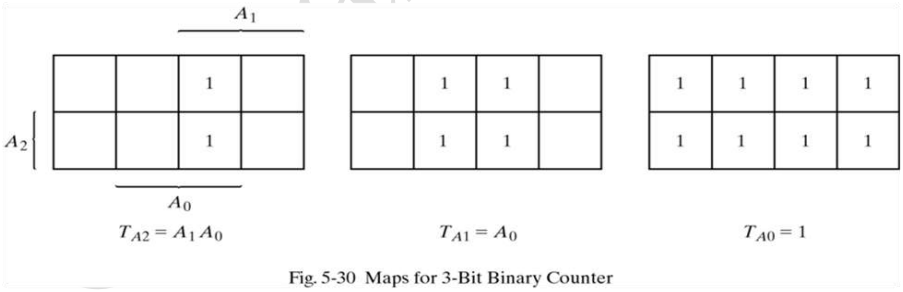
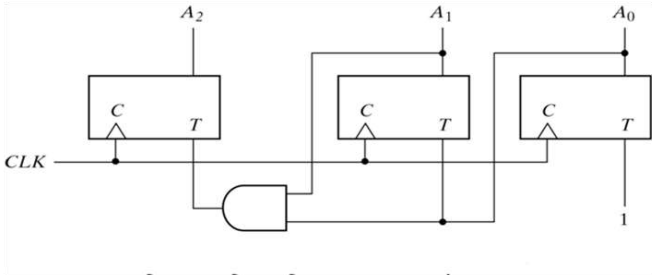


Fig. 5-30 Maps for 3-Bit Binary Counter



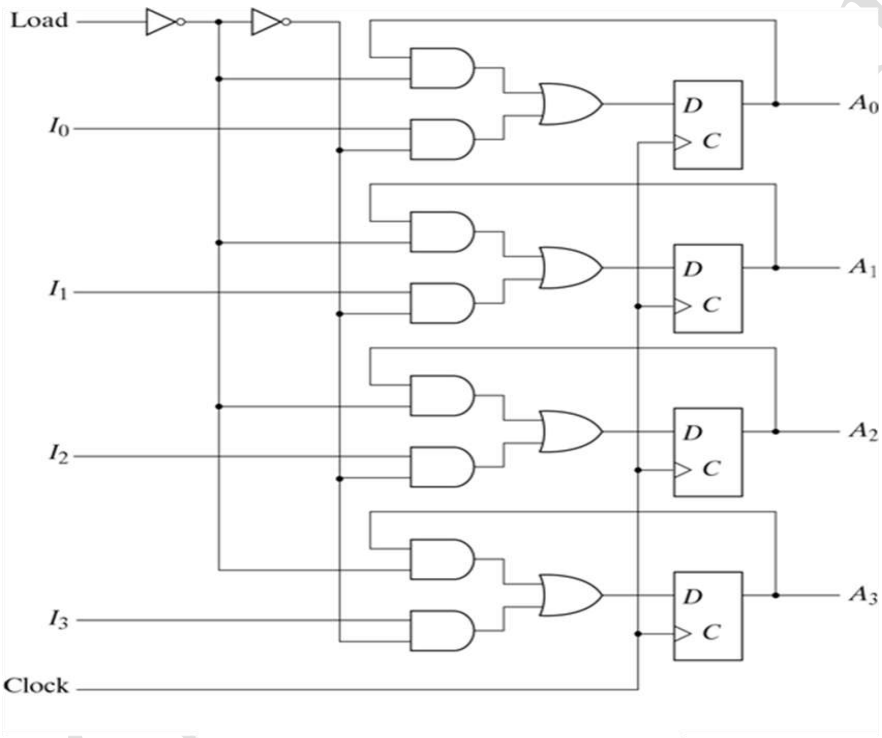
10. Draw the logic diagram for a 4-bit shift register with parallel load using D Flip flops.

    The transfer of new information into a register is referred to as loading the register.

    If all the bits of the register are loaded simultaneously with a common clock pulse, we say that the loading is done in parallel.

    For a register with parallel load, the load input determines whether the next pulse will accept new information or leave the information in the register intact.

    The transfer of information from the data inputs or the outputs of the register is done simultaneously with all four bits in response to a clock edge.

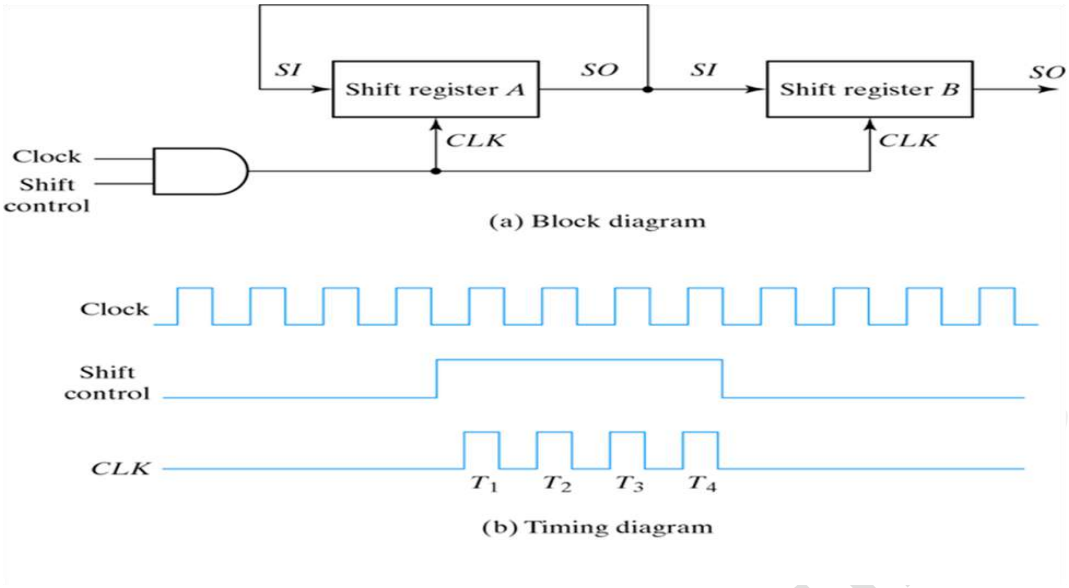


11. What is Serial Transfer? Design circuitry to accomplish serial transfer with shift registers.

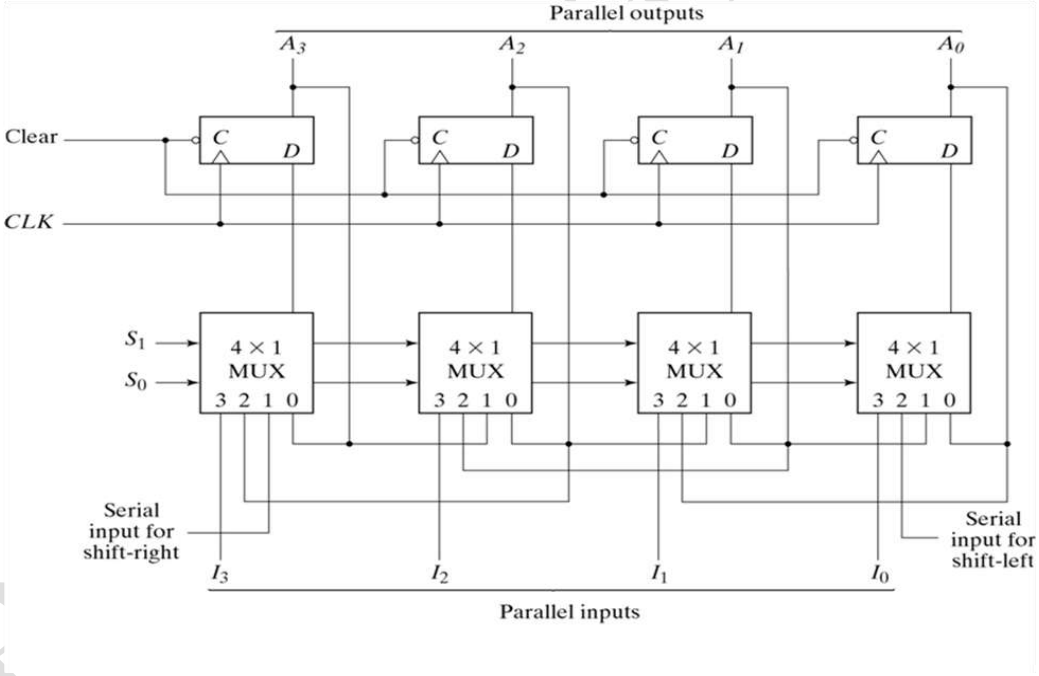
    A digital system is said to operate in a serial mode when information is transferred and manipulated one bit at a time.

    Information is transferred one bit at a time by shifting the bits out of the source register into the destination register. This is in contrast to parallel transfer where all the bits of the register are transferred at the same time.

    To attain serial transfer, the source and destination register are treated as shift registers with the serial output of source register is connected to the serial input of the destination register.



12. Draw the logic diagram for universal shift register.



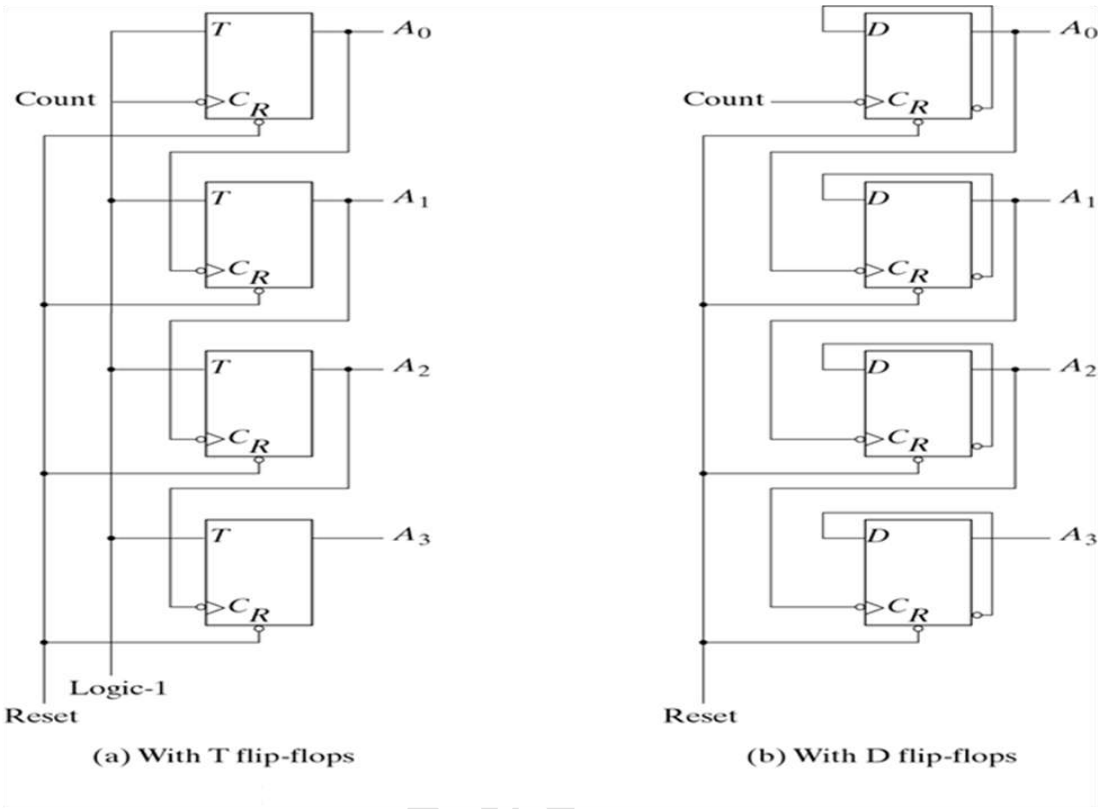
13. Design a Binary Ripple counter.

A binary ripple counter consists of a series connection of complementing flip-flops, with the output of each flip flop connected to the c input of the next higher order flip flop.

The flip flop holding the least significant bit receives the incoming count pulses.

The counter is connected with the D type or T type flip flops.

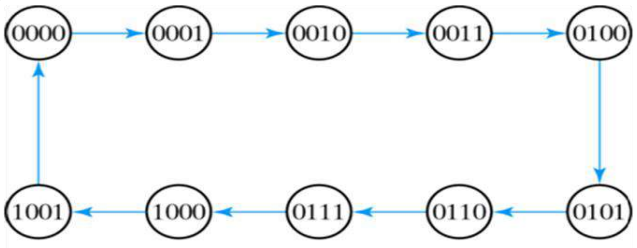
The output of each flip flop is connected to the C input of the next flip flop in sequence.



14. Design a BCD Ripple counter.

A decimal counter follows a sequence of ten states and return to 0 after the count of 9. Such a counter must have at least four flip flops to represent each decimal digit, since a decimal digit represented by a binary code with at least four bits.

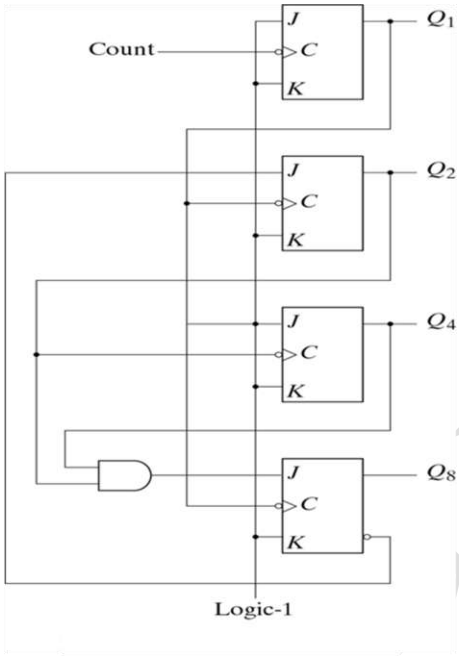
If a BCD Code is used, the sequence of states are as follows:



To verify the conditions result in the sequence required by BCD ripple counter, it is necessary to verify that the flip flop transitions indeed follows a sequence of states as specified by the state diagram.

- Q1 changes state after every clock pulse.

- Q2 complements every time Q1 goes from 1 to 0 as long as Q8 is 0.
- When Q8 becomes 1, Q2 remains at 0.
- Q4 complements every time Q2 goes from 1 to 0.
- Q8 remains at 0 as long as Q2 or Q4 is 0.
- When both Q2, Q4 become 1, Q8 complements when Q1 goes from 1 to 0.
- Q8 is cleared on the next transition of Q1.



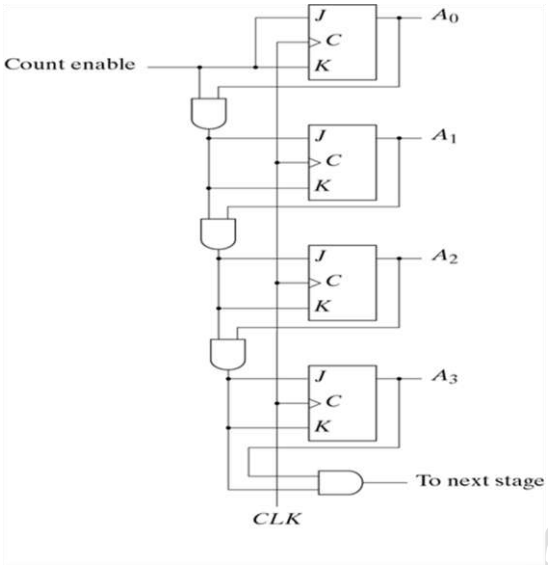
15. Design a 4 bit synchronous binary counter.

    In a Synchronous Binary Counter, the flip flop in the least significant position is complemented with every pulse.

    A flip flop in any other position is complemented when all the bits in the lower significant positions are equal to 1.

    Synchronous Binary Counters have a regular pattern and can be constructed with complementing flip flops and gates.

    The Synchronous Counters can be triggered with either positive or the negative clock edge.



16. Design a 4 bit synchronous BCD Counter with unused states.

Answer: BCD counter counts in binary coded decimal from 0000 to 1001 and back to 0000. Because of the return to 0 after a count of 9, a BCD counter does not have a regular pattern as in straight binary counter. The circuit for a BCD Counter can be obtained by normal design procedure.

The flip flop input equations can be simplified by means of maps. The unused states for minterms 10 to 15 are taken as don't care conditions.

Present State				Next State				Output	Flip Flop Inputs			
Q8	Q4	Q2	Q1	Q8	Q4	Q2	Q1	Y	TQ8	TQ4	TQ2	TQ1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

- $T_{Q1}=1$ $T_{Q2}=Q_8{}^1Q_1$ $T_{Q4}=Q_2Q_1$ $T_{Q8}=Q_8Q_1+Q_4Q_2Q_1$ $Y=Q_8Q_1$