G O K A R A J U R A N G A R A J U
Institute of Engineering and Technology
(Autonomous Institute under JNTU Hyderabad)
II B Tech I Semester – 2021-22 – GR20 Regulation

DIGITAL LOGIC DESIGN
Answers to Problem Sheet 3
Unit III (Combinational Logic)

Syllabus: **Combinational Logic**: Combinational Circuits, Analysis Procedure, Design Procedure, Binary Adder - Subtractor, Decimal Adder, Binary Multiplier, Magnitude Comparator, Decoders, Encoders, Multiplexers.

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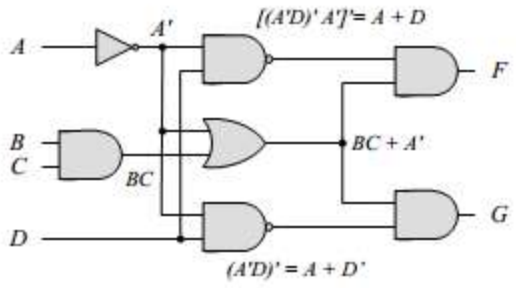
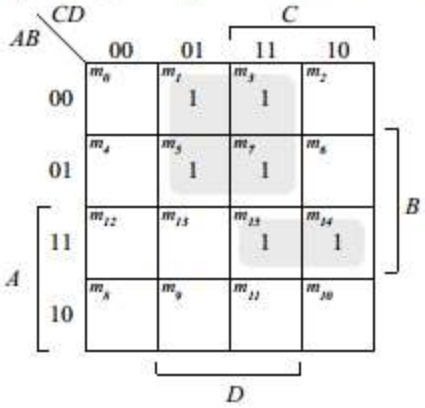
1. Obtain the simplified Boolean expressions for outputs F and G in terms of the input variables in the below circuit.

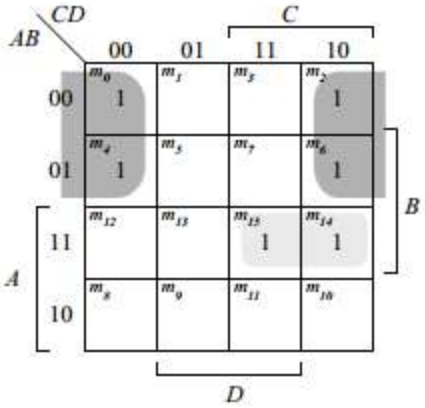


$F = (A + D)(A' + BC) = A'D + ABC + BCD + = A'D + ABC$

$F = (A + D')(A' + BC) = A'D' + ABC + BCD' = A'D' + ABC$



$F = A'D + ABC + BCD = A'D + ABC$



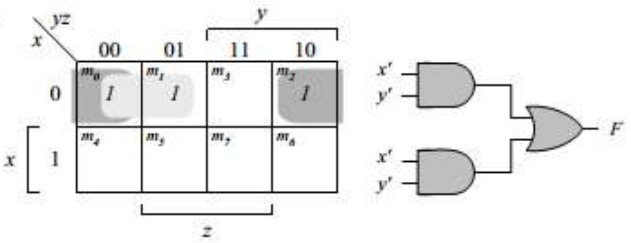
$G = A'D' + ABC + BCD' = A'D' + ABC$

2. Design a combinational circuit with three inputs and one output.
    a. The output is 1 when the binary value of the input is less than 3.

b. The output is 1 when the binary value of the input is an odd number.

(a)

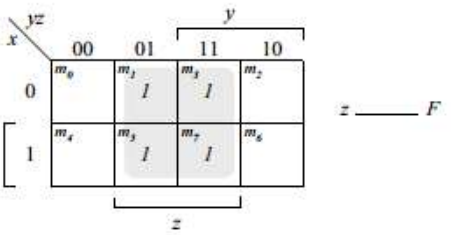
xyz	F
000	1
001	1
010	1
011	0
100	0
101	0
110	0
111	0



$F = x'y' + x'z'$

(b)

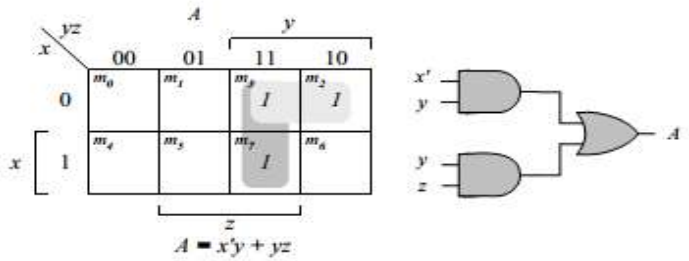
xyz	F
000	0
001	1
010	0
011	1
100	0
101	1
110	0
111	1

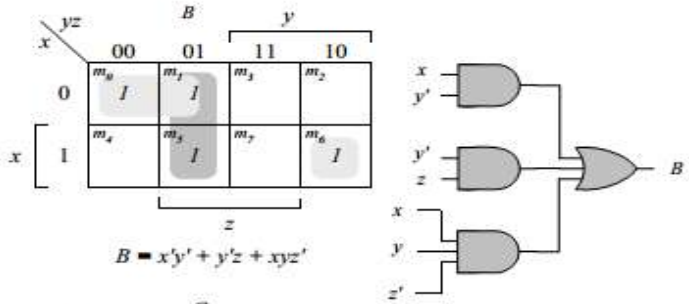


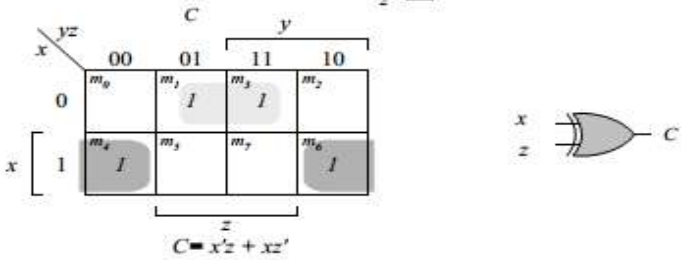
$F = z$

3. Design a combinational circuit with three inputs, x,y, and z, and three outputs, A,B, and C, when the binary input is 0,1,2, or 3, the binary output is two greater than the input. When the binary input is 4,5,6,7, the binary output is two less than the input.

xyz	ABC
000	010
001	011
010	100
011	101
100	001
101	010
110	011
111	100

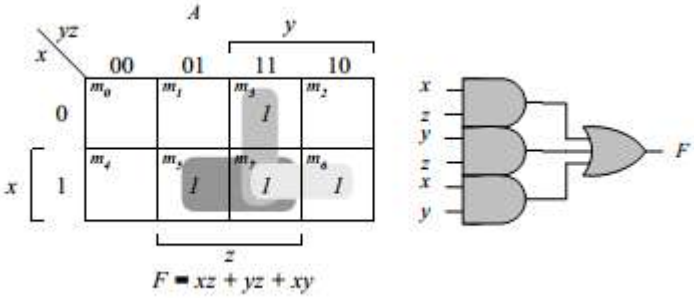






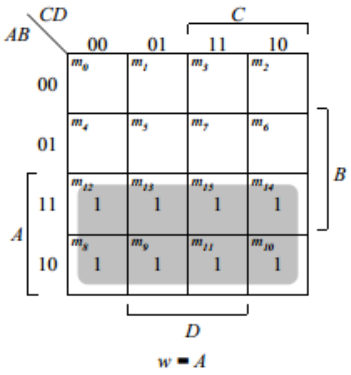
4. Design a 3-bit majority circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 other wise.

xyz	F
000	0
001	0
010	0
011	1
100	0
101	1
110	1
111	1

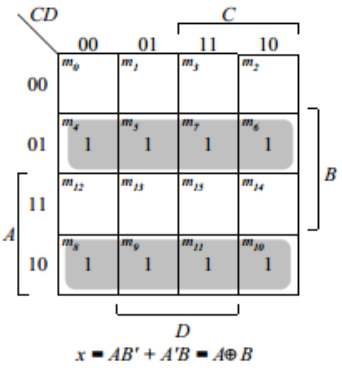


5. Design a combinational circuit with Ex OR gates that converts a four bit Gray code to a four bit binary number.

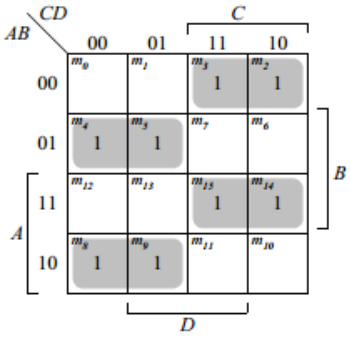
ABCD	wxyz
0000	0000
0001	0001
0011	0010
0010	0011
0110	0100
0111	0101
0101	0110
0100	0111
1100	1000
1101	1001
1111	1010
1110	1011
1010	1100
1011	1101
1001	1110
1000	1111



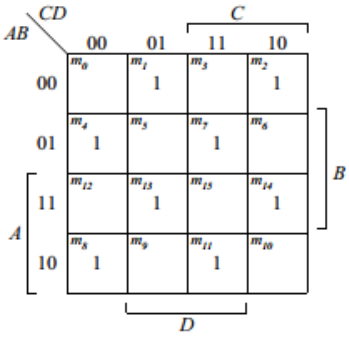
$w = A$



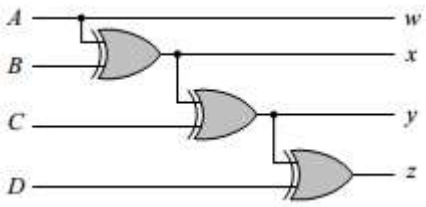
$x = AB' + A'B = A \oplus B$



$y = A'B'C\ A'BC' + ABC + AB'C'$
$= A'(A \oplus B) + A(B \oplus C)'$
$= A \oplus B \oplus C$
$= X \oplus C$

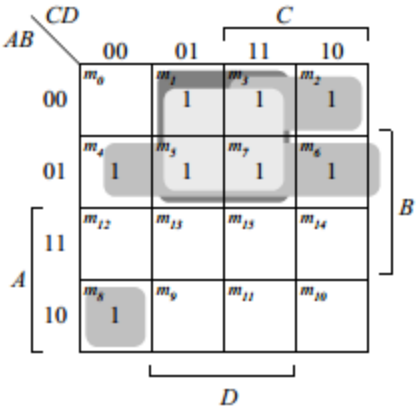


$z = A \oplus B \oplus C \oplus D$
$= y \oplus D$

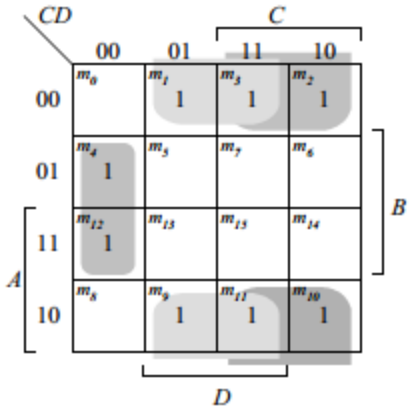


6. Design a combinational circuit that generates 2's complement of a given 4 bit binary number.

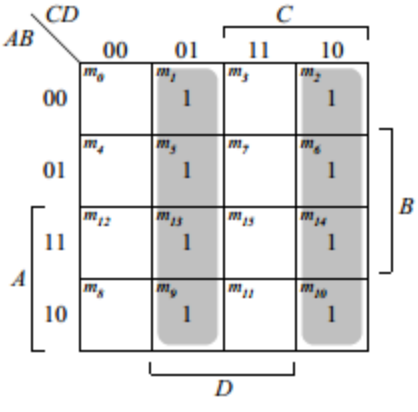
ABCD	wxyz
0000	0000
0001	1111
0010	1110
0011	1101
0100	1100
0101	1011
0110	1001
0111	1000
1000	1000
1001	0111
1010	0110
1011	0101
1100	0100
1101	0011
1110	0010
1111	0001



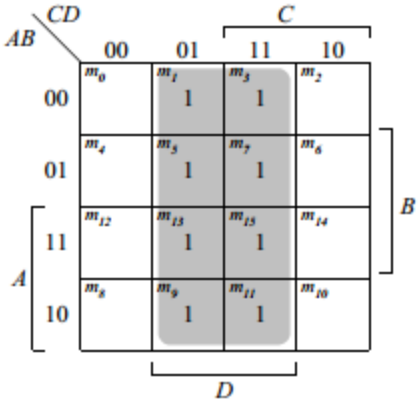
$w = A'(B + C + D) + AB'C'D'$
$= A \oplus (B + C + D)$



$x = B'(C + D) + CB'D'$
$= B \oplus (C + D)$

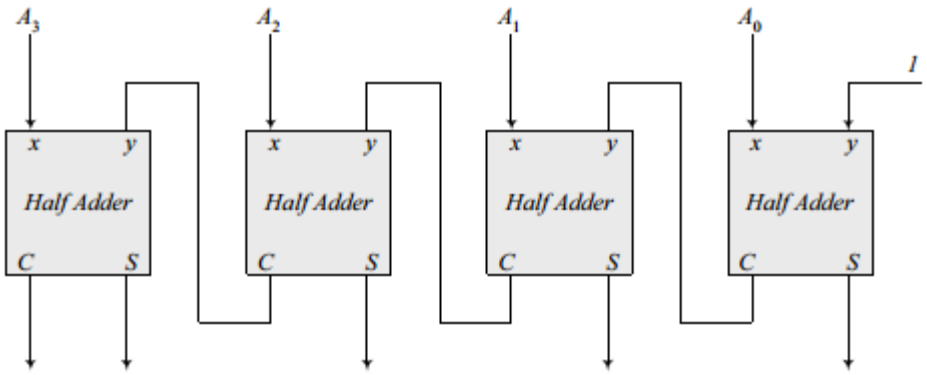


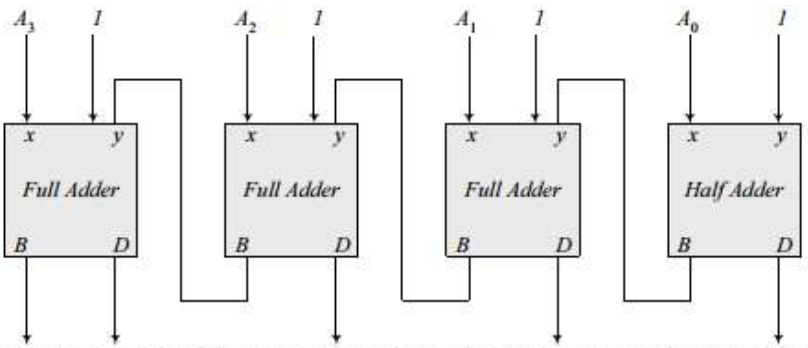
$y = CD' + C'D = C \oplus D$



$z = D$

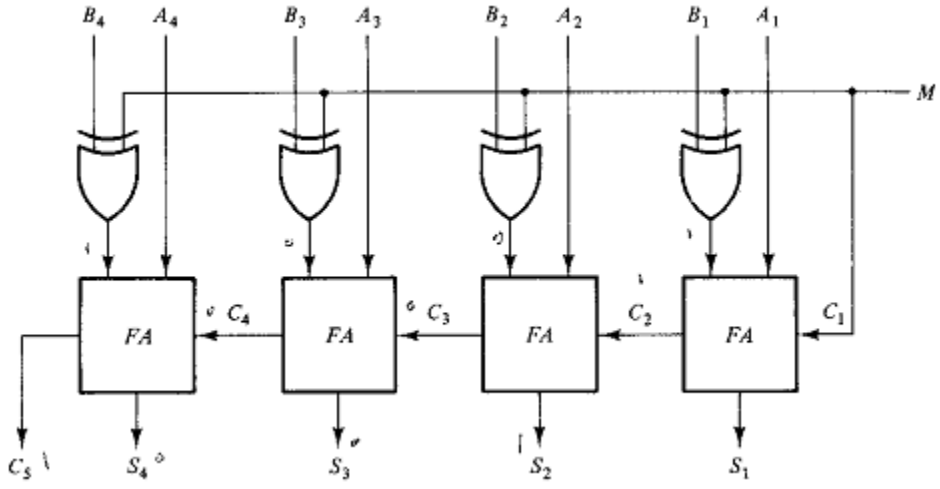
7. Using 4 Half adders, Design a four bit combinational circuit incrementer (a circuit that adds 1 to a four bit binary number), and a decrementer (a circuit that subtracts 1 from a four bit binary number).





Note: To decrement the 4-bit number, add -1 to the number. In 2's complement format (add F_h) to the number. An attempt to decrement 0 will assert the borrow bit.

8. Design a 4-bit binary adder subtractor for addition and subtraction of 2 four bit binary numbers.

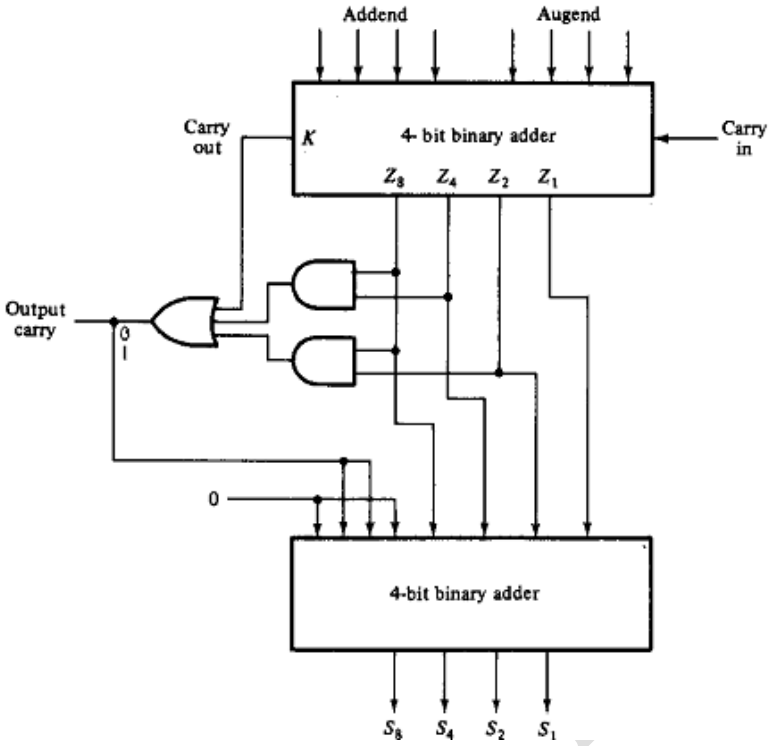


9. Design a 4 bit BCD Adder for addition of Decimal in BCD form.

Derivation of a BCD Adder

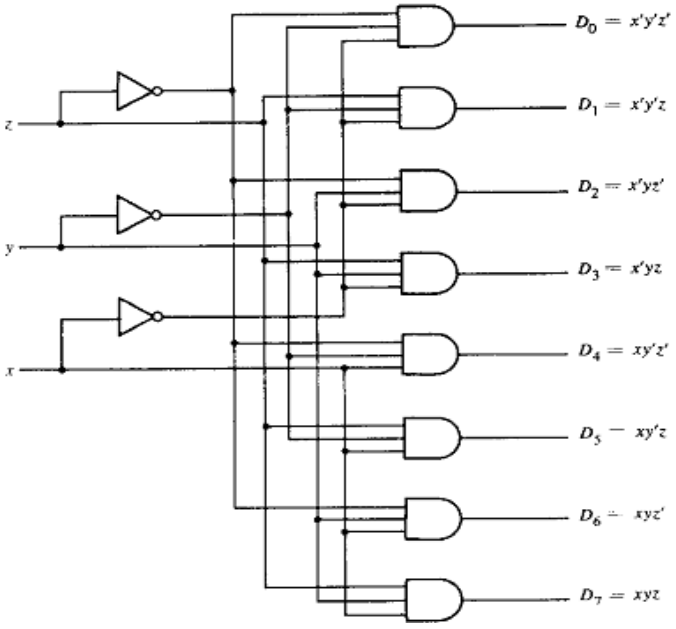
Binary Sum					BCD Sum					Decimal
K	Z_8	Z_4	Z_2	Z_1	C	S_8	S_4	S_2	S_1	
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	2
0	0	0	1	1	0	0	0	1	1	3
0	0	1	0	0	0	0	1	0	0	4
0	0	1	0	1	0	0	1	0	1	5
0	0	1	1	0	0	0	1	1	0	6
0	0	1	1	1	0	0	1	1	1	7
0	1	0	0	0	0	1	0	0	0	8
0	1	0	0	1	0	1	0	0	1	9
0	1	0	1	0	1	0	0	0	0	10
0	1	0	1	1	1	0	0	0	1	11
0	1	1	0	0	1	0	0	1	0	12
0	1	1	0	1	1	0	0	1	1	13
0	1	1	1	0	1	0	1	0	0	14
0	1	1	1	1	1	0	1	0	1	15
1	0	0	0	0	1	0	1	1	0	16
1	0	0	0	1	1	0	1	1	1	17
1	0	0	1	0	1	1	0	0	0	18
1	0	0	1	1	1	1	0	0	1	19

$$C = K + Z_8Z_4 + Z_8Z_2$$



10. What is a Decoder? Design a 2 X 4 Decoder with Basic gates.

    A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. If the n bit decode information has unused or don't care combinations, the decoder output will have fewer than 2^n outputs.

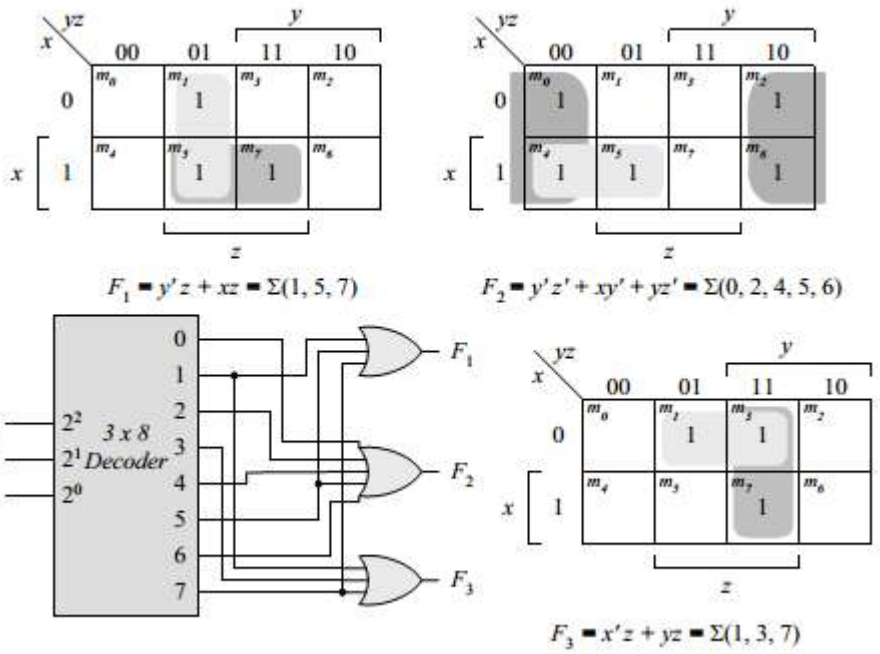


11. Using a Decoder and external gates, design the combinational circuit by the following three Boolean functions:

    F1=(y'+x)z

    F2=y'z'+xy'+yz'

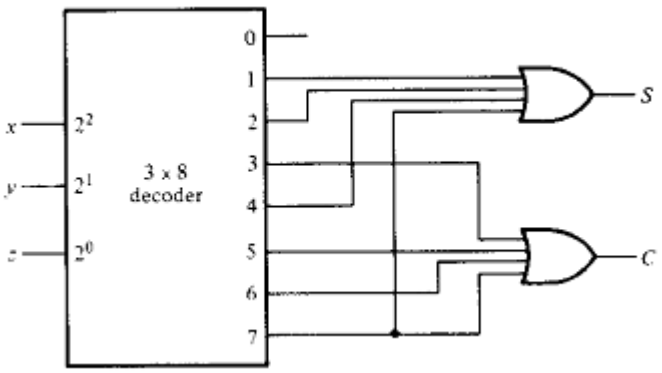
    F3=(x'+y)z



12. Implement a full adder circuit with decoder and OR gates.

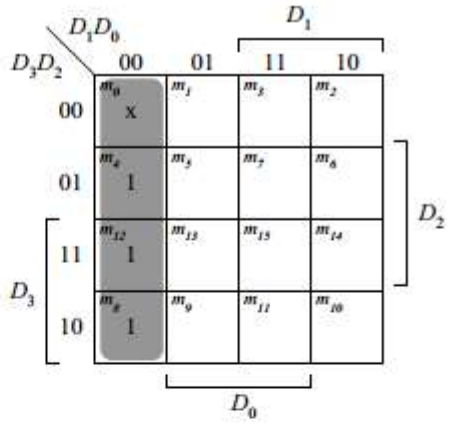
    For a full adder with three bits of information and two outputs like sum and carry, the Boolean functions for the outputs sum and carry can be derived from the truth table of the full adder and they are

$S(x, y, z) = \Sigma(1, 2, 4, 7)$
$C(x, y, z) = \Sigma(3, 5, 6, 7)$

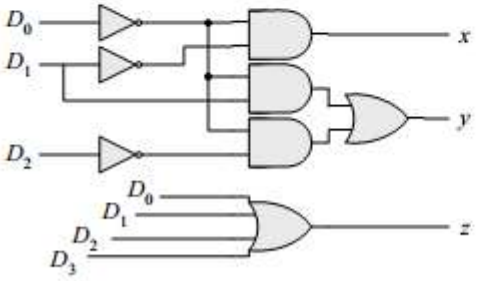


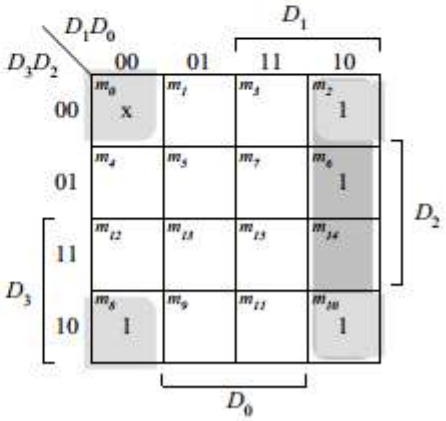
13. Design a four-input priority encoder with input D0 having the highest priority and input D3 the lowest priority.

Inputs $D_3\ D_2\ D_1\ D_0$	Outputs $X\ Y\ Z$
0 0 0 0	x x 0
x x x 1	0 0 1
x x 1 0	0 1 1
x 1 0 0	1 0 1
1 0 0 0	1 1 1



$v = D_0 + D_1 + D_2 + D_3$





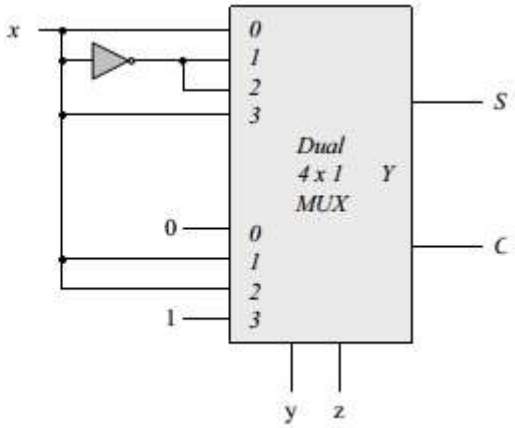
$y = D'_0D_1 + D'_0D'_2$

14. Implement a full adder with two 4 X 1 Multiplexers

$S(x, y, z) = \Sigma(1, 2, 4, 7)$
$C(x, y, z) = \Sigma(3, 5, 6, 7)$

S	I_0	I_1	I_2	I_3
x'	0	1	2	3
x	4	5	6	7
	x	x'	x'	x

C	I_0	I_1	I_2	I_3
x'	0	1	2	3
x	4	5	6	7
	0	x'	x'	1



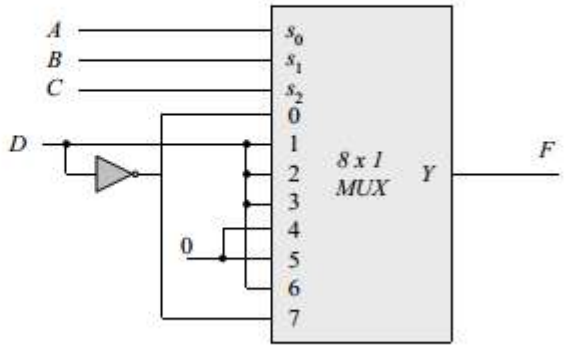
15. Implement the following Boolean functions with a multiplexer:

a. F = ∑(0, 2, 5, 7, 11, 14)

b. F = ∏(3, 8, 12)

(a) $F = \Sigma\,(0, 2, 5, 7, 11, 14)$

Inputs ABCD	F	
0000	1	$F = D'$
0001	0	
0010	1	$F = D$
0011	0	
0100	0	$F = D$
0101	1	
0110	0	$F = D$
0111	1	
1000	0	$F = 0$
1001	0	
1010	0	$F = 0$
1011	0	
1100	0	$F = D$
1101	1	
1110	1	$F = D'$
1111	0	

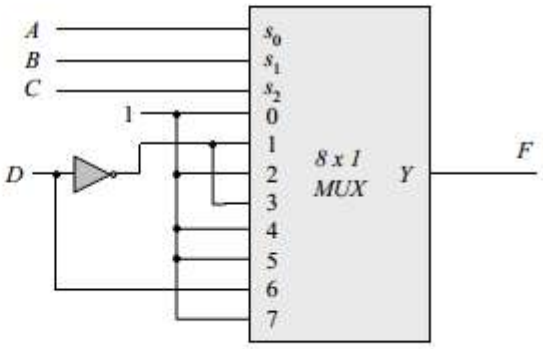


(b) $F = \Pi\,(3, 8, 12) = (A' + B' + C + D)(A + B' + C' + D')(A + B + C' + D')$

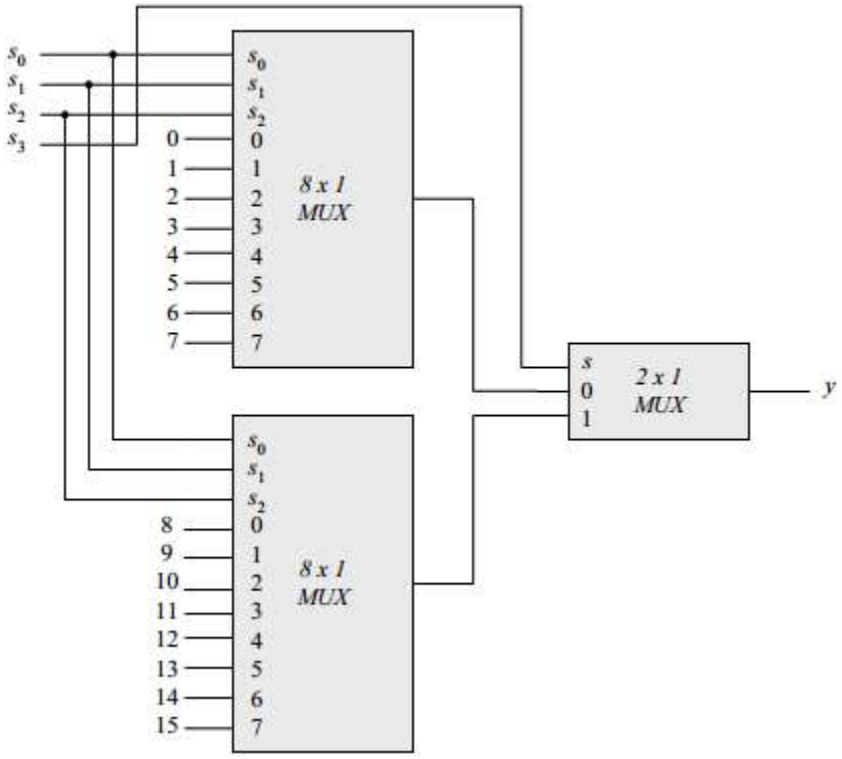
$F' = ABC'D' + A'BCD + A'B'CD = \Sigma(12, 7, 3)$

$F = \Sigma(0, 1, 2, 4, 5, 6, 8, 9, 10, 11, 13, 14, 15)$

Inputs ABCD	F	
0000	1	$F = 1$
0001	1	
0010	1	$F = D'$
0011	0	
0100	1	$F = 1$
0101	1	
0110	1	$F = D'$
0111	0	
1000	1	$F = 1$
1001	1	
1010	1	$F = 1$
1011	1	
1100	0	$F = D$
1101	1	
1110	1	$F = 1$
1111	1	



16. Construct a 16X 1 multiplexer with two 8 X 1 multiplexers and one 2 X 1 multiplexers.



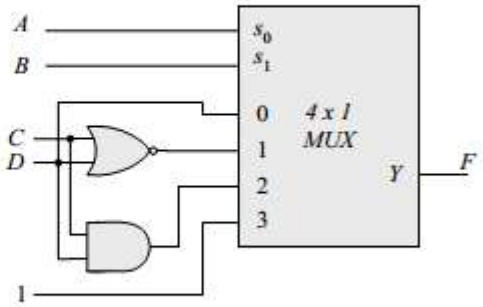
17. Implement the following Boolean functions with a 4 X 1 multiplexer and external gates.

    a. F(A,B,C,D)= ∑(1,3,4,11,12,13,14,15)

    b. F(A,B,C,D)= ∑(1,2,4,7,8,9,10,11,13,15)

(a)

Inputs ABCD	F	
0000	0	
0001	1	$AB = 00$
0010	0	$F = D$
0011	1	
0100	1	
0101	0	$AB = 01$
0110	0	$F = C'D'$
0111	0	$= (C + D)'$
1000	0	
1001	0	$AB = 10$
1010	0	$F = CD$
1011	1	
1100	1	
1101	1	$AB = 11$
1110	1	$F = 1$
1111	1	



(b)

Inputs ABCD	F	
0000	0	
0001	1	$AB = 00$
0010	1	$F = C'D + CD'$
0011	0	
0100	1	
0101	0	$AB = 01$
0110	0	$F = C'D' + CD$
0111	1	
1000	1	
1001	1	$AB = 10$
1010	1	$F = 1$
1011	1	
1100	0	
1101	1	$AB = 11$
1110	0	$F = D$
1111	1