BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

EEE 466 (July 2023)

Analogue Integrated Circuits and Laboratory

Final Project Report

Section: G1 Group: 01

1 to 8 Analogue Demultiplexer

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   Lecturer, Department of EEE, BUET

Signature of Instructor: _____

Academic Honesty Statement:

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"In signing this statement, We hereby certify that the work on this project is our own and that we have not copied the work of any other students (past or present), and cited all relevant sources while completing this project. We understand that if we fail to honor this agreement, We will each receive a score of ZERO for this project and be subject to failure of this course."

Signature: _____ **Full Name: MD Sumon Howlader** **Student ID: 1906018**	**Signature:** _____ **Full Name: Subhan Zawad Bihan** **Student ID: 1906037**
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Table of Contents

1 Abstract

Analog demultiplexers are also used in applications where a single analog signal needs to be routed to multiple devices. For example, an analog demultiplexer can be used to send an audio signal to multiple speakers.
In this project we are specifically designing a 1:8 Demultiplexer using CMOS logic gates. CMOS stands for Complementary Metal Oxide Semiconductor. And CMOS based logic gates uses complementary pair of NMOS and PMOS transistors. In both NMOS and PMOS transistor, the voltage applied between the gate and source acts as a control voltage. By controlling the gate to source voltage, PMOS and NMOS transistor can be used as a switch. And they can be used to design a logic gate.

2 Introduction

The goal of this project is to design a 1:8 demultiplexer, which meets the specifications given below.

Specification	**Range**
Supply Voltage	+/- 3V
Logic High Level	1.4 V
Logic Low Level	0 V
Input Capacitor (max)	50 pF
Charge Injection Over the full signal swing range (max)	5 pC
Switching On time (ton) (at RL= 1k, CL=10 pF(max)	100 ns
Analog Signal Range	-2 to 2 V
Power dissipation (max)	10 mW
On-Resistance	10 ohm
Bandwidth, 3dB	1 Mhz

3 Design

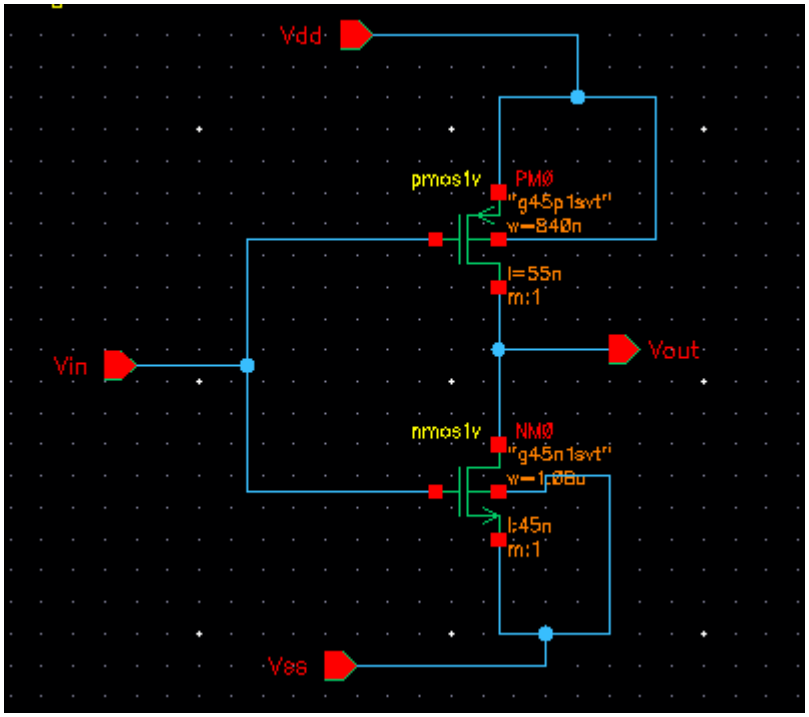
We used Cadence Virtuoso to design the 1 to 8 Analogue Demultiplexer. For this we have used the GPDK045 Library along with other basic libraries such as analoguelib and etc. for different elements.
For the application and to reach given requirements we used the 5nm process components embedded in GPDK045 library: pmos1v and nmos1v. In general, we designed CMOS logic gates using these pmos1v and nmos1v transistors. Then Using basic logic gates, we implemented the 1 to 8 demultiplexer step by step. First, we made a 1 to 2 demux block, from there a 2 to 4 demux block and finally using these blocks we were able to make a 1 to 8 analogue demultiplexer block that matched required specifications. We then used the output voltage of digital demux as the gating voltage of respective transmission gates to complete the design.

3.1 Design Method

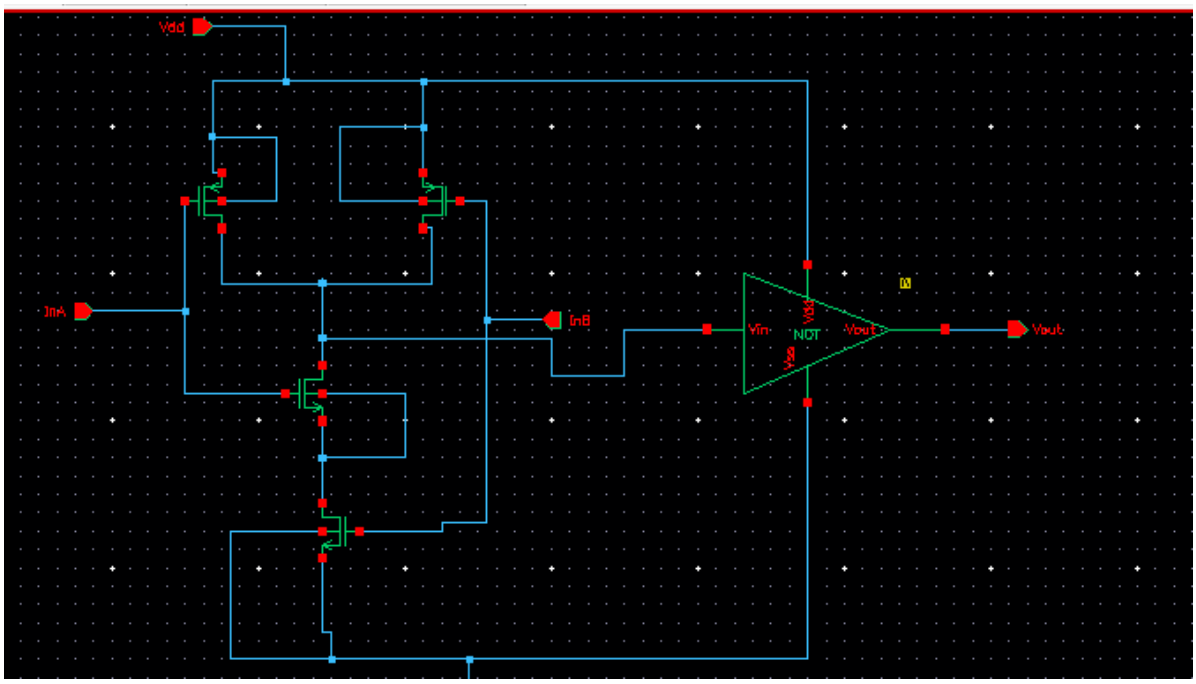
For the design we applied the knowledge gained from previous courses where we learnt how to implement CMOS complimentary logic to implement basic gates and other applications. From there we were able to implement step by step the 1 to 8 analogue Demultiplexer.

3.2 Circuit Diagram

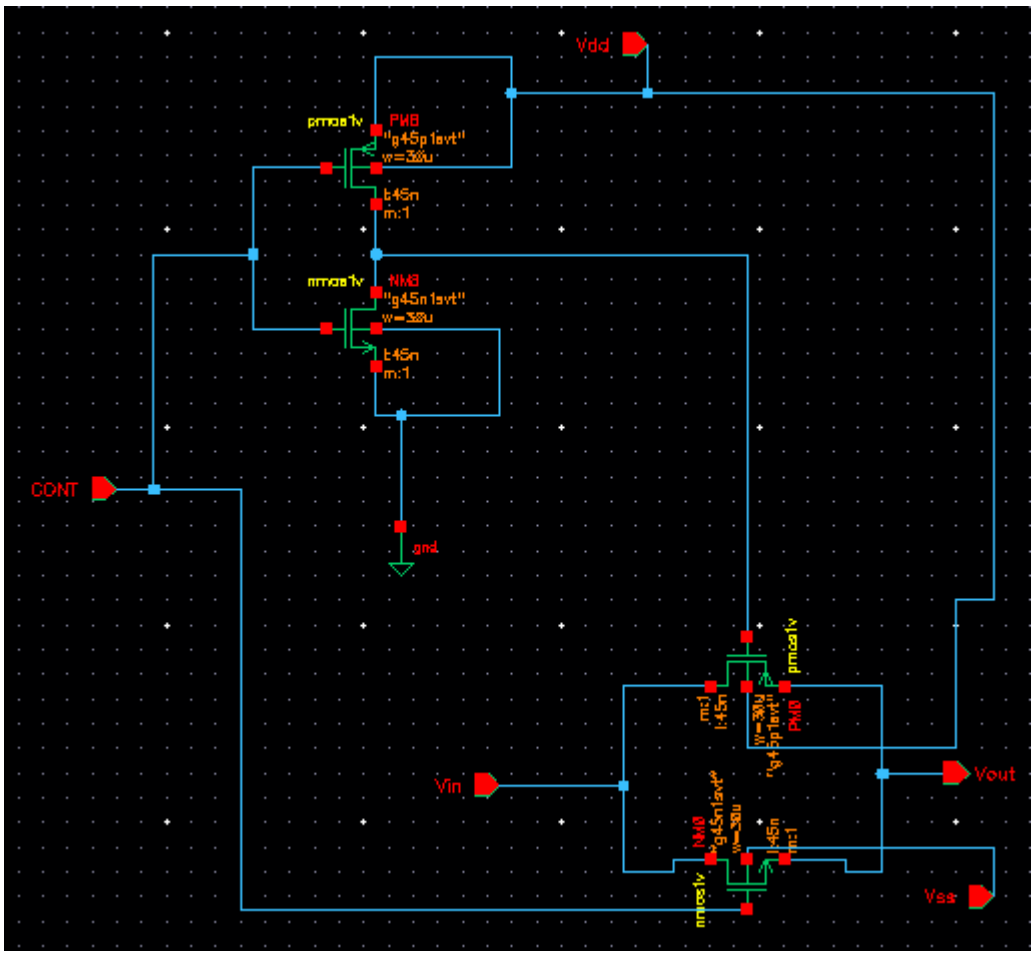
NOT Gate



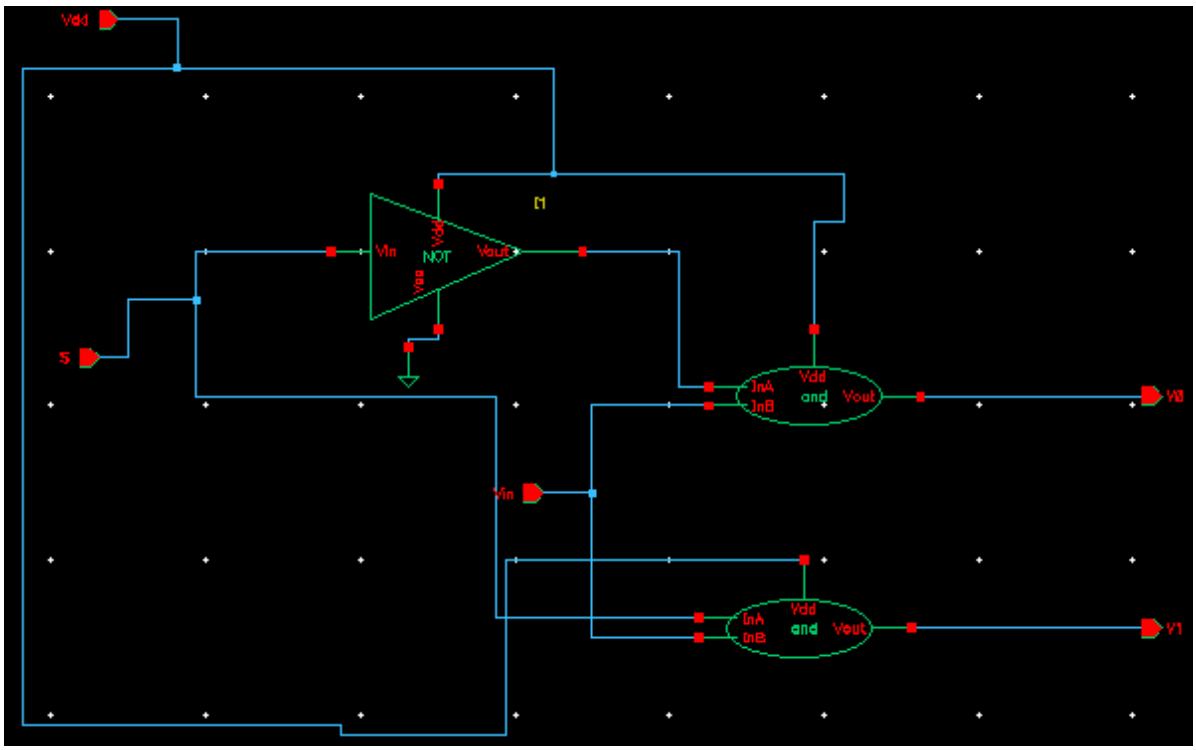
AND Gate



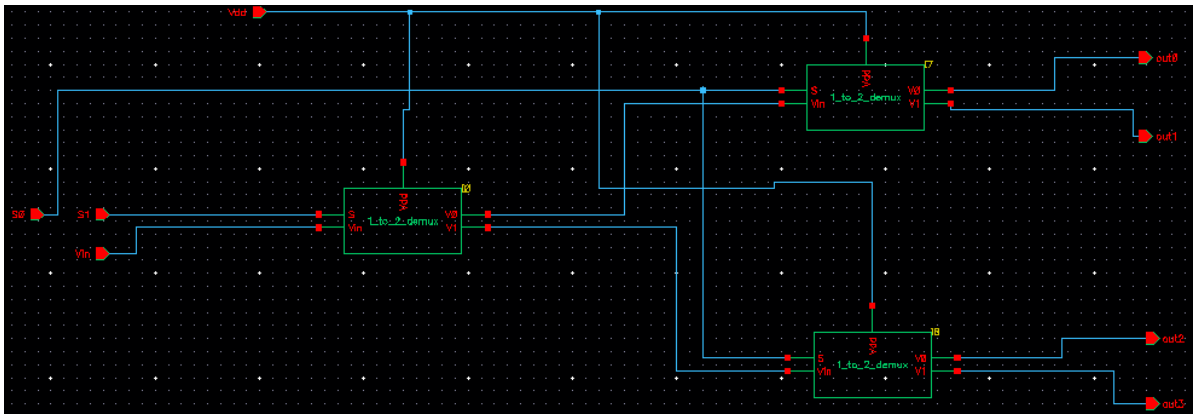
Transmission Gate



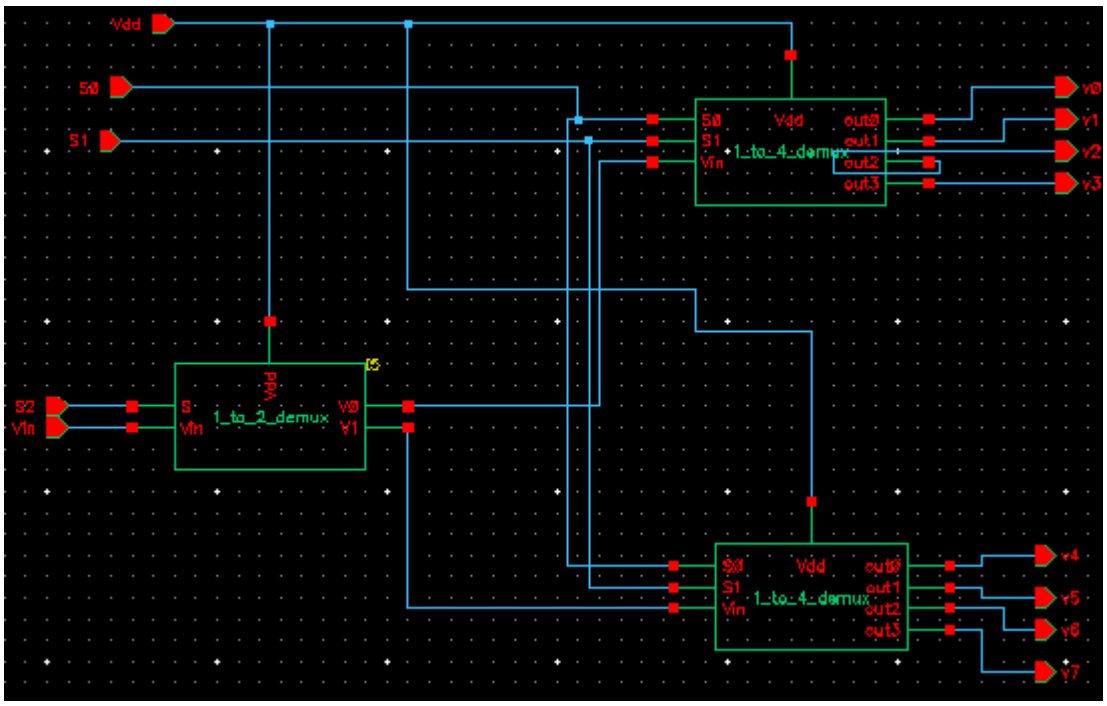
1-to-2 Digital Demux



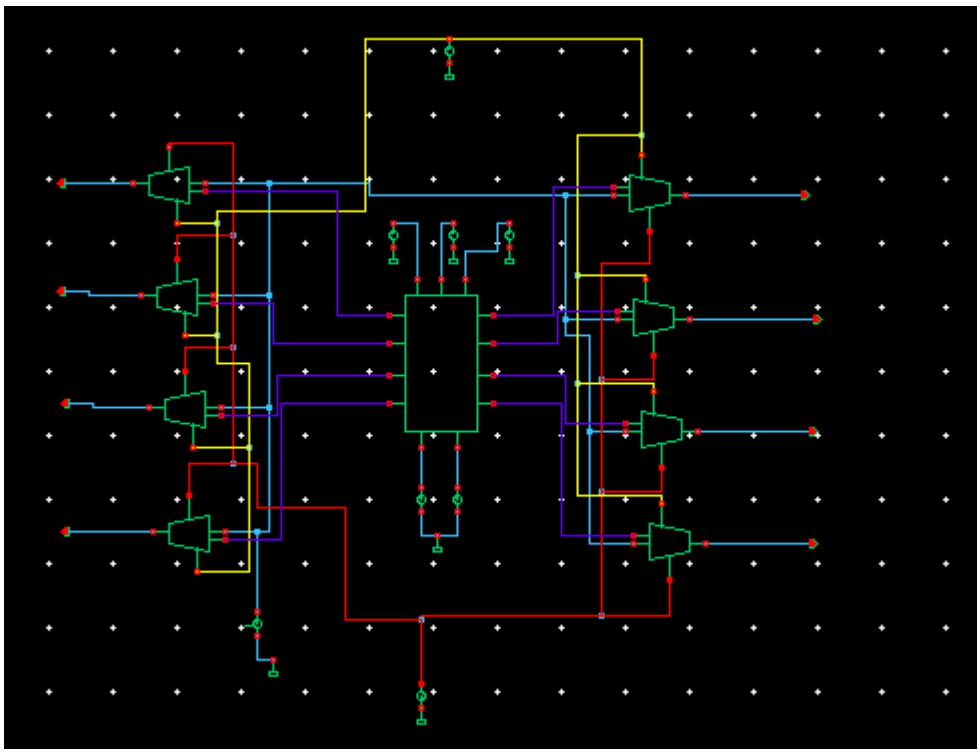
1-to-4 Digital Demux

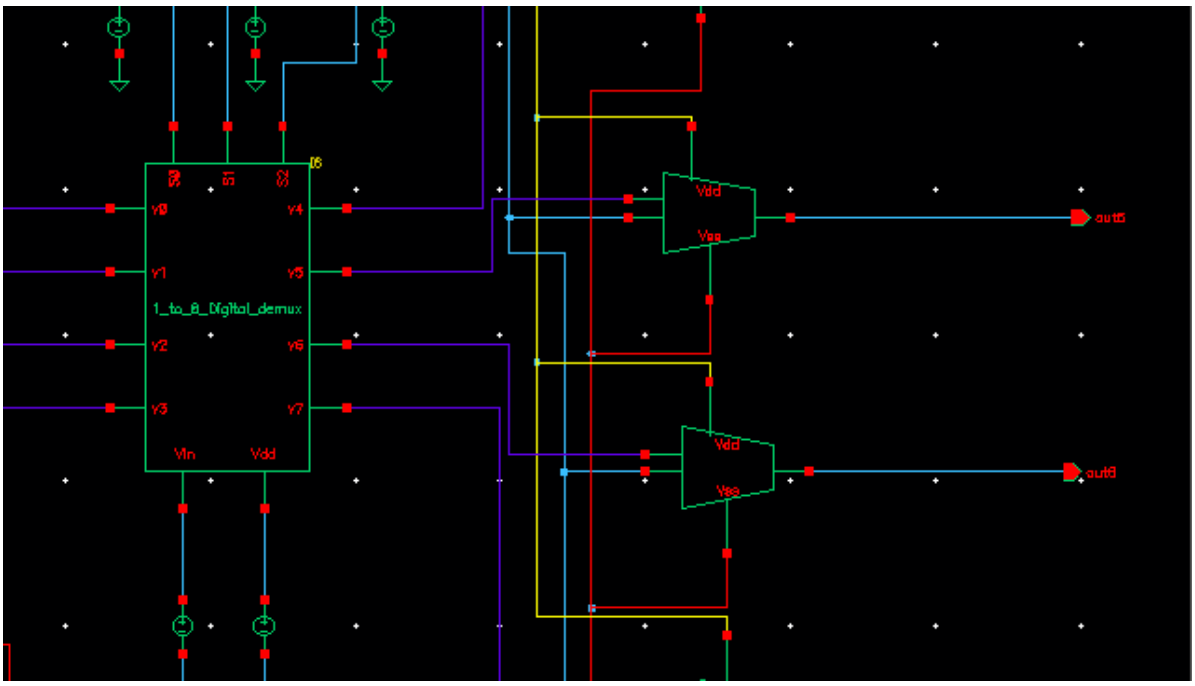


1-to-8 Digital Demux



Final Circuit (1-to-8 Analogue Demux)

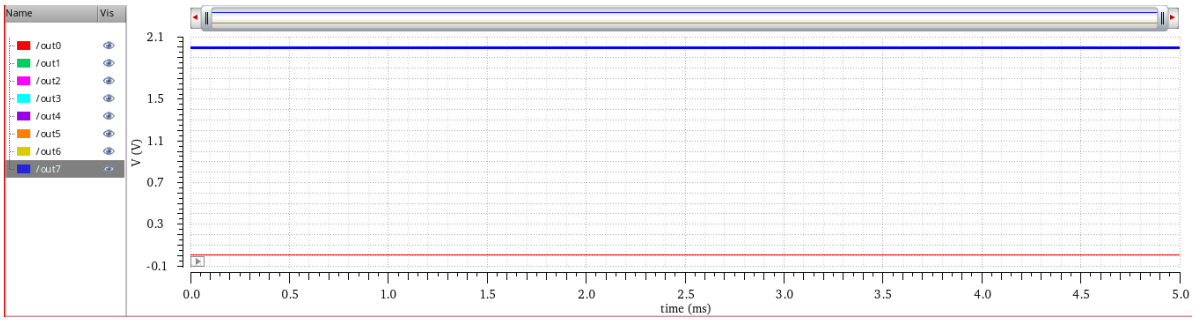




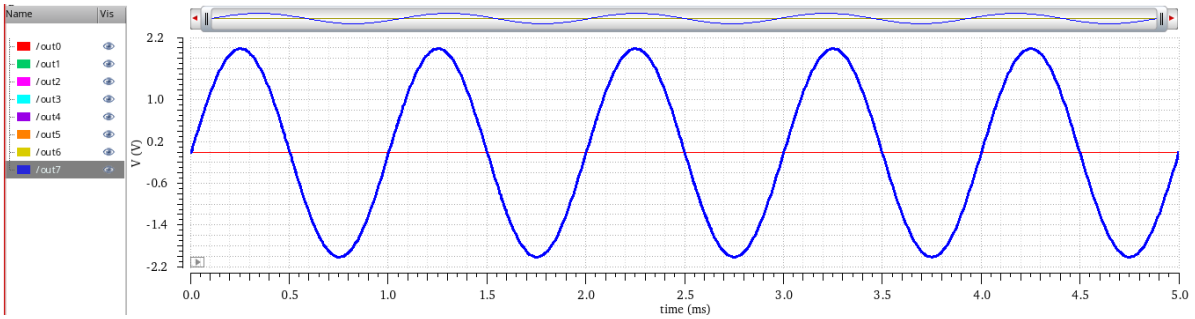
4 Implementation

4.1 Results

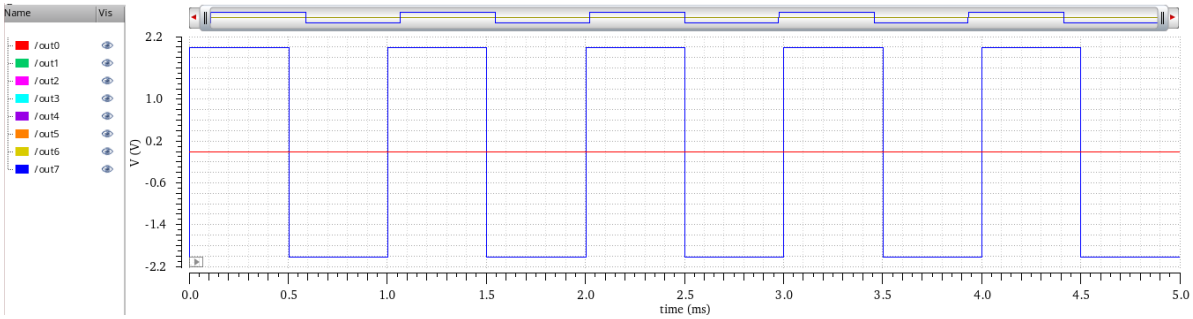
DC Input



SINE Input



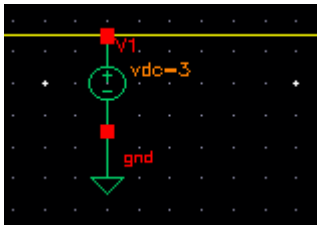
RECT PULSE Input

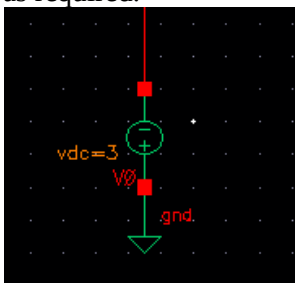


4.2 Specifications

4.2.1 Supply Voltage

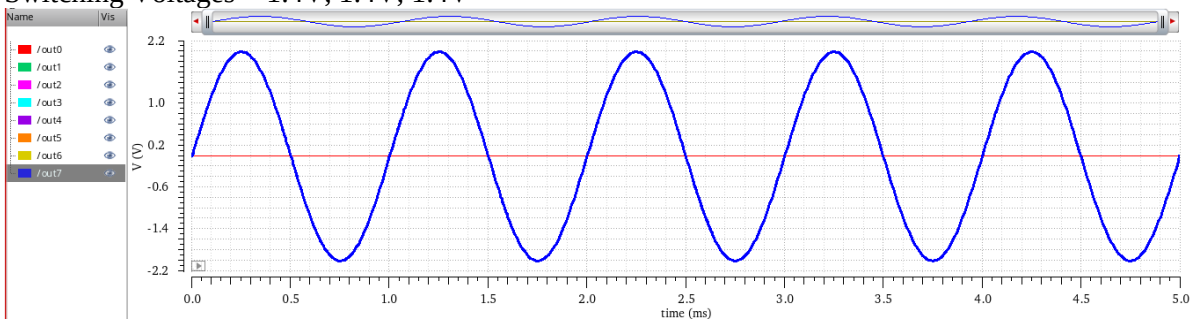
We have used **+3V and -3V** as required.



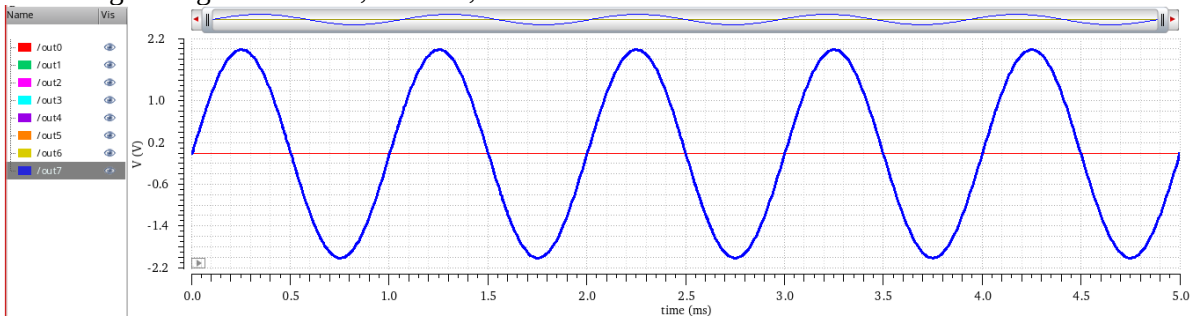


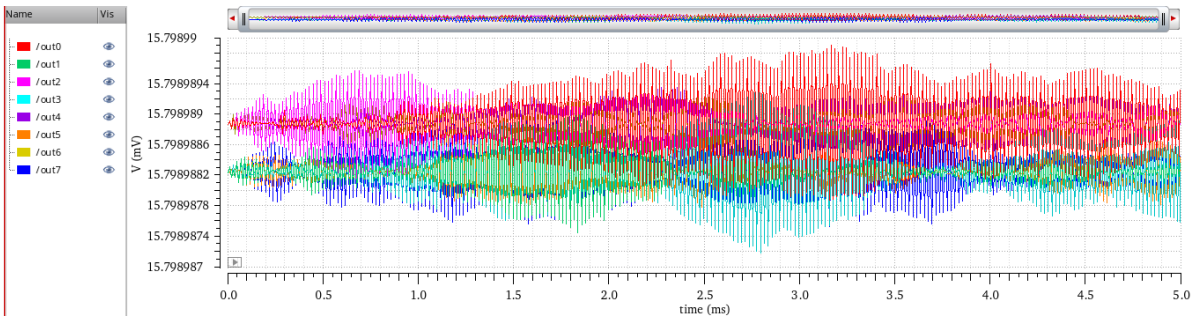
4.2.2 Logic Levels

Switching Voltages = 1.4V, 1.4V, 1.4V

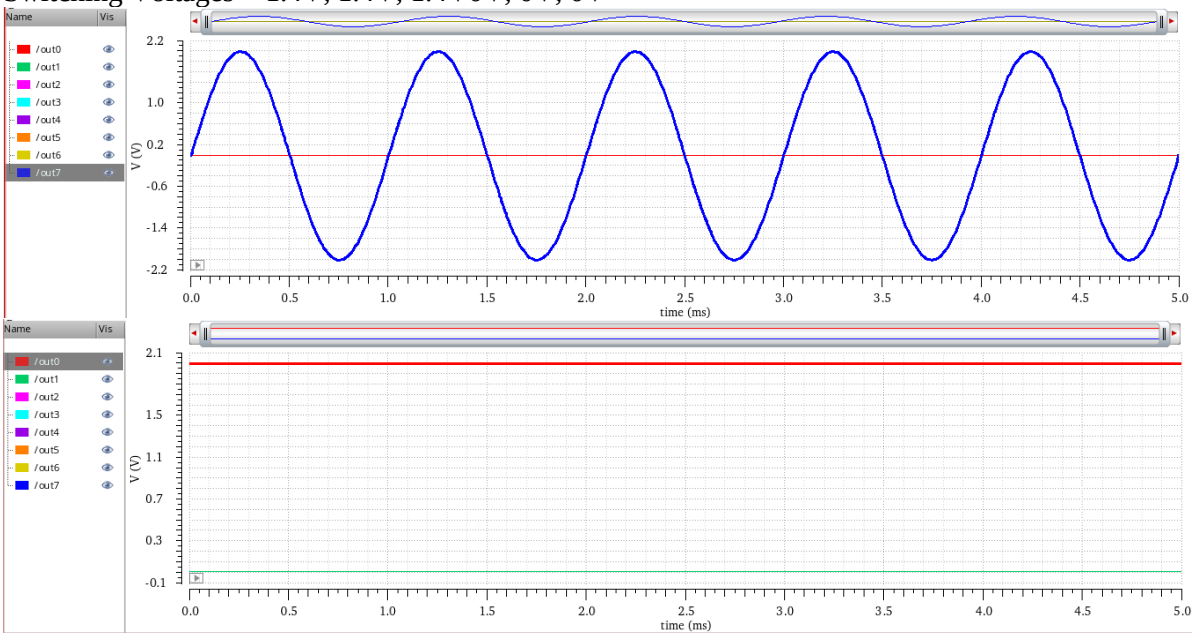


Switching Voltages = 1.4V3V, 1.4V3V, 1.4V3V





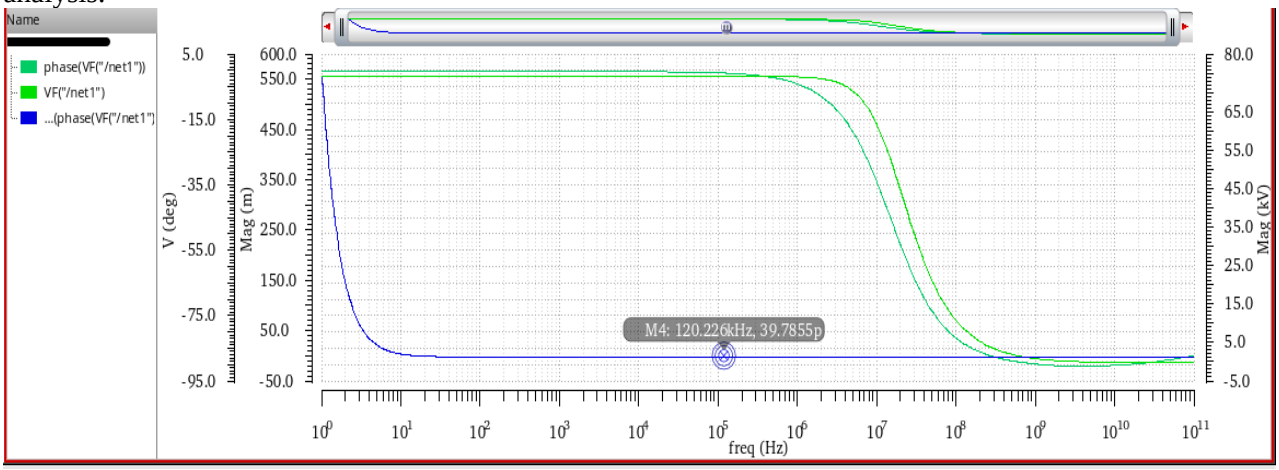
Switching Voltages = 1.4V, 1.4V, 1.4V0V, 0V, 0V



So the Logic High Level is **1.4V**. Any voltage lower than that (including **0V**) counts as logic low.

4.2.3 Input Capacitance

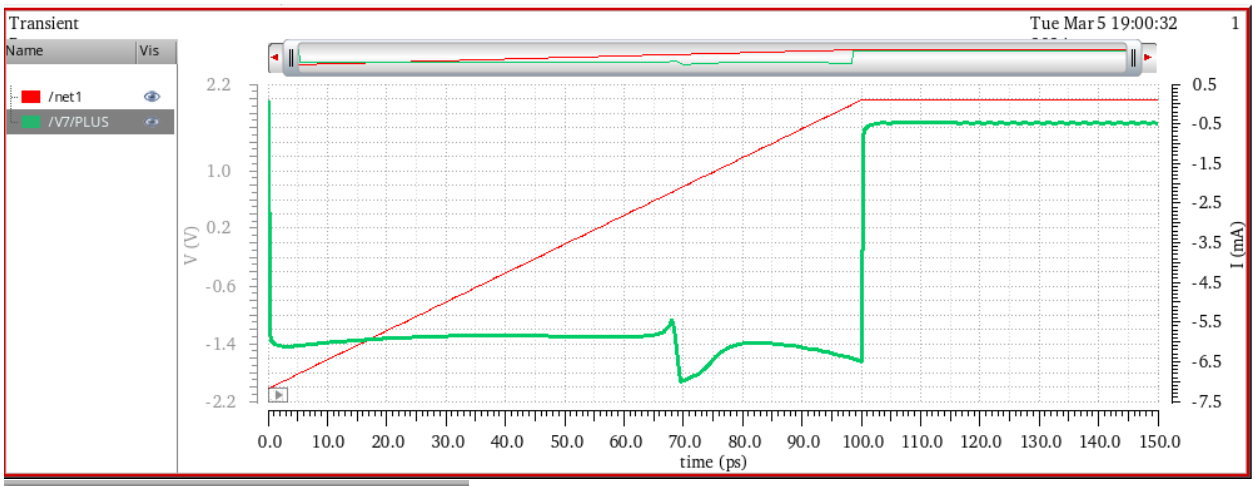
We plotted **-1/(2*pi*xval(VF("/net1"))*VF("/net1")*sin(phase(VF("/net1"))))** vs Freq. via AC analysis.



Input Capacitance = **39.79pF**

4.2.4 Charge Injection over the Full Signal Switch Range

Apply **vpwl** with short rise duration.



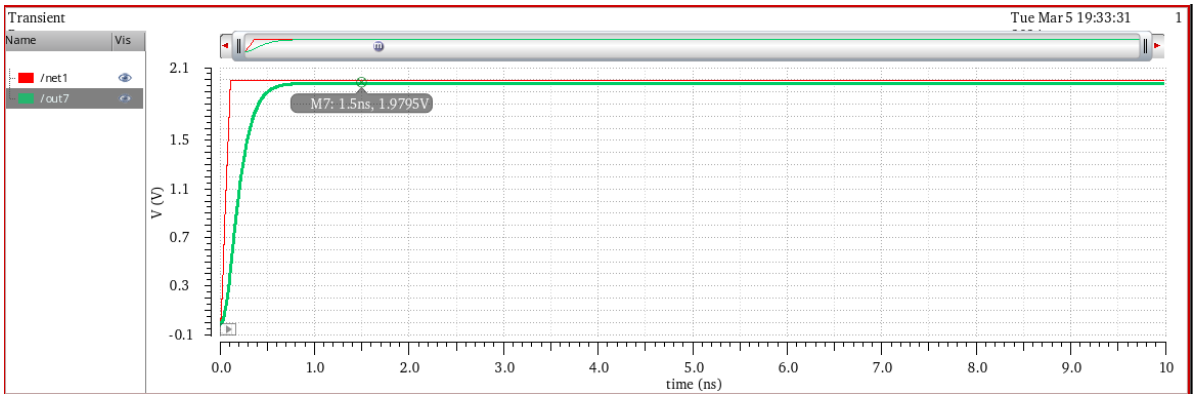
integ("/V7/PLUS" ?result "tran") 0 0.1n

	Expression	Value
1	-599.0E-15	-599.0E-15

Total charge = **-599 fC**

Average charge injection rate = **-599 uC/s**

4.2.5 Switching ON Time

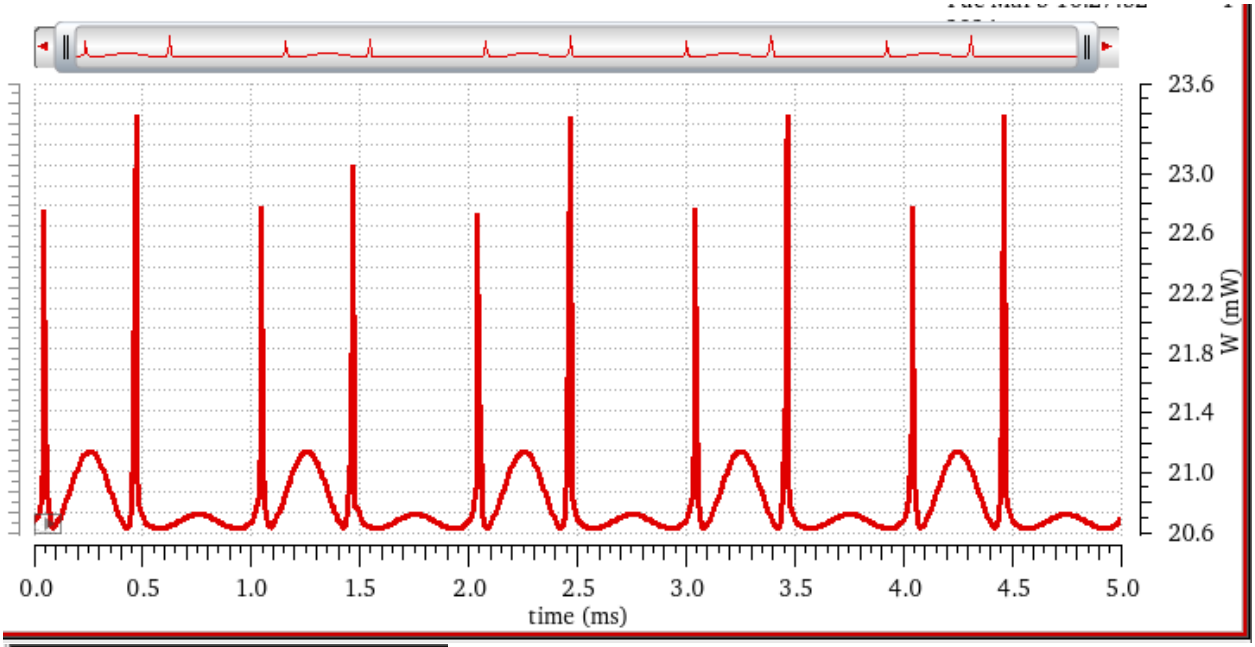


Switching ON time = **1.5ns**

4.2.6 Analogue Signal Range

We saw that it works perfectly for signal range of -2V to 2V and beyond.

4.2.7 Power Dissipation



	Expression	Value
1	average(getData...	20.81E-3

So power dissipation = **20.81 mW**

4.2.8 ON Resistance

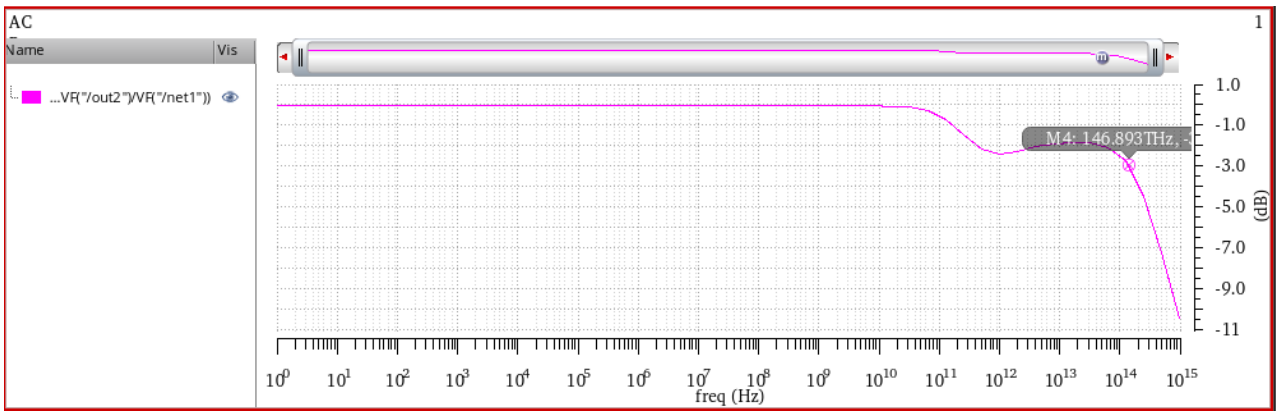
Apply 2V DC at Analogue Input and observe Output voltage and Input Current.

	Expression	Value
1	average(i("/V14/...	-2.336E-3

	Expression	Value
1	average(v("/out...	1.979

$R_{ON} = \frac{2-1.979}{-2.336\times10^{-3}} = \mathbf{8.99\ \Omega}$

4.2.9 3dB Bandwidth



Bandwidth = **146.89 THz**

5 Design Analysis and Evaluation

5.1 Novelty

- Meeting specification to be implementable in practical field.
- Implementable in signal processing
- Route multiple sensors to introduce home automation
- Mass scale possible implementation in industry
- Introduction to 1st analog circuit design

5.2 Investigations (PO(d))

5.2.1 Data Analysis and Spec Comparison

Our proposed design was successful in fulfilling maximum of the required specifications with some minor degree of error. Here's a table showcasing our values and the requirements and obtained experimental values in each part.

Specifications	Requirements	Experimental (Obtained) Value
Supply Voltage	+3/-3 V	+3/-3 V
Logic High Level	1.4 V	1.4 V
Logic Low Level	0 V	0 V (1.3 V and below)
Input Capacitance	50 pF	39.79 pF
Charge Injection	5 pC	0.599 pC
Analogue Signal Range	-2 to 2 V	-2 to 2 V (and beyond)
Power Dissipation	10 mW	20.81 mW
ON Resistance	10 ohm	8.99 ohm
3dB Bandwidth	1 MHz	146.89 THz

5.3 Limitations of Tools (PO(e))

There remains a trade-off between meeting specifications and output voltage swing. Again, we find a dependency of voltage level between which we can get erroneous output. We have used GPDK45 technology instead of TSMC18 to meet specification of threshold voltage and capacitance and used **L=55nm, W=850 nm (PMOS)** and **L=45nm, W=1080 nm (NMOS)**.

5.4 Sustainability and Environmental Impact Evaluation (PO(g))

- Our model is sustainable to perform in a desired temperature range.
- Integration of new technology in current technology architecture.
- Low requirement of material and power ensuring material and energy safety.

6 Reflection on Individual and Team work (PO(i))

6.1.1 Individual Contribution of Each Member

All member were involved in creating design, background studies. We met virtually and physically in classroom and lab to discuss and find solution to meet specification.

6.1.2 Mode of TeamWork

It was planned to meet in person and online. Initially, we held online meetings using Zoom where we brainstormed, spoke about our project goals, and swapped ideas. For communication purposes and to discuss project-related files and ideas, we created a messenger group. We worked offline together and implemented the circuits. As we encountered challenges or obstacles during the project, we have engaged in collaborative problem-solving to find solutions.

6.1.3 Diversity Statement of Team

Our project group is composed of four members who bring diverse perspectives, experiences, and backgrounds to the project. Here, we had the experience of fixing the time schedule that matches everyone's convenience and tried to work in an inclusive environment. Our different backgrounds and experiences allowed us to approach the project from a variety of perspectives, leading to more innovative solutions and better outcomes. We respected each other's ideas and perspectives and collaborated effectively to achieve our common goals.

6.1.4 Log Book of Project Implementation

Date	Milestone achieved	Individual Role	Team Role	Comments
All done combinedly in given timeframe	Background Study	-	All team members involved	
	Circuit Implementation	-	All team members involved	
	Debugging	-	All team members involved	
	Specification meeting	-	All team members involved	
	Redrawing Circuit	-	All team members involved	
	Circuit Finalization	-	All team members involved	

7 Future Work (PO(l))

- Specification further can be developed further
- Range improvement to meet voltage requirement and swing to make it versatile for application
- Device implementation in practical field.

8 References

[1] *Chary, Udary Gnaneshwara, R. Balabrahmam, and A. K. K. Sateesh. "Design of low voltage low power CMOS analog multiplexer for bio-medical applications." Int. J. Eng. Adv. Technol. 3 (2014): 21-24.*
[2] *Sipos, Emilia, Lelia Festila, and Gabriel Oltean. "Towards reconfigurable circuits based on ternary controlled analog multiplexers/demultiplexers." Knowledge-Based Intelligent Information and Engineering Systems: 12th International Conference, KES 2008, Zagreb, Croatia, September 3-5, 2008, Proceedings, Part III 12. Springer Berlin Heidelberg, 2008.*