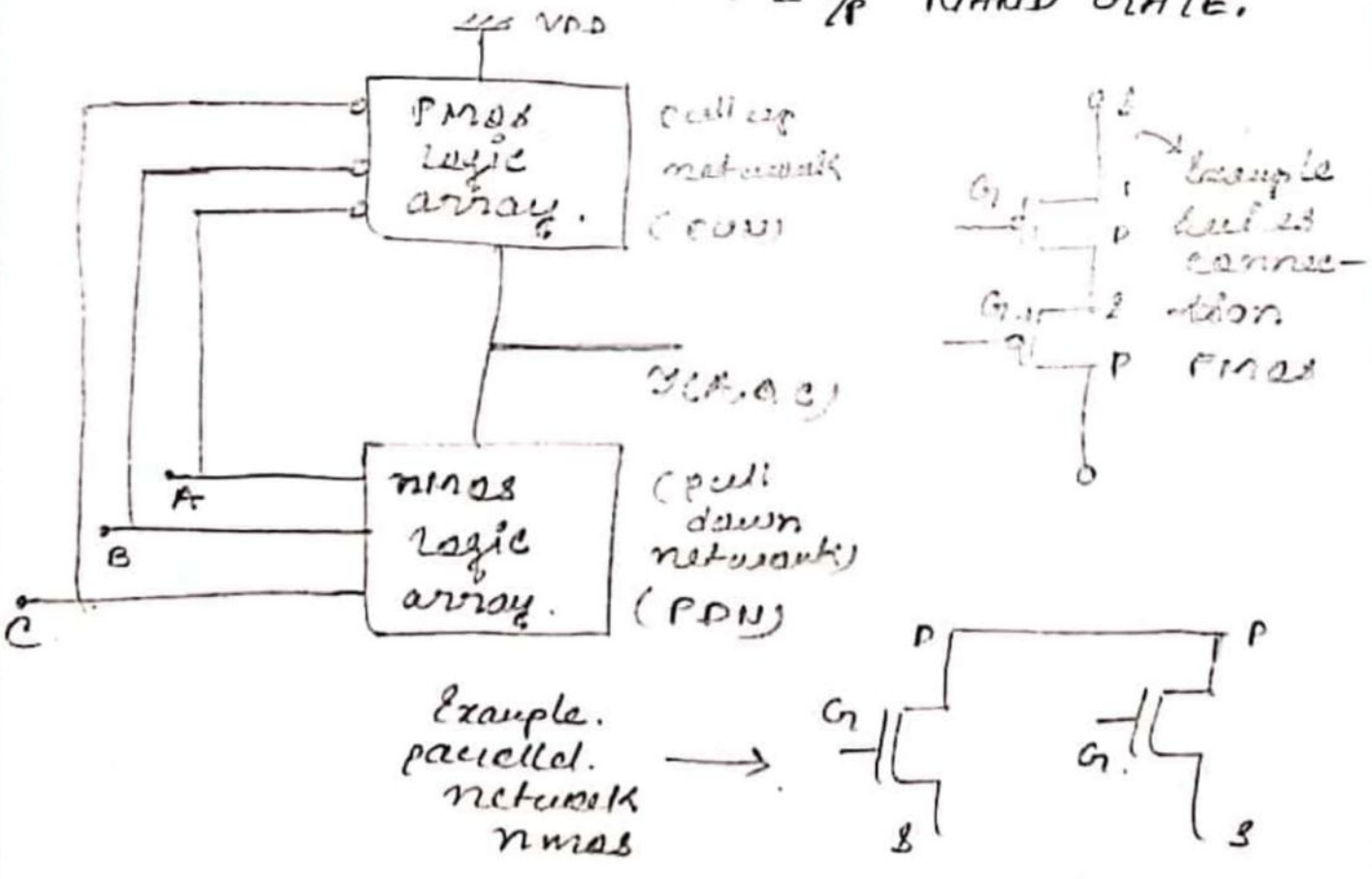
Experiment :- 1.C

Title:- SPICE Simulation of CMOS NAND GATE (2 I/P)

Objective:- To design and simulation of a 2 (I/P) NAND Gate using PSPICE and to get output as per truth table..

Apparatus:- Cadence / OrCAD Software.

Theory:- To build a NAND gate (2-i/p) circ. first have to know.. how a standard static CMOS logic gate design must be done and then with the help of which circ. can make a CMOS 2 i/p NAND GATE.



The above figure of static CMOS logic gate design is of a 3 i/p based CMOS logic gate and for design we need to consider that for pull up network if the main function to be realised has 'OR' then the CMOS transistors must be in series and if it has 'AND' then they should be placed in parallel.

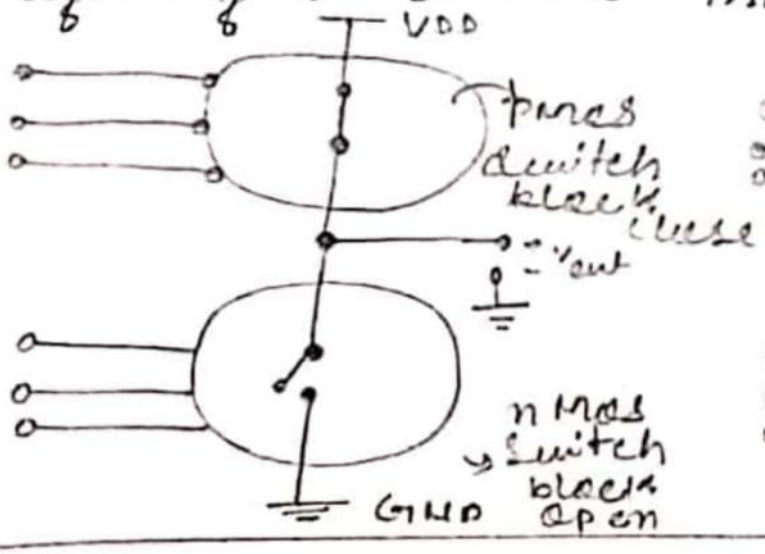
Alternatively for PDN if the function to be realised has 'OR' then the CMOS transistors should be in parallel and for 'AND' they should be in series.

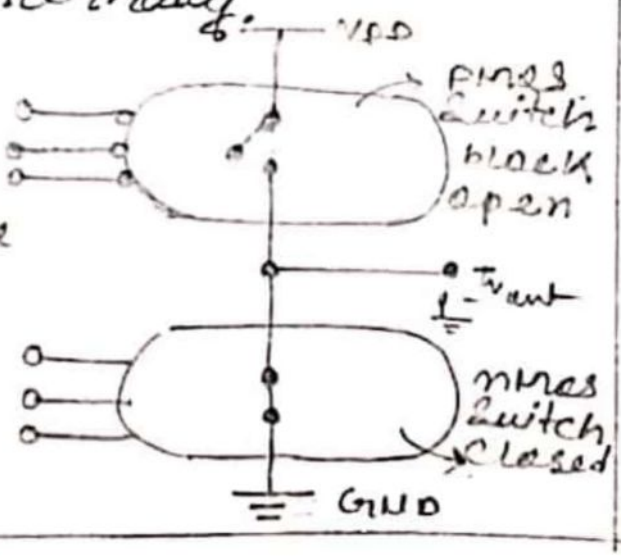
therefore,

PUN → pMOS logic array. { OR = series, AND = parallel }

PDN → nMOS logic array { OR = parallel, AND = series }

Now as we've seen how to arrange CMOS transistors so as they give us a desired logic output on a logic input, now we'll see how a CMOS logic gate works internally.





The above figure describes how we get a logic 1 o/p and now we get a logic 0 o/p. Now we'll see the truth table and symbol of NAND GATE.

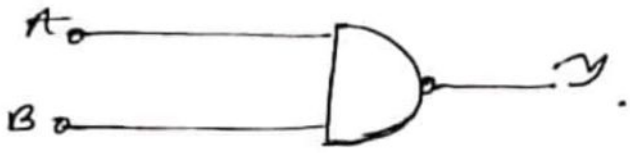


fig:- NAND GATE.

Truth table :-

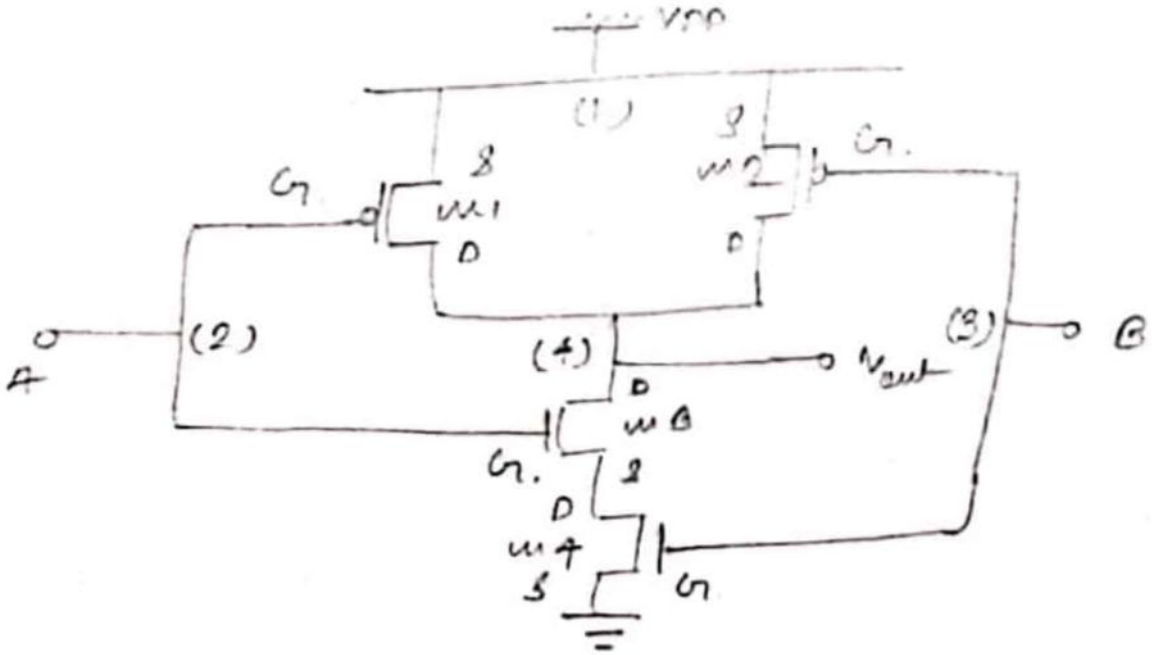
A	B	Y.
0	0	1
0	1	1
1	0	1
1	1	0.

$F = \overline{A.B}$

$= NOT(A.B)$

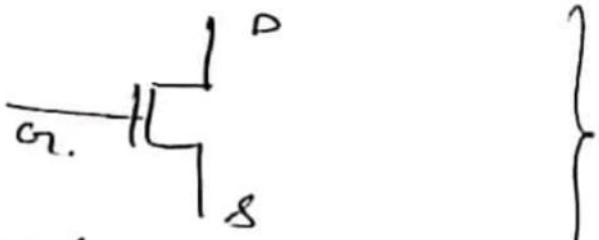
} NAND GATE operation function

CKT diagram :-



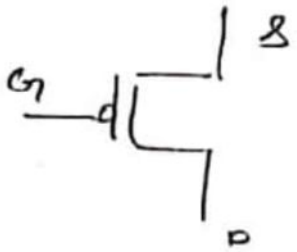
Operation of the ckt :-

For a normal CMOS (nMOS & pMOS) we know how the gate voltage works for giving O/P's. So we can summarize them as :-



$G = 1$; nMOS = ON

$G = 0$; nMOS = OFF



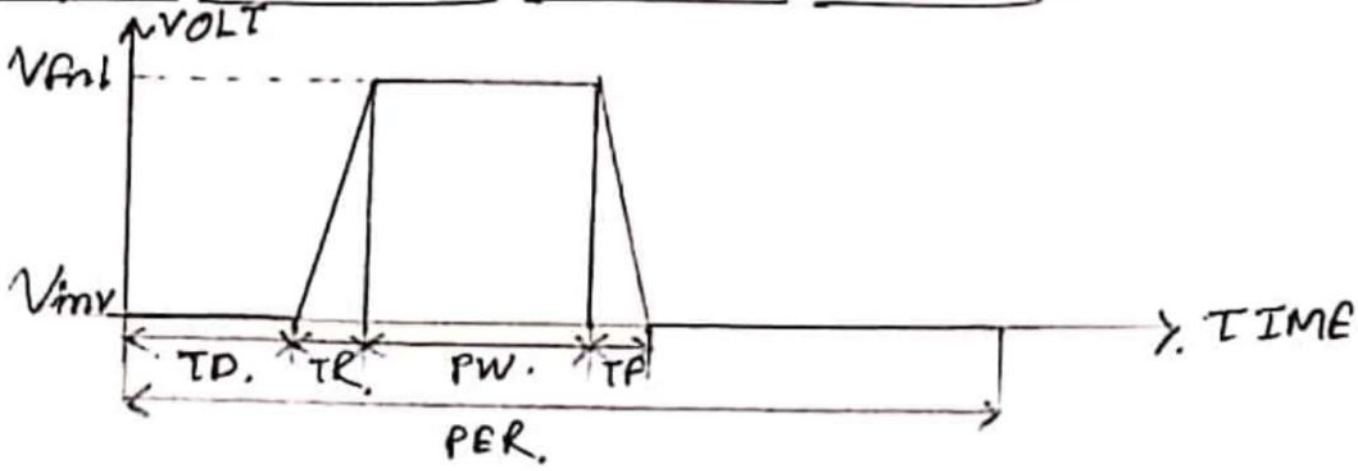
$G = 0$; pMOS ON

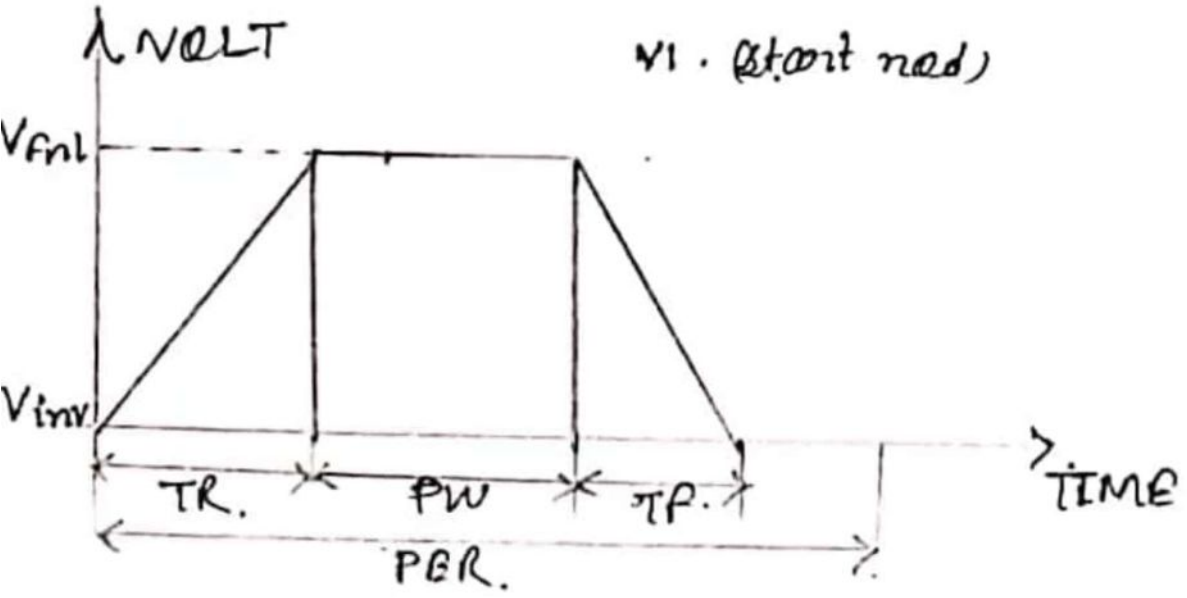
$G = 1$; pMOS OFF

↳ On basis of above conclusion we can draw the table to visualize the truth table with which transistors will be on, or off based on two I/P's A & B.

A	B	M1	M2	M3	M4	Y
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

To represent a pulse in PSPICE :-





V1 . (Start node)

V1 (startnode) (finishnode) pulse .(Vinv)(Vfnl) (TD)(TR)(TF)

V1 1 0 pulse 0 5 0 2ns 2ns

(PW) (PER)

8ns 20ns.

Program for the ckt :-

```
Vdd   1   0 . DC . 5v
Va    2   0 PULSE  0  5  0  0.1ns 0.1ns 50ns 100ns.
Vb    3   0 PULSE  0  5  0  0.1ns 0.1ns. 100ns 200ns
M1    4   2   1   1  pmod (W= 40u  l= 10u)
M2    4   3   1   1  pmod (W= 40u  l= 10u)
M3    4   2   5   5  nmod (W=10u  l=2u)
M4    5   3   0   0  nmod (W=10u  l=2u)
.MODEL pmod .pmos(Vto = -1  lambda = 0.02)
.MODEL nmod .nmos(Vto= 1  lambda =0.02)
.TRAN . 0ns  600 ns.
.PROBE
.END.
```

123_Amrita EXP-1(c) CMOS Two input NAND Gate DT-04112020

Date/Time run: 11/17/20 20:23:38 Temperature: 27.0

Date: November 17, 2020 Page 1 Time: 20:28:47

Precautions:-

→ The SPICE syntax should be proper.

→ Value of pulse should be appropriate.

→ Traces should be proper.

Conclusions:-

From the above exp we learnt to simulate NAND Gate using CMOS.