Design of a Single Stage Amplifier with 1 MHz Bandwidth, 25dB Gain and 50 µA Quiescent Current in 28nm CMOS Technology using Synopsys Custom Design Platform

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***Abstract*—The amplifiers are integral part of many analog and digital systems over the years. Amplifiers with different degrees of complexity are used in various circuits. The design of such amplifiers is still a challenge as supply voltage and transistor dimensions are getting reduced because of scaling. Here, a single stage amplifier *with 1 MHz Bandwidth, 25dB Gain and 50 µA Quiescent Current* has been implemented using Synopsys Custom Design Platform in 28nm CMOS Technology.**

I. INTRODUCTION

Amplification is an important operation in many analog and sometimes even in digital circuits. Usually amplification of a signal is needed because its amplitude may be too small to drive a load, have good noise margin, or provide certain logic level in a digital system. Amplification is also important for a feedback system.

II. A SINGLE STAGE AMPLIFIER

The circuit diagram of a single stage amplifier is shown in Fig. 1 [1]. In Fig. 1, M1, M2 are NMOS and M3, M4 are PMOS devices respectively.

Among various design parameters of the amplifier gain and bandwidth are most important one. The small signal, low frequency gain G of the circuit of Fig. 1 is,

$$G = g_{mN}(r_{OP} \,||\, r_{ON}) \qquad (1)$$

The subscripts N and P represent NMOS and PMOS respectively. The term g_m represents the transconductance and r_O is the output impedance. The bandwidth is usually determined by the load capacitance C_L. The bandwidth (BW) is given by

$$BW = \frac{g_m}{2\pi C_L} \qquad (2)$$

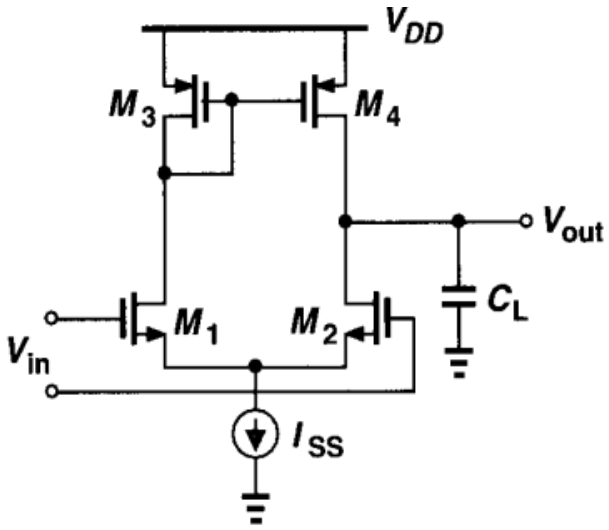

Fig. 1. Single stage amplifier [1]

III. SIMULATION RESULTS

The circuit of Fig. 1 has been implemented in Synopsys Custom Design Platform in 28nm CMOS Technology. The schematic of the circuit is shown in Fig. 2. The specifications of the two input voltage sources are 0.45V dc and 1V ac respectively. The value of the supply voltage source is V_{dd} = 1.8V. A load load capacitance of C_L = 1 pF has also been used. The aspect ratio of the transistors of Fig. 2 is shown in Table 1.

TABLE I. W/L ratio

Transistor	W in µm	L in µm
M1- M2	1	0.4
M3 - M6	1	0.3

It also to be noted from Fig. 2, that the current source (I_{SS}) of Fig. 1 has been implemented with a current mirror circuit represented by M5 and M6 respectively.

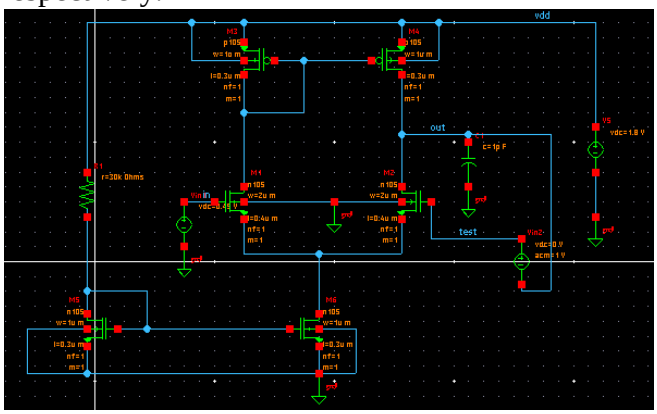

Fig. 2. Schematic diagram

The simulation result is shown in Fig. 3. A gain of 25.4 dB and UGB of 996.932 KHz has been obtained from Fig. 3 which are very close to the specification of 25 dB gain and 1 MHz bandwidth.

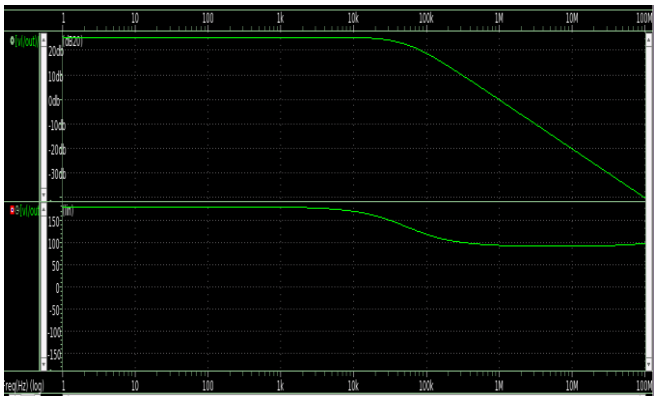

Fig. 3. Simulation result

REFERENCES

[1] B. Razavi. Design of Analog CMOS Integrated Circuits. McGraw-Hill, Singapore, 2001.