Al-Quds University
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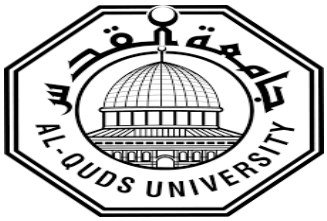

Advanced Computer Architecture
(0702475)

Pipeline MIPS Processor Verilog Design

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Section: 1
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❖ Table of contents:

❖ Project :

https://drive.google.com/file/d/1L3Wky1jsJEVYH5NprZLBqfUaxobOZbFA/view?usp=sharing

❖ Introduction:

This project involves the design and implementation of a 32-bit Five Stage Pipeline MIPS processor.The five stages of this processor include Instruction Fetch, Instruction Decode, Execution, Memory Access, and Write Back. Each stage plays a crucial role in the processing of instructions, contributing to the overall performance of the system. This project aims to explore these stages in detail, understand their workings, and implement them effectively to create a functional MIPS processor.

❖ Project Overview:

This Project is simply a Design of pipeline MIPS processor written in Verilog (VHDL) with handling of Data hazards and forwarding process to achieve the maximum performance in units of clock cycles. Also, this Design Code is written in simple way without any complexities, and every single module is written in a separate file to avoid coding traffic and to manage and distribute tasks on all members in the team; which makes the development process easier and co-operative

❖ Design:

2.1. Modules:

*In the single cycle the following modules are implemented:

✓ ALU32Bit.

✓ ALUControl.

✓ ControlUnit.

✓ Adder.

✓ InstructionMemory.

✓ PC.

✓ PCAdder.

✓ RegisterFile.

✓ ShiftLeft2.

✓ SignExtend.

✓ Mux2x1.

✓ DataMemory.

✓ *Modules for pipelining:

✓ IF_ID_reg.

✓ ID_EX_reg.

✓ EX_MemReg.

✓ Mem_Wbreg.

✓ Comparator (Beq).

✓ HazardDetectionUnit.

✓ ForwardingUnit.

✓ Mux3x1.

o The ID_EX_reg.v file is the register file between the instruction

Decoding stage and Execution stage which will pass the stored

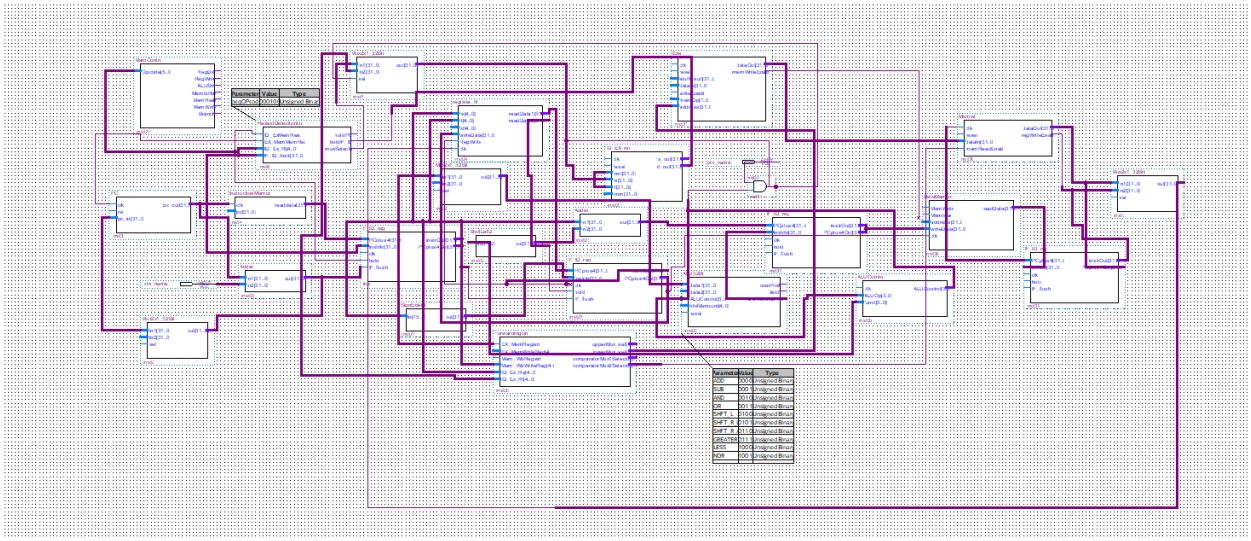
result of the first stage to the next stage (Execution stage) with

the next clock cycle.

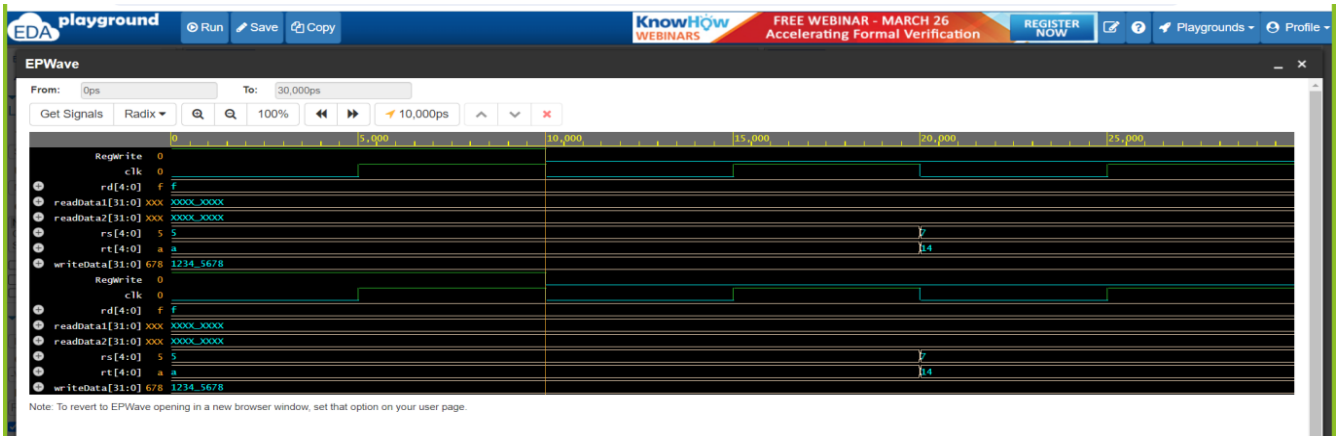
o The EX_MemReg.v file is the register file between the Execution stage and Memory stage which will pass the stored result of the first stage to the next stage (Memory stage) with the next clock cycle.

❖ Testing and Test Benches:

attached for the folder a file “MIPSTestBenchPhase1.v” which contain the test bench that we used and also attached file “Code.txt” which contain the code we used for testing. , also used EDA playground



Datapath



Test banch for Register File

❖ References

1. https://github.com/
2. https://www.edaplayground.com/x/Bfss
3. A single-cycle MIPS processor (washington.edu)