EG 212 Computer Architecture Assignment – 2: Marks: 40
Feb 2024

Guidelines:

- To be done individually or in groups of maximum 3 students (not more than 3)
- You can choose to do the design in any language you wish, C, C++, python, Verilog etc
- **What to submit:**
  - **Submit your report (in pdf format) which contains roll numbers and names of the students in the group, some explanation of the code, the program you chose to implement, any assumptions in your processor design, snapshots of result etc.**
  - **Upload codes separately.**
  - **Upload the machine code of the programs separately**
- The submission will be followed by a viva/demo
- When you submit the code, rename the filename of your code to <roll_numbers>_filename.< >
- All codes will run through a plagiarism check. Files found similar will get a 0 for the assignment. Repeat offence will attract Grade penalty on the overall grade
- Submit by Feb 26, 2024, 11:59pm on LMS under Assignment 2
- Marks: 30 + 10 for viva

1. Assembly programs and run it on MARS assembler– **10 marks**
   1. You can choose the same C programs that you used in the IAS assignment. Choose at least 3 programs. Write the MIPS assembly version of the 3 programs.
   2. The program should be chosen such that it must definitely include LW, SW, Branch or Jump and ALU instructions after assembling.
   3. Test these out using the MARS MIPS Assembler.
   4. For the demo, you should show **at least one program that is verified on MARS assembler.**
   5. You could also use the other instructions available in the MIPS reference guide (not covered in the class)

2. Non-pipelined MIPS processor design – **20 marks**
   1. Take as input the machine code of instructions generated by the assembler in the previous step. The program should do something substantial – such as, matrix multiplication, factorial, convolution and not just a simple add/mul. Store this machine code in instruction memory (array for example).

2. Design a MIPS non-pipelined processor with 5-stages: IF, ID, EX, Mem, WB. Use the set of registers that are allowed by the MIPS architecture.
3. Desired output: If you chose a sorting algorithm, the output should be sorted integers (either in ascending or descending order) stored in a certain array. You can also display outputs such as PC, outputs of each stage etc for better understanding.

Note

- You are free to use any programming language
- Instruction and Data memory can be declared as arrays of limited size (need not be 2^{32})
- Memory has to be byte addressable