Intel® Core™ i7 Processor Family for LGA2011-v3 Socket
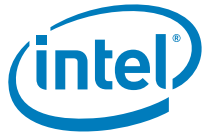
Datasheet – Volume 1 of 2

Supporting Desktop Intel® Core™ i7-6950X Extreme Edition Processor for the LGA2011-v3 Socket

Supporting Desktop Intel® Core™ i7-6900K, i7-6850K, and i7-6800K processors for the LGA2011-v3 Socket

August 2016

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Revision History

Revision Number	Description	Date
001	• Initial release	May 2016
002	• Section 1.3.1. Updated section to remove support for 2Gb and UDIMM x16	August 2006

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1 Introduction

The Intel® Core™ i7 processor family for LGA2011-v3 Socket processors are the next generation of 64-bit, multi-core enterprise processors built on 14-nm process technology. Based on the low power / high performance processor microarchitecture, the processor is designed for a platform consisting of a processor and Platform Controller Hub (PCH).

This datasheet, Volume 1 provides Electrical specifications (including DC specifications), signal definitions, and land listings for the Intel® Core™ i7 processor family for LGA2011-v3 Socket processors.

The datasheet is distributed as a part of a two volume set. Volume 2 provides register information. Refer to the Related Documents section for access to Volume 2.

The processor supports up to 46 bits of physical address space and 48 bits of virtual address space. The processor features up to 40 lanes of PCI Express* 3.0 links capable of 8.0 GT/s, and 4 lanes of DMI2/PCI Express* 2.0. It features an Integrated Memory Controller (IMC) that supports 4 channels of DDR4 memory.

The integrated memory controller (IMC) and integrated I/O (IIO) are on a single silicon die. This single-die solution is known as a monolithic processor.

This document covers the following processors:

- Desktop Intel® Core™ i7-6950X Extreme Edition Processor for the LGA2011-v3 Socket
- Desktop Intel® Core™ i7-6900K, i7-6850K, and i7-6800K processor for the LGA2011-v3 Socket

Note: Throughout this document, the Intel® Core™ i7 processor family for LGA2011-v3 Socket processors may be referred to as "processor".

Note: Some processor features are not available on all platform segments, processor types, and processor SKUs.

Figure 1-1. Platform Block Diagram Example
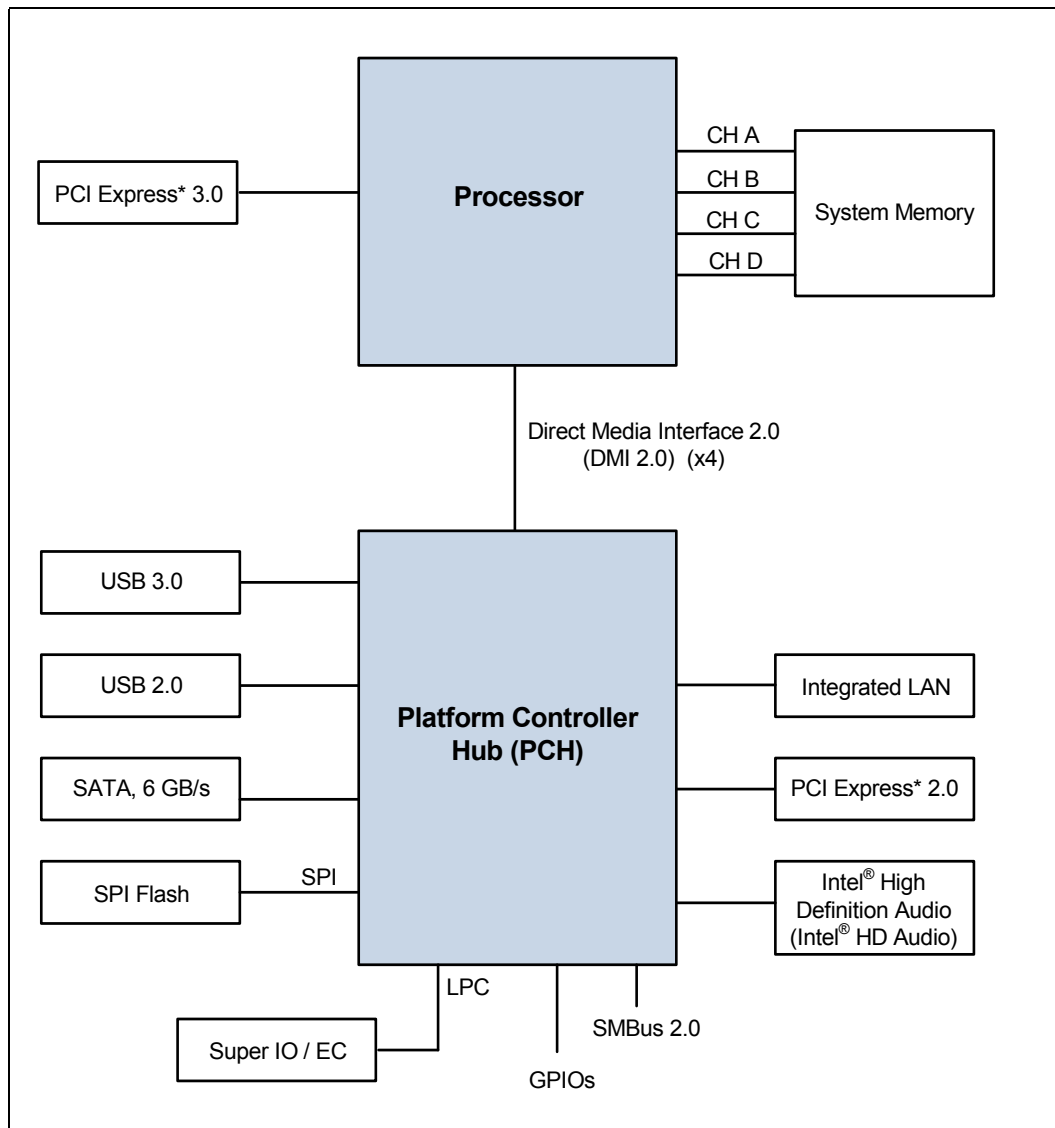
1.1   Processor Feature Details

- Up to 10execution cores
- Each core supports two threads (Intel® Hyper-Threading Technology)
- 32 KB instruction and 32 KB data first-level cache (L1) for each core
- 256 KB shared instruction/data mid-level (L2) cache for each core
- Up to 25 MB last level cache (LLC): up to 2.5 MB per core instruction/data last level cache (LLC), shared among all cores

1.2 Supported Technologies

- Intel® Virtualization Technology (Intel® VT)
- Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)
- Intel® Virtualization Technology (Intel® VT) Processor Extensions
- Intel® 64 Architecture
- Intel® Streaming SIMD Extensions 4.2 (Intel® SSE4.2)
- Intel® Advanced Vector Extensions 2.0 (Intel® AVX2)
- Intel® AVX Floating Point Bit Depth Conversion (Float 16)
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Execute Disable Bit
- Intel® Turbo Boost Technology
- Enhanced Intel® SpeedStep® Technology

1.3 Interfaces

1.3.1 System Memory Support

- Supports four DDR4 channels
- Unbuffered DDR4 DIMMs supported
- Independent channel mode or lockstep mode
- Data burst length of eight cycles for all memory organization modes
- Memory DDR4 data transfer rates of 1600 MT/s, 1866 MT/s, 2133 MT/s, and 2400 MT/s
- 64-bit wide channels
- DDR4 standard I/O Voltage of 1.2 V
- 4Gb, and 8Gb DDR4 DRAM technologies supported for these devices:
  - UDIMM x8
- Up to 4 ranks supported per memory channel, 1, 2, or 4 ranks per DIMM
- Open with adaptive idle page close timer or closed page policy
- Per channel memory test and initialization engine can initialize DRAM to all logical zeros or a predefined test pattern
- Minimum memory configuration: independent channel support with 1 DIMM populated
- Command launch modes of 1n/2n
- Improved Thermal Throttling
- Memory thermal monitoring support for DIMM temperature using two memory signals, MEM_HOT_C{01/23}_N

1.3.2   PCI Express*

- The PCI Express* port(s) are fully-compliant with the *PCI Express* Base Specification*, Revision 3.0 (PCIe 3.0)

- Support for PCI Express* 3.0 (8.0 GT/s), 2.0 (5.0 GT/s), and 1.0 (2.5 GT/s)

- Up to 40 lanes of PCI Express* interconnect for general purpose PCI Express* devices at PCIe* 3.0 speeds that are configurable for up to 10 independent ports

  — Intel® Core™ i7-6950X Extreme Edition processor supports 40 lanes

  — Intel® Core™ i7-6900K processor supports 40 lanes

  — Intel® Core™ i7-6850K processor supports 40 lanes

  — Intel® Core™ i7-6800K processor supports 28 lanes

- Negotiating down to narrower widths is supported. See Figure 1-2.

  — x16 port (Port 2 and Port 3) may negotiate down to x8, x4, x2, or x1

  — x8 port (Port 1) may negotiate down to x4, x2, or x1

  — x4 port (Port 0) may negotiate down to x2, or x1

  — When negotiating down to narrower widths, there are caveats as to how lane reversal is supported

- Address Translation Services (ATS) 1.0 support

- Hierarchical PCI-compliant configuration mechanism for downstream devices

- Traditional PCI style traffic (asynchronous snooped, PCI ordering)

- PCI Express* extended configuration space. The first 256 bytes of configuration space aliases directly to the PCI compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.

- PCI Express* Enhanced Access Mechanism – accessing the device configuration space in a flat memory mapped fashion

- Automatic discovery, negotiation, and training of link out of reset

- Supports receiving and decoding 64 bits of address from PCI Express*

  — Memory transactions received from PCI Express* that go above the top of physical address space (when Intel VT-d is enabled, the check would be against the translated Host Physical Address (HPA)) are reported as errors by the processor.

  — Outbound access to PCI Express* will always have address bits 63:46 cleared

- Re-issues Configuration cycles that have been previously completed with the Configuration Retry status

- Power Management Event (PME) functions

- Message Signaled Interrupt (MSI and MSI-X) messages

- Degraded Mode support and Lane Reversal support

- Static lane numbering reversal and polarity inversion support

- Support for PCIe* 3.0 atomic operation, PCIe* 3.0 optional extension on atomic read-modify-write mechanism

Figure 1-2. PCI Express* Lane Partitioning and Direct Media Interface Gen 2 (DMI2)
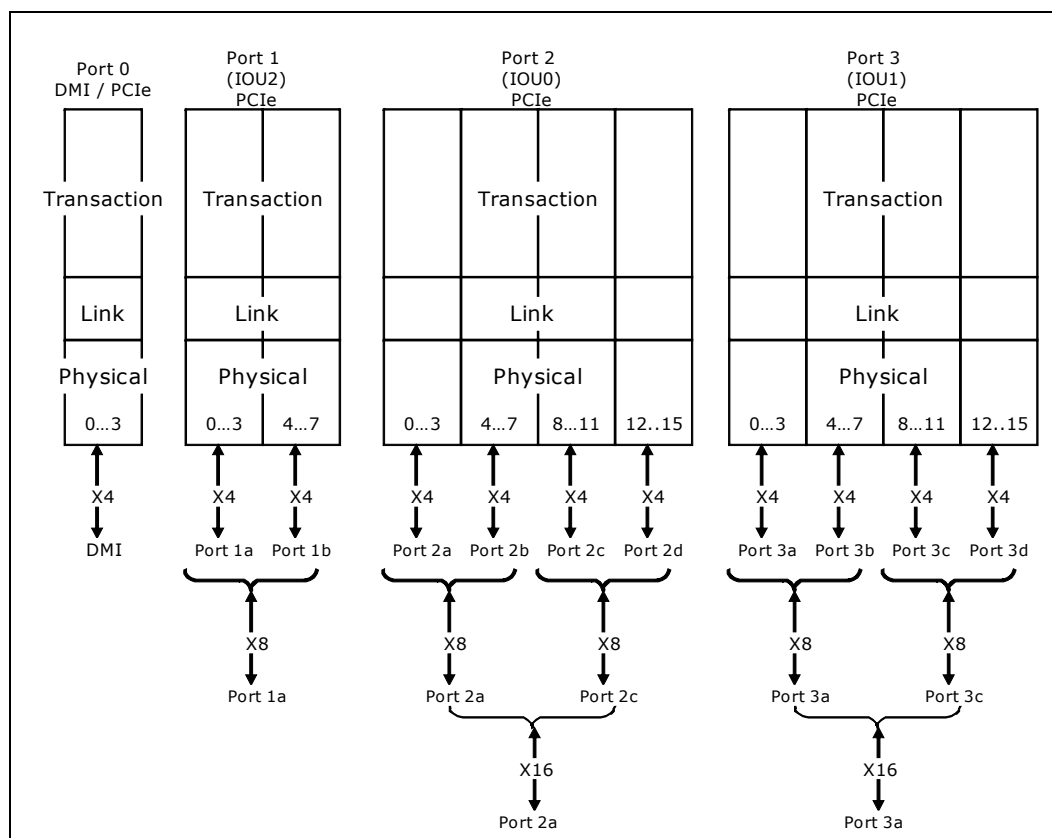
1.3.3 Direct Media Interface Gen 2 (DMI2)

- Serves as the chip-to-chip interface to the PCH
- The DMI2 port supports x4 link width and only operates in a x4 mode when in DMI2
- Operates at PCI Express* 1.0 or 2.0 speeds
- Transparent to software
- Processor and peer-to-peer writes and reads with 64-bit address support
- APIC and Message Signaled Interrupt (MSI) support. Will send Intel-defined "End of Interrupt" broadcast message when initiated by the processor.
- System Management Interrupt (SMI), SCI, and SERR error indication
- Static lane numbering reversal support
- Supports DMI2 virtual channels VC0, VC1, VCm, and VCp

1.3.4 Platform Environment Control Interface (PECI)

The PECI is a one-wire interface that provides a communication channel between a PECI client (the processor) and a PECI master (the PCH). Refer to the Processor Thermal Mechanical Specifications and Design Guide for additional details on PECI services available in the processor (Refer to the Related Documents section).

- Supports operation at up to 2 Mbps data transfers
- Link layer improvements to support additional services and higher efficiency over PECI 2.0 generation
- Services include processor thermal and estimated power information, control functions for power limiting, P-state and T-state control, and access for Machine Check Architecture registers and PCI configuration space (both within the processor package and downstream devices)
- Single domain (Domain 0) is supported

1.4 Power Management Support

1.4.1 Processor Package and Core States

- Advance Configuration and Power Interface (ACPI) C-states as implemented by the following processor C-states:
  — Package: PC0, PC1/PC1E, PC2, PC3, PC6 (Package C7 is not supported)
  — Core: CC0, CC1, CC1E, CC3, CC6, CC7
- Enhanced Intel SpeedStep Technology

1.4.2 System States Support

- S0, S1, S3, S4, S5

1.4.3 Memory Controller

- Multiple CKE power-down modes
- Multiple self-refresh modes
- Memory thermal monitoring using MEM_HOT_C01_N and MEM_HOT_C23_N signals

1.4.4 PCI Express*

- L1 ASPM power management capability; L0s is not supported

1.5 Thermal Management Support

- Digital Thermal Sensor with multiple on-die temperature zones
- Adaptive Thermal Monitor
- THERMTRIP_N and PROCHOT_N signal support
- On-Demand mode clock modulation
- Fan speed control with DTS
- Two integrated SMBus masters for accessing thermal data from DIMMs
- New Memory Thermal Throttling features using MEM_HOT_C{01/23}_N signals

1.6 Package Summary

The processor socket type is noted as LGA2011-v3. The processor package is a 52.5 x 45 mm FC-LGA package (LGA2011-v3). Refer to the Processor Thermal Mechanical Specification and Design Guide (see Related Documents section) for the package mechanical specifications.

1.7 Terminology

Table 1-1. Terminology (Sheet 1 of 3)

Term	Description
ASPM	Active State Power Management
Cbo	Caching Agent (also referred to as CA). It is a term used for the internal logic providing ring interface to LLC and Core. The Cbo is a functional unit in the processor.
DDR4	Fourth generation Double Data Rate SDRAM memory technology.
DMA	Direct Memory Access
DMI2	Direct Media Interface Gen2 operating at PCI Express 2.0 speed.
DSB	Data Stream Buffer. Part of the processor core architecture.
DTLB	Data Translation Look-aside Buffer. Part of the processor core architecture.
DTS	Digital Thermal Sensor
ECC	Error Correction Code
Enhanced Intel SpeedStep® Technology	Allows the operating system to reduce power consumption when performance is not needed.
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
Functional Operation	Refers to the normal operating conditions in which all processor specifications, including DC, AC, system bus, signal quality, mechanical, and thermal, are satisfied.
GSSE	Extension of the SSE/SSE2 (Streaming SIMD Extensions) floating point instruction set to 256b operands.
HA	Home Agent (HA)
ICU	Instruction Cache Unit. Part of the processor core architecture.
IFU	Instruction Fetch Unit. Part of the processor core.
IIO	The Integrated I/O Controller. An I/O controller that is integrated in the processor die.
IMC	The Integrated Memory Controller. A Memory Controller that is integrated in the processor die.
Integrated Heat Spreader (IHS)	A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture. Further details on Intel 64 architecture and programming model can be found at http://developer.intel.com/technology/intel64/.
Intel® Core™ i7 processor family for LGA2011-v3 Socket processor	Intel's 22-nm process based product. The processor supports Efficient Performance High-End Desktop platforms

Table 1-1.   Terminology (Sheet 2 of 3)

Term	Description
Intel® ME	Intel® Management Engine
Intel® QuickData Technology	Intel QuickData Technology is a platform solution designed to maximize the throughput of server data traffic across a broader range of configurations and server environments to achieve faster, scalable, and more reliable I/O.
Intel® QuickPath Interconnect (Intel® QPI)	A cache-coherent, link-based Interconnect specification for Intel processors, chipsets, and I/O bridge components.
Intel® Turbo Boost Technology	A feature that opportunistically enables the processor to run a faster frequency. This results in increased performance of both single and multi-threaded applications.
Intel® TXT	Intel® Trusted Execution Technology
Intel® Virtualization Technology (Intel® VT)	Processor Virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
Intel® VT-d	Intel® Virtualization Technology (Intel® VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or operating system) control, for enabling I/O device Virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
IOV	I/O Virtualization
IQ	Instruction Queue. Part of the core architecture.
IVR	Integrated Voltage Regulation (IVR): The processor supports several integrated voltage regulators.
Jitter	Any timing variation of a transition edge or edges from the defined Unit Interval (UI).
LGA2011-v3 Socket	The 2011-v3 land FC-LGA package mates with the system board through this surface mount, 2011-v3 contact socket.
LLC	Last Level Cache
LRDIMM	Load Reduced Dual In-line Memory Module
LRU	Least Recently Used. A term used in conjunction with cache allocation policy.
MESIF	Modified/Exclusive/Shared/Invalid/Forwarded. States used in conjunction with cache coherency
MLC	Mid Level Cache
NCTF	Non-Critical to Function: NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
PCH	Platform Controller Hub. The next generation chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features.
PCI Express 2.0	PCI Express Generation 2.0
PCI Express 3.0	The third generation PCI Express specification that operates at twice the speed of PCI Express 2.0 (8 Gb/s); PCI Express 3.0 is completely backward compatible with PCI Express 1.0 and 2.0.
PECI	Platform Environment Control Interface
Processor	Includes the 64-bit cores, uncore, I/Os, and package
Processor Core	The term "processor core" refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
R3QPI	Intel QPI Agent. An internal logic block providing interface between internal Ring and external Intel QPI.

Table 1-1.   Terminology (Sheet 3 of 3)

Term	Description
Rank	A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DDR4 DIMM.
RDIMM	Registered Dual In-line Memory Module
RTID	Request Transaction IDs are credits issued by the Cbo to track outstanding transaction, and the RTIDs allocated to a Cbo are topology dependent.
SCI	System Control Interrupt. Used in ACPI protocol.
SKU	Stock Keeping Unit (SKU) is a subset of a processor type with specific features, electrical, power and thermal specifications. Not all features are supported on all SKUs. A SKU is based on specific use condition assumption.
SMBus	System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system.
SSE	Intel$^®$ Streaming SIMD Extensions (Intel$^®$ SSE)
STD	Suspend-to-Disk
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
STR	Suspend-to-RAM
SVID	Serial Voltage Identification
TAC	Thermal Averaging Constant
TCC	Thermal Control Circuit
TDP	Thermal Design Power
TLP	Transaction Layer Packet
TSOD	Temperature Sensor On DIMM
UDIMM	Unbuffered Dual In-line Memory Module
Uncore	The portion of the processor comprising the shared LLC cache, Cbo, IMC, HA, PCU, Ubox, IIO and Intel QPI link interface.
Unit Interval	Signaling convention that is binary and unidirectional. In this binary signaling, one bit is sent for every edge of the forwarded clock, whether it be a rising edge or a falling edge. If a number of edges are collected at instances t_1, t_2, t_n,...., t_k then the UI at instance "n" is defined as: $UI_n = t_n - t_{n-1}$
V_{CCD}	DDR power rail
V_{CCIN}	Primary voltage input to the voltage regulators integrated into the processor.
V_{CCIO_IN}	IO voltage supply input
VSS	Processor ground
x1	Refers to a Link or Port with one Physical Lane
x16	Refers to a Link or Port with sixteen Physical Lanes
x4	Refers to a Link or Port with four Physical Lanes
x8	Refers to a Link or Port with eight Physical Lanes

1.8 Related Documents

Refer to the following documents for additional information.

Table 1-2. Related Documents

Document	Document Number/ Location
Intel® Core™ i7 Processor Family for the LGA2011-v3 Socket Datasheet, Volume 2 of 2	334207
Intel® Core™ i7 Processor Family for the LGA2011-v3 Socket Specification Update	334208
Advanced Configuration and Power Interface Specification 4.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/
PCI Express Base Specification, Revision 3.0	http://www.pcisig.com/
PCI Express Base Specification, Revision 2.1	
PCI Express Base Specification, Revision 1.1	
PCIe* Gen 3 Connector High Speed Electrical Test Procedure	325028-001 / http://www.intel.com/ content/www/us/en/io/pci-express/pci-express-architecture-devnet-resources.html
Connector Model Quality Assessment Methodology	326123-002 / http://www.intel.com/ content/www/us/en/ architecture-and-technology/ intel-connector-model-paper.html
DDR4 SDRAM Specification and Register Specification	http://www.jedec.org/
Intel® 64 and IA-32 Architectures Software Developer's Manuals • *Volume 1: Basic Architecture* • *Volume 2A: Instruction Set Reference, A-M* • *Volume 2B: Instruction Set Reference, N-Z* • *Volume 3A: System Programming Guide* • *Volume 3B: System Programming Guide* *Intel® 64 and IA-32 Architectures Optimization Reference Manual*	325462 / http://www.intel.com/ products/processor/manuals/ index.htm
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	http://www.intel.com/ content/www/us/en/ intelligent-systems/intel-technology/vt-directed-io-spec.html

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2 Interfaces

This chapter describes the functional behaviors supported by the processor. Topics covered include:

- System Memory Interface
- PCI Express* Interface
- Direct Media Interface 2 (DMI2) / PCI Express* Interface
- Platform Environment Control Interface (PECI)

2.1 System Memory Interface

2.1.1 System Memory Technology Support

The Integrated Memory Controller (IMC) supports DDR4 protocols with four independent 64-bit memory channels and supports 1 unbuffered DIMM per channel.

2.1.2 System Memory Timing Support

The IMC supports the following DDR4 Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1n indicates a new command may be issued every clock and 2n indicates a new command may be issued every 2 clocks. Command launch mode programming depends on the transfer rate and memory configuration.

2.2 PCI Express* Interface

This section describes the PCI Express* 3.0 interface capabilities of the processor. See the *PCI Express* Base Specification* for details of PCI Express* 3.0.

2.2.1 PCI Express* Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express* configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification.

The PCI Express* architecture is specified in three layers – Transaction Layer, Data Link Layer, and Physical Layer. The partitioning in the component is not necessarily along these same boundaries. Refer to the following figure for the PCI Express* Layering Diagram.

Figure 2-1. PCI Express* Layering Diagram
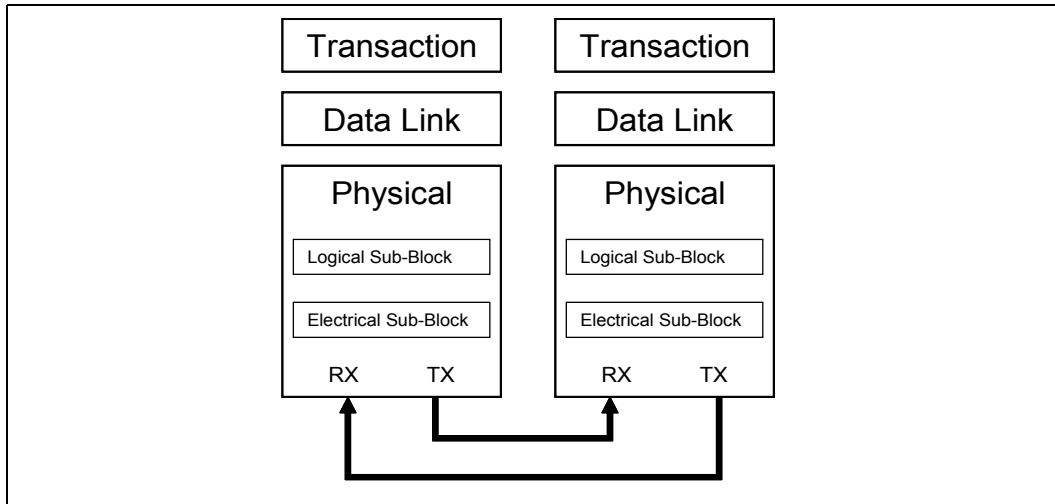
PCI Express* uses packets to communicate information between components. Packets are formed in the Transaction and Data Link Layers to carry the information from the transmitting component to the receiving component. As the transmitted packets flow through the other layers, the packets are extended with additional information necessary to handle packets at those layers. At the receiving side, the reverse process occurs and packets get transformed from their Physical Layer representation to the Data Link Layer representation and finally (for Transaction Layer Packets) to the form that can be processed by the Transaction Layer of the receiving device.

Figure 2-2. Packet Flow through the Layers
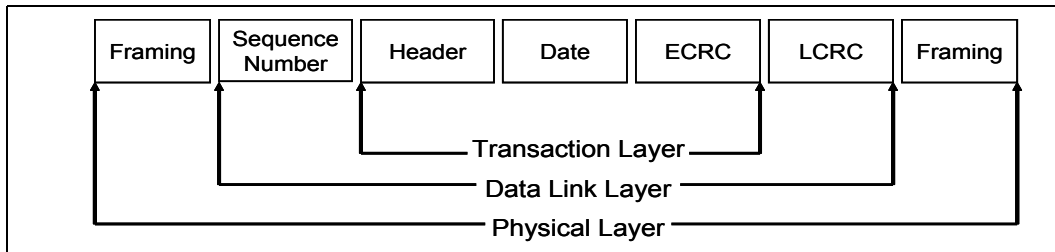
2.2.1.1 Transaction Layer

The upper layer of the PCI Express* architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

2.2.1.2 Data Link Layer

The middle layer in the PCI Express* stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

The transmission side of the Data Link Layer accepts TLPs assembled by the Transaction Layer, calculates and applies data protection code and TLP sequence number, and submits them to Physical Layer for transmission across the Link. The receiving Data Link Layer is responsible for checking the integrity of received TLPs and for submitting them to the Transaction Layer for further processing. On detection of TLP error(s), this layer is responsible for requesting retransmission of TLPs until information is correctly received, or the Link is determined to have failed. The Data Link Layer also generates and consumes packets that are used for Link management functions.

2.2.1.3 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry. It also includes logical functions related to interface initialization and maintenance. The Physical Layer exchanges data with the Data Link Layer in an implementation-specific format, and is responsible for converting this to an appropriate serialized format and transmitting it across the PCI Express* Link at a frequency and width compatible with the remote device.

2.2.2 PCI Express* Configuration Mechanism

The PCI Express* link is mapped through a PCI-to-PCI bridge structure.

PCI Express* extends the configuration space to 4096 bytes per-device/function, as compared to 256 bytes allowed by the Conventional PCI Specification. PCI Express* configuration space is divided into a PCI-compatible region (which consists of the first 256 bytes of a logical device's configuration space) and an extended PCI Express* region (which consists of the remaining configuration space). The PCI-compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express* configuration access mechanism described in the PCI Express* Enhanced Configuration Mechanism section.

The PCI Express* Host Bridge is required to translate the memory-mapped PCI Express* configuration space accesses from the host processor to PCI Express* configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only.

See the *PCI Express* Base Specification* for details of both the PCI-compatible and PCI Express* Enhanced configuration mechanisms and transaction rules.

2.3 Direct Media Interface 2 (DMI2) / PCI Express* Interface

Direct Media Interface 2 (DMI2) connects the processor to the Platform Controller Hub (PCH). DMI2 is similar to a four-lane PCI Express* supporting a speed of 5 GT/s per lane.

Note: Only DMI2 x4 configuration is supported.

2.3.1 DMI2 Error Flow

DMI2 can only generate SERR in response to errors, never SCI, SMI, MSI, PCI INT, or GPE. Any DMI2 related SERR activity is associated with Device 0.

2.3.2 Processor / PCH Compatibility Assumptions

The processor is compatible with the PCH and is not compatible with any previous Intel Memory Controller Hub (MCH) and Integrated Controller Hub (ICH) products.

2.3.3 DMI2 Link Down

The DMI2 link going down is a fatal, unrecoverable error. If the DMI2 data link goes to data link down, after the link was up, then the DMI2 link hangs the system by not allowing the link to retrain to prevent data corruption. This is controlled by the PCH.

Downstream transactions that had been successfully transmitted across the link prior to the link going down may be processed as normal. No completions from downstream, non-posted transactions are returned upstream over the DMI2 link after a link down event.

2.4 Platform Environment Control Interface (PECI)

The Platform Environment Control Interface (PECI) uses a single wire for self-clocking and data transfer. The bus requires no additional control lines. The physical layer is a self-clocked one-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a logic '0' or logic '1'. PECI also includes variable data transfer rate established with every message. In this way, it is highly flexible even though underlying logic is simple.

The interface design was optimized for interfacing to Intel processor and chipset components in both single processor and multiple processor environments. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

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3 Technologies

This chapter covers the following technologies:

- Intel® Virtualization Technology (Intel® VT)
- Security Technologies
- Intel® Hyper-Threading Technology (Intel® HT Technology)
- Intel® Turbo Boost Technology
- Enhanced Intel® SpeedStep® Technology
- Intel® Advanced Vector Extensions (Intel® AVX)

3.1 Intel® Virtualization Technology (Intel® VT)

Intel® Virtualization Technology (Intel® VT) makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to run simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets.

- **Intel® Virtualization Technology (Intel® VT) for Intel® 64 and IA-32 Intel® Architecture (Intel® VT-x)** adds hardware support in the processor to improve the virtualization performance and robustness. Intel VT-x specifications and functional descriptions are included in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B and is available at http://www.intel.com/products/processor/manuals/index.htm

- **Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d)** adds processor and uncore implementations to support and improve I/O virtualization performance and robustness. The Intel VT-d specification and other Intel VT documents can be referenced at http://www.intel.com/technology/virtualization/index.htm

3.1.1 Intel® VT-x Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide improved reliable virtualized platforms. By using Intel VT-x, a VMM is:

- **Robust:** VMMs no longer need to use para-virtualization or binary translation. This means that off-the-shelf operating systems and applications can be run without any special steps.

- **Enhanced:** Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.

- **More reliable:** Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.

- **More secure:** The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

3.1.2   Intel® VT-x Features

The processor core supports the following Intel VT-x features:

- Extended Page Tables (EPT)

  — hardware assisted page table virtualization.

  — eliminates VM exits from guest operating system to the VMM for shadow page-table maintenance.

- Virtual Processor IDs (VPID)

  — Ability to assign a VM ID to tag processor core hardware structures (such as, TLBs).

  — This avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.

- Guest Preemption Timer

  — Mechanism for a VMM to preempt the execution of a guest operating system after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest.

  — The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees.

- Descriptor-Table Exiting

  — Descriptor-table exiting allows a VMM to protect a guest operating system from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).

  — A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

- Pause Loop Exiting (PLE)

  — PLE aims to improve virtualization performance and enhance the scaling of virtual machines with multiple virtual processors

  — PLE attempts to detect lock-holder preemption in a VM and helps the VMM to make better scheduling decisions

3.1.3   Intel® VT-d Objectives

The key Intel VT-d objectives are domain-based isolation and hardware-based virtualization. A domain can be abstractly defined as an isolated environment in a platform to which a subset of host physical memory is allocated. Virtualization allows for the creation of one or more partitions on a single system. This could be multiple partitions in the same operating system, or there can be multiple operating system instances running on the same system – offering benefits such as system consolidation, legacy migration, activity partitioning, or security.

3.1.3.1 Intel® VT-d Features Supported

The processor supports the following Intel VT-d features:

- Root entry, context entry, and default context
- Support for 4-K page sizes only
- Support for register-based fault recording only (for single entry only) and support for MSI interrupts for faults
  — Support for fault collapsing based on Requester ID
- Support for both leaf and non-leaf caching
- Support for boot protection of default page table
  — Support for non-caching of invalid page table entries
- Support for hardware based flushing of translated but pending writes and pending reads upon IOTLB invalidation
- Support for page-selective IOTLB invalidation
- Support for ARI (Alternative Requester ID – a PCI SIG ECR for increasing the function number count in a PCIe* device) to support I/O Virtualization (IOV) devices
- Improved invalidation architecture
- End point caching support (ATS)
- Interrupt remapping

3.1.4 Intel® Virtualization Technology Processor Extensions

The processor supports the following Intel VT processor extension features:

- Large Intel VT-d Pages
  — Adds 2MB and 1GB page sizes to Intel VT-d implementations
  — Matches current support for Extended Page Tables (EPT)
  — Ability to share processor EPT page-table (with super-pages) with Intel VT-d
  — Benefits:
    - Less memory foot-print for I/O page-tables when using super-pages
    - Potential for improved performance – due to shorter page-walks, allows hardware optimization for IOTLB
- Transition latency reductions expected to improve virtualization performance without the need for VMM enabling. This reduces the VMM overheads further and increase virtualization performance.

3.2 Security Technologies

3.2.1 Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI) Instructions

These instructions enable fast and secure data encryption and decryption, using the Advanced Encryption Standard (Intel AES-NI) which is defined by FIPS Publication number 197. Since Intel AES-NI is the dominant block cipher, and it is deployed in various protocols, the new instructions will be valuable for a wide range of applications.

The architecture consists of six instructions that offer full hardware support for Intel AES-NI. Four instructions support the Intel AES-NI encryption and decryption, and the other two instructions support the Intel AES-NI key expansion. Together, they offer a significant increase in performance compared to pure software implementations.

The Intel AES-NI instructions have the flexibility to support all three standard Intel AES-NI key lengths, all standard modes of operation, and even some nonstandard or future variants.

Beyond improving performance, the Intel AES-NI instructions provide important security benefits. Since the instructions run in data-independent time and do not use lookup tables, the instructions help in eliminating the major timing and cache-based attacks that threaten table-based software implementations of Intel AES-NI. In addition, these instructions make AES simple to implement, with reduced code size. This helps reducing the risk of inadvertent introduction of security flaws, such as difficult-to-detect side channel leaks.

3.2.2 Execute Disable Bit

The Intel Execute Disable Bit functionality can help prevent certain classes of malicious buffer overflow attacks when combined with a supporting operating system.

- Allows the processor to classify areas in memory by where application code can execute and where it cannot.
- When a malicious worm attempts to insert code in the buffer, the processor disables code execution, preventing damage and worm propagation.

3.3 Intel® Hyper-Threading Technology (Intel® HT Technology)

The processor supports Intel® Hyper-Threading Technology (Intel® HT Technology) that allows an execution core to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support.

For more information on Intel Hyper-Threading Technology, see http://www.intel.com/products/ht/hyperthreading_more.htm.

3.4 Intel® Turbo Boost Max Technology 3.0

Intel Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating frequency if it is operating below power, temperature, and current limits. The result is increased performance in multi-threaded and single threaded workloads. It should be enabled in the BIOS for the processor to operate with maximum performance. Refer to the *BIOS Writer's Guide (BWG)* for enabling details (see Related Documents section).

Processors with Intel Turbo Boost Max Technology 3.0 feature contain at least one processor core whose maximum turbo frequency is higher than the others. To realize the higher performance benefit of such a core, targeted applications must run **on that core**. The processor core with the higher frequency may vary from one processor to another. BIOS calls to the mailbox interface is used to identify the core with the higher performance.

3.4.1 Intel® Turbo Boost Operating Frequency

The processor's rated frequency assumes that all execution cores are running an application at the thermal design power (TDP). However, under typical operation, not all cores are active. Therefore, most applications are consuming less than the TDP at the rated frequency. To take advantage of the available TDP headroom, the active cores can increase their operating frequency.

To determine the highest performance frequency amongst active cores, the processor takes the following into consideration:

- number of cores operating in the C0 state
- estimated current consumption
- estimated power consumption
- die temperature

Any of these factors can affect the maximum frequency for a given workload. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

Note: Intel Turbo Boost Technology is only active if the operating system is requesting the P0 state.

3.5 Enhanced Intel® SpeedStep® Technology

The processor supports Enhanced Intel SpeedStep® Technology as an advanced means of enabling very high performance while also meeting the power-conservation needs of the platform.

Enhanced Intel SpeedStep Technology builds upon that architecture using design strategies that include the following:

- **Separation between Voltage and Frequency Changes**. By stepping voltage up and down in small increments separately from frequency changes, the processor is able to reduce periods of system unavailability that occur during frequency change. Thus, the system is able to transition between voltage and frequency states more often, providing improved power/performance balance.

- **Clock Partitioning and Recovery**. The bus clock continues running during state transition, even when the core clock and Phase-Locked Loop are stopped, which allows logic to remain active. The core clock can also restart more quickly under Enhanced Intel SpeedStep Technology.

3.6 Intel® Advanced Vector Extensions (Intel® AVX)

Intel Advanced Vector Extensions (Intel AVX) is a new 256-bit vector SIMD extension of Intel Architecture. The introduction of Intel AVX started with the 2nd Generation Intel® Core™ processor family. Intel AVX accelerates the trend of parallel computation in general purpose applications like image, video and audio processing, engineering applications (such as 3D modeling and analysis), scientific simulation, and financial analysts.

Intel AVX is a comprehensive ISA extension of the Intel 64 Architecture. The main elements of Intel AVX are:

- Support for wider vector data (up to 256-bit) for floating-point computation
- Efficient instruction encoding scheme that supports 3 operand syntax and headroom for future extensions
- Flexibility in programming environment, ranging from branch handling to relaxed memory alignment requirements
- New data manipulation and arithmetic compute primitives, including broadcast, permute, fused-multiply-add, and so on
- Floating point bit depth conversion (Float 16)
    - A group of 4 instructions that accelerate data conversion between 16-bit floating point format to 32-bit and vice versa.
    - This benefits image processing and graphical applications allowing compression of data so less memory and bandwidth is required.

The key advantages of Intel AVX are:

- **Performance** – Intel AVX can accelerate application performance using data parallelism and scalable hardware infrastructure across existing and new application domains:
    — 256-bit vector data sets can be processed up to twice the throughput of 128-bit data sets
    — Application performance can scale up with the number of hardware threads and number of cores
    — Application domain can scale out with advanced platform interconnect fabrics
- **Power Efficiency** – Intel AVX is extremely power efficient. Incremental power is insignificant when the instructions are unused or scarcely used. Combined with the high performance that it can deliver, applications that lend themselves heavily to using Intel AVX can be much more energy efficient and realize a higher performance-per-watt.
- **Extensibility** – Intel AVX has built-in extensibility for the future vector extensions:
    — Operating System context management for vector-widths beyond 256 bits is streamlined
    — Efficient instruction encoding allows unlimited functional enhancements:
        - Vector width support beyond 256 bits

- 256-bit Vector Integer processing
- Additional computational and/or data manipulation primitives

- **Compatibility** – Intel AVX is backward compatible with previous ISA extensions including Intel SSE4:

  — Existing Intel SSE applications/library can:
    - Run unmodified and benefit from processor enhancements
    - Recompile existing Intel® SSE intrinsic using compilers that generate Intel AVX code
    - Inter-operate with library ported to Intel AVX

  — Applications compiled with Intel AVX can inter-operate with existing Intel SSE libraries.

§

4 Signal Descriptions

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category.

4.1 System Memory Interface

Table 4-1. Memory Channel DDR0, DDR1, DDR2, DDR3

Signal Name	Description
DDR{0/1/2/3}_ACT_N	Activate. When asserted, indicates MA[16:14] are command signals (RAS_N, CAS_N, WE_N).
DDR{0/1/2/3}_ALERT_N	Parity Error detected by the DIMM (one for each channel).
DDR{0/1/2/3}_BA[1:0]	Bank Address. Defines which bank is the destination for the current Activate, Read, Write, or Precharge command.
DDR{0/1/2/3}_BG[1:0]	Bank Group: Defines which bank group is the destination for the current Active, Read, Write or Precharge command. BG0 also determines which mode register is to be accessed during a MRS cycle.
DDR{0/1/2/3}_CAS_N	Column Address Strobe. Multiplexed with DDR{0/1/2/3}_MA[15].
DDR{0/1/2/3}_CID[4:0]	Chip ID. Used to select a single die out of the stack of a 3DS device. CID[4:3] are multiplexed with CS_N[7:6], respectively. CID[1:0] are multiplexed with CS_N[3:2], respectively.
DDR{0/1/2/3}_CKE[5:0]	Clock Enable.
DDR{0/1/2/3}_CLK_DN[3:0] DDR{0/1/2/3}_CLK_DP[3:0]	Differential clocks to the DIMM. All command and control signals are valid on the rising edge of clock.
DDR{0/1/2/3}_CS_N[9:0]	Chip Select. Each signal selects one rank as the target of the command and address. CS_N[7:6] are multiplexed with CID[4:3], respectively. CS_N[3:2] are multiplexed with CID[1:0], respectively.
DDR{0/1/2/3}_DQ[63:0]	Data Bus. DDR4 Data bits.
DDR{0/1/2/3}_DQS_DP[17:0] DDR{0/1/2/3}_DQS_DN[17:0]	Data strobes. Differential pair, Data/ECC Strobe. Differential strobes latch data/ECC for each DRAM. Different numbers of strobes are used depending on whether the connected DRAMs are x4,x8. Driven with edges in center of data, receive edges are aligned with data edges.
DDR{0/1/2/3}_ECC[7:0]	Check bits. An error correction code is driven along with data on these lines for DIMMs that support that capability
DDR{0/1/2/3}_MA[17:0]	Memory Address. Selects the Row address for Reads and writes, and the column address for activates. Also used to set values for DRAM configuration registers. MA[16], MA[15], and MA[14] are multiplexed with RAS_N, CAS_N, and WE_N, respectively.
DDR{0/1/2/3}_PAR	Even parity across Address and Command.
DDR{0/1/2/3}_ODT[5:0]	On Die Termination. Enables DRAM on die termination during Data Write or Data Read transactions.
DDR{0/1/2/3}_RAS_N	Row Address Strobe. Multiplexed with DDR{0/1/2/3}_MA[16].
DDR{0/1/2/3}_WE_N	Write Enable. Multiplexed with DDR{0/1/2/3}_MA[14].

Table 4-2.   Memory Channel Miscellaneous

Signal Name	Description
DDR_RESET_C01_N DDR_RESET_C23_N	System memory reset: Reset signal from processor to DRAM devices on the DIMMs. DDR_RESET_C01_N is used for memory channels 0 and 1 while DDR_RESET_C23_N is used for memory channels 2 and 3.
DDR_SCL_C01 DDR_SCL_C23	SMBus clock for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs. DDR_SCL_C01 is used for memory channels 0 and 1 while DDR_SCL_C23 is used for memory channels 2 and 3.
DDR_SDA_C01 DDR_SDA_C23	SMBus data for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs. DDR_SDA_C01 is used for memory channels 0 and 1 while DDR_SDA_C23 is used for memory channels 2 and 3.
DDR01_VREF DDR23_VREF	Voltage reference for CMD/ADD to the DIMMs. DDR01_VREF is used for memory channels 0 and 1 while DDR23_VREF is used for memory channels 2 and 3.
DRAM_PWR_OK_C01 DRAM_PWR_OK_C23	Power good for V_{CCD} rail used by the DRAM. This is an input signal used to indicate the V_{CCD} power supply is stable for memory channels 0 & 1 and channels 2 & 3.

4.2   PCI Express* Based Interface Signals

Note: PCI Express* Ports 1, 2 and 3 Signals are receive and transmit differential pairs.

Table 4-3.   PCI Express Port 1 Signals

Signal Name	Description
PE1A_RX_DN[3:0] PE1A_RX_DP[3:0]	PCIe Receive Data Input
PE1B_RX_DN[7:4] PE1B_RX_DP[7:4]	PCIe Receive Data Input
PE1A_TX_DN[3:0] PE1A_TX_DP[3:0]	PCIe Transmit Data Output
PE1B_TX_DN[7:4] PE1B_TX_DP[7:4]	PCIe Transmit Data Output

Table 4-4.   PCI Express* Port 2 Signals (Sheet 1 of 2)

Signal Name	Description
PE2A_RX_DN[3:0] PE2A_RX_DP[3:0]	PCIe Receive Data Input
PE2B_RX_DN[7:4] PE2B_RX_DP[7:4]	PCIe Receive Data Input
PE2C_RX_DN[11:8] PE2C_RX_DP[11:8]	PCIe Receive Data Input
PE2D_RX_DN[15:12] PE2D_RX_DP[15:12]	PCIe Receive Data Input
PE2A_TX_DN[3:0] PE2A_TX_DP[3:0]	PCIe Transmit Data Output

Table 4-4.   PCI Express* Port 2 Signals (Sheet 2 of 2)

Signal Name	Description
PE2B_TX_DN[7:4] PE2B_TX_DP[7:4]	PCIe Transmit Data Output
PE2C_TX_DN[11:8] PE2C_TX_DP[11:8]	PCIe Transmit Data Output
PE2D_TX_DN[15:12] PE2D_TX_DP[15:12]	PCIe Transmit Data Output

Table 4-5.   PCI Express* Port 3 Signals

Signal Name	Description
PE3A_RX_DN[3:0] PE3A_RX_DP[3:0]	PCIe Receive Data Input
PE3B_RX_DN[7:4] PE3B_RX_DP[7:4]	PCIe Receive Data Input
PE3C_RX_DN[11:8] PE3C_RX_DP[11:8]	PCIe Receive Data Input
PE3D_RX_DN[15:12] PE3D_RX_DP[15:12]	PCIe Receive Data Input
PE3A_TX_DN[3:0] PE3A_TX_DP[3:0]	PCIe Transmit Data Output
PE3B_TX_DN[7:4] PE3B_TX_DP[7:4]	PCIe Transmit Data Output
PE3C_TX_DN[11:8] PE3C_TX_DP[11:8]	PCIe Transmit Data Output
PE3D_TX_DN[15:12] PE3D_TX_DP[15:12]	PCIe Transmit Data Output

Table 4-6.   PCI Express* Miscellaneous Signals

Signal Name	Description
PE_HP_SCL	PCI Express* Hot-Plug SMBus Clock: Provides PCI Express* hot-plug support using a dedicated SMBus interface. Requires an external general purpose input/output (GPIO) expansion device on the platform.
PE_HP_SDA	PCI Express* Hot-Plug SMBus Data: Provides PCI Express* hot-plug support using a dedicated SMBus interface. Requires an external general purpose input/output (GPIO) expansion device on the platform.

4.3   Direct Media Interface 2 (DMI2) Signals

Table 4-7.   Direct Media Interface 2 (DMI2) Signals

Signal Name	Description
DMI_RX_DN[3:0] DMI_RX_DP[3:0]	DMI2 Receive Data Input
DMI_TX_DP[3:0] DMI_TX_DN[3:0]	DMI2 Transmit Data Output

4.4 Intel® QuickPath Interconnect (Intel® QPI) Signals

Table 4-8. Intel QPI Port 0 and 1 Signals

Signal Name	Description
QPI{0/1}_CLKRX_DN/DP	Reference Clock Differential Input. These pins provide the PLL reference clock differential input. 100 MHz typical.
QPI{0/1}_CLKTX_DN/DP	Reference Clock Differential Output. These pins provide the PLL reference clock differential input. 100 MHz typical.
QPI{0/1}_DRX_DN/DP[19:0]	QPI Receive data input.
QPI{0/1}_DTX_DN/DP[19:0]	QPI Transmit data output.

4.5 Platform Environment Control Interface (PECI) Signal

Table 4-9. Platform Environment Control Interface (PECI) Signal

Signal Name	Description
PECI	PECI (Platform Environment Control Interface) is the serial sideband interface to the processor and is used primarily for thermal, power and error management.

4.6 System Reference Clock Signals

Table 4-10. System Reference Clock (BCLK{0/1}) Signals

Signal Name	Description
BCLK{0/1}_D[N/P]	Reference Clock Differential input. These pins provide the required reference inputs to various PLLs inside the processor, such as Intel QPI and PCIe. BCLK0 and BCLK1 run at 100 MHz from the same clock source.

4.7 JTAG and TAP Signals

Table 4-11. JTAG and TAP Signals (Sheet 1 of 2)

Signal Name	Description
BPM_N[7:0]	Breakpoint and Performance Monitor Signals: I/O signals from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. These are 100 MHz signals.
PRDY_N	Probe Mode Ready is a processor output used by debug tools to determine processor debug readiness.
PREQ_N	Probe Mode Request is used by debug tools to request debug operation of the processor.
TCK	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.

Table 4-11. JTAG and TAP Signals (Sheet 2 of 2)

Signal Name	Description
TDO	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TMS	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRST_N	TRST_N (Test Reset) resets the Test Access Port (TAP) logic. TRST_N must be driven low during power on Reset.

4.8 Serial VID Interface (SVID) Signals

Table 4-12. SVID Signals

Signal Name	Description
SVIDALERT_N	Serial VID alert.
SVIDCLK	Serial VID clock.
SVIDDATA	Serial VID data out.

4.9 Processor Asynchronous Sideband and Miscellaneous Signals

Table 4-13. Processor Asynchronous Sideband Signals (Sheet 1 of 2)

Signal Name	Description
CATERR_N	Indicates that the system has experienced a fatal or catastrophic error and cannot continue to operate. The processor will assert CATERR_N for unrecoverable machine check errors and other internal unrecoverable errors. It is expected that every processor in the system will wire-OR CATERR_N for all processors. Since this is an I/O land, external agents are allowed to assert this land which will cause the processor to take a machine check exception. This signal is sampled after PWRGOOD assertion. On the processor, CATERR_N is used for signaling the following types of errors: • Legacy MCERR's, CATERR_N is asserted for 16 BCLKs. • Legacy IERR's, CATERR_N remains asserted until warm or cold reset.
ERROR_N[2:0]	Error status signals for integrated I/O (IIO) unit: • 0 = Hardware correctable error (no operating system or firmware action necessary) • 1 = Non-fatal error (operating system or firmware action required to contain and recover) • 2 = Fatal error (system reset likely required to recover)
MEM_HOT_C01_N MEM_HOT_C23_N	Memory throttle control. Signals external BMC-less controller that DIMM is exceeding temperature limit and needs to increase to max fan speed. MEM_HOT_C01_N and MEM_HOT_C23_N signals have two modes of operation - input and output mode. Input mode is externally asserted and is used to detect external events such as VR_HOT# from the memory voltage regulator and causes the processor to throttle the appropriate memory channels. Output mode is asserted by the processor known as level mode. In level mode, the output indicates that a particular branch of memory subsystem is hot. MEM_HOT_C01_N is used for memory channels 0 & 1 while MEM_HOT_C23_N is used for memory channels 2 & 3.
MSMI_N	Machine Check Exception (MCE) is signaled via this pin when eMCA2 is enabled.

Table 4-13. Processor Asynchronous Sideband Signals (Sheet 2 of 2)

Signal Name	Description
PMSYNC	Power Management Sync. A sideband signal to communicate power management status from the Platform Controller Hub (PCH) to the processor.
PROCHOT_N	PROCHOT_N will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal can also be driven to the processor to activate the Thermal Control Circuit. This signal is sampled after PWRGOOD assertion. If PROCHOT_N is asserted at the de-assertion of RESET_N, the processor will tri-state its outputs.
PWRGOOD	PWRGOOD is a processor input. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. PWRGOOD transitions from inactive to active when all supplies except VCCIN are stable. The signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
RESET_N	Global reset signal. Asserting the RESET_N signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. *Note:* Some PLL, Intel QuickPath Interconnect, and error states are not affected by reset and only PWRGOOD forces them to a known state.
THERMTRIP_N	Assertion of THERMTRIP_N (Thermal Trip) indicates one of two possible critical over-temperature conditions: One, the processor junction temperature has reached a level beyond which permanent silicon damage may occur and Two, the system memory interface has exceeded a critical temperature limit set by BIOS. Measurement of the processor junction temperature is accomplished through multiple internal thermal sensors that are monitored by the Digital Thermal Sensor (DTS). Simultaneously, the Power Control Unit (PCU) monitors external memory temperatures using the dedicated SMBus interface to the DIMMs. If any of the DIMMs exceed the BIOS defined limits, the PCU will signal THERMTRIP_N to prevent damage to the DIMMs. Once activated, the processor will stop all execution and shut down all PLLs. To further protect the processor, its core voltage (V_{CCIN}), V_{CCD}, V_{CCIO_IN}, V_{CCPECI} supplies must be removed following the assertion of THERMTRIP_N. Once activated, THERMTRIP_N remains latched until RESET_N is asserted. While the assertion of the RESET_N signal may de-assert THERMTRIP_N, if the processor's junction temperature remains at or above the trip level, THERMTRIP_N will again be asserted after RESET_N is de-asserted. This signal can also be asserted if the system memory interface has exceeded a critical temperature limit set by BIOS.

Table 4-14. Miscellaneous Signals (Sheet 1 of 2)

Signal Name	Description
BIST_ENABLE	BIST Enable Strap. Input which allows the platform to enable or disable built-in self test (BIST) on the processor. This signal is pulled up on the die. Refer to Table 5-6, "Signals with On-Die Weak Pull-Up/Pull-Down Resistors" on page 50 for details.
BMCINIT	BMC Initialization Strap. Indicates whether Service Processor Boot Mode should be used. Used in combination with FRMAGENT and SOCKET_ID inputs. 0 = Service Processor Boot Mode Disabled. Example boot modes: Local PCH (this processor hosts a legacy PCH with firmware behind it), Intel QPI Link Boot (for processors one hop away from the FW agent), or Intel QPI Link Init (for processors more than one hop away from the firmware agent). 1 = Service Processor Boot Mode Enabled. In this mode of operation the processor performs the absolute minimum internal configuration and then waits for the Service Processor to complete its initialization. The socket boots after receiving a "GO" handshake signal using a firmware scratchpad register. This signal is pulled down on the die. Refer to Table 5-6, "Signals with On-Die Weak Pull-Up/Pull-Down Resistors" on page 50 for details.
DEBUG_EN_N	This pin is used to force debug to be enabled when the ITP is connected to the main board. This allows debug to occur beginning from cold boot.
EAR_N	External Alignment of Reset, used to bring the processor up into a deterministic state. This signal is pulled up on the die. Refer to Table 5-6, "Signals with On-Die Weak Pull-Up/Pull-Down Resistors" on page 50 for details.
FIVR_FAULT	Indicates an internal error has occurred with the integrated voltage regulator. The FIVR_FAULT signal can be sampled any time after 1.5 ms after the assertion of PWRGOOD. FIVR_FAULT must be qualified by THERMTRIP_N assertion.
FRMAGENT	Bootable Firmware Agent Strap. This input configuration strap used in combination with SOCKET_ID to determine whether the socket is a legacy socket, bootable firmware agent is present, and DMI links are used in PCIe* mode (instead of DMI2 mode). The firmware flash ROM is located behind the local PCH attached to the processor using the DMI2 interface.This signal is pulled down on the die. Refer to Table 5-6, "Signals with On-Die Weak Pull-Up/Pull-Down Resistors" on page 50 for details.
PM_FAST_WAKE_N	Power Management Fast Wake. Enables quick package C3–C6 exits of all sockets. Asserted if any socket detects a break from package C3–C6 state requiring all sockets to exit the low-power state to service a snoop, memory access, or interrupt. Expected to be wired-OR among all processor sockets within the platform.
PROC_ID	This output can be used by the platform to determine if the installed processor is an Intel® Core™ processor family for the LGA2011-v3 socket processor or a future processor planned for the platforms. There is no connection to the processor silicon for this signal. The processor package grounds or floats the pin to set '0' or '1', respectively. 1 = Intel® Core™ processor family for the LGA2011-v3 socket processor 0 = Reserved for future use
RSVD	RESERVED. All signals that are RSVD must be left unconnected on the board. Refer to Section 5.2.9, "Reserved or Unused Signals" for details.
SAFE_MODE_BOOT	Safe Mode Boot Strap. SAFE_MODE_BOOT allows the processor to wake up safely by disabling all clock gating. This allows BIOS to load registers or patches if required. This signal is sampled after PWRGOOD assertion. The signal is pulled down on the die. Refer to Table 5-6, "Signals with On-Die Weak Pull-Up/Pull-Down Resistors" on page 50 for details.
SKTOCC_N	SKTOCC_N (Socket Occupied) is used to indicate that a processor is present. This is pulled to ground on the processor package. There is no connection to the processor silicon for this signal.

Table 4-14. Miscellaneous Signals (Sheet 2 of 2)

Signal Name	Description
SOCKET_ID[1:0]	Socket ID Strap. Socket identification configuration straps for establishing the PECI address, Intel® QPI Node ID, and other settings. This signal is used in combination with FRMAGENT to determine whether the socket is a legacy socket, bootable firmware agent is present, and DMI links are used in PCIe* mode (instead of DMI2 mode). Each processor socket consumes one Node ID, and there are 128 Home Agent tracker entries. This signal is pulled down on the die. Refer to Table 5-6, "Signals with On-Die Weak Pull-Up/Pull-Down Resistors" on page 50 for details.
TEST[3:0]	Test[3:0] must be individually connected to an appropriate power source or ground through a resistor for proper processor operation.
TXT_AGENT	Intel® Trusted Execution Technology (Intel® TXT) Agent Strap. 0 = Default. The socket is not the Intel TXT Agent. 1 = The socket is the Intel TXT Agent. The legacy socket (identified by SOCKET_ID[1:0] = 00b) with Intel TXT Agent should always set the TXT_AGENT to 1b. This signal is pulled down on the die. Refer to Table 5-6, "Signals with On-Die Weak Pull-Up/Pull-Down Resistors" on page 50 for details.
TXT_PLTEN	Intel Trusted Execution Technology (Intel TXT) Platform Enable Strap. 0 = The platform is not Intel TXT enabled. All sockets should be set to zero. Scalable DP (sDP) platforms should choose this setting if the Node Controller does not support Intel TXT. 1 = Default. The platform is Intel TXT enabled. All sockets should be set to one. In a non-Scalable DP platform this is the default. When this is set, Intel TXT functionality requires the user to explicitly enable Intel TXT using BIOS setup. This signal is pulled up on the die. Refer to Table 5-6, "Signals with On-Die Weak Pull-Up/Pull-Down Resistors" on page 50 for details. This processor does not support Intel TXT. This signal should be strapped to disable Intel TXT.

4.10 Processor Power and Ground Supplies

Table 4-15. Power and Ground Signals

Signal Name	Description
V_{CCIN}	Input to the Integrated Voltage Regulator (IVR) for the processor cores, lowest level caches (LLC), ring interface, PLL, IO, and home agent. It is provided by a VR 12.5 compliant motherboard voltage regulator (MBVR) for each CPU socket. The output voltage of this MBVR is controlled by the processor, using the serial voltage ID (SVID) bus.
V_{CCIN_SENSE} $V_{SS\_VCCIN\_SENSE}$	V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$ are remote sense signals for V_{CCIN} MBVR12.5 and are used by the voltage regulator to ensure accurate voltage regulation. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage remains within specification.
V_{CCD_01} V_{CCD_23}	Fixed 1.2V power supply for the processor system memory interface. Provided by two MBVR 12.0 or 12.5 compliant regulators per CPU socket. V_{CCD_01} and V_{CCD_23} are used for memory channels 0 &1 and 2 & 3, respectively. The valid voltage of this supply (1.20V) is configured by BIOS after determining the operating voltages of the installed memory. V_{CCD_01} and V_{CCD_23} will also be referred to as V_{CCD}. *Note:* The processor must be provided V_{CCD_01} and V_{CCD_23} for proper operation, even in configurations where no memory is populated. A MBVR 12.0 or 12.5 controller is required.
V_{SS}	Processor ground return.
V_{CCIO_IN}	IO voltage supply input.
V_{CCPECI}	Power supply for PECI. Refer to the PDG for specific connection options for this pin.

§ §

5 Electrical Specifications

5.1 Integrated Voltage Regulation

A feature to the processor is the integration of platform voltage regulators into the processor. Due to this integration, the processor has one main voltage rail (VCCIN) and a voltage rail for the memory interface (VCCD01, VCCD23 - one for each memory channel pair), compared to five voltage rails (VCC, VTTA, VTTD, VSA, and VCCPLL) on previous processors. The VCCIN voltage rail will supply the integrated voltage regulators which in turn will regulate to the appropriate voltages for the cores, cache, and system agents. This integration allows the processor to better control on-die voltages to optimize for both performance and power savings. The processor VCCIN rail will remain a sVID -based voltage with a loadline similar to the core voltage rail (called VCC) in previous processors.

5.2 Processor Signaling

The processor includes 2011 lands that use various signaling technologies. Signals are grouped by electrical characteristics and buffer type into various signal groups. These include DDR4 (Reference Clock, Command, Control, and Data), PCI Express*, DMI2, Intel® QuickPath Interconnect, Platform Environmental Control Interface (PECI), System Reference Clock, SMBus, JTAG and Test Access Port (TAP), SVID Interface, Processor Asynchronous Sideband, Miscellaneous, and Power/Other signals. Refer to Table 5-5, "Signal Groups" on page 47 for details.

Intel strongly recommends performing analog simulations of all interfaces.

5.2.1 System Memory Interface Signal Groups

The system memory interface uses DDR4 technology that consists of numerous signal groups. These include: Reference Clocks, Command Signals, Control Signals, and Data Signals. Each group consists of numerous signals that may use various signaling technologies. Refer to Table 5-5, "Signal Groups" on page 47 for further details. Throughout this chapter, the system memory interface may be referred to as DDR4.

5.2.2 PCI Express* Signals

The PCI Express Signal Group consists of PCI Express* ports 1, 2, and 3, and PCI Express miscellaneous signals. Refer to Table 5-5, "Signal Groups" on page 47 for further details.

5.2.3 Direct Media Interface 2 (DMI2) / PCI Express* Signals

The Direct Media Interface Gen 2 (DMI2) sends and receives packets and/or commands to the PCH. The DMI2 is an extension of the standard PCI Express Specification. The DMI2/PCI Express signals consist of DMI2 receive and transmit input/output signals and a control signal to select DMI2 or PCIe* 2.0 operation for port 0. Refer to Table 5-5, "Signal Groups" on page 47 for further details.

5.2.4 Platform Environmental Control Interface (PECI)

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external system management logic and thermal monitoring devices. The processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read processor temperature, perform processor manageability functions, and manage processor interface tuning and diagnostics.

The PECI interface operates at a nominal voltage set by V_{CCPECI}. The set of DC electrical specifications shown in PECI DC Specifications is used with devices normally operating from a V_{CCPECI} interface supply.

5.2.4.1 Input Device Hysteresis

The PECI client and host input buffers must use a Schmitt-triggered input design for improved noise immunity. Refer to the following figure and PECI DC Specifications.

Figure 5-1. Input Device Hysteresis
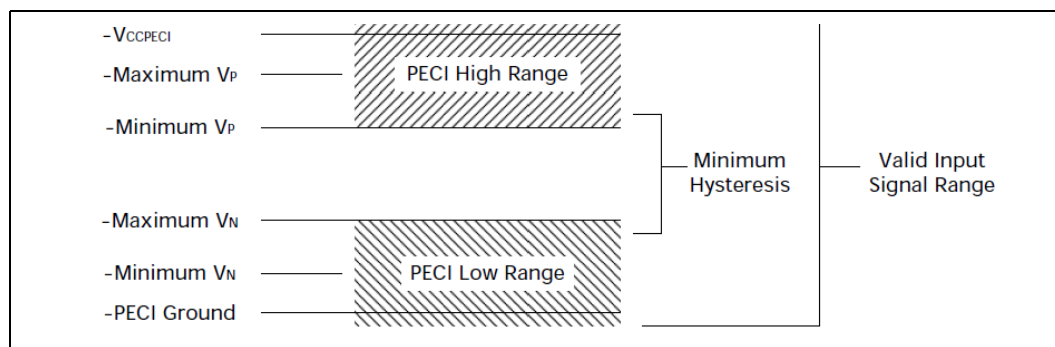
5.2.5 System Reference Clocks (BCLK{0/1}_DP, BCLK{0/1}_DN)

The processor Core, processor Uncore, Intel® QuickPath Interconnect link, PCI Express* and DDR4 memory interface frequencies are generated from BCLK{0/1}_DP and BCLK{0/1}_DN signals. There is no direct link between core frequency and Intel QuickPath Interconnect link frequency (such as, no core frequency to Intel QuickPath Interconnect multiplier). The processor maximum core frequency, Intel QuickPath Interconnect link frequency, and DDR memory frequency are set during manufacturing. It is possible to override the processor core frequency setting using software. This permits operation at lower core frequencies than the factory set maximum core frequency.

The processor core frequency is configured during reset by using values stored within the device during manufacturing. The stored value sets the lowest core multiplier at which the particular processor can operate. If higher speeds are desired, the appropriate ratio can be configured using the IA32_PERF_CTL MSR (MSR 199h); Bits [15:0].

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK{0/1}_DP, BCLK{0/1}_DN input, with exceptions for spread spectrum clocking. DC specifications for the BCLK{0/1}_DP,

BCLK{0/1}_DN inputs are provided in Table 5-20, "Processor Asynchronous Sideband DC Specifications" on page 62. These specifications must be met while also meeting the associated signal quality specifications.

5.2.6 JTAG and Test Access Port (TAP) Signals

Due to the voltage levels supported by other components in the JTAG and Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

5.2.7 Processor Sideband Signals

The processor includes asynchronous sideband signals that provide asynchronous input, output, or I/O signals between the processor and the platform or Platform Controller Hub. Details can be found in Table 5-5, "Signal Groups" on page 47.

All processor Asynchronous Sideband input signals are required to be asserted/de-asserted for a defined number of BCLKs in order for the processor to recognize the proper signal state. These are outlined in Table 5-20, "Processor Asynchronous Sideband DC Specifications" on page 62.

5.2.8 Power, Ground and Sense Signals

Processors also include various other signals including power/ground and sense points. Details can be found in Table 5-5, "Signal Groups" on page 47.

5.2.8.1 Power and Ground Lands

All V_{CCD}, V_{CCIN}, and V_{CCIO_IN}, and V_{CCPECI} lands must be connected to their respective processor power planes, while all V_{SS} lands must be connected to the system ground plane.

For clean on-chip power distribution, processors include lands for all required voltage supplies. These are listed in the following table.

Table 5-1. Power and Ground Lands

Power and Ground Lands	Number of Lands	Comments
V_{CCIN}	173	Each V_{CCIN} land must be supplied with the voltage determined by the SVID Bus signals. Table 5-3 defines the voltage level associated with each core SVID pattern. Table 5-12 and Table 5-4 represent V_{CCIN} static and transient limits.
V_{CCD_01} V_{CCD_23}	56	Each V_{CCD} land is connected to a switchable 1.20 V supply, provide power to the processor DDR4 interface. V_{CCD} is also controlled by the SVID Bus. V_{CCD} is the generic term for V_{CCD_01} and V_{CCD_23}.
V_{CCIO_IN}	1	IO voltage supply input
V_{CCPECI}	1	Power supply for PECI.
V_{SS}	631	Ground

5.2.8.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Large electrolytic bulk capacitors (CBULK) help maintain the output voltage during current transients; for example, coming out of an idle condition. Care must be taken in the baseboard design to ensure that the voltages provided to the processor remain within the specifications listed in Table 5-10, "Voltage Specification" on page 52. Failure to do so can result in timing violations or reduced lifetime of the processor.

5.2.8.3 Voltage Identification (VID)

The reference voltage or the VID setting is set using the SVID communication bus between the processor and the voltage regulator controller chip. The VID settings are the nominal voltages to be delivered to the processor's V_{CCIN} lands. Table 5-3, "VR12.5 Reference Code Voltage Identification (VID) Table" on page 45 specifies the reference voltage level corresponding to the VID value transmitted over serial VID. The VID codes will change due to temperature and/or current load changes in order to minimize the power and to maximize the performance of the part. The specifications are set so that a voltage regulator can operate with all supported frequencies.

Individual processor VID values may be calibrated during manufacturing such that two processor units with the same core frequency may have different default VID settings.

The processor uses voltage identification signals to support automatic selection of V_{CCIN} power supply voltage. If the processor socket is empty (SKTOCC_N high), or a "not supported" response is received from the SVID bus, then the voltage regulation circuit cannot supply the voltage that is requested. The voltage regulator must disable itself or not power on. Vout MAX register (30h) is programmed by the processor to set the maximum supported VID code and if the programmed VID code is higher than the VID supported by the VR, then VR will respond with a "not supported" acknowledgment.

5.2.8.4 SVID Commands

The processor provides the ability to operate while transitioning to a new VID setting and its associated processor voltage rail (V_{CCIN}). This is represented by a DC shift. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target voltage. Transitions above the maximum specified VID are not supported. The processor supports the following VR commands:

- SetVID_Fast (20 mV/µs)
- SetVID_Slow (5 mV/µs)
- Slew Rate Decay (downward voltage only and it is a function of the output capacitance's time constant) commands. Table 5-3, "VR12.5 Reference Code Voltage Identification (VID) Table" on page 45 includes SVID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Section 5-10, "Voltage Specification" .

The VRM or EVRD used must be capable of regulating its output to the value defined by the new VID.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

5.2.8.5   SetVID Fast Command

The SetVID_Fast command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a fast slew rate as defined in the slew rate data register. It is minimum of 20 mV/μs, depending on the amount of decoupling capacitance.

The SetVID_Fast command is preemptive. The VR interrupts its current processes and moves to the new VID. The SetVID_Fast command operates on 1 VR address at a time. This command is used in the processor for package C6 fast exit.

5.2.8.6   SetVID Slow

The SetVID_Slow command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a "slow" slew rate as defined in the slow slew rate data register. The SetVID_Slow is nominally 4x slower than the SetVID_Fast slew rate.

The SetVID_Slow command is preemptive, the VR interrupts its current processes and moves to the new VID. This is the instruction used for normal P-state voltage change. This command is used in the processor for the Intel Enhanced Intel SpeedStep Technology transitions.

5.2.8.7   SetVID Decay

The SetVID_Decay command is the slowest of the DVID transitions. It is normally used for VID down transitions. The VR does not control the slew rate; the output voltage declines with the output load current only.

The SetVID_Decay command is preemptive; the VR interrupts its current processes and moves to the new VID. This command is used in the processor for package C6 entry, allowing capacitor discharge by the leakage; thus, saving energy. This command is normally used in VID down direction in the processor package C6 entry.

5.2.8.8   SVID Power State Functions: SetPS

The processor has three power state functions and these will be set seamlessly using the SVID bus and the SetPS command. Based on the power state command, the SetPS commands send information to the VR controller to configure the VR to improve efficiency, especially at light loads. For example, typical power states are:

- PS0(00h): Represents full power or active mode
- PS1(01h): Represents a light load 5A to 20A
- PS2(02h): Represents a very light load <5A

Note: In PS2 some CPUs can have idle or leakage currents up to 20A. the MBVR must handle high idle currents if they are present even in PS2 condition.

The VR may change its configuration to meet the processor's power needs with greater efficiency. For example, it may reduce the number of active phases, transition from CCM (Continuous Conduction Mode) to DCM (Discontinuous Conduction Mode) mode,

reduce the switching frequency or pulse skip, or change to asynchronous regulation. For example, typical power states are 00h = run in normal mode; a command of 01h = shed phases mode, and an 02h = pulse skip.

The VR may reduce the number of active phases from PS(00h)-to-PS(01h) or PS(00h)-to-PS(02h) for example. There are multiple VR design schemes that can be used to maintain a greater efficiency in these different power states. Work with your VR controller suppliers for optimizations.

If a power state is not supported by the controller, the slave should acknowledge the SetPS command and enter the lowest power state that is supported.

If the VR is in a low power state and receives a SetVID command moving the VID up, then the VR exits the low power state to normal mode (PS0) to move the voltage up as fast as possible. The processor must re-issue the low-power state (PS1 or PS2) command if it is in a low current condition at the new higher voltage. See the following figure for VR power state transitions.

Figure 5-2.   Voltage Regulator (VR) Power State Transitions
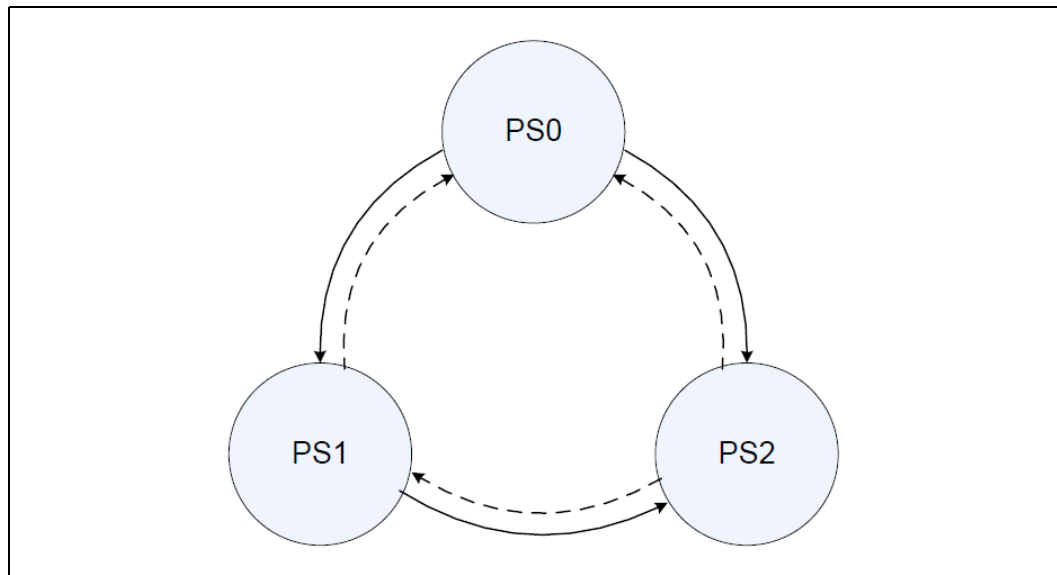
5.2.8.9   SVID Voltage Rail Addressing

The processor addresses three different voltage rail control segments within VR12.5 (V_{CCIN}, V_{CCD_01}, and V_{CCD_23}). The SVID data packet contains a 4-bit addressing code.

Table 5-2.   SVID Address Usage (Sheet 1 of 2)

PWM Address (HEX)	Processor
00	V_{CCIN}
01	NA
02	V_{CCD_01}
03	+1 not used

Table 5-2. SVID Address Usage (Sheet 2 of 2)

PWM Address (HEX)	Processor
04	V_{CCD_23}
05	+1 not used

Notes:
1. Check with VR vendors for determining the physical address assignment method for their controllers.
2. VR addressing is assigned on a per voltage rail basis.
3. Dual VR controllers will have two addresses with the lowest order address, always being the higher phase count.
4. For future platform flexibility, the VR controller should include an address offset, as shown with +1 not used.

Table 5-3. VR12.5 Reference Code Voltage Identification (VID) Table (Sheet 1 of 2)

HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN
00	0.00	55	1.34	78	1.69	9B	2.04	BE	2.39	E1	2.74
33	1.00	56	1.35	79	1.70	9C	2.05	BF	2.40	E2	2.75
34	1.01	57	1.36	7A	1.71	9D	2.06	C0	2.41	E3	2.76
35	1.02	58	1.37	7B	1.72	9E	2.07	C1	2.42	E4	2.77
36	1.03	59	1.38	7C	1.73	9F	2.08	C2	2.43	E5	2.78
37	1.04	5A	1.39	7D	1.74	A0	2.09	C3	2.44	E6	2.79
38	1.05	5B	1.40	7E	1.75	A1	2.10	C4	2.45	E7	2.80
39	1.06	5C	1.41	7F	1.76	A2	2.11	C5	2.46	E8	2.81
3A	1.07	5D	1.42	80	1.77	A3	2.12	C6	2.47	E9	2.82
3B	1.08	5E	1.43	81	1.78	A4	2.13	C7	2.48	EA	2.83
3C	1.09	5F	1.44	82	1.79	A5	2.14	C8	2.49	EB	2.84
3D	1.10	60	1.45	83	1.80	A6	2.15	C9	2.50	EC	2.85
3E	1.11	61	1.46	84	1.81	A7	2.16	CA	2.51	ED	2.86
3F	1.12	62	1.47	85	1.82	A8	2.17	CB	2.52	EE	2.87
40	1.13	63	1.48	86	1.83	A9	2.18	CC	2.53	EF	2.88
41	1.14	64	1.49	87	1.84	AA	2.19	CD	2.54	F0	2.89
42	1.15	65	1.50	88	1.85	AB	2.20	CE	2.55	F1	2.90
43	1.16	66	1.51	89	1.86	AC	2.21	CF	2.56	F2	2.91
44	1.17	67	1.52	8A	1.87	AD	2.22	D0	2.57	F3	2.92
45	1.18	68	1.53	8B	1.88	AE	2.23	D1	2.58	F4	2.93
46	1.19	69	1.54	8C	1.89	AF	2.24	D2	2.59	F5	2.94
47	1.20	6A	1.55	8D	1.90	B0	2.25	D3	2.60	F6	2.95
48	1.21	6B	1.56	8E	1.91	B1	2.26	D4	2.61	F7	2.96
49	1.22	6C	1.57	8F	1.92	B2	2.27	D5	2.62	F8	2.97
4A	1.23	6D	1.58	90	1.93	B3	2.28	D6	2.63	F9	2.98
4B	1.24	6E	1.59	91	1.94	B4	2.29	D7	2.64	FA	2.99
4C	1.25	6F	1.60	92	1.95	B5	2.30	D8	2.65	FB	3.00
4D	1.26	70	1.61	93	1.96	B6	2.31	D9	2.66	FC	3.01
4E	1.27	71	1.62	94	1.97	B7	2.32	DA	2.67	FD	3.02
4F	1.28	72	1.63	95	1.98	B8	2.33	DB	2.68	FE	3.03

Table 5-3. **VR12.5 Reference Code Voltage Identification (VID) Table (Sheet 2 of 2)**

HEX	VCCIN	HEX	VCCIN	HEX	VCCIN		HEX	VCCIN	HEX	VCCIN	HEX	VCCIN
50	1.29	73	1.64	96	1.99		B9	2.34	DC	2.69	FF	3.04
51	1.30	74	1.65	97	2.00		BA	2.35	DD	2.70		
52	1.31	75	1.66	98	2.01		BB	2.36	DE	2.71		
53	1.320	76	1.67	99	2.02		BC	2.37	DF	2.72		
54	1.33	77	1.68	9A	2.03		BD	2.38	E0	2.73		

Notes:
1. 00h = Off State
2. VID Range HEX 01-32 are not used by the processor
3. For VID Ranges supported, see Table 5-10, "Voltage Specification" on page 52
4. V_{CCD} is a fixed voltage of 1.20V

5.2.8.10 Reserved or Unused Signals

All Reserved (RSVD) signals must not be connected. Connection of these signals to V_{CCIN}, V_{CCD}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability.

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5.3 Signal Group Summary

Signals are grouped by buffer type and similar characteristics as listed in the following table. The buffer type indicates which signaling technology and specifications apply to the signals.

Table 5-4.   Signal Description Buffer Types

Signal	Description
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation
Asynchronous[1]	Signal has no timing relationship with any system reference clock.
CMOS	CMOS buffers: 1.05V
DDR4	buffers: 1.2V
DMI2	Direct Media Interface Gen 2 signals. These signals are compatible with PCI Express* 2.0 and 1.0 Signaling Environment AC Specifications.
Intel® QPI	Current-mode 9.6 GT/s, 8.0 GT/s, and 6.4 GT/s, forwarded-clock Intel QuickPath Interconnect signaling
Open Drain CMOS	Open Drain CMOS (ODCMOS) buffers: 1.05V tolerant
PCI Express*	PCI Express* interface signals. These signals are compatible with PCI Express 3.0 Signalling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Refer to the PCIe specification.
Reference	Voltage reference signal.
SSTL	Source Series Terminated Logic (JEDEC SSTL_15)

Note:
1.   Qualifier for a buffer type.

Table 5-5.   Signal Groups (Sheet 1 of 3)

Differential/Single Ended	Buffer Type	Signal
DDR4 Reference Clocks		
Differential	SSTL Output	DDR{0/1/2/3}_CLK_D[N/P][3:0]
DDR4 Command Signals		
Single-ended	SSTL Output	DDR{0/1/2/3}_ACT_N DDR{0/1/2/3}_BA[1:0] DDR{0/1/2/3}_BG[1:0] DDR{0/1/2/3}_MA[17] DDR{0/1/2/3}_MA[16]/_RAS_N DDR{0/1/2/3}_MA[15]/_CAS_N DDR{0/1/2/3}_MA[14]/_WE_N DDR{0/1/2/3}_MA[13:0] DDR{0/1/2/3}_PAR
DDR4 Control Signals		
Single-ended	SSTL Output	DDR{0/1/2/3}_CS_N[9:8] DDR{0/1/2/3}CS_N[7]/CID[4] DDR{0/1/2/3}CS_N[6]/CID[3] DDR{0/1/2/3}_CS_N[5:4] DDR{0/1/2/3}CS_N[3]/CID[1] DDR{0/1/2/3}CS_N[2]/CID[0] DDR{0/1/2/3}_CS_N[1:0] DDR{0/1/2/3}_CID[2] DDR{0/1/2/3}_ODT[5:0] DDR{0/1/2/3}_CKE[5:0]

Table 5-5.   Signal Groups (Sheet 2 of 3)

Differential/Single Ended	Buffer Type	Signal
DDR4 Data Signals		
Differential	SSTL Input/Output	DDR{0/1/2/3}_DQS_D[N/P][17:0]
Single ended	SSTL Input/Output	DDR{0/1/2/3}_DQ[63:0] DDR{0/1/2/3}_ECC[7:0]
DDR4 Miscellaneous Signals		
Single ended	SSTL Input	DDR{0/1/2/3}_ALERT_N
	CMOS Input ***Note:*** Input voltage from platform cannot exceed 1.08V maximum.	DRAM_PWR_OK_C01 DRAM_PWR_OK_C23
	CMOS 1.2V Output	DDR_RESET_C{01/23}_N
	Open Drain CMOS Input/Output	DDR_SCL_C01 DDR_SCL_C23 DDR_SDA_C01 DDR_SDA_C23
	DC Output	DDR01_VREF DDR23_VREF
PCI Express* Port 1, 2, and 3 Signals		
Differential	PCI Express* Input	PE1A_RX_D[N/P][3:0] PE1B_RX_D[N/P][7:4] PE2A_RX_D[N/P][3:0] PE2B_RX_D[N/P][7:4] PE2C_RX_D[N/P][11:8] PE2D_RX_D[N/P][15:12] PE3A_RX_D[N/P][3:0] PE3B_RX_D[N/P][7:4] PE3C_RX_D[N/P][11:8] PE3D_RX_D[N/P][15:12]
Differential	PCI Express* Output	PE1A_TX_D[N/P][3:0] PE1B_TX_D[N/P][7:4] PE2A_TX_D[N/P][3:0] PE2B_TX_D[N/P][7:4] PE2C_TX_D[N/P][11:8] PE2D_TX_D[N/P][15:12] PE3A_TX_D[N/P][3:0] PE3B_TX_D[N/P][7:4] PE3C_TX_D[N/P][11:8] PE3D_TX_D[N/P][15:12]
PCI Express* Miscellaneous Signals		
Single ended	Open Drain CMOS Input/Output	PE_HP_SCL
		PE_HP_SDA
DMI2/PCI Express* Signals		
Differential	DMI2 Input	DMI_RX_D[N/P][3:0]
	DMI2 Output	DMI_TX_D[N/P][3:0]
Intel® QuickPath Interconnect (Intel® QPI) Signals		
Differential	Intel® QPI Input	QPI{0/1}_DRX_D[N/P][19:0] QPI{0/1}_CLKRX_D[N/P]
	Intel® QPI Output	QPI{0/1}_DTX_D[N/P][19:0] QPI{0/1}_CLKTX_D[N/P]
Platform Environmental Control Interface (PECI)		
Single ended	PECI Input/Output	PECI

Table 5-5. **Signal Groups (Sheet 3 of 3)**

Differential/Single Ended	Buffer Type	Signal
System Reference Clock (BCLK{0/1})		
Differential	CMOS 1.05V Input	BCLK{0/1}_D[N/P]
JTAG & TAP Signals		
Single ended	CMOS 1.05V Input	TCK TDI TMS TRST_N
	CMOS 1.05V Input/Output	PREQ_N
	CMOS1.05V Output	PRDY_N
	Open Drain CMOS Input/Output	BPM_N[7:0]
	Open Drain CMOS Output	TDO
Serial VID Interface (SVID) Signals		
Single ended	CMOS 1.05V Input	SVIDALERT_N
	Open Drain CMOS Input/Output	SVIDDATA
	Open Drain CMOS Output	SVIDCLK
Processor Asynchronous Sideband Signals		
Single ended	CMOS 1.05V Input	BIST_ENABLE BMCINIT DEBUG_EN_N FRMAGENT PWRGOOD PMSYNC RESET_N SAFE_MODE_BOOT SOCKET_ID[1:0] TXT_AGENT TXT_PLTEN
	CMOS 1.05V Output	FIVR_FAULT
	Open Drain CMOS Input/Output	CATERR_N MEM_HOT_C01_N MEM_HOT_C23_N MSMI_N PM_FAST_WAKE_N PROCHOT_N
	Open Drain CMOS Output	ERROR_N[2:0] THERMTRIP_N
Miscellaneous Signals		
	CMOS 1.05V Input	EAR_N
	Output	SKTOCC_N
Power/Other Signals		
	Power / Ground	V_{CCIN}, V_{CCD_01}, V_{CCD_23}, V_{CCIO_IN}, V_{CCPECI}, V_{SS}
	Sense Points	VCCIN_SENSE VSS_VCCIN_SENSE

Notes:
1. Refer to Chapter 4, "Signal Descriptions" for signal description details.
2. DDR{0/1/2/3} refers to DDR4 Channel 0, DDR4 Channel 1, DDR4 Channel 2, and DDR4 Channel 3.

Table 5-6.   Signals with On-Die Weak Pull-Up/Pull-Down Resistors

Signal Name	Pull Up/Pull Down	Rail	Value	Units	Notes
BIST_ENABLE	Pull Up	VCCIO_IN	5K–15K	Ω	
BMCINIT	Pull Down	VSS	5K–15K	Ω	
DEBUG_EN_N	Pull Up	VCCIO_IN	5K–15K	Ω	
EAR_N	Pull Up	VCCIO_IN	5K–15K	Ω	
FRMAGENT	Pull Down	VSS	5K–15K	Ω	
PM_FAST_WAKE_N	Pull Up	VCCIO_IN	5K–15K	Ω	
PREQ_N	Pull Up	VCCIO_IN	5K–15K	Ω	
SAFE_MODE_BOOT	Pull Down	VSS	5K–15K	Ω	
SOCKET_ID[1:0]	Pull Down	VSS	5K–15K	Ω	
TCK	Pull Down	VSS	5K–15K	Ω	
TDI	Pull Up	VCCIO_IN	5K–15K	Ω	
TMS	Pull Up	VCCIO_IN	5K–15K	Ω	
TRST_N	Pull Up	VCCIO_IN	5K–15K	Ω	
TXT_AGENT	Pull Down	VSS	5K–15K	Ω	
TXT_PLTEN	Pull Up	VCCIO_IN	5K–15K	Ω	

5.4   Power-On Configuration (POC) Options

Several configuration options can be configured by hardware. The processor samples its hardware configuration at reset, on the active-to-inactive transition of RESET_N, or upon assertion of PWRGOOD (inactive-to-active transition). For specifics on these options, refer to the following table.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed, except by another reset transition of the latching signal (RESET_N or PWRGOOD).

Table 5-7.   Power-On Configuration Option Lands

Configuration Option	Land Name	Notes
Output tri state	PROCHOT_N	
Execute BIST (Built-In Self Test)	BIST_ENABLE	1
Enable Service Processor Boot Mode	BMCINIT	2
Power-up Sequence Halt	EAR_N	2
Enable Intel® Trusted Execution Technology (Intel® TXT) Platform	TXT_PLTEN	2
Enable Bootable Firmware Agent	FRMAGENT	2
Enable Intel Trusted Execution Technology (Intel TXT) Agent	TXT_AGENT	2
Enable Safe Mode Boot	SAFE_MODE_BOOT	2
Configure Socket ID	SOCKET_ID[1:0]	2
Enables debug from cold boot	DEBUG_EN_N	2

Note:
1. BIST_ENABLE is sampled at RESET_N de-assertion
2. This signal is sampled after PWRGOOD assertion.

5.5 Absolute Maximum and Minimum Ratings

The following table specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded, depending on exposure to conditions exceeding the functional operation condition limits.

Although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Table 5-8.   Processor Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CCIN}	Processor input voltage with respect to V_{SS}	-0.3	1.98	V
V_{CCD}	Processor IO supply voltage for DDR4 (standard voltage) with respect to V_{SS}	-0.3	1.35	V
V_{CCIO_IN}	IO voltage supply input with respect to V_{SS}	-0.3	1.35	V
V_{CCPECI}	Power supply for PECI with respect to V_{SS}	-0.3	1.35	V

Note:
1. For functional operation, all processor electrical, signal quality, mechanical, and thermal specifications must be satisfied.
2. Excessive Overshoot or undershoot on any signal will likely result in permanent damage to the processor.

5.5.1 Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity limits to which the device is exposed to while being stored in a Moisture Barrier Bag. The specified storage conditions are for component level prior to board attach (see notes in the following table for post board attach limits).

The following table specifies absolute maximum and minimum storage temperature limits that represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. These limits specify the maximum or minimum device storage conditions for a sustained period of time. At conditions outside sustained limits, but within absolute maximum and minimum ratings, quality and reliability may be affected.

Table 5-9.   Storage Condition Ratings (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Unit
$T_{absolute\ storage}$	The minimum/maximum device storage temperature beyond which damage (latent or otherwise) may occur when subjected to for any length of time.	-25	125	°C
$T_{sustained\ storage}$	The minimum/maximum device storage temperature for a sustained period of time.	-5	40	°C
$T_{short\ term\ storage}$	The ambient storage temperature (in shipping media) for a short period of time.	-20	85	°C
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24		°C

Table 5-9.   Storage Condition Ratings (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Unit
Time$_{sustained}$ storage	A prolonged or extended period of time; typically associated with sustained storage conditions. Unopened bag, includes 6 months storage time by customer.	0	30	months
Time$_{short\ term}$ storage	A short period of time (in shipping media).	0	72	hours

Notes:
1. Storage conditions are applicable to storage environments only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
2. These ratings apply to the Intel component and do not include the tray or packaging.
3. Failure to adhere to this specification can affect the long-term reliability of the processor.
4. Non-operating storage limits post board attach: Storage condition limits for the component once attached to the application board are not specified. Intel does not conduct component level certification assessments post board attach given the multitude of attach methods, socket types and board types used by customers. Provided as general guidance only, Intel board products are specified and certified to meet the following temperature and humidity limits (Non-Operating Temperature Limit: -40 °C to 70 °C and Humidity: 50% to 90%, non condensing with a maximum wet bulb of 28 °C).
5. Device storage temperature qualification methods follow JEDEC High and Low Temperature Storage Life Standards: *JESD22-A119* (low temperature) and *JESD22-A103* (high temperature).

5.6   DC Specifications

DC specifications are defined at the processor pads, unless otherwise noted.
DC specifications are only valid while meeting specifications for case temperature (T$_{CASE}$ specified in the Processor Thermal/Mechanical Specification and Design Guide) (See Related Documents Section), clock frequency, and input voltages. Care should be taken to read all notes associated with each specification.

Table 5-10. Voltage Specification (Sheet 1 of 2)

Symbols	Parameter	Voltage Plane	Min	Nom	Max	Unit	Notes[1]
V$_{CCIN}$	Input to Integrated Voltage Regulator	V$_{CCIN}$	1.47	1.82	1.85	V	2, 3, 4, 5, 9, 12
V$_{VID\_STEP}$ (V$_{CCIN}$, V$_{CCD}$)	VID step size during a transition	–	–	10.0	–	mV	6
V$_{CCD}$ (V$_{CCD\_01}$, V$_{CCD\_23}$)	I/O Voltage for DDR4 (Standard Voltage)	V$_{CCD}$	0.97*V$_{CCD\_NOM}$	1.2	1.044*V$_{CCD\_NOM}$	V	7, 8, 9, 10, 11

Table 5-10. Voltage Specification (Sheet 2 of 2)

Symbols	Parameter	Voltage Plane	Min	Nom	Max	Unit	Notes[1]
VCCIO_IN	Power rail for all misc I/O	VCCIO_IN	$0.95 * V_{CCIO\_IN\_NOM}$	0.95	$1.05 * V_{CCIO\_IN\_NOM}$	V	
VCCPECI	Power rail for PECI pin	VCCPECI	$0.95 * V_{CCPECI\_NOM}$	0.95	$1.05 * V_{CCIO\_IN\_NOM}$	V	

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processors.
2. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required.
3. The V_{CCIN} voltage specification requirements are measured across the remote sense pin pairs (V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$) on the processor package. Voltage measurement should be taken with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20MHz for older model oscilloscopes), using a 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
4. Refer to Table 5-12, "V_{CCIN} Static and Transient Tolerance Processor" on page 54 and corresponding Table 5-4, "V_{CCIN} Static and Transient Tolerance Loadlines" on page 55. The processor should not be subjected to any static V_{CCIN} level that exceeds the V_{CCIN_MAX} associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
5. Minimum V_{CCIN} and maximum I_{CCIN} are specified at the maximum processor case temperature (T_{CASE}) shown in the Processor Thermal/Mechanical Specification and Design Guide (See Related Document Section). I_{CCIN_MAX} is specified at the relative V_{CC_MAX} point on the V_{CCIN} load line. The processor is capable of drawing I_{CCIN_MAX} for up to 4 ms.
6. This specification represents the V_{CCIN} reduction or V_{CCIN} increase due to each VID transition. For Voltage Identification (VID), see Table 5-3, "VR12.5 Reference Code Voltage Identification (VID) Table" on page 45.
7. Baseboard bandwidth is limited to 20 MHz.
8. DC + AC + Ripple = Total Tolerance
9. For SVID Power State Functions (SetPS) see Section 5.2.8.8, "SVID Power State Functions: SetPS" .
10. V_{CCD} tolerance at processor pins. Required in order to meet ±5% tolerance at processor die.
11. The V_{CCD01}, V_{CCD23} voltage specification requirements are measured across vias on the platform. Choose V_{CCD01} or V_{CCD23} vias close to the socket and measure with a DC to 100MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using 1.5 pF maximum probe capacitance, and 1M ohm minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
12. V_{CCIN} has a V_{boot} setting of 0.0V and is not included in the PWRGOOD indication.

Figure 5-3. Serial VID Interface (SVID) Signals Clock Timings
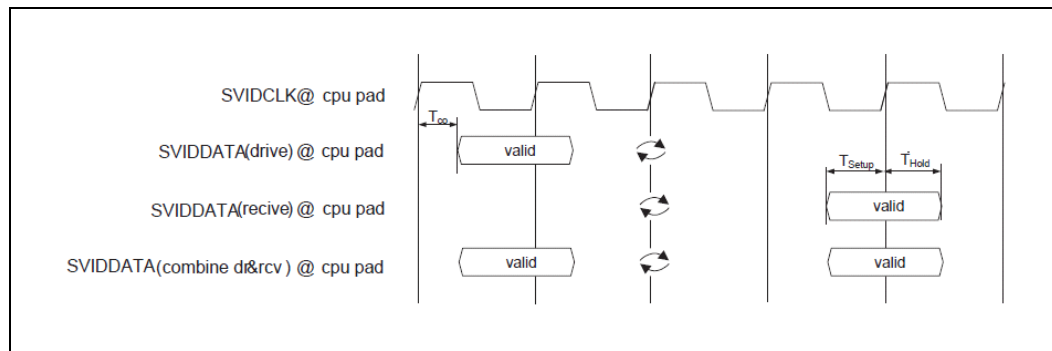
Table 5-11. Current (I_{CCIN_MAX} and I_{CCIN_TDC}) Specification

Segment	TDP	I_{CCIN_MAX} @ V_{CCIN}(A)	I_{CC_MAX} @ V_{CCIO_IN} (A)	I_{CC_MAX} @ V_{CCPECI} (A)	I_{CCD01_MAX} (A)	I_{CCD23_MAX} (A)	$I_{CCIN\_TDC}^3$ @ V_{CCIN}(A)	$I_{CC\_TDC}^3$ @ V_{CCIO_IN}(A)	$I_{CC\_TDC}^3$ @ V_{CCPECI}(A)	I_{CCD01_TDC} (A)	$I_{CCD23\_TDC}^3$ (A)	P_{max}^5 @ V_{CCIN}(W)	$P_{max\_Package}^5$ (W)	Notes[1]
High End Desktop (HEDT)	140W 8-Core	175	0.1	0.001	1.4	1.4	82	0.02	0.001	0.8	0.8	267	270	2, 4
	140W 6-Core	175	0.1	0.001	1.4	1.4	82	0.02	0.001	0.8	0.8	267	270	2, 4

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processors.
2. FMB is the flexible motherboard guidelines.
3. I_{CCIN_TDC} (Thermal Design Current) is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator thermal assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion.
4. Minimum V_{CCIN} and maximum I_{CCIN} are specified at the maximum processor case temperature (T_{CASE}). I_{CCIN_MAX} is specified at the relative V_{CCIN_MAX} point on the V_{CCIN} load line. The processor is capable of drawing I_{CCIN_MAX} for up to 4 ms.

Table 5-12. V_{CCIN} Static and Transient Tolerance Processor (Sheet 1 of 2)

I_{CCIN} (A)	V_{CCIN_Max} (V)	V_{CCIN_Nom} (V)	V_{CCIN_Min} (V)	Notes
0	VID + 0.022	VID - 0.000	VID - 0.022	
10	VID + 0.012	VID - 0.011	VID - 0.033	
20	VID + 0.001	VID - 0.021	VID - 0.043	
30	VID - 0.010	VID - 0.032	VID - 0.054	
40	VID - 0.020	VID - 0.042	VID - 0.064	
50	VID - 0.031	VID - 0.053	VID - 0.075	
60	VID - 0.041	VID - 0.063	VID - 0.085	
70	VID - 0.052	VID - 0.074	VID - 0.096	
80	VID - 0.062	VID - 0.084	VID - 0.106	
90	VID - 0.073	VID - 0.095	VID - 0.117	
100	VID - 0.083	VID - 0.105	VID - 0.127	
110	VID - 0.094	VID - 0.116	VID - 0.138	
120	VID - 0.104	VID - 0.126	VID - 0.148	
130	VID - 0.115	VID - 0.137	VID - 0.159	
140	VID - 0.125	VID - 0.147	VID - 0.169	
150	VID - 0.136	VID - 0.158	VID - 0.180	
160	VID - 0.146	VID - 0.168	VID - 0.190	
170	VID - 0.157	VID - 0.179	VID - 0.201	
180	VID - 0.167	VID - 0.189	VID - 0.211	
190	VID - 0.178	VID - 0.200	VID - 0.222	
200	VID - 0.188	VID - 0.210	VID - 0.232	

Table 5-12. V$_{CCIN}$ Static and Transient Tolerance Processor (Sheet 2 of 2)

I$_{CCIN}$ (A)	V$_{CCIN\_Max}$ (V)	V$_{CCIN\_Nom}$ (V)	V$_{CCIN\_Min}$ (V)	Notes
210	VID - 0.199	VID - 0.221	VID - 0.243	
220	VID - 0.209	VID - 0.231	VID - 0.253	

Notes:
1. The V$_{CCIN\_MIN}$ and V$_{CCIN\_MAX}$ loadlines represent static and transient limits. See Section 5.6.1, "Die Voltage Validation" for V$_{CCIN}$ Overshoot specifications.
2. This table is intended to aid in reading discrete points on graph in Figure 5-4.
3. The loadlines specify voltage limits at the die measured at the VCCIN_SENSE and VSS_VCCIN_SENSE lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCCIN_SENSE and VSS_VCCIN_SENSE lands.
4. The Adaptive Loadline Positioning slope is 1.05 mΩ (mohm) with ±22mV TOB (Tolerance of Band).
5. Processor core current (I$_{CCIN}$) ranges are valid up to I$_{CCIN\_MAX}$ of the processor SKU as defined in the previous table.

Figure 5-4. V$_{CCIN}$ Static and Transient Tolerance Loadlines
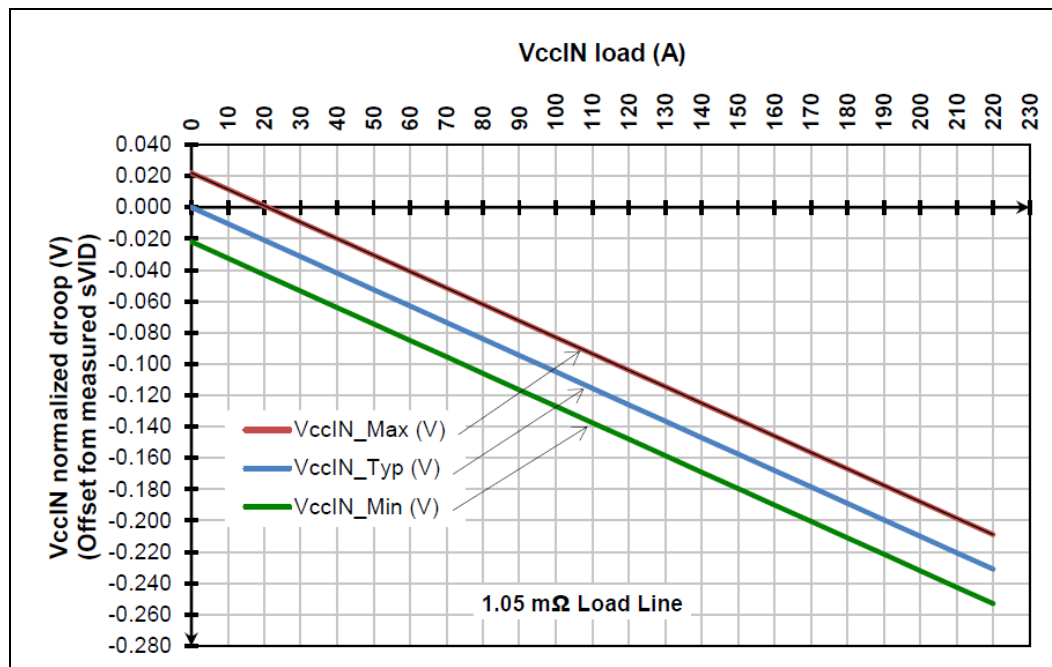
5.6.1 Die Voltage Validation

Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

5.6.1.1 V$_{CCIN}$ Overshoot Specifications

The processor can tolerate short transient overshoot events where V$_{CCIN}$ exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID + V$_{OS\_MAX}$ (V$_{OS\_MAX}$ is the maximum allowable overshoot above VID). These specifications apply to the processor die voltage as measured across the VCCIN_SENSE and VSS_VCCIN_SENSE lands.

Table 5-13. **V_{CCIN} Overshoot Specifications**

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CCIN} overshoot above VID	–	50	mV	5-5	
T_{OS_MAX}	Time duration of V_{CCIN} overshoot above V_{CCIN_Max} value at the new lighter load	–	25	µs	5-5	

Figure 5-5. **V_{CCIN} Overshoot Example Waveform**
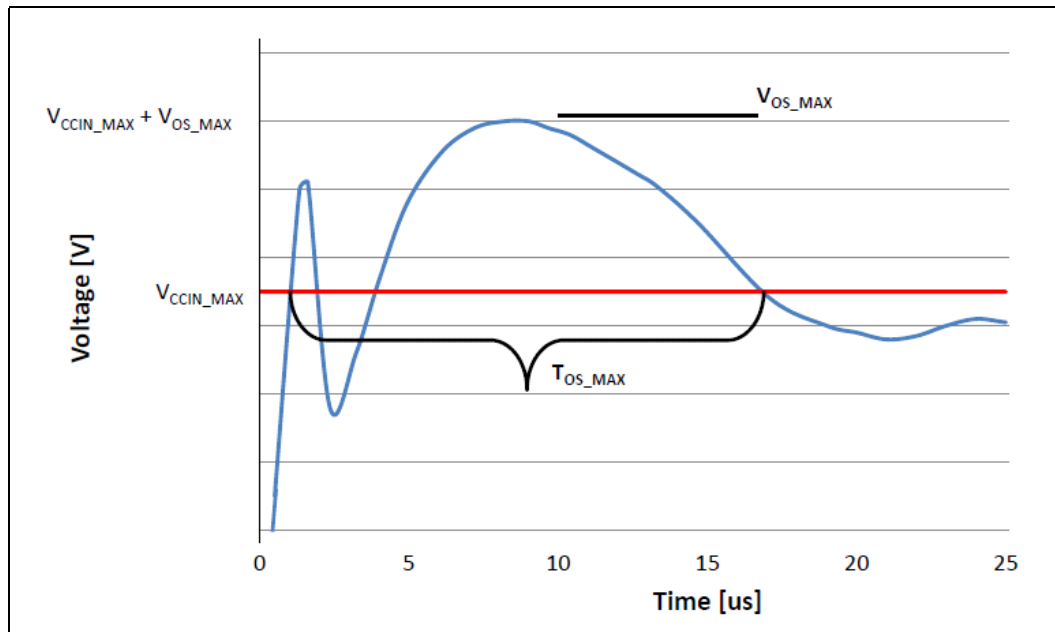
Notes:
1. V_{OS_MAX} is the measured overshoot voltage above V_{CCIN_MAX}.
2. T_{OS_MAX} is the measured time duration above V_{CCIN_MAX}.
3. V_{CCIN_MAX} = VID + TOB

5.6.2 Signal DC Specifications

For additional specifications, refer to the Related Documents Section.

5.6.2.1 DDR4 Signal DC Specifications

Table 5-14. **DDR4 Signal DC Specifications (Sheet 1 of 2)**

Symbol	Parameter	Min	Nom	Max	Units	Notes[1]
I_{IL}	Input Leakage Current	-1.4	–	+1.4	mA	9
Data Signals						
R_{ON}	DDR4 Data Buffer On Resistance	27	–	33	ohm	6
Data ODT	On-Die Termination for Data Signals	45	–	55	ohm	8
Reference Clock and Command Signals						
V_{OL}	Output Low Voltage	–	$(V_{CCD} / 2)* (R_{ON} / (R_{ON} + R_{VTT\_TERM}))$	–	V	2, 7

Table 5-14. DDR4 Signal DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Nom	Max	Units	Notes[1]
V_{OH}	Output High Voltage	–	$V_{CCD} - ((V_{CCD}/2) * (R_{ON}/(R_{ON} + R_{VTT\_TERM})))$	–	V	2, 5, 7
Data Signals						
V_{OL}	Output Low Voltage	–	Varies	–		10
V_{OH}	Output High Voltage	–	V_{CCD}	–		
Reference Clock Signal						
R_{ON}	DDR4 Clock Buffer On Resistance	27	–	33	ohm	6
Command Signals						
R_{ON}	DDR4 Command Buffer On Resistance	16	–	20	ohm	6
R_{ON}	DDR4 Reset Buffer On Resistance	–	78	–	ohm	6
$V_{OL\_CMOS1.2V}$	Output Low Voltage, Signals DDR_RESET_ C{01/23}_N	–	–	$0.2*V_{CCD}$	V	1, 2
$V_{OH\_CMOS1.2V}$	Output High Voltage, Signals DDR_RESET_ C{01/23}_N	$0.9*V_{CCD}$	–	–	V	1, 2
Control Signals						
R_{ON}	DDR4 Control Buffer On Resistance	27	–	33	ohm	6
DDR4 Miscellaneous Signals						
ALERT_N	On-Die Termination for Parity Error Signals	81	90	99	ohm	
V_{IL}	Input Low Voltage DRAM_PWR_OK_C{01/23}	–	–	304	mV	2, 3
V_{IH}	Input High Voltage DRAM_PWR_OK_C{01/23}	800	–		mV	2, 4, 5

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The voltage rail V_{CCD} which will be set to 1.2V nominal depending on the voltage of all DIMMs connected to the processor.
3. V_{IL} is the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
4. V_{IH} is the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{CCD}. However, input signal drivers must comply with the signal quality specifications.
6. This is the pull down driver resistance. Reset drive does not have a termination.
7. R_{VTT_TERM} is the termination on the DIMM and not controlled by the processor. Refer to the applicable DIMM datasheet.
8. The minimum and maximum values for these signals are programmable by BIOS to one of the pairs.
9. Input leakage current is specified for all DDR4 signals.
10. Vol = Ron * [VCCD/(Ron + Rtt_Eff)], where Rtt_Eff is the effective pull-up resistance of all DIMMs in the system, including ODTs and series resistors on the DIMMs.

5.6.2.2   PECI DC Specifications

Table 5-15. PECI DC Specifications

Symbol	Definition and Conditions	Min	Max	Units	Figure	Notes[1]
V_{In}	Input Voltage Range	-0.150	V_{CCPECI} + 0.150	V		
$V_{Hysteresis}$	Hysteresis	$0.100 * V_{CCPECI}$	–	V		
V_N	Negative-edge threshold voltage	$0.275 * V_{CCPECI}$	$0.500 * V_{CCPECI}$	V	5-1	2
V_P	Positive-edge threshold voltage	$0.550 * V_{CCPECI}$	$0.725 * V_{CCPECI}$	V	5-1	2
I_{Source}	Pullup Resistance (V_{OH} = $0.75 * V_{CCPECI}$)	-6.00	–	mA		
I_{Leak+}	High impedance state leakage to V_{CCIO_IN} (V_{leak} = V_{OL})	50	200	μA		
R_{ON}	High impedance leakage to GND (V_{leak} = V_{OH})	20	36	Ω		
C_{Bus}	Bus capacitance per node	N/A	10	pF		4, 5
V_{Noise}	Signal noise immunity above 300 MHz	$0.100 * V_{CCPECI}$	N/A	V_{p-p}		
	Output Edge Rate (50 ohm to V_{SS}, between V_{IL} and V_{IH})	1.5	4	V/ns		

Notes:
1. V_{CCPECI} supplies the PECI interface. PECI behavior does not affect V_{CCPECI} min/max specification.
2. It is expected that the PECI driver will take into account, the variance in the receiver input thresholds and consequently, be able to drive its output within safe limits (-0.150 V to $0.275*V_{CCPECI}$ for the low level and $0.725*V_{CCPEC}$ to V_{CCPECI}+0.150 V for the high level).
3. The leakage specification applies to powered devices on the PECI bus.
4. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.
5. Excessive capacitive loading on the PECI line may slow down the signal rise/fall times and consequently limit the maximum bit rate at which the interface can operate.

5.6.2.3   System Reference Clock (BCLK{0/1}) DC Specifications

Table 5-16. System Reference Clock (BCLK{0/1}) DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Signal	Min	Max	Unit	Figure	Notes[1]
$V_{BCLK\_diff\_ih}$	Differential Input High Voltage	Differential	0.150	N/A	V	5-6	9
$V_{BCLK\_diff\_il}$	Differential Input Low Voltage	Differential	–	-0.150	V	5-6	9
V_{cross} (abs)	Absolute Crossing Point	Single Ended	0.250	0.550	V	5-7, 5-8	2, 4, 7, 9
V_{cross} (rel)	Relative Crossing Point	Single Ended	0.250 + 0.5* (VH_{avg} − 0.700)	0.550 + 0.5* (VH_{avg} − 0.700)	V	5-7	3, 4, 5, 9
ΔV_{cross}	Range of Crossing Points	Single Ended	N/A	0.140	V	5-9	6, 9
V_{TH}	Threshold Voltage	Single Ended	Vcross − 0.1	Vcross + 0.1	V		9

Table 5-16. System Reference Clock (BCLK{0/1}) DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Signal	Min	Max	Unit	Figure	Notes[1]
I_{IL}	Input Leakage Current	N/A	–	1.50	mA		8, 9
C_{pad}	Pad Capacitance	N/A	1.12	1.7	pF		9

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as the instantaneous voltage value when the rising edge of BCLK{0/1}_DN is equal to the falling edge of BCLK{0/1}_DP.
3. V_{Havg} is the statistical average of the VH measured by the oscilloscope.
4. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
5. V_{Havg} can be measured directly using "Vtop" on Agilent* and "High" on Tektronix oscilloscopes.
6. V_{CROSS} is defined as the total variation of all crossing voltages as defined in Note 3.
7. The rising edge of BCLK{0/1}_DN is equal to the falling edge of BCLK{0/1}_DP.
8. For Vin between 0 and Vih.
9. Specifications can be validated at the pin.

Figure 5-6. BCLK{0/1} Differential Clock Measurement Point for Ringback
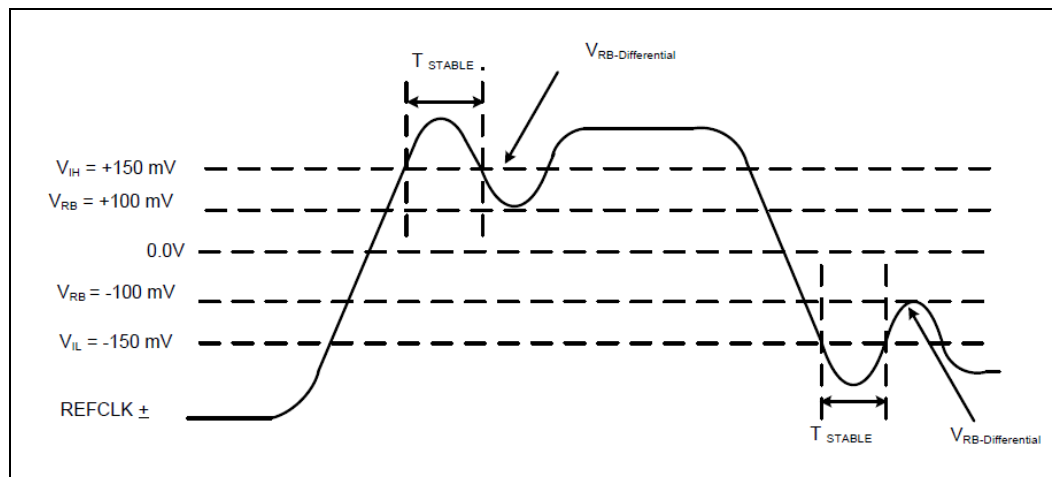
Figure 5-7. BCLK{0/1} Differential Clock Cross Point Specification
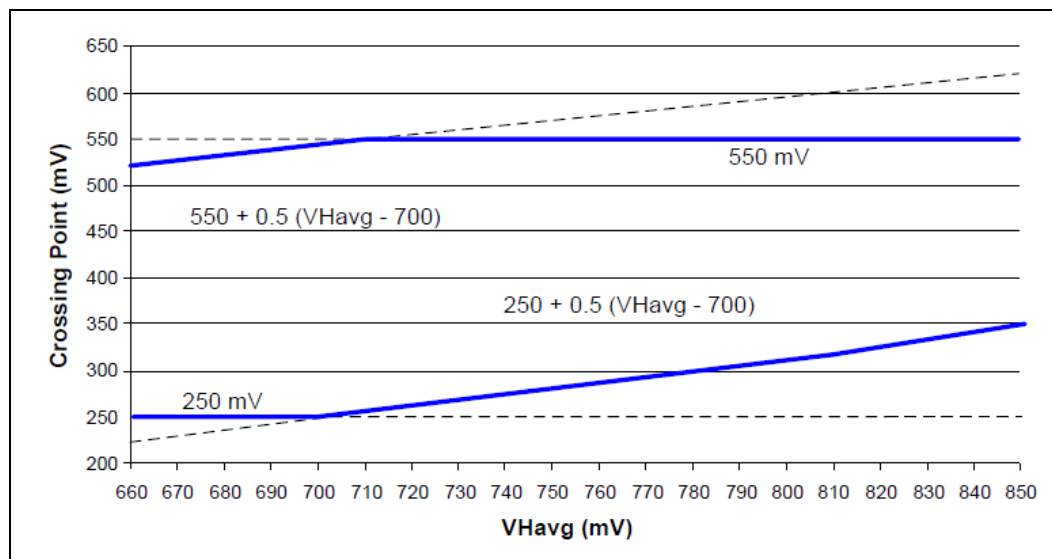
Figure 5-8. BCLK{0/1} Single-Ended Clock Measurement Points for Absolute Cross Point and Swing
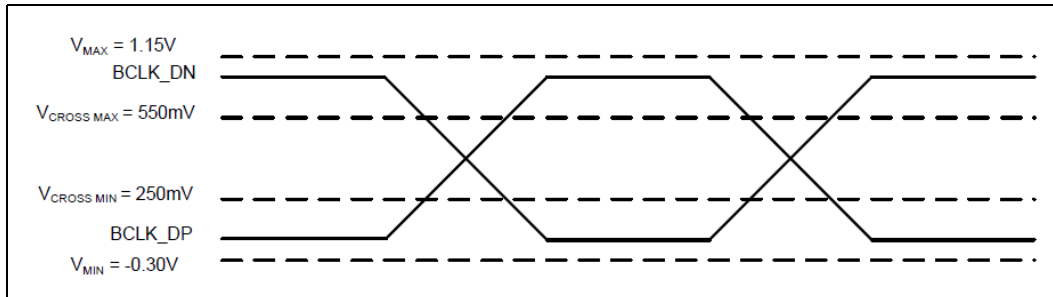
Figure 5-9. BCLK{0/1} Single-Ended Clock Measure Points for Delta Cross Point
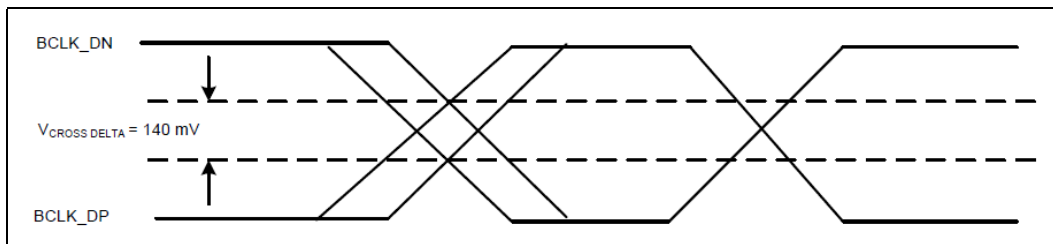
5.6.2.4 SMBus DC Specifications

Table 5-17. SMBus DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	–	$0.3{*}V_{CCIO\_IN}$	V	
V_{IH}	Input High Voltage	$0.7{*}V_{CCIO\_IN}$	–	V	
$V_{Hysteresis}$	Hysteresis	$0.1{*}V_{CCIO\_IN}$	–	V	
V_{OL}	Output Low Voltage	–	$0.2{*}V_{CCIO\_IN}$	V	
R_{ON}	Buffer On Resistance	4	14	Ω	
I_L	Leakage Current Signals	50	200	µA	
	Output Edge Rate (50 ohm to V_{CCIO_IN}, between V_{IL} and V_{IH})	0.05	0.6	V/ns	1

Note:
1. Value obtained through test bench with 50Ω pull-up to V_{CCIO_IN}.

5.6.2.5   JTAG and TAP Signals DC Specifications

Table 5-18. JTAG and TAP Signals DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	–	$0.4*V_{CCIO\_IN}$	V	
V_{IH}	Input High Voltage	$0.8*V_{CCIO\_IN}$	–	V	
V_{IL}	Input Low Voltage: TCK	–	$0.4*V_{CCIO\_IN}$	V	
V_{IH}	Input High Voltage: TCK	$0.6*V_{CCIO\_IN}$	–	V	
V_{OL}	Output Low Voltage	–	$0.2*V_{CCIO\_IN}$	V	
$V_{Hysteresis}$	Hysteresis	$0.1*V_{CCIO\_IN}$	–		
R_{ON}	Buffer On Resistance Signals BPM_N[7:0], TDO	4	14	Ω	
I_{IL}	Input Leakage Current Signals	50	200	µA	
	Output Edge Rate (50 ohm to V_{CCIO_IN}) Signal: BPM_N[7:0], PRDY_N, TDO	0.2	1.5	V/ns	1

Notes:
1.   These are measured between V_{IL} and V_{IH}.
2.   The signal edge rate must be met or the signal must transition monotonically to the asserted state.

5.6.2.6   Serial VID Interface (SVID) DC Specifications

Table 5-19. Serial VID Interface (SVID) DC Specifications

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{CCIO_IN}	CPU I/O Voltage	$V_{CCIO\_IN} - 5\%$	0.95	$V_{CCIO\_IN} + 5\%$	V	1
V_{IL}	Input Low Voltage Signals SVIDDATA, SVIDALERT_N	–	–	$0.4*V_{CCIO\_IN}$	V	1
V_{IH}	Input High Voltage Signals SVIDDATA, SVIDALERT_N	$0.7*V_{CCIO\_IN}$	–	–	V	1
V_{OL}	Output Low Voltage Signals: SVIDCLK, SVIDDATA	–	–	$0.2*V_{CCIO\_IN}$	V	1, 5
$V_{Hysteresis}$	Hysteresis	$0.05*V_{CCIO\_IN}$	–	–	V	1
R_{ON}	Buffer On Resistance Signals SVIDCLK, SVIDDATA	4	–	14	Ω	2
I_{IL}	Input Leakage Current	50	–	200	µA	3
	Input Edge Rate Signal: SVIDALERT_N	0.05	–	–	V/ns	4
	Output Edge Rate	0.20	–	1.5	V/ns	4, 5

Notes:
1. V_{CCIO_IN} refers to instantaneous V_{CCIO_IN}.
2.   Measured at $0.31*V_{CCIO\_IN}$.
3.   Vin between 0V and V_{CCIO_IN} (applies to SVIDDATA and SVIDALERT_N only).
4.   These are measured between V_{IL} and V_{IH}.
5.   Value obtained through test bench with 50Ω pull up to V_{CCIO_IN}.

5.6.2.7 Processor Asynchronous Sideband DC Specifications

Table 5-20. Processor Asynchronous Sideband DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
CMOS1.05v Signals					
$V_{IL\_CMOS1.05V}$	Input Low Voltage	–	$0.4*V_{CCIO\_IN}$	V	1, 2
$V_{IH\_CMOS1.05V}$	Input High Voltage	$0.6*V_{CCIO\_IN}$	–	V	1, 2
$I_{IL\_CMOS1.05V}$	Input Leakage Current	50	200	µA	1,2
Open Drain CMOS (ODCMOS) Signals					
V_{IL_ODCMOS}	Input Low Voltage Signals: CATERR_N, MSMI_N, PM_FAST_WAKE_N	–	$0.4*V_{CCIO\_IN}$	V	1, 2
V_{IL_ODCMOS}	Input Low Voltage Signals: MEM_HOT_C01/23_N, PROCHOT_N	–	$0.3*V_{CCIO\_IN}$	V	1, 2
V_{IH_ODCMOS}	Input High Voltage	$0.7*V_{CCIO\_IN}$	–	V	1, 2
V_{OL_ODCMOS}	Output Low Voltage	–	$0.2*V_{CCIO\_IN}$	V	1, 2
$V_{Hysteresis}$	Hysteresis Signals: MEM_HOT_C01/23_N, PROCHOT_N	$0.1*V_{CCIO\_IN}$	–		
$V_{Hysteresis}$	Hysteresis Signal: CATERR_N, MSMI_N, PM_FAST_WAKE_N	$0.05*V_{CCIO\_IN}$	–		
I_L	Input Leakage Current	50	200	µA	
R_{ON}	Buffer On Resistance	4	14	Ω	1, 2
	Output Edge Rate Signal: MEM_HOT_C{01/23}_ N, ERROR_N[2:0], THERMTRIP, PROCHOT_N	0.05	0.60	V/ns	3
	Output Edge Rate Signal: CATERR_N, MSMI_N, PM_FAST_WAKE_N	0.2	1.5	V/ns	3

Notes:
1. This table applies to the processor sideband and miscellaneous signals specified in Table 5-5, "Signal Groups" on page 47.
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. These are measured between V_{IL} and V_{IH}.

5.6.2.8 Miscellaneous Signals DC Specifications

Table 5-21. Miscellaneous Signals DC Specifications

Symbol	Parameter	Min	Nominal	Max	Units	Notes
SKTOCC_N Signal						
$V_{O\_ABS\_MAX}$	Output Absolute Max Voltage	–	3.30	3.50	V	
I_{OMAX}	Output Max Current	–	–	1	mA	

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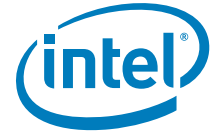
6 Processor Land Listing

Table 6-1 provides the processor land listing organized alphabetically by signal name.

Table 6-1.   Processor Land List

Land Name	Land Number
BCLK0_DN	CN41
BCLK0_DP	CL41
BCLK1_DN	AW45
BCLK1_DP	BA45
BIST_ENABLE	AJ43
BMCINIT	AM48
BPM_N[0]	BC43
BPM_N[1]	BB44
BPM_N[2]	BE47
BPM_N[3]	BF46
BPM_N[4]	BE45
BPM_N[5]	BD46
BPM_N[6]	BA43
BPM_N[7]	AW43
CATERR_N	CC51
DDR_RESET_C01_N	DC15
DDR_RESET_C23_N	C23
DDR_SCL_C01	CK42
DDR_SCL_C23	V40
DDR_SDA_C01	CM42
DDR_SDA_C23	Y40
DDR0_ACT_N	CK16
DDR0_ALERT_N	CD16
DDR0_BA[0]	CL21
DDR0_BA[1]	CH20
DDR0_BG[0]	CL17
DDR0_BG[1]	CN17
DDR0_CID[2]	CJ25
DDR0_CKE[0]	CJ17
DDR0_CKE[1]	CE17
DDR0_CKE[2]	CF16
DDR0_CKE[3]	CC17
DDR0_CKE[4]	CN15
DDR0_CKE[5]	CC15
DDR0_CLK_DN[0]	CE21
DDR0_CLK_DN[1]	CF18
DDR0_CLK_DN[2]	CF20
DDR0_CLK_DN[3]	CE19
DDR0_CLK_DP[0]	CC21

Table 6-1.   Processor Land List

Land Name	Land Number
DDR0_CLK_DP[1]	CD18
DDR0_CLK_DP[2]	CD20
DDR0_CLK_DP[3]	CC19
DDR0_CS_N[0]	CD22
DDR0_CS_N[1]	CH22
DDR0_CS_N[2]/ CID[0]	CF26
DDR0_CS_N[3]/ CID[1]	CC25
DDR0_CS_N[4]	CK22
DDR0_CS_N[5]	CH24
DDR0_CS_N[6]/ CID[3]	CH26
DDR0_CS_N[7]/ CID[4]	CD26
DDR0_CS_N[8]	CK24
DDR0_CS_N[9]	CK26
DDR0_DQ[0]	BU7
DDR0_DQ[1]	BT6
DDR0_DQ[10]	BW13
DDR0_DQ[11]	BY14
DDR0_DQ[12]	BT14
DDR0_DQ[13]	BU15
DDR0_DQ[14]	CA11
DDR0_DQ[15]	BY12
DDR0_DQ[16]	CE9
DDR0_DQ[17]	CF8
DDR0_DQ[18]	CK10
DDR0_DQ[19]	CJ11
DDR0_DQ[2]	CA9
DDR0_DQ[20]	CD10
DDR0_DQ[21]	CE11
DDR0_DQ[22]	CK8
DDR0_DQ[23]	CJ9
DDR0_DQ[24]	CE13
DDR0_DQ[25]	CG15
DDR0_DQ[26]	CM14
DDR0_DQ[27]	CH14
DDR0_DQ[28]	CC13
DDR0_DQ[29]	CD14
DDR0_DQ[3]	CB8

Table 6-1.   Processor Land List

Land Name	Land Number
DDR0_DQ[30]	CM12
DDR0_DQ[31]	CL13
DDR0_DQ[32]	CK28
DDR0_DQ[33]	CH28
DDR0_DQ[34]	CK32
DDR0_DQ[35]	CH32
DDR0_DQ[36]	CL27
DDR0_DQ[37]	CJ27
DDR0_DQ[38]	CL31
DDR0_DQ[39]	CJ31
DDR0_DQ[4]	BT8
DDR0_DQ[40]	CD28
DDR0_DQ[41]	CB28
DDR0_DQ[42]	CD32
DDR0_DQ[43]	CB32
DDR0_DQ[44]	CE27
DDR0_DQ[45]	CC27
DDR0_DQ[46]	CE31
DDR0_DQ[47]	CC31
DDR0_DQ[48]	CE35
DDR0_DQ[49]	CC35
DDR0_DQ[5]	BU9
DDR0_DQ[50]	CE39
DDR0_DQ[51]	CC39
DDR0_DQ[52]	CF34
DDR0_DQ[53]	CD34
DDR0_DQ[54]	CF38
DDR0_DQ[55]	CD38
DDR0_DQ[56]	CL35
DDR0_DQ[57]	CJ35
DDR0_DQ[58]	CL39
DDR0_DQ[59]	CJ39
DDR0_DQ[6]	CA7
DDR0_DQ[60]	CM34
DDR0_DQ[61]	CK34
DDR0_DQ[62]	CM38
DDR0_DQ[63]	CK38
DDR0_DQ[7]	CB6
DDR0_DQ[8]	BT12

Table 6-1. **Processor Land List**

Land Name	Land Number
DDR0_DQ[9]	BU11
DDR0_DQS_DN[0]	BV6
DDR0_DQS_DN[1]	BW11
DDR0_DQS_DN[10]	BV14
DDR0_DQS_DN[11]	CH8
DDR0_DQS_DN[12]	CF14
DDR0_DQS_DN[13]	CJ29
DDR0_DQS_DN[14]	CC29
DDR0_DQS_DN[15]	CD36
DDR0_DQS_DN[16]	CK36
DDR0_DQS_DN[17]	CW9
DDR0_DQS_DN[2]	CG11
DDR0_DQS_DN[3]	CJ13
DDR0_DQS_DN[4]	CM30
DDR0_DQS_DN[5]	CF30
DDR0_DQS_DN[6]	CE37
DDR0_DQS_DN[7]	CL37
DDR0_DQS_DN[8]	CT10
DDR0_DQS_DN[9]	BW9
DDR0_DQS_DP[0]	BY6
DDR0_DQS_DP[1]	BV12
DDR0_DQS_DP[10]	BU13
DDR0_DQS_DP[11]	CG9
DDR0_DQS_DP[12]	CG13
DDR0_DQS_DP[13]	CL29
DDR0_DQS_DP[14]	CE29
DDR0_DQS_DP[15]	CF36
DDR0_DQS_DP[16]	CM36
DDR0_DQS_DP[17]	CU9
DDR0_DQS_DP[2]	CH10
DDR0_DQS_DP[3]	CK14
DDR0_DQS_DP[4]	CK30
DDR0_DQS_DP[5]	CD30
DDR0_DQS_DP[6]	CC37
DDR0_DQS_DP[7]	CJ37
DDR0_DQS_DP[8]	CV10
DDR0_DQS_DP[9]	BV8
DDR0_ECC[0]	CT8
DDR0_ECC[1]	CV8

Table 6-1. **Processor Land List**

Land Name	Land Number
DDR0_ECC[2]	CW11
DDR0_ECC[3]	CU11
DDR0_ECC[4]	CP8
DDR0_ECC[5]	CN9
DDR0_ECC[6]	CP10
DDR0_ECC[7]	CR11
DDR0_MA[0]	CP22
DDR0_MA[1]	CR21
DDR0_MA[10]	CP24
DDR0_MA[11]	CP18
DDR0_MA[12]	CR17
DDR0_MA[13]	CE23
DDR0_MA[14]	CJ21
DDR0_MA[15]	CL25
DDR0_MA[16]	CL23
DDR0_MA[17]	CD24
DDR0_MA[2]	CT22
DDR0_MA[3]	CN21
DDR0_MA[4]	CP20
DDR0_MA[5]	CL19
DDR0_MA[6]	CN19
DDR0_MA[7]	CH18
DDR0_MA[8]	CJ19
DDR0_MA[9]	CK18
DDR0_ODT[0]	CF22
DDR0_ODT[1]	CN25
DDR0_ODT[2]	CJ23
DDR0_ODT[3]	CC23
DDR0_ODT[4]	CF24
DDR0_ODT[5]	CE25
DDR0_PAR	CK20
DDR01_VREF	BY16
DDR1_ACT_N	CT16
DDR1_ALERT_N	CR15
DDR1_BA[0]	CW23
DDR1_BA[1]	CV22
DDR1_BG[0]	CV16
DDR1_BG[1]	CP16
DDR1_CID[2]	CR25

Table 6-1. **Processor Land List**

Land Name	Land Number
DDR1_CKE[0]	DA17
DDR1_CKE[1]	DC17
DDR1_CKE[2]	DD16
DDR1_CKE[3]	DF16
DDR1_CKE[4]	CY16
DDR1_CKE[5]	DA15
DDR1_CLK_DN[0]	DC21
DDR1_CLK_DN[1]	DD18
DDR1_CLK_DN[2]	DD20
DDR1_CLK_DN[3]	DC19
DDR1_CLK_DP[0]	DE21
DDR1_CLK_DP[1]	DF18
DDR1_CLK_DP[2]	DF20
DDR1_CLK_DP[3]	DE19
DDR1_CS_N[0]	DF22
DDR1_CS_N[1]	DE23
DDR1_CS_N[2]/ CID[0]	CT26
DDR1_CS_N[3]/ CID[1]	CP26
DDR1_CS_N[4]	DA23
DDR1_CS_N[5]	DD24
DDR1_CS_N[6]/ CID[3]	CY26
DDR1_CS_N[7]/ CID[4]	CV26
DDR1_CS_N[8]	DF24
DDR1_CS_N[9]	DF26
DDR1_DQ[0]	BV4
DDR1_DQ[1]	BU1
DDR1_DQ[10]	CL5
DDR1_DQ[11]	CM4
DDR1_DQ[12]	CE5
DDR1_DQ[13]	CF6
DDR1_DQ[14]	CK6
DDR1_DQ[15]	CL3
DDR1_DQ[16]	CR3
DDR1_DQ[17]	CV2
DDR1_DQ[18]	CT6
DDR1_DQ[19]	CP6
DDR1_DQ[2]	CA3

Table 6-1. Processor Land List

Land Name	Land Number
DDR1_DQ[20]	CR1
DDR1_DQ[21]	CP2
DDR1_DQ[22]	CU5
DDR1_DQ[23]	CR5
DDR1_DQ[24]	DA7
DDR1_DQ[25]	DB8
DDR1_DQ[26]	DE11
DDR1_DQ[27]	DC11
DDR1_DQ[28]	DA5
DDR1_DQ[29]	CY6
DDR1_DQ[3]	CB4
DDR1_DQ[30]	DE9
DDR1_DQ[31]	DF10
DDR1_DQ[32]	CT28
DDR1_DQ[33]	CP28
DDR1_DQ[34]	CT32
DDR1_DQ[35]	CP32
DDR1_DQ[36]	CU27
DDR1_DQ[37]	CR27
DDR1_DQ[38]	CU31
DDR1_DQ[39]	CR31
DDR1_DQ[4]	BT4
DDR1_DQ[40]	DA29
DDR1_DQ[41]	DB30
DDR1_DQ[42]	DC33
DDR1_DQ[43]	DF34
DDR1_DQ[44]	DB28
DDR1_DQ[45]	CY28
DDR1_DQ[46]	DA33
DDR1_DQ[47]	DE33
DDR1_DQ[48]	CU35
DDR1_DQ[49]	CR35
DDR1_DQ[5]	BT2
DDR1_DQ[50]	CU39
DDR1_DQ[51]	CR39
DDR1_DQ[52]	CV34
DDR1_DQ[53]	CT34
DDR1_DQ[54]	CV38
DDR1_DQ[55]	CT38

Table 6-1. Processor Land List

Land Name	Land Number
DDR1_DQ[56]	DC37
DDR1_DQ[57]	DF36
DDR1_DQ[58]	DC39
DDR1_DQ[59]	DA39
DDR1_DQ[6]	CA1
DDR1_DQ[60]	DC35
DDR1_DQ[61]	DB36
DDR1_DQ[62]	DF38
DDR1_DQ[63]	DE39
DDR1_DQ[7]	BY2
DDR1_DQ[8]	CE3
DDR1_DQ[9]	CF4
DDR1_DQS_DN[0]	BW3
DDR1_DQS_DN[1]	CH6
DDR1_DQS_DN[10]	CG3
DDR1_DQS_DN[11]	CU3
DDR1_DQS_DN[12]	DD8
DDR1_DQS_DN[13]	CR29
DDR1_DQS_DN[14]	CY32
DDR1_DQS_DN[15]	CT36
DDR1_DQS_DN[16]	DE37
DDR1_DQS_DN[17]	CY14
DDR1_DQS_DN[2]	CV4
DDR1_DQS_DN[3]	DC9
DDR1_DQS_DN[4]	CV30
DDR1_DQS_DN[5]	DB32
DDR1_DQS_DN[6]	CU37
DDR1_DQS_DN[7]	DA37
DDR1_DQS_DN[8]	DA13
DDR1_DQS_DN[9]	BW1
DDR1_DQS_DP[0]	BY4
DDR1_DQS_DP[1]	CJ5
DDR1_DQS_DP[10]	CH4
DDR1_DQS_DP[11]	CW3
DDR1_DQS_DP[12]	DC7
DDR1_DQS_DP[13]	CU29
DDR1_DQS_DP[14]	DA31
DDR1_DQS_DP[15]	CV36
DDR1_DQS_DP[16]	DD36

Table 6-1. Processor Land List

Land Name	Land Number
DDR1_DQS_DP[17]	CW13
DDR1_DQS_DP[2]	CT4
DDR1_DQS_DP[3]	DB10
DDR1_DQS_DP[4]	CT30
DDR1_DQS_DP[5]	DD32
DDR1_DQS_DP[6]	CR37
DDR1_DQS_DP[7]	DB38
DDR1_DQS_DP[8]	DB14
DDR1_DQS_DP[9]	BV2
DDR1_ECC[0]	CU13
DDR1_ECC[1]	CV14
DDR1_ECC[2]	DD14
DDR1_ECC[3]	DF14
DDR1_ECC[4]	CR13
DDR1_ECC[5]	CT14
DDR1_ECC[6]	DC13
DDR1_ECC[7]	DE13
DDR1_MA[0]	CY22
DDR1_MA[1]	DA21
DDR1_MA[10]	CR23
DDR1_MA[11]	CV18
DDR1_MA[12]	CW17
DDR1_MA[13]	CW25
DDR1_MA[14]	CN23
DDR1_MA[15]	CV24
DDR1_MA[16]	CY24
DDR1_MA[17]	CT24
DDR1_MA[2]	CV20
DDR1_MA[3]	CW21
DDR1_MA[4]	CR19
DDR1_MA[5]	CY20
DDR1_MA[6]	CW19
DDR1_MA[7]	CT18
DDR1_MA[8]	DA19
DDR1_MA[9]	CY18
DDR1_ODT[0]	DD22
DDR1_ODT[1]	DE25
DDR1_ODT[2]	DC23
DDR1_ODT[3]	DC25

Table 6-1. Processor Land List

Land Name	Land Number
DDR1_ODT[4]	DA25
DDR1_ODT[5]	DD26
DDR1_PAR	CT20
DDR2_ACT_N	AE21
DDR2_ALERT_N	P22
DDR2_BA[0]	M14
DDR2_BA[1]	U17
DDR2_BG[0]	AA21
DDR2_BG[1]	AD20
DDR2_CID[2]	U13
DDR2_CKE[0]	R21
DDR2_CKE[1]	U21
DDR2_CKE[2]	T22
DDR2_CKE[3]	Y22
DDR2_CKE[4]	AB22
DDR2_CKE[5]	AD22
DDR2_CLK_DN[0]	W17
DDR2_CLK_DN[1]	Y20
DDR2_CLK_DN[2]	Y18
DDR2_CLK_DN[3]	W19
DDR2_CLK_DP[0]	AA17
DDR2_CLK_DP[1]	AB20
DDR2_CLK_DP[2]	AB18
DDR2_CLK_DP[3]	AA19
DDR2_CS_N[0]	AB16
DDR2_CS_N[1]	T16
DDR2_CS_N[2]/ CID[0]	W13
DDR2_CS_N[3]/ CID[1]	AA13
DDR2_CS_N[4]	P16
DDR2_CS_N[5]	U15
DDR2_CS_N[6]/ CID[3]	AC13
DDR2_CS_N[7]/ CID[4]	AD16
DDR2_CS_N[8]	AD18
DDR2_CS_N[9]	T12
DDR2_DQ[0]	AD38
DDR2_DQ[1]	AA37
DDR2_DQ[10]	V30

Table 6-1. Processor Land List

Land Name	Land Number
DDR2_DQ[11]	T30
DDR2_DQ[12]	U35
DDR2_DQ[13]	R35
DDR2_DQ[14]	T32
DDR2_DQ[15]	W31
DDR2_DQ[16]	AD34
DDR2_DQ[17]	AB34
DDR2_DQ[18]	AD30
DDR2_DQ[19]	AB30
DDR2_DQ[2]	R37
DDR2_DQ[20]	AC35
DDR2_DQ[21]	AA35
DDR2_DQ[22]	AE31
DDR2_DQ[23]	AC31
DDR2_DQ[24]	U27
DDR2_DQ[25]	R27
DDR2_DQ[26]	U23
DDR2_DQ[27]	R23
DDR2_DQ[28]	V28
DDR2_DQ[29]	T28
DDR2_DQ[3]	Y38
DDR2_DQ[30]	V24
DDR2_DQ[31]	T24
DDR2_DQ[32]	N9
DDR2_DQ[33]	K8
DDR2_DQ[34]	R7
DDR2_DQ[35]	P6
DDR2_DQ[36]	J9
DDR2_DQ[37]	L9
DDR2_DQ[38]	K6
DDR2_DQ[39]	M6
DDR2_DQ[4]	AE37
DDR2_DQ[40]	U9
DDR2_DQ[41]	W11
DDR2_DQ[42]	AA11
DDR2_DQ[43]	AB8
DDR2_DQ[44]	T10
DDR2_DQ[45]	U11
DDR2_DQ[46]	AA9

Table 6-1. Processor Land List

Land Name	Land Number
DDR2_DQ[47]	Y8
DDR2_DQ[48]	AE11
DDR2_DQ[49]	AF12
DDR2_DQ[5]	AC39
DDR2_DQ[50]	AK12
DDR2_DQ[51]	AL13
DDR2_DQ[52]	AG15
DDR2_DQ[53]	AF14
DDR2_DQ[54]	AK14
DDR2_DQ[55]	AL15
DDR2_DQ[56]	AG9
DDR2_DQ[57]	AG7
DDR2_DQ[58]	AK10
DDR2_DQ[59]	AL9
DDR2_DQ[6]	T38
DDR2_DQ[60]	AE7
DDR2_DQ[61]	AE9
DDR2_DQ[62]	AK8
DDR2_DQ[63]	AL7
DDR2_DQ[7]	U37
DDR2_DQ[8]	V34
DDR2_DQ[9]	U33
DDR2_DQS_DN[0]	W37
DDR2_DQS_DN[1]	V32
DDR2_DQS_DN[10]	R33
DDR2_DQS_DN[11]	AA33
DDR2_DQS_DN[12]	T26
DDR2_DQS_DN[13]	L7
DDR2_DQS_DN[14]	W9
DDR2_DQS_DN[15]	AJ15
DDR2_DQS_DN[16]	AJ9
DDR2_DQS_DN[17]	AB26
DDR2_DQS_DN[2]	AD32
DDR2_DQS_DN[3]	W25
DDR2_DQS_DN[4]	P8
DDR2_DQS_DN[5]	Y10
DDR2_DQS_DN[6]	AJ13
DDR2_DQS_DN[7]	AH8
DDR2_DQS_DN[8]	AE25

Table 6-1. Processor Land List

Land Name	Land Number
DDR2_DQS_DN[9]	AC37
DDR2_DQS_DP[0]	V38
DDR2_DQS_DP[1]	U31
DDR2_DQS_DP[10]	T34
DDR2_DQS_DP[11]	AC33
DDR2_DQS_DP[12]	V26
DDR2_DQS_DP[13]	M8
DDR2_DQS_DP[14]	V8
DDR2_DQS_DP[15]	AH16
DDR2_DQS_DP[16]	AH10
DDR2_DQS_DP[17]	AD26
DDR2_DQS_DP[2]	AB32
DDR2_DQS_DP[3]	U25
DDR2_DQS_DP[4]	N7
DDR2_DQS_DP[5]	AB10
DDR2_DQS_DP[6]	AH12
DDR2_DQS_DP[7]	AJ7
DDR2_DQS_DP[8]	AC25
DDR2_DQS_DP[9]	AB38
DDR2_ECC[0]	AC27
DDR2_ECC[1]	AA27
DDR2_ECC[2]	AC23
DDR2_ECC[3]	AA23
DDR2_ECC[4]	AD28
DDR2_ECC[5]	AB28
DDR2_ECC[6]	AD24
DDR2_ECC[7]	AB24
DDR2_MA[0]	L15
DDR2_MA[1]	M16
DDR2_MA[10]	AA15
DDR2_MA[11]	T20
DDR2_MA[12]	W21
DDR2_MA[13]	P12
DDR2_MA[14]	Y14
DDR2_MA[15]	R13
DDR2_MA[16]	P14
DDR2_MA[17]	T14
DDR2_MA[2]	T18
DDR2_MA[3]	L17

Table 6-1. Processor Land List

Land Name	Land Number
DDR2_MA[4]	R19
DDR2_MA[5]	P18
DDR2_MA[6]	M18
DDR2_MA[7]	U19
DDR2_MA[8]	L19
DDR2_MA[9]	P20
DDR2_ODT[0]	Y16
DDR2_ODT[1]	W15
DDR2_ODT[2]	R15
DDR2_ODT[3]	AB14
DDR2_ODT[4]	AE17
DDR2_ODT[5]	AD14
DDR2_PAR	R17
DDR23_VREF	T40
DDR3_ACT_N	L21
DDR3_ALERT_N	M22
DDR3_BA[0]	G13
DDR3_BA[1]	K14
DDR3_BG[0]	J21
DDR3_BG[1]	G21
DDR3_CID[2]	J11
DDR3_CKE[0]	F22
DDR3_CKE[1]	E21
DDR3_CKE[2]	A21
DDR3_CKE[3]	D22
DDR3_CKE[4]	B22
DDR3_CKE[5]	K22
DDR3_CLK_DN[0]	C17
DDR3_CLK_DN[1]	D20
DDR3_CLK_DN[2]	D18
DDR3_CLK_DN[3]	C19
DDR3_CLK_DP[0]	A17
DDR3_CLK_DP[1]	B20
DDR3_CLK_DP[2]	B18
DDR3_CLK_DP[3]	A19
DDR3_CS_N[0]	B16
DDR3_CS_N[1]	C15
DDR3_CS_N[2]/CID[0]	F10

Table 6-1. Processor Land List

Land Name	Land Number
DDR3_CS_N[3]/CID[1]	H10
DDR3_CS_N[4]	A15
DDR3_CS_N[5]	F14
DDR3_CS_N[6]/CID[3]	G11
DDR3_CS_N[7]/CID[4]	A11
DDR3_CS_N[8]	B14
DDR3_CS_N[9]	B12
DDR3_DQ[0]	D38
DDR3_DQ[1]	B38
DDR3_DQ[10]	G31
DDR3_DQ[11]	E31
DDR3_DQ[12]	F34
DDR3_DQ[13]	E35
DDR3_DQ[14]	D32
DDR3_DQ[15]	E33
DDR3_DQ[16]	K34
DDR3_DQ[17]	M34
DDR3_DQ[18]	K30
DDR3_DQ[19]	M30
DDR3_DQ[2]	L37
DDR3_DQ[20]	J35
DDR3_DQ[21]	L35
DDR3_DQ[22]	L31
DDR3_DQ[23]	N31
DDR3_DQ[24]	F28
DDR3_DQ[25]	E27
DDR3_DQ[26]	F24
DDR3_DQ[27]	E23
DDR3_DQ[28]	G29
DDR3_DQ[29]	E29
DDR3_DQ[3]	M38
DDR3_DQ[30]	C25
DDR3_DQ[31]	B24
DDR3_DQ[32]	K4
DDR3_DQ[33]	H4
DDR3_DQ[34]	J1
DDR3_DQ[35]	L1
DDR3_DQ[36]	P4

Table 6-1. Processor Land List

Land Name	Land Number
DDR3_DQ[37]	N3
DDR3_DQ[38]	K2
DDR3_DQ[39]	R3
DDR3_DQ[4]	C39
DDR3_DQ[40]	E9
DDR3_DQ[41]	F8
DDR3_DQ[42]	E5
DDR3_DQ[43]	F6
DDR3_DQ[44]	C9
DDR3_DQ[45]	A9
DDR3_DQ[46]	D6
DDR3_DQ[47]	G7
DDR3_DQ[48]	AG3
DDR3_DQ[49]	AG1
DDR3_DQ[5]	J39
DDR3_DQ[50]	AL3
DDR3_DQ[51]	AL5
DDR3_DQ[52]	AG5
DDR3_DQ[53]	AE3
DDR3_DQ[54]	AJ3
DDR3_DQ[55]	AL1
DDR3_DQ[56]	V4
DDR3_DQ[57]	W3
DDR3_DQ[58]	AC5
DDR3_DQ[59]	AE5
DDR3_DQ[6]	G37
DDR3_DQ[60]	U5
DDR3_DQ[61]	V6
DDR3_DQ[62]	AC3
DDR3_DQ[63]	AB6
DDR3_DQ[7]	K38
DDR3_DQ[8]	A35
DDR3_DQ[9]	B34
DDR3_DQS_DN[0]	C37
DDR3_DQS_DN[1]	A33
DDR3_DQS_DN[10]	D34
DDR3_DQS_DN[11]	L33
DDR3_DQS_DN[12]	D26
DDR3_DQS_DN[13]	L3

Table 6-1. Processor Land List

Land Name	Land Number
DDR3_DQS_DN[14]	D8
DDR3_DQS_DN[15]	AJ5
DDR3_DQS_DN[16]	W5
DDR3_DQS_DN[17]	K26
DDR3_DQS_DN[2]	K32
DDR3_DQS_DN[3]	G25
DDR3_DQS_DN[4]	G3
DDR3_DQS_DN[5]	C7
DDR3_DQS_DN[6]	AJ1
DDR3_DQS_DN[7]	AA5
DDR3_DQS_DN[8]	N25
DDR3_DQS_DN[9]	H38
DDR3_DQS_DP[0]	E37
DDR3_DQS_DP[1]	B32
DDR3_DQS_DP[10]	C35
DDR3_DQS_DP[11]	J33
DDR3_DQS_DP[12]	F26
DDR3_DQS_DP[13]	M4
DDR3_DQS_DP[14]	B8
DDR3_DQS_DP[15]	AH4
DDR3_DQS_DP[16]	Y6
DDR3_DQS_DP[17]	M26
DDR3_DQS_DP[2]	M32
DDR3_DQS_DP[3]	E25
DDR3_DQS_DP[4]	H2
DDR3_DQS_DP[5]	E7
DDR3_DQS_DP[6]	AK2
DDR3_DQS_DP[7]	AB4
DDR3_DQS_DP[8]	L25
DDR3_DQS_DP[9]	F38
DDR3_ECC[0]	L27
DDR3_ECC[1]	J27
DDR3_ECC[2]	L23
DDR3_ECC[3]	J23
DDR3_ECC[4]	K28
DDR3_ECC[5]	M28
DDR3_ECC[6]	M24
DDR3_ECC[7]	K24
DDR3_MA[0]	G15

Table 6-1. Processor Land List

Land Name	Land Number
DDR3_MA[1]	K16
DDR3_MA[10]	L13
DDR3_MA[11]	K20
DDR3_MA[12]	M20
DDR3_MA[13]	M12
DDR3_MA[14]	K12
DDR3_MA[15]	F12
DDR3_MA[16]	J13
DDR3_MA[17]	L11
DDR3_MA[2]	F16
DDR3_MA[3]	G17
DDR3_MA[4]	J17
DDR3_MA[5]	K18
DDR3_MA[6]	F18
DDR3_MA[7]	J19
DDR3_MA[8]	G19
DDR3_MA[9]	F20
DDR3_ODT[0]	D16
DDR3_ODT[1]	A13
DDR3_ODT[2]	D14
DDR3_ODT[3]	D12
DDR3_ODT[4]	E13
DDR3_ODT[5]	E11
DDR3_PAR	J15
DEBUG_EN_N	F40
DMI_RX_DN[0]	B50
DMI_RX_DN[1]	C49
DMI_RX_DN[2]	B48
DMI_RX_DN[3]	C47
DMI_RX_DP[0]	D50
DMI_RX_DP[1]	E49
DMI_RX_DP[2]	D48
DMI_RX_DP[3]	E47
DMI_TX_DN[0]	C45
DMI_TX_DN[1]	B44
DMI_TX_DN[2]	C43
DMI_TX_DN[3]	B42
DMI_TX_DP[0]	E45
DMI_TX_DP[1]	D44

Table 6-1. Processor Land List

Land Name	Land Number
DMI_TX_DP[2]	E43
DMI_TX_DP[3]	D42
DRAM_PWR_OK_C01	CH16
DRAM_PWR_OK_C23	W29
EAR_N	CE53
ERROR_N[0]	BD50
ERROR_N[1]	BB48
ERROR_N[2]	BB52
FIVR_FAULT	CY40
FRMAGENT	Y48
MEM_HOT_C01_N	CL33
MEM_HOT_C23_N	P36
MSMI_N	H52
PE_HP_SCL	B46
PE_HP_SDA	D46
PE1A_RX_DN[0]	C51
PE1A_RX_DN[1]	D52
PE1A_RX_DN[2]	D54
PE1A_RX_DN[3]	E55
PE1A_RX_DP[0]	E51
PE1A_RX_DP[1]	F52
PE1A_RX_DP[2]	F54
PE1A_RX_DP[3]	G55
PE1A_TX_DN[0]	H42
PE1A_TX_DN[1]	J43
PE1A_TX_DN[2]	H44
PE1A_TX_DN[3]	J45
PE1A_TX_DP[0]	K42
PE1A_TX_DP[1]	L43
PE1A_TX_DP[2]	K44
PE1A_TX_DP[3]	L45
PE1B_RX_DN[4]	J53
PE1B_RX_DN[5]	K54
PE1B_RX_DN[6]	J57
PE1B_RX_DN[7]	K56
PE1B_RX_DP[4]	L53
PE1B_RX_DP[5]	M54
PE1B_RX_DP[6]	L57
PE1B_RX_DP[7]	M56

Table 6-1. Processor Land List

Land Name	Land Number
PE1B_TX_DN[4]	H46
PE1B_TX_DN[5]	J47
PE1B_TX_DN[6]	H48
PE1B_TX_DN[7]	J49
PE1B_TX_DP[4]	K46
PE1B_TX_DP[5]	L47
PE1B_TX_DP[6]	K48
PE1B_TX_DP[7]	L49
PE2A_RX_DN[0]	L55
PE2A_RX_DN[1]	T54
PE2A_RX_DN[2]	T56
PE2A_RX_DN[3]	U55
PE2A_RX_DP[0]	N55
PE2A_RX_DP[1]	V54
PE2A_RX_DP[2]	V56
PE2A_RX_DP[3]	W55
PE2A_TX_DN[0]	AN49
PE2A_TX_DN[1]	AM50
PE2A_TX_DN[2]	AN51
PE2A_TX_DN[3]	AM52
PE2A_TX_DP[0]	AR49
PE2A_TX_DP[1]	AP50
PE2A_TX_DP[2]	AR51
PE2A_TX_DP[3]	AP52
PE2B_RX_DN[4]	AB54
PE2B_RX_DN[5]	AB56
PE2B_RX_DN[6]	AC55
PE2B_RX_DN[7]	AE57
PE2B_RX_DP[4]	AD54
PE2B_RX_DP[5]	AD56
PE2B_RX_DP[6]	AE55
PE2B_RX_DP[7]	AF58
PE2B_TX_DN[4]	AG53
PE2B_TX_DN[5]	AH54
PE2B_TX_DN[6]	AN53
PE2B_TX_DN[7]	AP54
PE2B_TX_DP[4]	AJ53
PE2B_TX_DP[5]	AK54
PE2B_TX_DP[6]	AR53

Table 6-1. Processor Land List

Land Name	Land Number
PE2B_TX_DP[7]	AT54
PE2C_RX_DN[10]	AJ57
PE2C_RX_DN[11]	AR57
PE2C_RX_DN[8]	AH56
PE2C_RX_DN[9]	AK58
PE2C_RX_DP[10]	AL57
PE2C_RX_DP[11]	AU57
PE2C_RX_DP[8]	AK56
PE2C_RX_DP[9]	AM58
PE2C_TX_DN[10]	AY54
PE2C_TX_DN[11]	AW51
PE2C_TX_DN[8]	AV52
PE2C_TX_DN[9]	AW53
PE2C_TX_DP[10]	BB54
PE2C_TX_DP[11]	BA51
PE2C_TX_DP[8]	AY52
PE2C_TX_DP[9]	BA53
PE2D_RX_DN[12]	AT58
PE2D_RX_DN[13]	AP56
PE2D_RX_DN[14]	AY58
PE2D_RX_DN[15]	AY56
PE2D_RX_DP[12]	AV58
PE2D_RX_DP[13]	AT56
PE2D_RX_DP[14]	BA57
PE2D_RX_DP[15]	BB56
PE2D_TX_DN[12]	AV50
PE2D_TX_DN[13]	AW49
PE2D_TX_DN[14]	AV48
PE2D_TX_DN[15]	AW47
PE2D_TX_DP[12]	AY50
PE2D_TX_DP[13]	BA49
PE2D_TX_DP[14]	AY48
PE2D_TX_DP[15]	BA47
PE3A_RX_DN[0]	AF44
PE3A_RX_DN[1]	AG45
PE3A_RX_DN[2]	AF46
PE3A_RX_DN[3]	AA49
PE3A_RX_DP[0]	AH44
PE3A_RX_DP[1]	AJ45

Table 6-1.   Processor Land List

Land Name	Land Number
PE3A_RX_DP[2]	AH46
PE3A_RX_DP[3]	AC49
PE3A_TX_DN[0]	H50
PE3A_TX_DN[1]	J51
PE3A_TX_DN[2]	R47
PE3A_TX_DN[3]	P48
PE3A_TX_DP[0]	K50
PE3A_TX_DP[1]	L51
PE3A_TX_DP[2]	U47
PE3A_TX_DP[3]	T48
PE3B_RX_DN[4]	Y50
PE3B_RX_DN[5]	Y52
PE3B_RX_DN[6]	AA53
PE3B_RX_DN[7]	AA51
PE3B_RX_DP[4]	AB50
PE3B_RX_DP[5]	AB52
PE3B_RX_DP[6]	AC53
PE3B_RX_DP[7]	AC51
PE3B_TX_DN[4]	P52
PE3B_TX_DN[5]	R51
PE3B_TX_DN[6]	P50
PE3B_TX_DN[7]	R49
PE3B_TX_DP[4]	T52
PE3B_TX_DP[5]	U51
PE3B_TX_DP[6]	T50
PE3B_TX_DP[7]	U49
PE3C_RX_DN[10]	AF50
PE3C_RX_DN[11]	AG49
PE3C_RX_DN[8]	AF48
PE3C_RX_DN[9]	AG51
PE3C_RX_DP[10]	AH50
PE3C_RX_DP[11]	AJ49
PE3C_RX_DP[8]	AH48
PE3C_RX_DP[9]	AJ51
PE3C_TX_DN[10]	AA47
PE3C_TX_DN[11]	Y46
PE3C_TX_DN[8]	P46
PE3C_TX_DN[9]	R45
PE3C_TX_DP[10]	AC47

Table 6-1.   Processor Land List

Land Name	Land Number
PE3C_TX_DP[11]	AB46
PE3C_TX_DP[8]	T46
PE3C_TX_DP[9]	U45
PE3D_RX_DN[12]	AG47
PE3D_RX_DN[13]	AN47
PE3D_RX_DN[14]	AM46
PE3D_RX_DN[15]	AN45
PE3D_RX_DP[12]	AJ47
PE3D_RX_DP[13]	AR47
PE3D_RX_DP[14]	AP46
PE3D_RX_DP[15]	AR45
PE3D_TX_DN[12]	AA45
PE3D_TX_DN[13]	Y44
PE3D_TX_DN[14]	AC43
PE3D_TX_DN[15]	T44
PE3D_TX_DP[12]	AC45
PE3D_TX_DP[13]	AB44
PE3D_TX_DP[14]	AA43
PE3D_TX_DP[15]	P44
PECI	CG55
PM_FAST_WAKE_N	AV44
PMSYNC	K52
PRDY_N	CU49
PREQ_N	CW49
PROC_ID	AB48
PROCHOT_N	BL51
PWR_DEBUG_N	AC41
PWRGOOD	BJ53
QPI0_CLKRX_DN	BM58
QPI0_CLKRX_DP	BK58
QPI0_CLKTX_DN	CF44
QPI0_CLKTX_DP	CD44
QPI0_DRX_DN[0]	BG51
QPI0_DRX_DN[1]	BF52
QPI0_DRX_DN[10]	BN55
QPI0_DRX_DN[11]	BP54
QPI0_DRX_DN[12]	BN53
QPI0_DRX_DN[13]	BP52
QPI0_DRX_DN[14]	BR51

Table 6-1.   Processor Land List

Land Name	Land Number
QPI0_DRX_DN[15]	BP50
QPI0_DRX_DN[16]	BR49
QPI0_DRX_DN[17]	BJ49
QPI0_DRX_DN[18]	BP48
QPI0_DRX_DN[19]	BR47
QPI0_DRX_DN[2]	BG53
QPI0_DRX_DN[3]	BG55
QPI0_DRX_DN[4]	BH56
QPI0_DRX_DN[5]	BH54
QPI0_DRX_DN[6]	BH50
QPI0_DRX_DN[7]	BF58
QPI0_DRX_DN[8]	BG57
QPI0_DRX_DN[9]	BP56
QPI0_DRX_DP[0]	BJ51
QPI0_DRX_DP[1]	BH52
QPI0_DRX_DP[10]	BL55
QPI0_DRX_DP[11]	BM54
QPI0_DRX_DP[12]	BL53
QPI0_DRX_DP[13]	BM52
QPI0_DRX_DP[14]	BN51
QPI0_DRX_DP[15]	BM50
QPI0_DRX_DP[16]	BN49
QPI0_DRX_DP[17]	BG49
QPI0_DRX_DP[18]	BM48
QPI0_DRX_DP[19]	BN47
QPI0_DRX_DP[2]	BE53
QPI0_DRX_DP[3]	BE55
QPI0_DRX_DP[4]	BF56
QPI0_DRX_DP[5]	BF54
QPI0_DRX_DP[6]	BF50
QPI0_DRX_DP[7]	BD58
QPI0_DRX_DP[8]	BE57
QPI0_DRX_DP[9]	BM56
QPI0_DTX_DN[0]	BW49
QPI0_DTX_DN[1]	BW51
QPI0_DTX_DN[10]	CF46
QPI0_DTX_DN[11]	BY52
QPI0_DTX_DN[12]	CA47
QPI0_DTX_DN[13]	CA49

Table 6-1. Processor Land List

Land Name	Land Number
QPI0_DTX_DN[14]	CG47
QPI0_DTX_DN[15]	CF48
QPI0_DTX_DN[16]	CF50
QPI0_DTX_DN[17]	CF52
QPI0_DTX_DN[18]	CG51
QPI0_DTX_DN[19]	CG49
QPI0_DTX_DN[2]	BW53
QPI0_DTX_DN[3]	BY54
QPI0_DTX_DN[4]	BW55
QPI0_DTX_DN[5]	BV58
QPI0_DTX_DN[6]	BW47
QPI0_DTX_DN[7]	BW57
QPI0_DTX_DN[8]	BY56
QPI0_DTX_DN[9]	BW45
QPI0_DTX_DP[0]	BV50
QPI0_DTX_DP[1]	BV52
QPI0_DTX_DP[10]	CD46
QPI0_DTX_DP[11]	CA51
QPI0_DTX_DP[12]	BY48
QPI0_DTX_DP[13]	BY50
QPI0_DTX_DP[14]	CE47
QPI0_DTX_DP[15]	CD48
QPI0_DTX_DP[16]	CD50
QPI0_DTX_DP[17]	CD52
QPI0_DTX_DP[18]	CE51
QPI0_DTX_DP[19]	CE49
QPI0_DTX_DP[2]	BU53
QPI0_DTX_DP[3]	BV54
QPI0_DTX_DP[4]	BU55
QPI0_DTX_DP[5]	BT58
QPI0_DTX_DP[6]	BV48
QPI0_DTX_DP[7]	BU57
QPI0_DTX_DP[8]	BV56
QPI0_DTX_DP[9]	BV46
QPI1_CLKRX_DN	CL53
QPI1_CLKRX_DP	CJ53
QPI1_CLKTX_DN	CY54
QPI1_CLKTX_DP	DB54
QPI1_DRX_DN[0]	CM44

Table 6-1. Processor Land List

Land Name	Land Number
QPI1_DRX_DN[1]	CN45
QPI1_DRX_DN[10]	CT54
QPI1_DRX_DN[11]	CR55
QPI1_DRX_DN[12]	CT56
QPI1_DRX_DN[13]	CR57
QPI1_DRX_DN[14]	CP58
QPI1_DRX_DN[15]	CK56
QPI1_DRX_DN[16]	CL55
QPI1_DRX_DN[17]	CF54
QPI1_DRX_DN[18]	CF56
QPI1_DRX_DN[19]	CE55
QPI1_DRX_DN[2]	CM46
QPI1_DRX_DN[3]	CN47
QPI1_DRX_DN[4]	CM48
QPI1_DRX_DN[5]	CN49
QPI1_DRX_DN[6]	CM50
QPI1_DRX_DN[7]	CN51
QPI1_DRX_DN[8]	CV52
QPI1_DRX_DN[9]	CU53
QPI1_DRX_DP[0]	CK44
QPI1_DRX_DP[1]	CL45
QPI1_DRX_DP[10]	CP54
QPI1_DRX_DP[11]	CU55
QPI1_DRX_DP[12]	CV56
QPI1_DRX_DP[13]	CU57
QPI1_DRX_DP[14]	CT58
QPI1_DRX_DP[15]	CM56
QPI1_DRX_DP[16]	CJ55
QPI1_DRX_DP[17]	CD54
QPI1_DRX_DP[18]	CD56
QPI1_DRX_DP[19]	CC55
QPI1_DRX_DP[2]	CK46
QPI1_DRX_DP[3]	CL47
QPI1_DRX_DP[4]	CK48
QPI1_DRX_DP[5]	CL49
QPI1_DRX_DP[6]	CK50
QPI1_DRX_DP[7]	CL51
QPI1_DRX_DP[8]	CT52
QPI1_DRX_DP[9]	CR53

Table 6-1. Processor Land List

Land Name	Land Number
QPI1_DTX_DN[0]	DE41
QPI1_DTX_DN[1]	DB42
QPI1_DTX_DN[10]	DD48
QPI1_DTX_DN[11]	CW45
QPI1_DTX_DN[12]	DC49
QPI1_DTX_DN[13]	DD50
QPI1_DTX_DN[14]	CW47
QPI1_DTX_DN[15]	DC51
QPI1_DTX_DN[16]	DD52
QPI1_DTX_DN[17]	CV48
QPI1_DTX_DN[18]	CV46
QPI1_DTX_DN[19]	CV44
QPI1_DTX_DN[2]	CW41
QPI1_DTX_DN[3]	DE43
QPI1_DTX_DN[4]	DB44
QPI1_DTX_DN[5]	CV42
QPI1_DTX_DN[6]	DE45
QPI1_DTX_DN[7]	DB46
QPI1_DTX_DN[8]	CW43
QPI1_DTX_DN[9]	DE47
QPI1_DTX_DP[0]	DC41
QPI1_DTX_DP[1]	DD42
QPI1_DTX_DP[10]	DB48
QPI1_DTX_DP[11]	CU45
QPI1_DTX_DP[12]	DE49
QPI1_DTX_DP[13]	DB50
QPI1_DTX_DP[14]	CU47
QPI1_DTX_DP[15]	DE51
QPI1_DTX_DP[16]	DB52
QPI1_DTX_DP[17]	CT48
QPI1_DTX_DP[18]	CT46
QPI1_DTX_DP[19]	CT44
QPI1_DTX_DP[2]	CU41
QPI1_DTX_DP[3]	DC43
QPI1_DTX_DP[4]	DD44
QPI1_DTX_DP[5]	CT42
QPI1_DTX_DP[6]	DC45
QPI1_DTX_DP[7]	DD46
QPI1_DTX_DP[8]	CU43

Table 6-1. Processor Land List

Land Name	Land Number
QPI1_DTX_DP[9]	DC47
RESET_N	CR43
RSVD	CF40
RSVD	CP40
RSVD	R41
RSVD	M40
RSVD	AV46
RSVD	N41
RSVD	CU51
RSVD	CW51
RSVD	B54
RSVD	F58
RSVD	E57
RSVD	DB56
RSVD	A53
RSVD	AL55
RSVD	BD48
RSVD	AJ55
RSVD	AY46
RSVD	CR51
RSVD	BK44
RSVD	BN45
RSVD	BH46
RSVD	BG43
RSVD	BE43
RSVD	BJ45
RSVD	BH44
RSVD	BJ43
RSVD	BM44
RSVD	BR45
RSVD	BL43
RSVD	BP44
RSVD	BU43
RSVD	BR43
RSVD	BD44
RSVD	BF44
RSVD	BT44
RSVD	CA43
RSVD	BV44

Table 6-1. Processor Land List

Land Name	Land Number
RSVD	BY44
RSVD	DE53
RSVD	C53
RSVD	F56
RSVD	D56
RSVD	K58
RSVD	H58
RSVD	AU55
RSVD	AR55
RSVD	DE55
RSVD	DD54
RSVD	CY58
RSVD	DA57
RSVD	BP46
RSVD	BM46
RSVD	DC3
RSVD	CY56
RSVD	R53
RSVD	U53
RSVD	CT50
RSVD	DA11
RSVD	BL47
RSVD	CA53
RSVD	AM54
RSVD	AP48
RSVD	AE45
RSVD	AA41
RSVD	Y54
RSVD	W41
RSVD	V42
RSVD	R43
RSVD	P42
RSVD	J41
RSVD	H56
RSVD	G43
RSVD	F46
RSVD	E53
RSVD	BF48
RSVD	C41

Table 6-1. Processor Land List

Land Name	Land Number
RSVD	BH48
RSVD	AM44
RSVD	CN43
RSVD	CL43
SAFE_MODE_BOOT	BK56
SKTOCC_N	BU49
SOCKET_ID[0]	CP52
SOCKET_ID[1]	CC53
SVIDALERT_N	AN43
SVIDCLK	AU43
SVIDDATA	AR43
TCK	CA45
TDI	CF42
TDO	CG41
TEST[0]	DB2
TEST[1]	DB4
TEST[2]	D2
TEST[3]	C3
TEST[4]	BA55
THERMTRIP_N	BJ47
TMS	BY46
TRST_N	CV50
TXT_AGENT	AH52
TXT_PLTEN	AF52
VCCD_01	CB16
VCCD_01	CB18
VCCD_01	CB20
VCCD_01	CB22
VCCD_01	CB24
VCCD_01	CB26
VCCD_01	CG17
VCCD_01	CG19
VCCD_01	CG21
VCCD_01	CG23
VCCD_01	CG25
VCCD_01	CM16
VCCD_01	CM18
VCCD_01	CM20
VCCD_01	CM22

Table 6-1. **Processor Land List**

Land Name	Land Number
VCCD_01	CM24
VCCD_01	CM26
VCCD_01	CU17
VCCD_01	CU19
VCCD_01	CU21
VCCD_01	CU23
VCCD_01	CU25
VCCD_01	DB16
VCCD_01	DB18
VCCD_01	DB20
VCCD_01	DB22
VCCD_01	DB24
VCCD_01	DB26
VCCD_01	DE17
VCCD_23	AC15
VCCD_23	AC17
VCCD_23	AC19
VCCD_23	AC21
VCCD_23	C11
VCCD_23	C13
VCCD_23	C21
VCCD_23	E15
VCCD_23	E17
VCCD_23	E19
VCCD_23	H12
VCCD_23	H14
VCCD_23	H16
VCCD_23	H18
VCCD_23	H20
VCCD_23	H22
VCCD_23	N11
VCCD_23	N13
VCCD_23	N15
VCCD_23	N17
VCCD_23	N19
VCCD_23	N21
VCCD_23	V14
VCCD_23	V16
VCCD_23	V18

Table 6-1. **Processor Land List**

Land Name	Land Number
VCCD_23	V20
VCCD_23	V22
VCCIN	CE41
VCCIN	AF42
VCCIN	AG23
VCCIN	AG27
VCCIN	AG29
VCCIN	AG33
VCCIN	AG35
VCCIN	AG39
VCCIN	AG41
VCCIN	AH42
VCCIN	AL17
VCCIN	AM42
VCCIN	AN11
VCCIN	AN17
VCCIN	AP10
VCCIN	AP12
VCCIN	AP14
VCCIN	AP16
VCCIN	AP2
VCCIN	AP4
VCCIN	AP6
VCCIN	AP8
VCCIN	AR1
VCCIN	AR11
VCCIN	AR13
VCCIN	AR15
VCCIN	AR17
VCCIN	AR3
VCCIN	AR5
VCCIN	AR7
VCCIN	AR9
VCCIN	AT10
VCCIN	AT12
VCCIN	AT14
VCCIN	AT16
VCCIN	AT2
VCCIN	AT4

Table 6-1. **Processor Land List**

Land Name	Land Number
VCCIN	AT42
VCCIN	AT6
VCCIN	AT8
VCCIN	AU1
VCCIN	AU11
VCCIN	AU13
VCCIN	AU15
VCCIN	AU17
VCCIN	AU3
VCCIN	AU5
VCCIN	AU7
VCCIN	AU9
VCCIN	AV10
VCCIN	AV12
VCCIN	AV14
VCCIN	AV16
VCCIN	AV2
VCCIN	AV4
VCCIN	AV6
VCCIN	AV8
VCCIN	AW1
VCCIN	AY42
VCCIN	BA1
VCCIN	BA11
VCCIN	BA13
VCCIN	BA15
VCCIN	BA17
VCCIN	BA3
VCCIN	BA5
VCCIN	BA7
VCCIN	BA9
VCCIN	BB10
VCCIN	BB12
VCCIN	BB14
VCCIN	BB16
VCCIN	BB2
VCCIN	BB4
VCCIN	BB6
VCCIN	BB8

Table 6-1. Processor Land List

Land Name	Land Number
VCCIN	BC1
VCCIN	BC11
VCCIN	BC13
VCCIN	BC15
VCCIN	BC17
VCCIN	BC3
VCCIN	BC5
VCCIN	BC7
VCCIN	BC9
VCCIN	BD10
VCCIN	BD12
VCCIN	BD14
VCCIN	BD16
VCCIN	BD2
VCCIN	BD4
VCCIN	BD42
VCCIN	BD6
VCCIN	BD8
VCCIN	BE1
VCCIN	BE11
VCCIN	BE13
VCCIN	BE15
VCCIN	BE17
VCCIN	BE3
VCCIN	BE5
VCCIN	BE7
VCCIN	BE9
VCCIN	BG1
VCCIN	BH10
VCCIN	BH12
VCCIN	BH14
VCCIN	BH16
VCCIN	BH2
VCCIN	BH4
VCCIN	BH42
VCCIN	BH6
VCCIN	BH8
VCCIN	BJ1
VCCIN	BJ11

Table 6-1. Processor Land List

Land Name	Land Number
VCCIN	BJ13
VCCIN	BJ15
VCCIN	BJ17
VCCIN	BJ3
VCCIN	BJ5
VCCIN	BJ7
VCCIN	BJ9
VCCIN	BK10
VCCIN	BK12
VCCIN	BK14
VCCIN	BK16
VCCIN	BK2
VCCIN	BK4
VCCIN	BK6
VCCIN	BK8
VCCIN	BL1
VCCIN	BL11
VCCIN	BL13
VCCIN	BL15
VCCIN	BL17
VCCIN	BL3
VCCIN	BL5
VCCIN	BL7
VCCIN	BL9
VCCIN	BM10
VCCIN	BM12
VCCIN	BM14
VCCIN	BM16
VCCIN	BM2
VCCIN	BM4
VCCIN	BM42
VCCIN	BM6
VCCIN	BM8
VCCIN	BN11
VCCIN	BN13
VCCIN	BN15
VCCIN	BN17
VCCIN	BN3
VCCIN	BN5

Table 6-1. Processor Land List

Land Name	Land Number
VCCIN	BN7
VCCIN	BN9
VCCIN	BP10
VCCIN	BP16
VCCIN	BP42
VCCIN	BR17
VCCIN	BU17
VCCIN	BV42
VCCIN	BY18
VCCIN	BY20
VCCIN	BY22
VCCIN	BY24
VCCIN	BY26
VCCIN	BY30
VCCIN	BY34
VCCIN	BY36
VCCIN	BY38
VCCIN	BY40
VCCIN	BY42
VCCIN_SENSE	BN1
VCCIO_IN	CC41
VCCPECI	CD42
VSS	A23
VSS	A37
VSS	A39
VSS	A41
VSS	A43
VSS	A45
VSS	A47
VSS	A49
VSS	A5
VSS	A51
VSS	A7
VSS	AA25
VSS	AA29
VSS	AA3
VSS	AA31
VSS	AA39
VSS	AA55

Table 6-1. Processor Land List

Land Name	Land Number
VSS	AA7
VSS	AB12
VSS	AB36
VSS	AB40
VSS	AB42
VSS	AC11
VSS	AC29
VSS	AC7
VSS	AC9
VSS	AD10
VSS	AD12
VSS	AD36
VSS	AD4
VSS	AD40
VSS	AD42
VSS	AD44
VSS	AD46
VSS	AD48
VSS	AD50
VSS	AD52
VSS	AD6
VSS	AD8
VSS	AE13
VSS	AE15
VSS	AE19
VSS	AE23
VSS	AE27
VSS	AE29
VSS	AE33
VSS	AE35
VSS	AE39
VSS	AE41
VSS	AE43
VSS	AE47
VSS	AE49
VSS	AE51
VSS	AE53
VSS	AF10
VSS	AF16

Table 6-1. Processor Land List

Land Name	Land Number
VSS	AF18
VSS	AF2
VSS	AF20
VSS	AF22
VSS	AF24
VSS	AF26
VSS	AF28
VSS	AF30
VSS	AF32
VSS	AF34
VSS	AF36
VSS	AF38
VSS	AF4
VSS	AF40
VSS	AF54
VSS	AF56
VSS	AF6
VSS	AF8
VSS	AG11
VSS	AG13
VSS	AG17
VSS	AG19
VSS	AG21
VSS	AG25
VSS	AG31
VSS	AG37
VSS	AG43
VSS	AG55
VSS	AG57
VSS	AH14
VSS	AH2
VSS	AH58
VSS	AH6
VSS	AJ11
VSS	AJ17
VSS	AK16
VSS	AK4
VSS	AK42
VSS	AK44

Table 6-1. Processor Land List

Land Name	Land Number
VSS	AK46
VSS	AK48
VSS	AK50
VSS	AK52
VSS	AK6
VSS	AL11
VSS	AL43
VSS	AL45
VSS	AL47
VSS	AL49
VSS	AL51
VSS	AL53
VSS	AM10
VSS	AM12
VSS	AM14
VSS	AM16
VSS	AM2
VSS	AM4
VSS	AM56
VSS	AM6
VSS	AM8
VSS	AN1
VSS	AN13
VSS	AN15
VSS	AN3
VSS	AN5
VSS	AN55
VSS	AN57
VSS	AN7
VSS	AN9
VSS	AP42
VSS	AP44
VSS	AP58
VSS	AT44
VSS	AT46
VSS	AT48
VSS	AT50
VSS	AT52
VSS	AU45

Table 6-1.   Processor Land List

Land Name	Land Number
VSS	AU47
VSS	AU49
VSS	AU51
VSS	AU53
VSS	AV42
VSS	AV54
VSS	AV56
VSS	AW11
VSS	AW13
VSS	AW15
VSS	AW17
VSS	AW3
VSS	AW5
VSS	AW55
VSS	AW57
VSS	AW7
VSS	AW9
VSS	AY10
VSS	AY12
VSS	AY14
VSS	AY16
VSS	AY2
VSS	AY4
VSS	AY44
VSS	AY6
VSS	AY8
VSS	B10
VSS	B36
VSS	B40
VSS	B52
VSS	B6
VSS	BB42
VSS	BB46
VSS	BB50
VSS	BB58
VSS	BC45
VSS	BC47
VSS	BC49
VSS	BC51

Table 6-1.   Processor Land List

Land Name	Land Number
VSS	BC53
VSS	BC55
VSS	BC57
VSS	BD52
VSS	BD54
VSS	BD56
VSS	BE49
VSS	BE51
VSS	BF10
VSS	BF12
VSS	BF14
VSS	BF16
VSS	BF2
VSS	BF4
VSS	BF42
VSS	BF6
VSS	BF8
VSS	BG11
VSS	BG13
VSS	BG15
VSS	BG17
VSS	BG3
VSS	BG45
VSS	BG47
VSS	BG5
VSS	BG7
VSS	BG9
VSS	BH58
VSS	BJ55
VSS	BJ57
VSS	BK42
VSS	BK46
VSS	BK48
VSS	BK50
VSS	BK52
VSS	BK54
VSS	BL45
VSS	BL49
VSS	BL57

Table 6-1.   Processor Land List

Land Name	Land Number
VSS	BN43
VSS	BN57
VSS	BP12
VSS	BP14
VSS	BP4
VSS	BP58
VSS	BP6
VSS	BP8
VSS	BR1
VSS	BR11
VSS	BR13
VSS	BR15
VSS	BR3
VSS	BR5
VSS	BR53
VSS	BR55
VSS	BR57
VSS	BR7
VSS	BR9
VSS	BT10
VSS	BT16
VSS	BT42
VSS	BT46
VSS	BT48
VSS	BT50
VSS	BT52
VSS	BT54
VSS	BT56
VSS	BU3
VSS	BU45
VSS	BU47
VSS	BU5
VSS	BU51
VSS	BV10
VSS	BV16
VSS	BW15
VSS	BW17
VSS	BW43
VSS	BW5

Table 6-1.   Processor Land List

Land Name	Land Number
VSS	BW7
VSS	BY10
VSS	BY28
VSS	BY32
VSS	BY58
VSS	BY8
VSS	C33
VSS	C5
VSS	C55
VSS	CA13
VSS	CA15
VSS	CA17
VSS	CA19
VSS	CA21
VSS	CA23
VSS	CA25
VSS	CA27
VSS	CA29
VSS	CA31
VSS	CA33
VSS	CA35
VSS	CA37
VSS	CA39
VSS	CA41
VSS	CA5
VSS	CA55
VSS	CA57
VSS	CB10
VSS	CB12
VSS	CB14
VSS	CB2
VSS	CB30
VSS	CB34
VSS	CB36
VSS	CB38
VSS	CB40
VSS	CB42
VSS	CB44
VSS	CB46

Table 6-1.   Processor Land List

Land Name	Land Number
VSS	CB48
VSS	CB50
VSS	CB52
VSS	CB54
VSS	CB56
VSS	CC11
VSS	CC3
VSS	CC33
VSS	CC43
VSS	CC45
VSS	CC47
VSS	CC49
VSS	CC5
VSS	CC7
VSS	CC9
VSS	CD12
VSS	CD4
VSS	CD40
VSS	CD6
VSS	CD8
VSS	CE15
VSS	CE33
VSS	CE43
VSS	CE45
VSS	CE7
VSS	CF10
VSS	CF12
VSS	CF28
VSS	CF32
VSS	CG27
VSS	CG29
VSS	CG31
VSS	CG33
VSS	CG35
VSS	CG37
VSS	CG39
VSS	CG43
VSS	CG45
VSS	CG5

Table 6-1.   Processor Land List

Land Name	Land Number
VSS	CG53
VSS	CG7
VSS	CH12
VSS	CH30
VSS	CH34
VSS	CH36
VSS	CH38
VSS	CH40
VSS	CH42
VSS	CH44
VSS	CH46
VSS	CH48
VSS	CH50
VSS	CH52
VSS	CH54
VSS	CH56
VSS	CJ15
VSS	CJ3
VSS	CJ33
VSS	CJ41
VSS	CJ43
VSS	CJ45
VSS	CJ47
VSS	CJ49
VSS	CJ51
VSS	CJ7
VSS	CK12
VSS	CK4
VSS	CK40
VSS	CK52
VSS	CK54
VSS	CL11
VSS	CL15
VSS	CL7
VSS	CL9
VSS	CM10
VSS	CM28
VSS	CM32
VSS	CM40

Table 6-1.   Processor Land List

Land Name	Land Number
VSS	CM52
VSS	CM54
VSS	CM6
VSS	CM8
VSS	CN11
VSS	CN13
VSS	CN27
VSS	CN29
VSS	CN3
VSS	CN31
VSS	CN33
VSS	CN35
VSS	CN37
VSS	CN39
VSS	CN5
VSS	CN53
VSS	CN55
VSS	CN57
VSS	CN7
VSS	CP12
VSS	CP14
VSS	CP30
VSS	CP34
VSS	CP36
VSS	CP38
VSS	CP4
VSS	CP42
VSS	CP44
VSS	CP46
VSS	CP48
VSS	CP50
VSS	CP56
VSS	CR33
VSS	CR41
VSS	CR45
VSS	CR47
VSS	CR49
VSS	CR7
VSS	CR9

Table 6-1.   Processor Land List

Land Name	Land Number
VSS	CT12
VSS	CT2
VSS	CT40
VSS	CU1
VSS	CU15
VSS	CU33
VSS	CU7
VSS	CV12
VSS	CV28
VSS	CV32
VSS	CV40
VSS	CV54
VSS	CV58
VSS	CV6
VSS	CW1
VSS	CW15
VSS	CW27
VSS	CW29
VSS	CW31
VSS	CW33
VSS	CW35
VSS	CW37
VSS	CW39
VSS	CW5
VSS	CW53
VSS	CW55
VSS	CW57
VSS	CW7
VSS	CY10
VSS	CY12
VSS	CY2
VSS	CY30
VSS	CY34
VSS	CY36
VSS	CY38
VSS	CY4
VSS	CY42
VSS	CY44
VSS	CY46

Table 6-1.   Processor Land List

Land Name	Land Number
VSS	CY48
VSS	CY50
VSS	CY52
VSS	CY8
VSS	D10
VSS	D24
VSS	D36
VSS	D4
VSS	D40
VSS	DA27
VSS	DA3
VSS	DA35
VSS	DA41
VSS	DA43
VSS	DA45
VSS	DA47
VSS	DA49
VSS	DA51
VSS	DA53
VSS	DA55
VSS	DA9
VSS	DB12
VSS	DB34
VSS	DB40
VSS	DB58
VSS	DB6
VSS	DC5
VSS	DC53
VSS	DC55
VSS	DD10
VSS	DD12
VSS	DD34
VSS	DD38
VSS	DD40
VSS	DD6
VSS	DE15
VSS	DE35
VSS	DE7
VSS	DF12

Table 6-1. Processor Land List

Land Name	Land Number
VSS	DF40
VSS	DF42
VSS	DF44
VSS	DF46
VSS	DF48
VSS	DF50
VSS	DF52
VSS	DF8
VSS	E1
VSS	E3
VSS	E39
VSS	E41
VSS	F2
VSS	F30
VSS	F32
VSS	F36
VSS	F4
VSS	F42
VSS	F44
VSS	F48
VSS	F50
VSS	G1
VSS	G23
VSS	G27
VSS	G33
VSS	G35
VSS	G39
VSS	G41
VSS	G45
VSS	G47
VSS	G49
VSS	G5
VSS	G51
VSS	G53
VSS	G57
VSS	G9
VSS	H24
VSS	H26
VSS	H28

Table 6-1. Processor Land List

Land Name	Land Number
VSS	H30
VSS	H32
VSS	H34
VSS	H36
VSS	H40
VSS	H54
VSS	H6
VSS	H8
VSS	J25
VSS	J29
VSS	J3
VSS	J31
VSS	J37
VSS	J5
VSS	J55
VSS	J7
VSS	K10
VSS	K36
VSS	K40
VSS	L29
VSS	L39
VSS	L41
VSS	L5
VSS	M10
VSS	M2
VSS	M36
VSS	M42
VSS	M44
VSS	M46
VSS	M48
VSS	M50
VSS	M52
VSS	N23
VSS	N27
VSS	N29
VSS	N33
VSS	N35
VSS	N37
VSS	N39

Table 6-1. Processor Land List

Land Name	Land Number
VSS	N43
VSS	N45
VSS	N47
VSS	N49
VSS	N5
VSS	N51
VSS	N53
VSS	P10
VSS	P24
VSS	P26
VSS	P28
VSS	P30
VSS	P32
VSS	P34
VSS	P38
VSS	P40
VSS	P54
VSS	P56
VSS	R11
VSS	R25
VSS	R29
VSS	R31
VSS	R39
VSS	R5
VSS	R55
VSS	R9
VSS	T36
VSS	T4
VSS	T42
VSS	T6
VSS	T8
VSS	U29
VSS	U3
VSS	U39
VSS	U41
VSS	U43
VSS	U7
VSS	V10
VSS	V12

Table 6-1. **Processor Land List**

Land Name	Land Number
VSS	V36
VSS	V44
VSS	V46
VSS	V48
VSS	V50
VSS	V52
VSS	W23
VSS	W27
VSS	W33
VSS	W35
VSS	W39
VSS	W43
VSS	W45
VSS	W47
VSS	W49
VSS	W51
VSS	W53
VSS	W7
VSS	Y12
VSS	Y24
VSS	Y26
VSS	Y28
VSS	Y30
VSS	Y32
VSS	Y34
VSS	Y36
VSS	Y4
VSS	Y42
VSS	Y56
VSS_VCCIN_SENSE	BP2

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