Design Simulation Activity

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Course: EN1014 Electronic Engineering

(a) Simulated Results: Input V vs Output V

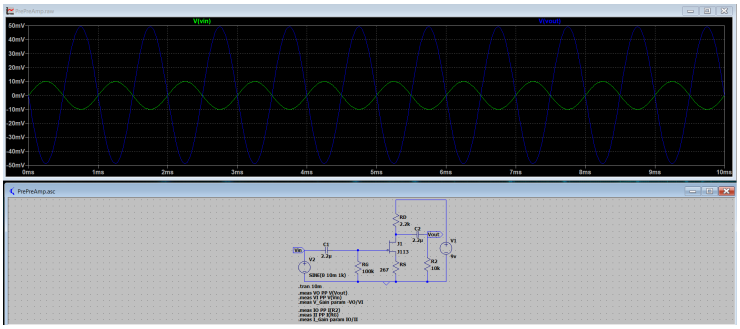

Figure 1: Simulated input and output waveforms with JFET circuit

Drawbacks

- The source resistor R_S introduces **negative feedback** to the input side. This reduces the gate-source voltage V_{GS}, thereby lowering the voltage gain.
- The quiescent point (Q-point) is not positioned at the center of the DC load line. As a result, when the input signal amplitude increases, the output waveform clips on the negative half-cycle.

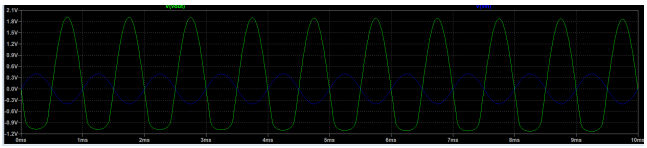

Figure 2: Output waveform showing negative half-cycle clipping

(b) Design Improvements

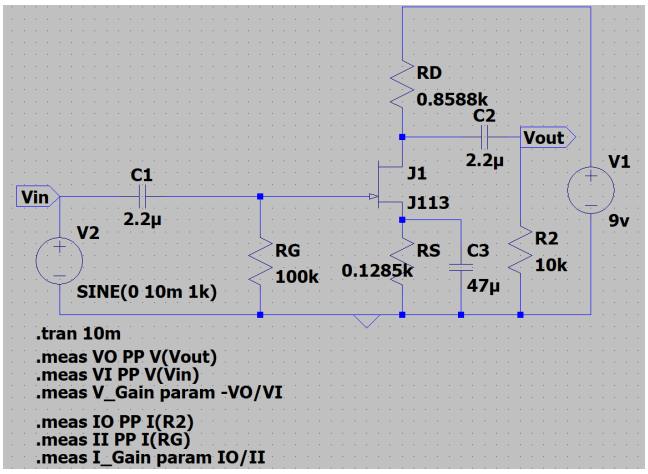

Figure 3: After design improvents

Q point

To center the Q-point on the DC load line, the drain current was chosen as:

$$I_D = \frac{I_{DSS}}{2} = \frac{9.116\,\text{mA}}{2} = 4.558\,\text{mA}$$

The corresponding gate-source voltage was calculated as:

$$V_{GS} = -0.5858\,\text{V}$$

Using Ohm's law, the resistor values were calculated as:

$$R_S = \frac{|V_{GS}|}{I_D} = \frac{0.5858}{4.558} \approx 0.1285\,\text{k}\Omega$$

$$R_D = \frac{V_{DD} - V_{DS(Q)}}{I_D} = \frac{9 - 4.5}{4.558} \approx 0.8588\,\text{k}\Omega$$

These resistor values reposition the Q-point to the center of the DC load line, allowing for maximum undistorted signal swing and improved amplifier performance.

Bypass capacitor

To increase the AC gain of the amplifier, a bypass capacitor was placed in parallel with the source resistor R_S. This capacitor effectively removes the negative feedback for AC signals while preserving the DC biasing condition.

The condition for proper bypassing is:

$$\frac{1}{2\pi f C} \ll R_S$$

Where:

- f is the lowest frequency of interest (guitar low E string: $f = 82.4\,\text{Hz}$),
- C is the capacitance of the bypass capacitor,
- $R_S = 0.1285\,\text{k}\Omega = 128.5\,\Omega$.

We choose:

$$C = 47\,\mu\text{F}$$

Calculating the capacitive reactance:

$$X_C = \frac{1}{2\pi f C} = \frac{1}{2\pi \cdot 82.4 \cdot 47 \times 10^{-6}} \approx 40.9\,\Omega$$

Now comparing:

$$X_C = 40.9\,\Omega < R_S = 128.5\,\Omega$$

This shows that the capacitor's impedance is significantly lower than R_S, satisfying the bypass condition for frequencies above 82.4Hz.

Conclusion: A 47μF capacitor effectively bypasses R_S for the frequency range of a guitar signal. It reduces AC negative feedback and increases the amplifier's gain while maintaining proper DC biasing.

Input Coupling Capacitor

The input coupling capacitor, together with the gate resistor R_G, forms a high-pass RC filter. This filter blocks DC components from the input signal and allows AC signals (i.e., the guitar signal) to pass.

The cutoff frequency f_c of a high-pass RC filter is given by:

$$f_c = \frac{1}{2\pi R_G C}$$

Where I Choose:

- $R_G = 100\,\text{k}\Omega$
- $C = 2.2\,\mu\text{F}$

Substituting the values:

$$f_c = \frac{1}{2\pi \cdot 100 \times 10^3 \cdot 2.2 \times 10^{-6}} \approx 0.724\,\text{Hz}$$

Conclusion: The cutoff frequency is approximately 0.724 Hz, which is well below the lowest frequency produced by a guitar (82.4 Hz). Therefore, the high-pass filter formed by the input capacitor and gate resistor will allow all guitar frequencies to pass through with minimal attenuation.

(c) Gain Calculations After Design Improvements

```
vo: PP(V(Vout))=0.211159497499 FROM 0 TO 0.01
vi: PP(V(Vin))=0.0199996996671 FROM 0 TO 0.01
v_gain: -VO/VI=-10.5581334227
io: PP(I(R2))=2.11159485843e-05 FROM 0 TO 0.01
ii: PP(I(RG))=1.99993174022e-07 FROM 0 TO 0.01
i_gain: IO/II=105.58334647
```

Figure 4: Gain Calculations After Design Improvements

After implementing the proposed design changes, the amplifier was simulated, and the following measurements were taken:

$$\begin{aligned} V_{\text{out(pp)}} &= 0.2112\,\text{V} \\ V_{\text{in(pp)}} &= 0.0200\,\text{V} \\ I_{\text{out(pp)}} &= 2.1116 \times 10^{-5}\,\text{A} \\ I_{\text{in(pp)}} &= 1.9993 \times 10^{-7}\,\text{A} \end{aligned}$$

Voltage Gain

$$A_V = \frac{V_{\text{out(pp)}}}{V_{\text{in(pp)}}} = \frac{-0.2112}{0.0200} = -10.56$$

Current Gain

$$A_I = \frac{I_{\text{out(pp)}}}{I_{\text{in(pp)}}} = \frac{2.1116 \times 10^{-5}}{1.9993 \times 10^{-7}} \approx 105.58$$

Power Gain

$$A_P = A_V \times A_I = 10.56 \times 105.58 \approx 1113.5$$

Conclusion: The amplifier provides a voltage gain of approximately 10.56, a current gain of 105.58, and a power gain of about 1113.5, indicating substantial signal amplification across all domains.

(e) Need for a Power Amplifier After the Preamplifier

The JFET preamplifier is designed primarily to amplify weak input signals, such as those from a musical instrument, to a usable voltage level. However, it does not provide sufficient current or power to drive low-impedance loads such as speakers or headphones.

A **power amplifier** is therefore connected in cascade after the preamplifier for the following reasons:

- **Current and Power Drive:** The preamplifier has high voltage gain but limited current driving capability. Power amplifiers are designed to deliver large amounts of current and power to drive low-impedance loads (e.g., $8\,\Omega$ speakers).
- **Impedance Matching:** Power amplifiers have low output impedance, allowing efficient power transfer to the load, whereas preamplifiers typically have high output impedance.
- **Load Isolation:** A power amplifier isolates the preamplifier from the effects of varying load conditions, ensuring stable operation and signal integrity.
- **Final Signal Boost:** The power amplifier provides the final amplification stage required to bring the signal up to a level suitable for audible output through a speaker system.

Conclusion: While the preamplifier conditions and amplifies the input signal voltage, the power amplifier ensures that the signal has sufficient power to effectively drive the intended output load.