UNIVERSITY OF MORATUWA
Faculty of Engineering
Department of Electronic and Telecommunication Engineering
B.Sc.Engineering
Semester 2 (2018 Batch) Examination

EN1013 ELECTRONICS I

Time allowed: *Two (2)* hours February 2020

INSTRUCTIONS TO CANDIDATES:

- This paper contains 4 questions on 7 pages.
- Answer **all** questions.
- This paper contains **two** sections. Use a **separate** answer book for each section.
- All questions carry **equal** marks.
- This examination accounts for **70**% of the module assessment. The total maximum mark attainable is **100**. The marks assigned for each question & sections thereof are indicated in square brackets.
- The symbols used in this paper have their usual meanings.
- This is a closed book examination.
- Electronic/communication devices are not permitted. Only equipment allowed is a calculator approved and labeled by the Faculty of Engineering.
- Derivations are not required if they are not explicitly requested in the question.
- Assume reasonable values for any data not given in or with the examination paper. Clearly state such assumptions.
- If you have any doubt as to the interpretation of the wording of a question, make your own decision, and clearly state it.

ADDITIONAL MATERIAL:

- No additional material is provided.

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SECTION A

Question 1.

(a) Draw the energy band diagram of a *pn* junction at equilibrium state. [3 marks]

(b) Explain why the majority carriers will not continue to cross the *pn* junction until the energy levels of the two sides equalize. [3 marks]

(c) Define the dynamic resistance of a diode. [2 marks]

(d) Prove that the dynamic resistance of a forward-biased diode is inversely proportional to the forward DC current flowing through it. [3 marks]

(e) A diode conducts a forward current of 10 mA when a 5 V battery is connected through a 1 kΩ resister to forward bias it. In this instance, the forward voltage measured across the diode is 0.72 V.

i. Calculate the values of *DC* resistance and *dynamic* resistance of the diode. [2 marks]

ii. Derive the equation of the DC load line. Sketch it and mark the operating point. [3 marks]

iii. If an additional AC source of $2\sin(\omega t)$ V is connected in series with the battery in the above circuit, find the new voltage across the diode. [5 marks]

(f) Compare and contrast between the bipolar junction transistor (BJT) and the field effect transistor (FET). Give your answer in tabulated format. [4 marks]

Question 2.

A simple fixed-biased small signal amplifier made of the following electronic components produce an output signal of 4 V (peak to peak) across the collector load resistance when the input signal source provides a base current variation of 20 μA (peak to peak).

A 12V DC supply

An input signal source

A 2.2 μF coupling capacitor

BC547 BJT having a DC current gain (β_{DC}) of 325 and R_i of 1 kΩ

A Collector load having 820 Ω resistance

A variable resistor with variation ranging from 200 kΩ to 2 MΩ

(a) Sketch the circuit diagram of the amplifier. Properly label all circuit components, voltages and currents. [3 marks]

(b) Find the required bias resistance to set the DC base bias current to 22.6 mA. [2 marks]

(c) Find the quiescent collector current and voltage. [2 marks]

(d) Derive the equation of the DC load line. [2 marks]

(e) Sketch the DC load line. Mark the quiescent point on it and comment on its location on the DC load line. [2 marks]

(f) Using the equation of the DC load line, find the peak to peak variation of the collector current. [2 marks]

(g) Find the AC signal power delivered to the load. [2 marks]

(h) Find the DC power dissipation in the load. [2 marks]

(i) Mark all relevant points on the DC load line and graphically illustrate the operation of the circuit using appropriate waveforms on the graph. Clearly label the axes and the waveforms. [2 marks]

(j) Find the voltage gain, current gain and the power gain of the circuit. [3 marks]

(k) In what scenario you should not use the DC load line for gain calculations of an amplifier. Briefly explain the method used for gain calculations in such cases. [3 marks]

SECTION B

Question 3.

(a) Consider the following 5-variable Boolean function;

$$f(a,b,c,d,e) = \prod(2,5,7,10,13,15,16,24,31) \cdot D(0,1,18,23,26,30),$$

where $D(\cdot)$ denotes don't care maxterms.

i. Draw the corresponding 4-variable Karnaugh maps for the two cases: $a = 0$ and $a = 1$. [4 marks]

ii. Hence, express the Boolean function f in the *product-of-sums* form with a minimal number of literals. [9 marks]

(b) A two-bit magnitude comparator compares the magnitude of two 2-bit binary numbers A and B. The 2-bit magnitude comparator has four inputs A_1, A_0, B_1 and B_0, and three outputs X, Y and Z. Here, A_1, A_0, B_1 and B_0 are the bits of A and B, that is, $A = A_1A_0$ and $B = B_1B_0$. Furthermore, the outputs X, Y and Z indicate $A > B$, $A = B$ and $A < B$, respectively.

i. Express the truth table corresponding to the 2-bit magnitude comparator. [3 marks]

ii. Derive the simplified Boolean expressions, in the *sum-of-products* form with a minimal number of literals, for the outputs X, Y and Z. [6 marks]

iii. Draw the realization of the digital circuit of X using only 2-input and 3-input NAND gates. [3 marks]

Question 4.

(a) Consider the design of a full adder of which the inputs are X, Y and C_{i-1} and the outputs are S and C_i. Here, X and Y denote the two bits to be added, and C_{i-1} denotes the carry from the previous full adder. Further, S and C_i denote the sum and carry of the full adder, respectively.

i. Express the truth table corresponding to the full adder. [2 marks]

ii. Draw the realization of the full adder using two 2-to-4-line decoders with *active-high* enable inputs, and NOT and OR gates. Clearly indicate all the inputs and outputs of the 2-to-4-line decoders. [5 marks]

(b) The parameters of a 2-input transistor-transistor logic (TTL) NAND gate is presented in Table Q4. Calculate the following specifications of the 2-input TTL NAND gate using the values given in Table Q4.

i. Fan-out [2 marks]

ii. Propagation delay [2 marks]

iii. Power dissipation [2 marks]

iv. Noise margin [2 marks]

Table Q4

Parameter	Description	Value
V_{CC}	Supply voltage	5 V
I_{CCH}	High-level supply current	2 mA
I_{CCL}	Low-level supply current	4 mA
V_{OH}	High-level output voltage (min)	2.8 V
V_{OL}	Low-level output voltage (max)	0.5 V
V_{IH}	High-level input voltage (min)	2 V
V_{IL}	Low-level input voltage (max)	0.8 V
I_{OH}	High-level output current (max)	1 mA
I_{OL}	Low-level output current (max)	20 mA
I_{IH}	High-level input current (max)	0.05 mA
I_{IL}	Low-level input current (max)	2 mA
t_{PLH}	Low-to-high delay	12 ns
t_{PHL}	High-to-low delay	8 ns

(c) A 2-input NAND gate of the diode-transistor logic (DTL) family is shown in Figure Q4. The transistor $Q1$ and all the diodes are made of Si, and h_{FE} (β_{DC}) of the transistor $Q1$ is 20. Consider the case where the output Y of this logic gate is connected to N similar logic gates, and the transistor $Q1$ is *saturated*. Further, assume that I_B of the transistor $Q1$ is 0.45 mA.

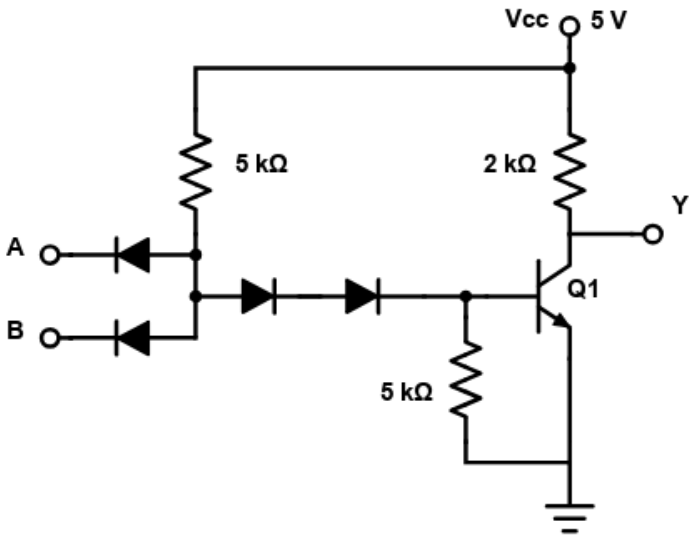

Figure Q4

i. Calculate the total collector current I_C of the transistor $Q1$ as a function of N. [6 marks]

ii. Find the highest value of N that will keep the transistor $Q1$ in saturation. [4 marks]

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