UNIVERSITY OF MORATUWA
Faculty of Engineering
Department of Electronic and Telecommunication Engineering
B.Sc. Engineering
Semester 2 (2020 Batch) Examination

EN1014 ELECTRONIC ENGINEERING

Time allowed: *Three (3)* hours September 2022

INSTRUCTIONS TO CANDIDATES:

- This paper contains 5 questions on 6 pages.
- Answer **all** questions.
- This paper contains **two** sections. Use a **separate** answer book for each section.
- All questions carry **equal** marks.
- This examination accounts for **60%** of the module assessment. The total maximum mark attainable is **100**. The marks assigned for each question & sections thereof are indicated in square brackets.
- The symbols used in this paper have their usual meanings.
- This is a **closed-book** examination.
- Electronic/communication devices are not permitted. Only equipment allowed is a calculator approved and labeled by the Faculty of Engineering.
- Derivations are not required if they are not explicitly requested in the question.
- Assume reasonable values for any data not given in or with the examination paper. Clearly state such assumptions.
- If you have any doubt as to the interpretation of the wording of a question, make your own decision, and clearly state it.

ADDITIONAL MATERIAL:

- No additional material is provided.

SECTION A

Question 1.

(a) i. What is meant by a model? [2 marks]

ii. Differentiate between lumped element abstraction and lumped module abstraction. [2 marks]

iii. Illustrate module level abstraction of a rechargeable multi-speed hair dryer with a built-in battery and a battery charger. Assume that the concept of central control has been employed in the design. [5 marks]

(b) A speech signal from a microphone is applied as V_i to the circuit given in Figure Q1.

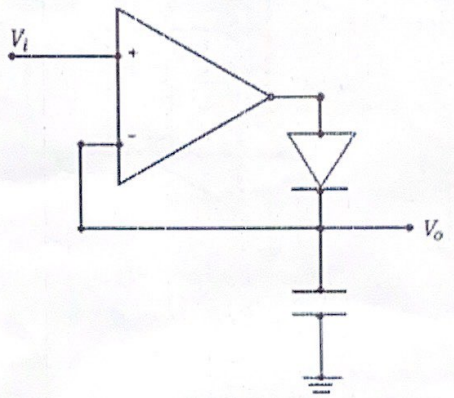

Figure Q1

i. Explain the output signal V_o. [2 marks]

ii. Identify a practical use of the circuit. [2 marks]

(c) i. What are the special requirements of an instrumentation amplifier? [1 mark]

ii. Explain with derivations how you would modify a unity gain differential amplifier to achieve the special requirements identified in c(i). [6 marks]

Question 2.

(a) If $v_1(t)$ and $v_2(t)$ voltage waveforms are available from two sensors, show how you would obtain the following output voltage waveform using operational amplifies. [4 marks]

$$v_o(t) = k \int [v_1(t) + v_2(t)]\, dt$$

(b) In the circuit shown in Figure Q2(a), the input source produces a sinusoidal waveform of 2 V amplitude.

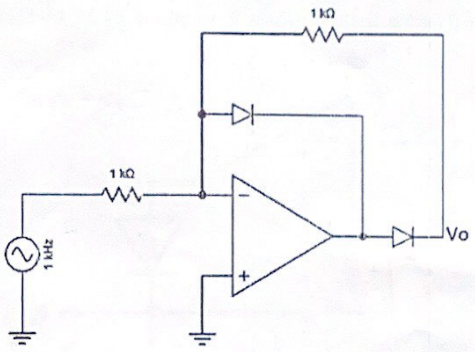

Figure Q2(a)

i. Sketch the output waveform. [6 marks]
(*Hint*: Only one diode will be conducting at a time.)

ii. Identify the function of the circuit. [1 mark]

iii. What is the effect of the forward voltage drop of the diodes on the output waveform? [2 marks]

(c) In the circuit shown in Figure Q2(b), the Zener diode has the specifications $V_Z = 15$ V, $I_{ZK} = 2$ mA, $Z_Z = 0$ and 750 mW max power dissipation. If the input voltage is 35 V $\pm$ 6 V, find out the range of the load resistance that can be accommodated by this regulator while maintaining the voltage regulation. [7 marks]

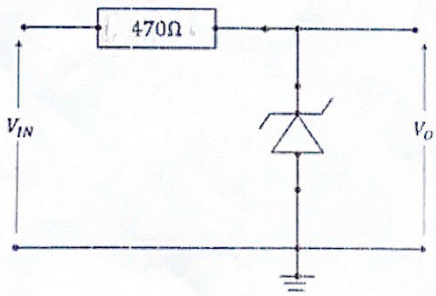

Figure Q2(b)

Question 3.

The amplifier shown in Figure Q3 has following component values. $R_1 = 4$ MΩ, $R_2 = 1$ kΩ, $R_3 = 200$ Ω, $C_1 = 2.2$ μF, $C_2 = 4$ μF, and for the JFET, pinch-off voltage $= -4$ V, Drain-Source Saturation current $= 10$ mA.

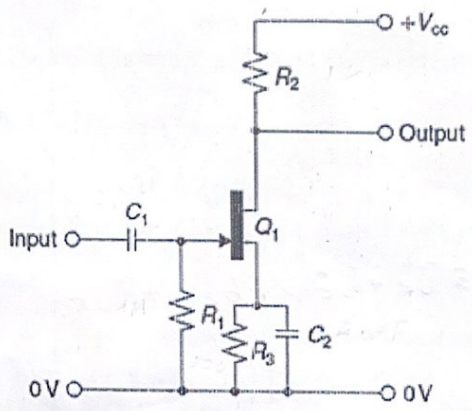

Figure Q3

(a) Find out the quiescent Gate-Source voltage ($V_{GS,Q}$) [6 marks]

(b) Find out the quiescent Channel current ($I_{D,Q}$) [2 marks]

(c) Derive the equation of the DC load line. [2 marks]

(d) If the quiescent Drain-Source voltage ($V_{DS,Q}$) should be exactly 50% of the power supply voltage (V_{CC}), what should be the power supply voltage (V_{CC})? [2 marks]

(e) Sketch the DC load line and mark the co-ordinates of the Q-point. [1 mark]

(f) Derive the equation of the AC load line and sketch the AC load line. [3 marks]

(g) If an AC signal power of 1.125 mW should be delivered to the load, calculate the coordinates of the two points (A and B) on the DC load line between which the operating point will be oscillating around the Q point. [4 marks]

SECTION B

Question 4.

(a) Consider the following 5-variable Boolean function

$$f(a,b,c,d,e) = \sum(1,3,5,7,10,17,19,26,30,31) + d(2,8,14,15,18,20,25),$$

where $d(\cdot)$ denotes don't care minterms.

i. Draw the corresponding 4-variable Karnaugh maps for the two cases: $a = 0$ and $a = 1$. [3 marks]

ii. Hence, express the Boolean function f in the *sum-of-products* form with a minimal number of literals. [7 marks]

iii. Draw the realization of the digital circuit corresponding to the simplified Boolean function f using a minimal number of 2-input and 3-input NAND gates. [3 marks]

(b) Consider the Boolean function f defined as

$$f(a,b,c,d) = \prod(0,2,4,6,7,12) \cdot D(9,11),$$

where $D(\cdot)$ denotes don't care maxterms. The Boolean function f is required to be implemented using *only two* 4×1 multiplexers with *active-high* enable inputs, *one* NOT gate, and *one* 2-input OR gate.

i. Construct the truth table by selecting the binary variable d as the input to the multiplexers. [3 marks]

ii. Draw the realization of the digital circuit corresponding to f. Clearly indicate all the inputs and the outputs of the multiplexers and the decoder. [4 marks]

Question 5.

(a) Draw the logic circuit of a D latch with an enable input, and state its function table. [3 marks]

(b) Consider the design of a sequential logic circuit (having one input and one output) that can detect 1101 bit stream including *overlaps*. This circuit is designed as a Mealy machine and is implemented using D flip-flops.

i. Draw the corresponding state diagram. [6 marks]

ii. Obtain the binary-coded state table. [3 marks]

iii. Based on the excitation table of a D flip-flop, derive the simplified Boolean expressions for the flip-flop input equations. [4 marks]

iv. Derive the simplified Boolean expression for the output equation. [1 mark]

v. Draw the realization of the sequential logic circuit using D flip-flops, 2-input and 3-input AND gates and OR gates, and NOT gates. [3 marks]

- End of Question Paper -