FET Biasing Methods

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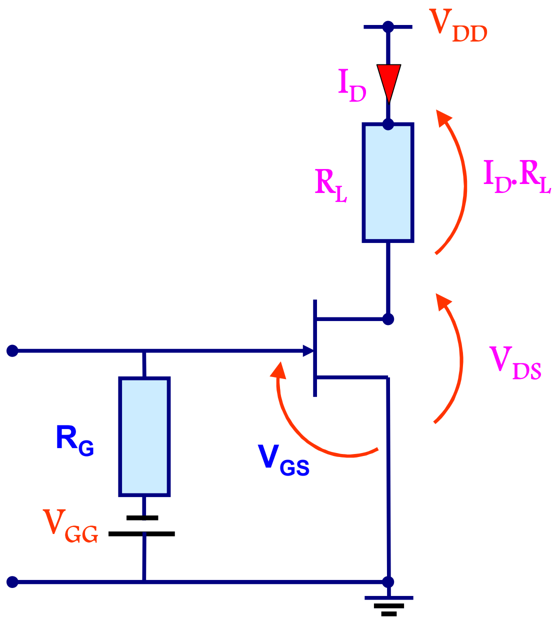
Gate Bias Method

Since $I_G=0$

$V_{GS} = -V_{GG}$



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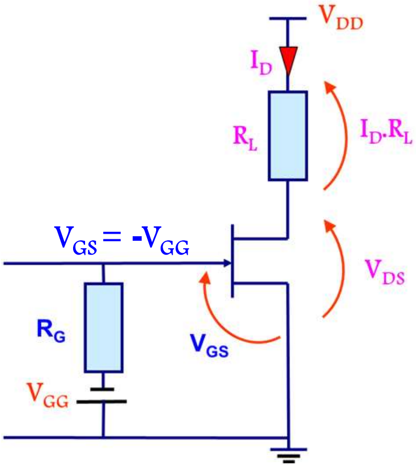
DC Load Line



$$V_{DS} + I_D.RL = VDD$$

$$I_D.RL = -VDS + V_{DD}$$

$$I_D = -\left(\frac{1}{R_L}\right)V_{DS} + \frac{V_{DD}}{R_L}$$

50

For locating the Q point at the center

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\frac{I_D}{I_{DSS}} = \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\sqrt{\frac{I_D}{I_{DSS}}} = 1 - \frac{V_{GS}}{V_P}$$

$$\frac{V_{GS}}{V_P} = 1 - \sqrt{\frac{I_D}{I_{DSS}}}$$

$$\frac{V_{GS}}{V_P} = 1 - \sqrt{0.5} = 0.2929$$

$$\frac{V_P}{V_{GS}} \approx 3.41$$

Choose $V_{GS} \approx \dfrac{V_P}{3.4}$

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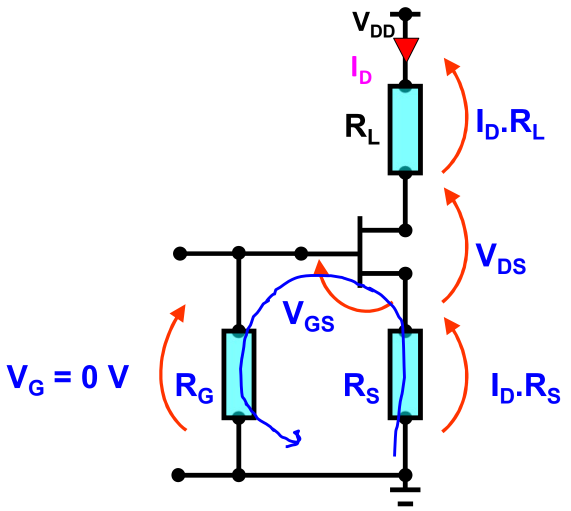
Self-Bias Method



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negative feedback is here === when drain current increased Vgs become more nagative ---> drain current decrases

Calculating the value of Source Resistance

$$I_D \,.\, R_S + V_{GS} - V_G = 0$$

$$I_D \,.\, R_S + V_{GS} = 0$$

$$V_{GS} = -I_D . R_S$$

$$R_S = -\left[\frac{V_{GS}}{I_D}\right] = -\left[\frac{V_{GSQ}}{I_{DQ}}\right]$$

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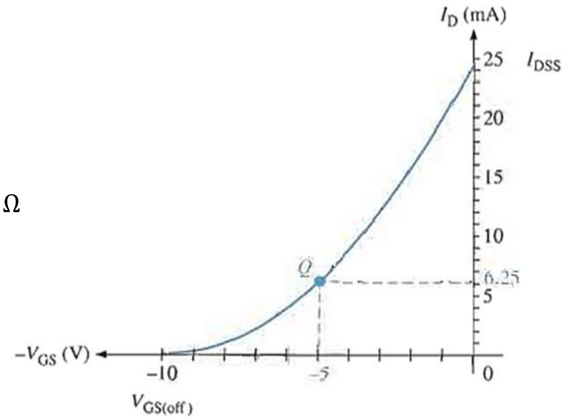
Tutorial Question

$$R_S = -\left[\frac{V_{GS,Q}}{I_{D,Q}}\right]$$

$$R_S = -\left[\frac{-5V}{6.25\ mA}\right] = 800\ \Omega$$



Find bias resistance for this operating point?

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Tutorial Question

Determine the value of R_S required to self-bias a p-channel JFET at a V_{GS} of 5V. This JFET has an I_{DSS} of 25mA and a pinch-off voltage of 15V.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 25.\left(1 - \frac{5}{15}\right)^2$$

$$= 25.(1 - 0.3333)^2$$

$$= 11.1\ \text{mA}$$

$$R_S = \left|\frac{V_{GS,Q}}{I_{D,Q}}\right|$$

$$= \left|\frac{5V}{11.1\ mA}\right|$$

$$= 450\ \Omega$$

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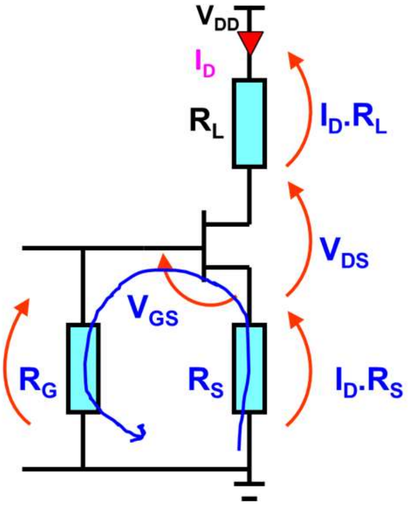
DC Load Line



$$I_D\,R_S + V_{DS} + I_D.R_L = V_{DD}$$

$$I_D(R_S + R_L) = -V_{DS} + V_{DD}$$

$$I_D = \underbrace{-\left[\frac{1}{R_S + R_L}\right]}_{m} V_{DS} + \underbrace{\frac{V_{DD}}{R_S + R_L}}_{C}$$

$$Y = m \quad X + C$$

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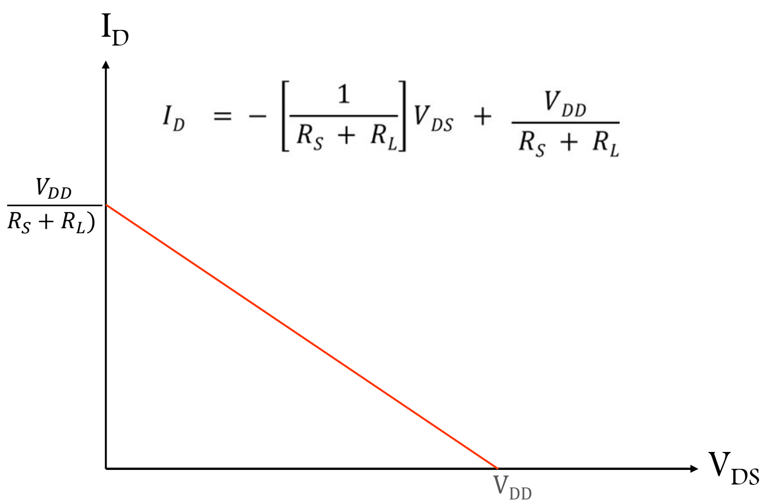
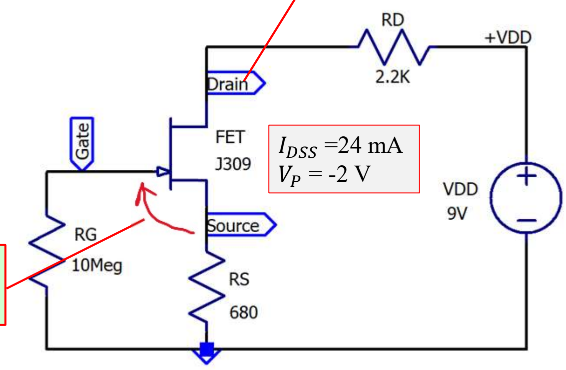
DC Load Line is Kirchoff's Law



Tutorial Question

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 24\left(1-\frac{V_{GS}}{-2}\right)^2$$



V_{GS}= -(0.68 I_D) Volts

$$I_D = 24\left(1-\frac{(0.68\ I_D)}{2}\right)^2$$

$$I_{DQ} = 2.09\ \text{mA}$$

$$I_D(R_S + R_L) + V_{DS} = V_{DD}$$

$$2.88\ I_D + V_{DS} = 9$$

$$V_{DSQ} = 2.98\ \text{V}$$

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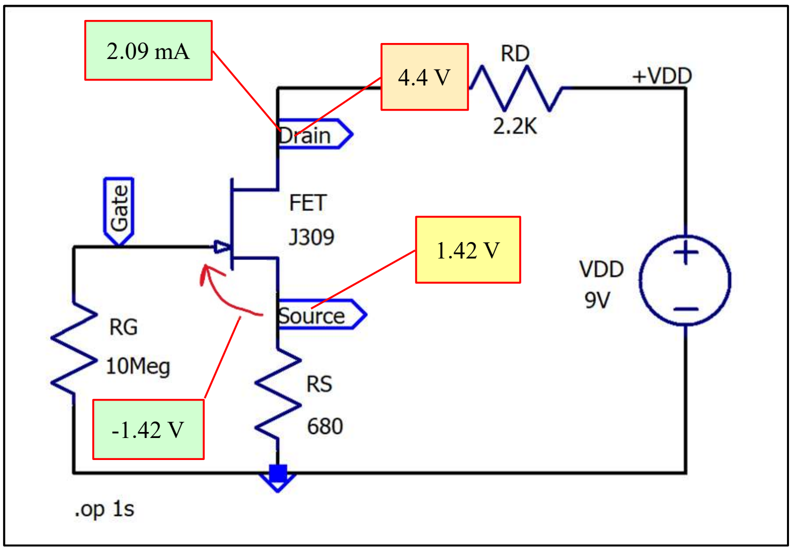

V(+vdd):	9
V(drain):	4.40799
V(source):	1.41935
V(gate):	0.000131759
Id(Fet):	0.00208728
Ig(Fet):	-1.31759e-011
Is(Fet):	-0.00208728
I(Rg):	1.31759e-011
I(Rs):	0.00208728
I(Rd):	0.00208728
I(Vdd):	-0.00208728

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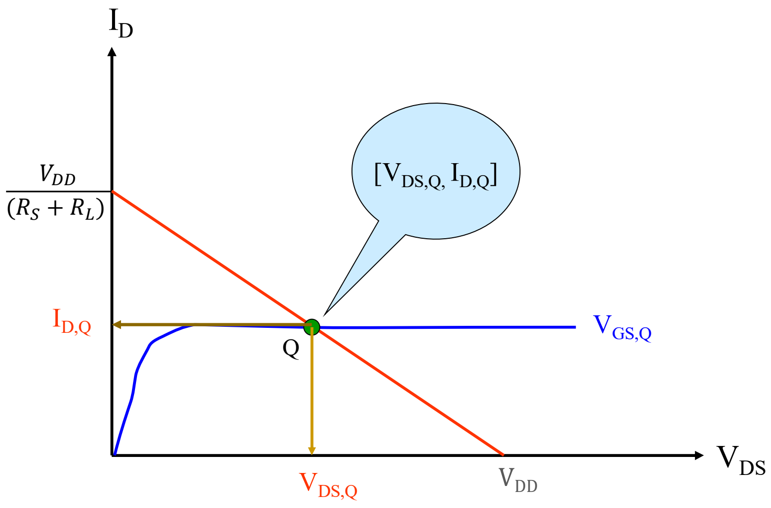
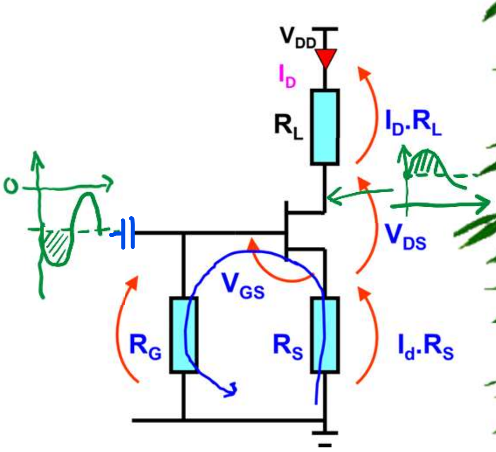
Finding Quiescent Point using DC Load Line



AC Analysis : Action during the negative half cycle

When the input signal voltage (V_{GS}) goes more negative:

- Drain current (I_D) is reduced
- Voltage across the drain resistor drops.
- The drain voltage (V_{DS}) goes more positive.



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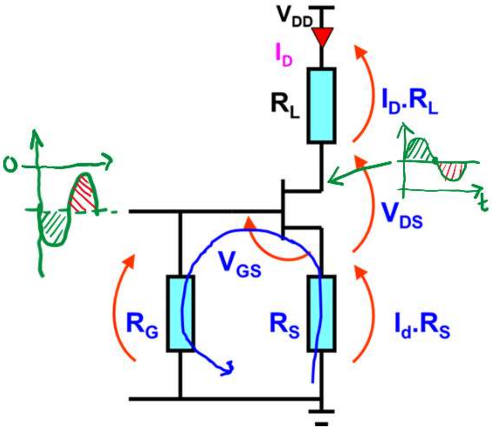
AC Analysis : Action during positive half cycle



When the signal voltage (V_{GS}) goes less negative (more positive) :

- Drain current (I_D) is increased
- Voltage across the drain resistor is more.
- The drain voltage (V_{DS}) goes less positive.

In both cases the drain voltage does the opposite of the gate voltage.

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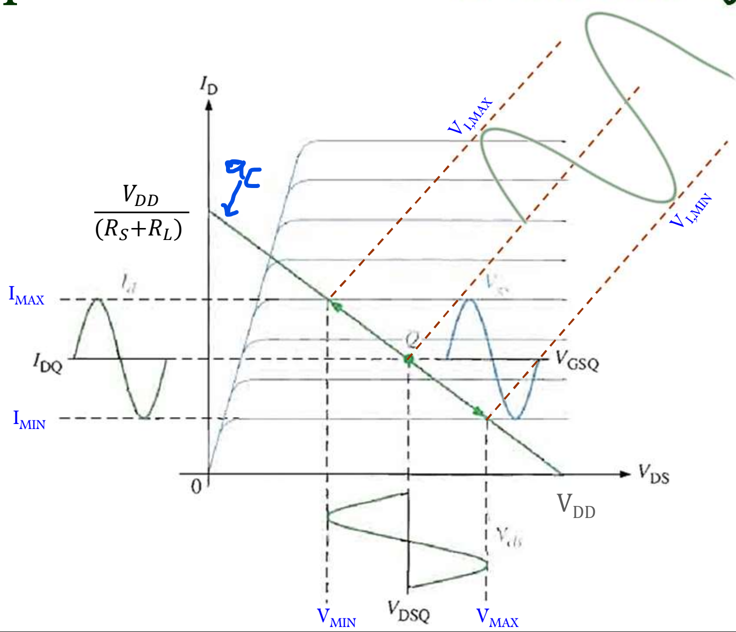
Graphical Illustration of the full cycle



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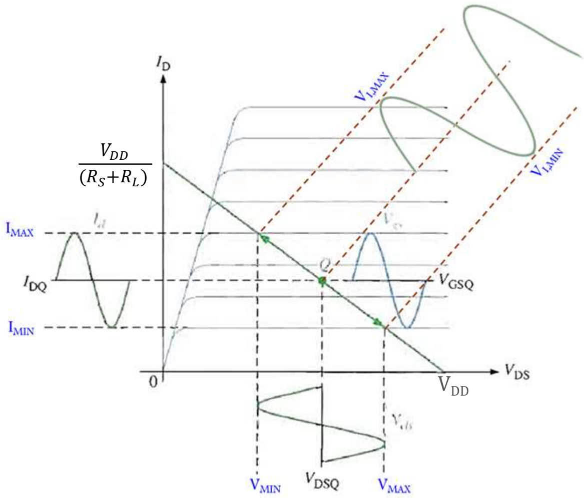
Calculations



$$A_v = \frac{V_{o,(pk-pk)}}{V_{i,(pk-pk)}}$$

$$A_i = \frac{I_{o,(pk-pk)}}{I_{i,(pk-pk)}}$$

$$G = \frac{P_o}{P_i} = |A_v|.|A_i|$$

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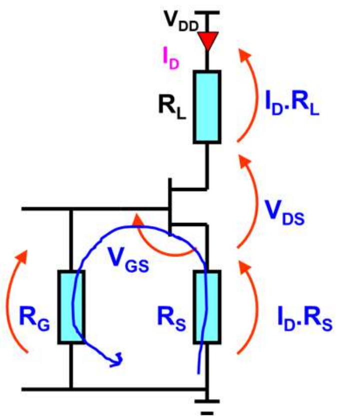
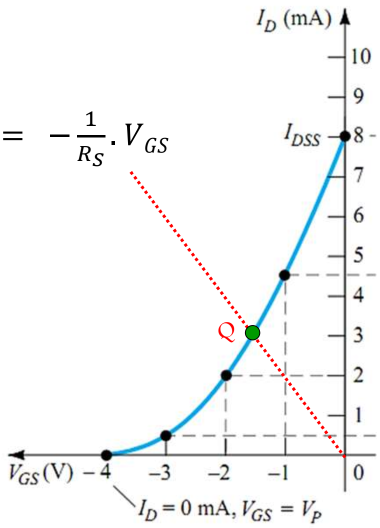
Q~point on Mutual Characteristics



$$I_D \,.\, R_S + V_{GS} - V_G = 0$$
$$I_D \,.\, R_S + V_{GS} = 0$$
$$I_D = -\frac{1}{R_S}.V_{GS}$$

$$I_D = -\frac{1}{R_S}.V_{GS}$$



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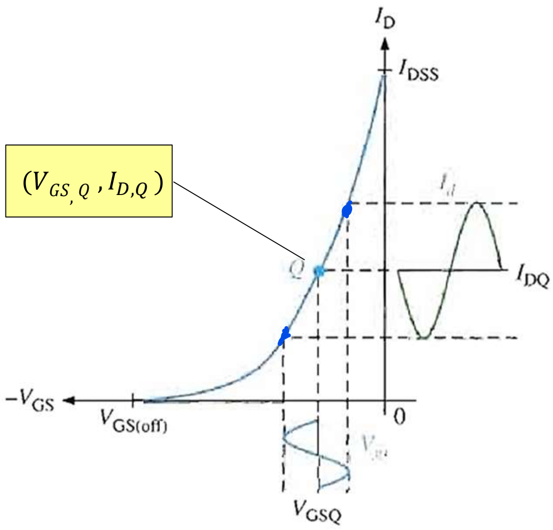
Graphical Illustration on Mutual Characteristics



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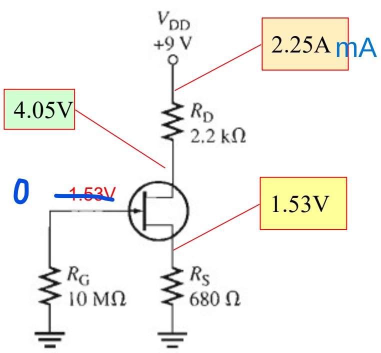
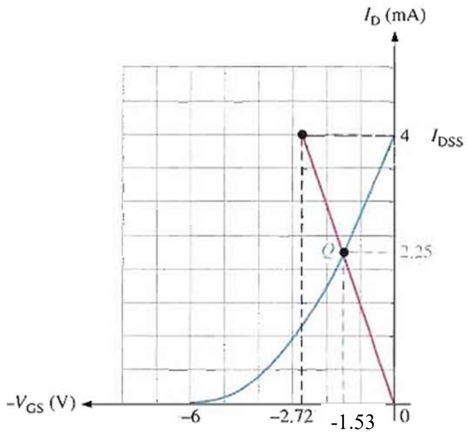
if too much drive --> amplification become non lenear --> calculated gain not be correct

Ex. Mark DC Voltages and Currents at each point on the circuit





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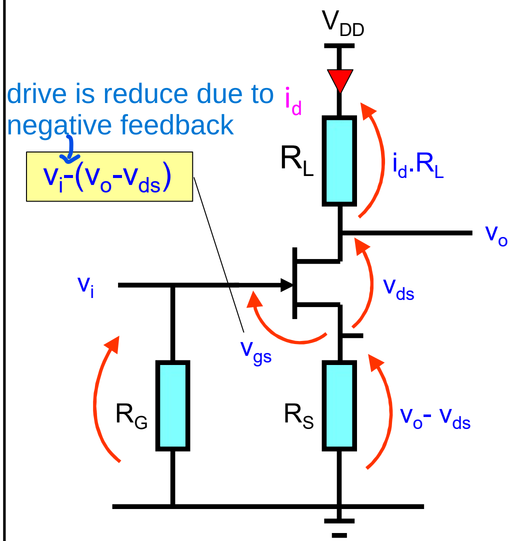
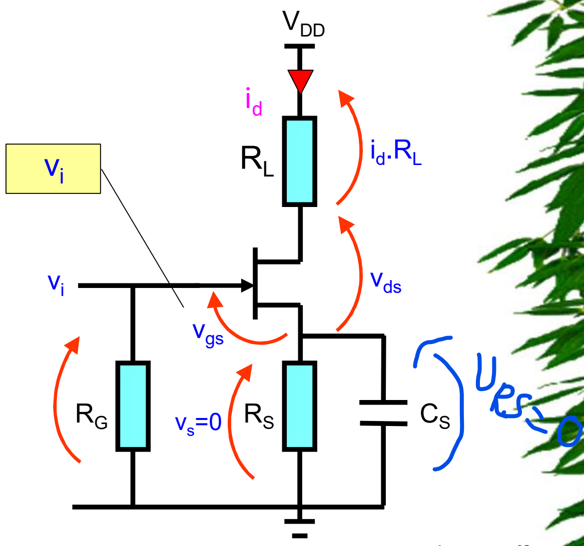
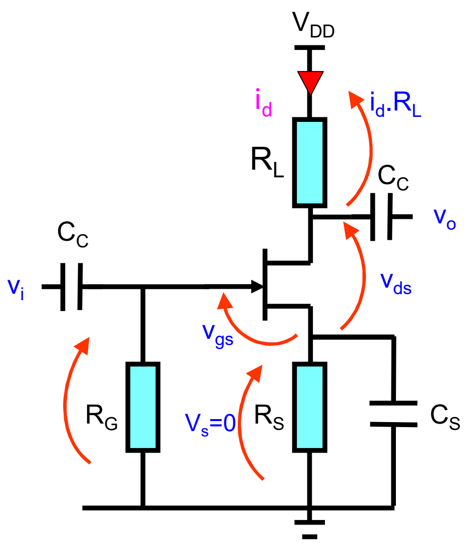
Use of a Source Bypass Capacitor





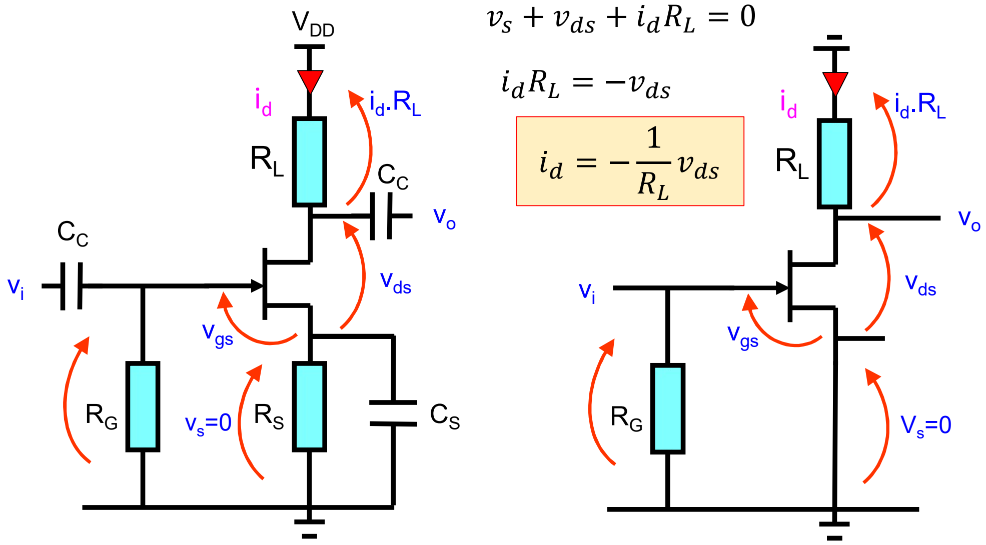
$\frac{1}{\omega C} << \frac{R_S}{10}$

Use of a Source Bypass Capacitor



- Coupling and Bypass capacitors can be considered as short-circuits for ac signals
- Draw an AC equivalent circuit
- Then use KVL on the ac equivalent circuit (only for AC signals)
- Find the new gradient (for AC operation)

Use of a Source Bypass Capacitor



$$v_s + v_{ds} + i_d R_L = 0$$

$$i_d R_L = -v_{ds}$$

$$\boxed{i_d = -\frac{1}{R_L} v_{ds}}$$

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AC Load Line and Gain Calculations….

- Coupling and Bypass capacitors can be considered as S/C connections for ac signals
- Draw an ac equivalent circuit
- Using KVL for ac signals find the new gradient of the load line

$$i_d = -\left[\frac{1}{R_L}\right] v_{ds}$$

- Draw ac load line with that gradient to go through the Q point.
- Then use ac load line for gain calculations

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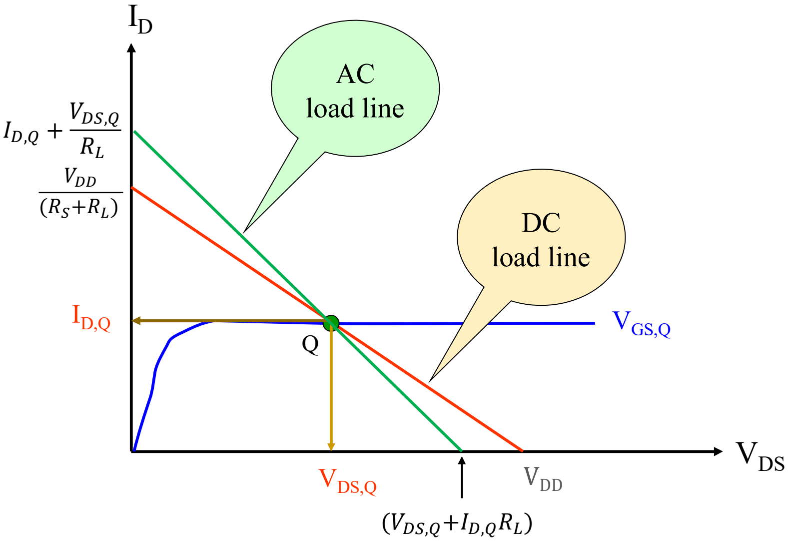
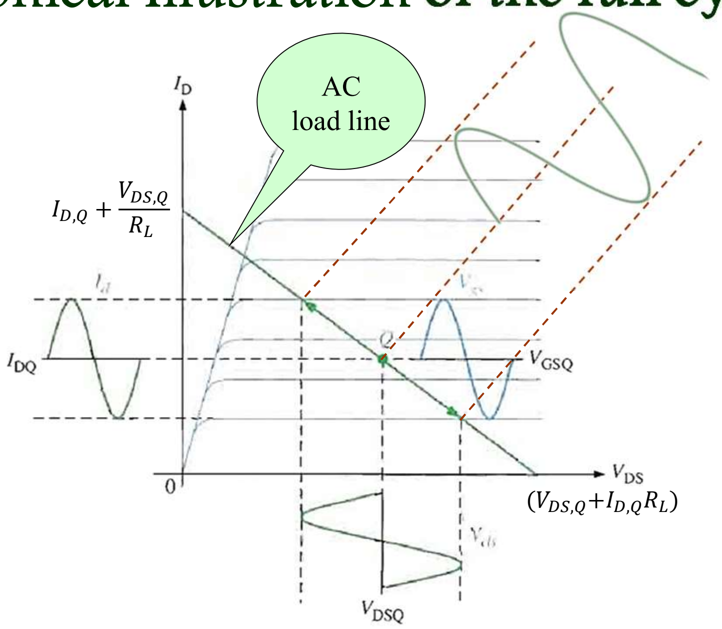
Drawing the ac load line



Graphical Illustration of the full cycle



A Design Example

- Requirement: To build a JFET preamplifier for a musical instrument.
- Given : Drain Resistance = 2.2 kΩ
- The parameters you need to design are:
  - DC Bias (V_{cc})
  - Quiescent channel current
  - Quiescent Gate voltage
  - Cut off frequency of the preamplifier
  - Coupling capacitors

typical guitar coil = 100-200 mV
typical guitar wire(line transmission) = 1 - 2 V
pre amplifier power gain
20 -30 dB
9V power source
input typical impedance = 10kom

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Design Choices

1) JFET selection : Use J113 general purpose FET
   - V_{DS} (maximum) = 35V
   - $V_{GS, (off)}$ = -2 V
   - I_{DSS} = 8.34 mA
   - Max Power Dissipation = 625 mW
   - Drain to Source Resistance = 100 Ω
2) Supply Voltage Selection :
   - Choose 9v as V_{CC}
   - Most musical instrument circuits run on 9V
3) Gate-Source Voltage : Let us choose $V_{GS,Q}$ = 0.8 V

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J113 JFET

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Max.	Unit
Off Characteristics						
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	I_G = -1.0 µA, V_{DS} = 0		-35		V
I_{GSS}	Gate Reverse Current	V_{GS} = -15 V, V_{DS} = 0			-1.0	nA
V_{GS}(off)	Gate-Source Cut-Off Voltage	V_{DS} = 15 V, I_D = 1.0 µA	**111**	-3.0	-10.0	V
			112	-1.0	-5.0	
			113	-0.5	-3.0	
I_D(off)	Drain Cutoff Leakage Current	V_{DS} = 5.0 V, V_{GS} = -10 V			1.0	nA
On Characteristics						
I_{DSS}	Zero-Gate Voltage Drain Current(5)	V_{DS} = 15 V, V_{GS} = 0	**111**	20		mA
			112	5.0		
			113	2.0		
r_{DS}(on)	Drain-Source On Resistance	$V_{DS} \leq$ 0.1 V, V_{GS} = 0	**111**		30	Ω
			112		50	
			113		100	
Small Signal Characteristics						
C_{dg}(on) C_{sg}(on)	Drain-Gate &Source-Gate On Capacitance	V_{DS} = 0, V_{GS} = 0, f = 1.0 MHz			28	pF
C_{dg}(off)	Drain-Gate Off Capacitance	V_{DS} = 0, V_{GS} = -10 V, f = 1.0 MHz			5.0	pF
C_{sg}(off)	Source-Gate Off Capacitance	V_{DS} = 0, V_{GS} = -10 V, f = 1.0 MHz			5.0	pF

Note:

5. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%.

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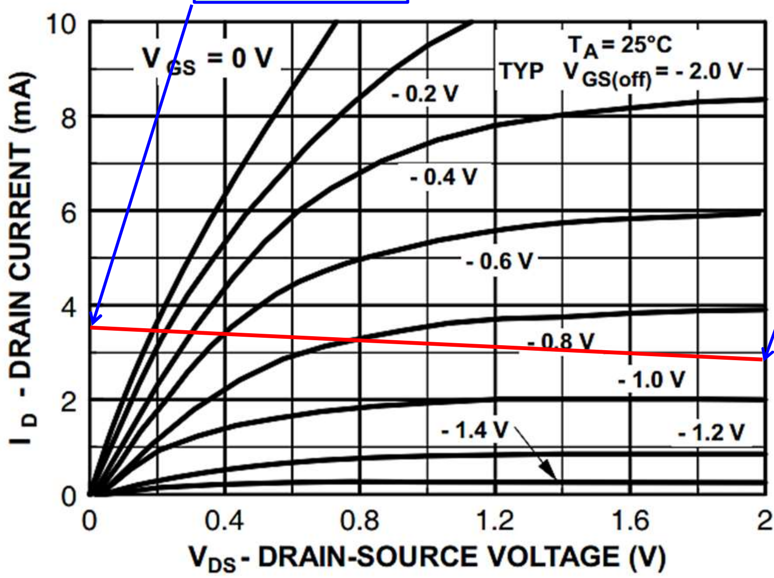
J113 JFET

$$\frac{9}{2.2 + 0.267} = 3.65$$

$$\frac{9 - 2}{2.2 + 0.267} = 2.84$$

2.25A



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Design (cont.) : Operating Point

Chosen $V_{GS} = -0.8$ V

$$R_S = \left|\frac{0.8\,V}{3\,mA}\right| = 267\ \text{k}\Omega$$

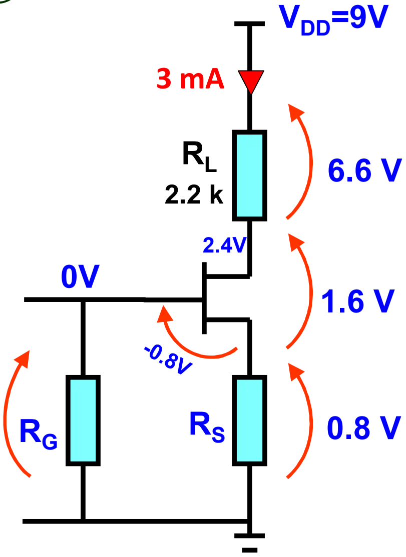
$$I_D = 8.34\left(1 - \frac{0.8}{2}\right)^2 = 3\ mA$$

$$V_S = I_D R_S = 3 \text{ x } 267 = 0.8V$$

$$V_L = I_D R_D = 3 \text{ x } 2200 = 6.6V$$

$$V_D = 9 - 6.6 = 2.4\ \text{V}$$

$$V_{DS} = 2.4 - 0.8 = 1.6\ \text{V}$$



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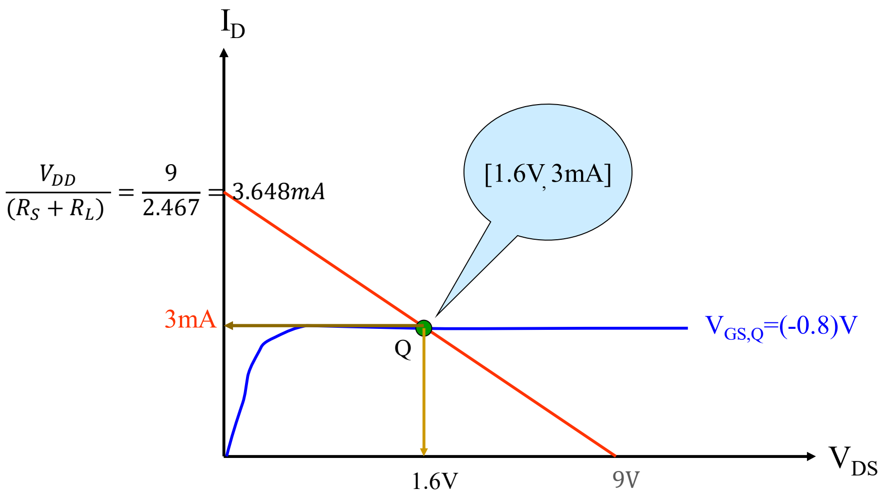
Design (cont.) : Operating Point



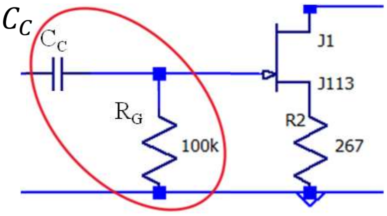
Design (Cont.) : Input Interface with Source

- Input Impedance
  - Too low : Loading on the source i.e Guitar pickup.
  - Too high : Circuit will be noisier due to the thermal noise of the resistor
  - 100 kΩ to 1 MΩ is OK.
  - Let us use a value of 100 kΩ for R_G

$$\tau = R_G . C_C$$

$$f_c = \frac{1}{2.\pi.\tau}$$

$$f_c = \frac{1}{2.\pi.R_G.C_C}$$



Design (Cont.) : Input Interface with Source

Assuming standard guitar;

We can choose the lower cutoff frequency as 82.4Hz

$$f_c = \frac{1}{2.\pi.R_G.C_C} = 82.4\text{Hz (assuming standard guitar)}$$

$$C_C = \frac{1}{2.\pi.R_G.f_c} = \frac{1}{2.\pi.(100{,}000).(82.4)} = 19.1 \text{ nF}$$

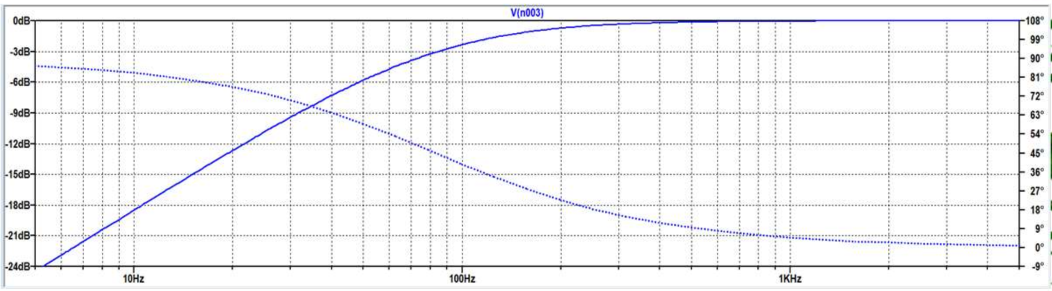
$$C_C > 19.1 \text{ nF}$$

Any higher value is OK. Therefore, we can choose a typical μF value.

Design (Cont.) : Input Interface with Source

When $C_C = 19.1$ nF; $\quad f_c = \dfrac{1}{2.\pi.R_G.C_C} = 82.4\text{Hz}$

Use the command; .ac dec 10 0.1 2000



However, $X_c = \dfrac{1}{2.\pi.f.C_C} = \dfrac{1}{2.\pi.(82.4).(19.1)} \approx 100k\Omega\,!\,(too\ much)$

For C_C any higher value is OK. Therefore, we can choose a typical μF value.

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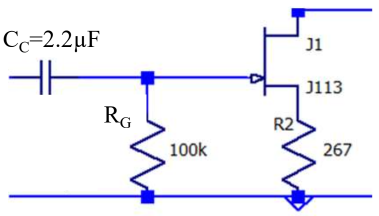
Design (Cont.) : Input Interface with Source

Let us use C_C=2.2μF



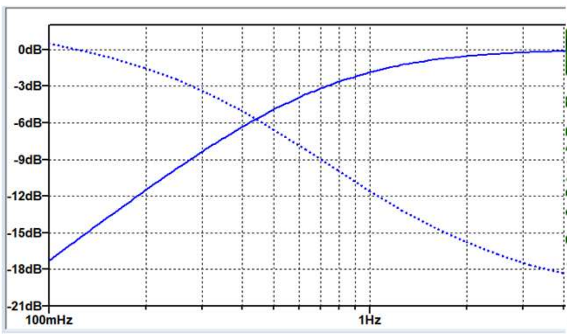
$$f_c = \frac{1}{2.\pi.R_G.C_C}$$

$$f_c = \frac{1}{2.\pi.(100).(2.2)} kHz = 0.7Hz$$

$$X_c = \frac{1}{2.\pi.f.C_C}$$

$$X_c = \frac{1}{2.\pi.(82.4).(2.2)} M\Omega$$

$$X_c = 878\Omega$$



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Design (Cont.) : Output Interface with Load

- Input impedance of the next stage?
  - Let us assume a standard and quite low value, such as 10kΩ.
  - Always make sure this is larger than R_D.

$$C_C = \frac{1}{2.\pi.R_L.f_c} = \frac{1}{2.\pi.(10{,}000).(82.4)} = 194 \text{ nF}$$

$$C > 194 \text{ nF}$$

- Any higher value is OK. Therefore, we can choose a typical μF value.
- E.g. 1μF coupling capacitor can give us a lower cut off frequency of 7 Hz.

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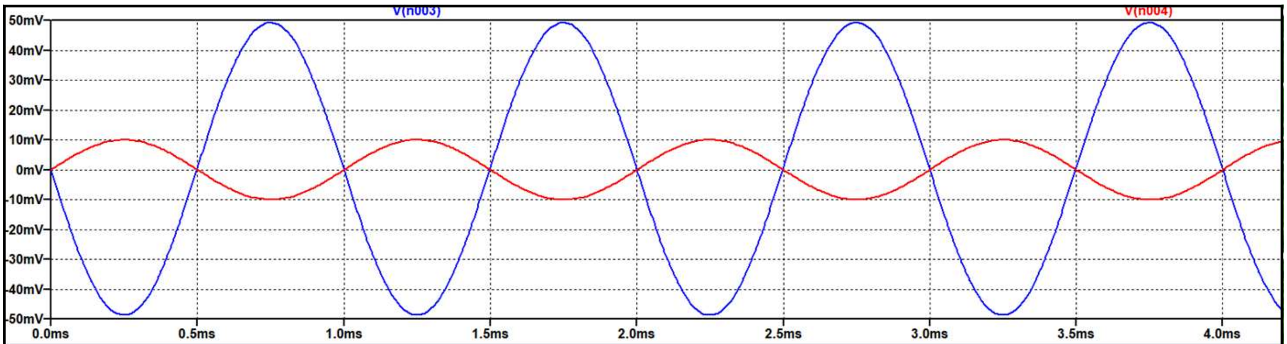
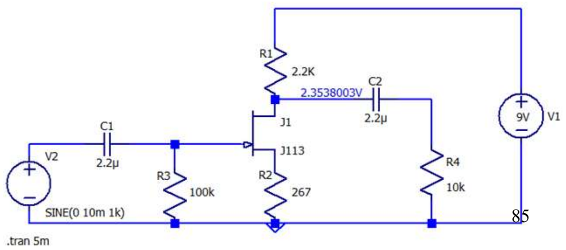


Self bias JFET Amplifier_Design Example

```
--- Operating Point ---

V(n001):      9
V(n002):      2.3538
V(p001):      0.806607
V(n005):      9.35467e-007
V(n004):      0
V(n003):      2.3538e-014
I(C2):        -2.3538e-018
I(C1):        2.05803e-027
Id(J1):       0.003021
Ig(J1):       -9.35467e-012
Is(J1):       -0.003021
I(R4):        2.3538e-018
I(R3):        9.35467e-012
I(R2):        0.003021
I(R1):        0.003021
I(V2):        2.05803e-027
I(V1):        -0.003021
```



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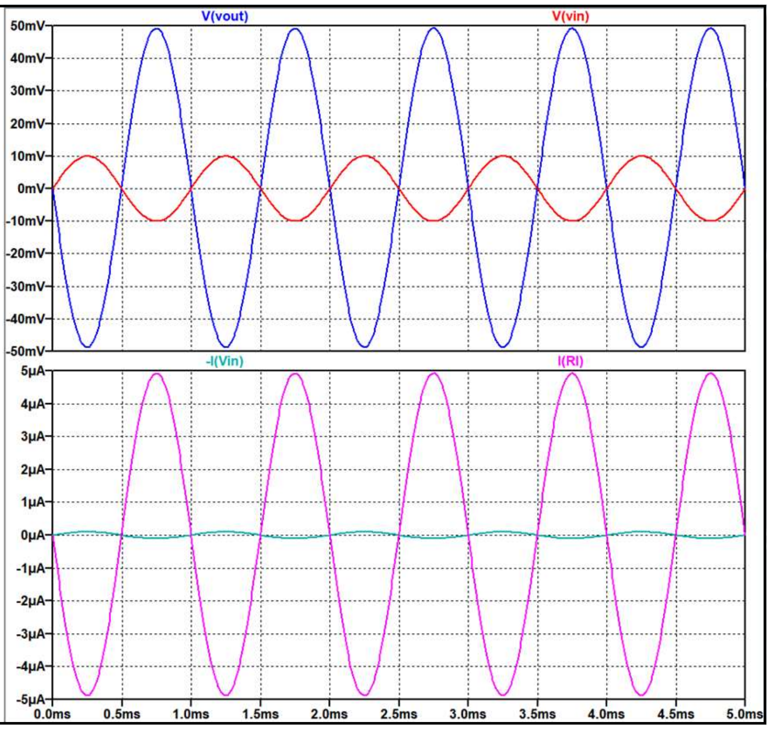
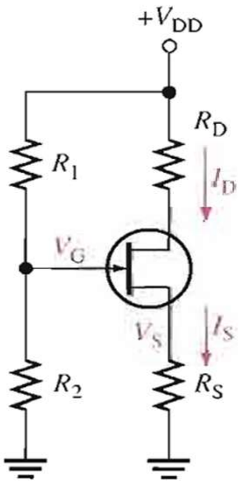
$$A_v = -\frac{V_{o,(pk-pk)}}{V_{i,(pk-pk)}} = -\frac{100mV}{20mV} = -5$$

$$A_i = \frac{I_{o,(pk-p\ \ )}}{I_{i,(pk-pk)}} = -\frac{10\mu A}{200nA} = 50$$

$$G = \frac{P_o}{P_i} = |A_v|.|A_i| = 5\ x50 = 250$$



Potential Divider Biasing Method



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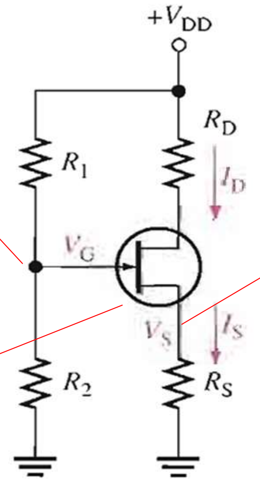
Potential Divider Bias

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$$



$$V_S = I_D R_S$$

$$V_{GS} = V_G - V_S$$

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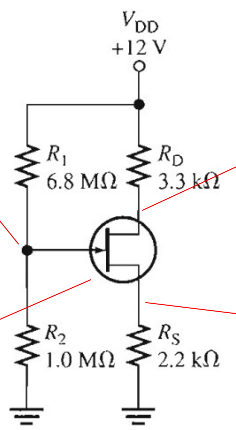
Potential Divider Bias Example

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12\ \text{V} - 7\ \text{V}}{3.3\ \text{k}\Omega} = \frac{5\ \text{V}}{3.3\ \text{k}\Omega} = \mathbf{1.52\ mA}$$

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = 1.54V$$



You decide this 7v

$$V_D \approx 7V$$

$$V_S = I_D R_S = 3.39V$$

$$V_{GS} = V_G - V_S = -1.85V$$

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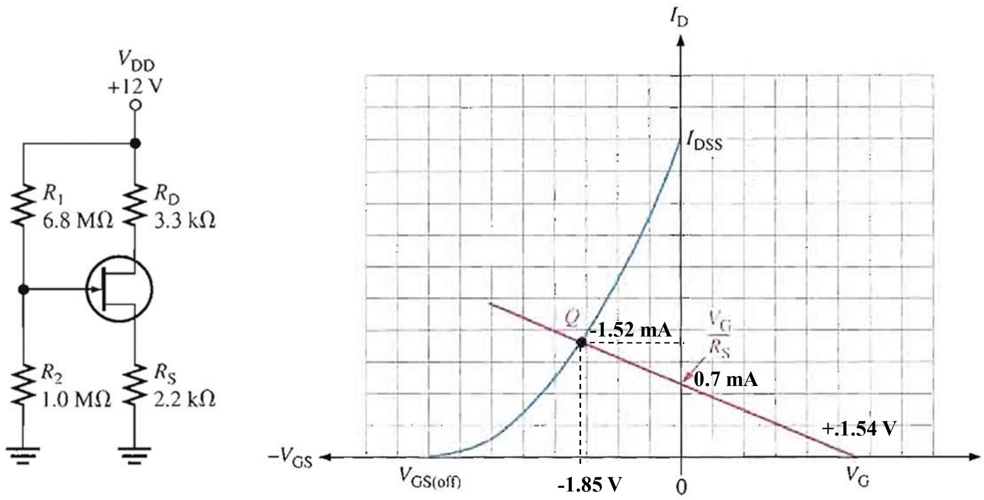
DC Load Line…
on Static Mutual Characteristics



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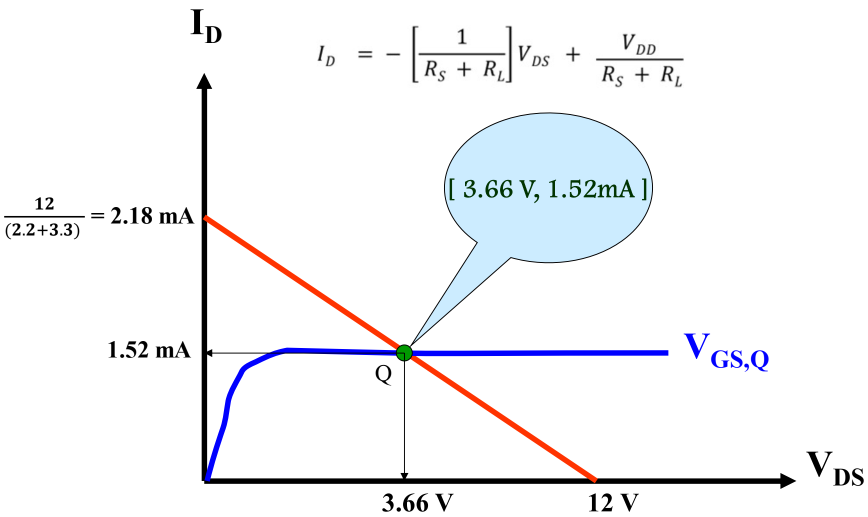
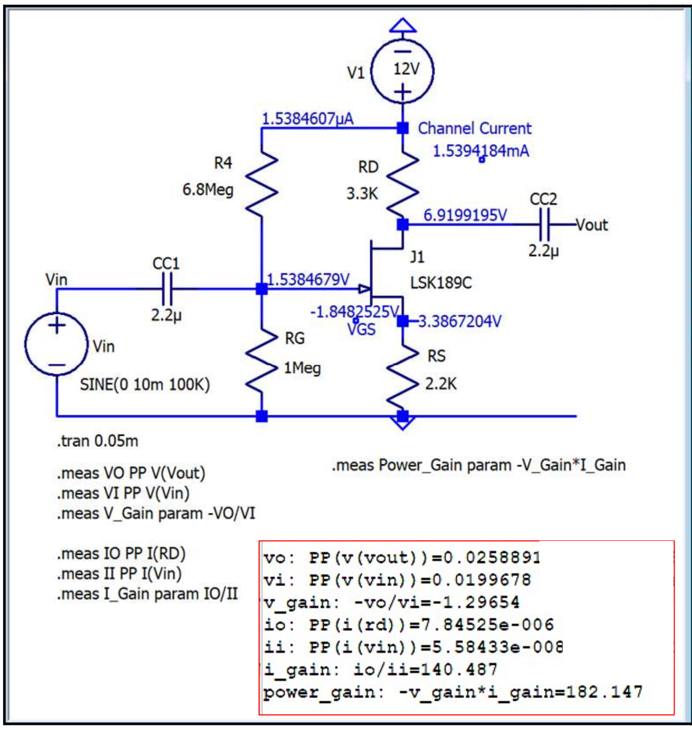
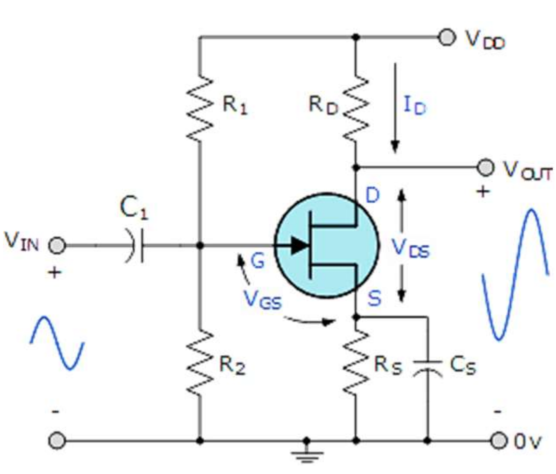
DC Load Line…
on Static Output Characteristics

$$I_D = -\left[\frac{1}{R_S + R_L}\right]V_{DS} + \frac{V_{DD}}{R_S + R_L}$$





Use of Bypass Capacitors



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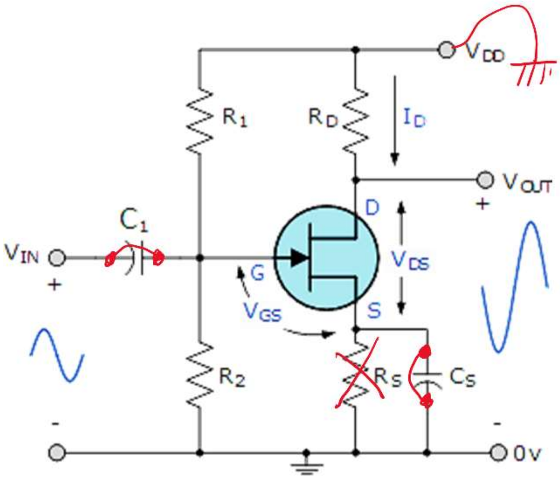
AC Equivalent Circuit



$v_{ds} + i_d R_D = 0$

$i_d = \left(\frac{-1}{R_D}\right) v_{ds}$

Gradient

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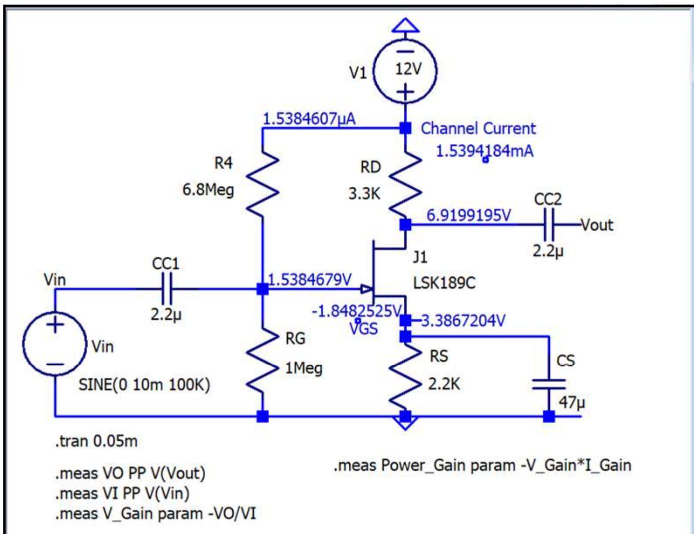
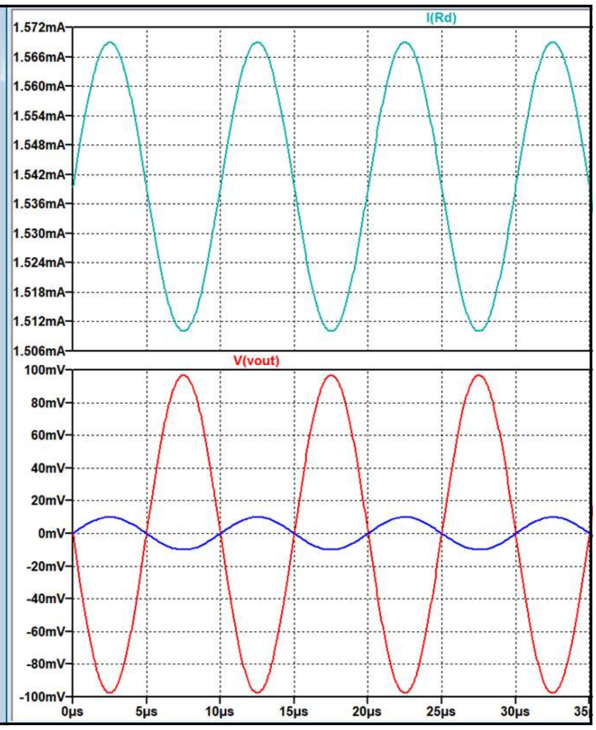



```
vo: PP(v(vout))=0.194613
vi: PP(v(vin))=0.019993
v_gain: -vo/vi=-9.73406
io: PP(i(rd))=5.89735e-005
ii: PP(i(vin))=2.46457e-007
i_gain: io/ii=239.285
power_gain: -v_gain*i_gain=2329.21
```



AC Load Line and Gain Calculations….

- Coupling and Bypass capacitors can be considered as S/C connections for ac signals
- Draw an ac equivalent circuit
- Using KVL for ac signals find the new gradient of the load line
- Draw ac load line with that gradient <u>to go through the Q point</u>.
- Then use ac load line for gain calculations

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