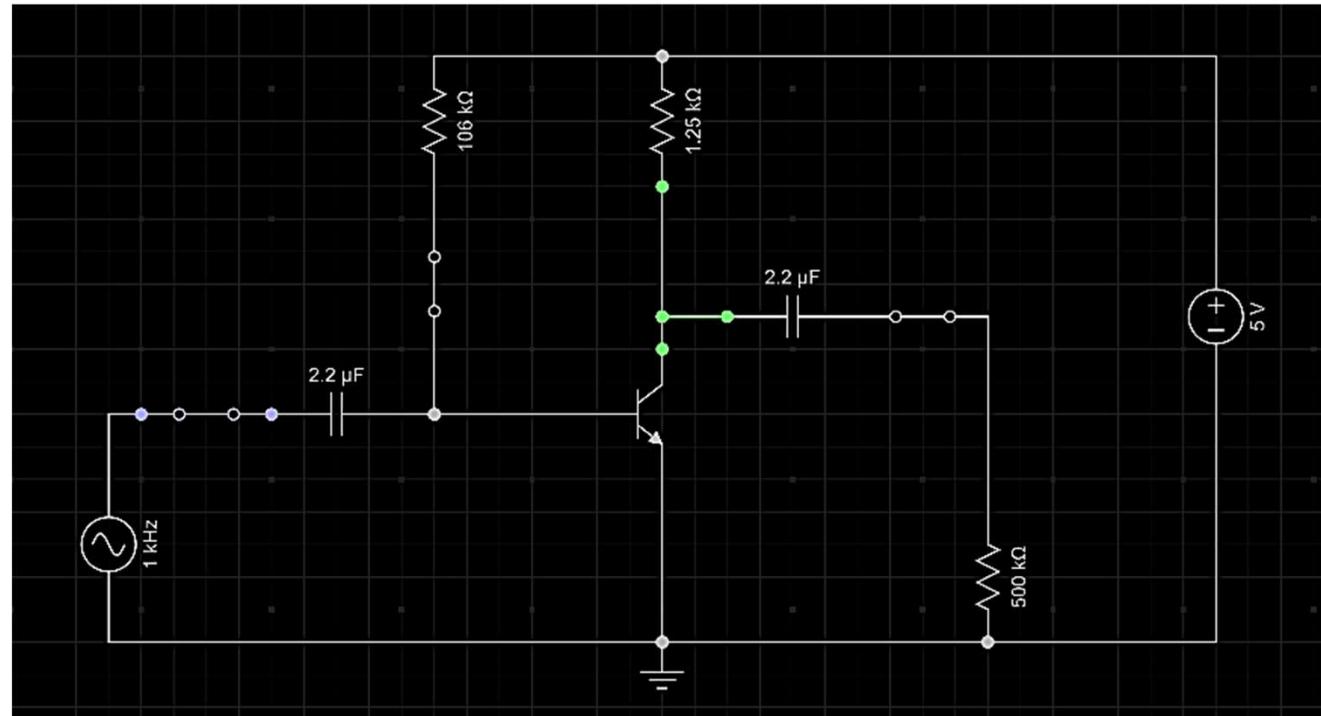


## When the Load is External

Assume capacitor coupling  
(RC Coupling)





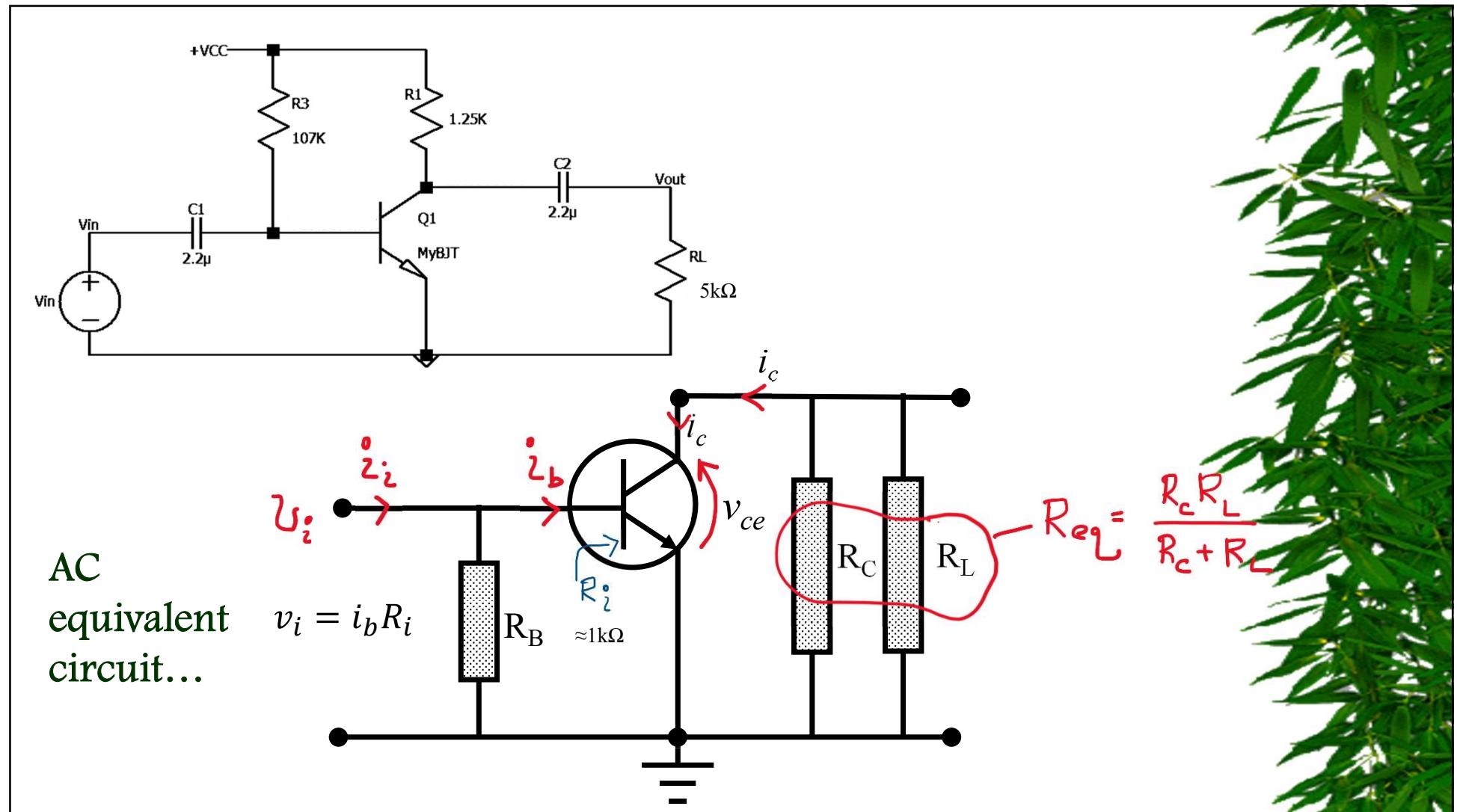
- The external load resistance is decoupled by output coupling capacitor. So, it does not affect Q-point. Therefore, DC analysis is same as before.

# AC Analysis

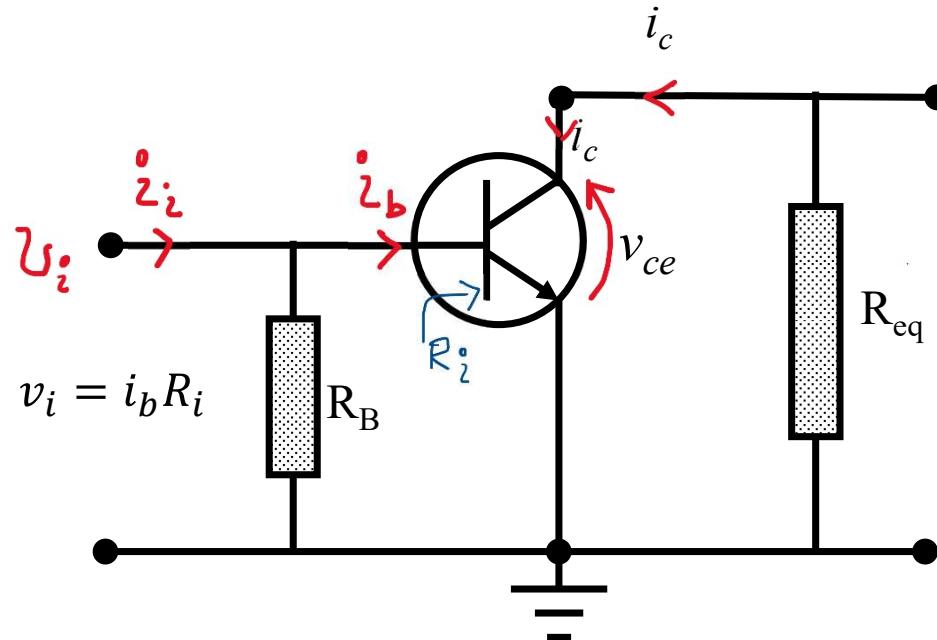
- Assumptions for AC analysis;
  - 1) Coupling capacitors act as short circuits for AC.
  - 2) Bypass capacitors act as short circuits for AC.
  - 3) DC power supplies act as short circuits (to ground) for AC.

Apply these assumptions and draw the AC equivalent circuit of the given amplifier.





## AC load line



Applying KCL for input side...

$$i_i = i_b + \frac{v_i}{R_B} = i_b \left( 1 + \frac{R_i}{R_B} \right)$$

Applying KVL for output side...

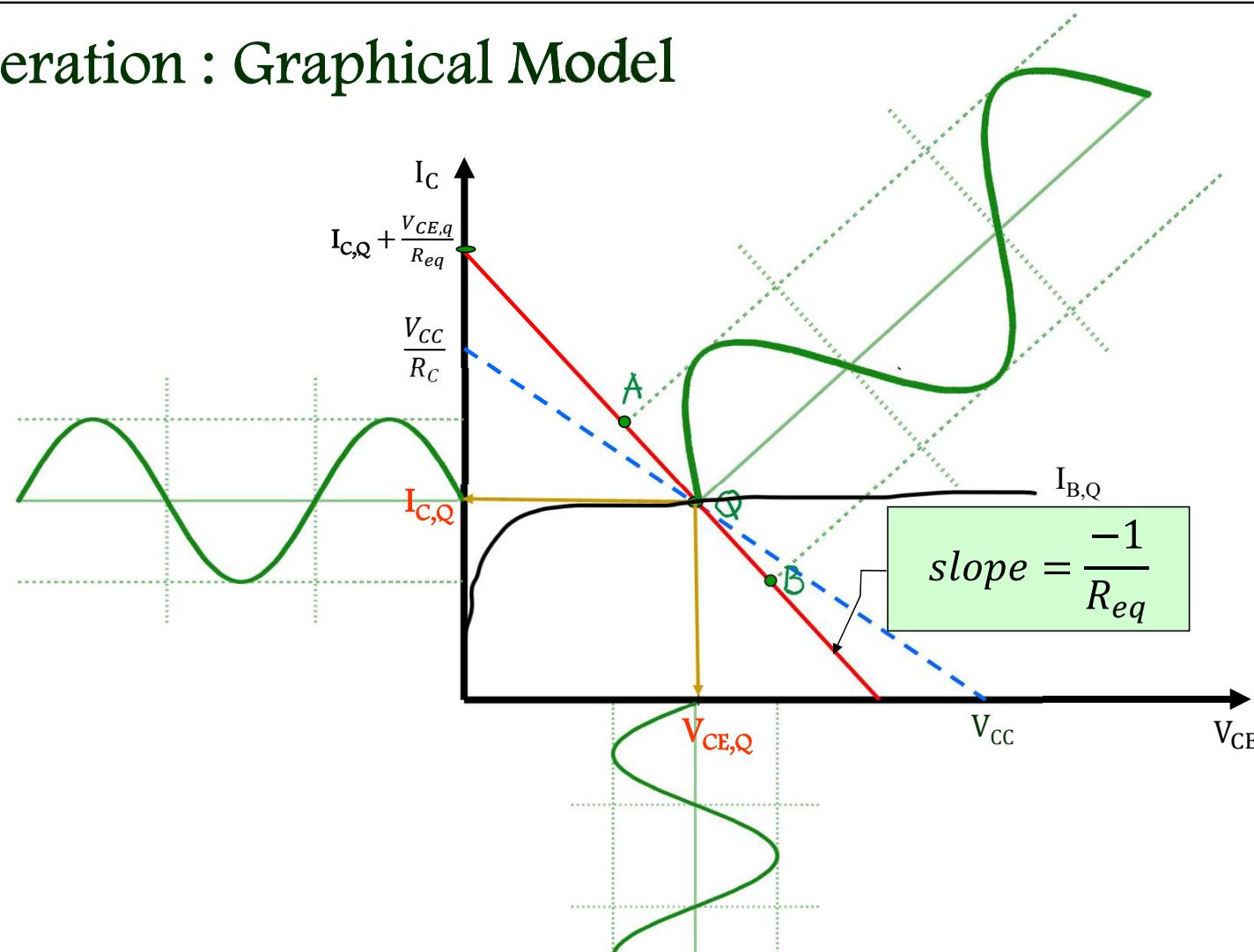
$$v_{ce} + i_c R_{eq} = 0$$

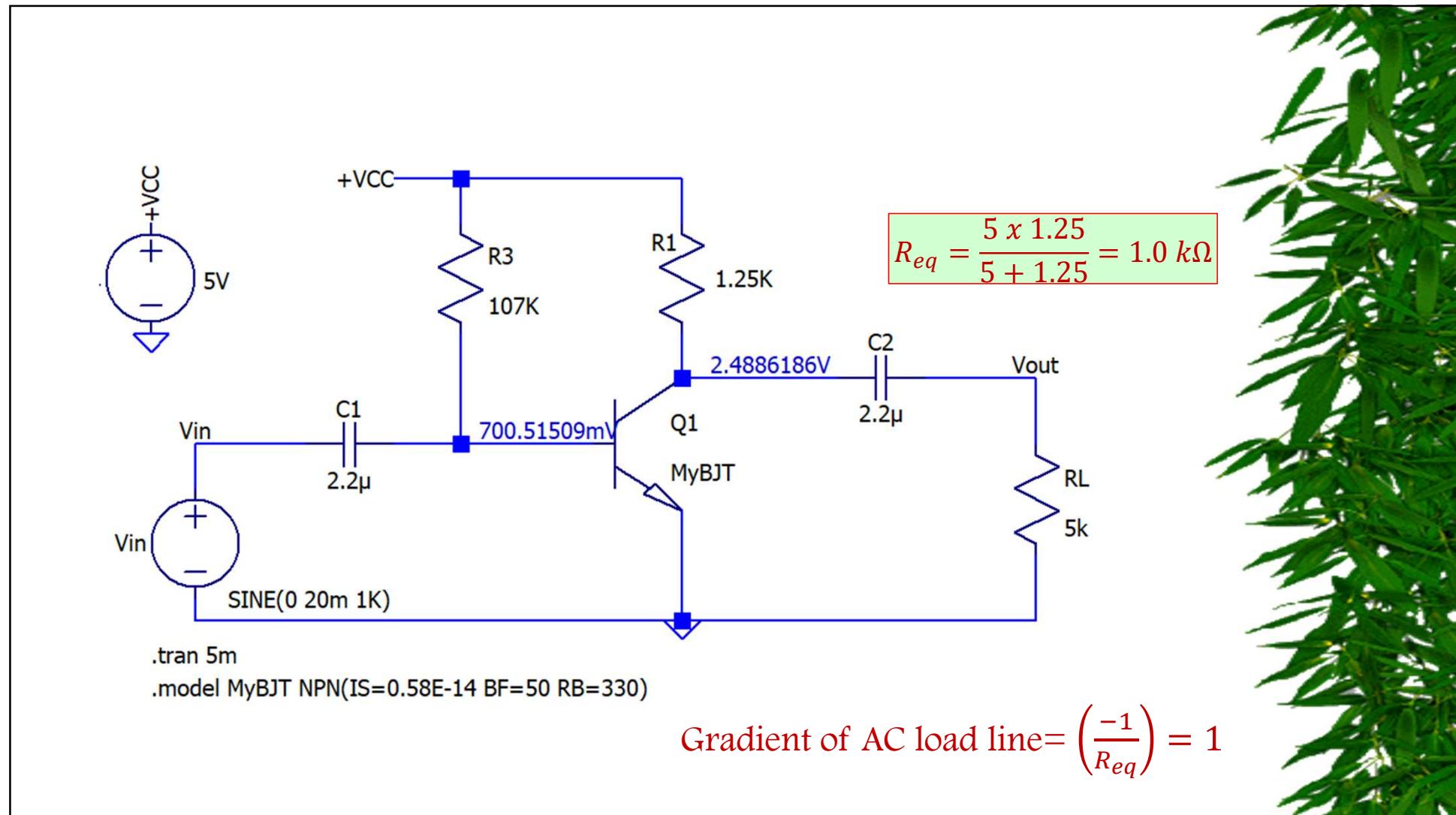
$$i_c = \left( \frac{-1}{R_{eq}} \right) v_{ce}$$

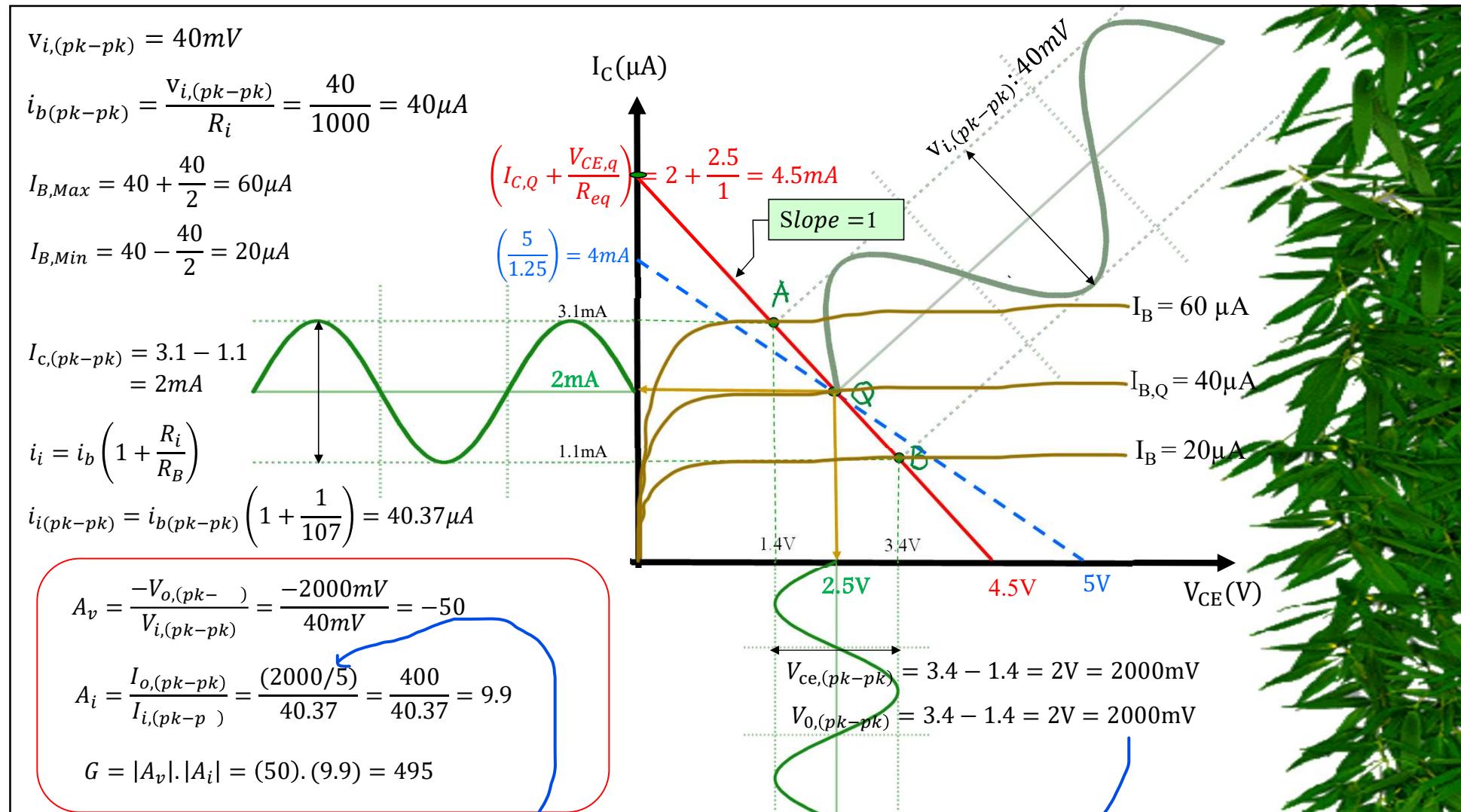
$$\text{Gradient of AC load line} = \left( \frac{-1}{R_{eq}} \right)$$

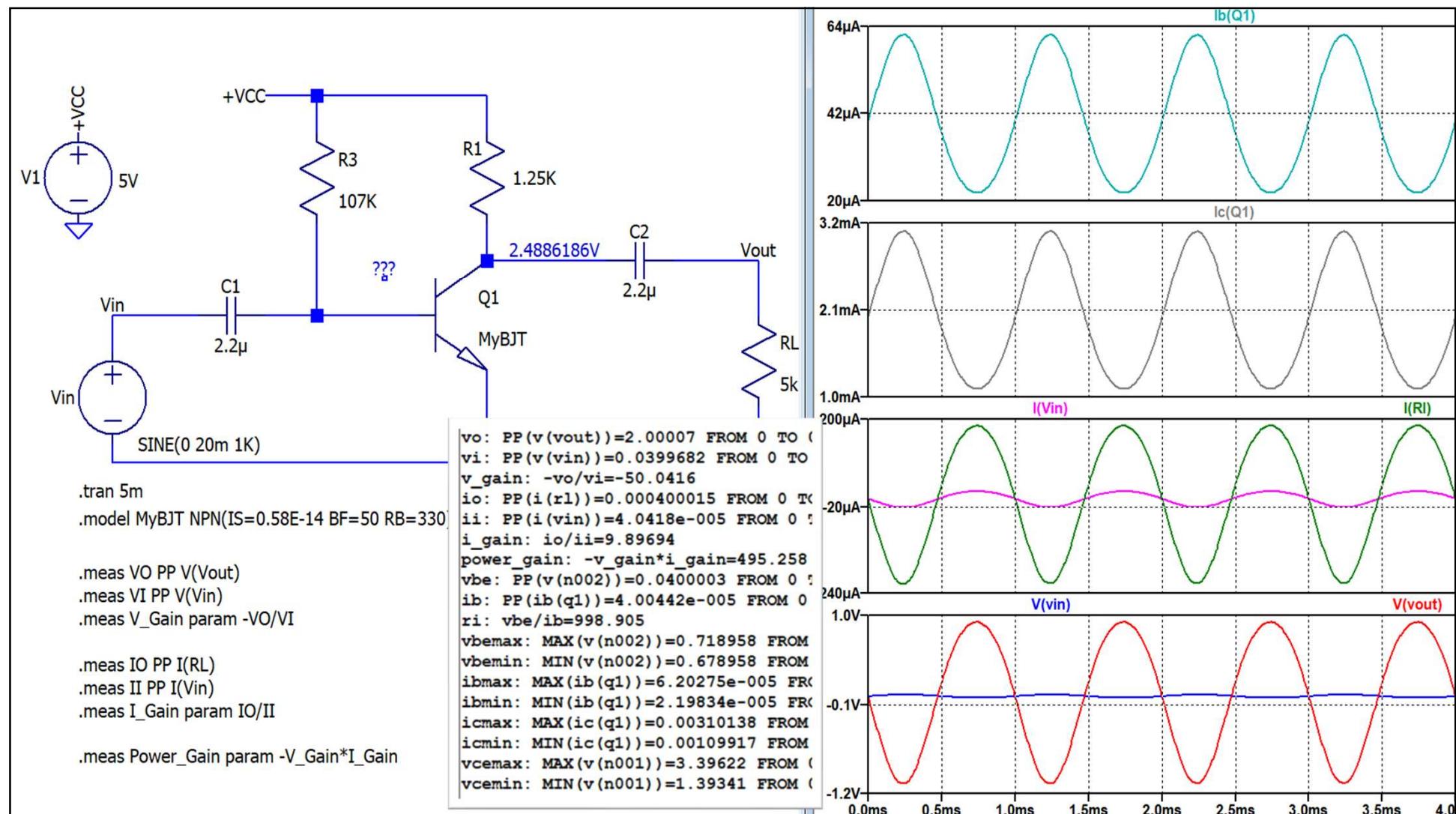


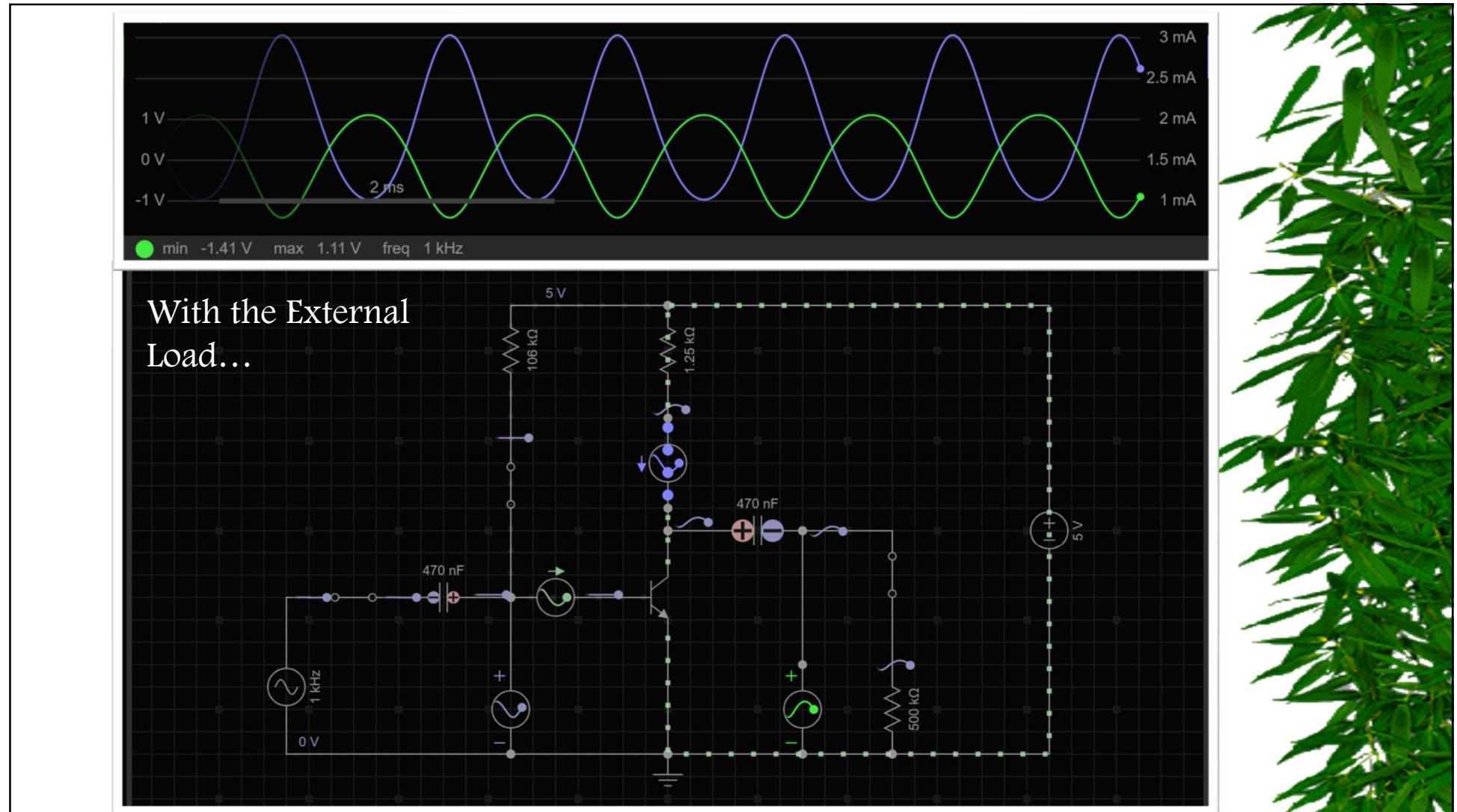
## Operation : Graphical Model











With the External Load...

## Thermal Runaway

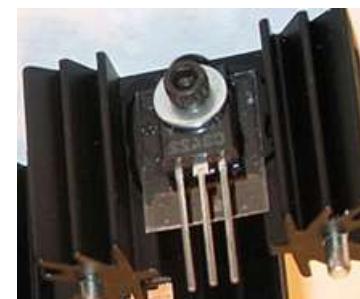
- \* Power is dissipated in the collector and hence it is made physically larger than the emitter and base region.
- \* As the power is dissipated, the base-collector junction temperature increase.
- \* The reverse leakage current ( $I_{CBO}$ ) increases due to the flow of thermally generated minority carriers

$$I_C = \alpha I_E + I_{CBO}$$

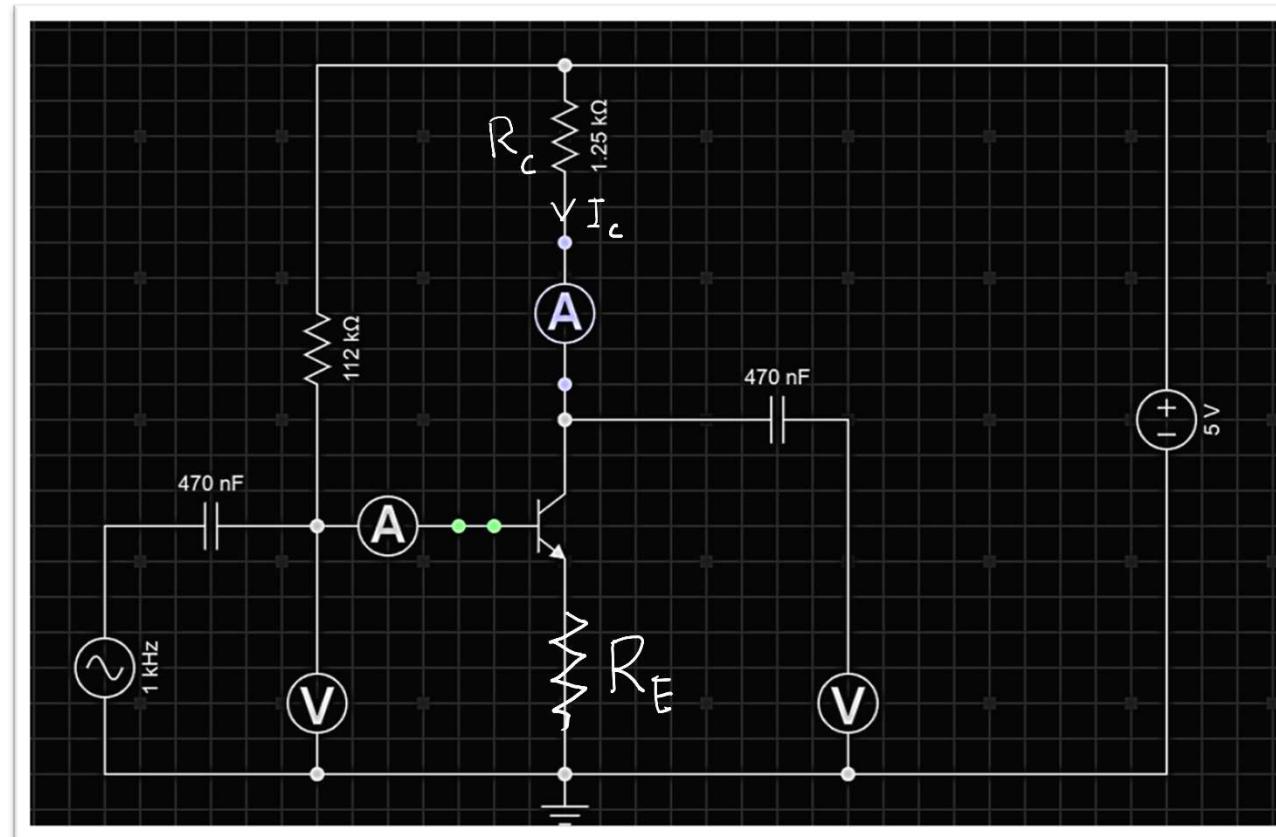


# Thermal Runaway

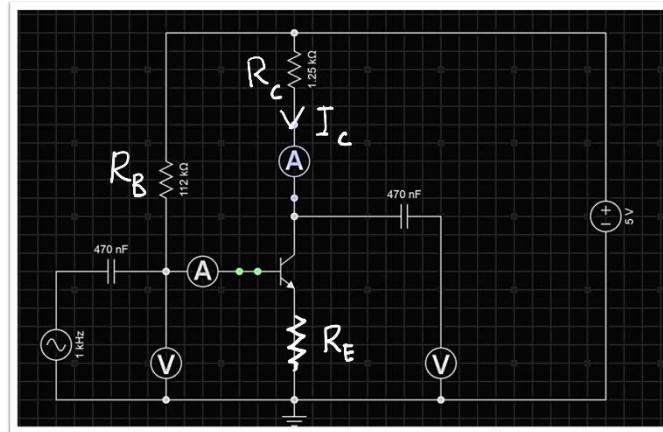
- \* Process is cumulative leading eventually to the destruction of the transistor.
- \* This 'Thermal Runaway' can be prevented by using a heat sink.
- \* Emitter degenerative feedback can also be used.



## Emitter Degeneration with degenerative feedback



## Emitter Degeneration with degenerative feedback



$$I_C (R_L + R_E) = - (V_{CE}) + V_{CC}$$

$$I_C = - \left( \frac{V_{CE}}{R_L + R_E} \right) + \left( \frac{V_{CC}}{R_L + R_E} \right)$$

$$I_E R_E + V_{CE} + I_C R_L = V_{CC}$$

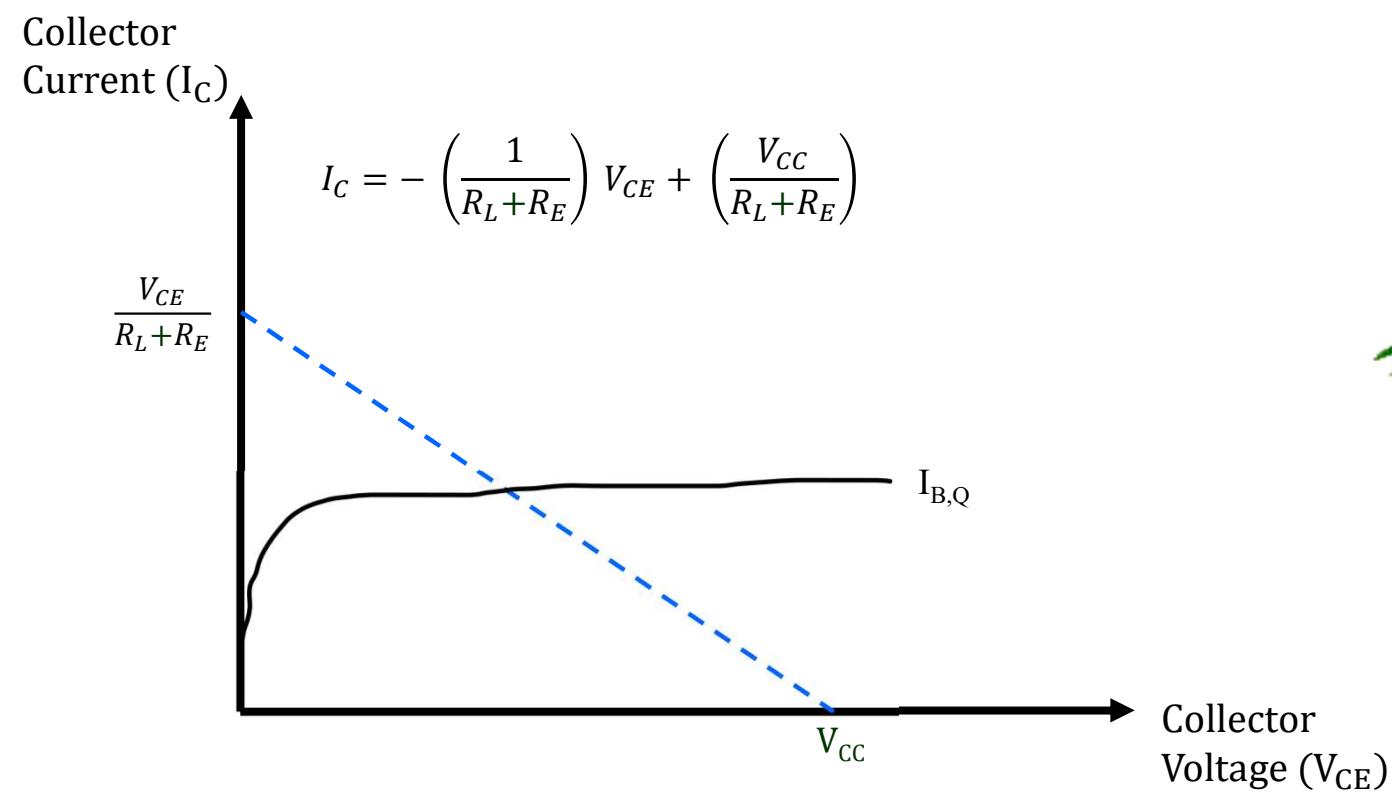
$$I_C = - \left( \frac{1}{R_L + R_E} \right) V_{CE} + \left( \frac{V_{CC}}{R_L + R_E} \right)$$

$$I_C R_E + V_{CE} + I_C R_L = V_{CC}$$

$$\textcolor{red}{Y} = \textcolor{magenta}{m} \textcolor{blue}{X} + \textcolor{cyan}{C}$$



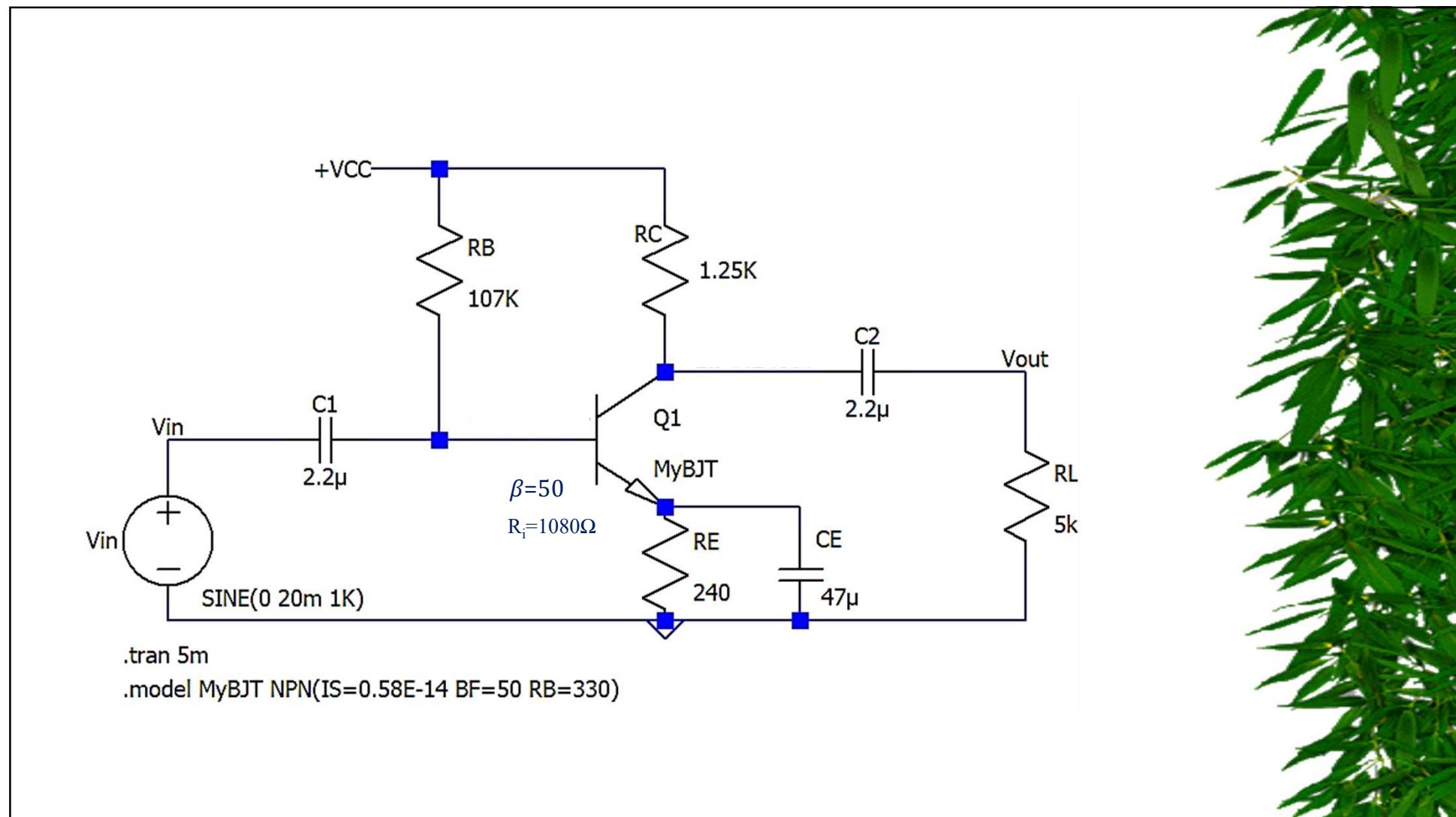
## DC Load Line

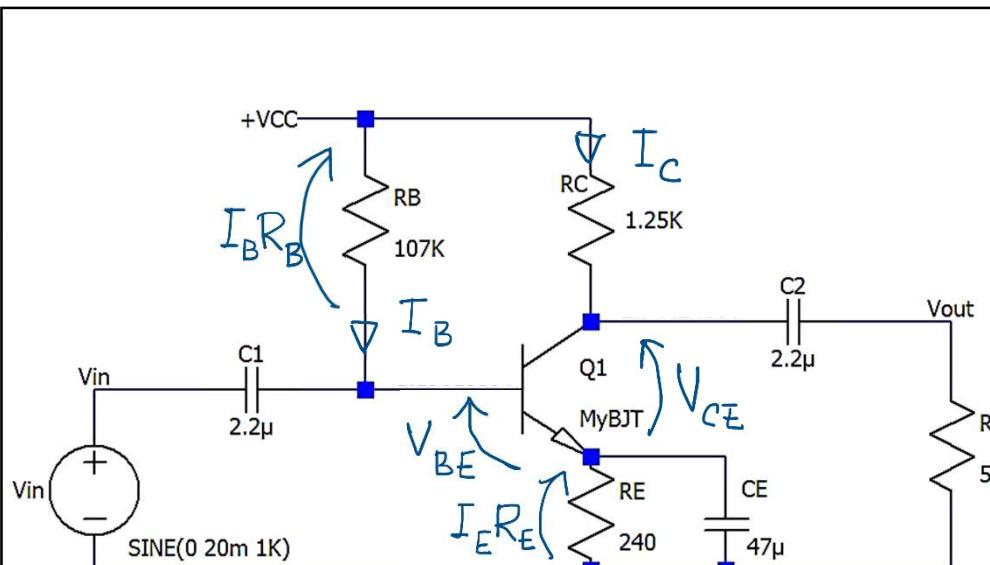


## Emitter by-pass capacitor

- Now Q point is stabilized against drift caused by variations of  $\beta$ .
- However, gain will reduce significantly due to the ac signal at the output being negatively fed-back to the input side through emitter degeneration resistor.
- Solution : Bypass the  $R_E$  for ac signal using an emitter by-pass capacitor across  $R_E$ .
- Capacitance of the by-pass capacitor should be high in order to provide a low reactance path for ac signal.







$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta)R_E}$$

$$I_B = \frac{5 - 0.7}{107 + 0.24(1 + 50)}$$

$$I_B = 36\mu A$$

$$I_C = 50 \times 36.06 = 1.8mA$$

$$I_E = (1 + 50)36 = 1.836 mA$$

$$I_E R_E + V_{BE} + I_B R_B = V_{CC}$$

$$V_E = I_E R_E = 1.836 \times 240 = 440.64mV$$

$$(I_B + I_C)R_E + V_{BE} + I_B R_B = V_{CC}$$

$$V_C = V_{CC} - (I_C)R_C = 5 - 1.8 \times 1.25$$

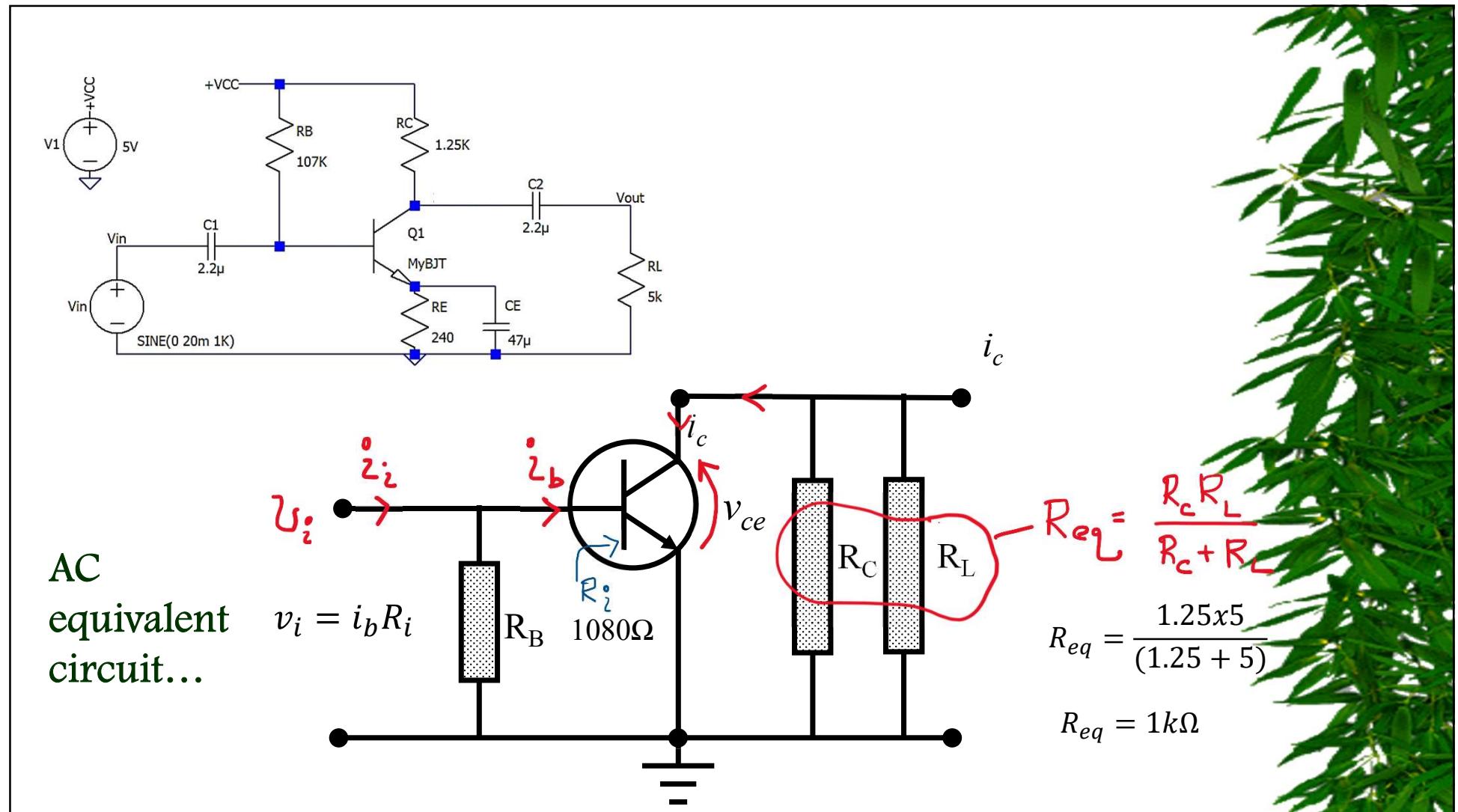
$$(1 + \beta)I_B R_E + V_{BE} + I_B R_B = V_{CC}$$

$$= 2.75 V$$

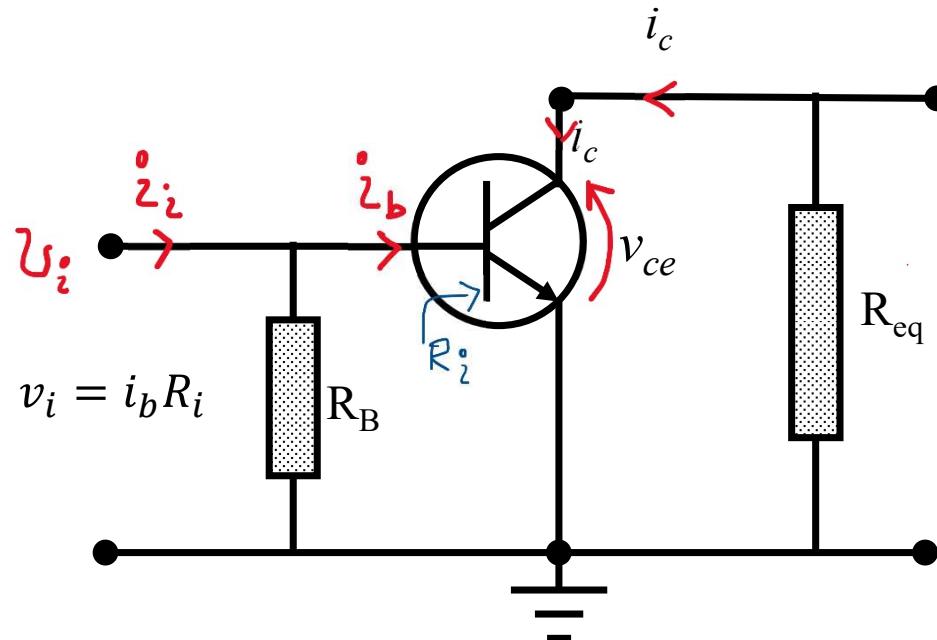
$$V_{BE} + I_B [R_B + (1 + \beta)R_E] = V_{CC}$$

$$V_{CE} = V_C - V_E = 2.75 - 0.4406 = 2.31mV$$





## AC load line



Applying KCL for input side...

$$i_i = i_b + \frac{v_i}{R_B} = i_b \left( 1 + \frac{R_i}{R_B} \right)$$

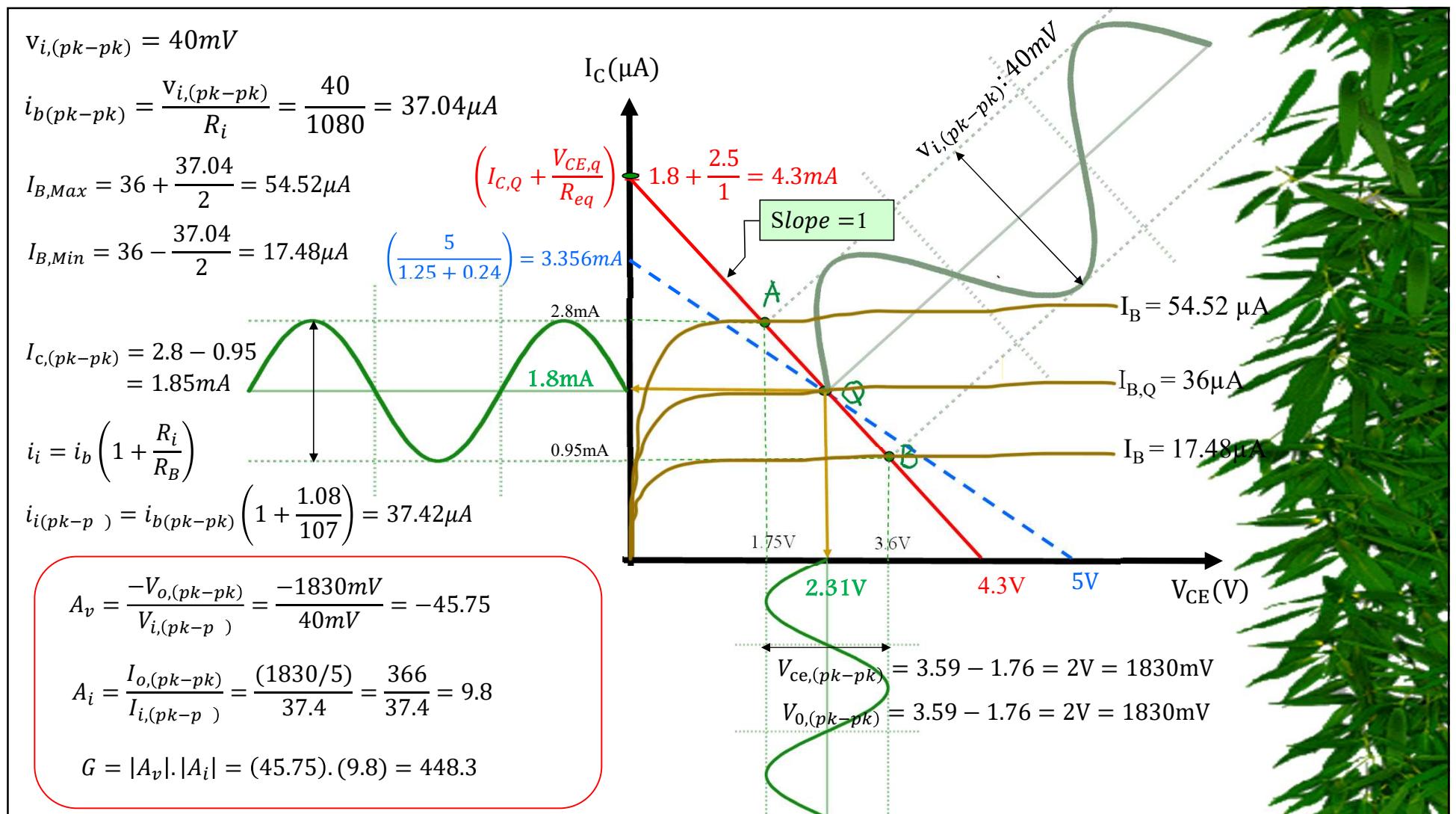
Applying KVL for output side...

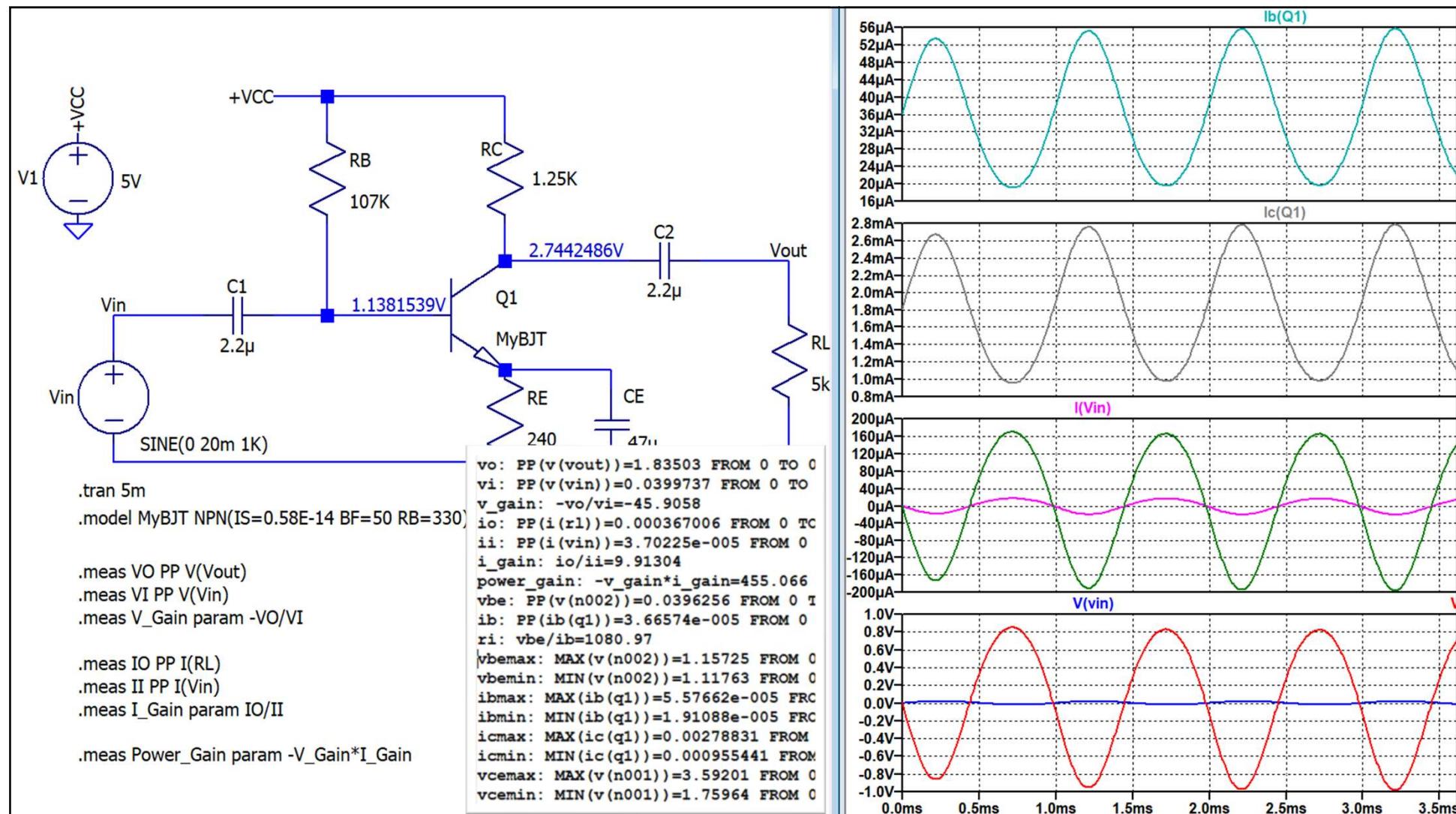
$$v_{ce} + i_c R_{eq} = 0$$

$$i_c = \left( \frac{-1}{R_{eq}} \right) v_{ce}$$

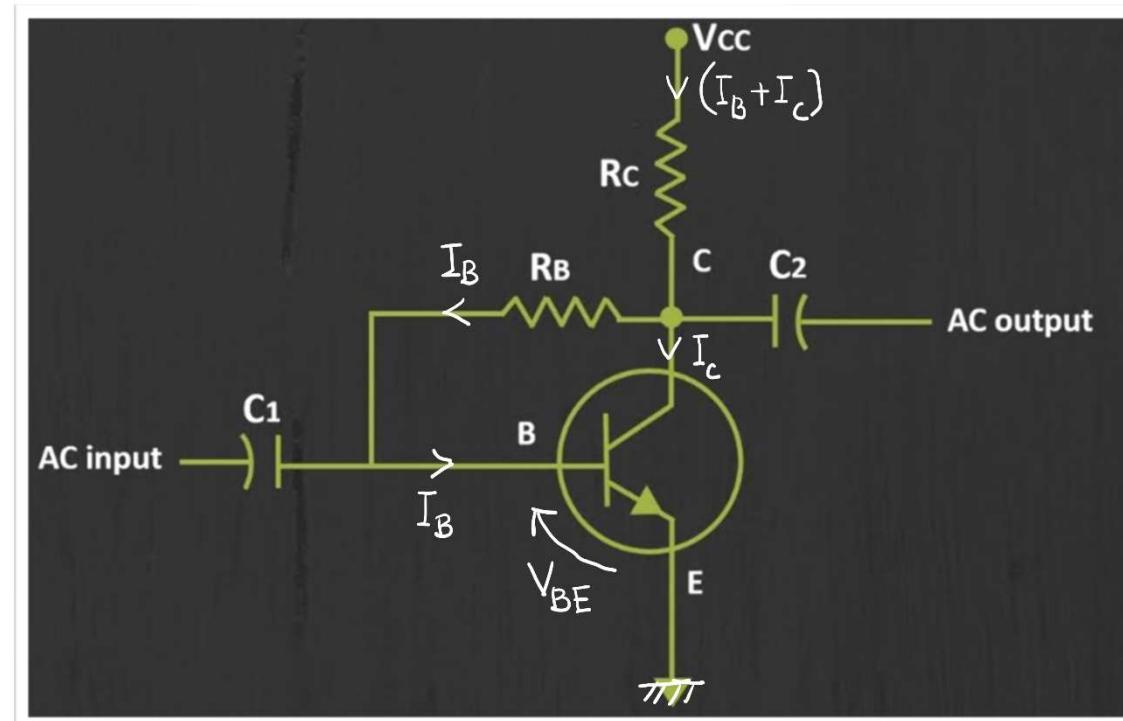
$$\text{Gradient of AC load line} = \left( \frac{-1}{R_{eq}} \right)$$





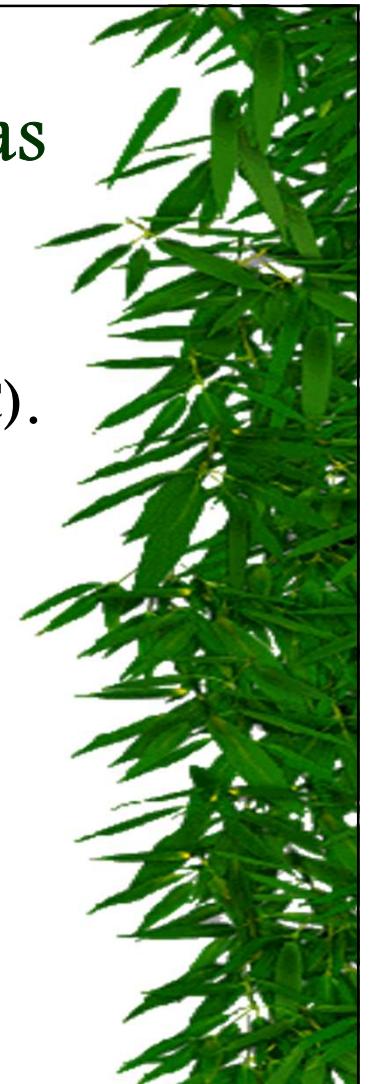


## Collector-to-Base Bias / Collector Feedback bias

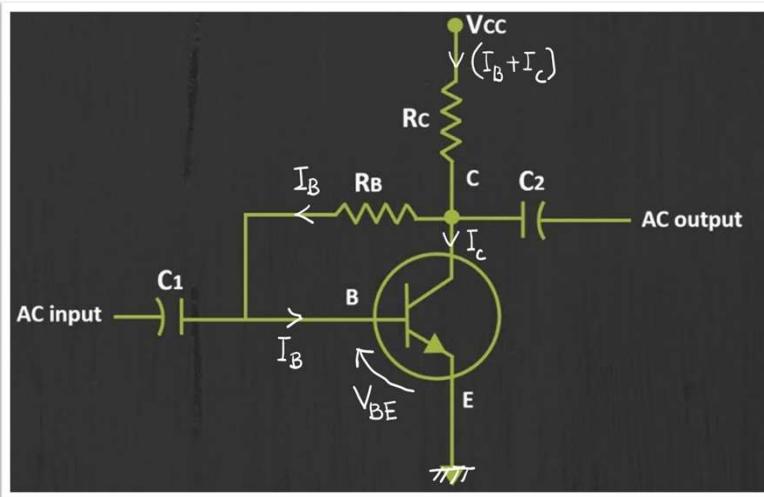


## Collector-to-Base Bias / Collector Feedback bias

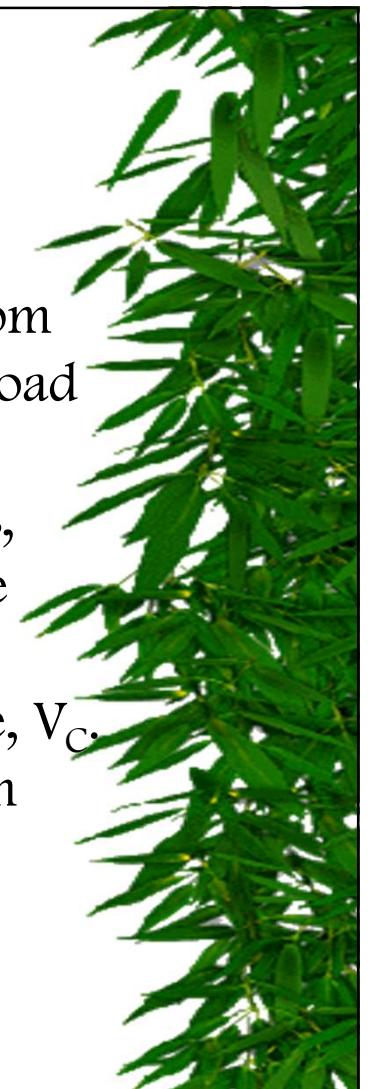
- The base bias resistor,  $R_B$  is connected to the collector (C). Not to the supply voltage rail,  $V_{CC}$ .
- The DC base bias voltage is derived from the collector voltage  $V_C$ , thus providing good stability.
- This ensures that the transistor is always biased in the active region irrespective of the value of Beta ( $\beta$ ).



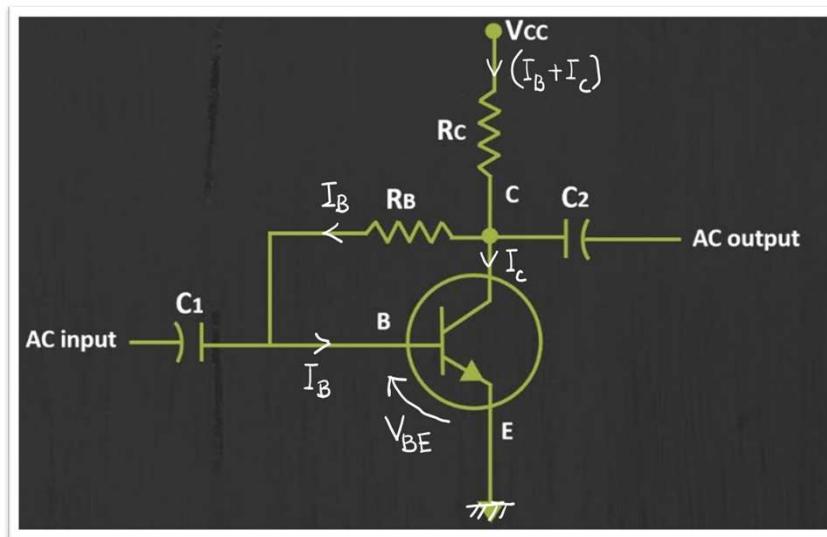
## Stability in Collector-to-Base Bias



- Biasing voltage is derived from the voltage drop across the load resistor  $R_L$
- If the load current increases, there will be a larger voltage drop across  $R_L$ 
  - Reduced collector voltage,  $V_C$ .
  - Base current  $I_B$  reduces in turn
  - $I_C$  is stabilized



## Collector-to-Base Bias/Collector Feedback bias

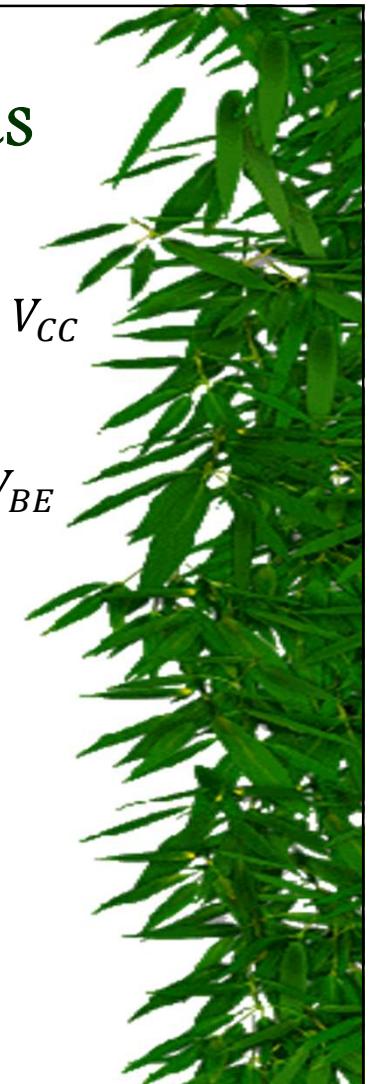


$$V_{BE} + I_B R_B + (1 + \beta) I_B R_C = V_{CC}$$

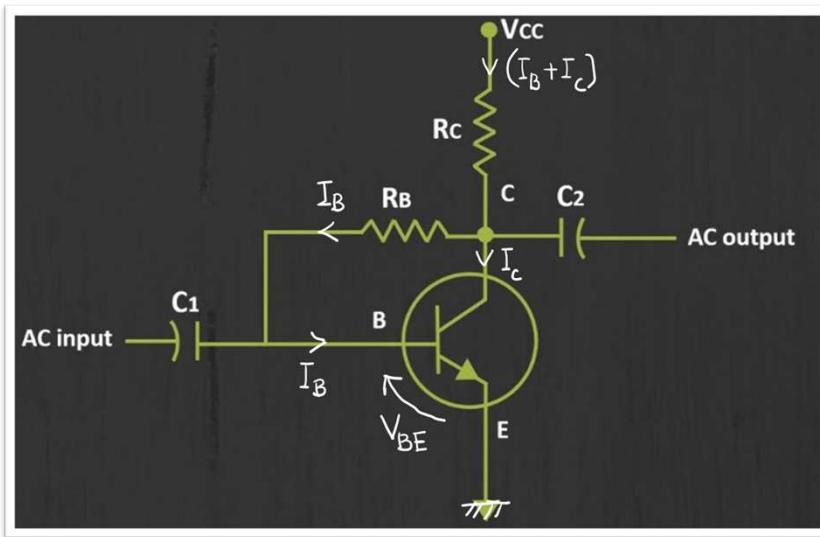
$$I_B (R_B + (1 + \beta) R_C) = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_C}$$

$$V_{BE} + I_B R_B + (I_B + I_C) R_C = V_{CC}$$



## Collector-to-Base Bias/Collector Feedback bias



$$V_{CE} + (I_B + I_C)R_C = V_{CC}$$

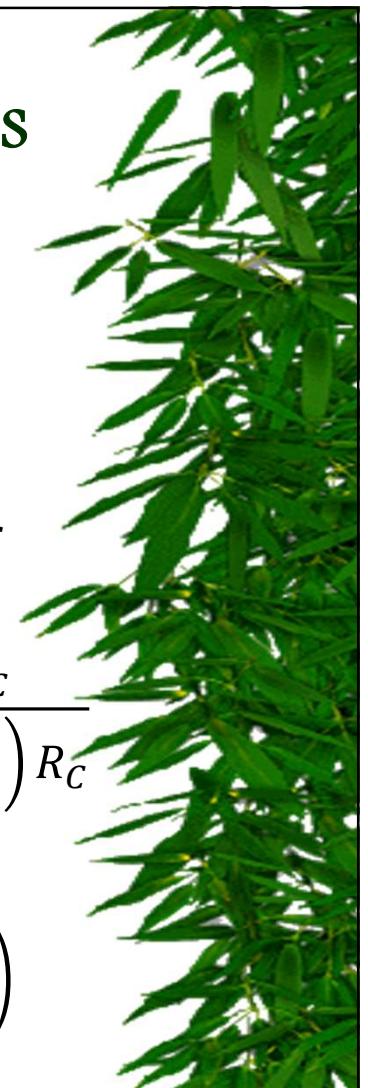
$$V_{CE} + I_C \left( \frac{I_B}{I_C} + 1 \right) R_C = V_{CC}$$

$$V_{CE} + I_C \left( \frac{1}{\beta} + 1 \right) R_C = V_{CC}$$

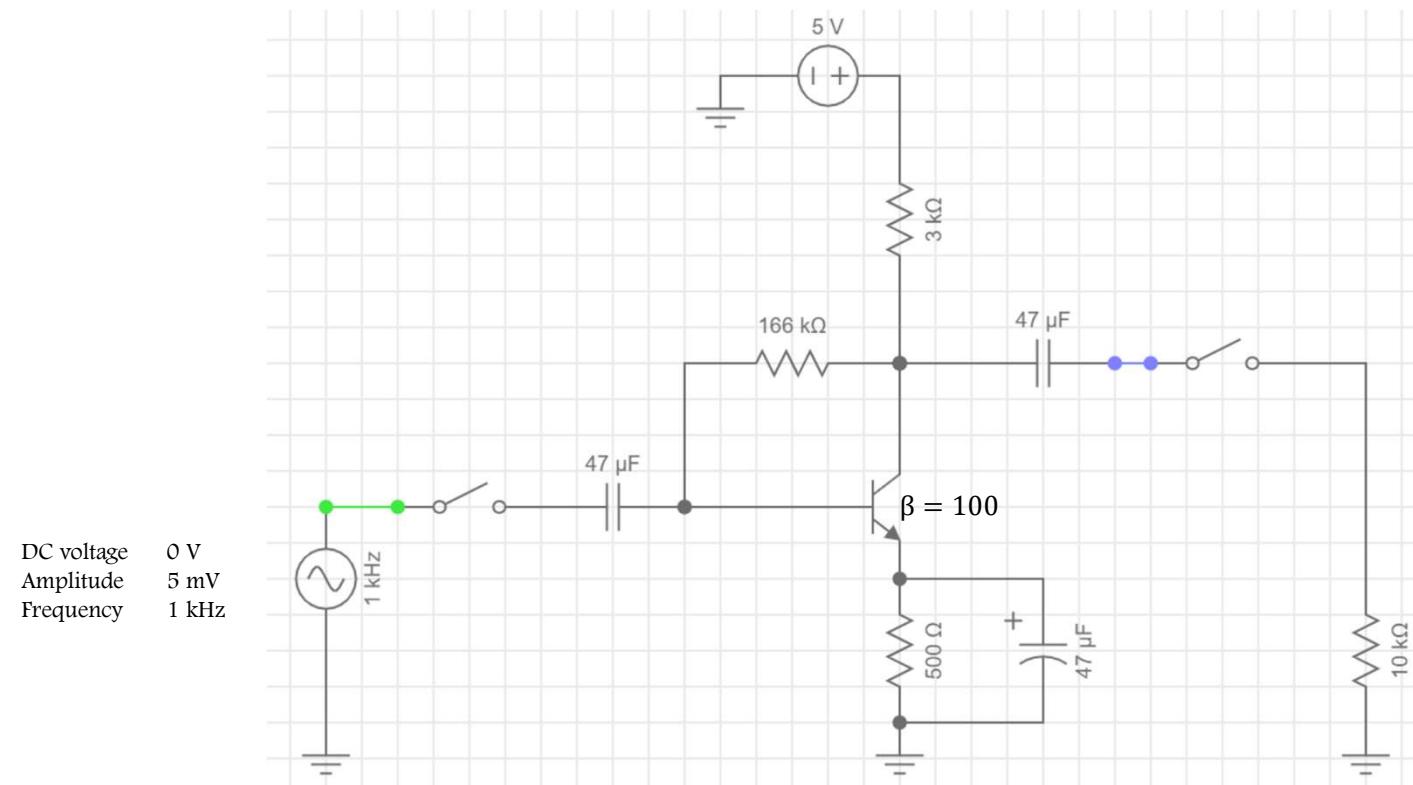
$$I_C \left( \frac{1}{\beta} + 1 \right) R_C = -V_{CE} + V_{CC}$$

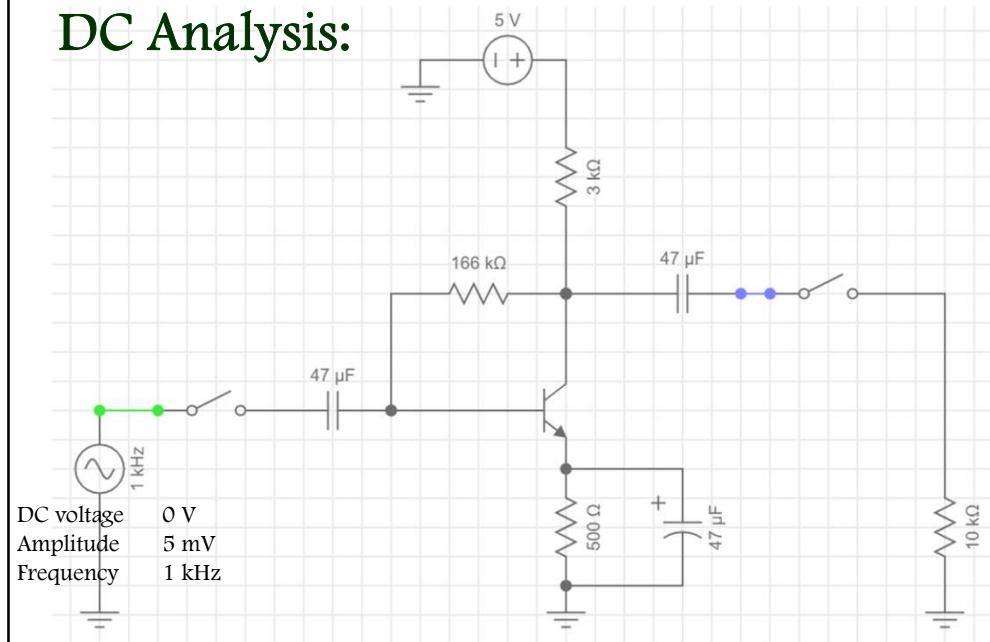
$$I_C = -\frac{1}{\left( \frac{1}{\beta} + 1 \right) R_C} V_{CE} + \frac{V_{CC}}{\left( \frac{1}{\beta} + 1 \right) R_C}$$

$$I_C \approx -\left( \frac{1}{R_C} \right) V_{CE} + \left( \frac{V_{CC}}{R_C} \right)$$



# Tutorial Question



**DC Analysis:**

$$I_B = \frac{5 - 0.7}{519.5} \quad I_B = 8.28 \mu A$$

$$I_C = 828 \mu A$$

$$\begin{aligned} V_E &= (I_B + I_C)R_E \\ &= (8.28 + 828)\mu A \times 500\Omega \\ &= 418 mV \end{aligned}$$

$$\begin{aligned} V_C &= V_{CC} - (I_B + I_C)R_C \\ &= 5 - 3.(0.8363) \\ &= 2.49 V \end{aligned}$$

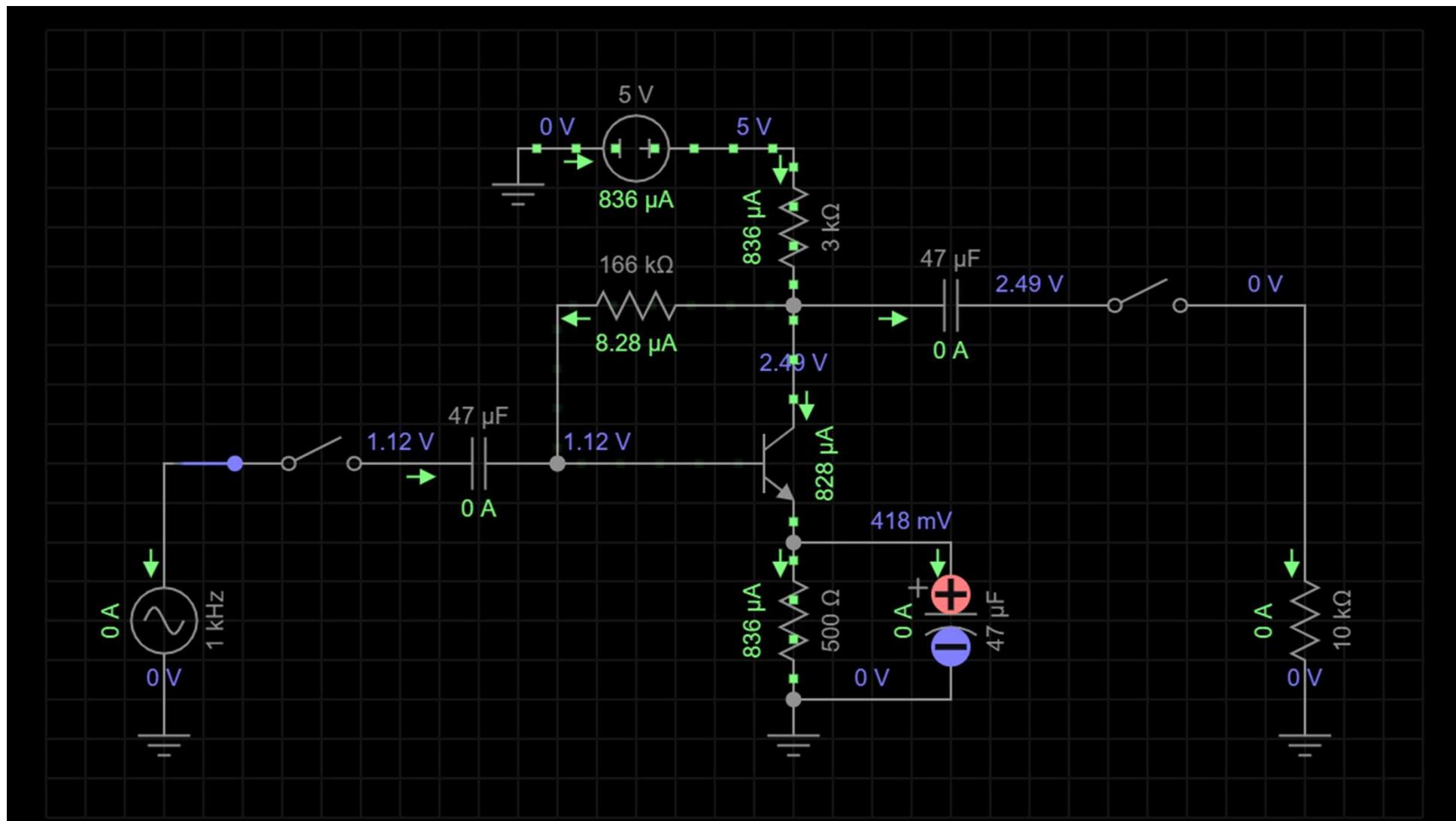
$$\begin{aligned} V_{CE} &= V_C - V_E \\ &= 2.072 V \end{aligned}$$



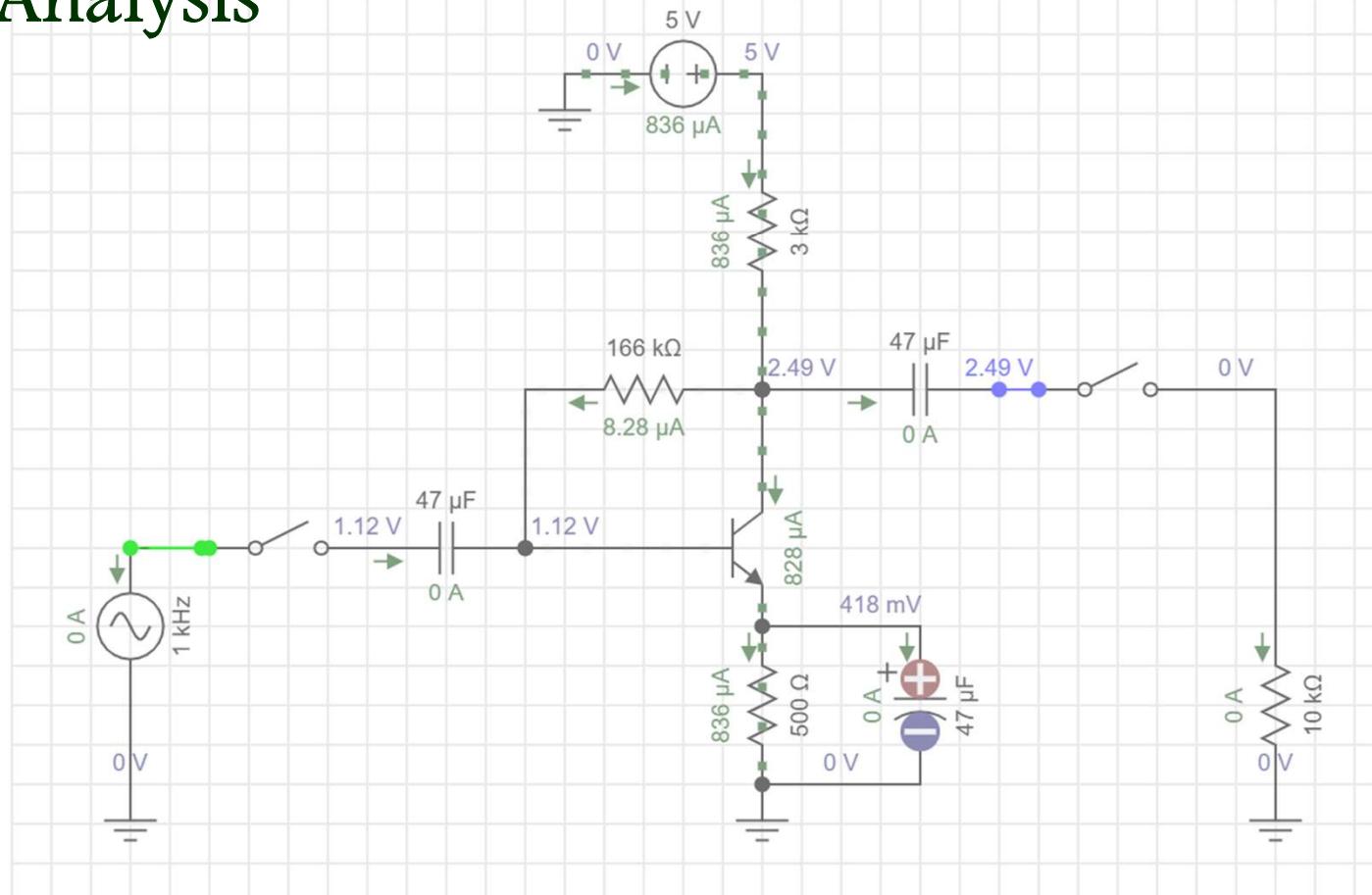
$$V_{BE} + I_B R_B + (I_B + I_C)(R_C + R_E) = V_{CC}$$

$$0.7 + 166.I_B + (3.5)(I_B + 100I_B) = 5$$

$$519.5.I_B = 5 - 0.7$$



# DC Analysis



$$V_{BE} + I_B R_B + (I_B + I_C)(R_C + R_E) = V_{CC}$$

$$0.7 + 166 \cdot I_B + (3.5)(I_B + 100I_B) = 5$$

$$519.5 \cdot I_B = 5 - 0.7$$

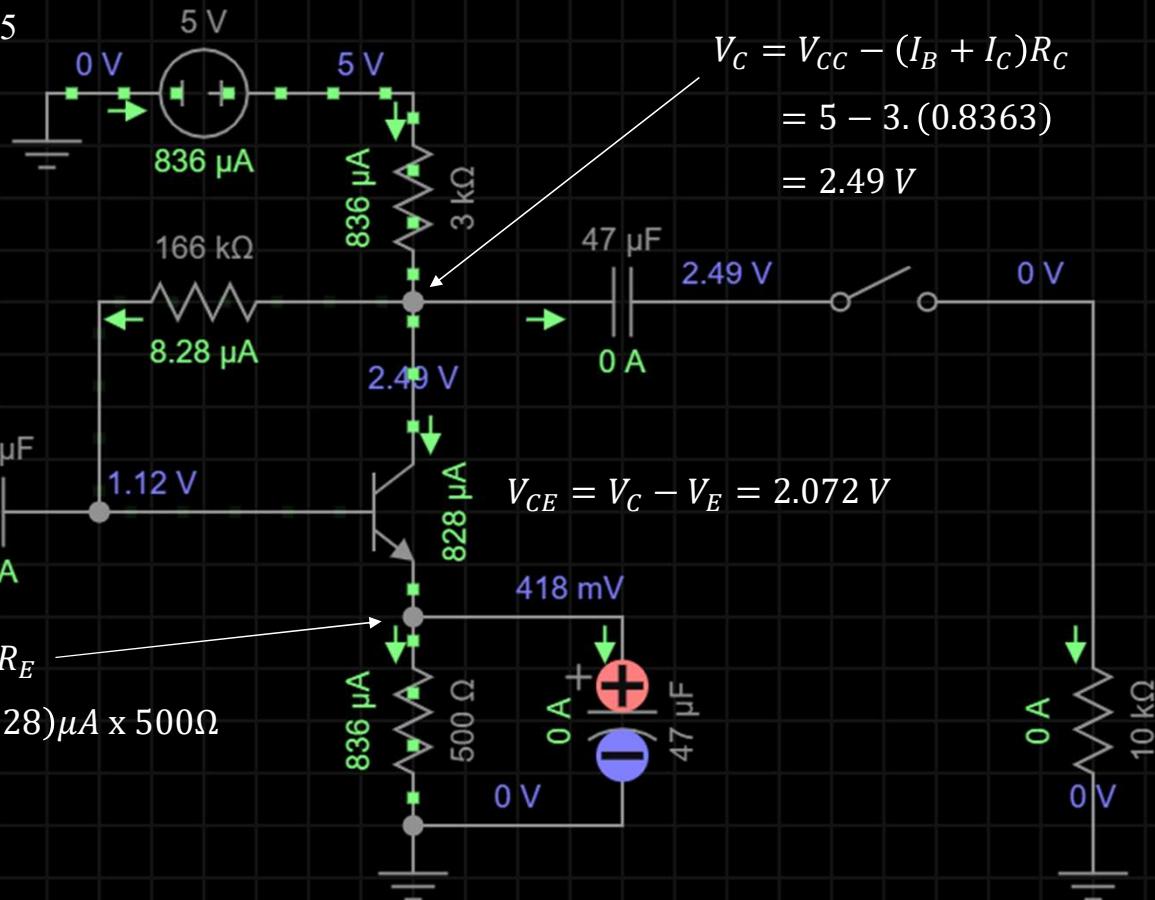
$$I_B = \frac{5 - 0.7}{519.5}$$

$$I_B = 8.28 \mu A$$

$$I_C = 828 \mu A$$



$$\begin{aligned} V_E &= (I_B + I_C)R_E \\ &= (8.28 + 828)\mu A \times 500\Omega \\ &= 418 mV \end{aligned}$$



$$V_C = V_{CC} - (I_B + I_C)R_C$$

$$= 5 - 3 \cdot (0.8363)$$

$$= 2.49 V$$

$$V_{CE} = V_C - V_E = 2.072 V$$

## DC Analysis

$$V_{BE} + I_B R_B + (I_B + I_C)(R_C + R_E) = V_{CC}$$

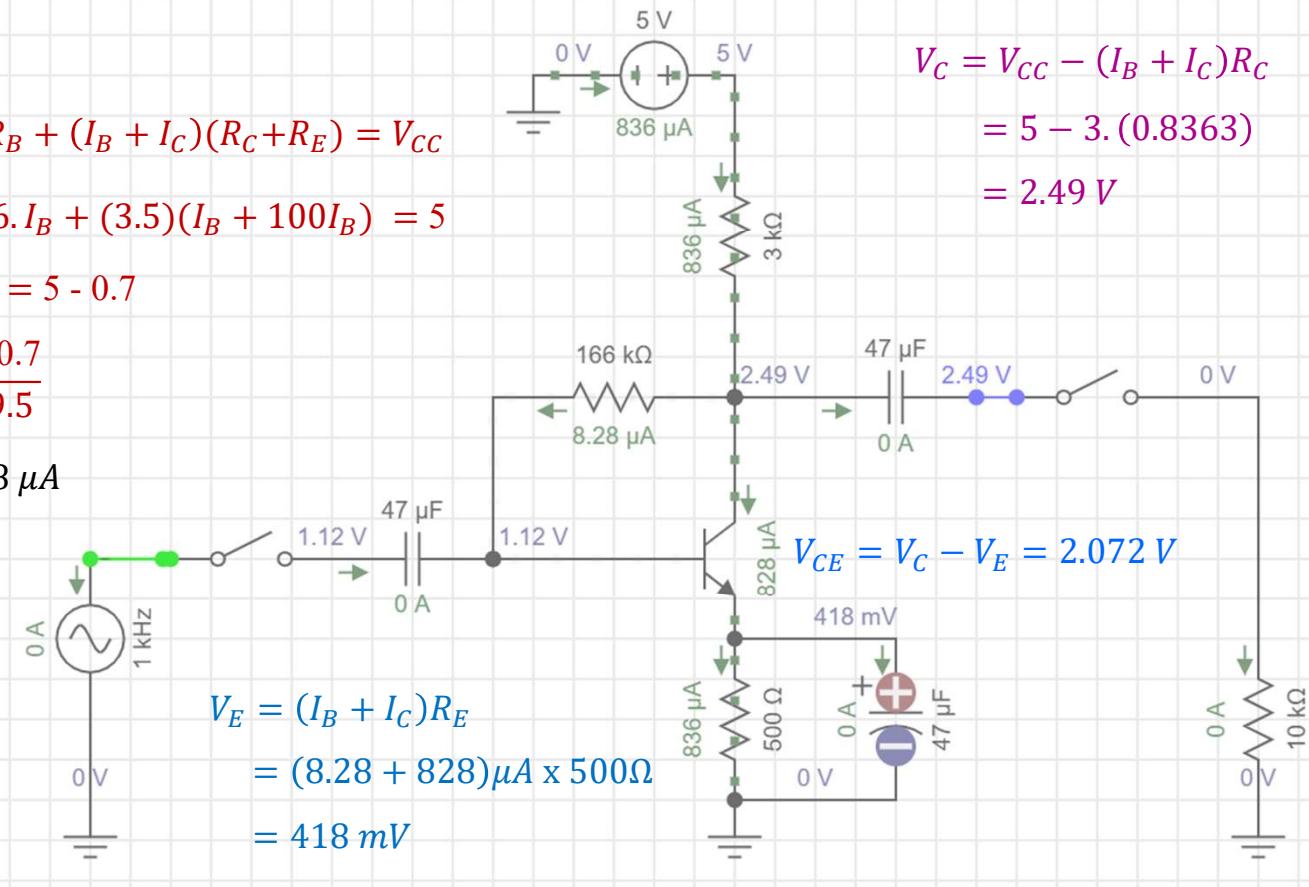
$$0.7 + 166. I_B + (3.5)(I_B + 100I_B) = 5$$

$$519.5. I_B = 5 - 0.7$$

$$I_B = \frac{5 - 0.7}{519.5}$$

$$I_B = 8.28 \mu A$$

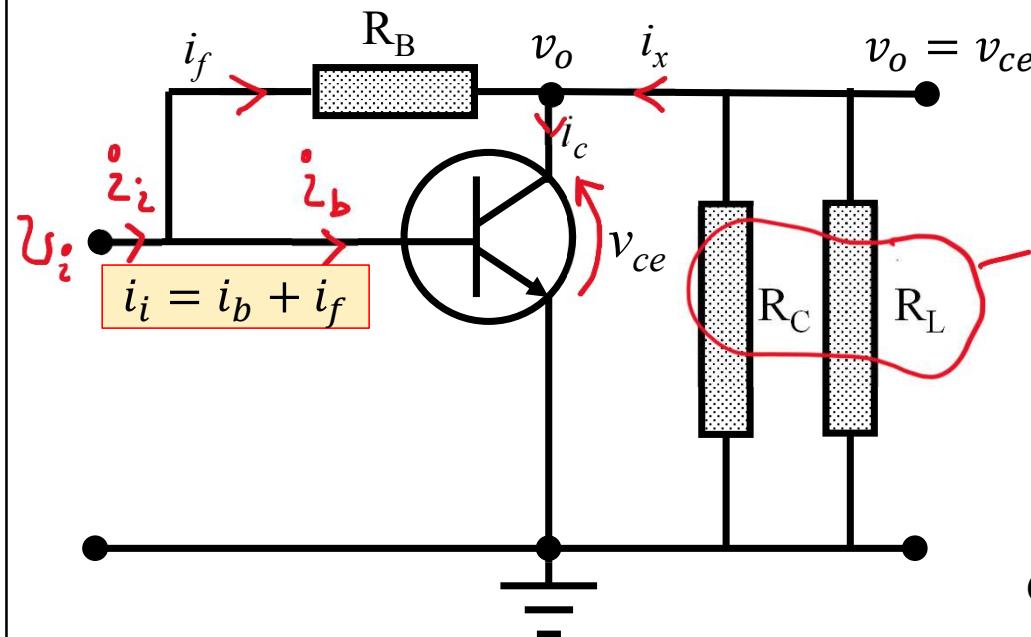
$$\begin{aligned} V_E &= (I_B + I_C)R_E \\ &= (8.28 + 828)\mu A \times 500\Omega \\ &= 418 mV \end{aligned}$$



## AC Analysis

Applying KVL for AC operation...

$$i_f = \frac{v_i - v_o}{R_B}$$



$$v_{ce} + (i_x)R_{eq} = 0$$

$$v_{ce} + (i_c - i_x)R_{eq} = 0$$

$$v_{ce} + (i_c)R_{eq} = 0$$

$$R_{eq} = \frac{R_C R_L}{R_C + R_L}$$

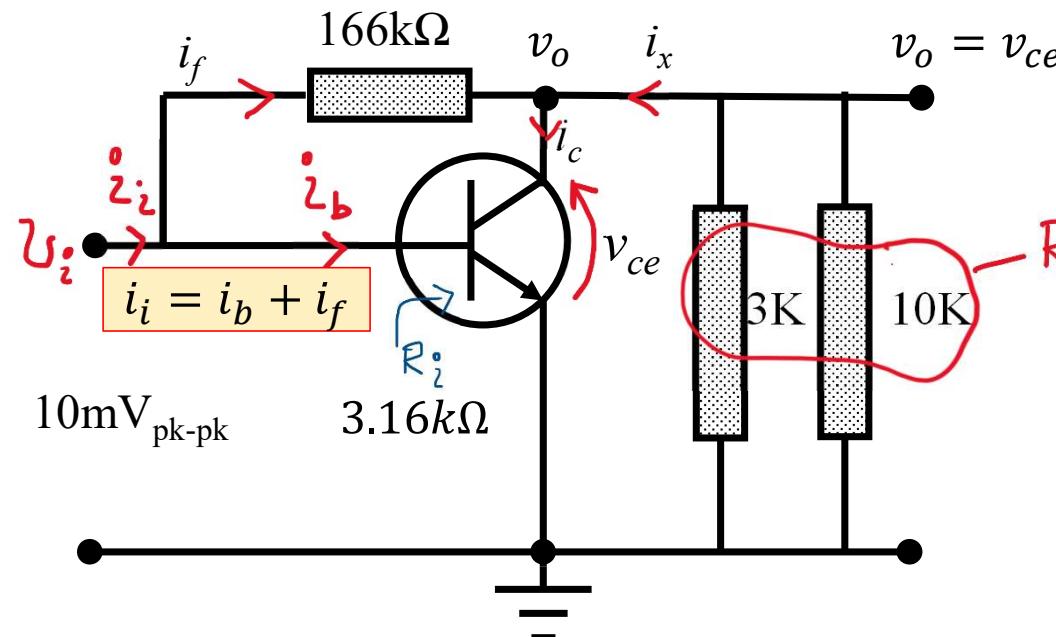
$$i_c = \left( \frac{-1}{R_{eq}} \right) v_{ce}$$

$$\text{Gradient of AC load line} = \left( \frac{-1}{R_{eq}} \right)$$



## AC Analysis

$$i_f = \frac{10 - v_o}{166}$$



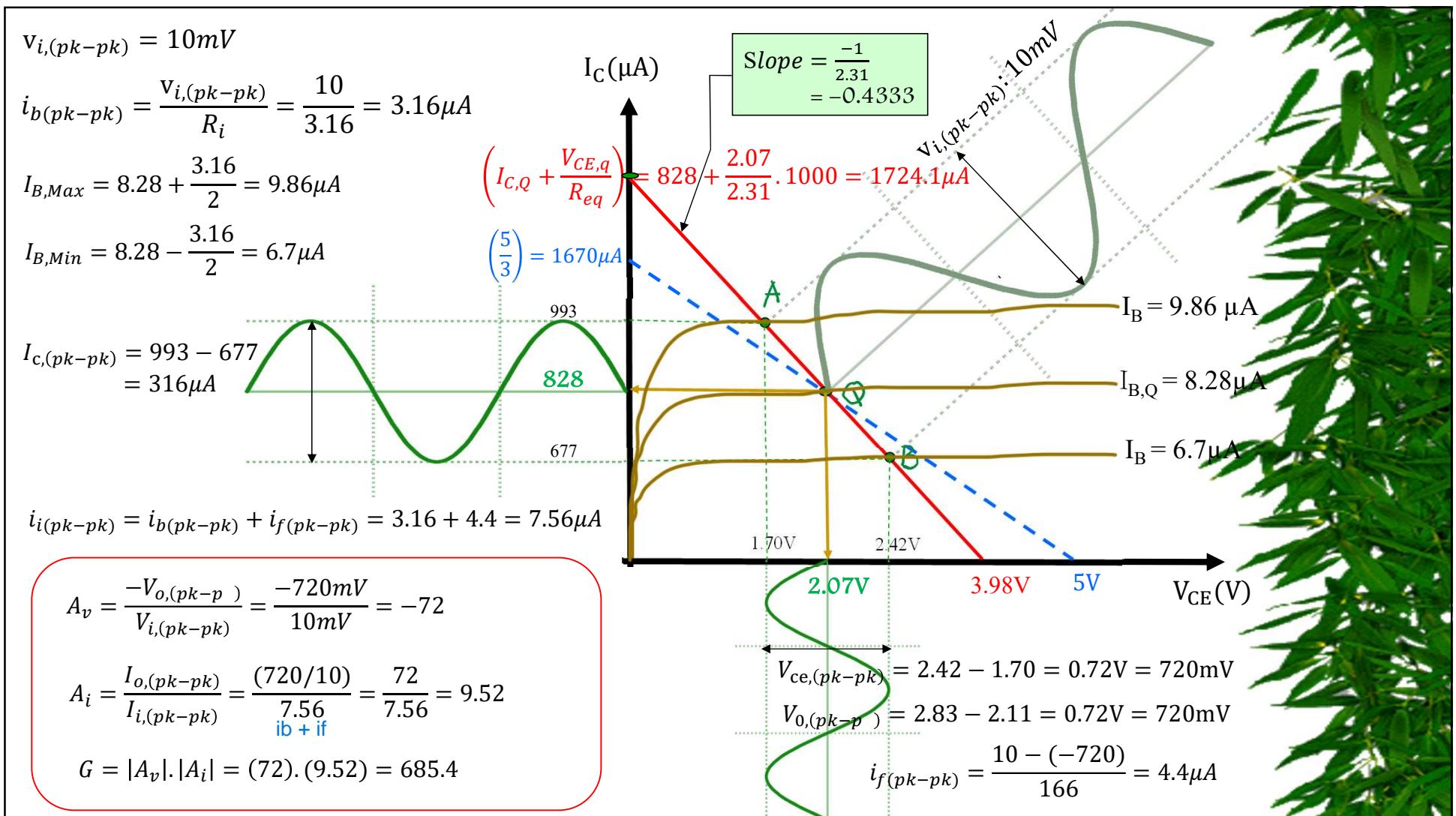
$$R_{eq} = \frac{R_c R_L}{R_c + R_L} = \frac{30}{13} = 2.31\text{k}\Omega$$

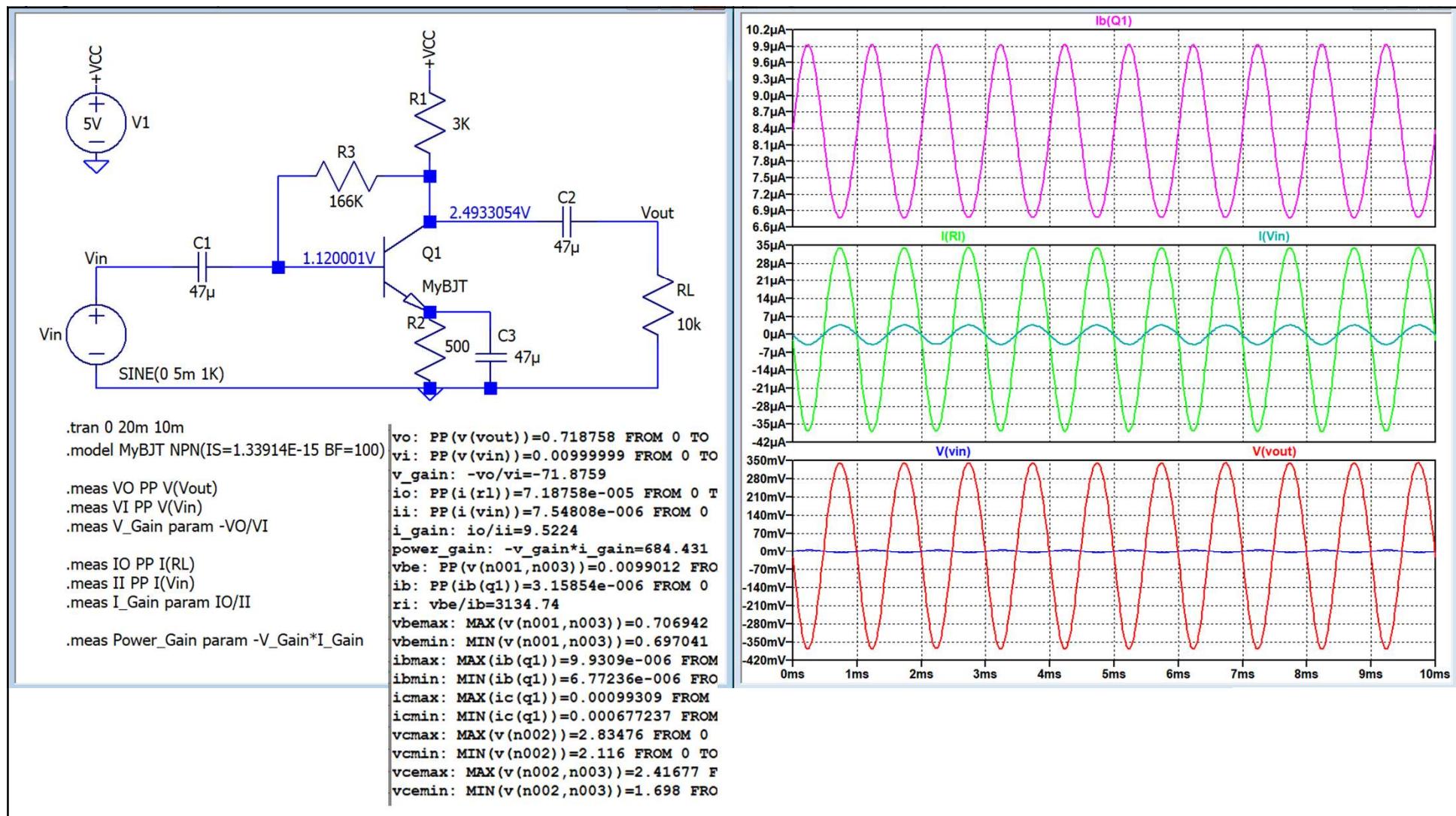
Gradient of AC load line

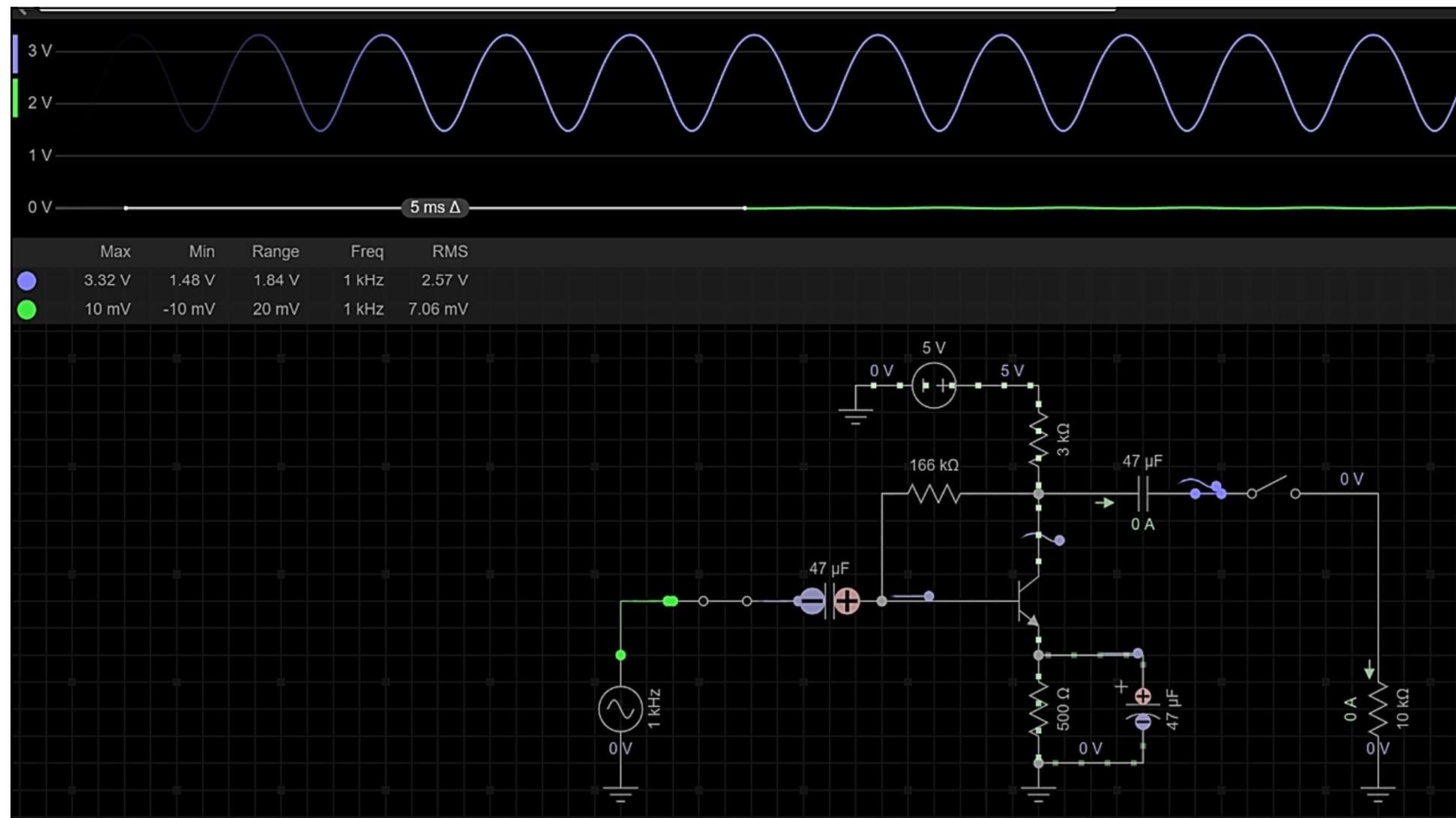
$$= \left( \frac{-1}{R_{eq}} \right)$$

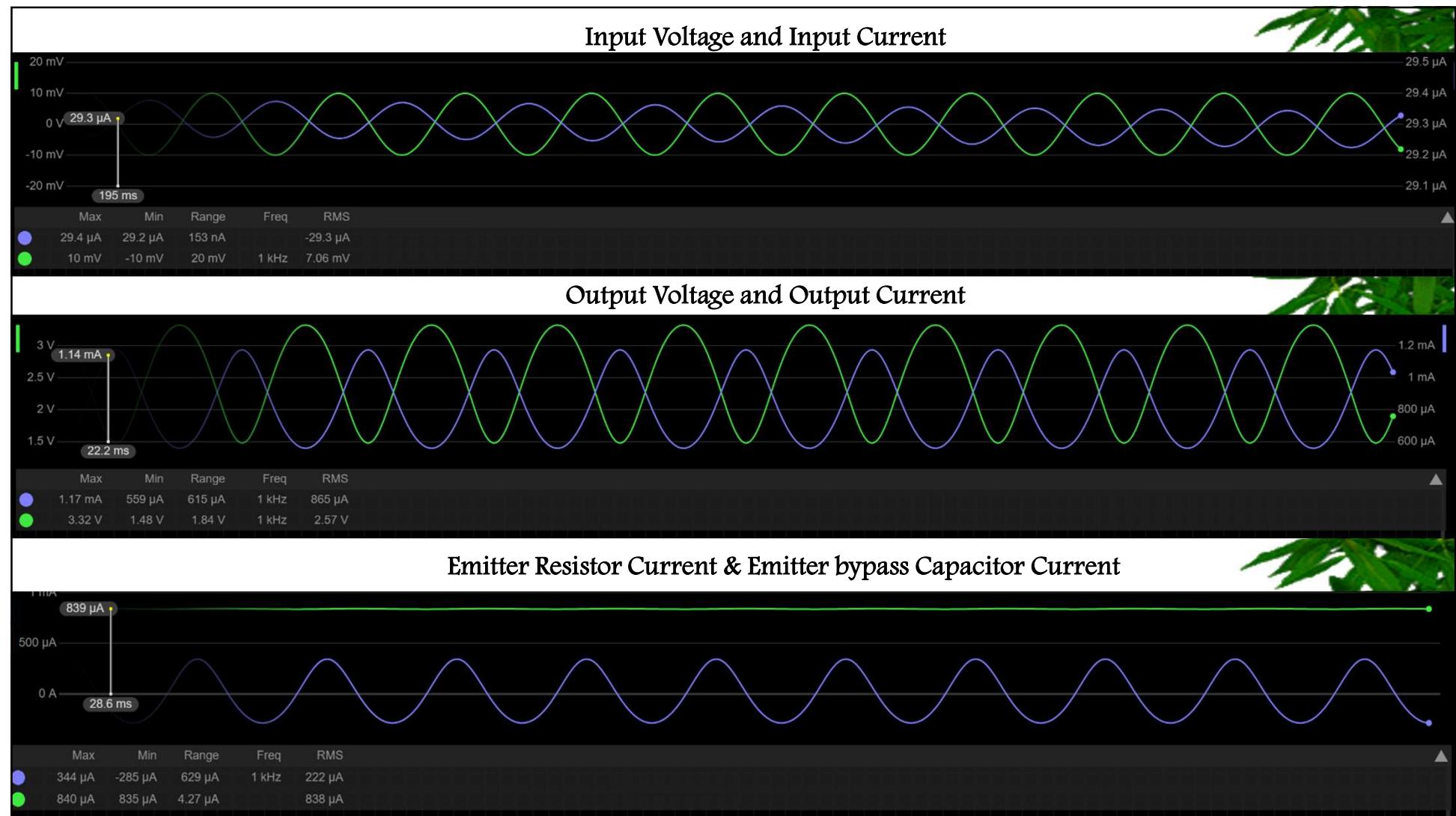
$$= -0.4333$$









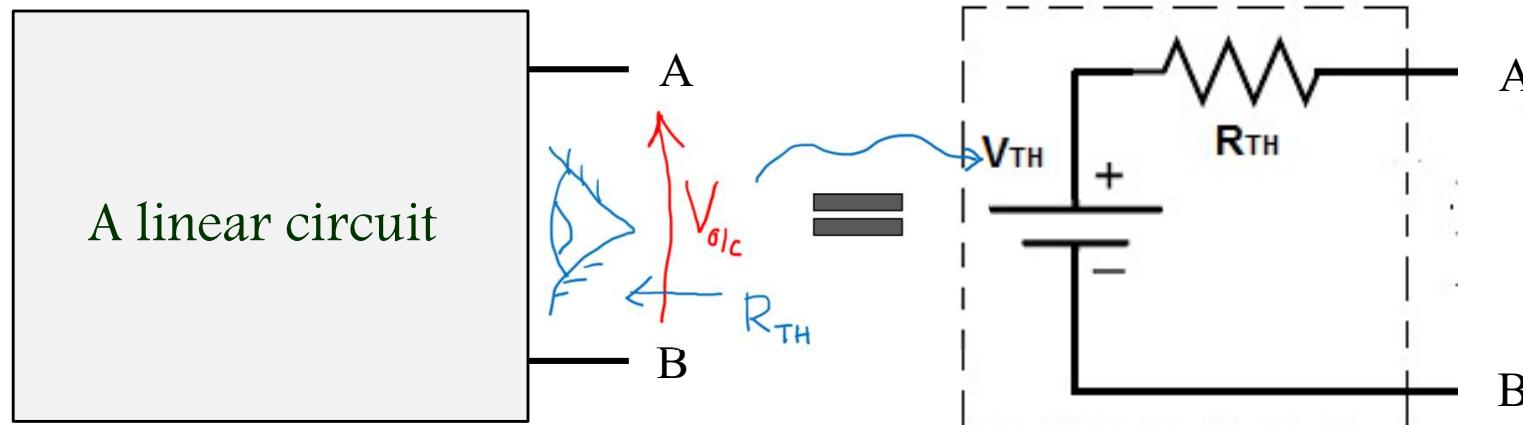


# Potential Divider Bias



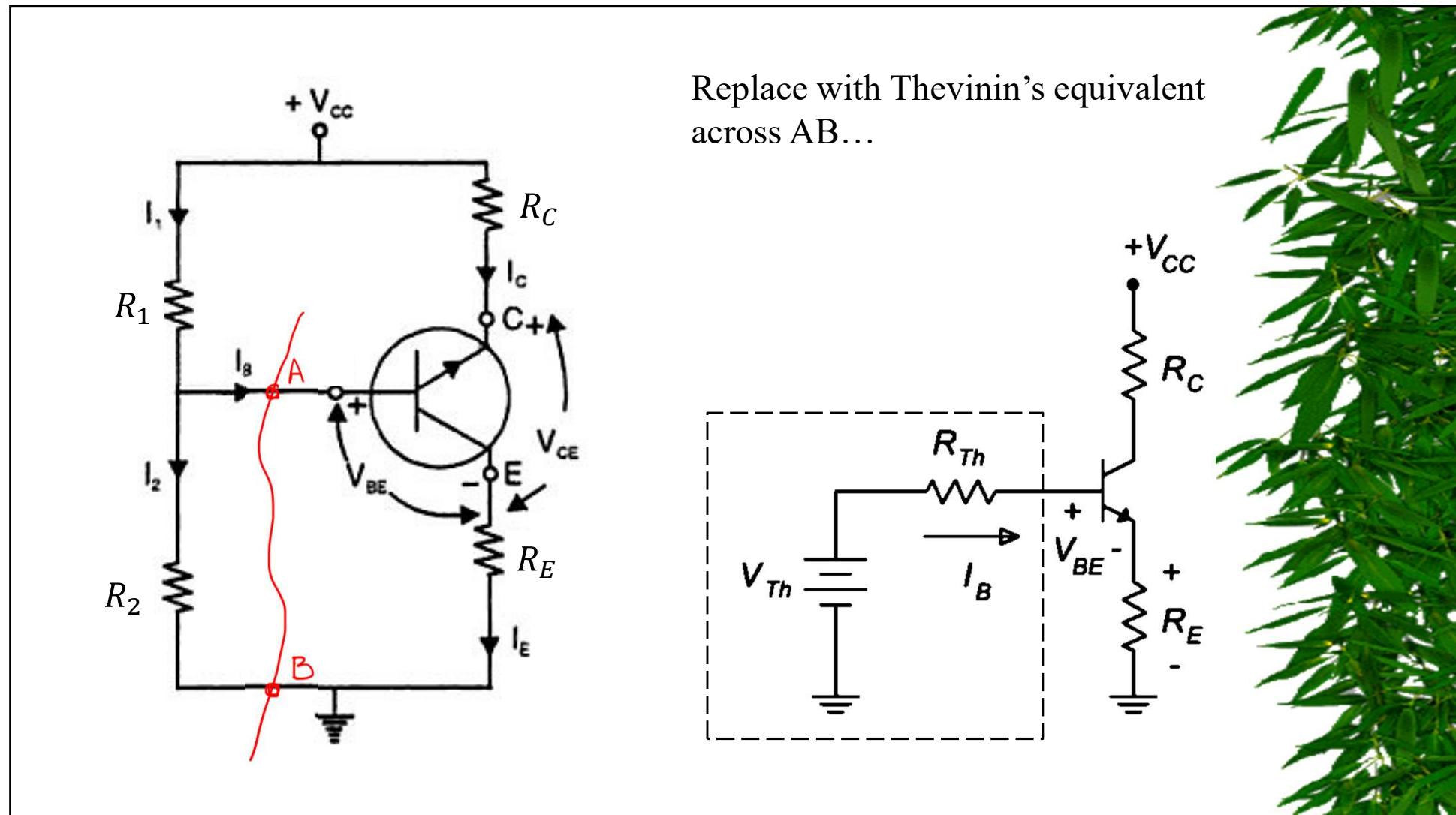
# Thevenin's Theorem

It is possible to simplify any linear circuit, irrespective of how complex it is, to an equivalent circuit with a single voltage source and a series resistance.

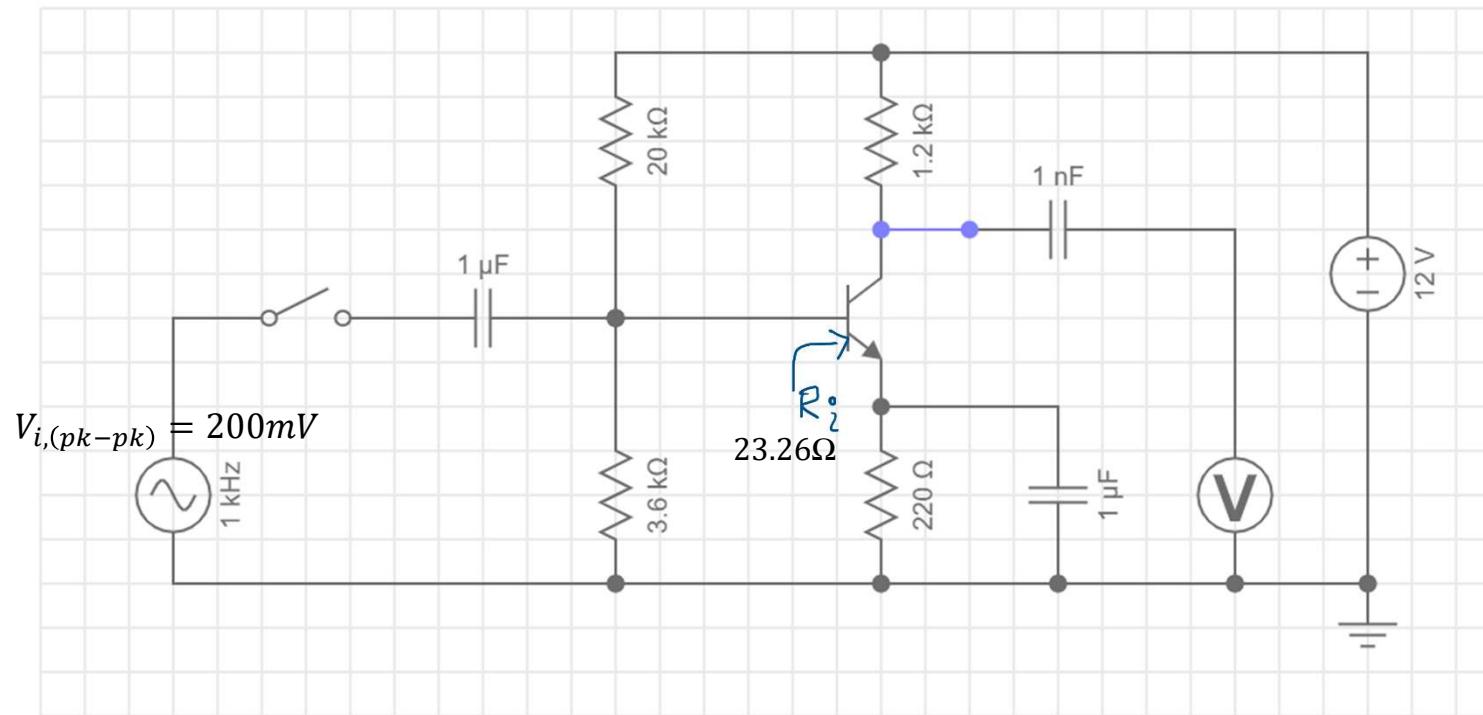


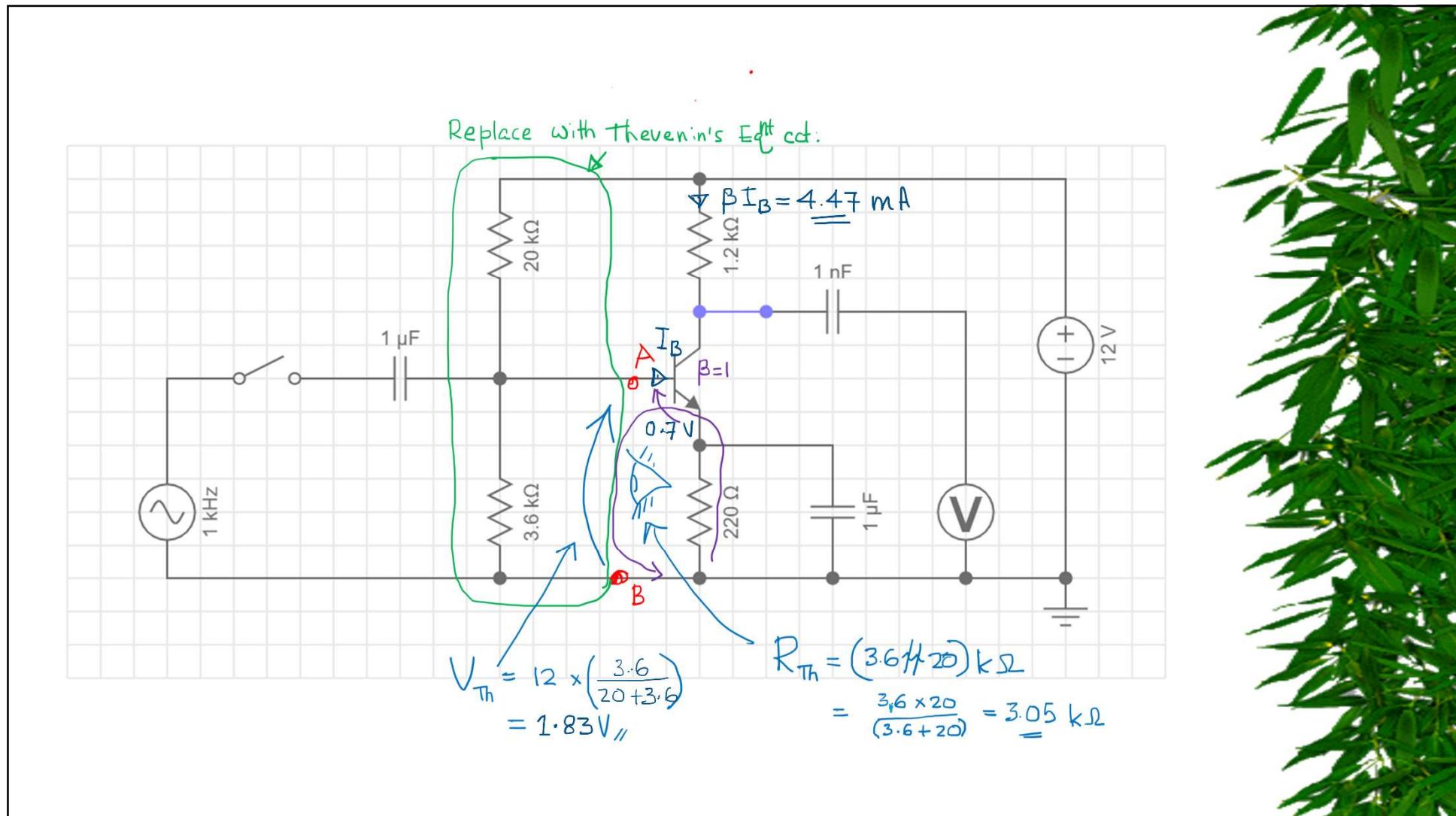
When calculating  $R_{TH}$  first replace all sources with their internal resistance.





# Example





For Loop ① :

Applying KVL :

$$(1+\beta)I_B \cdot R_E + V_{BE} + I_B R_{Th} - V_{Th} = 0$$

$$I_B [101 \times 0.22 + 3.05] = 1.83 - 0.7$$

$$I_B = \frac{1.13}{25.27} = 44.7 \mu A$$

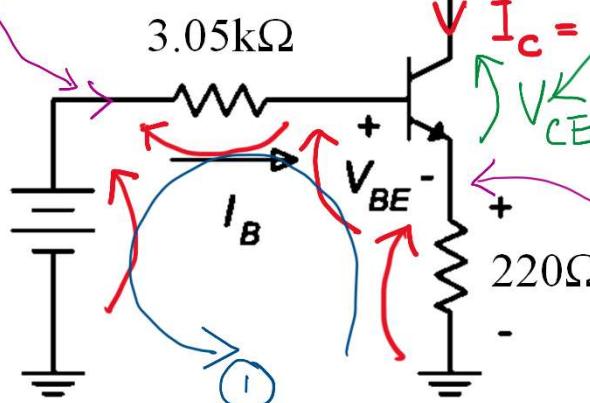
$$V_{Th} = 12 \times \left( \frac{3.6}{20+3.6} \right)$$

$$= 1.83 V$$

$$R_{Th} = (3.6 \parallel 20) k\Omega$$

$$= \frac{3.6 \times 20}{(3.6 + 20)} = 3.05 k\Omega$$

1.83V



$$V_{CE} = 12 - (5.36 + 0.9932)$$

$$= 5.647 V$$

$$I_c = \beta I_B = 100 \times 44.7 \mu A$$

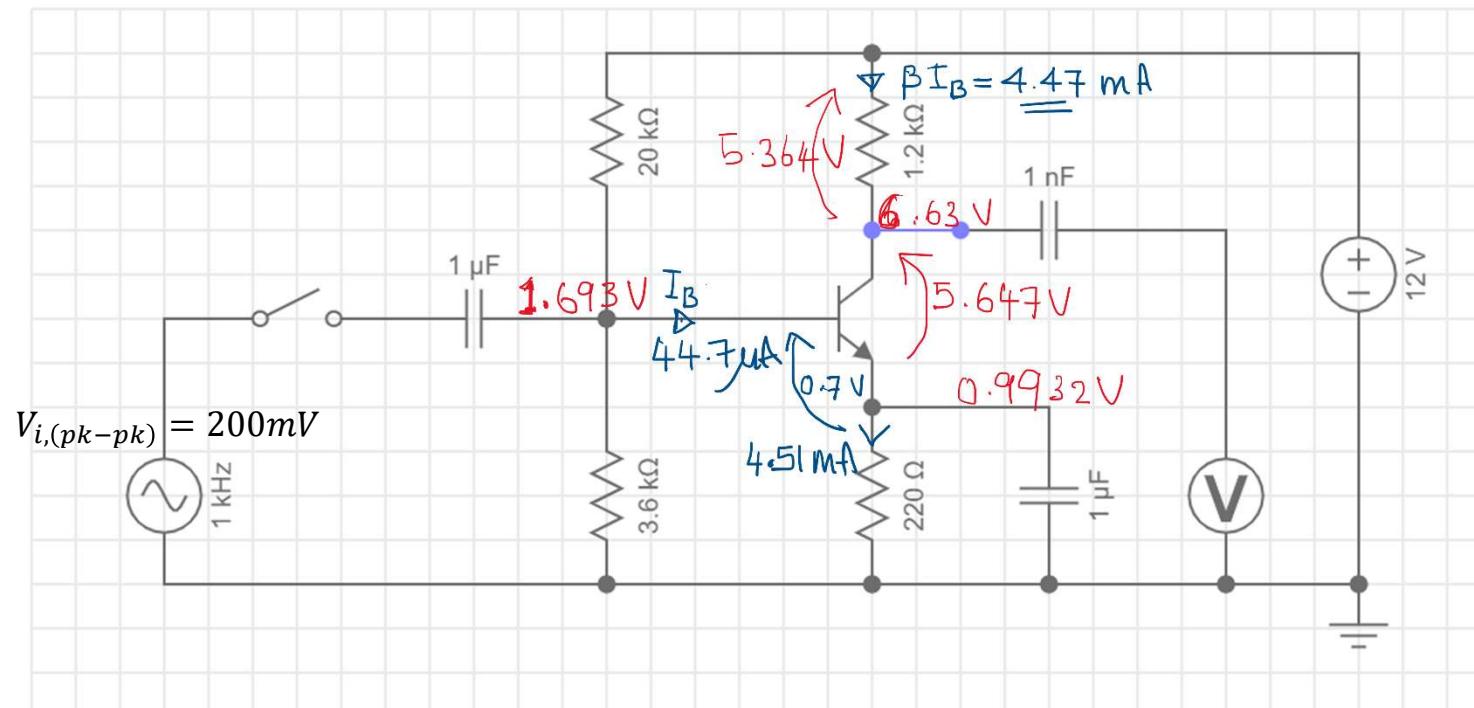
$$= 4.47 mA$$

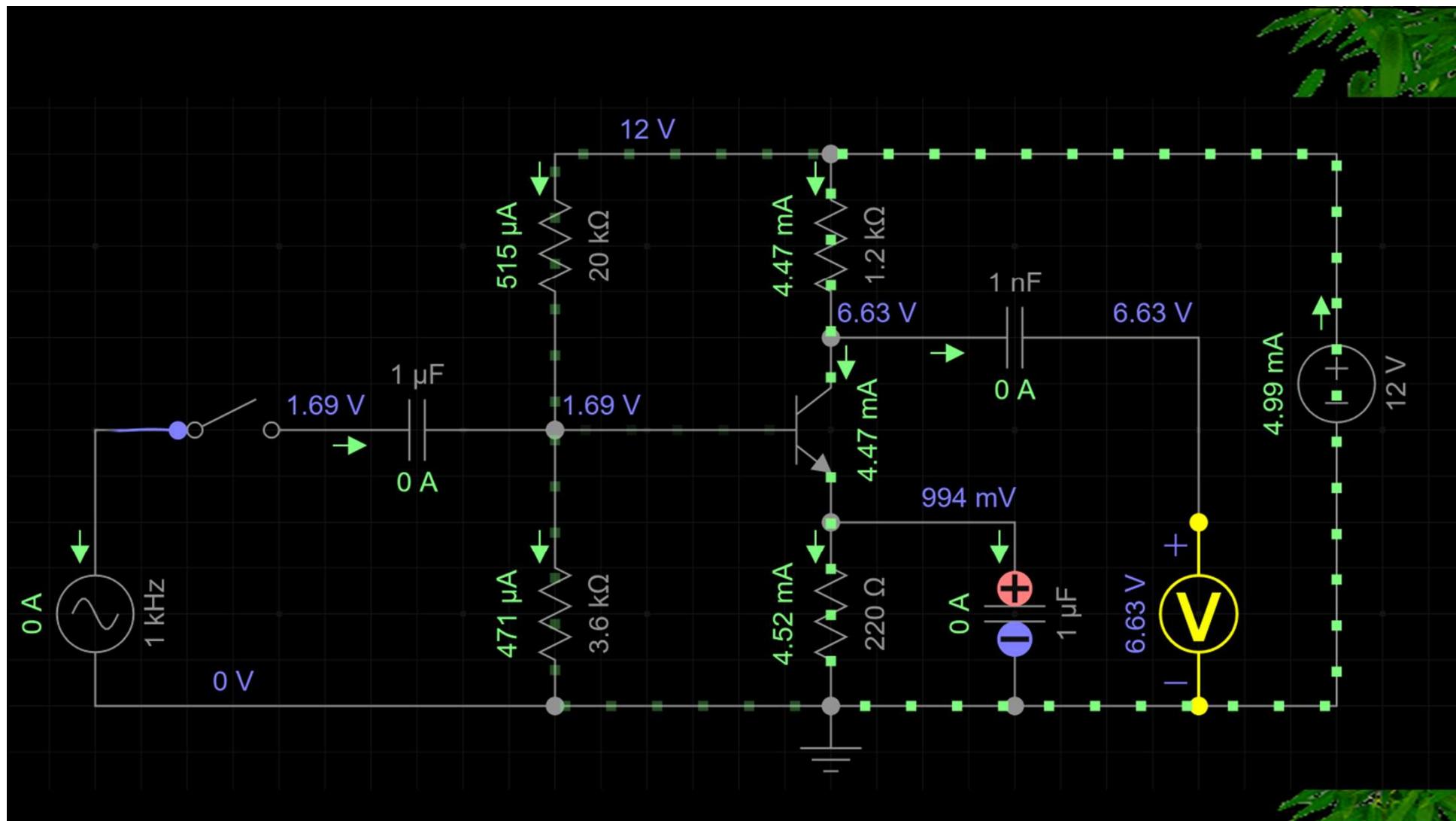
$$V_E = (1+\beta) I_B \times R_E$$

$$= 101 \times 44.7 \times 220 \mu V$$

$$= 0.9932 V$$

## Results of the DC Analysis

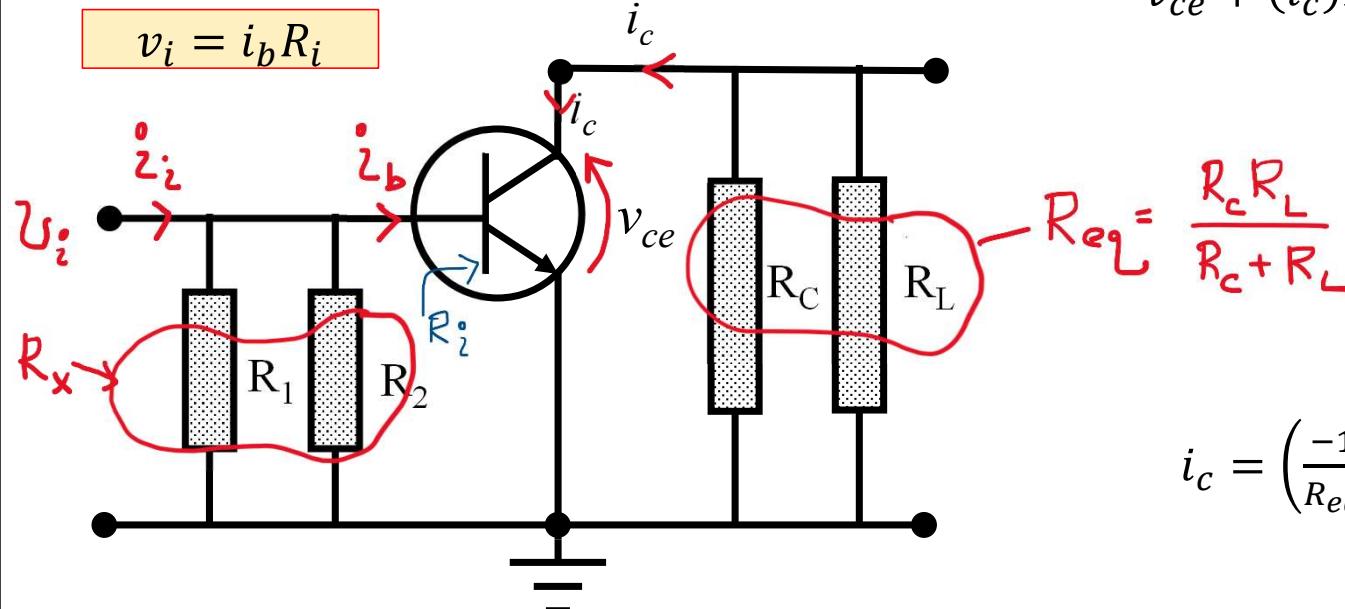




## AC Analysis

$$i_i = i_b + \frac{v_i}{R_X} = i_b \left( 1 + \frac{R_i}{R_X} \right)$$

$$v_i = i_b R_i$$



Applying KVL for AC operation...

$$v_{ce} + (i_c)R_{eq} = 0$$

$$i_c = \left( \frac{-1}{R_{eq}} \right) v_{ce}$$

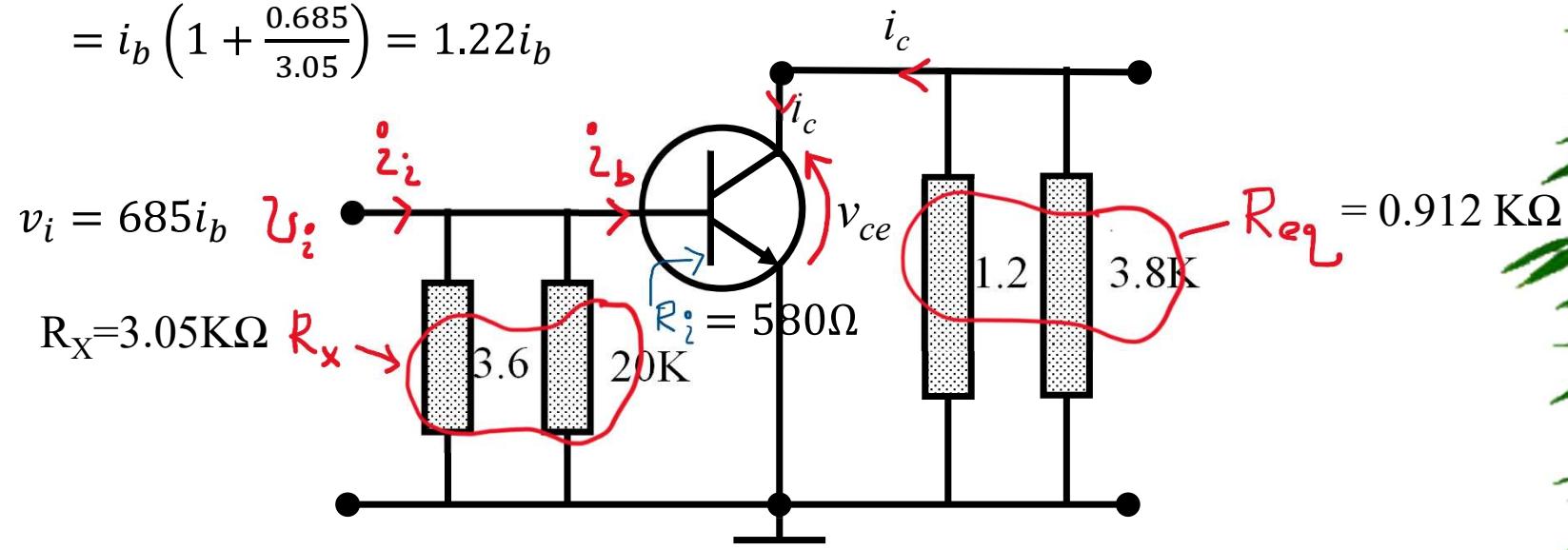
$$\text{Gradient of AC load line} = \left( \frac{-1}{R_{eq}} \right)$$



## AC Analysis

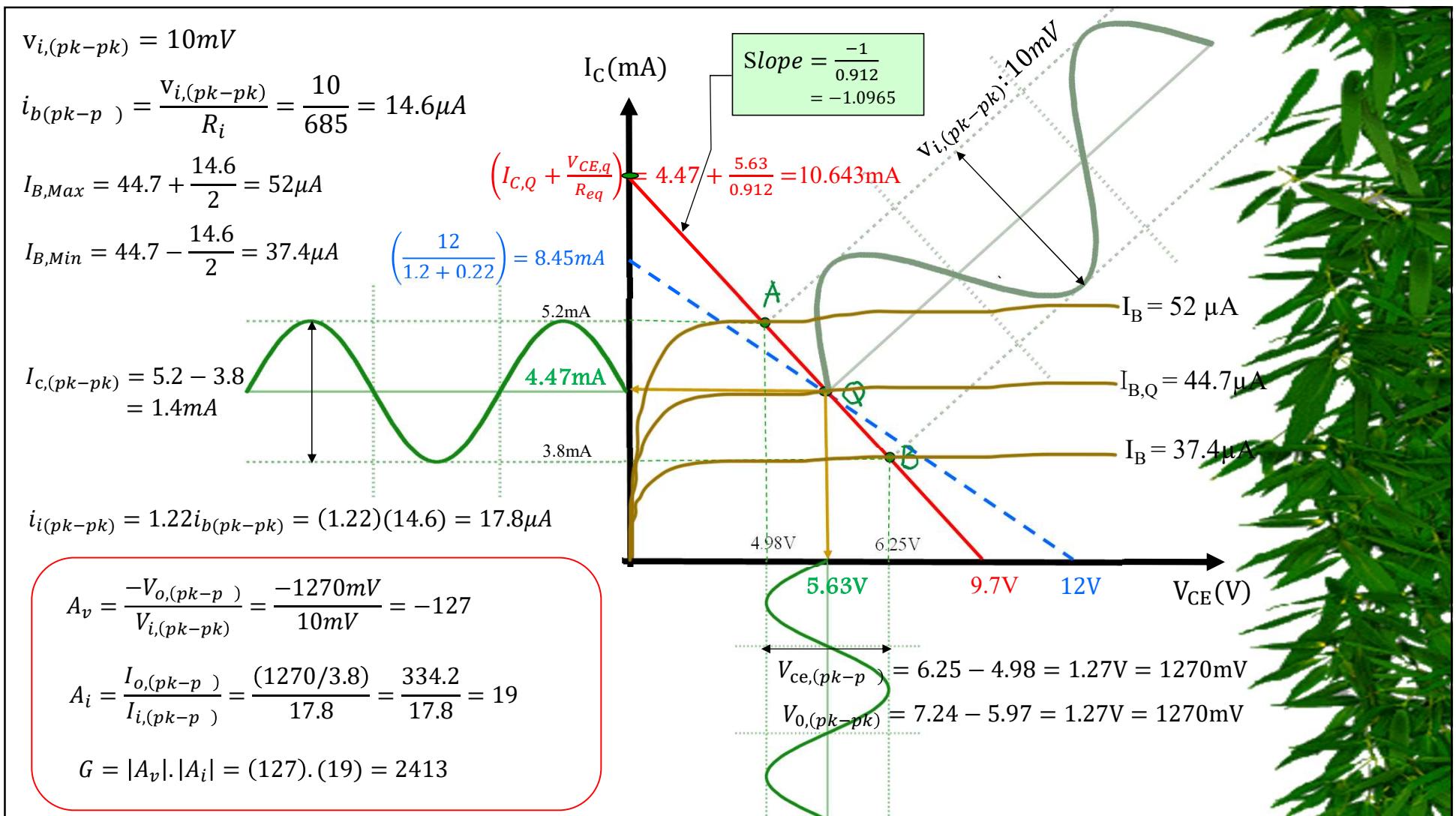
$$i_i = i_b + \frac{v_i}{R_X}$$

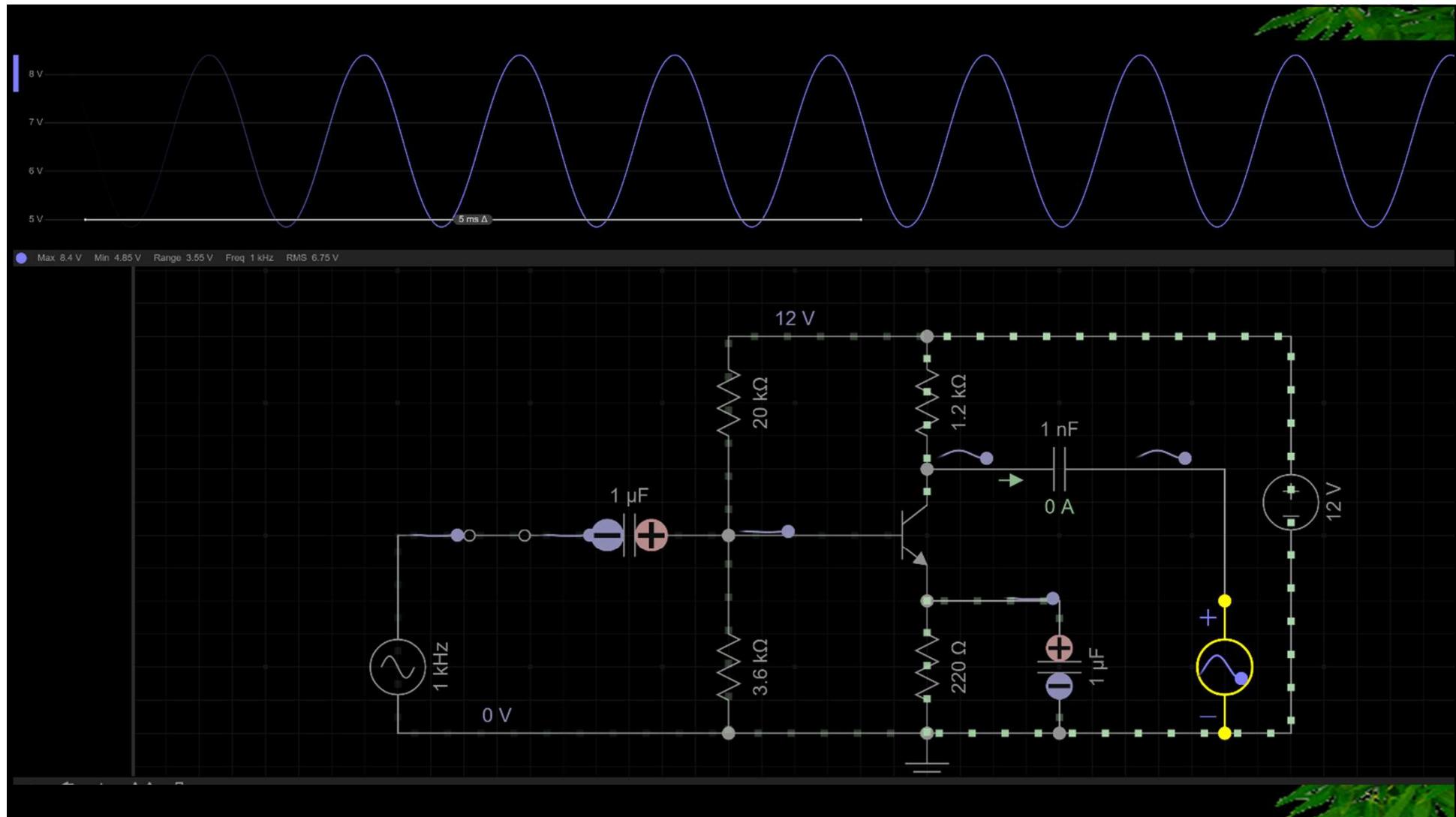
$$= i_b \left(1 + \frac{0.685}{3.05}\right) = 1.22i_b$$

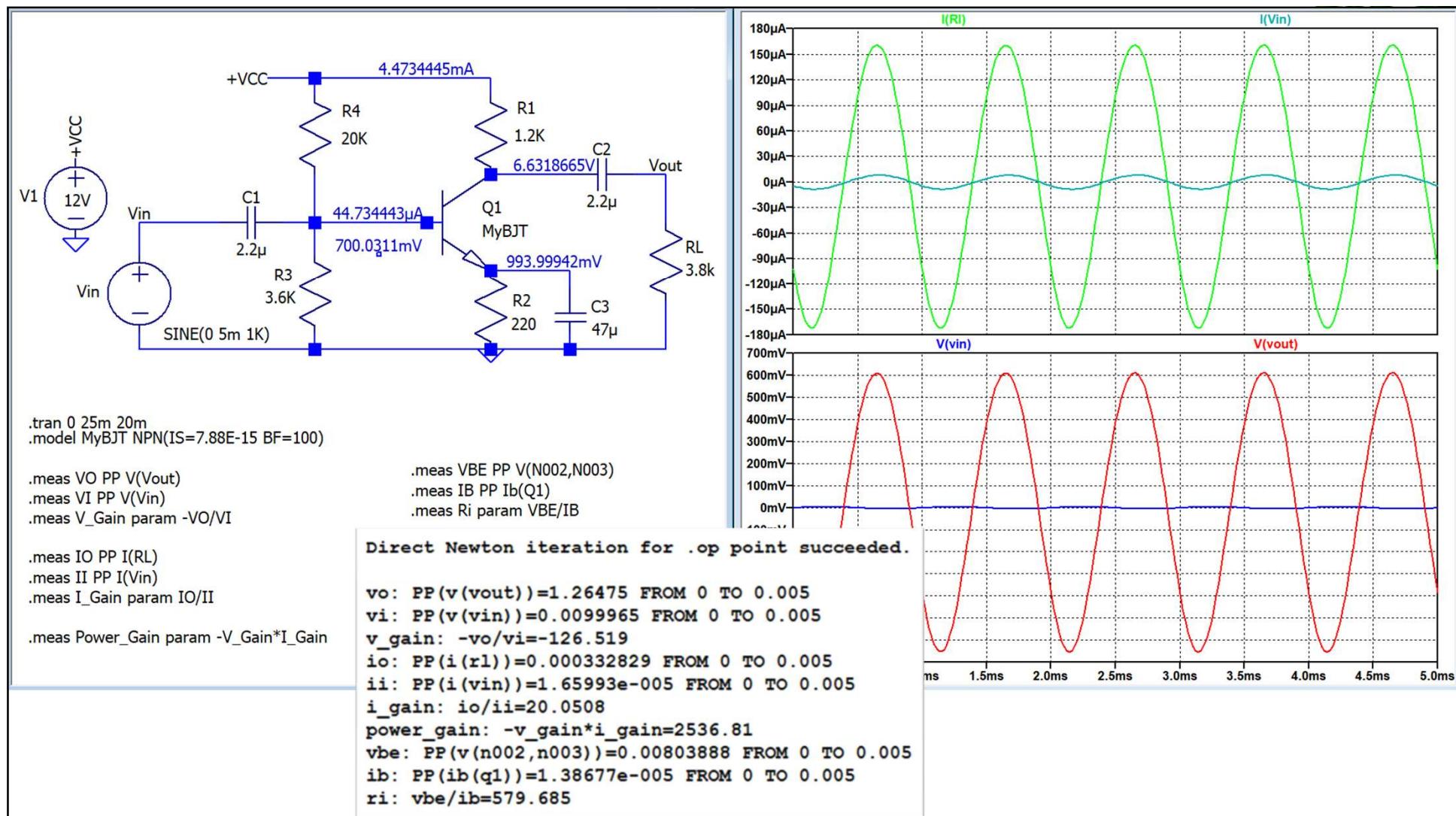


$$\text{Gradient of AC load line} = \left(\frac{-1}{R_{eq}}\right) = 1.096mS$$

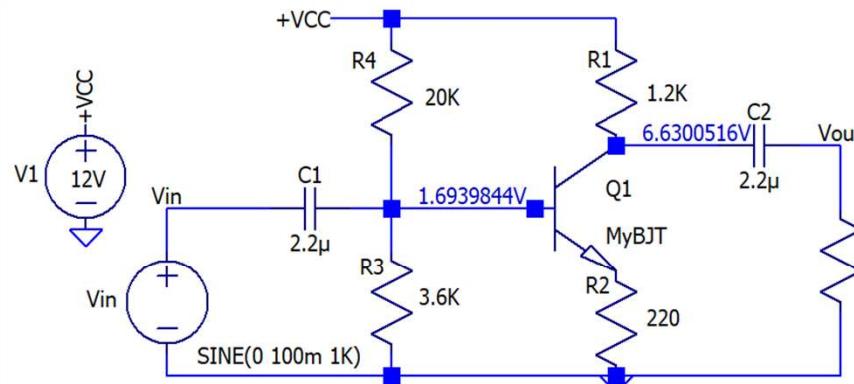








## Without by-pass capacitor...



```
.tran 10m
.model MyBJT NPN(IS=8E-15 BF=100)
```

```
.meas VO PP V(Vout)
.meas VI PP V(Vin)
.meas V_Gain param -VO/VI

.meas IO PP I(RL)
.meas II PP I(Vin)
.meas I_Gain param IO/II
```

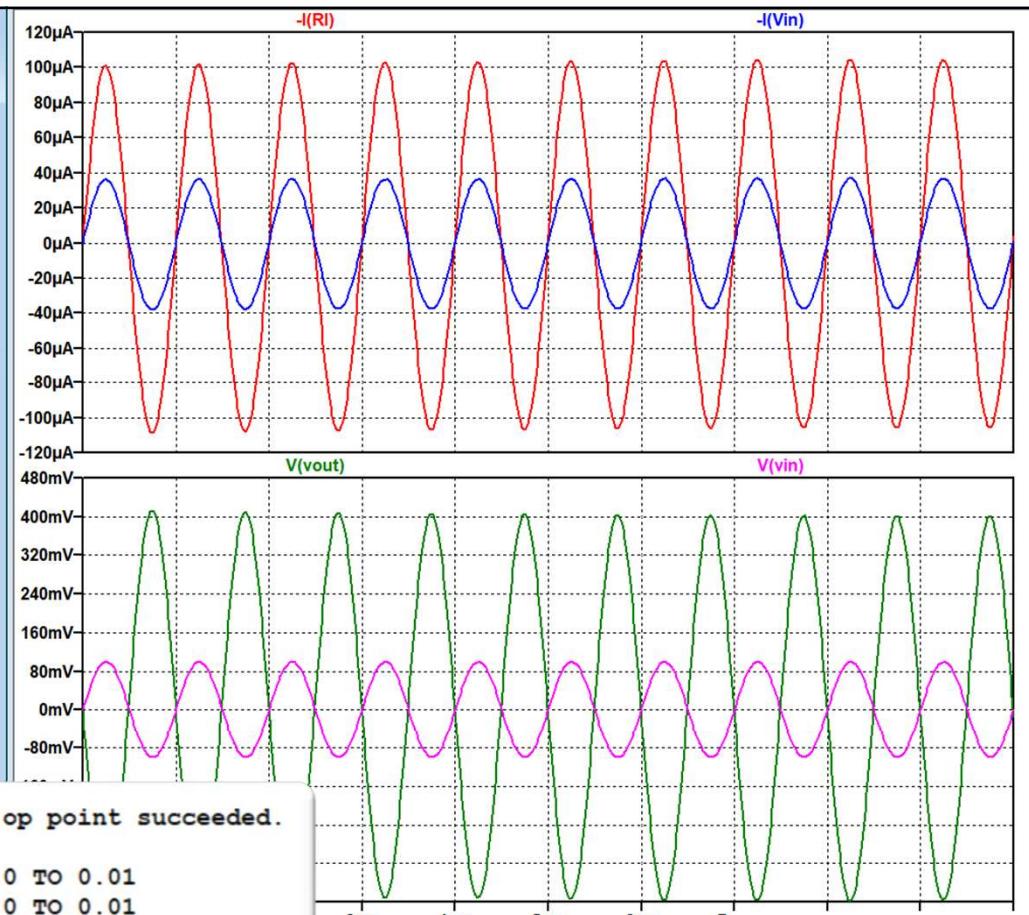
```
.meas Power_Gain param -V_Gain*I_Gain
```

Direct Newton iteration for .op point succeeded.

```

vo: PP(v(vout))=0.81047 FROM 0 TO 0.01
vi: PP(v(vin))=0.199953 FROM 0 TO 0.01
v_gain: -vo/vi=-4.0533
io: PP(i(rl))=0.000213282 FROM 0 TO 0.01
ii: PP(i(vin))=7.48783e-005 FROM 0 TO 0.01
i_gain: io/ii=2.84838
power_gain: -v_gain*i_gain=11.5453

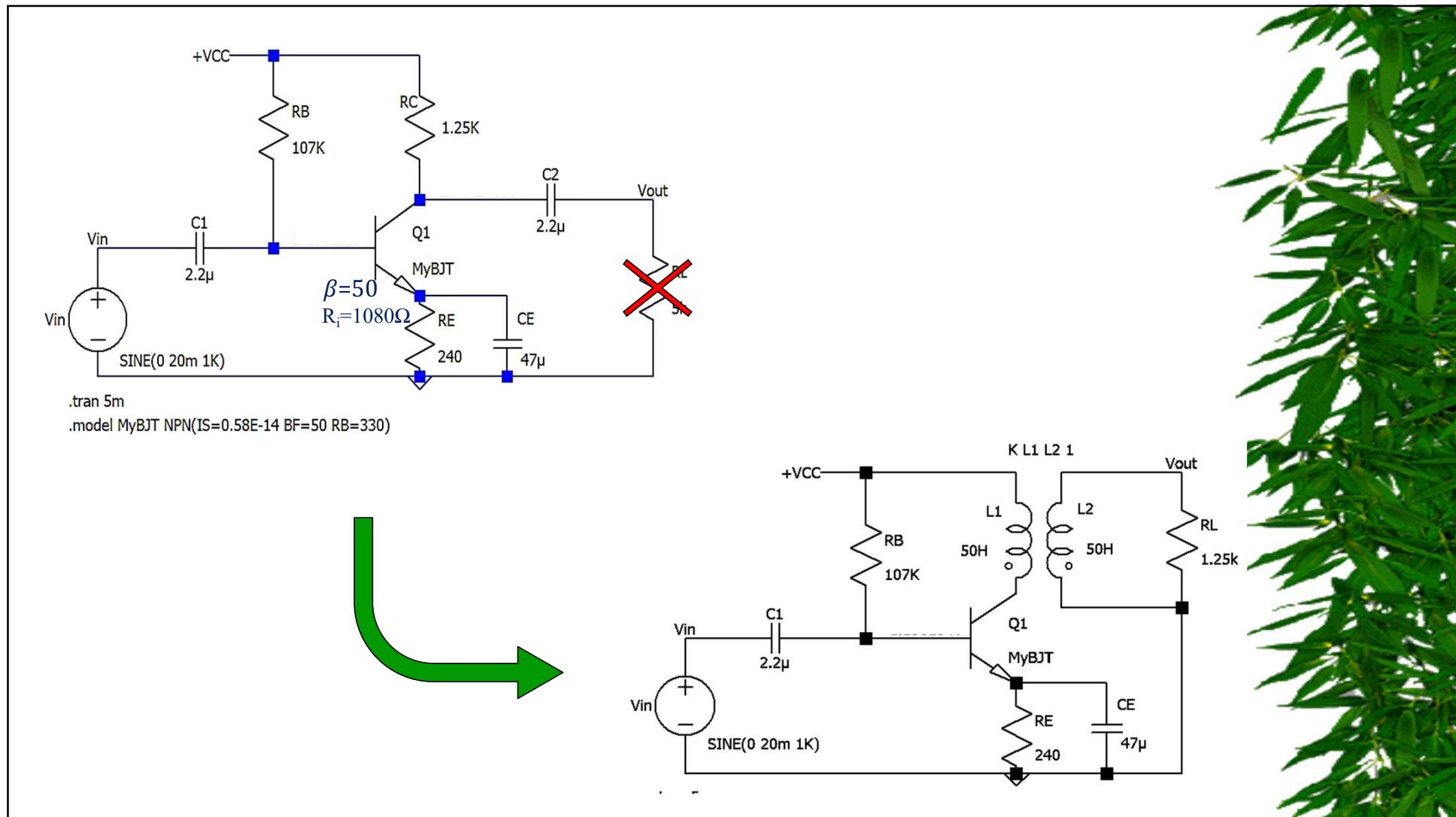
```

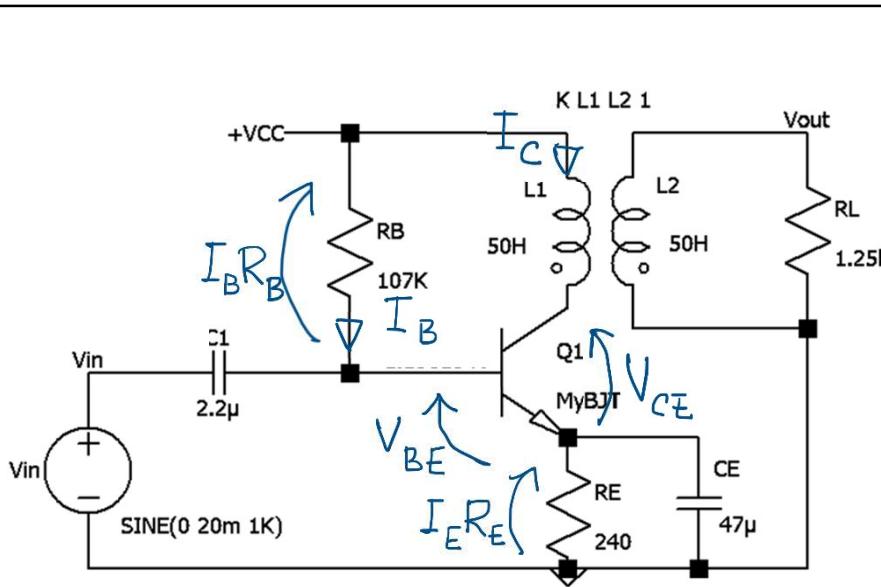


## Transformer-coupled load

- 1) Very good impedance matching is provided.
- 2) Gain achieved is higher.
- 3) Better power efficiency
- 1) Poor frequency response.
- 2) T/Fs are bulky and costly.
- 3) T/Fs tend to produce hum.







$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta)R_E}$$

$$I_B = \frac{5 - 0.7}{107 + 0.24(1 + 50)}$$

$$I_B = 36\mu A$$

$$I_C = 50 \times 36.06 = 1.8mA$$

$$I_E = (1 + 50)36 = 1.836 mA$$

$$I_E R_E + V_{BE} + I_B R_B = V_{CC}$$

$$(I_B + I_C)R_E + V_{BE} + I_B R_B = V_{CC}$$

$$(1 + \beta)I_B R_E + V_{BE} + I_B R_B = V_{CC}$$

$$V_{BE} + I_B [R_B + (1 + \beta)R_E] = V_{CC}$$

$$V_E = I_E R_E = 1.836 \times 240 = 440.64mV$$

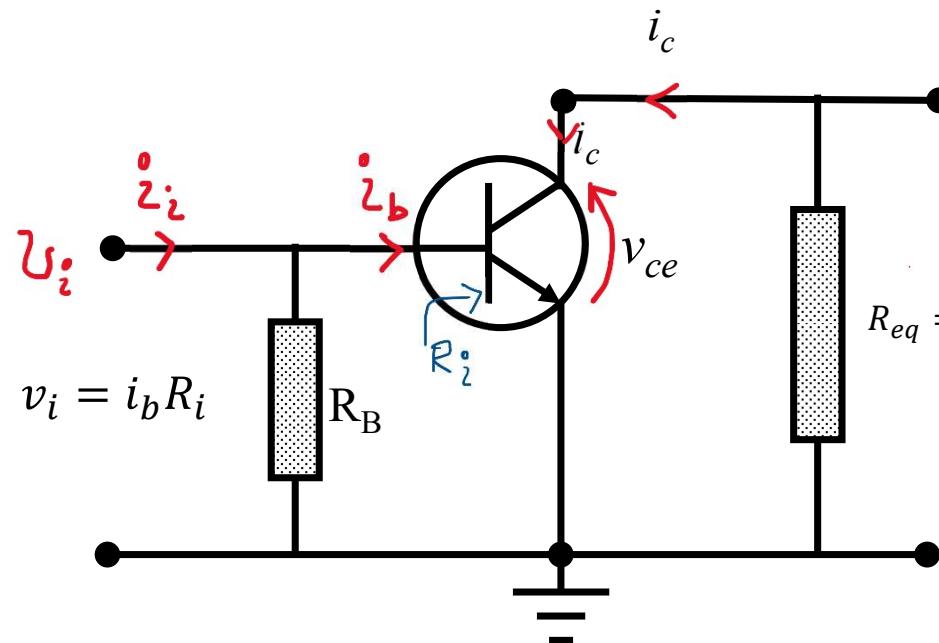
$$V_C = V_{CC} = 5V$$

$$V_{CE} = V_C - V_E = 5 - 0.4406 = 4.5594mV$$



## AC load line

Applying KCL for input side...



$$i_i = i_b + \frac{v_i}{R_B} = i_b \left(1 + \frac{R_i}{R_B}\right)$$

Applying KVL for output side...

$$R_{eq} = \left(\frac{n_1}{n_2}\right)^2 R_L$$

$$v_{ce} + i_c R_{eq} = 0$$

$$i_c = \left(\frac{-1}{R_{eq}}\right) v_{ce}$$

$$\text{Gradient of AC load line} = \left(\frac{-1}{R_{eq}}\right)$$

