Field-Effect Transistor (FET) Amplifier

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Introduction to FET – Key Points

- The concept : Julius Edgar Lilienfeld, 1925
- Theoretical development : William Shockley, 1952
- Working model : George Dacey and Ian Ross, 1953
- Three-terminal solid-state device.
- More compact and less power than a BJT
- More downsizing and miniaturizing.
- Voltage control concept

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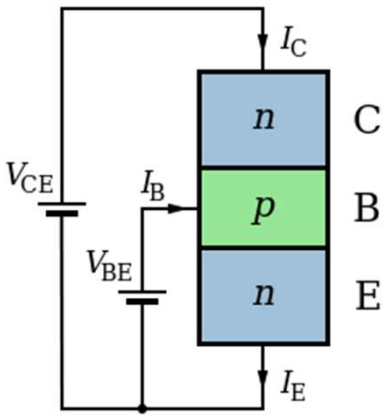
Recap: Current Control Concept of BJT



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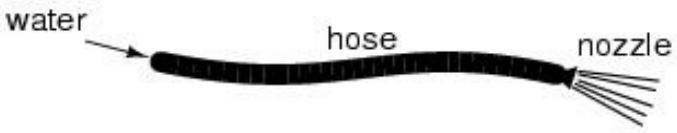
Another Concept



Hose constricted by squeezing, water flow reduced or stopped

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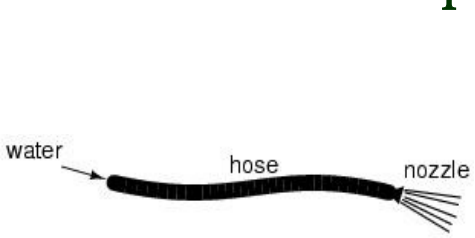
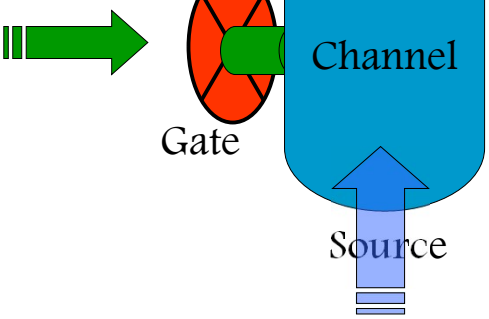
Concept Development



Concept



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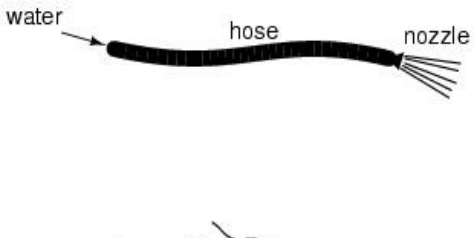
Concept Development



Concept

A Device

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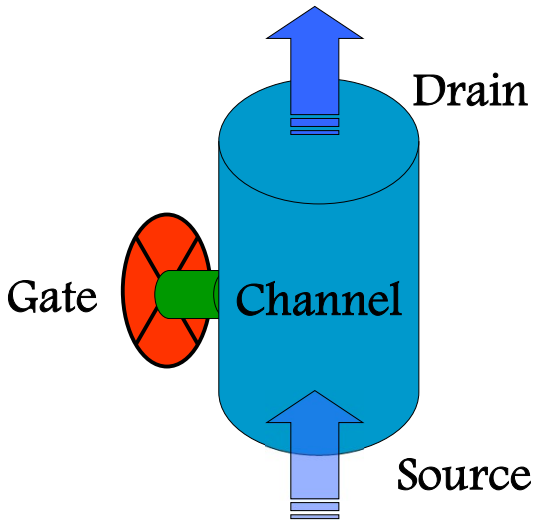
Concept Development



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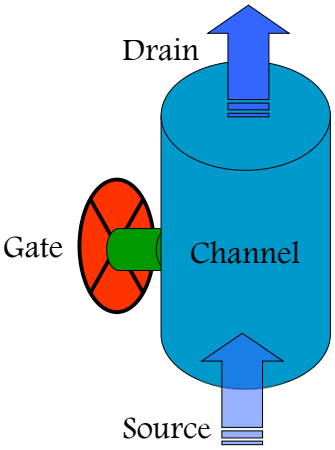
Concept Developed as a Solid-State Semiconductor Device



- Channel is an uninterrupted block of semiconductor.
- No P-N junction to go through.
  - Channel current is flowing between Dain and Source.
- N-channel and P-channel types.
- Channel current is controlled by the gate.

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Two Main Types of FETs

Junction Gate FET	• JUGFET / JFET
Insulated Gate FET or Metal Oxide Semiconductor FET	• IGFET / MOSFET

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Gate Implementation

JFET has a reverse biased p-n junction at the gate for controlling.

IGFET has a small capacitance at the gate for controlling.

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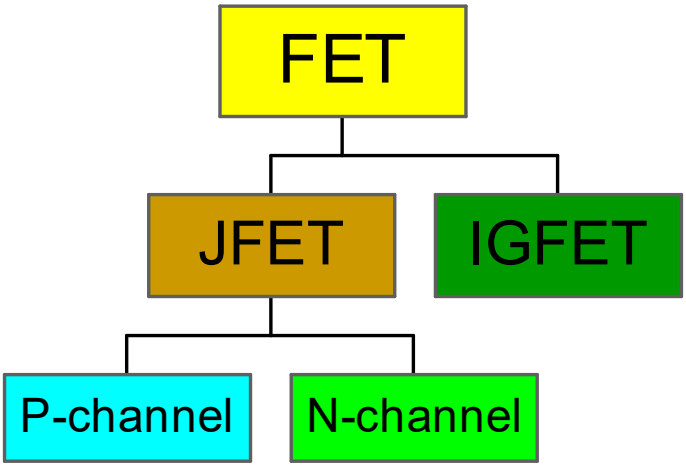
Further Classification



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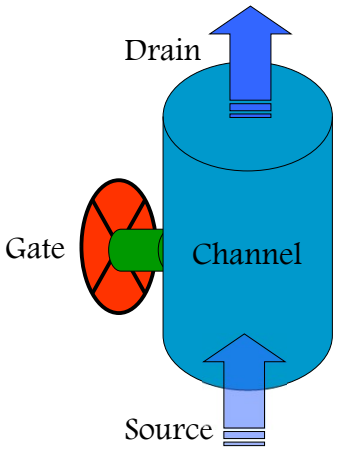
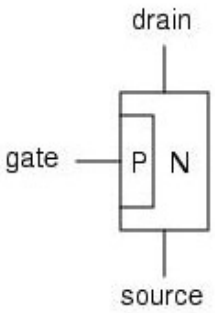
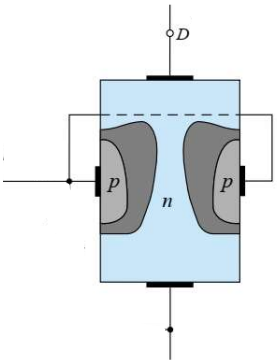
N-channel JFET







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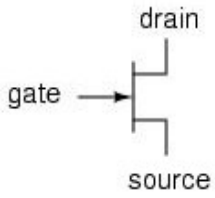
N-channel JFET



- Channel is an N type S/C layer.
- An electron current.
- Gate arrow points towards the N-channel.
- Gate terminal arrow differentiate between P-Channel and N-Channel FETs.

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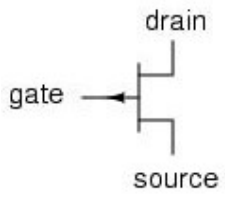
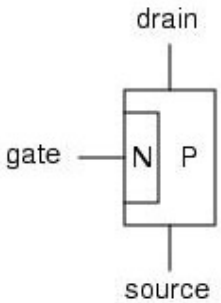
P-channel JFET





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Channel Resistance

- Measured between the Drain and Source terminals
- Relatively low (a few hundred ohms at most) when the gate-bias voltage is zero.
- Resistance from source to drain is same value as from drain to source.

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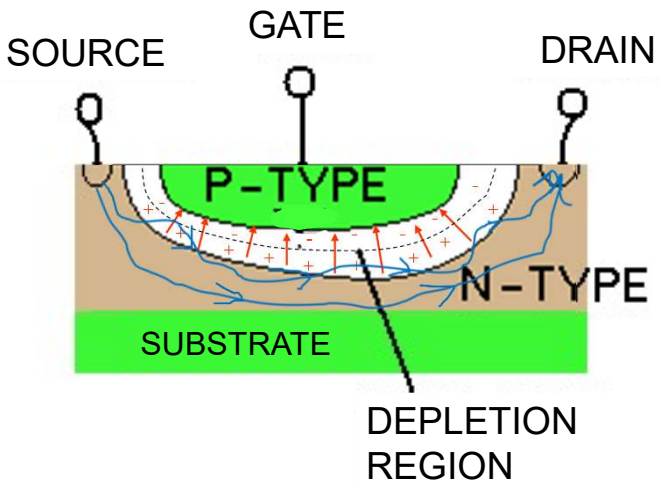
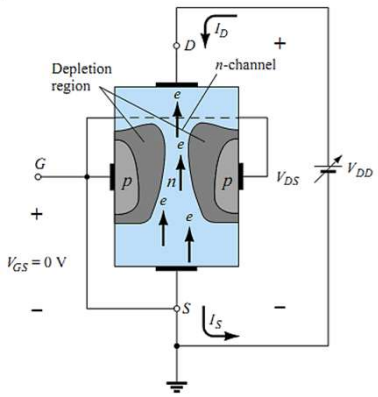
Internal Operation



Transistor Action

- When the reverse bias of p-n junctior is increased,
  - Depletion layer widens,
  - Electric field repels electrons,
  - Effective channel width is reduced
  - Channel current is reduced.

..and vice versa.



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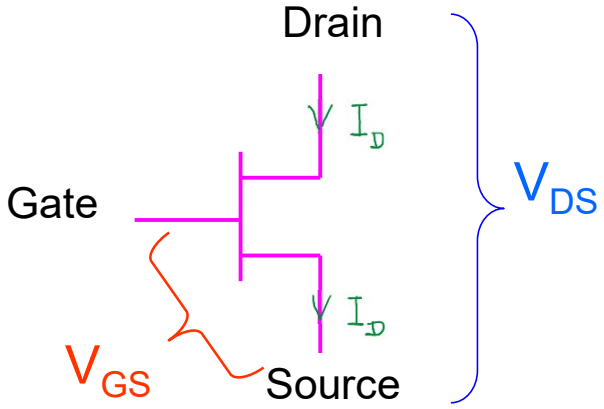
External Voltages & Currents



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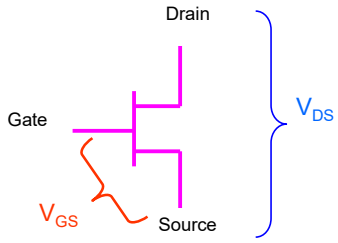
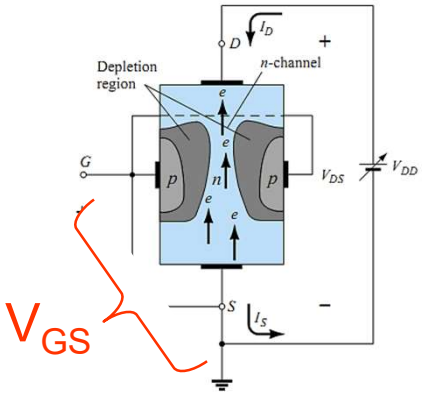
External Voltages & Currents





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Operating Modes

Switching

- Cut-off
- Saturation

Amplifying

- Active

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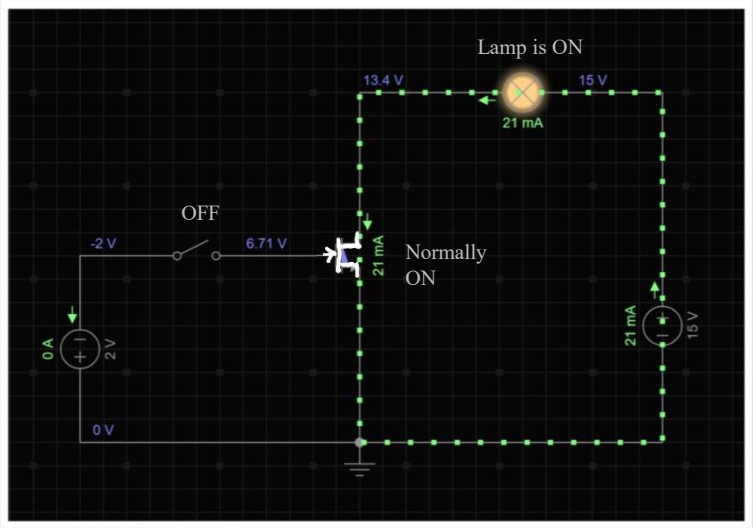
Switching Mode



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'Normally-ON' Device

- JFETs are normally-on devices.
- A reverse-biasing voltage between G &S expands Depletion layer
- Pinching-off the channel between source and drain

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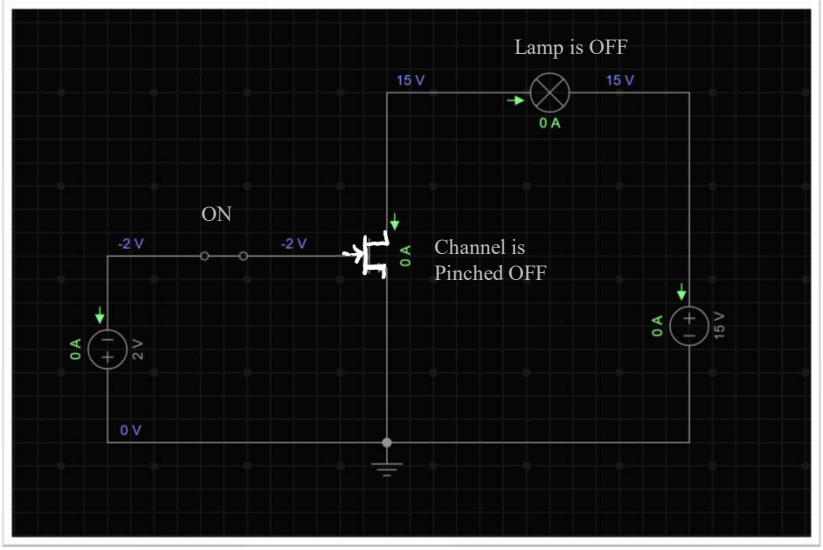
Lamp is OFF



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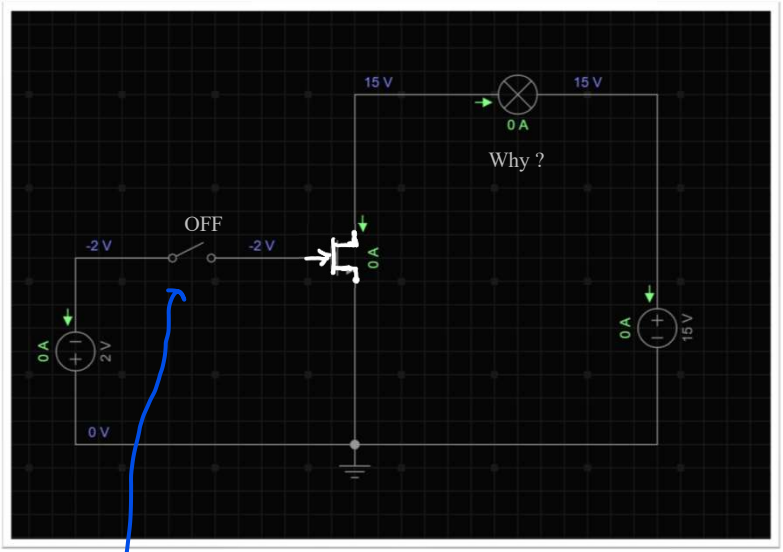
Lamp Does Not Light-UP !



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no way to flow out for stored chagers in deplition layer

Stored Charge

- Stored charge built up across the junction's natural capacitance when the controlling voltage is removed.
- Attach a "bleed-off" resistor between gate and source to discharge
- Otherwise, JFET remains cutoff

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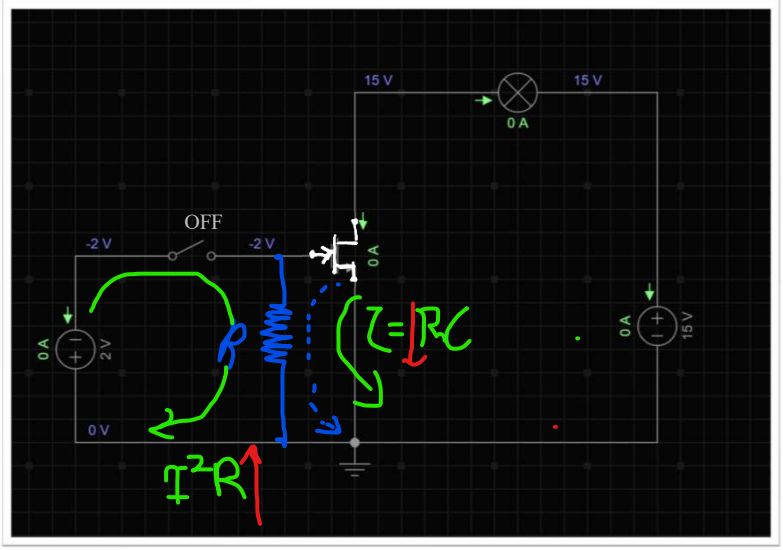
Method of Removing Stored Charge



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$P = \frac{V^2}{R}$

But when switch is on current flow through resistor R decepated more power that s darwback

to less the power decepation R should be high but discharge fast R should be less . so there is a delima

FET Characteristics

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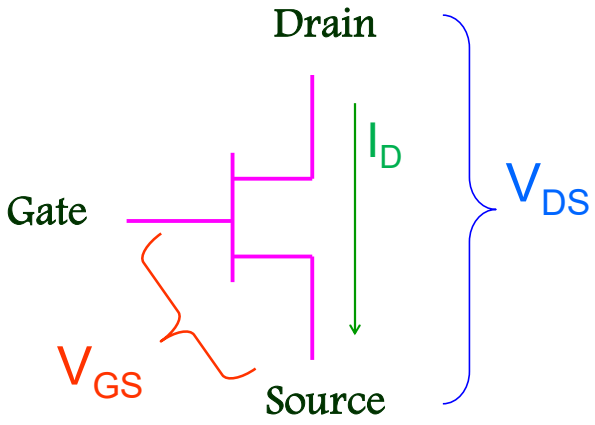
Three Variables



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Static Mutual Characteristics

- Mutual = Between input & output
- Controlled Variable = Drain current (I_D)
- Controlling variable = Gate Voltage (V_{GS})
- Plot of Controlled Vs. Controlling

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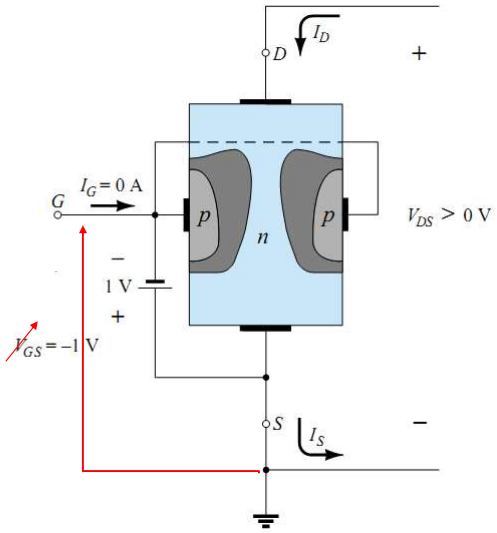
N channel JFET: Negative voltage on Gate



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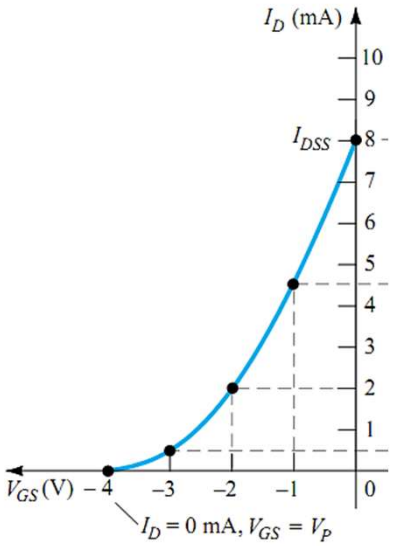
Static Mutual Characteristics



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Mathematical Model

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Non-Linear Behavior : Square Law

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Mutual Conductance

Corresponding change in the Drain current

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

Mutual Conductance (Transconductance)

Change in Gate Voltage

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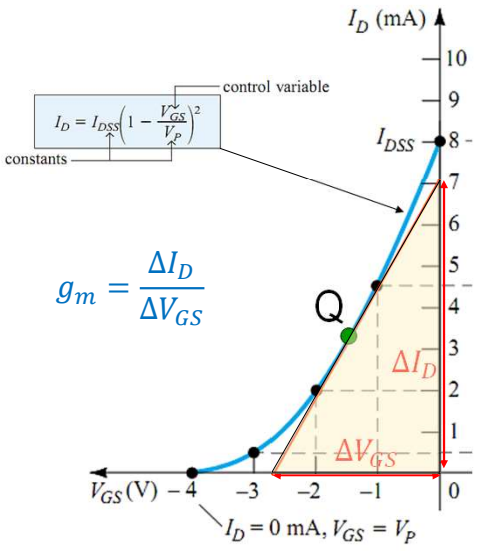
Calculating the Mutual Conductance…



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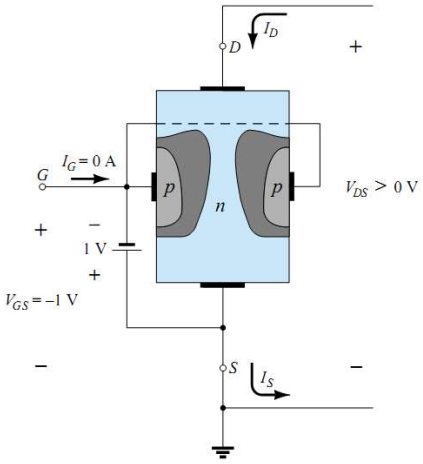
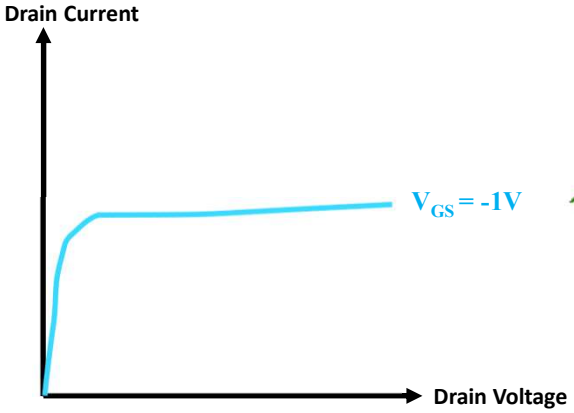
Static Output (Drain) Characteristics





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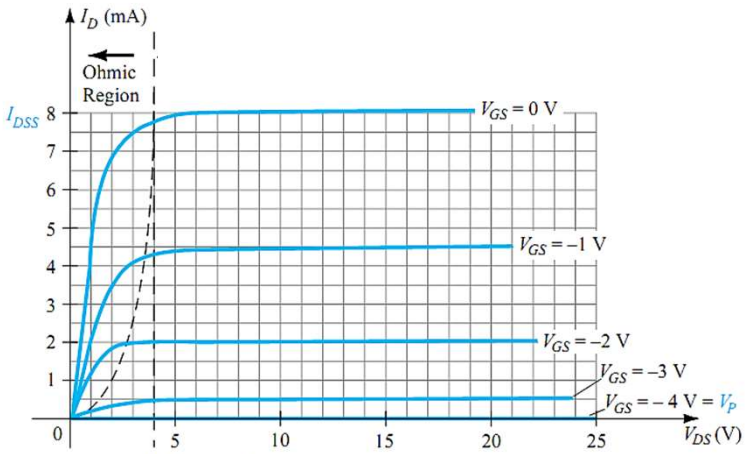
Static Output (Drain) Characteristics



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Compare with BJT

JFET		BJT
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0$ A	$\Leftrightarrow$	$V_{BE} \cong 0.7$ V

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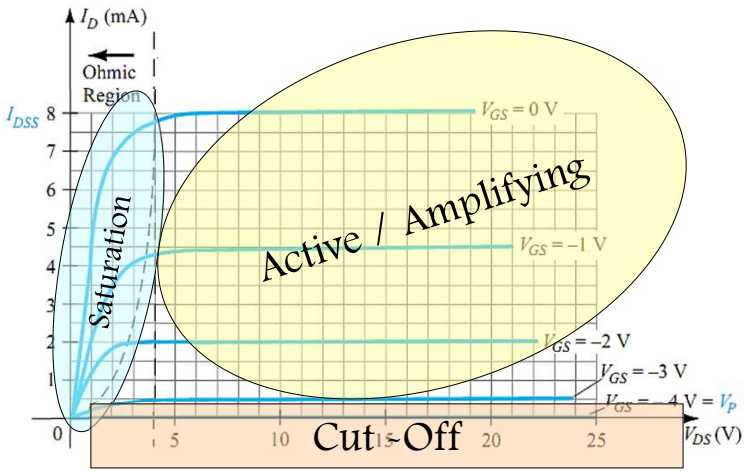
Static Output (Drain) Characteristics



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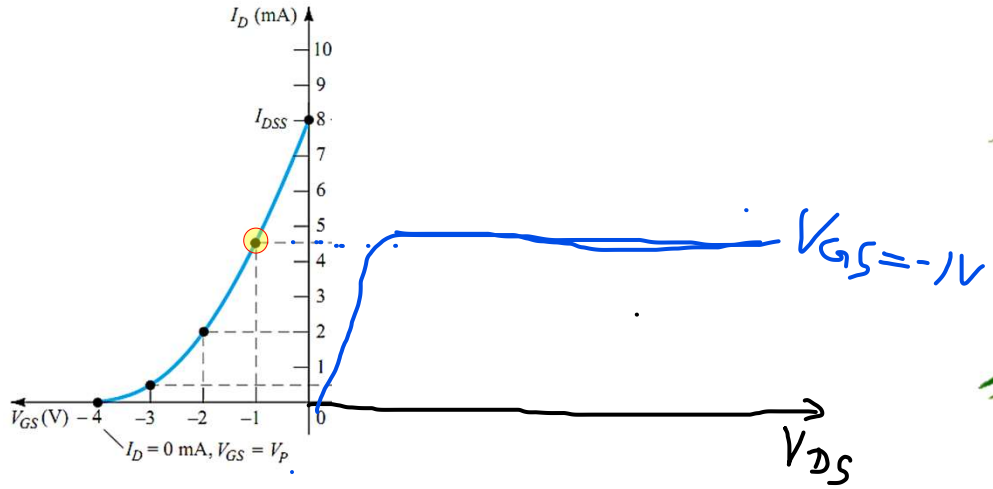


$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 8\text{ mA}\left(1 - \frac{-1\text{ V}}{-4\text{ V}}\right)^2 = 8\text{ mA}\left(1 - \frac{1}{4}\right)^2 = 8\text{ mA}(0.75)^2$$

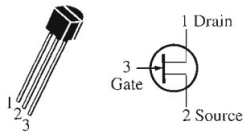
$$= 8\text{ mA}(0.5625)$$

$$\mathbf{= 4.5\text{ mA}}$$

A General Purpose JFET – 2N5457

2N5457
thru
2N5459

Case 29-04, Style 5
TO-92 (TO-226AA)



Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source voltage	V_{DS}	25	V dc
Drain-Gate voltage	V_{DG}	25	V dc
Reverse gate-source voltage	V_{GSR}	–25	V dc
Gate current	I_G	10	mA dc
Total device dissipation @ T_A = 25°C Derate above 25°C	P_D	310 2.82	mW mW/°C
Junction temperature	T_J	125	°C
Storage channel temperature range	T_{stg}	–65 to +150	°C

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

SYMBOL	PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
BV_{GSS}	Gate-Source Breakdown Voltage		-25		V	I_G = -10μA, V_{DS} = 0
I_{GSS}	Gate Reverse Current			-1.0	nA	V_{GS} = -15V, V_{DS} = 0
				-200		V_{GS} = -15V, V_{DS} = 0, T_A = 100°C
$V_{GS(off)}$	Gate-Source Cutoff Voltage	2N5457	-0.5	-6.0	V	V_{DS} = 15V, I_D = 10nA
		2N5458	-1.0	-7.0		
		2N5459	-2.0	-8.0		
V_{GS}	Gate-Source Voltage	2N5457	2.5		V	V_{DS} = 15V, I_D = 100μA, Typical
		2N5458	3.5			V_{DS} = 15V, I_D = 200μA, Typical
		2N5459	4.5			V_{DS} = 15V, I_D = 400μA, Typical
I_{DSS}	Zero-Gate-Voltage Drain Current (Note 1)	2N5457	1.0	5.0	mA	V_{DS} = 15V, V_{GS} = 0
		2N5458	2.0	9.0		
		2N5459	4.0	16		
$\lvert y_{fs} \rvert$	Forward Transfer Admittance	2N5457	1000	5000	μS	V_{DS} = 15V, V_{GS} = 0 , f = 1kHz
		2N5458	1500	5500		
		2N5459	2000	6000		
$\lvert y_{os} \rvert$	Output Admittance			50	μS	V_{DS} = 15V, V_{GS} = 0, f = 1kHz
C_{iss}	Input Capacitance (Note 2)			7.0	pF	V_{DS} = 15V, V_{GS} = 0, f = 1MHz
C_{rss}	Reverse Transfer Capacitance (Note 2)			3.0	pF	V_{DS} = 15V, V_{GS} = 0, f = 1MHz
NF	Noise Figure (Note 2)			3.0	dB	V_{DS} = 15V, V_{GS} = 0, R_G = 1MHz, BW = 1Hz, f = 1kHz

NOTES: **1.** Pulse test required. PW ≤630ms, duty cycle ≤10%.
2. For design reference only, not 100% tested.

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J309, J310

Preferred Device

JFET VHF/UHF Amplifiers

N−Channel — Depletion

Features

- Pb−Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DS}	25	Vdc
Gate−Source Voltage	V_{GS}	25	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above = 25°C	P_D	350 2.8	mW mW/°C
Junction Temperature Range	T_J	−65 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

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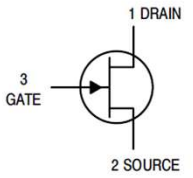

TO−92
CASE 29−11
STYLE 5

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J309 JFET Data

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate−Source Breakdown Voltage (I_G = −1.0 μAdc, V_{DS} = 0)		$V_{(BR)GSS}$	−25	–	–	Vdc
Gate Reverse Current (V_{GS} = −15 Vdc, V_{DS} = 0, T_A = 25°C) (V_{GS} = −15 Vdc, V_{DS} = 0, T_A = +125°C)		I_{GSS}	– –	– –	−1.0 −1.0	nAdc μAdc
Gate Source Cutoff Voltage (V_{DS} = 10 Vdc, I_D = 1.0 nAdc)	J309 J310	$V_{GS(off)}$	−1.0 −2.0	– –	−4.0 −6.5	Vdc
ON CHARACTERISTICS						
Zero−Gate−Voltage Drain Current[1] (V_{DS} = 10 Vdc, V_{GS} = 0)	J309 J310	I_{DSS}	12 24	– –	30 60	mAdc
Gate−Source Forward Voltage (V_{DS} = 0, I_G = 1.0 mAdc)		$V_{GS(f)}$	–	–	1.0	Vdc

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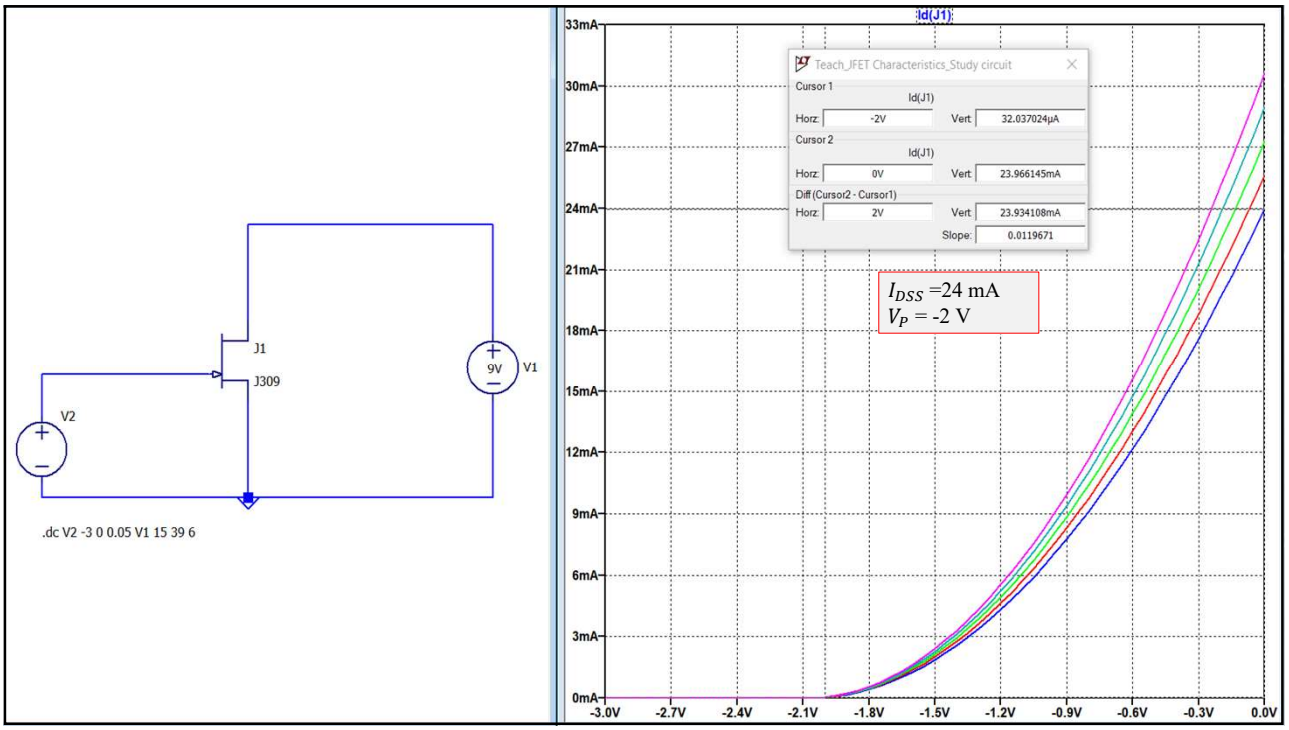
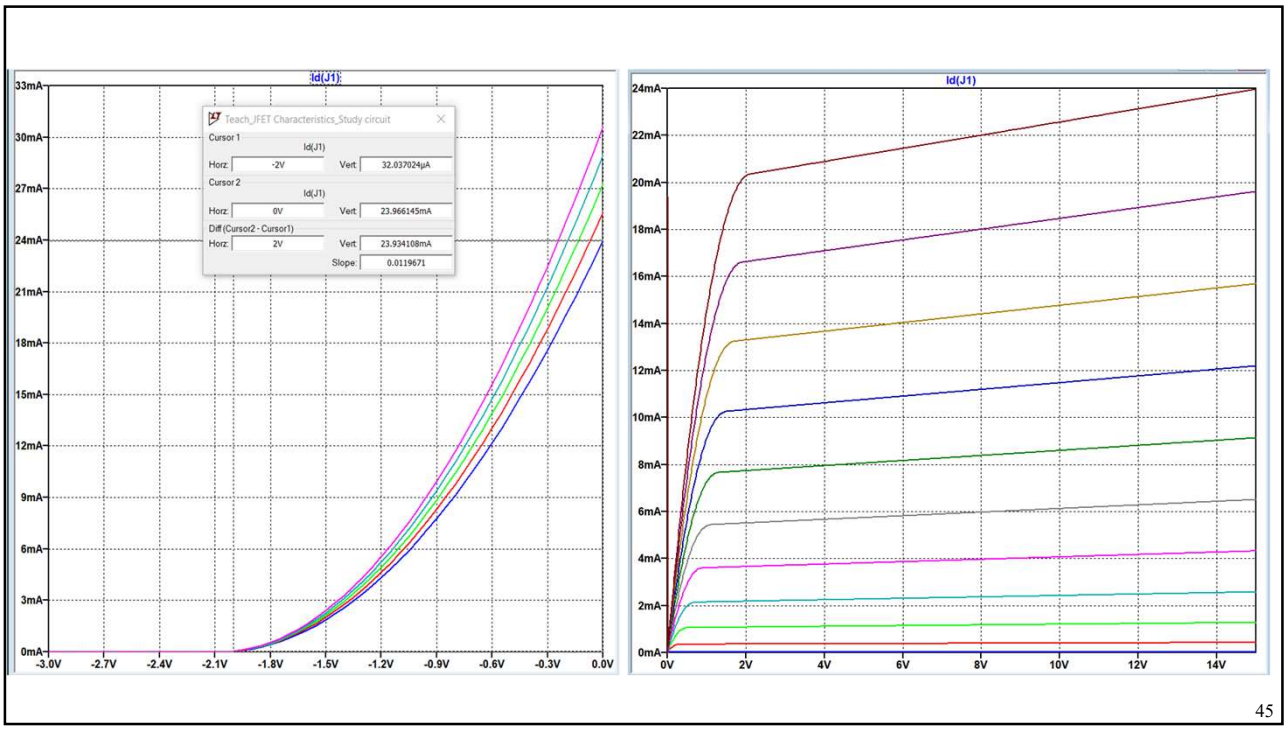


I_{DSS} =24 mA
V_P = -2 V


Id(J1)
Teach_JFET Characteristics_Study circuit
Cursor 1
Id(J1)
Horz: -2V
Vert: 32.037024µA
Cursor 2
Id(J1)
Horz: 0V
Vert: 23.966145mA
Diff (Cursor2 - Cursor1)
Horz: 2V
Vert: 23.934108mA
Slope: 0.0119671
33mA
30mA
27mA
24mA
21mA
18mA
15mA
12mA
9mA
6mA
3mA
0mA
-3.0V -2.7V -2.4V -2.1V -1.8V -1.5V -1.2V -0.9V -0.6V -0.3V 0.0V
Id(J1)
24mA
22mA
20mA
18mA
16mA
14mA
12mA
10mA
8mA
6mA
4mA
2mA
0mA
0V 2V 4V 6V 8V 10V 12V 14V

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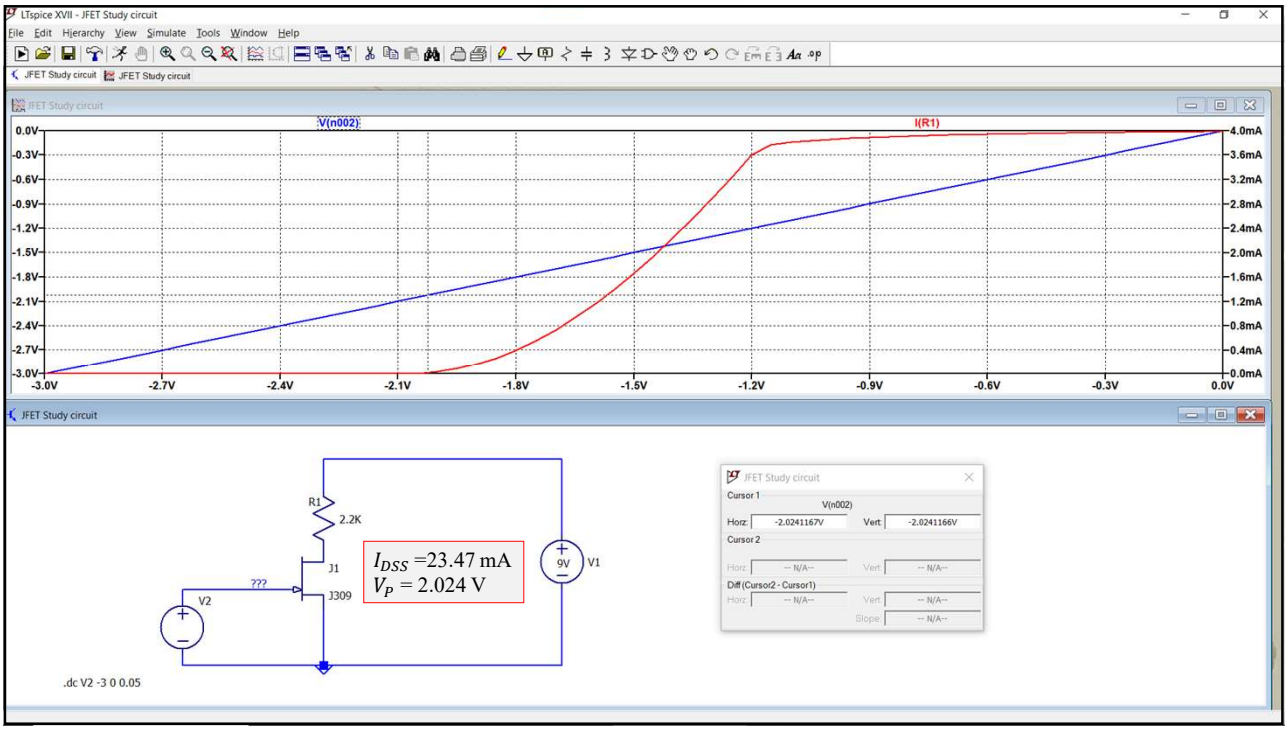
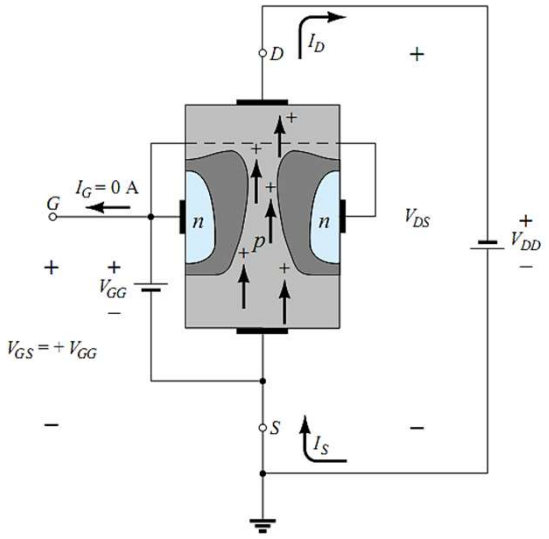

LTspice XVII - JFET Study circuit
File Edit Hierarchy View Simulate Tools Window Help
JFET Study circuit
JFET Study circuit
V(n002)
I(R1)
0.0V
-0.3V
-0.6V
-0.9V
-1.2V
-1.5V
-1.8V
-2.1V
-2.4V
-2.7V
-3.0V
4.0mA
3.6mA
3.2mA
2.8mA
2.4mA
2.0mA
1.6mA
1.2mA
0.8mA
0.4mA
0.0mA
-3.0V -2.7V -2.4V -2.1V -1.8V -1.5V -1.2V -0.9V -0.6V -0.3V 0.0V
JFET Study circuit
R1
2.2K
J1
J309
???
V2
9V
V1
I_{DSS} =23.47 mA
V_P = 2.024 V
.dc V2 -3 0 0.05
JFET Study circuit
Cursor 1
V(n002)
Horz: -2.0241167V
Vert: -2.0241166V
Cursor 2
Horz: -- N/A--
Vert: -- N/A--
Diff (Cursor2 - Cursor1)
Horz: -- N/A--
Vert: -- N/A--
Slope: -- N/A--

P Channel JFET



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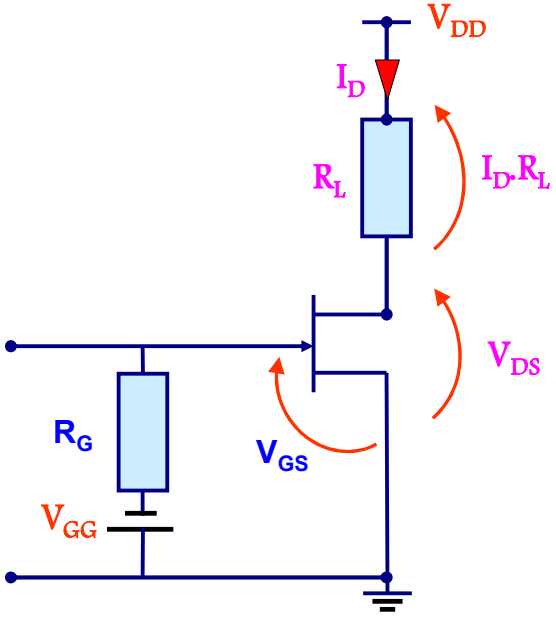
Gate Bias Method

Since I_G=0

$V_{GS} = -V_{GG}$



Rg should be very high to no current flow

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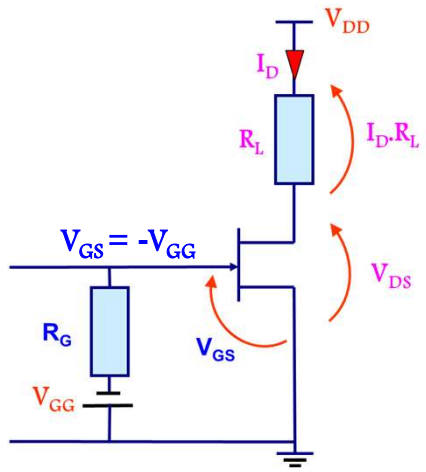
DC Load Line



$$V_{DS} + I_D.RL = VDD$$

$$I_D.RL = -VDS + V_{DD}$$

$$I_D = -\left(\frac{1}{R_L}\right)V_{DS} + \frac{V_{DD}}{R_L}$$

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For locating the Q point at the center

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\frac{I_D}{I_{DSS}} = \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

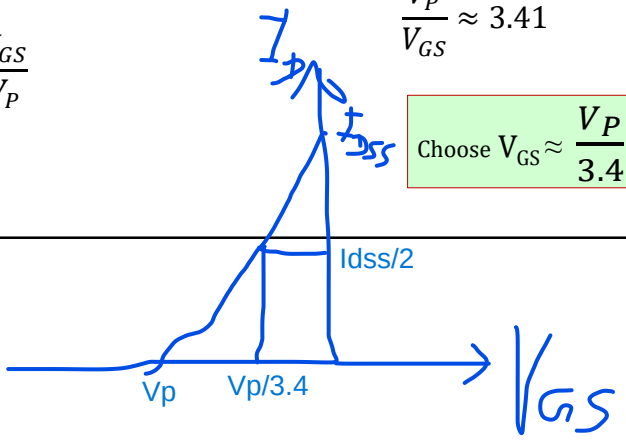
$$\sqrt{\frac{I_D}{I_{DSS}}} = 1 - \frac{V_{GS}}{V_P}$$

$$\frac{V_{GS}}{V_P} = 1 - \sqrt{\frac{I_D}{I_{DSS}}}$$

$$\frac{V_{GS}}{V_P} = 1 - \sqrt{0.5} = 0.2929$$

$$\frac{V_P}{V_{GS}} \approx 3.41$$

Choose $V_{GS} \approx \frac{V_P}{3.4}$



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