UNIVERSITY OF MORATUWA
Faculty of Engineering
Department of Electronic and Telecommunication Engineering
B.Sc. Engineering
Semester 2 (2022 Batch) Examination

EN1014 ELECTRONIC ENGINEERING

Time allowed: *Three (3)* hours August 2024

INSTRUCTIONS TO CANDIDATES:

- This paper contains 5 questions on 6 pages.
- Answer **all** questions.
- This paper contains **two** sections. Use a **separate** answer book for each section.
- All questions carry **equal** marks.
- This examination accounts for **60%** of the module assessment. The total maximum mark attainable is **100**. The marks assigned for each question & sections thereof are indicated in square brackets.
- The symbols used in this paper have their usual meanings.
- This is a **closed-book** examination.
- Electronic/communication devices are not permitted. Only equipment allowed is a calculator approved and labeled by the Faculty of Engineering.
- Derivations are not required if they are not explicitly requested in the question.
- Assume reasonable values for any data not given in or with the examination paper. Clearly state such assumptions.
- If you have any doubt as to the interpretation of the wording of a question, make your own decision, and clearly state it.

ADDITIONAL MATERIAL:

- No additional material is provided.

SECTION A

Question 1.

(a) Draw a lumped element abstraction model for a coil. Define each lumped element. [2 marks]

(b) Draw a module-level abstraction of a battery powered electronic toothbrush which has a brush head as the output device that oscillates. Internally, there is a mechanism to convert a rotary motion of a battery powered motor to an oscillating motion. Users expect several brushing modes as well. Apply the concept of central control in your design. [4 marks]

(c) In the circuit shown in Figure Q1(c), the input signal is a 1 kHz sinusoidal waveform with a peak value of 800 mV. Note that a diode has been added to the negative feedback loop so that, when the diode is off, the negative feedback loop is broken.

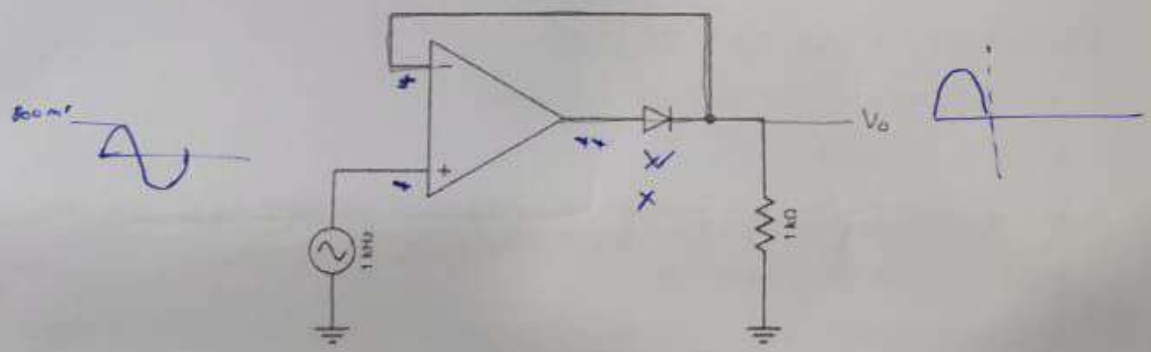


Figure Q1(c)

i. Briefly explain the operation of the circuit during each half cycle. [2 marks]

ii. Sketch the output waveform and identify the specialty of this circuit. [2 marks]

(d) Positive feedback has been applied to the opamp in the circuit given in Figure Q1(d). V_X is a DC threshold voltage and V_i is the external input voltage.

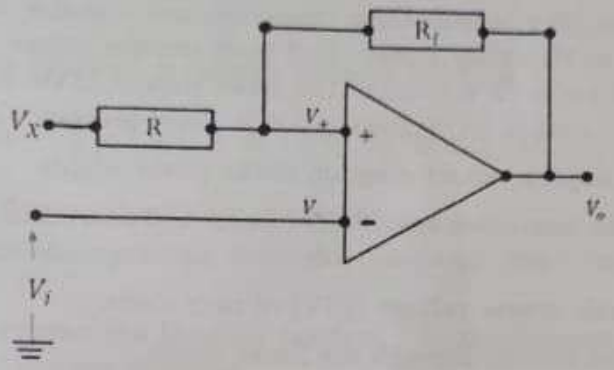


Figure Q1(d)

i. Name the circuit. Shmitt Trigger [1 mark]

ii. Identify a possible application where this circuit will be useful. [2 marks]

(e) i. Derive the equation of the output signal (V_o) for the circuit given in Figure Q1(e). [5 marks]

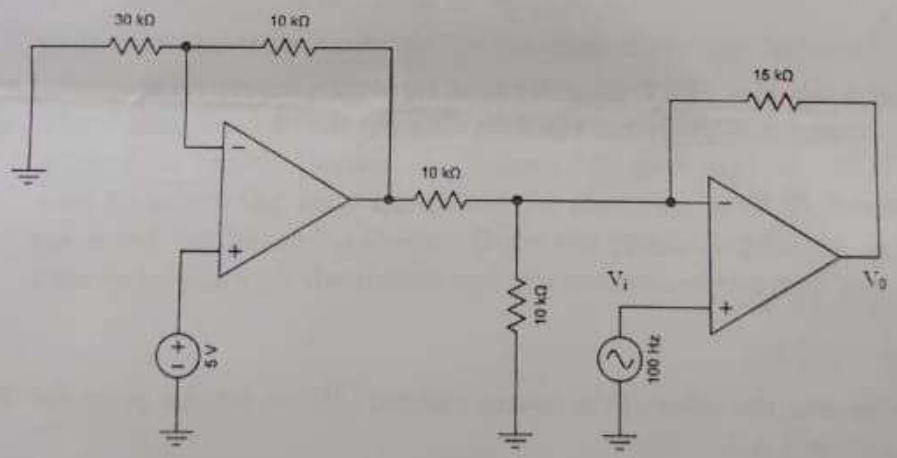
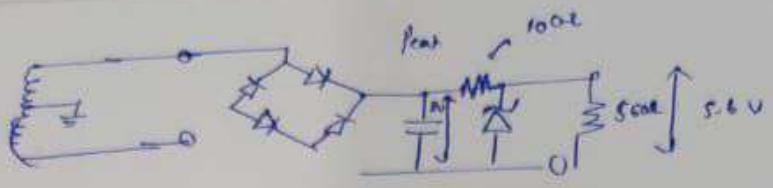


Figure Q1(e)

ii. Draw the output waveform when V_i oscillates between 0 V and 5 V, and interpret the change between the input and output waveforms. [2 marks]



Question 2.

A conventional regulated DC power supply consists of a center-tapped transformer, a full-wave rectifier, a smoothing capacitor, and a simple Zener regulator. The input is 230 V, 50 Hz utility power. Full wave rectifier output measured across the smoothing capacitor is 12 V (peak). The series resistor of the Zener regulator is 100 Ω. The regulated output DC voltage is 5.6 V. Load resistance is 560 Ω.

(a) Draw the complete circuit diagram of the power supply. [3 marks]

(b) Calculate the step-down transformer ratio. Use near-ideal diode model for your calculations. [3 marks]

(c) Find the peak inverse voltage (PIV) of each diode. [3 marks]

(d) Calculate the current through the Zener diode. [3 marks]

(e) Find the equivalent resistance across the smoothing capacitor, and hence calculate the value of the smoothing capacitor required to keep the peak-to- peak ripple voltage at 400 mV. [4 marks]

(f) The regulator should work even when the load is removed. If the supply voltage can have ±30% variation, what should be the maximum power dissipation capacity of the Zener diode? [4 marks]

Question 3.

Consider a self-bias JFET amplifier that employs a source resistor (R_S) and a source bypass capacitor (C_S). It has the following parameters:

- $I_{DSS} = 10$ mA
- $V_{GS(off)} = V_P = -4$ V
- $V_{DD} = 15$ V
- $R_D = 2.2$ kΩ

(a) Determine the value of the source resistor (R_S) to set the quiescent drain current ($I_{D,Q}$) at 4 mA. [3 marks]

(b) Determine the drain-source voltage ($V_{DS,Q}$) at the quiescent point. [3 marks]

(c) Estimate the typical minimum value of the source bypass capacitor to ensure proper operation at a signal frequency of 1 kHz. [3 marks]

(d) Sketch the DC load line and mark the co-ordinates of the Q-point. [3 marks]

(e) Derive the equation of the AC load line. [3 marks]

(f) When a single-tone audio test signal having a peak voltage of 50 mV is applied to the amplifier it was observed that the drain current drops to its minimum of 3.1 mA during the operation. Calculate voltage gain of the amplifier. [3 marks]

(g) Find the mutual conductance of the JFET. [2 marks]

SECTION B

Question 4.

(a) Consider the following 5-variable Boolean function

$$f(a,b,c,d,e) = \prod(2,5,7,8,10,17,19,26,30,31) \cdot D(1,3,14,15,18,20,25,28),$$

where $D(\cdot)$ denotes don't care maxterms.

i. Draw the corresponding 4-variable Karnaugh maps for the two cases: $a = 0$ and $a = 1$. [3 marks]

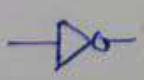
ii. Hence, express the Boolean function f in the *product-of-sums* form with a minimal number of literals. [6 marks]

iii. Draw the realization of the digital circuit corresponding to the simplified Boolean function f using a minimal number of 2-input and 3-input NOR gates. [3 marks]

(b) Consider the design of a low fuel-level indicator of a car of which the output Y should be 1 if the fuel level drops below a threshold. The fuel-level is indicated in 16 discrete levels (0 to 15), and the threshold is selected as the level 5, i.e, $Y = 1$ if the fuel level is less than or equal to 5.

i. Construct the truth table for the function of the low fuel-level indicator. [4 marks]

ii. The digital circuit is implemented using *only two* 4×1 multiplexers with *active-high* enable inputs, *one* 2-input OR gate and *one* NOT gate. You need to select the *least significant bit* that represent 16 discrete levels as the input to the multiplexers. Draw the realization of the digital circuit. Clearly indicate all the inputs and the outputs of the multiplexers. [4 marks]



Question 5.

(a) Flip flops have *asynchronous* preset and reset as direct inputs. Briefly explain a condition for which these inputs are used in a sequential digital circuit. [2 marks]

(b) Consider the design of a sequential logic circuit (having one input and one output) that can detect 1101 bit stream *with overlaps*. This circuit is designed as a Mealy machine and is implemented using D flip-flops.

i. Draw the corresponding state diagram. [5 marks]

ii. Obtain the binary-coded state table. [3 marks]

iii. Based on the excitation table of a D flip-flop, derive the simplified Boolean expressions for the flip-flop input equations. [4 marks]

iv. Derive the simplified Boolean expression for the output equation. [2 marks]

v. Draw the realization of the sequential logic circuit using D flip-flops, 2-input and 3-input AND gates and OR gates, and NOT gates. [4 marks]

- End of Question Paper -

1101 Overlaps Mealy D f.f.