A Design Example

- Requirement: To build a JFET preamplifier for a musical instrument.
- Given : Drain Resistance = 2.2 kΩ
- The parameters you need to design are:
  - DC Bias (V_{cc})
  - Quiescent channel current
  - Quiescent Gate voltage
  - Cut off frequency of the preamplifier
  - Coupling capacitors

Design Choices

1) JFET selection : Use J113 general purpose FET
   - V_{DS} (maximum) = 35V
   - $V_{GS,\,(off)}$ = -2 V
   - I_{DSS} = 8.34 mA
   - Max Power Dissipation = 625 mW
   - Drain to Source Resistance = 100 Ω
2) Supply Voltage Selection :
   - Choose 9v as V_{CC}
   - Most musical instrument circuits run on 9V
3) Gate-Source Voltage : Let us choose $V_{GS,Q}$ = 0.8 V

J113 JFET

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Max.	Unit
Off Characteristics						
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	I_G = -1.0 µA, V_{DS} = 0		-35		V
I_{GSS}	Gate Reverse Current	V_{GS} = -15 V, V_{DS} = 0			-1.0	nA
V_{GS}(off)	Gate-Source Cut-Off Voltage	V_{DS} = 15 V, I_D = 1.0 µA	**111**	-3.0	-10.0	V
			112	-1.0	-5.0	
			113	-0.5	-3.0	
I_D(off)	Drain Cutoff Leakage Current	V_{DS} = 5.0 V, V_{GS} = -10 V			1.0	nA
On Characteristics						
I_{DSS}	Zero-Gate Voltage Drain Current[(5)]	V_{DS} = 15 V, V_{GS} = 0	**111**	20		mA
			112	5.0		
			113	2.0		
r_{DS}(on)	Drain-Source On Resistance	V_{DS} ≤ 0.1 V, V_{GS} = 0	**111**		30	Ω
			112		50	
			113		100	
Small Signal Characteristics						
C_{dg}(on) C_{sg}(on)	Drain-Gate &Source-Gate On Capacitance	V_{DS} = 0, V_{GS} = 0, f = 1.0 MHz			28	pF
C_{dg}(off)	Drain-Gate Off Capacitance	V_{DS} = 0, V_{GS} = -10 V, f = 1.0 MHz			5.0	pF
C_{sg}(off)	Source-Gate Off Capacitance	V_{DS} = 0, V_{GS} = -10 V, f = 1.0 MHz			5.0	pF

Note:

5. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2%.

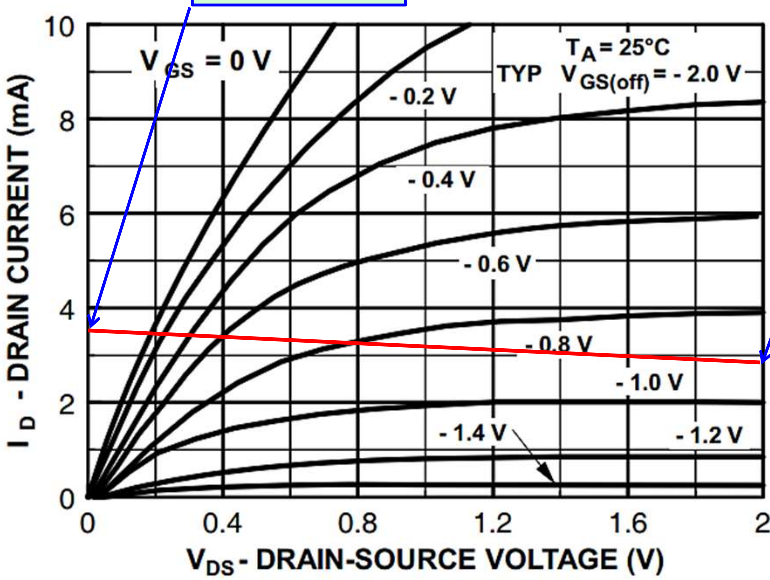
76

J113 JFET

$$\frac{9}{2.2 + 0.267} = 3.65$$

$$\frac{9 - 2}{2.2 + 0.267} = 2.84$$

2.25A



77

Design (cont.) : Operating Point

Chosen $V_{GS} = -0.8$ V

$$R_S = \left|\frac{0.8\ V}{3\ mA}\right| = 267\ k\Omega$$

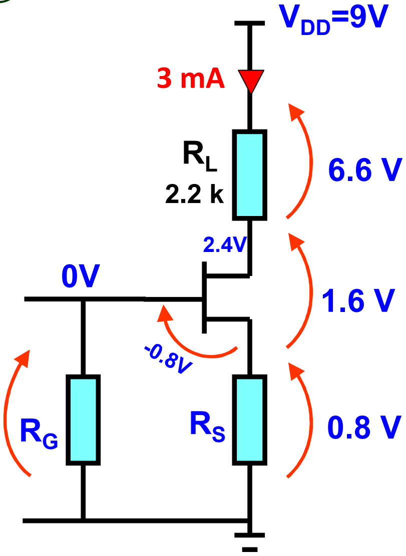
$$I_D = 8.34\left(1 - \frac{0.8}{2}\right)^2 = 3\ mA$$

$$V_S = I_D R_S = 3 \text{ x } 267 = 0.8V$$

$$V_L = I_D R_D = 3 \text{ x } 2200 = 6.6V$$

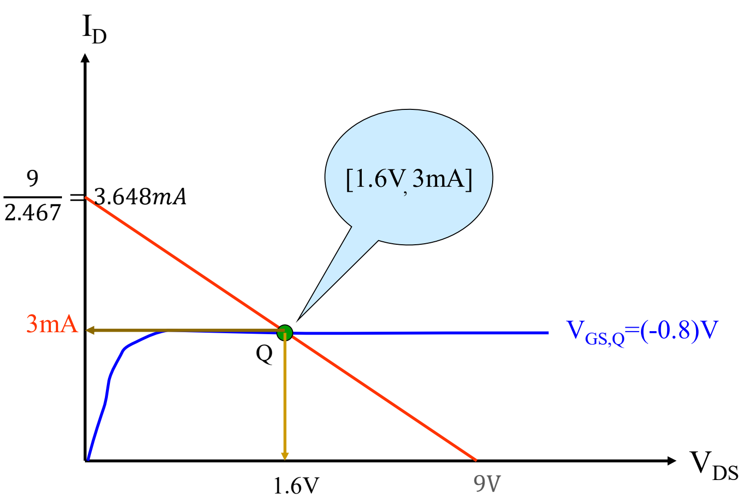
$$V_D = 9 - 6.6 = 2.4 \text{ V}$$

$$V_{DS} = 2.4 - 0.8 = 1.6 \text{ V}$$



78

Design (cont.) : Operating Point



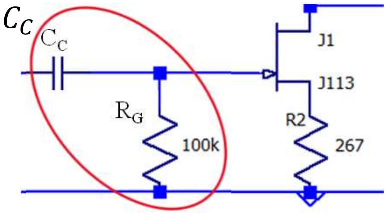
Design (Cont.) : Input Interface with Source

- Input Impedance
  - Too low : Loading on the source i.e Guitar pickup.
  - Too high : Circuit will be noisier due to the thermal noise of the resistor
  - 100 kΩ to 1 MΩ is OK.
  - Let us use a value of 100 kΩ for R_G

$$\tau = R_G . C_C$$

$$f_c = \frac{1}{2.\pi.\tau}$$

$$f_c = \frac{1}{2.\pi.R_G.C_C}$$



Design (Cont.) : Input Interface with Source

Assuming standard guitar;

We can choose the lower cutoff frequency as 82.4Hz

$$f_c = \frac{1}{2.\pi.R_G.C_C} = 82.4\text{Hz (assuming standard guitar)}$$

$$C_C = \frac{1}{2.\pi.R_G.f_c} = \frac{1}{2.\pi.(100{,}000).(82.4)} = 19.1 \text{ nF}$$

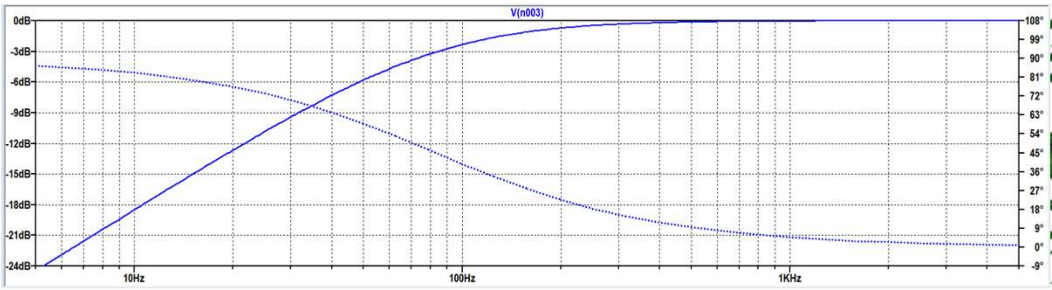
$$C_C > 19.1 \text{ nF}$$

Any higher value is OK. Therefore, we can choose a typical μF value.

Design (Cont.) : Input Interface with Source

When $C_C = 19.1$ nF; $f_c = \dfrac{1}{2.\pi.R_G.C_C} = 82.4\text{Hz}$

Use the command; .ac dec 10 0.1 2000

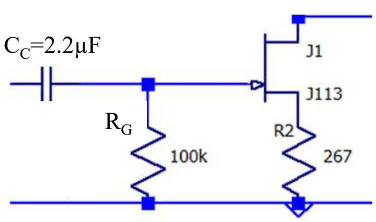


However, $X_c = \dfrac{1}{2.\pi.f.C_C} = \dfrac{1}{2.\pi.(82.4).(19.1)} \approx 100k\Omega\,!\,(too\ much)$

For C_C any higher value is OK. Therefore, we can choose a typical µF value.

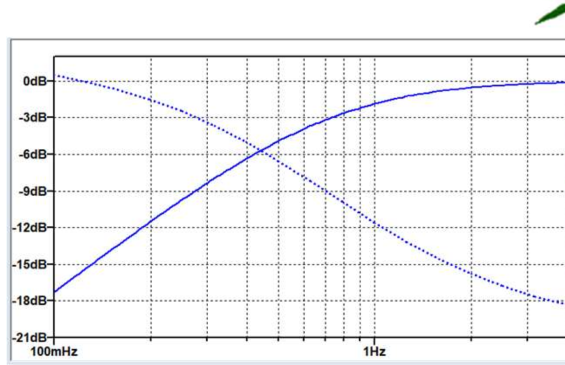
Design (Cont.) : Input Interface with Source

Let us use C_C=2.2µF



$$f_c = \frac{1}{2.\pi.R_G.C_C}$$

$$f_c = \frac{1}{2.\pi.(100).(2.2)}kHz = 0.7Hz$$



$$X_c = \frac{1}{2.\pi.f.C_C}$$

$$X_c = \frac{1}{2.\pi.(82.4).(2.2)}M\Omega$$

$$X_c = 878\Omega$$

Design (Cont.) : Output Interface with Load

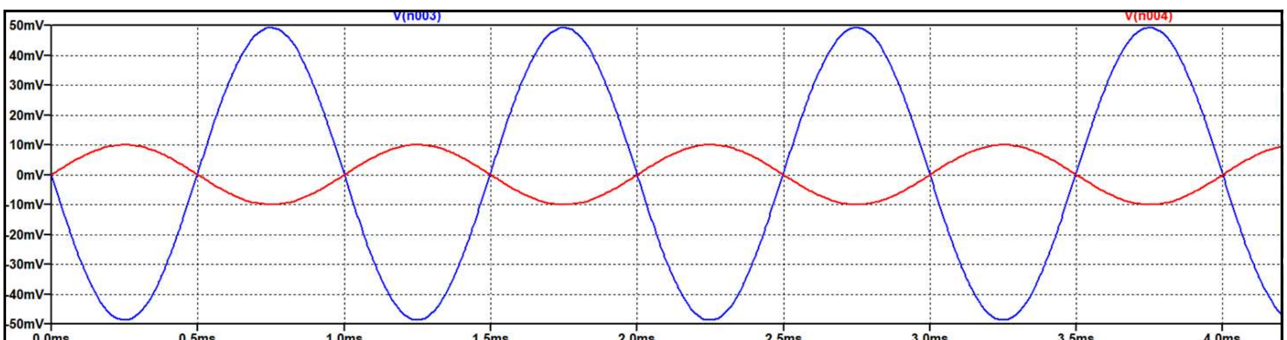
- Input impedance of the next stage?
  - Let us assume a standard and quite low value, such as 10kΩ.
  - Always make sure this is larger than R_D.

$$C_C = \frac{1}{2.\pi.R_L.f_c} = \frac{1}{2.\pi.(10{,}000).(82.4)} = 194 \text{ nF}$$

$$C > \ 194 \text{ nF}$$

- Any higher value is OK. Therefore, we can choose a typical μF value.
- E.g. 1μF coupling capacitor can give us a lower cut off frequency of 7 Hz.

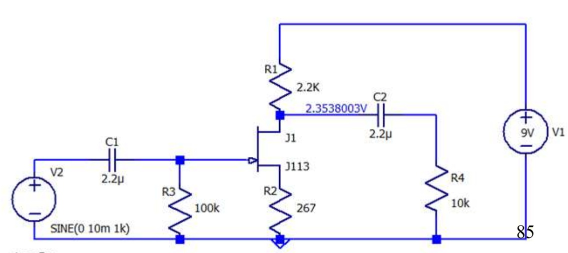
84



Self bias JFET Amplifier_Design Example

```
--- Operating Point ---

V(n001):      9
V(n002):      2.3538
V(p001):      0.806607
V(n005):      9.35467e-007
V(n004):      0
V(n003):      2.3538e-014
I(C2):        -2.3538e-018
I(C1):        2.05803e-027
Id(J1):       0.003021
Ig(J1):       -9.35467e-012
Is(J1):       -0.003021
I(R4):        2.3538e-018
I(R3):        9.35467e-012
I(R2):        0.003021
I(R1):        0.003021
I(V2):        2.05803e-027
I(V1):        -0.003021
```

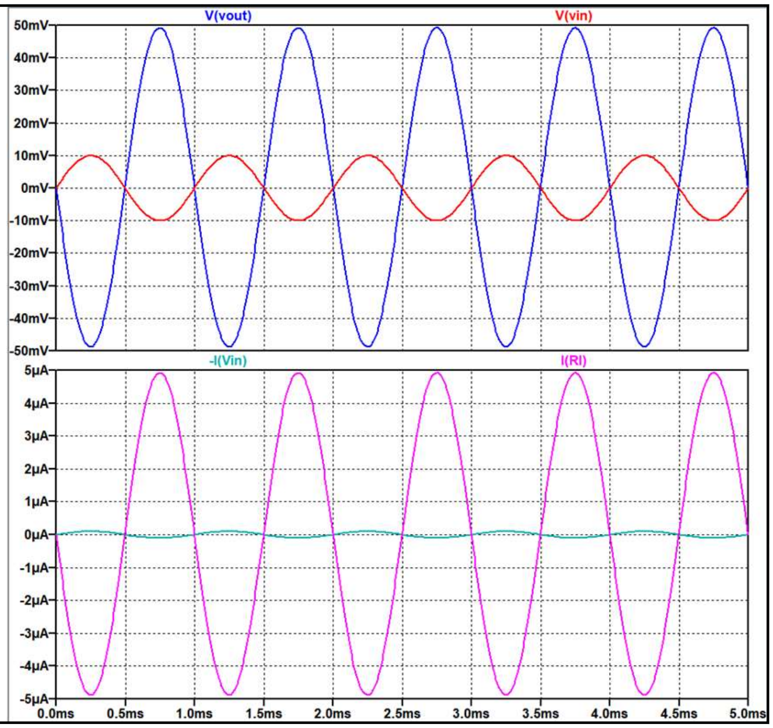


85

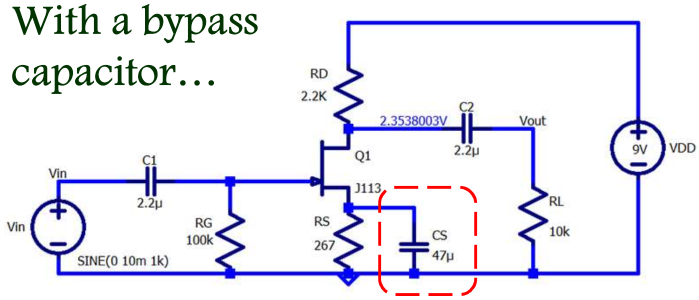
$$A_v = -\frac{V_{o,(pk-pk)}}{V_{i,(pk-p\ \ )}} = -\frac{100mV}{20mV} = -5$$

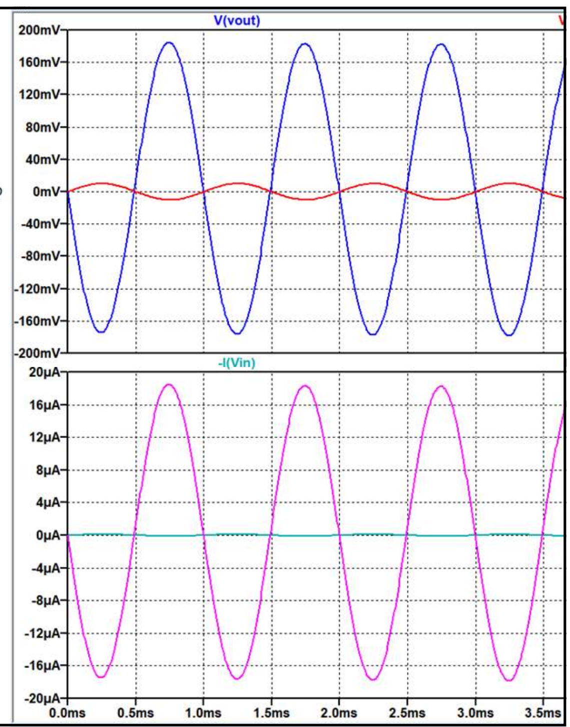
$$A_i = \frac{I_{o,(pk-pk)}}{I_{i,(pk-pk)}} = -\frac{10\mu A}{200nA} = 50$$

$$G = \frac{P_o}{P_i} = |A_v|.|A_i| = 5\ x50 = 250$$



With a bypass capacitor…



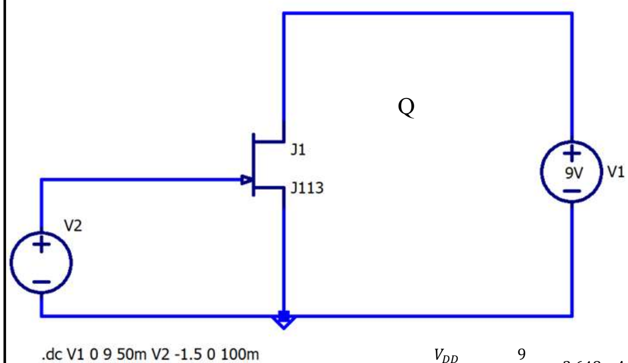


$$A_v = -\frac{V_{o,(pk-pk)}}{V_{i,(pk-pk)}} = -\frac{364mV}{20mV} = -18.2$$

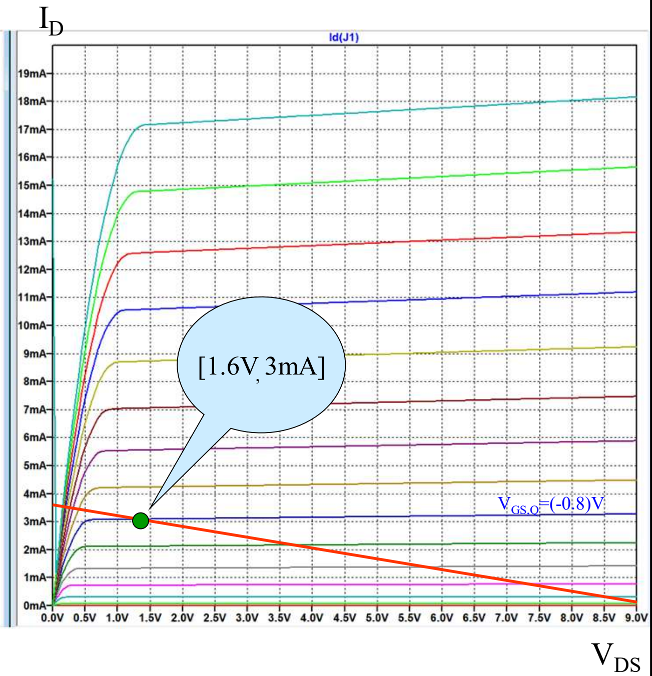
$$A_i = \frac{I_{o,(pk-pk)}}{I_{i,(pk-pk)}} = -\frac{36.4\mu A}{199.7nA} = 182.2$$

$$G = \frac{P_o}{P_i} = |A_v|.|A_i| = 18.2\ x182.2 = 3316 = 35.2dB$$

Graphical Illustration

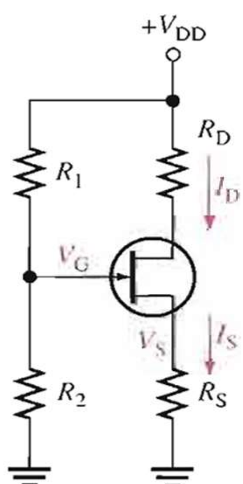


$$\frac{V_{DD}}{(R_S + R_L)} = \frac{9}{2.467} = 3.648mA$$



Ex. Draw AC load line and calculate the gains. Compare with simulator.

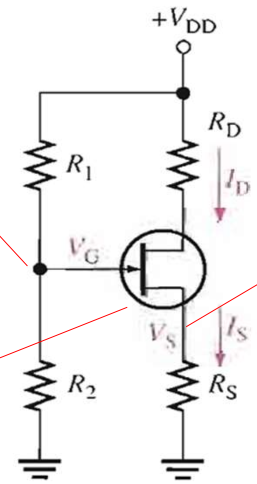
Potential Divider Biasing Method



89

Potential Divider Bias

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$$



$$V_S = I_D R_S$$

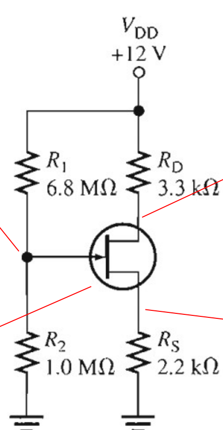
$$V_{GS} = V_G - V_S$$

90

Potential Divider Bias Example

$$I_D = \frac{V_{DD} - V_D}{R_D} = \frac{12\text{ V} - 7\text{ V}}{3.3\text{ k}\Omega} = \frac{5\text{ V}}{3.3\text{ k}\Omega} = \mathbf{1.52\text{ mA}}$$

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} = 1.54V$$



$$V_D \approx 7V$$

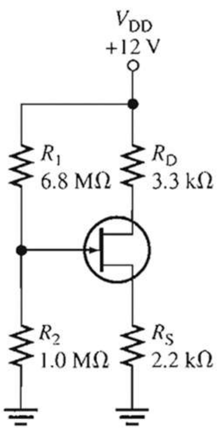
$$V_{GS} = V_G - V_S = -1.85V$$

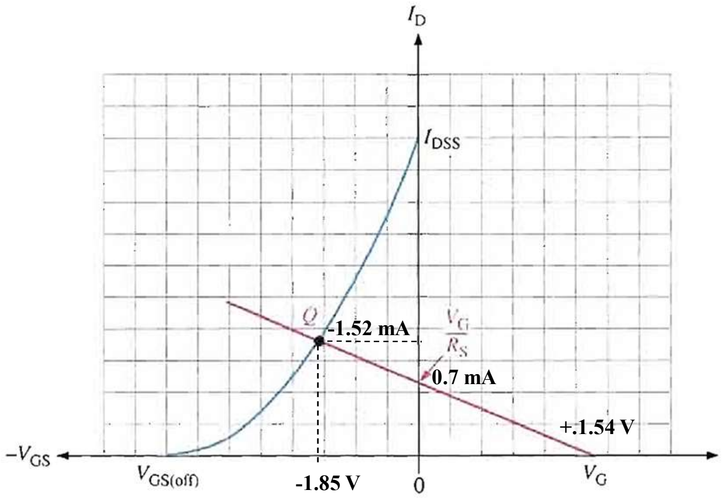
$$V_S = I_D R_S = 3.39V$$

91

DC Load Line…

on Static Mutual Characteristics

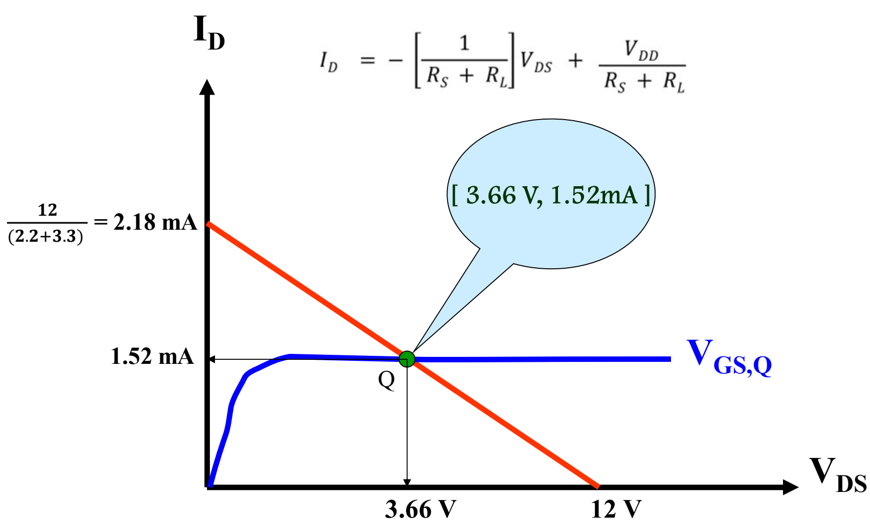


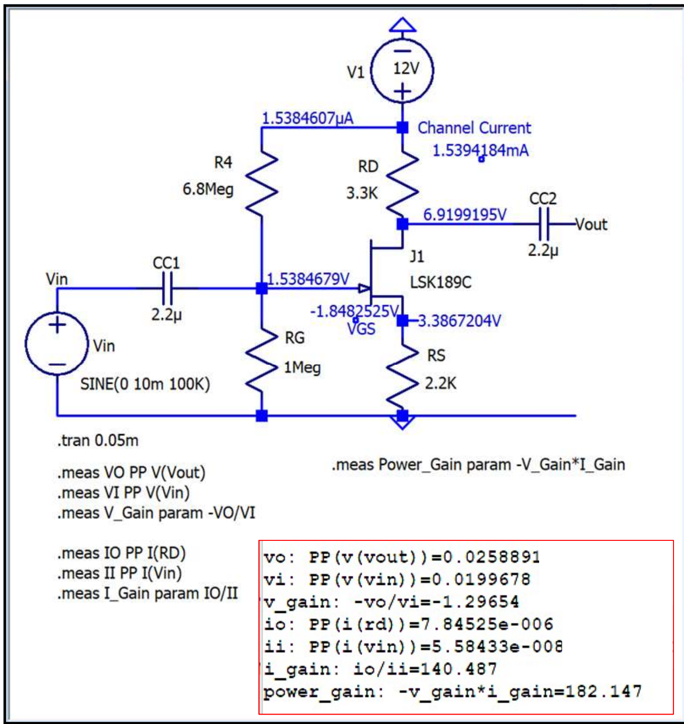


DC Load Line…

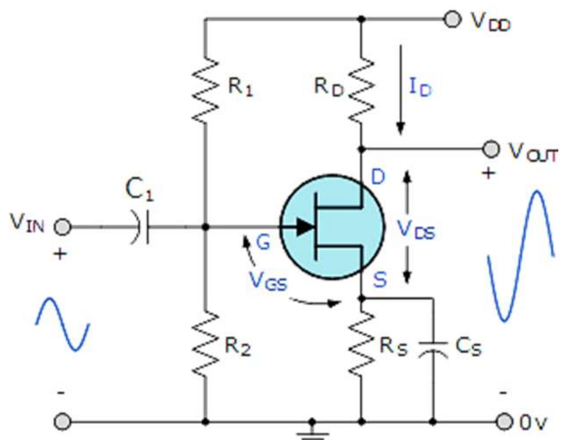
on Static Output Characteristics

$$I_D = -\left[\frac{1}{R_S + R_L}\right] V_{DS} + \frac{V_{DD}}{R_S + R_L}$$



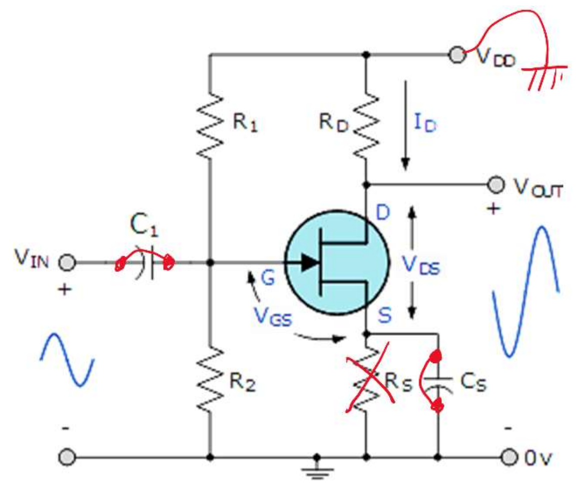


Use of Bypass Capacitors



95

AC Equivalent Circuit

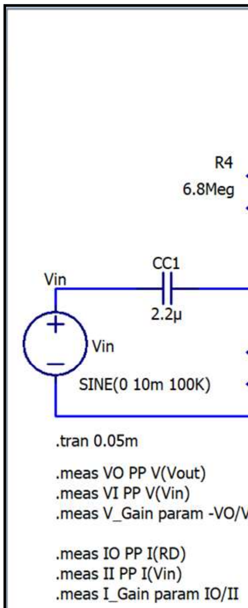


$v_{ds} + i_d R_D = 0$

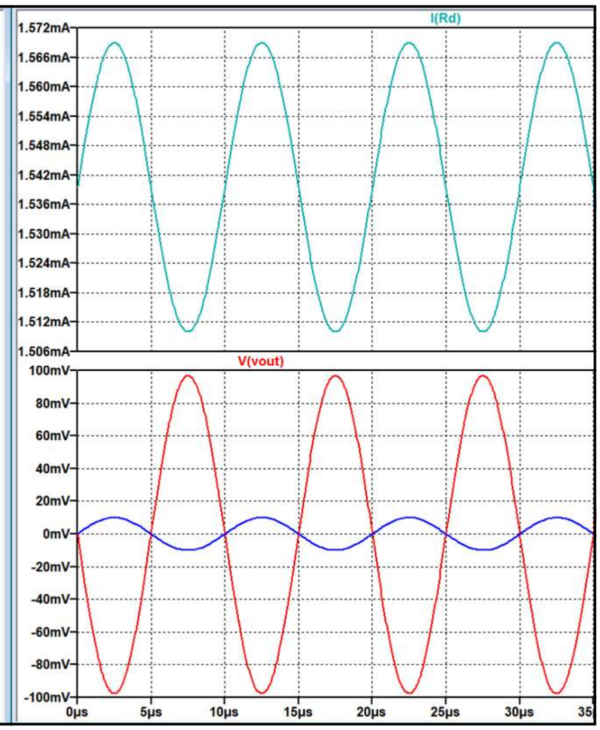
$i_d = \left(\frac{-1}{R_D}\right) v_{ds}$

Gradient

96




```
vo: PP(v(vout))=0.194613
vi: PP(v(vin))=0.019993
v_gain: -vo/vi=-9.73406
io: PP(i(rd))=5.89735e-005
ii: PP(i(vin))=2.46457e-007
i_gain: io/ii=239.285
power_gain: -v_gain*i_gain=2329.21
```



AC Load Line and Gain Calculations….

- Coupling and Bypass capacitors can be considered as S/C connections for ac signals
- Draw an ac equivalent circuit
- Using KVL for ac signals find the new gradient of the load line
- Draw ac load line with that gradient to go through the Q point.
- Then use ac load line for gain calculations

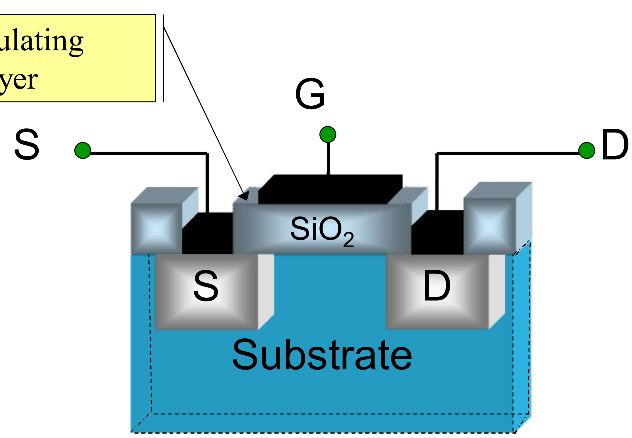
98

Moving on to MOSFET….

Watch: 1. https://youtu.be/Bine_PbyFSQ
2. https://youtu.be/rkbjHNEKcRw

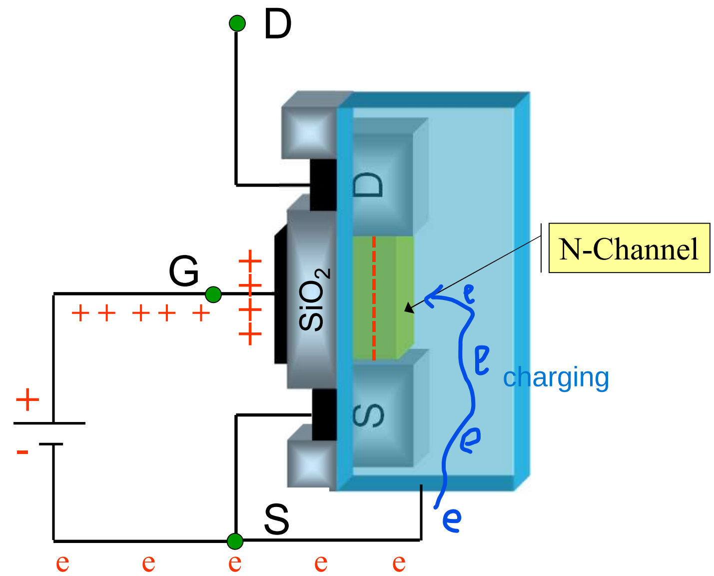
Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET)

MOSFET

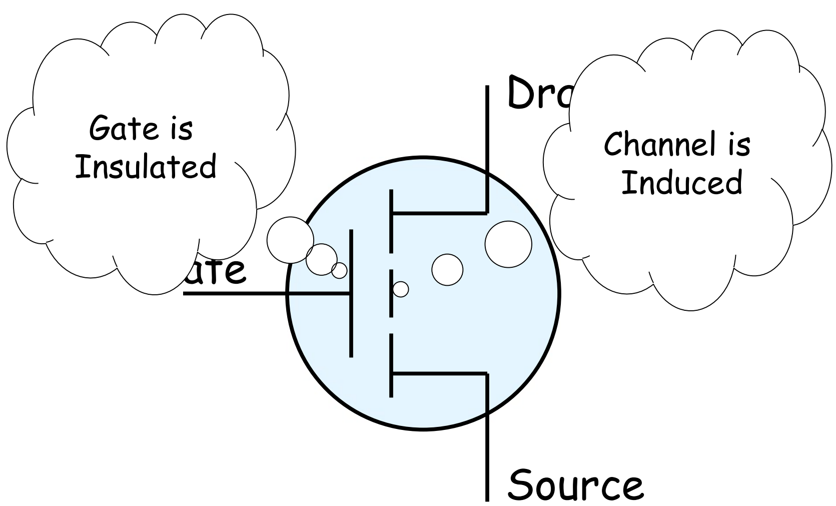


101

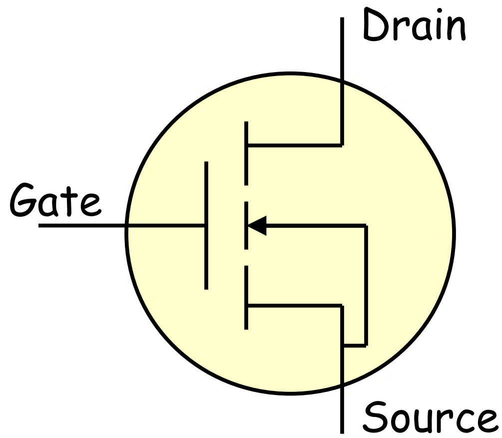
Induced N-Channel



Idea of EMOSFET Symbol

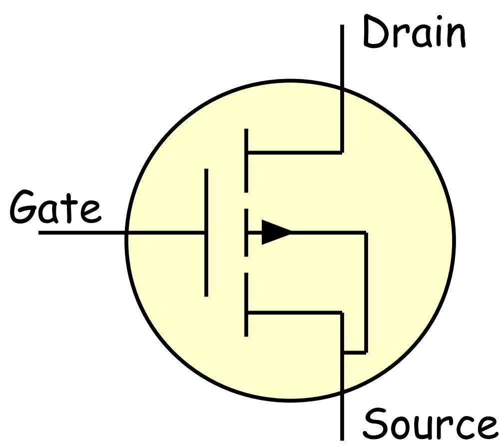


Normally-OFF Type
N-Channel



104

Normally-OFF Type
P-Channel

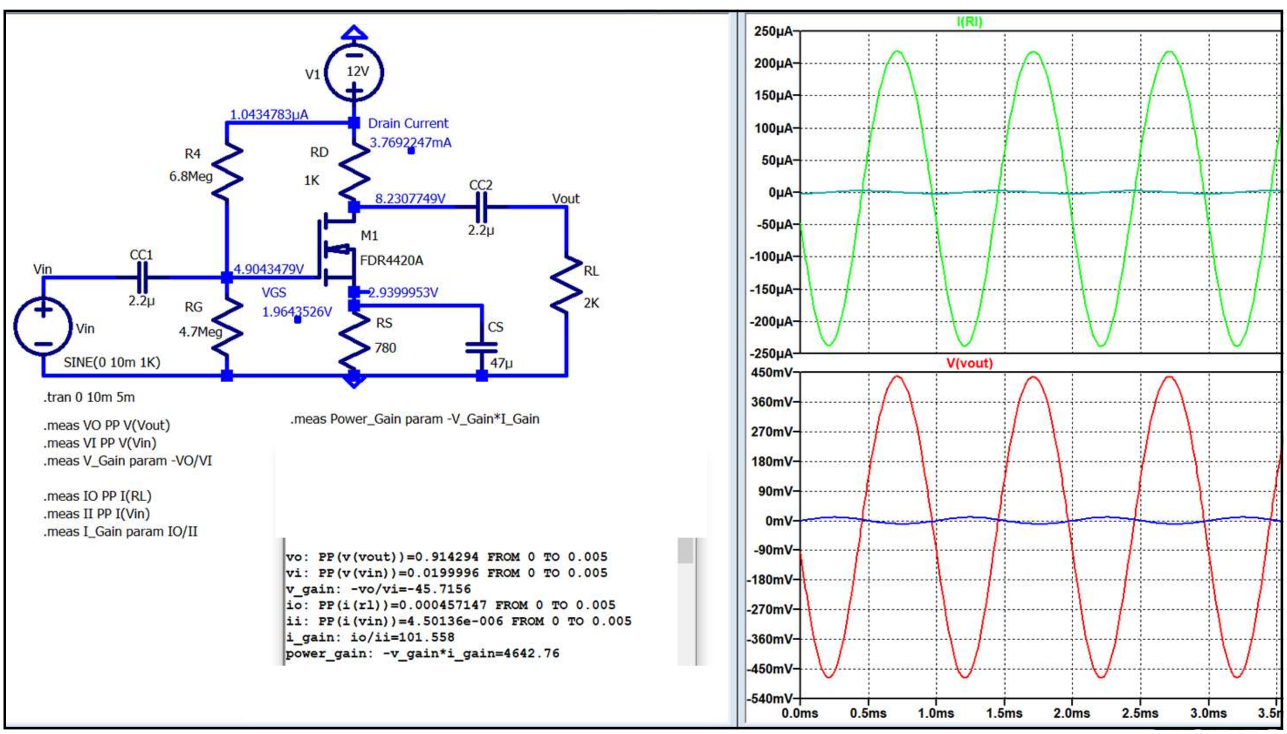


105

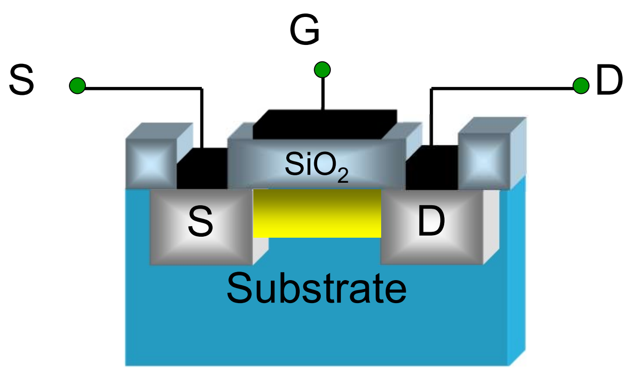
Handle with Care

- The insulating layer is extremely thin and can be easily damaged by static charges.
- The workplace must be grounded safely.
- Touch some earthed point just before handling static sensitive devices
- Some devices have Zener diodes built in, between gate and source, for protection.
- Soldering iron tips must be earthed. You must be grounded via a wriststraps

106

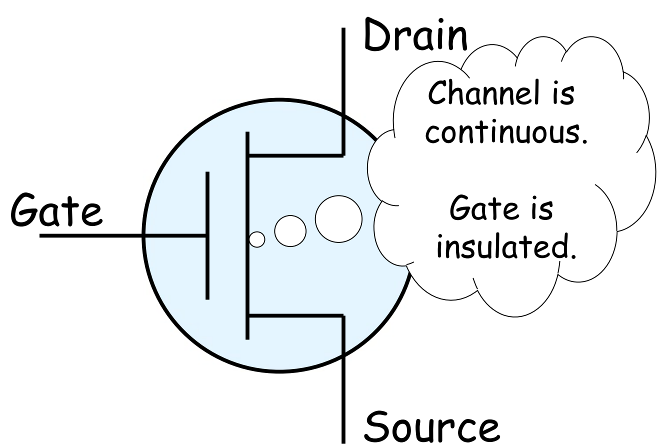


DMOSFET



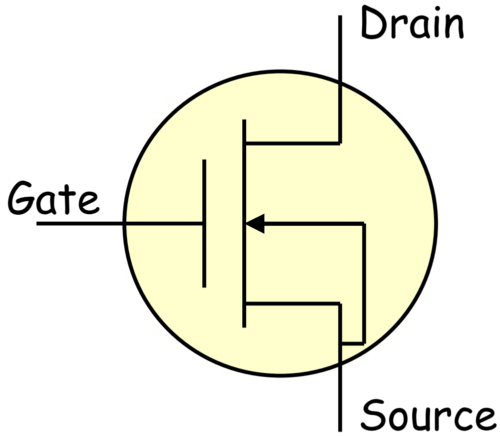
108

Idea of DMOSFET Symbol



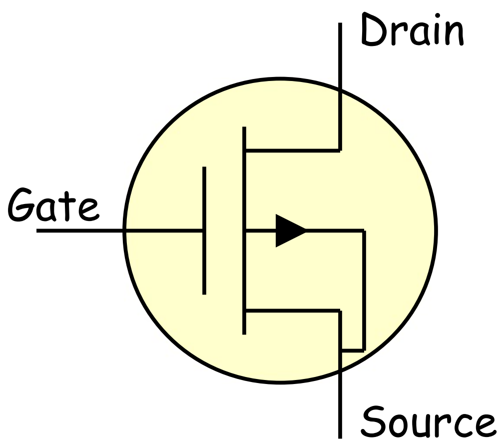
109

Normally-On Type
N-Channel



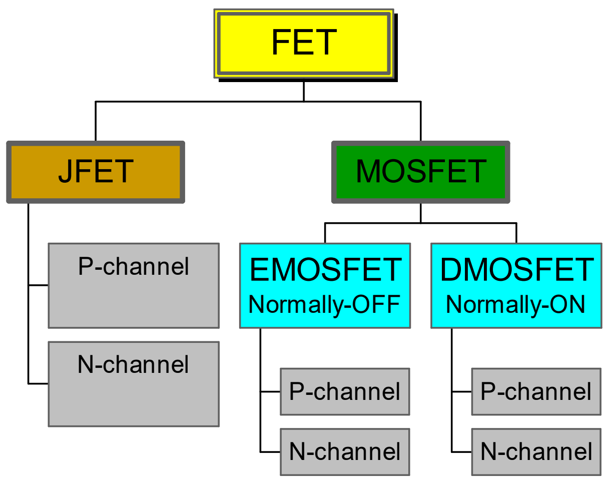
110

Normally-On Type
P-Channel



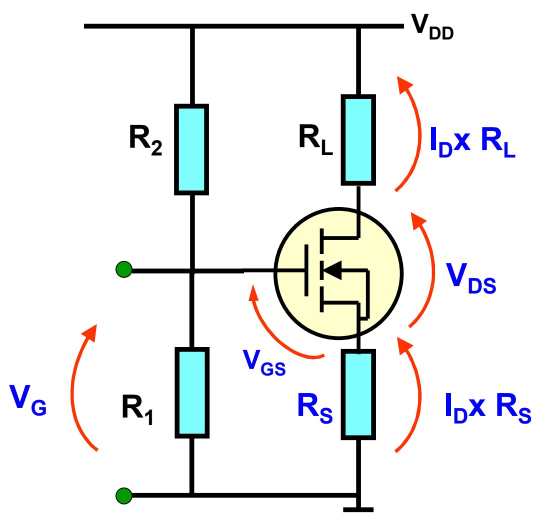
111

FET Classification



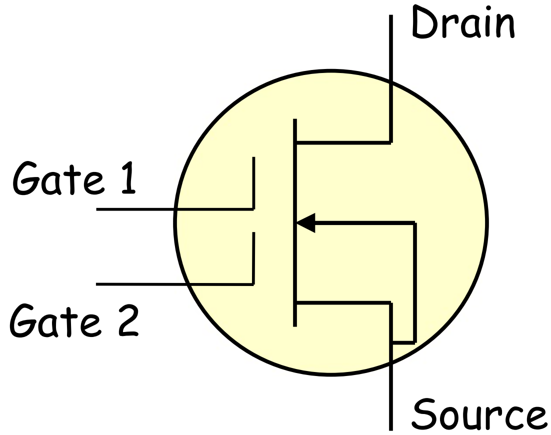
112

With Potential Divider Bias…



113

Dual Gate FETS

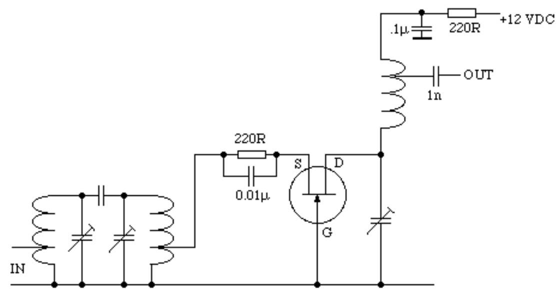


114

Some RF Applications

RF Stage of a Radio
Common Gate Amplifier

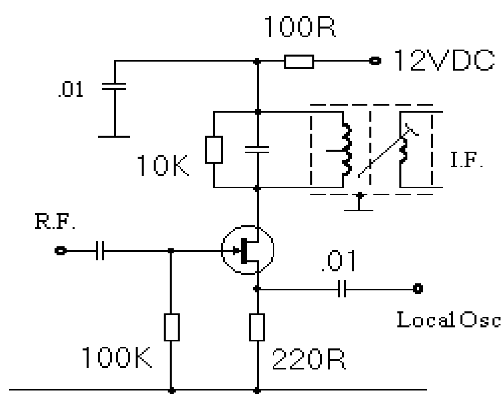
Widely used in VHF and UHF receivers



The grounded gate FET amplifer has 10 to 15dB of gain, and a low noise figure

116

FET Mixers in a Radio



A Mixer Down-converts RF to IF

117