070

UNIVERSITY OF MORATUWA

Faculty of Engineering

Department of Electronic and Telecommunication Engineering

B.Sc. Engineering

Semester 2 (2021 Batch) Examination

EN1014 ELECTRONIC ENGINEERING

Time allowed: *Three (3)* hours — July 2023

INSTRUCTIONS TO CANDIDATES:

- This paper contains 5 questions on 6 pages.
- Answer **all** questions.
- This paper contains **two** sections. Use a **separate** answer book for each section.
- All questions carry **equal** marks.
- This examination accounts for **60%** of the module assessment. The total maximum mark attainable is **100**. The marks assigned for each question & sections thereof are indicated in square brackets.
- The symbols used in this paper have their usual meanings.
- This is a **closed-book** examination.
- Electronic/communication devices are not permitted. Only equipment allowed is a calculator approved and labeled by the Faculty of Engineering.
- Derivations are not required if they are not explicitly requested in the question.
- Assume reasonable values for any data not given in or with the examination paper. Clearly state such assumptions.
- If you have any doubt as to the interpretation of the wording of a question. make your own decision. and clearly state it.

ADDITIONAL MATERIAL:

- No additional material is provided.

SECTION A

Question 1.

(a) i. What are the advantages of lumped abstractions in electronic product design? [2 marks]

ii. A microwave oven uses a magnetron unit to produce microwave energy for heating/cooking food. The concept of central control should be implemented in the design of a microwave oven. Draw a module-level abstraction of the microwave oven. [4 marks]

(b) In the circuit shown in Figure Q1(b), the input source produces a sinusoidal waveform of 7 V amplitude.

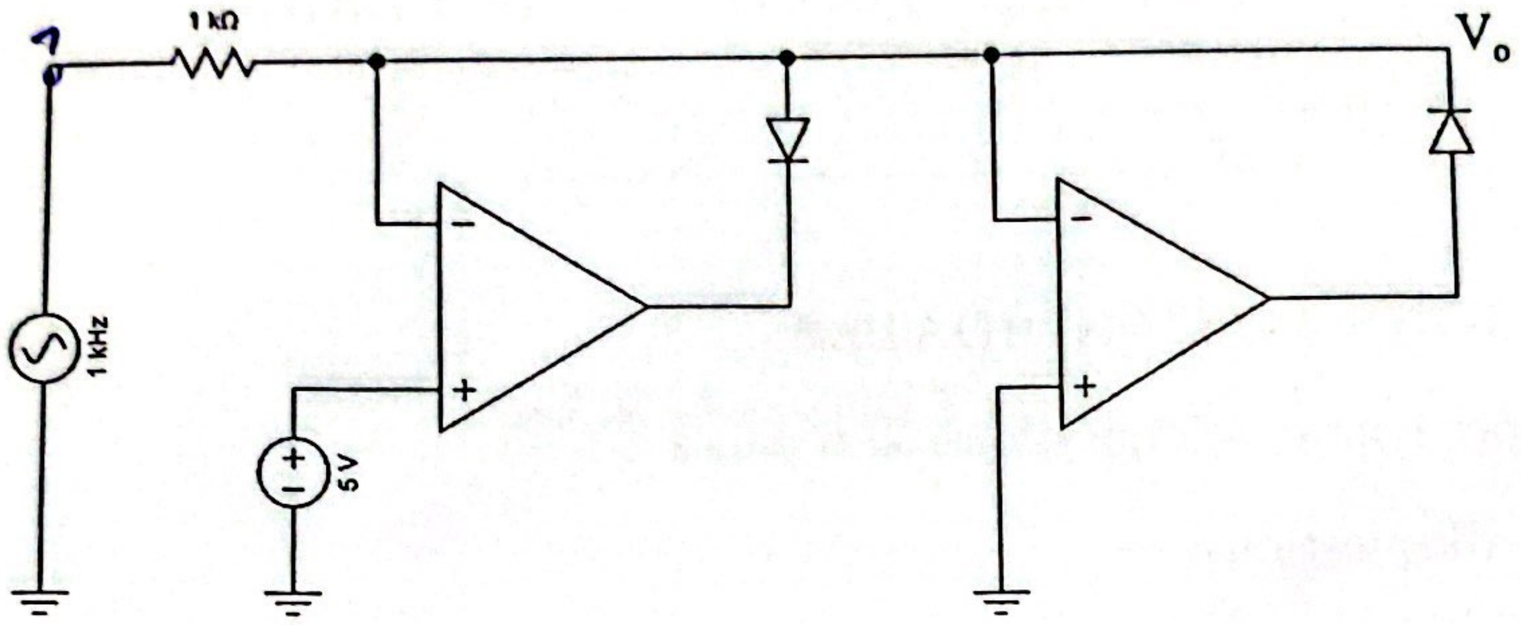

Figure Q1(b)

i. Sketch the output waveform. [6 marks]

ii. Identify the function of the circuit. [1 mark]

iii. What is the effect of the forward voltage drop of the diodes on the output waveform? [1 mark]

(c) Derive the equation of the output signal (V_o) for the circuit given in Figure Q1(c). [6 marks]

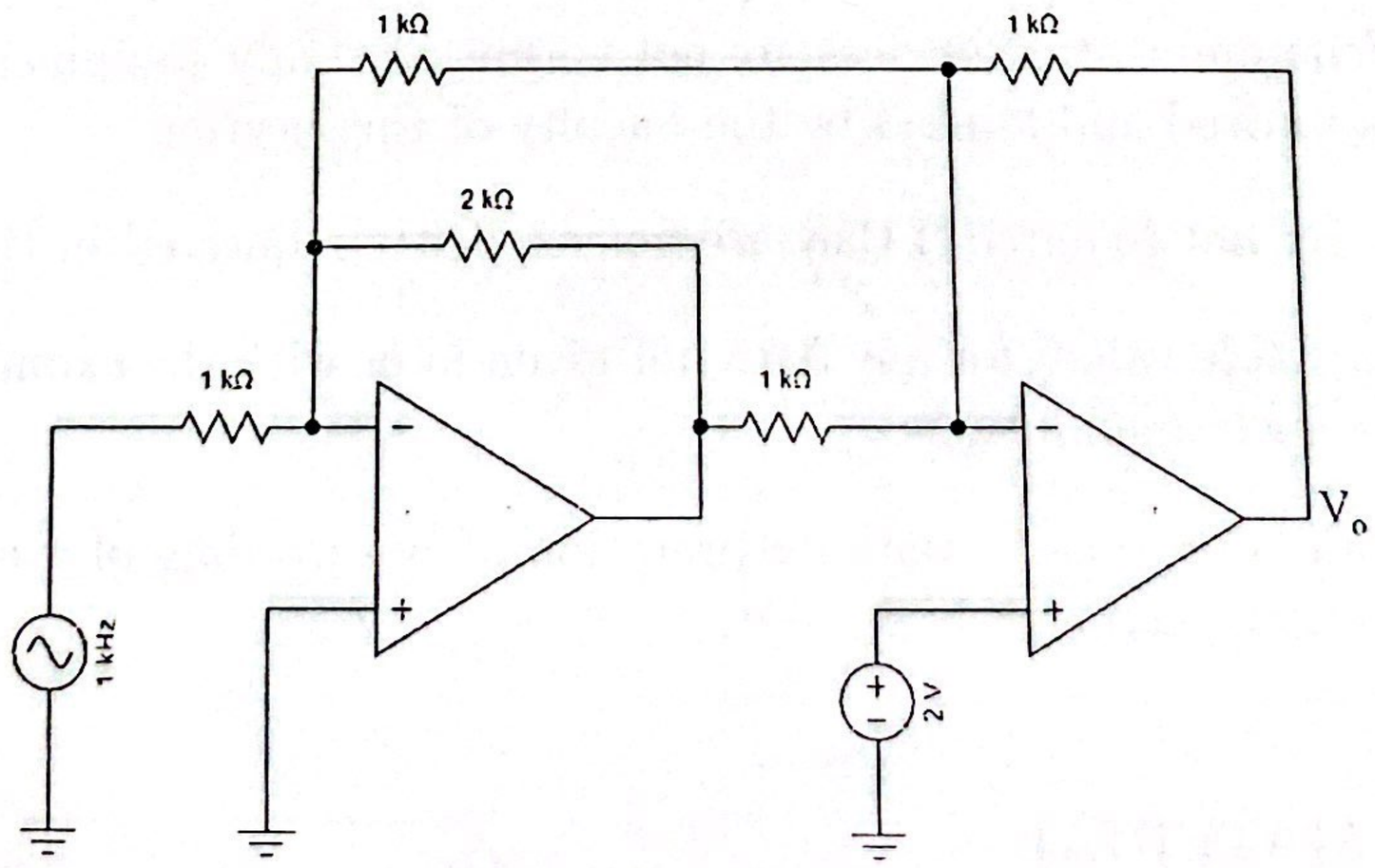

Figure Q1(c)

Question 2.

(a) The 50 Hz sinusoidal input waveform in Figure Q2 has a peak voltage of 6 V.

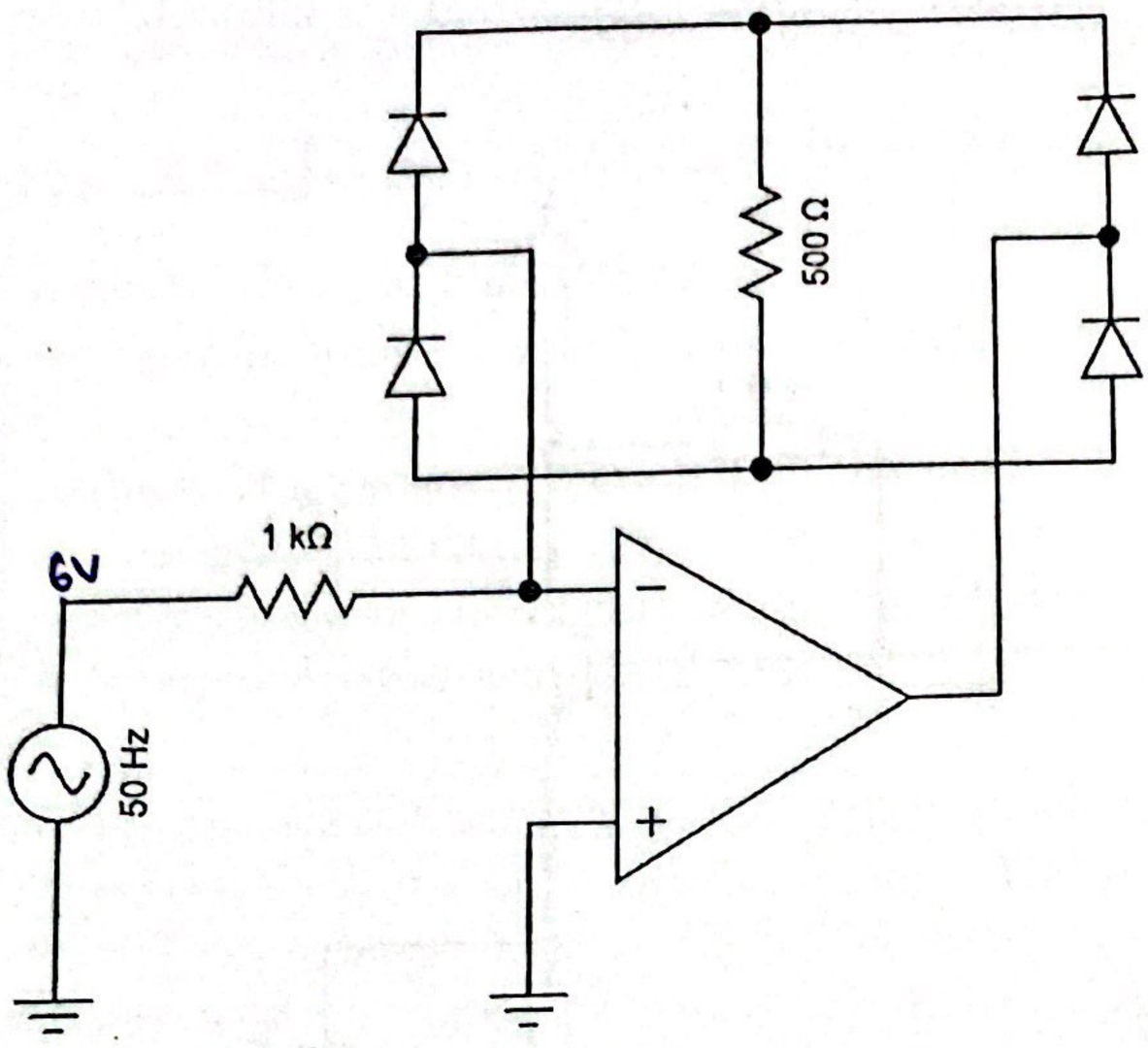

Figure Q2

i. Draw the current waveform through the 500 Ω load resistor. [3 marks]

ii. Draw the voltage waveform across the 500 Ω load resistor. [2 marks]

iii. Find the average (DC) voltage through the load. [3 marks]

iv. Comment on the value and the waveshape of voltage across the load if a high value smoothing capacitor is connected across the 500 Ω load resistor. [4 marks]

(b) A simple Zener regulator circuit uses a series resistance of 100 Ω and a Zener diode which has following characteristics:

- $V_Z = 12$ V
- $I_{ZK} = 10$ mA
- $Z_Z = 0$
- Max(PD) = 1.14 W.

Input to the Zener regulator is a smoothened DC voltage of 18 V from a rectifier circuit. Output of the regulator is fed to a variable load resistor which has an average value of 1.2 kΩ.

i. Investigate whether the regulator can maintain voltage regulation against a source voltage variation of ±20% and a load current variation of ±30% that occur independently. [5 marks]

ii. What is the maximum percentage (%) load current variation it can handle if the source voltage variation remains the same as in (b)i. [3 marks]

Question 3.

An audio amplifier circuit is given in Figure Q3. The bipolar junction transistor used in this amplifier has a static current gain of 100. Base-Emitter junction dynamic input resistance is 1 kΩ. The input audio signal is a sinusoidal waveform with a peak voltage of 5 mV.

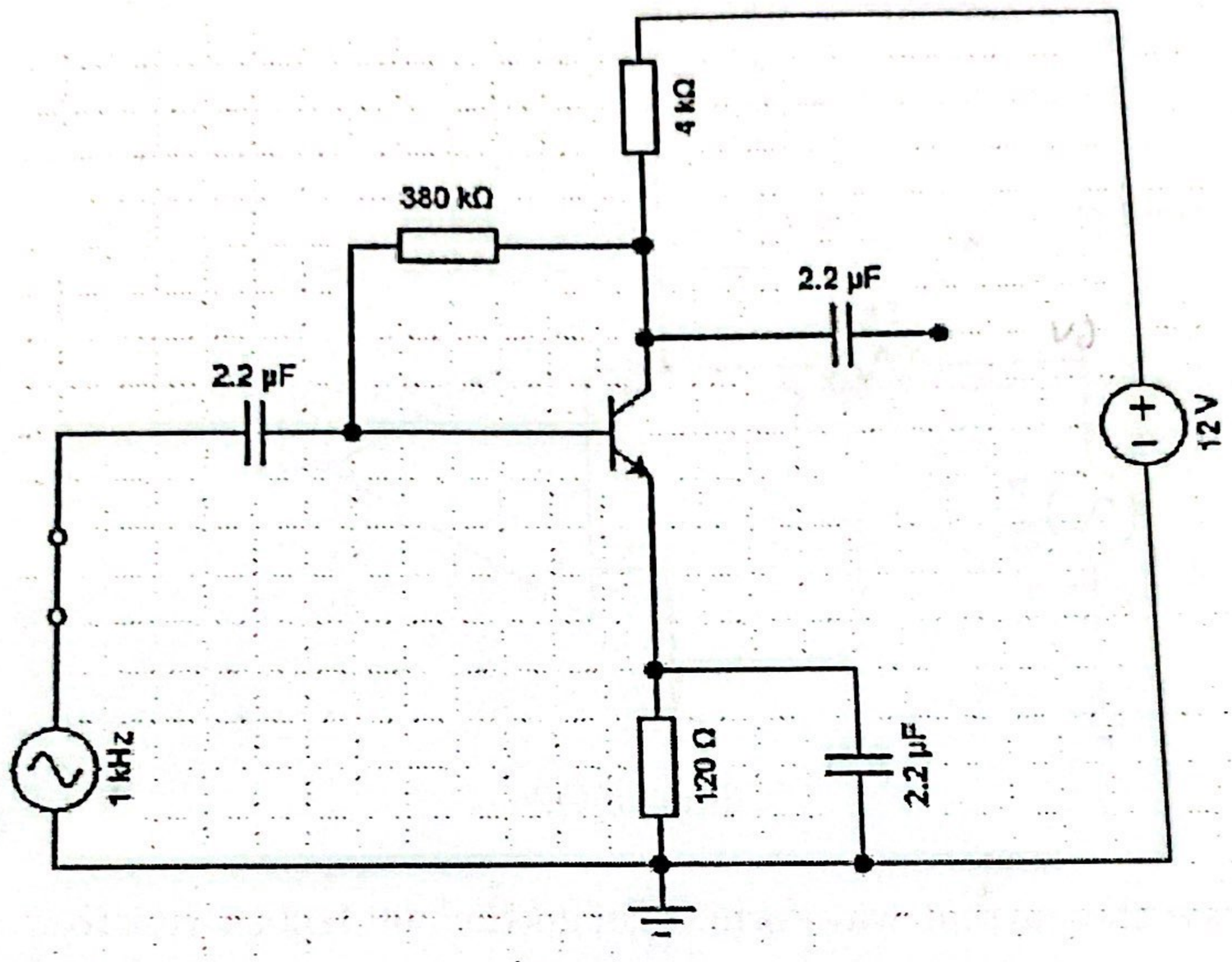

Figure Q3

(a) Name the biasing techniques used in this design. [1 mark]

(b) What are the advantages of this biasing technique over the fixed-bias? [2 marks]

(c) Derive the equation of the DC load line. Clearly state your assumptions. [3 marks]

(d) Find out the quiescent base current ($I_{B,Q}$). [3 marks]

(e) Sketch the DC load line and mark the co-ordinates of the Q-point. [2 marks]

(f) Derive the equation of the AC load line and sketch the AC load line. [4 marks]

(g) It was observed that the collector current rises to a maximum of 1.5 mA during the operation. Calculate the current gain, voltage gain and the power gain of the amplifier. Clearly state your assumptions. [5 marks]

SECTION B

Question 4.

(a) Consider the following 5-variable Boolean function

$$f(a,b,c,d,e) = \prod(1,3,5,7,8,10,17,18,19,26,28) \cdot D(0,2,21,23,24),$$

where $D(\cdot)$ denotes don't care maxterms.

i. Draw the corresponding 4-variable Karnaugh maps for the two cases: $a = 0$ and $a = 1$. [3 marks]

ii. Hence, express the Boolean function f in the *product-of-sums* form with a minimal number of literals. [6 marks]

iii. Draw the realization of the digital circuit corresponding to the simplified Boolean function f using a minimal number of 2-input and 3-input NOR gates. [3 marks]

(b) Consider the design of a 4-input (D_0 to D_3) priority encoder having the 2-bit output Y_1Y_0, where Y_1 is the most significant bit. The priority encoder has another output V to indicate at least one of the four inputs is present. The priority increases with the subscript of the input, i.e., the input D_3 has the highest priority whereas the input D_0 has the lowest priority.

The output Y_1 of the priority encoder is implemented using *only two* 4×1 multiplexers with *active-low* enable inputs, *one* 2-input OR gate and *one* NOT gate.

i. Construct the truth table for Y_1 by selecting the binary variable D_0 as the input to the multiplexers. [4 marks]

ii. Draw the realization of the digital circuit corresponding to Y_1. Clearly indicate all the inputs and the outputs of the multiplexers. [4 marks]

Question 5.

(a) Express an advantage and a disadvantage of a Moore machine compared to a Mealy machine. [2 marks]

(b) Consider the design of a sequential logic circuit (having one input and one output) that can detect 101 bit stream *without overlaps*. This circuit is designed as a Moore machine and is implemented using *JK* flip-flops.

i. Draw the corresponding state diagram. [5 marks]

ii. Obtain the binary-coded state table. [3 marks]

iii. Based on the excitation table of a *JK* flip-flop, derive the simplified Boolean expressions for the flip-flop input equations. [6 marks]

iv. Derive the simplified Boolean expression for the output equation. [1 mark]

v. Draw the realization of the sequential logic circuit using *JK* flip-flops, 2-input and 3-input AND gates and OR gates, and NOT gates. [3 marks]

- End of Question Paper -