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-- Company:
-- Engineer: Olasubomi Borishade
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-- Create Date: 02/04/2026 07:10:07 PM
-- Design Name: Rotational Logic Block
-- Module Name: Rotational_Logic_Block - Behavioral
-- Project Name: EENG 5560 Homework 2

-- Description: A logical block that can shift an input A by the magnitude of
another
-- input B either left or right

-- Revision:
-- Revision 0.01 - File Created
-- Additional Comments:
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use work.OPERATIONS_ARRAY_CUSTOM_PACK.ALL;
use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Rotational_Logic_Block is
    Generic (d_w: integer:= 3);

    Port (  A : in STD_LOGIC_VECTOR (d_w - 1 downto 0); -- Declaring A as a input
vector
            B : in STD_LOGIC_VECTOR (d_w - 1 downto 0); -- Declaring B as a input
vector
            OpSelR : in RLB_Operation; -- Declaring the operation selection signal
as an input vector
            Y : out STD_LOGIC_VECTOR (d_w - 1 downto 0) -- Declaring Y as a vector
            );

end Rotational_Logic_Block;

architecture Behavioral of Rotational_Logic_Block is
```

```
begin
CLB_proc: process (A, B, OpSelR)
begin
    case OpSelR is
        when rLSL =>
            Y <= to_stdlogicvector(to_bitvector(A) sll to_integer(unsigned(B)));

        when rLSR =>
            Y <= to_stdlogicvector(to_bitvector(A) srl to_integer(unsigned(B)));

        when NoOp =>
            Y <= (others => '0');

        when others =>
            Y <= (others => '0');

    end case;
end process;
end Behavioral;
```