# SIC1182K
# SCALE-iDriver Family

Up to 8 A Single Channel SiC MOSFET Gate Driver Providing Advanced Active Clamping and Reinforced Isolation up to 1200 V

## Product Highlights

### Highly Integrated, Compact Footprint

- ±8 A peak gate output current
- Integrated FluxLink™ technology providing reinforced isolation
- Advanced Active Clamping
- UVLO primary and secondary side
- Over-current fault turn-off
- Short-circuit current fault turn-off
- Rail-to-rail stabilized output voltage
- Unipolar supply voltage for secondary-side
- Suitable for 600 V / 650 V / 1200 V SiC MOSFET switches
- Up to 150 kHz switching frequency
- Propagation delay jitter ±5 ns
- -40 °C to +125 °C operating ambient temperature
- High common-mode transient immunity
- eSOP package with 9.5 mm creepage and clearance

### Protection / Safety Features

- Undervoltage lock-out protection for primary and secondary-side including fault feedback
- Over-current detection for SiC MOSFETs with current-sense terminal
- Ultrafast short-circuit monitoring
- Turn off overvoltage limitation (Advanced Active Clamping)

### Full Safety and Regulatory Compliance

- 100% production partial discharge test
- 100% production HIPOT compliance testing
- Reinforced insulation VDE V 0884-10 certified
- UL 1577 recognition pending

### Green Package

- Halogen free and RoHS compliant

### Applications

- General purpose and servo drives
- UPS, PV, welding inverters and power supplies
- Other industrial applications

## Description

The SIC1182K is a single channel gate driver in an eSOP-R16B package for SiC MOSFETs. Reinforced galvanic isolation is provided by Power Integrations' revolutionary solid insulator FluxLink technology. Up to ±8 A peak output drive current enables the product to drive devices with nominal currents of up to 600 A (typical).

Additional features such as undervoltage lock-out (UVLO) for primary-side and secondary-side and rail-to-rail output with temperature and process compensated output impedance guarantee safe operation even in harsh conditions.

Furthermore, this gate driver IC comes along with a new feature, combining short-circuit protection (at and during turn-on phase) as well as overvoltage limitation by advanced active clamping (at turn-off phase) through a single sensing pin. In case driven semiconductor provides a current-sense terminal, an adjustable over-current detection can be realized.

**Product Portfolio**

| Product[1] | Peak Output Drive Current |
|---|---|
| **SIC1182K** | 8.0 A |

Table 1. *SCALE-iDriver Portfolio.*
Notes:
1. Package: eSOP-R16B.


Figure 2. *eSOP-R16B Package.*

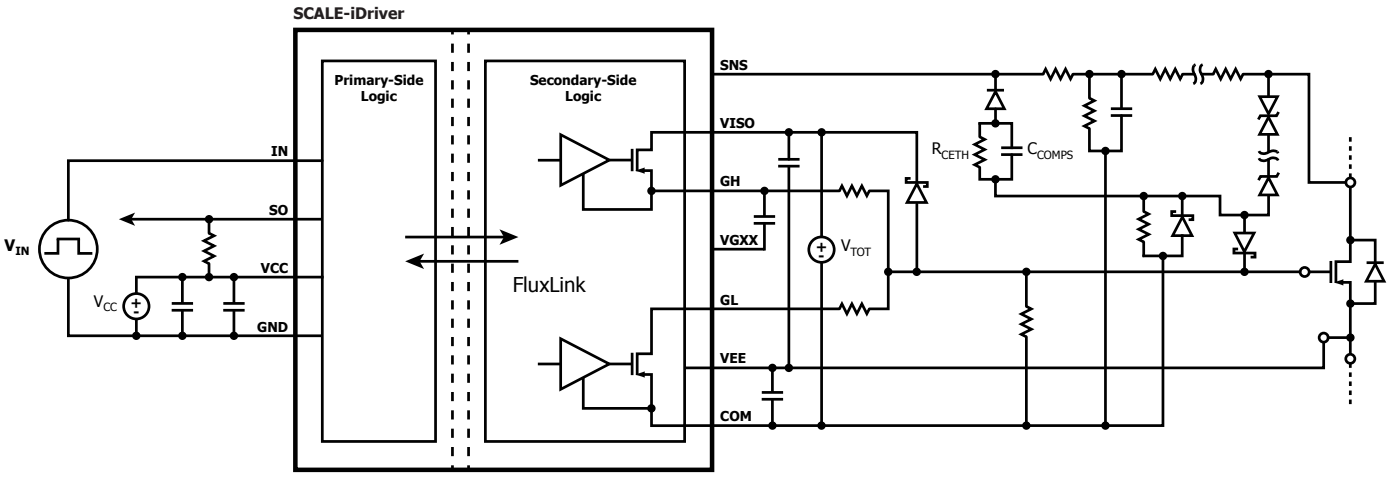



Figure 1. *Typical Application Schematic.*

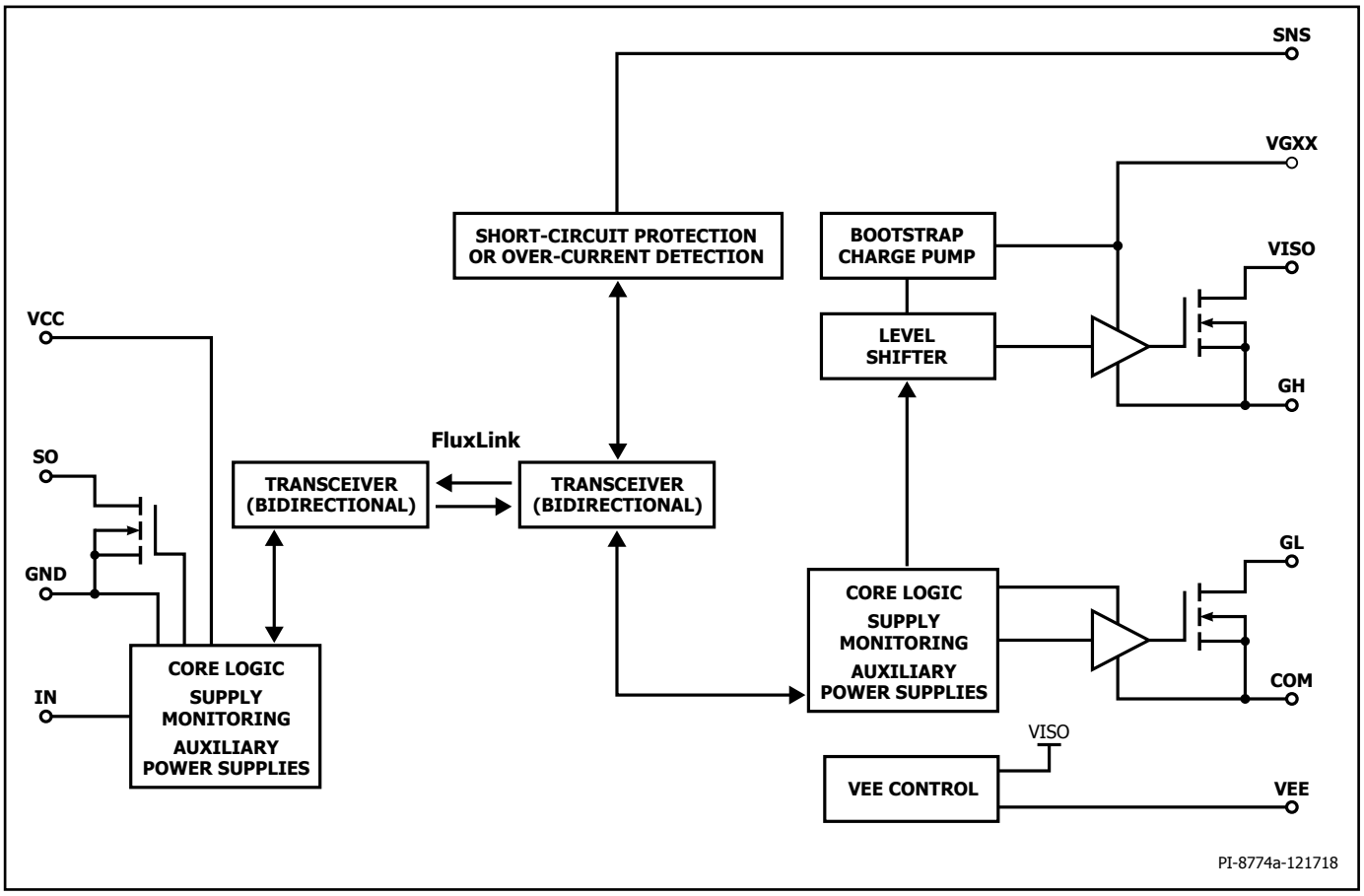



Figure 3. *Functional Block Diagram.*

## Pin Functional Description

**VCC Pin (Pin 1)**
This pin is the primary-side supply voltage connection.

**GND Pin (Pin 3-6)**
This pin is the connection for the primary-side ground potential. All primary-side voltages refer to this pin.

**IN Pin (Pin 7)**
This pin is the input for the logic command signal.

**SO Pin (Pin 8)**
This pin is the output for the logic fault signal (open drain).

**NC Pins (Pin 9)**
This pin must be un-connected. Minimum PCB pad size for soldering is required.

**VEE Pin (Pin 10)**
Common (MOSFET source) output supply voltage.

**SNS Pin (Pin 11)**
This pin is the sense input detecting short-circuit events at turn-on and limiting overvoltages at turn-off.

**VGXX Pin (Pin 12)**
This pin is the bootstrap and charge pump supply voltage source.

**GH Pin (Pin 13)**
This pin is the driver output-sourcing current (turn-on) connection.

**VISO Pin (Pin 14)**
This pin is the input for the secondary-side positive supply voltage.

**COM Pin (Pin 15)**
This pin provides the secondary-side reference potential.

**GL Pin (Pin 16)**
This pin is the driver output-sinking current (turn-off) connection.

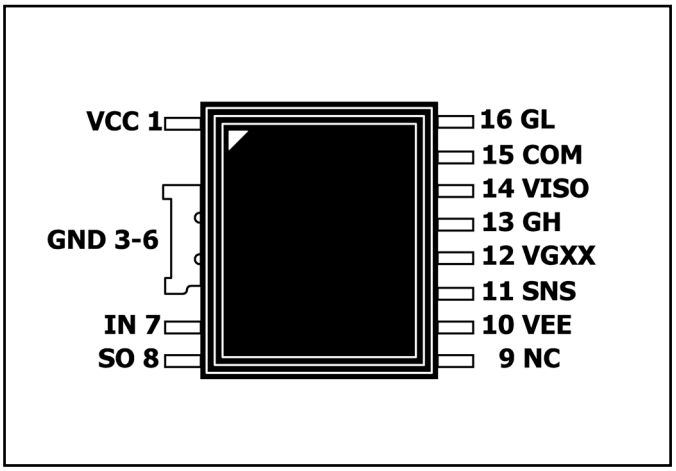



Figure 4. *Pin Configuration.*

## SCALE-iDriver SIC1182K Functional Description

The single channel SCALE-iDriver™ family SIC1182K drives SiC MOSFET semiconductor devices with a blocking voltage of up to 1200 V and provides reinforced isolation between superior controller and the semiconductor device. The logic input (PWM) command signal applied via IN and the primary supply voltage supplied via VCC are both referenced to GND. The working status of the semiconductor device and SCALE-iDriver is monitored via SO.

Command signals are transferred from the primary (IN) to secondary-side via FluxLink isolation technology. GH supplies a positive gate voltage and charges the semiconductor gate during the turn-on process. GL supplies a negative gate voltage and discharges the gate during turn-off process.

Short-circuit protection as well as overvoltage limitation can be implemented by connecting a network between SNS and drain terminal of the semiconductor device. In case of a turn-on event SNS senses short-circuits, which will lead to a driver initiated turn-off to protect the semiconductor device from short-circuit damage. In case of a turn-off event SNS senses turn-off overvoltages and limits them by (Advanced Active Clamping) to a save value below the semiconductor devices blocking voltage. In case the semiconductor device offers a current-sense terminal, an adjustable over-current detection can be realized as alternative to a short-circuit monitoring.

### Power Supplies

The SIC1182K is equipped with an integrated power and voltage failure management. These features control power turn-on and turn-off and generate a regulated secondary side bipolar supply voltage. Two supply voltages are required. One for the primary-side ($V_{VCC}$), which powers the primary-side logic and communication with the secondary (insulated) side. The other supply voltage ($V_{TOT}$) is required for the secondary-side as an unipolar voltage. $V_{TOT}$ is applied between VISO and COM. $V_{TOT}$ has to be insulated from the primary-side and should provide at least the same insulation capabilities as the SCALE-iDriver. $V_{TOT}$ should have a low coupling capacitance to the primary or any other secondary-side. The positive gate-source voltage is provided by $V_{VISO}$, which is internally generated and stabilized to 15 V (typically) with respect to VEE. The negative gate-source voltage is provided by $V_{VEE}$ with respect to COM. Due to the limited current sourcing/sinking capabilities of the VEE, any additional load needs to be applied between the VISO and COM. No additional load between VISO and VEE or between VEE and COM is allowed.

### Input and Fault Logic (Primary-Side)

The input (IN) logic is designed to work directly with higher level controllers using 5 V CMOS logic. It is recommended to use a pull-down resistor R1 close to the input pin of the SIC1182K.

If the physical distance between the controller and the SCALE-iDriver is large or if a different logic level is required, the resistive divider in Figure 6 is recommended. This solution adjusts the logic level as necessary and will also improve driver's noise immunity.

Gate driver commands are transferred from IN to GH (turn-on) and GL (turn-off) with a propagation delay $t_{P(LH)}$ and $t_{P(HL)}$.

During normal operation, when there is no fault detected, the SO pin stays at high impedance (open drain). Any fault is reported by connecting the SO pin to GND. SO stays low as long as $V_{VCC}$ (primary-side) stays below $UVLO_{VCC}$. If a short-circuit is detected or the supply voltages $V_{VISO}$, (secondary-side) drop below $UVLO_{VISO}$, the SO status changes with a delay time $t_{FAULT}$ and keeps status low for a time defined as $t_{SO}$. In case of a fault condition the driver applies the off-state (GL is connected to COM). During the $t_{SO}$ period, command signal transitions from IN are ignored. A new turn-on command transition is required before the driver will enter the on-state.

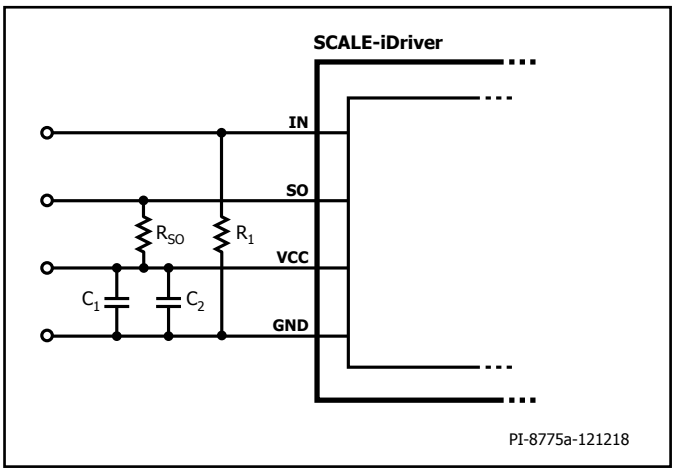



Figure 5. *Recommended Circuitry for Standard 5 V IN Logic Level.*

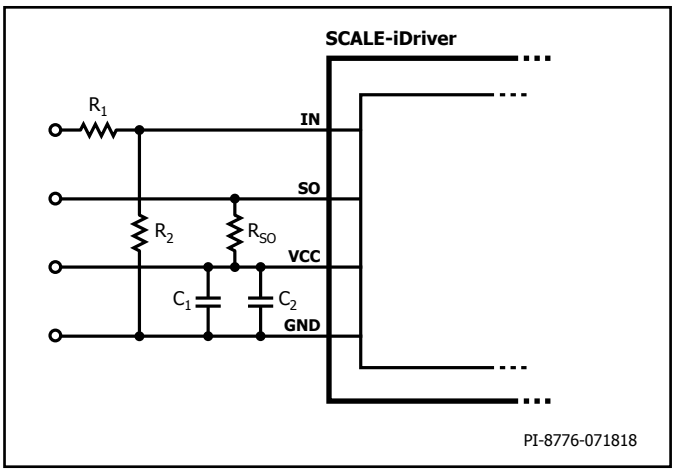



Figure 6. *Recommended Circuitry for Increased IN Logic Levels. For $R_1$ = 3.3 kΩ and $R_2$ = 1.2 kΩ the IN Logic Level is 15 V.*

### Output (Secondary-Side)

The gate of the semiconductor device to be driven can be connected to the SCALE-iDriver output via GH and GL, using two different resistor values. Turn-on gate resistor $R_{GON}$ needs to be connected to the GH pin and turn-off gate resistor $R_{GOFF}$ to GL. If both gate resistors have the same value, GL and GH can be connected together.
The SCALE-iDriver data sheet defines the $R_{GH}$ and $R_{GL}$ values as total resistances connected to the respective GH and GL. Note that most semiconductor device data sheets specify an internal gate resistor $R_{GINT}$ which is already integrated into the semiconductor device. In addition to $R_{GINT}$, external resistor devices $R_{GON}$ and $R_{GOFF}$ are specified to setup the gate current levels to the application requirements. Consequently, $R_{GH}$ is the sum of $R_{GON}$ and $R_{GINT}$. Careful consideration should be given to the power dissipation and peak current associated with the external gate resistors. The GH pin output current source ($I_{GH}$) of SIC1182K is capable of handling up to 7.8 A during turn-on, and the GL pin output current source ($I_{GL}$) is able to sink up to 7.3 A during turn-off. The SCALE-iDriver's internal resistances are described as $R_{GHI}$ and $R_{GLI}$ respectively. If the gate resistors for SCALE-iDriver attempt to draw a higher peak current, the peak current will be internally limited to a safe value.

**Safe Power-Up and Power-Down**
It is recommended during power-up and power-down that the IN pin stays at logic low. Any supply voltage related to VCC, VISO, VEE and VGXX pins should be stabilized using ceramic capacitors $C_1$, $C_2$, $C_{S1}$, $C_{S2}$, and $C_{GXX}$ respectively as shown in Figure 5, 6, 7 and 8. After supply voltages reach their nominal values, the driver will begin to function after a time delay $t_{START}$.

**Short-Pulse Operation**
If command signals applied to IN are shorter than the minimum specified by $t_{GE(MIN)}$, then SIC1182K output signals at GH and GL will extend to a value of $t_{GE(MIN)}$. The duration of pulses longer than $t_{GE(MIN)}$ will not be changed.

**Short-Circuit Protection**
The SIC1182K uses the semiconductor device drain to source voltage to detect a short-circuit utilizing a sensing resistor network. With the help of a well stabilized $V_{VISO}$ and a Schottky diode connected between semiconductor device gate and VISO the VGE is clamped to the regulated VISO and the short-circuit current as well related SiC semiconductor energy will be limited.

During the off-state, SNS is internally connected to the COM pin. In case an optional filter-capacitor is applied between SNS pin and COM this capacitor is discharged.

When the driver is in turn-on transition or in on-state, the short-circuit detection algorithm through SNS is activated after an ASIC internally blanking time has elapsed. If now a voltage drop of about 0.4 V (typically) is detected at SNS referenced to VEE, this is interpreted as a detected short-circuit. The driver initiates a short-circuit turn-off without receiving a primary-side command. A fault command is sent to the primary side and SO is pulled to GND for typically 10 µs. During this time the driver ignores any command signal at the IN pin. In parallel to the short-circuit turn-off transition phase, the SCALE-iDriver's internal Advanced Active Clamping overvoltage limitation scheme is activated.

**$V_{DS}$ Overvoltage Limitation (Advanced Active Clamping)**
If the driver is in turn-off transition or in off-state the overvoltage limitation algorithm is activated at SNS and the internal reference is COM. In case a current of typically 440 µA (turn-off transition) to 520 µA (off-state) is feed to SNS, the driver will regulate the gate current to limit the turn-off di/dt and therefore the overvoltage at drain to source during turn-off.

**Over-Current Detection**
In case the semiconductor device offers a so called current-sense terminal, this signal can be fed into SNS with reference to VEE. As described in the short-circuit protection section, a voltage of about 0.4 V at SNS with reference to VEE will now be handled as an over-current. That leads to an over-current turn-off, following the same scheme as for a short-circuit condition.

## Application Example

This example describes how to set up the SIC1182K to use overvoltage limitation with a chain of TVS-diodes between the SiC MOSFET device Drain and SIC1182K SNS pin as well as a short-circuit detection via a resistive network also connected to the SNS pin.

### Primary-Side

For the input the circuitry of Figure 6 is recommended, when using 15 V input logic. $R_1$ and $R_2$ represent a voltage divider to get a 5 V signal at the IN pin. If additional filtering is required a capacitor $C_F$ can be placed in parallel to $R_2$ as depicted in Figure 7. The time constant $\tau$ can be calculated by Equation (1). In case direct 5 V logic is used at the IN pin, $R_2$ can be omitted and $R_1$ can be reduced to 100 Ω.

$$t = \frac{R_1 \times R_2}{R_1 + R_2} \times C_F \quad (1)$$

The pull up resistor $R_{SO}$ shall be connected to VCC and SO, with a value of 1 kΩ, to provide at least 5 mA to SO (open drain) in a fault condition. The primary-side power supply is connected to VCC and COM, where C1 is buffering $V_{VCC}$ and $C_2$ acts as high frequency filter.

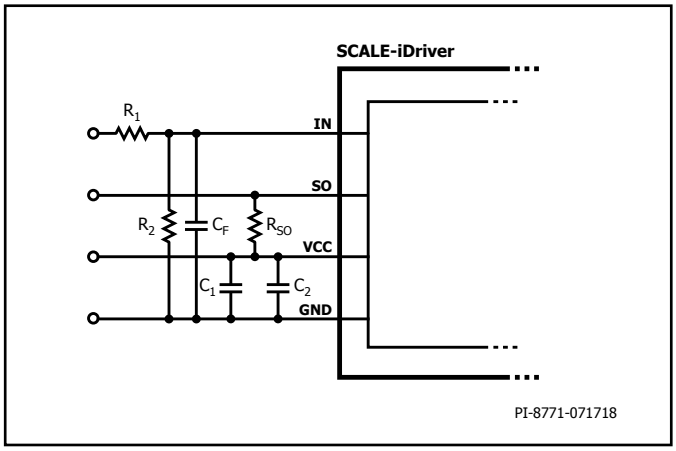



Figure 7. *Primary-Side of Example Circuitry.*

### Secondary-Side

The secondary-side power supply is connected to VISO and COM as shown in Figure 8. It is for instance recommended for SiC MOSFET to use $V_{TOT}$ = 20 V, to get $V_{GH}$ = 15 V for turn-on referenced to VEE and $V_{GL}$ = -5 V referenced to VEE for turn-off, to avoid additional components.

For each µC of semiconductor's gate charge a buffer capacitor of at least 3 µF shall be placed at VEE to COM ($C_{S1}$) as well as between VISO and VEE ($C_{S2}$). A 10 nF capacitor is connected between GH and VGXX.

To ensure gate voltage stabilization and drain current limitation during short-circuit the gate is connected to $V_{VISO}$ through Schottky diode $D_{STO}$.

To avoid parasitic turn-on during system power-on, the gate is connected to COM via a 22 kΩ resistor $R_{DIS}$.

The SNS pin has an alternating function that can be used for an overvoltage limitation, the so called Advanced Active Clamping, via a TVS-diodes chain during the turn-off transient as well as for a short-circuit detection via a resistive network during the turn-on transient.

The Advanced Active Clamping is triggered with the current $I_{SNS}$ flowing into the SNS pin of the SIC1182K which gradually reduces the GL-current down to typically 20 mA with increased $I_{SNS}$. This increases the effectiveness of the Basic Active Clamping function provided by the TVS-diodes drastically. The total voltage limit of the TVS chain is set to 900 V for a 1200 V-SiC MOSFET device.

During the turn-on transient the SNS pin serves the short-circuit detection and shut-down is triggered by a detection level referenced to VEE of $V_{SNS}$. The resistor chain to the Drain of the SiC MOSFET consisting of the resistors from $R_{CE2}$ to $R_{CE10}$ has a total resistance of 2.43 MΩ for a 1200 V-SiC MOSFET device.

If the SiC MOSFET has a sense terminal referenced to VEE which provide a fraction of the actual Source current this signal can also be fed back to the SNS pin via a shunt resistor. If here the SNS detection level of $V_{SNS}$ is reached the SIC1182K will turn-off the SiC MOSFET and thus provide an over-current detection.

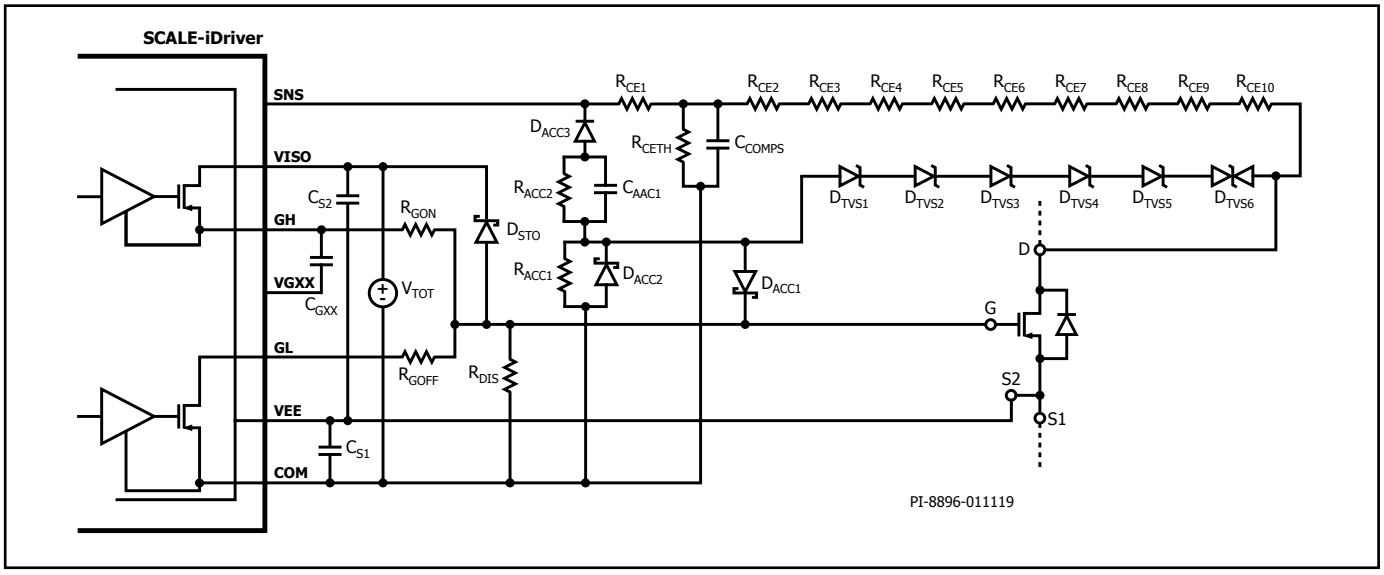



Figure 8. *Secondary-Side of Example Circuitry.*

## Power Dissipation and IC Junction Temperature Estimation

First calculation in designing the power semiconductor switch gate driver stage is to calculate the required gate power $P_{DRV}$. The power is calculated based on equation (2):

$$P_{DRV} = Q_{GATE} \times f_S \times V_{TOT} \quad (2)$$

where,

$Q_{GATE}$ – Controlled power semiconductor switch gate charge derived for the particular gate potential range defined by $V_{TOT}$.

$f_S$ – Switching frequency which is the same as applied to the IN pin of SCALE-iDriver.

$V_{TOT}$ – SCALE-iDriver secondary-side supply voltage.

In addition to $P_{DRV}$, the primary-side IC power dissipation $P_P$ and the secondary-side IC power dissipation without capacitive load $P_{SNL}$ must be considered according to Equation (3) and (4). Both are ambient temperature and switching frequency dependent (see Typical Performance Characteristics).

$$P_P = V_{VCC} \times I_{VCC} \quad (3)$$

$$P_{SNL} = V_{TOT} \times I_{VISO} \quad (4)$$

During IC operation, the $P_{DRV}$ is shared between the external turn-on gate resistor $R_{GH}$, turn-off gate resistor $R_{GL}$, the internal gate resistor $R_{GINT}$ of the power switch (if available) and internal driver resistances $R_{GHI}$ and $R_{GLI}$.

For junction temperature estimation purposes, the dissipated power under load $P_{OL}$ inside the IC can be calculated according to Equation (5).

$$P_{OL} = 0.5 \times Q_{GATE} \times f_S \times V_{TOT} \times \left( \frac{R_{GHI}}{R_{GHI} + R_{GX}} + \frac{R_{GLI}}{R_{GLI} + R_{GX}} \right) \quad (5)$$

$R_{GH}$ and $R_{GL}$ represent the sum of the external gate resistors ($R_{GON}$, $R_{GOFF}$) as well as the internal gate resistance of the SiC power semiconductor $R_{GINT}$ as shown in Equation (6) and (7).

$$R_{GH} = R_{GON} + R_{GINT} \quad (6)$$

$$R_{GL} = R_{GOFF} + R_{GINT} \quad (7)$$

Total IC power dissipation $P_{DIS}$ is estimated as per Equation (8) as sum of Equation (3), (4) and (5).

$$P_{DIS} = P_P + P_{SNL} + P_{OL} \quad (8)$$

The operating junction temperature $T_J$ for a given ambient temperature $T_A$ can be estimated with the thermal resistance from junction to ambient $\theta_{JA}$ according to Equation (9).

$$T_J = \theta_{JA} \times P_{DIS} + T_A \quad (9)$$

| Parameter | Symbol | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| **Absolute Maximum Ratings[1]** | | | | | |
| Primary-Side Supply Voltage[2] | $V_{VCC}$ | VCC to GND | -0.5 | 6.5 | V |
| Secondary-Side Total Supply Voltage | $V_{TOT}$ | VISO to COM | -0.5 | 30 | V |
| Secondary-Side Positive Supply Voltage | $V_{VISO}$ | VISO to VEE | -0.5 | 20 | V |
| Secondary-Side Negative Supply Voltage | $V_{VEE}$ | VEE to COM | -0.5 | 15 | V |
| Logic Input Voltage (command signal) | $V_{IN}$ | IN to GND | -0.5 | $V_{VCC}$ + 0.5 | V |
| Logic Output Voltage (fault signal) | $V_{SO}$ | SO to GND | -0.5 | $V_{VCC}$ + 0.5 | V |
| Logic Output Current (fault signal) | $I_{SO}$ | Positive Current Flowing into the Pin | | 10 | mA |
| Switching Frequency | $f_S$ | | | 150 | kHz |
| Storage Temperature | $T_S$ | | -65 | 150 | °C |
| Operating Junction Temperature | $T_J$ | | -40 | 150[3] | °C |
| Operating Ambient Temperature | $T_A$ | | -40 | 125 | °C |
| Operating Case Temperature | $T_C$ | | -40 | 125 | °C |
| Input Power Dissipation[4] | $P_P$ | $V_{VCC}$ = 5 V, $V_{TOT}$ = 28 V, $T_A$ = 25 °C $f_S$ = 150 kHz | | 188 | mW |
| Output Power Dissipation[4] | $P_S$ | | | 1602 | |
| Total IC Power Dissipation | $P_{DIS}$ | | | 1790 | mW |

NOTES:

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. Defined as peak voltage measured directly on VCC pin.
3. Transmission of command signals could be affected by PCB layout parasitic inductances at junction temperatures higher than recommended.
4. Input Power Dissipation refers to Equation (3). Output Power Dissipation is secondary-side IC power dissipation without capacitive load ($P_{SNL}$, Equation (4)) and dissipated power under load ($P_{OL}$, Equation (5)). Total IC power dissipation is sum of $P_P$ and $P_S$.

## Thermal Resistance

Thermal Resistance: eSOP-R16B Package:

($\theta_{JA}$) ..... 67 °C/W[1]

($\theta_{JC}$) ..... 34 °C/W[2]

Notes:

1. 2 oz. (610 g/m$^2$) copper clad.
2. The case temperature is measured at the plastic surface at the top of the package.

| Parameter | Symbol | Conditions<br>$T_J$ = -40 °C to +125 °C<br>See Note 1 (Unless Otherwise Specified) | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Recommended Operation Conditions** | | | | | | |
| **Primary-Side Supply Voltage** | $V_{VCC}$ | VCC – GND | 4.75 | | 5.25 | V |
| **Secondary-Side Total Supply Voltage** | $V_{TOT}$ | VISO – COM | 18 | | 28 | V |
| **Logic Low Input Voltage** | $V_{IL}$ | | | | 0.5 | V |
| **Logic High Input Voltage** | $V_{IH}$ | | 3.3 | | | V |
| **Switching Frequency** | $f_S$ | | 0 | | 150 | kHz |
| **Operating IC Junction Temperature** | $T_J$ | | -40 | | 125 | °C |
| **Electrical Characteristics** | | | | | | |
| **Logic Low Input Threshold Voltage** | $V_{IN+LT}$ | | 0.6 | 1.25 | 1.8 | V |
| **Logic High Input Threshold Voltage** | $V_{IN+HT}$ | | 1.7 | 2.2 | 3.05 | V |
| **Logic Input Voltage Hysteresis** | $V_{IN+HS}$ | See Note 8 | 0.1 | | | V |
| **Input Bias Current** | $I_{IN}$ | $V_{IN}$ = 4 V | 14 | 23 | 30 | µA |
| **Supply Current (Primary-Side)** | $I_{VCC}$ | $V_{IN}$ = 0 V | | 15 | 22 | mA |
| | | $V_{IN}$ = 5 V | | 25 | 35 | |
| | | $f_S$ = 20 kHz | | 22 | 30 | |
| | | $f_S$ = 75 kHz | | 25 | 35 | |
| **Supply Current (Secondary-Side)** | $I_{VISO}$ | $V_{IN}$ = 0 V | | 7 | 9 | mA |
| | | $V_{IN}$ = 5 V | | 7.5 | 9 | |
| | | $f_S$ = 20 kHz | | 8 | 10 | |
| | | $f_S$ = 75 kHz | | 11 | 14 | |
| **Power Supply Monitoring Threshold (Primary-Side)** | $UVLO_{VCC}$ | Resume Operation | | 4.3 | 4.65 | V |
| | | Suspend Operation | 3.85 | 4.15 | | |
| | | Hysteresis<br>See Note 8 | 0.02 | | | |
| **Power Supply Monitoring Threshold (Secondary-Side, Positive Rail $V_{VISO}$)** | $UVLO_{VISO}$ | Resume Operation | | 12.85 | 13.5 | V |
| | | Suspend Operation | 11.7 | 12.35 | | |
| | | Hysteresis<br>See Note 8 | 0.3 | | | |
| **Power Supply Monitoring Blanking Time (Secondary-Side, Positive Rail $V_{VISO}$)** | $UVLO_{VISO(BL)}$ | VISO Voltage Drop 13.5 V to 11.5 V<br>See Note 8 | 0.5 | | | µs |

| Parameter | Symbol | Conditions<br>$T_J$ = -40 °C to +125 °C<br>See Note 1 (Unless Otherwise Specified) | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Electrical Characteristics (cont.)** | | | | | | |
| **Secondary-Side Positive Supply Voltage Regulation** | $V_{VISO(HS)}$ | 21 V < $V_{TOT}$ ≤ 30 V: $\lvert I_{VEE}\rvert$ ≤ 1500 µA<br>$V_{TOT}$ = 19 V, $\lvert I_{VEE}\rvert$ ≤ 750 µA<br>$V_{TOT}$ = 18 V, $\lvert I_{VEE}\rvert$ ≤ 400 µA | 14.4 | | 15.75 | V |
| **VEE Source Capability** | $I_{VEE(SO)}$ | $V_{TOT}$ = 15 V, $V_{VEE}$ set to 0 V | 0.1 | | | mA |
| | | $V_{TOT}$ = 25 V, $V_{EE}$ set to 7.5 V, See Note 9 | 1.85 | 3.3 | 4.5 | |
| **VEE Sink Capability** | $I_{VEE(SI)}$ | $V_{TOT}$ = 25 V, $V_{EE}$ set to 12.5 V, See Note 9 | 1.74 | 3.1 | 4.5 | mA |
| **SNS Fault Monitoring Threshold** | $V_{SNS}$ | During turn-On transient,<br>Referenced to VEE, See Note 8 | | 400 | | mV |
| **SNS Fault Monitoring Blanking Time** | $t_{SNS(BL)}$ | Time between SNS rises at $V_{SNS}$ and GH falls at 16 V | 450 | 650 | 900 | ns |
| **SNS Current Required to Reduce GL-Current to 20 mA** | $I_{SNS}$ | During turn-On transient, $T_J$ = 25 °C | | 535 | | µA |
| **Turn-On Propagation Delay** | $t_{P(LH)}$ | $T_J$ = 25 °C<br>See Note 3 | 250 | 265 | 305 | ns |
| | | $T_J$ = 125 °C<br>See Note 3 | 255 | 282 | 300 | |
| **Turn-Off Propagation Delay** | $t_{P(HL)}$ | $T_J$ = 25 °C<br>See Note 4 | 240 | 270 | 325 | ns |
| | | $T_J$ = 125 °C<br>See Note 4 | 250 | 288 | 320 | |
| **Minimum Turn-On and Turn-Off Pulses** | $t_{GE(MIN)}$ | See Note 8 | | | 650 | ns |
| **Output Rise Time** | $t_R$ | No $C_G$,<br>See Note 5 | | 22 | 45 | ns |
| | | $C_G$ = 10 nF,<br>See Note 5 | 55 | 113 | 150 | |
| | | $C_G$ = 47 nF,<br>See Note 5 | 300 | 475 | 650 | |

| Parameter | Symbol | Conditions<br>$T_J$ = -40 °C to +125 °C<br>See Note 1 (Unless Otherwise Specified) | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Electrical Characteristics (cont.)** | | | | | | |
| **Output Fall Time** | $t_F$ | No $C_G$<br>See Note 6 | | 18 | 45 | ns |
| | | $C_G$ = 10 nF | 55 | 105 | 150 | |
| | | $C_G$ = 47 nF | 300 | 447 | 650 | |
| **Propagation Delay Jitter** | $\Delta_{TP}$ | See Note 8 | | ±5 | | ns |
| **Fault Signalization Delay Time** | $t_{FAULT}$ | See Note 13 | | 0.8 | 1.4 | µs |
| **SO Fault Signalization Time** | $t_{SO}$ | | 6.8 | 10 | 13.4 | µs |
| **Power-On Start-Up Time** | $t_{START}$ | See Note 7, 8 | | | 10 | ms |
| **Gate Sourcing Peak Current, GH Pin** | $I_{G(H)}$ | $V_{GH} \geq V_{TOT} - 11$ V<br>$C_G$ = 470 nF<br>See Note 9 | 3.6 | 4.35 | 5.5 | A |
| | | $R_G$ = 0 Ω<br>$T_A$ = 25 °C<br>$f_S$ = 1 kHz<br>See Notes 2, 8, 9 | | 7.8 | | |
| **Gate Sinking Peak Current, GL Pin** | $I_{G(L)}$ | $V_{GL} \leq 7.5$ V, $C_G$ = 470 nF<br>$V_{GL}$ referenced to COM | 3.6 | 4.55 | 5.5 | A |
| | | $R_G$ = 0 Ω,<br>$f_S$ = 1 kHz<br>See Notes 2, 8 | | 7.3 | | |
| **Internal Turn-On Gate Resistance** | $R_{GHI}$ | $I_G$ = 250 mA<br>$V_{IN}$= 5 V<br>See Note 9 | | 0.74 | 1.2 | Ω |
| **Turn-Off Internal Gate Resistance** | $R_{GLI}$ | $I_G$ = 250 mA<br>$V_{IN}$ = 0 V<br>See Note 9 | | 0.68 | 1.1 | Ω |
| **Turn-On Gate Output Voltage (Referred to COM Pin)** | $V_{GH(ON)}$ | $I_G$ = 20 mA<br>$V_{IN}$ = 5 V<br>See Note 9 | $V_{TOT}$ - 0.04 | | | V |
| **Turn-Off Gate Output Voltage (Referred to COM Pin)** | $V_{GL(OFF)}$ | $I_G$ = -20 mA<br>$V_{IN}$ = 5 V<br>See Note 9 | | | 0.04 | V |
| **SO Output Voltage** | $V_{SO(FAULT)}$ | Fault Condition,<br>$I_{SO}$ = 3.4 mA<br>$V_{VCC} \geq$ 3.9 V | | 210 | 450 | mV |

| Parameter | Symbol | Conditions<br>$T_J$ = -40 °C to +125 °C<br>See Note 1 (Unless Otherwise Specified) | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Package Characteristics (See Notes 8, 10)** | | | | | | |
| **Distance Through the Insulation** | DTI | Minimum Internal Gap (Internal Clearance) | 0.4 | | | mm |
| **Minimum Air Gap (Clearance)** | L1 (IO1) | Shortest Terminal-to-Terminal Distance Through Air | 9.5 | | | mm |
| **Minimum External Tracking (Creepage)** | L2 (IO2) | Shortest Terminal-to-Terminal Distance Across the Package Surface | 9.5 | | | mm |
| **Tracking Resistance (Comparative Tracking Index)** | CTI | DIN EN 60112 (VDE 0303-11): 2010-05 EN / IEC 60112:2003 + A1:2009 | 600 | | | |
| **Isolation Resistance, Input to Output** | $R_{IO}$ | $V_{IO}$ = 500 V, $T_J$ = 25 °C<br>See Note 12 | $10^{12}$ | | | Ω |
| | | $V_{IO}$ = 500 V, 100 °C ≤ $T_J$ ≤ $T_{C(MAX)}$<br>See Note 12 | $10^{11}$ | | | |
| **Isolation Capacitance, Input to Output** | $C_{IO}$ | See Note 12 | | 1 | | pF |
| **Package Insulation Characteristics** | | | | | | |
| **Maximum RMS Working Isolation Voltage** | $V_{IORM}$ | | | | 1000 | $V_{RMS}$ |
| **Maximum Repetitive Peak Isolation Voltage** | $V_{IORM}$ | | | | 1414 | $V_{PEAK}$ |
| **Input to Output Test Peak Voltage** | $V_{PD}$ | Method A, After Environmental Tests Sub-group 1, $V_{PR}$ = 1.6 × $V_{IORM}$, t = 10 s (qualification) Partial Discharge < 5 pC | | | 2263 | $V_{PEAK}$ |
| | | Method A, After Input/Output Safety Test Subgroup 2/3, $V_{PR}$ = 1.2 × $V_{IORM}$, t = 10 s, (qualification) Partial Discharge < 5 pC | | | 1697 | |
| | | Method B1, 100% Production Test, $V_{PR}$ = 1.875 × $V_{IORM}$, t = 1 s Partial Discharge < 5 pC | | | 2652 | |
| **Maximum Transient Peak Isolation Voltage** | $V_{IOTM}$ | $V_{TEST}$ = $V_{IOTM}$, t = 60 s (qualification), t = 1 s (100% production) | | | 8000 | $V_{PEAK}$ |
| **Insulation Resistance** | $R_S$ | $V_{IO}$ = 500 V at $T_S$ | | | >$10^9$ | Ω |
| **Maximum Case Temperature** | $T_S$ | | | | 150 | °C |
| **Safety Total Dissipated Power** | $P_S$ | $T_A$ = 25 °C<br>Derating See Figure 9 | | | 1.79 | W |
| **Pollution Degree** | | | | 2 | | |
| **Climatic Classification** | | | | 40/125/21 | | |
| **RMS Withstanding Isolation Voltage** | $V_{ISO}$ | $V_{TEST}$ = $V_{ISO}$, t = 60 s (qualification), $V_{TEST}$ = 1.2 × $V_{ISO}$ = 6000 $V_{RMS}$, t = 1 s (100% production) | | 5000 | | $V_{RMS}$ |

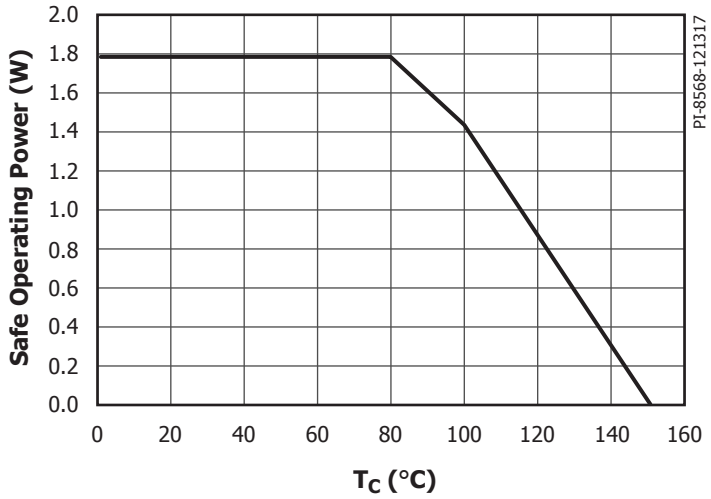


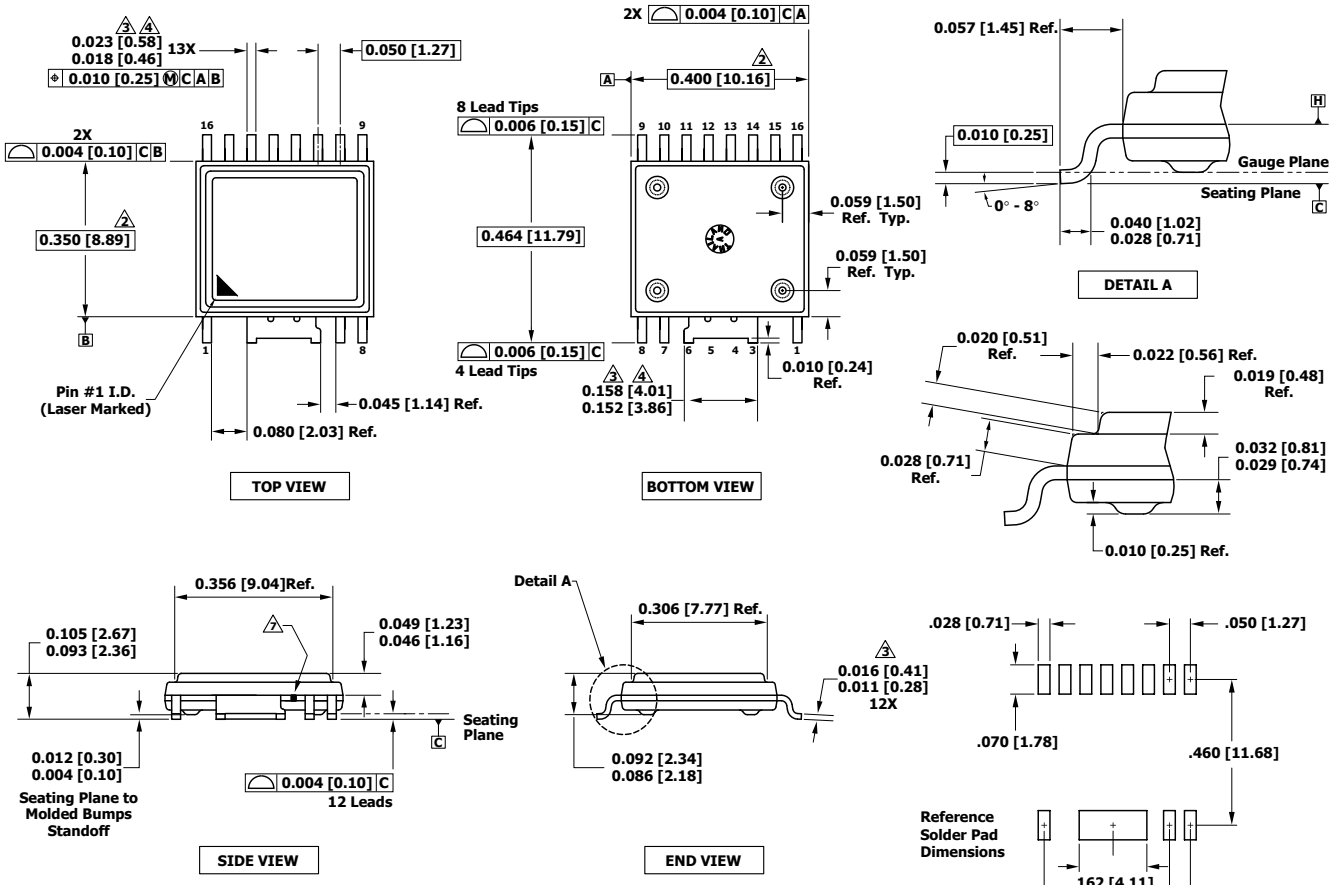

Figure 9. *Thermal Derating Curve Showing Dependence of Limited Dissipated Power $P_S$ on Case Temperature $T_C$ (DIN V VDE 0884-10).*

Operation is allowed until reaching $T_C$ and/or case temperature of 125 °C. Thermal stress beyond those values but below thermal derating curve may lead to permanent functional product damage. Operating beyond thermal SOP derating curve may affect product reliability.

NOTES:

1. $V_{VCC}$ = 5 V, $V_{TOT}$ = 25 V. $R_G$ = 5.6 Ω, no $C_G$. The VGXX pin is connected to the G pin through a 10 nF capacitor.
   Typical values are defined at $T_J$ = 25 °C, $f_S$ = 150 kHz, duty cycle = 50%. Positive currents are assumed to be flowing into pins.
2. Pulse width ≤ 10 µs, duty cycle ≤ 1%. The maximum value is controlled by the ASIC to a safe level. The internal peak power is safely controlled for $R_G$ ≥ 0 Ω and power semiconductor module input gate capacitance $C_{IES}$ ≤ 47 nF. The gate sourcing peak current was determined by the time required to charge a gate capacitance of 388 nF with $R_{GH}$ = 0 (and $R_{GL}$ = 4 Ω) from a voltage level of 2.5 V to a voltage level of 12.5 V. The gate sinking peak current was determined by the time required to discharge a gate capacitance of 388 nF with $R_{GL}$ = 0 (and $R_{GH}$ = 4 Ω) from a voltage level of 22.5 V to a voltage level of 12.5 V.
3. $V_{IN}$ potential changes from 0 V to 5 V within 10 ns. Delay is measured from 50% voltage increase on IN pin to 10% voltage increase on G pin.
4. $V_{IN}$ potential changes from 5 V to 0 V within 10 ns. Delay is measured from 50% voltage decrease on IN pin to 10% voltage decrease on G pin.
5. Measured from 10% to 90% of $V_{GE}$ ($C_G$ simulates semiconductor gate capacitance). The $V_{GE}$ is measured across $C_G$.
6. Measured from 90% to 10% of $V_{GE}$ ($C_G$ simulates semiconductor gate capacitance). The $V_{GE}$ is measured across $C_G$.
7. The amount of time after primary and secondary-side supply voltages ($V_{VCC}$ and $V_{TOT}$) reach minimal required level for driver proper operation. No signal is transferred from primary to secondary-side during that time.
8. Guaranteed by design.
9. Positive current is flowing out of the pin.
10. Safety distances are application dependent and the creepage and clearance requirements should follow specific equipment isolation standards of an application. Board design should ensure that the soldering pads of an IC maintain required safety relevant distances.
11. Measured accordingly to IEC 61000-4-8 ($f_S$ = 50 Hz, and 60 Hz) and IEC 61000-4-9.
12. All pins on each side of the barrier tied together creating a two-terminal device.
13. The amount of time needed to transfer fault event (UVLO or SNS fault) from secondary-side to SO pin.

## eSOP-R16B




**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches [mm].
6. Datums A and B to be determined in Datum H.
7. Exposed metal at the plastic package body outline/surface between leads 6 and 7, connected internally to wide lead 3/4/5/6.

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## MSL Table

| Part Number | MSL Rating |
|---|---|
| SIC1182K | 3 |

## ESD and Latch-Up Table

| Test | Conditions | Results |
|---|---|---|
| Latch-up at 125 °C | JESD78D | > ±100 mA or > 1.5 × $V_{MAX}$ on all pins |
| Human Body Model ESD | JESD22-A114F | > ±2000 V on all pins |
| Charged Device Model ESD | JESD22-C101 | > ±500 V on all pins |

## IEC 60664-1 Rating Table

| Parameter | Conditions | Specifications |
|---|---|---|
| Basic Isolation Group | Material Group | I |
| Installation Classification | Rated mains RMS voltage ≤ 150 V | I - IV |
| | Rated mains RMS voltage ≤ 300 V | I - IV |
| | Rated mains RMS voltage ≤ 600 V | I - IV |
| | Rated mains RMS voltage ≤ 1000 V | I - III |

## Electrical Characteristics (EMI) Table

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Common-Mode Transient Immunity, Logic High** | $CM_H$ | Typical values measured according to Figure 10 and Figure 11. Maximum values are design values assuming trapezoid waveforms. | | -35 / 50 | -100 / 100 | kV/µs |
| **Common-Mode Transient Immunity, Logic Low** | $CM_L$ | | | | | |
| **Variable Magnetic Field Immunity** | $H_{HPEAK}$ | See Note 11 | | 1000 | | A/m |
| | $H_{LPEAK}$ | | | | | |

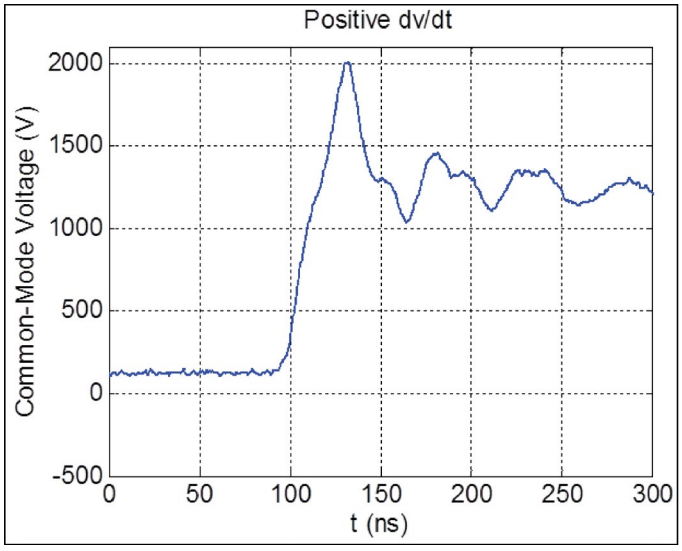



Figure 10. *Applied Common Mode Pulses for Generating Positive dv/dt.*

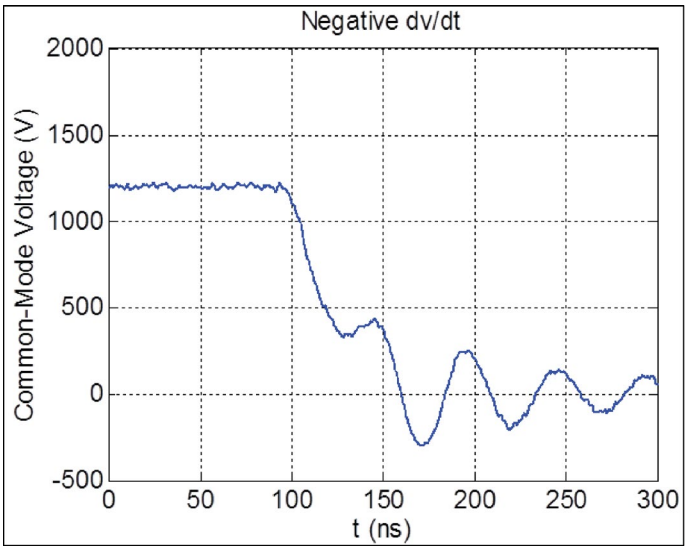
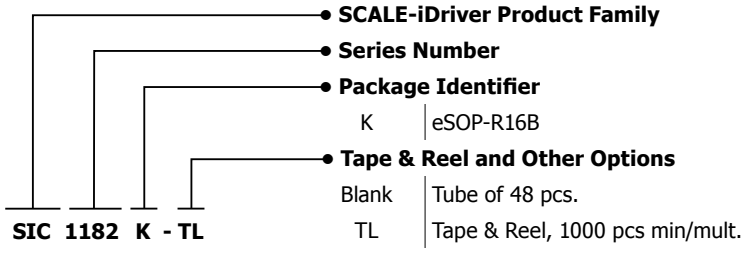



Figure 11. *Applied Common Mode Pulses for Generating Negative dv/dt.*

## Regulatory Information Table

| VDE | UL | CSA |
|---|---|---|
| Pending certification to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 | Pending UR recognition under UL1577 Component Recognition Program | Pending UR recognition under UL1577 Component Recognition Program |
| Reinforced insulation for Max. Transient Isolation voltage 8 kV,<br>Max. Surge Isolation voltage 8 kV,<br>Max. Repetitive Peak Isolation voltage 1414 V | Single protection,<br>5000 $V_{RMS}$ dielectric voltage withstand | Single protection,<br>5000 $V_{RMS}$ dielectric voltage withstand |

## Part Ordering Information



| Revision | Notes | Date |
|---|---|---|
| A | Code A release. | 12/18 |
| B | Various typos corrected throughout document. Updated $t_{P(LH)}$, $t_{P(HL)}$, $I_{IN}$, $I_{VCC}$, $I_{VISO}$, $UVLO_{VISO(BL)}$ and $t_{START}$ parameter conditions, Figures 1 and 8 per PCN-19031. | 01/19 |
| C | Reinforced insulation VDE V 0884-10 certified. | 09/19 |
| D | Added Notes under Conditions column for $V_{IN+HS}$, $UVLO_{VCC}$ and $UVLO_{VISO}$ parameters. | 09/24/19 |

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