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Paper Code : PC-ECS302/PCC- CS302/PCC-CS302/PCCCS302 Computer Organisation

UPID : 003444

Time Allotted : 3 Hours *Full Marks :70*

The Figures in the margin indicate full marks.
Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer *any ten* of the following : [1 x 10 = 10]

(I) In a microprocessor the address of the next instruction to be executed is stored in _____.

(II) In Booth's multiplication algorithm which type of sign number representation is used?

(III) Principle of locality justifies the use of _____ memory.

(IV) Specify the statement is true or False. When DMA operation takes place then always CPU seats idle.

(V) Operating System is categorised under which type of software?

(VI) Maximum n bit 2's complement number is _____.

(VII) How many locations are present in 2K RAM chip?

(VIII) In case of polling using 8 lines how many different bus grant response can generate?

(IX) During the transfer of data between the processor and memory we use _____.

(X) When we perform subtraction on -7 and 1 the answer in 2's complement form is _____.

(XI) To construct a 32K x 16 RAM chip by using 8KB RAM chips decoder is required. What is the specification of this decoder?

(XII) In DMA operation
i) Data is transferred between main memory and I/O device
ii) Data is transferred between main memory and secondary memory
iii) Data is transferred between main memory and CPU
a) i) and ii)
b) i) only
c) i), ii) and iii)
d) ii) Only

Group-B (Short Answer Type Question)

Answer *any three* of the following : [5 x 3 = 15]

2. Difference between hardwired and microprogrammed control [5]
3. Define Instruction Cycle, Machine Cycle and T-state. [5]
4. Design a 4-bit adder-subtractor composite unit. [5]
5. A three level memory system having cache access time of 15 ns, main memory access time of 25 ns and disk access time of 40 ns has a cache hit ratio of 0.96 and main memory hit ratio of 0.9. What should be the Average Memory Access Time? [5]
6. Draw a flowchart of Restoring division algorithm. [5]

Group-C (Long Answer Type Question)

Answer *any three* of the following : [15 x 3 = 45]

7. (a) What is bus arbitration? [2]
   (b) Explain with a suitable diagram the daisy chaining priority interrupts technique. [5]
   (c) What are the disadvantages of daisy chaining technique? [2]
   (d) Explain the working principle of polling method and How the limitations of daisy chaining method are reduced by using polling? [6]
8. (a) Draw the functional diagram of a computer and explain each block. [6]
   (b) What is signed number and unsigned number? [1]
   (c) Explain zero address, one address, two address and three address instruction with suitable example. [6]
   (d) Convert the binary number $(1101101110)_2$ into its equivalent Hexadecimal number. [1]

(e) What is the 16 bit representation of -6 ? [1]

9. (a) Draw the flowchart of Booth's Multiplication algorithm. [5]

(b) Multiply – 9 by +6 using Booth's algorithm. Assume the multiplicand and multiplier to be 5 bits each. [6]

(c) Explain the operation of 4 bit carry look ahead adder with suitable diagram. [4]

10. (a) Explain the associative and direct mapped cache mapping approaches. [4]

(b) Identify size of the sub-fields (in bits) in the address for direct mapping, associative and set associative mapping cache schemes where processor address is 32 bit. We have 2MB cache memory.
The block size is 64 bytes.
There are 4 blocks in cache set. [6]

(c) Explain the working principle of CMOS Static RAM Cell. [5]

11. (a) Draw the block diagram of a basic hardwired control unit. [5]

(b) Design Booth's Multiplier control logic using Microprogrammed Control unit approach. [7]

(c) What is programmed I/O technique? Why it is not very useful? [3]

*** END OF PAPER ***