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Paper Code : ESC301/PC-ROB301 Analog and Digital Electronics

UPID : 003442

Time Allotted : 3 Hours *Full Marks :70*

The Figures in the margin indicate full marks.
Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer any ten of the following : [1 x 10 = 10]

(I) In the astable amplifier, up to what voltage the capacitor charges ?

(II) The state 1110 is a valid state in 8-4-2-1 Binary Coded Decimal counter . State True / False.

(III) A 4 bit mod 16 ripple counter uses JK flip-flop. If the propagation delay of each flip flop is 100 ns, what will be the maximum clock frequency (in MHz) that can be used in the counter ?

(IV) In Asynchronous circuit Race condition always arises. State True / False.

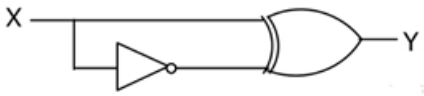
(V) What is the mininmum number of NAND gates required to design a Full adder circuit ?

(VI) Which type of ADC (analog-to-digital converter) is slowest of all ?

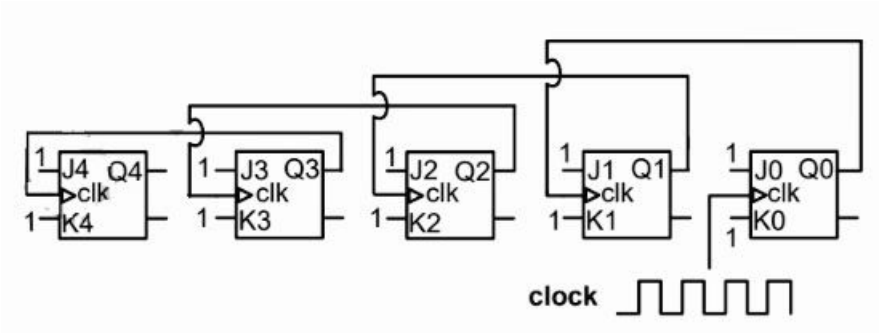
(VII) Which A/D converters are used for High speed operation ?

(VIII) The input of a Schmitt Trigger is sawtooth wave , what will be shape of the output?

(IX) The output Y of the logic circuit given below is _____

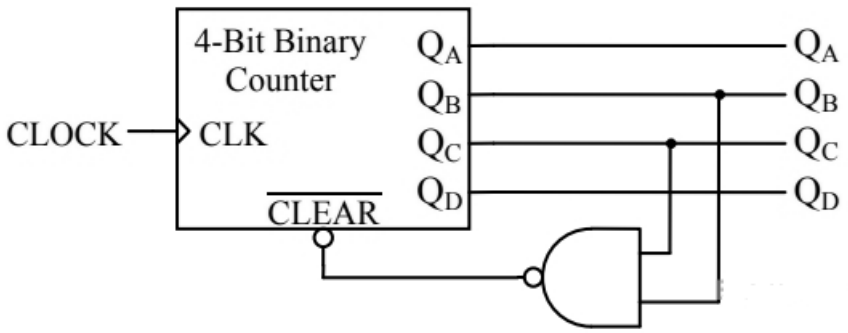


(X) Five JK flip - flops are cascaded to form circuit shown in figure. Clock pulses at a frequency of 1 MHz are applied as shown. What will be the frequency (in kHz) of the waveform at Q_3 ?



(XI) If $(212)_X - (23)_{10}$, where X is the base of the number system , find X

(XII) A mod-n counter using a synchronous binary up-counter with synchronous clear input is shown in the figure. What will be the value of n ?



Group-B (Short Answer Type Question)

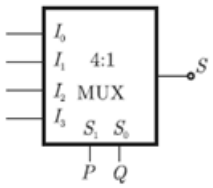
Answer any three of the following [5 x 3 = 15]

2. Perform Conversion of D flip Flop to J-K Flip Flop [5]

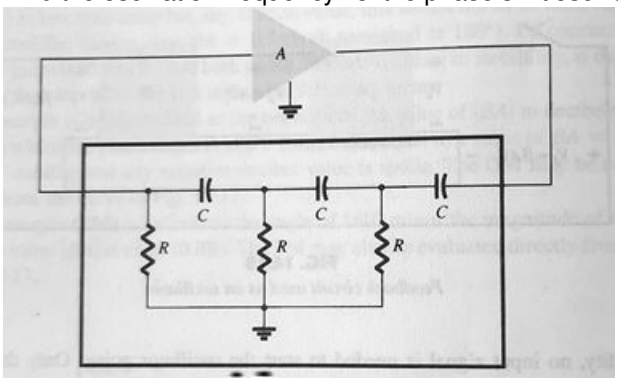
3. Perform conversion of S-R Flip flop to J-K Flip Flop [5]

4. Design a 5 to 32 decoder using 3 to 8 decoder and 2 to 4 decoder. [5]

5. Figure shows a 4 to 1 MUX to be used to implement the sum S of a 1-bit full adder with input bits P and Q and the carry input Cin. Find the combinations of inputs to I_0, I_1, I_2 and I_3 of the MUX which will realize the sum S [5]



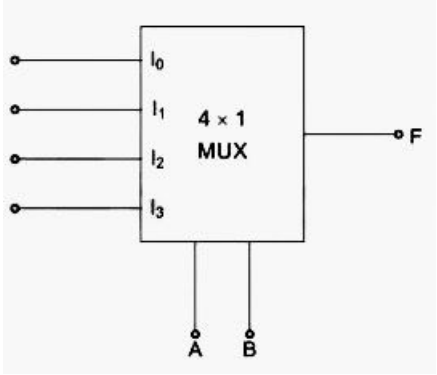
6. Find the oscillation frequency *f* of the phase shift oscillator when R = 10KΩ and C= 6.5nf [5]



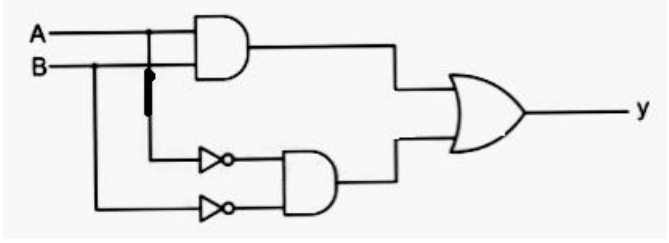
Group-C (Long Answer Type Question)

Answer any three of the following [15 x 3 = 45]

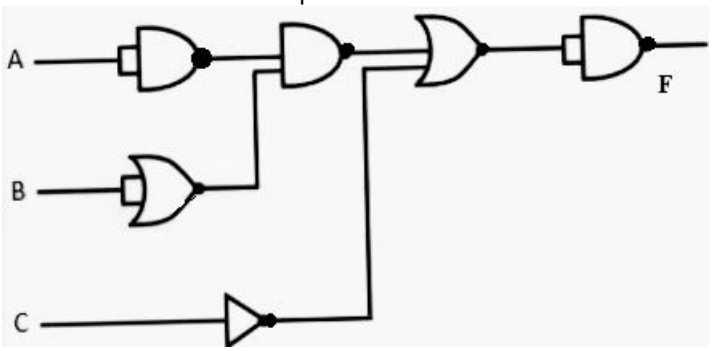
7. (a) In the given MUX the output is F = A XOR B . What will be the inputs I_0, I_1, I_2, I_3 ? [5]



(b) Check the following digital circuit. What will be the equivalent logic gate of the whole circuit ? [5]



(c) What wil be minimised output F of the circuit [5]



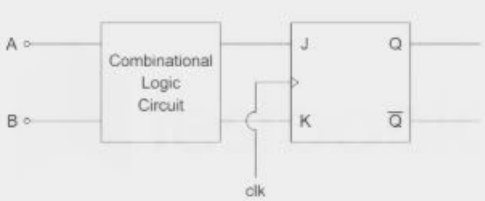
8. (a) Define Voltage , Current and Power amplifier [3]

(b) Write the different classes of Power amplifier [3]

(c) Draw the circuit diagram of a class B push pull transistor amplifier Explain the operation [5]

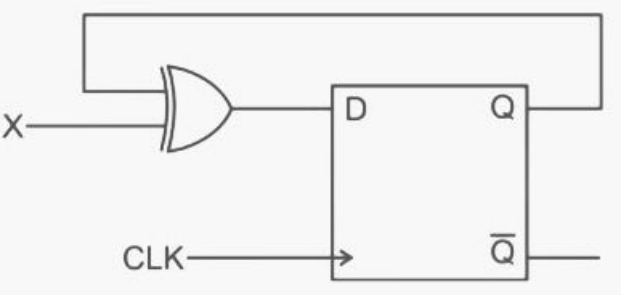
(d) Derive the maximum efficiency of a class B amplifier [4]

9. (a) To realize the given truth table from the circuit shown in the figure, find the input to J in terms of A and B. [7]

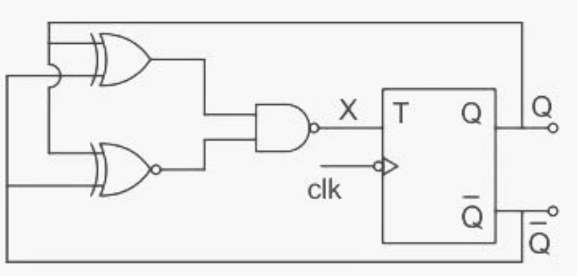


A	B	Q_{n+1}
0	0	$\overline{Q_n}$
0	1	1
1	0	Q_n
1	1	0

(b) What is the equivalent flip-flop of the digital circuit given below ; explain with reason. [4]



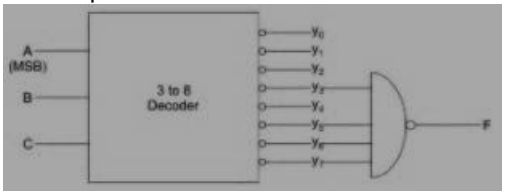
(c) The clock frequency applied to the digital circuit shown in the figure below is 1KHz. If the initial state of the output of the flip-flop is 0, what will be the frequency of the output waveform Q in KHz ? [4]



10. (a) Find the simplified form of the Boolean expression Y , where [8]

Y=(A'.BC+D)(A'.D+B'.C')

(b) The output F of decoder can be realised with best logic gates. Find out the Boolean expression. [7]



11. (a) Draw the circuit diagram of a Astable Multivibrator using IC 555 timer [6]

(b) Derive the expression duty cycle and frequency of oscillation [6]

(c) Explain why this is called Free running oscillator. [3]