

REVIEW OF BASIC COMPUTER ARCHITECTURE

Computer Architecture -

It refers to those attributes of a system visible to a programmer that have direct impact on the logical execution of a program.

Examples of those attributes that are known as architectural attributes are, instruction set, addressing modes, IO mechanism, techniques of addressing memory, no. of bits required to represent data type.

Computer Organization -

It refers to the operational or functional units of computer & their interconnection to realize the architectural specification.

Examples of organizational attributes are, hardware details that are transparent to the programmer, interface between computer system and Peripheral devices.

Structural & Functional View of Computer System -

Functional view -

Functional view describes the basic functions that a computer can perform. S.a -

1. Data processing - A wide variety of fundamental methods that performs several task.
2. Data storage - Supports temporary storage for short term or long term.
3. Input / output - When data are received from or delivered to a peripheral device through IO interface or IO Module.
4. Data communication - When data is moved over long distances, to or from a remote device.

Structural view -

It describes internal structure of computer & internal structure of CPU or processor.

Internal structure of Computer -

1. CPU (Central processing unit) - It controls operations of computer & performs data processing functions. It is also known as processor.
2. Main Memory - It is the storage unit of computer. It is a storage media that stores both instructions & data in binary form on machine readable form. Main memory consists of several register known as memory registers & each register of memory identified by an address or memory address. So, a memory address is used to identify memory location.

A memory can be byte addressable or word addressable.

3. I/O (Peripheral device) device - These devices are external to the processor or peripheral to the processor. An input device send data to the processor or the processor takes input from input device. e.g - Keyboard, sensor

Similarly an output device is used to display the result ~~or~~ to the outside world.

Therefore, I/O devices moves data between the computer & external environment.

e.g of I/O devices - Monitor, printer, scanner

4. System interconnection - It is the Bus System that provides communication among CPU, main memory, peripheral devices.

Internal structure of CPU or processor -

1. Arithmetic and Logical Unit (ALU) - It is the execution unit of computer that perform the computation on any kind of arithmetic or logical operation or any kind of data processing function.

2. Control Unit - It generate timing & control signals to control the operation of CPU & hence the Computer. The timing signals are used to provide synchronization among different components of computer. The control signals are used to specify the type of operation the processor going to perform.

3. Registers - It is also known as processor register because these are internal to the processor. These processor register provides storage internal to the CPU.

4. CPU Interconnection - It is also known as internal Bus because it is internal to the processor. Hence internal bus provides communication among the control unit, ALU & Registers.

VON Neumann Concept -

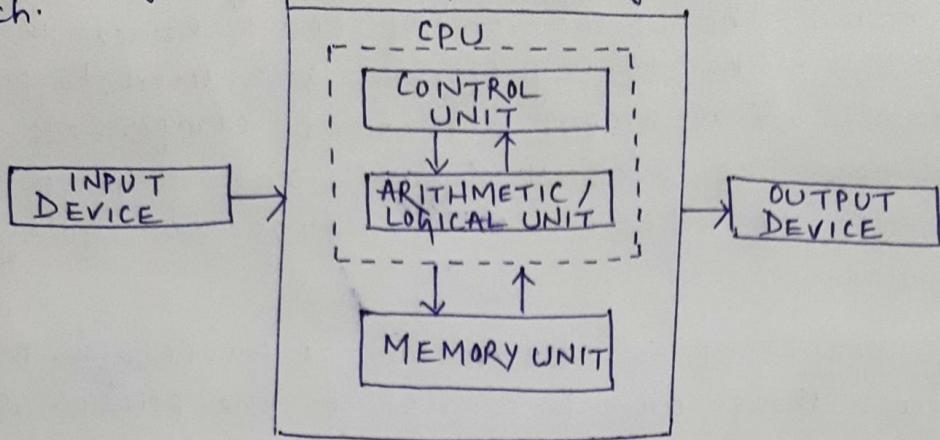
Von Neumann is a scientist who is known as father of modern computer because of his developed idea or concept known as Von Neumann Concept or stored-program concept.

Stored-Program Concept says that programming process can be advantageous if the program could be represented in a form of suitable for storing in memory alongside data. Then a computer could get its instruction by reading them from memory and a program could be altered or modified by changing the values of a portion of memory.

According to stored-Program Concept -

1. Data & instruction can be stored in a single Read-Write memory (R/W Memory) or RAM or Main memory of computer.
2. The contents of memory are addressable by location without regard to the type of data contained there.
3. Executions occur in a sequential manner from one instruction to the next unless there is an exception or interrupt or there are some branch control.

Block Diagram of a computer system based on Von Neumann arch.



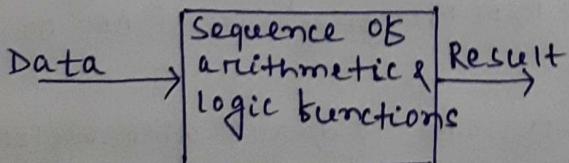
Designing of Computer ALU -

Based on the design of ALU, it can be said that the design of computer system is of which type. i.e.: the design of a system can be -

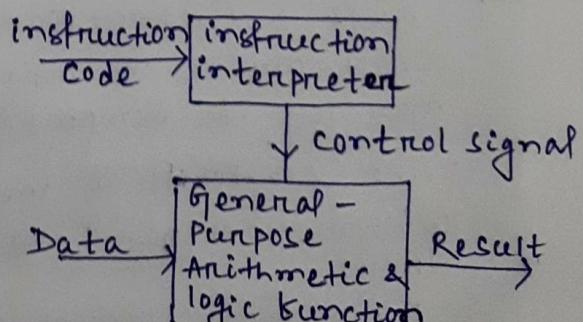
- (a) Hardwired programmed.
- (b) Software programmed.

(a) Hardwired programmed - If there is a particular computation to be performed then the configuration of logic components in ALU designed specifically for that computation could be constructed. So this is just connecting various components in desired configuration known as hardwired programmed.

(b) Software programmed - On this use a sequence of codes known as instructions and these instructions get interpreted by some specific hardware & general control signals for execution of instruction. Collection of instructions in a sequential manner is called software, hence it is known as software programming.

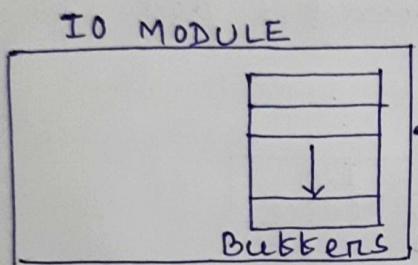
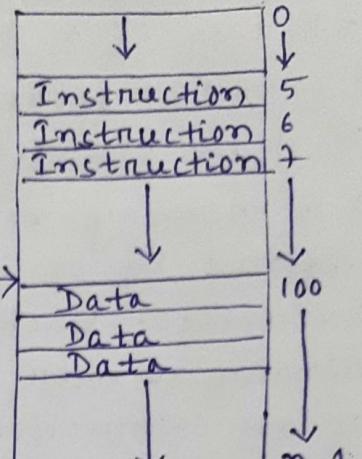
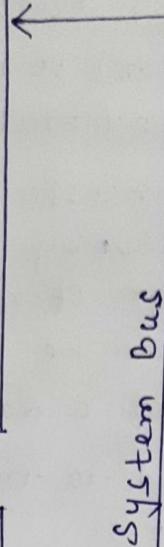
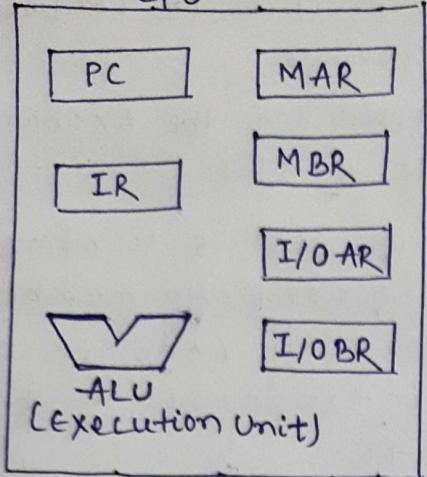


(Programming in hardware)



(Programming in software)

Block Diagram of Computer Components → Top-Level View.



Each location of memory is addressed by using 'n' bits.

$$\Rightarrow \text{No. of memory location} = 2^n.$$

- PC = Program Counter
- IR = Instruction Register
- MAR = Memory Address Register
- MBR = Memory Buffer Register
- I/O AR = I/O Address Register
- I/O BR = I/O Buffer Register

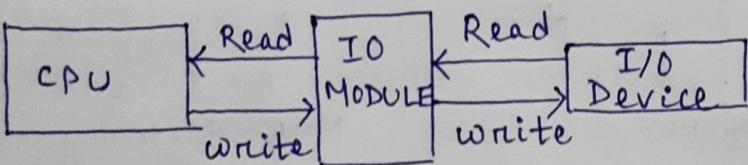
Description—

The above figure describes the top-level view of computer system.

- The CPU exchanges data with memory. So for this CPU uses two different processor register that is internal to the CPU. These are - MAR & MBR.
- MAR (Memory address register) contains or holds the address of memory location from where data is to be read or written currently.
- MBR (Memory Buffer Register) contains or holds the data that is read from memory or & holds the data that is to be written onto memory.
- When CPU exchanges data with peripheral devices or IO devices, CPU uses 2 different registers. These

Registers are - IOAR, IOBR.

- IOAR (I/O Address Register) specifies or contain address of a particular I/O devices.
- IOBR (I/O Buffer Register) is used for the exchange of data between an I/O Module & CPU.
- A memory module consists of set of locations, defined by or identified by sequentially numbered addresses. Each location of memory contain a binary number that can be interpreted either as an instruction or as a data.
- The I/O Module is used to transfer data to or from I/O device & CPU.

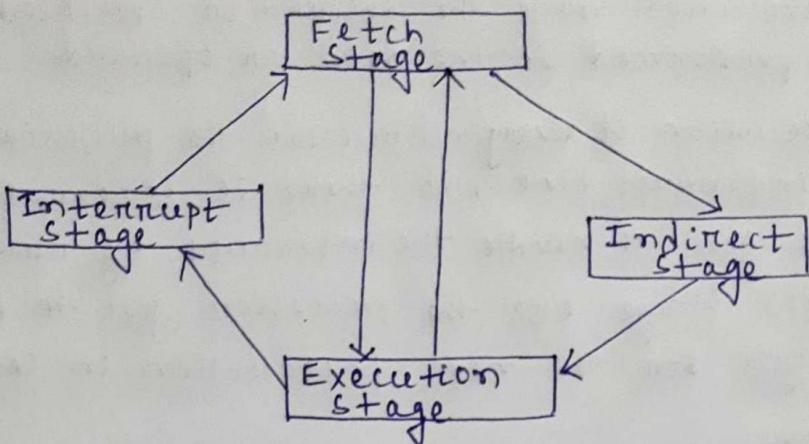


Instruction cycle -

The task of computer is to execute a program. And a program consist of no. of instructions written in a systematical manner. The processor execute the instructions of a program stored in memory in a sequential manner unless there is an exception or control shift instruction.

Each instruction of the program go through a cycle for their execution, Known as instruction cycle. An instruction cycle consist of 4 different phases. They are -

1. Fetch stage
2. Indirect stage
3. Execution stage
4. Interrupt stage.



(BLOCK Diagram of instruction cycle)

→ During Fetch stage, an instruction is fetched or read from memory whose address is specified in MAR. After fetching instruction, that instruction get decoded to specify the type of operation & specify the data.

The decode operation require less time for its completion. Hence decode phase is combined with fetch stage.

An instruction is a binary pattern or code that instruct the processor to perform a specified operation. An instruction has two different part, they are - opcode, operand.

opcode — operation to be performed by CPU.

operand — Data on which the operation is to be performed.

opcode	operand
← instruction →	

→ During indirect stage, the data or operand is retrieved from the memory by using 2 (two) memory references. Therefore during execution of indirect addressing memory instruction there are two MEMR (Memory read operation) to retrieve the data on operand.

→ During execution stage the desired or specified operation is to be performed on the data or operand.

→ After execution of every instruction the processor goes to check the interrupt line, if there is interrupt then the processor goes to handle the interrupt by running the interrupt stage else the processor goes to execute the fetch cycle for the next instruction in sequence.

Addressing Mode

Addressing Mode specifies where the operand is present. There are some bits present in instruction that specify the type of addressing mode.

→ If the operand or data is present in processor register then it requires very less time for its retrieval. Because processor registers internal to CPU.

→ If the operand or data is present in memory then it requires more time for its retrieval. Because to access memory location the system bus is required.

→ Data can be present in any one of the following -

- (a) Register
- (b) Memory
- (c) Instruction.

→ Types of addressing mode

(a) Register addressing mode - In this data is present in any one of the processor register.

e.g. ADD R₁, R₂ ; R₁ ← R₁ + R₂

↓
opcode ↗ operand

(b) Direct addressing mode - Here the data is present in the memory & the address of that memory location is given in the instruction.

e.g. LDA 4000 ; AC ← [4000]

Load ↗ to AC
Register ↗ Memory location.

(C) Indirect Addressing Mode - Here the data is present in memory & the address of that memory location where the data is present is also present in memory. To retrieve the address of data, the address given in the instruction is used.

→ The address given in instruction gives 1st reference to the memory from where the address of data is retrieved.

→ Now after retrieval of address, 2nd reference is given to memory by using the previous ~~retrieved~~ retrieved address. This 2nd reference is used to retrieve the data.

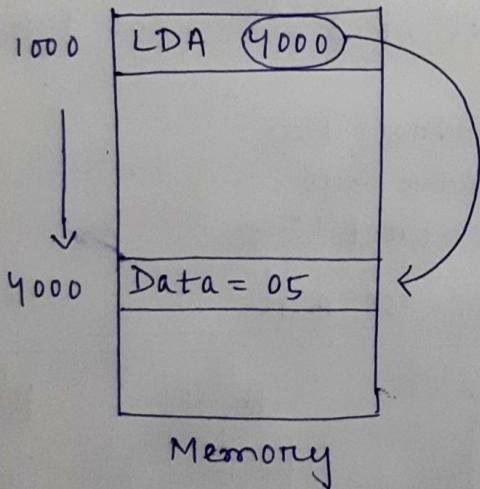
→ e.g - LXI H, 4000 ; HL \leftarrow 4000

Indirect addressing instruction → MOV A, M ; A \leftarrow (M)

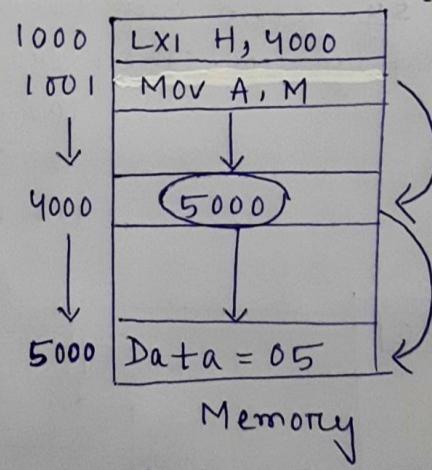
Memory location

$$M = HL \therefore A = [HL]$$

$$A = [4000]$$



(Direct addressing)



(Indirect Addressing)

(d) Immediate Addressing
by the instruction itself or the data is present in the instruction itself.

— Here the data is given

e.g - ADI B, 05 ; A \leftarrow B + 05

Operation

→ Data given in instruction

(e) Implicit Addressing Mode - Here the data is given in the implicit register of the processor and there is only one operand or data in instruction
[AC or Accumulator is the implicit register because it is internal to the ALU circuit]

e.g. CMA ; AC $\leftarrow \overline{AC}$

↳ complement Accumulator content.

CLA ; AC $\leftarrow 0$

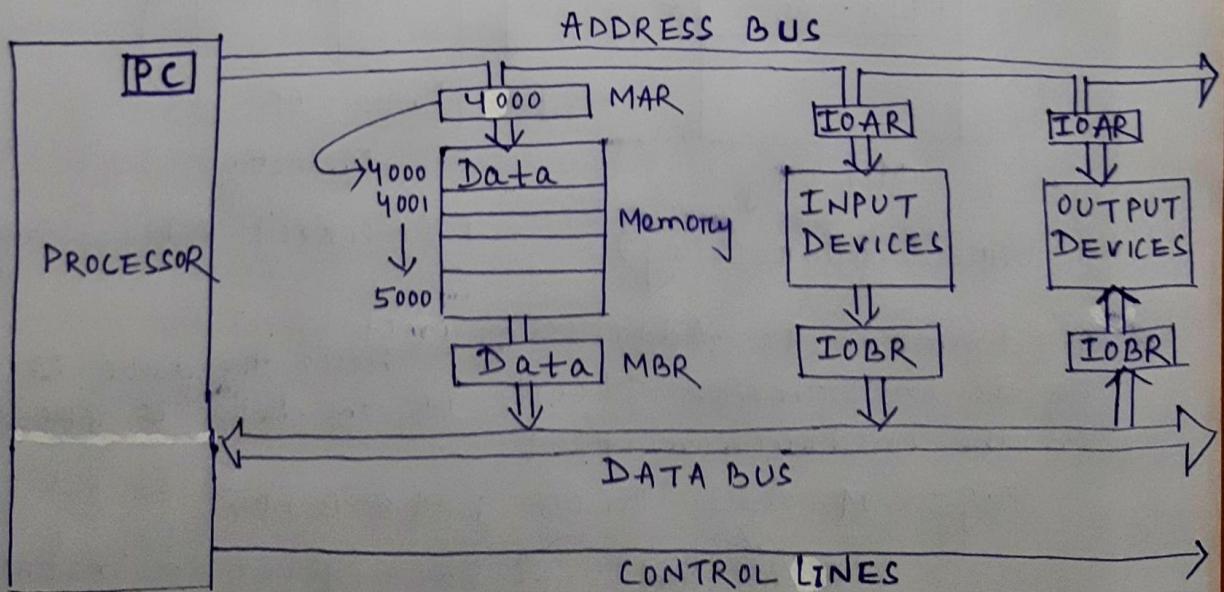
↳ clear Accumulator.

BUS Structure -

It is also known as system bus structure. A System Bus is a group of wire used to interconnect processor, Memory & IO devices. It is a communication path that carry signal or transmit signal or transmit binary digits in between Processor & Memory or in between Processor & IO Devices.

The System Bus consist of 3 different types of functional groups. They are -

- (a) Address Bus
- (b) Data Bus
- (c) Control lines

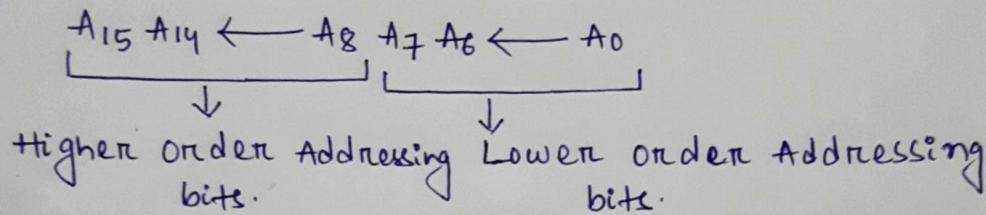


(a) Address Bus - Address bus is a group of wire that carry the address of memory or IO device from where data is to be read or onto which data is to be written.

Total Addressing bits is divided into Lower order addressing bits & higher order addressing bits.

- To address memory total no.of addressing bits are used.
- To address IO devices only lower order addressing bits are used.
- The addressing bits are used to kind out the capacity of memory of the computer system.

e.g -



∴ no.of addressing bits = 12.

$$\Rightarrow \text{Capacity of memory} = 2^{12} = 2^2 \times 2^{10} = 4 \text{ KB}$$

$\hookrightarrow 1 \text{ KB} = 2^{10}$
 $\hookrightarrow 2^2 = 4 \text{ Byte}$

(b) Data Bus - It is also a group of wire that carry data read from memory or input device or the data bus carry data to be written onto the memory or output device.

→ Data bus represent word length of computer system or processor. Word length specify how many bits can be read or write into by the processor at a time.

(c) Control lines - It is not group of wires rather these are single lines that are used to providing timing & control signals to the memory & IO devices.

e.g. of control signals - MEMRD, MEMWR, IOR, IOW

e.g. of timing signals - t₁, t₂, t₃, t₄ etc