CE220924 - PSoC 6 MCU VDAC Sine Wave Generator Using DMA

Objective

This example demonstrates how to use the Voltage DAC (12-bit) Component and CTDAC Peripheral Driver Library (PDL) as a sine-wave generator using high-speed DMA transfers from a lookup table in a PSoC® 6 MCU device.

Overview

This example generates a sine wave using the Voltage DAC (12-bit) and DMA Components. The DMA Component transfers data from a lookup table to the DAC value register without any CPU intervention. Other than function calls to initialize and enable the hardware, there are no other software operations. Both the PSoC Creator™ Voltage DAC (12-bit) Component and underlying low-level Continuous Time DAC (CTDAC) PDL function calls are shown.

Requirements

Tool: PSoC Creator™ 4.2 with PDL 3.0.1

Programming Language: C (Arm® GCC 5.4-2016-q2-update)

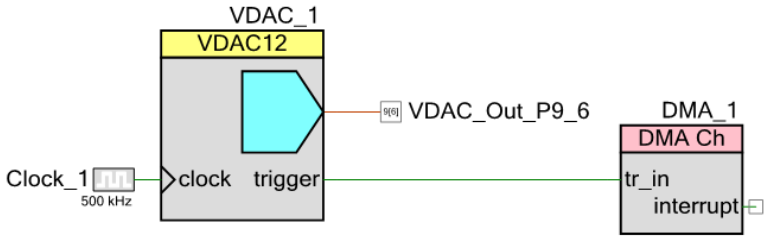
Associated Parts: PSoC 6 MCU family of devices

Related Hardware: CY8CKIT-062-BLE PSoC 6 MCU BLE Pioneer Kit and CY8CKIT-062-WiFi-BT PSoC 6 MCU Pioneer Kit

Design

The design shown in Figure 1 implements continuous updating of the VDAC Component's output voltage using DMA. The DMA transfers are initiated by a trigger signal generated by the previous update's completion. The VDAC Component is placed into an available CTDAC hardware block and the output voltage waveform is routed to pin P9[6]. An oscilloscope connected to pin P9[6] can display the waveform.

Figure 1. PSoC Creator Component Schematic



The VDAC trigger output tells the DMA Component when the VDAC is ready to accept a new value. The DMA updates the VDAC values from a 100-entry lookup table. With the 500-kHz VDAC input clock, the sine-wave frequency is 5 kHz.

Design Considerations

This code example is designed to run on the CY8CKIT-062-BLE Pioneer Kit with the CY8C6347BZI-BLD53 device. To port the design to a different PSoC 6 MCU device and/or kit, change the target device using **Device Selector** and update the pin assignments in the **Design Wide Resources Pins** settings as needed. For single-core PSoC 6 MCUs, port the code from *main_cm4.c* to *main.c*.

Hardware Setup

This example uses the kit's default configuration. Refer to the kit guide to ensure that the kit is configured correctly.

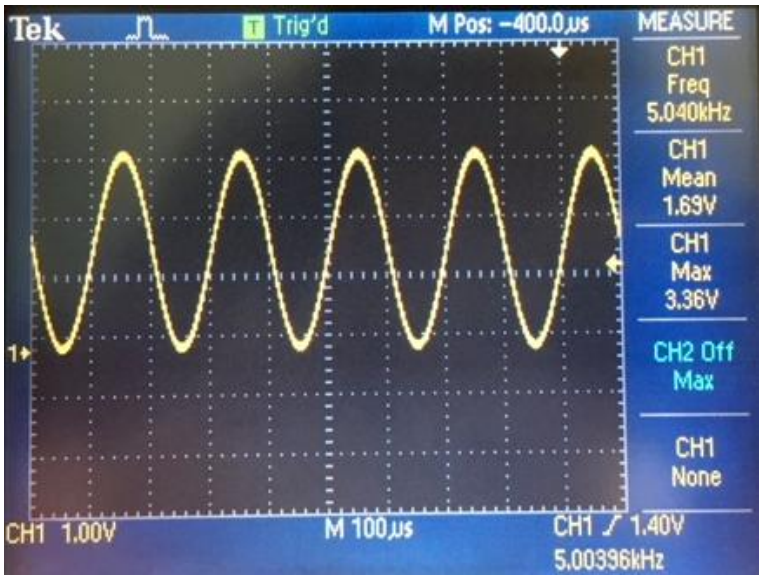
Software Setup

By default, the code example uses Component API function calls. Alternatively, the `PDL_CONFIGURATION` macro can be set to (1u) to demonstrate how to use the low-level PDL CTDAC function calls.

Operation

1. Plug the CY8CKIT-062 BLE kit into your computer's USB port.
2. Build the project and program it into the PSoC 6 MCU device. Choose **Debug** > **Program**. For more information on device programming, see PSoC Creator Help. Flash for both CPUs is programmed in a single program operation.
3. Connect an oscilloscope probe to pin P9[6] (on the J2 connector for the pioneer kit). With the oscilloscope properly configured, confirm that the signal is a 5-kHz sine wave with a 0–V_{DDA} voltage range.

Figure 2. VDAC Sine Wave Output

1. 

Components

Table 1 lists the PSoC Creator Components used in this example, the hardware resources used by each, and non-default settings.

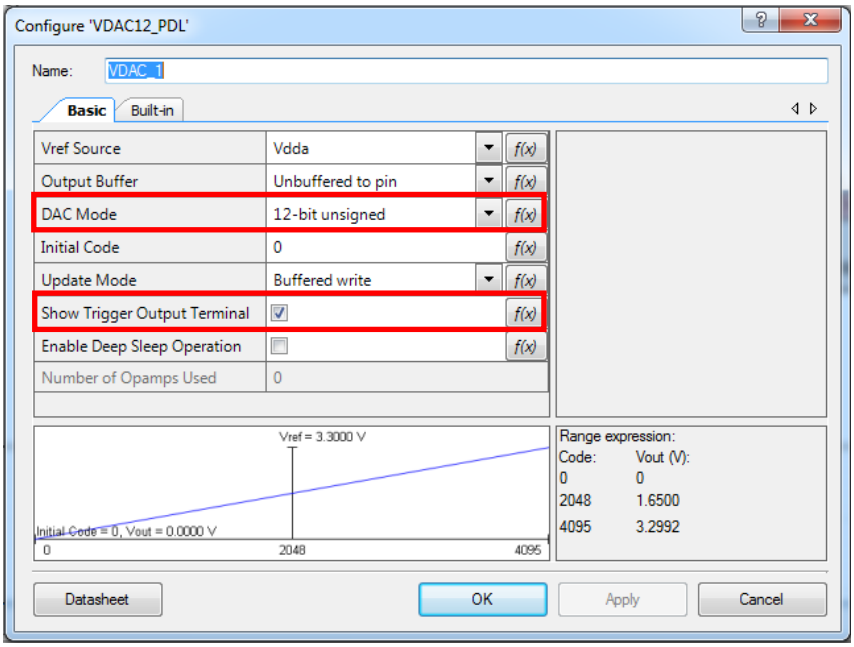
Table 1. PSoC Creator Components

Component	Instance Name	Hardware Resources
Voltage DAC (12-bit)	VDAC_1	1 Continuous time DAC
DMA	DMA_1	1 DMA channel
Clock	Clock_1	1 Peripheral clock divider
Analog Pin	VDAC_Out_P9_6	1 Analog output pin

Parameter Settings

Figure 3 through Figure 5 highlight the non-default settings for each Component in this example.

Figure 3. VDAC Component Parameter Settings



The values in the DMA lookup table are unsigned; therefore, the DAC mode for the VDAC is set to unsigned. Enable the trigger output terminal so that it can be connected to the DMA.

Figure 4. DMA Component Channel Parameter Settings

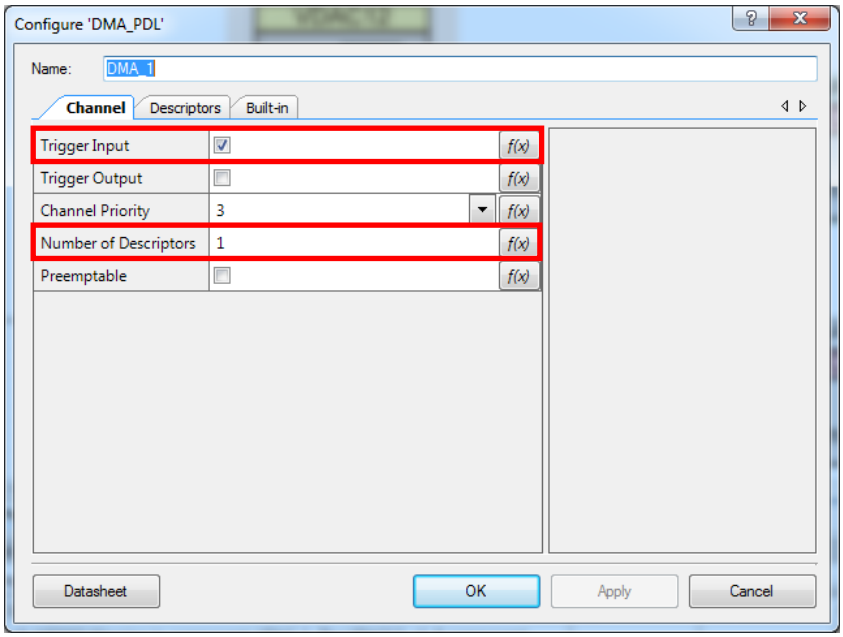
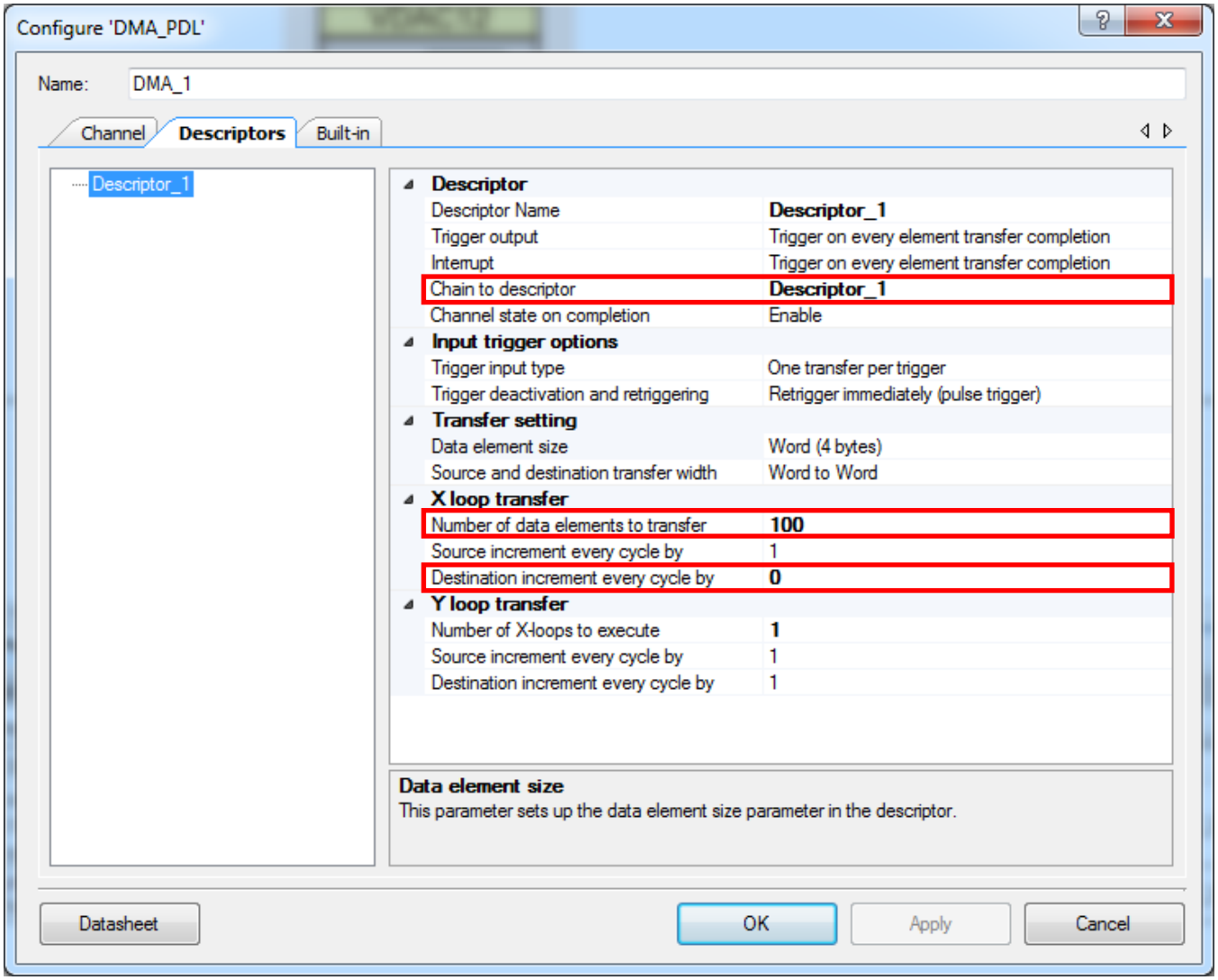


Figure 5. DMA Component Descriptors Parameter Settings



Chain Descriptor_1 to itself so that the sine wave output is continuous. The number of data elements to transfer is set to 100 to match the number of elements in the lookup table. The destination address (that of the VDAC buffered value register) will not change so the “Destination increment every cycle by” is set to 0.

Design-Wide Resources

Table 2 shows the pin assignment for the code example.

Table 2. Pin Names and Location

Pin Name	Pin Location
VDAC_Out_P9_6	P9[6]

Related Documents

Application Notes	
AN210781	Getting Started with PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity
PSoC Creator Component Datasheets	
VDAC12	Supports continuous-time DAC functions
Direct Memory Access	Supports data transfers to and from memory, components, and registers
General Purpose Input / Output (GPIO)	Supports all GPIO pin features
Device Documentation	
PSoC 6 MCU: PSoC 63 with BLE Datasheet	
PSoC 6 MCU: PSoC 63 with BLE Architecture Technical Reference Manual	
PSoC 6 MCU: PSoC 63 with BLE Register Technical Reference Manual	
PSoC 6 MCU: PSoC 62 Datasheet	
Development Kit (DVK) Documentation	
PSoC 6 MCU BLE Pioneer Kit	
PSoC 6 MCU WiFi BT Pioneer Kit	

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5947247	GJV	02/19/2018	New code example

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